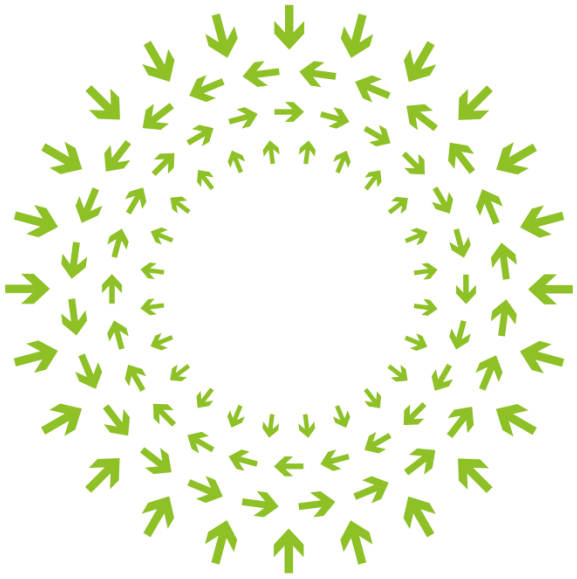

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Project Olympus Server Motherboard Specification

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Revision History

Date	Description
10/24/16	Version 1.0
2/27/17	Version 2.0 - Added Section 11.3 PCIe x32 connector definition - Section 11.9, Table 15 corrected Pin 18 definition - Section 11.10 Table 16 corrected pin 18 definition

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1 Project Olympus Specifications List

Table 1 lists the Project Olympus system specifications.

Table 1. List of Specifications

Specification title	Description
Project Olympus Server Rack Specification	Describes the mechanical rack hardware used in the system
Project Olympus Server Mechanical Specification	Describes the mechanical structure for the server used in the system.
Project Olympus Server Motherboard Specification	Describes the server motherboard general requirements.
Project Olympus PSU Specification	Describes the custom Power Supply Unit (PSU) used in the server
Project Olympus Power Management Distribution Unit Specification	Describes the Power Management Distribution Unit (PMDU).
Project Olympus Rack Manager Specification	Describes the Rack Manager PCBA used in the PMDU.

This document is intended for designers and engineers who will be building servers for Project Olympus systems.

2 Overview

This specification focuses on the Project Olympus Server Motherboard which is the computational element of the full-width Server.

Refer to respective specifications for other elements of the Project Olympus system such as Power Supply Unit (PSU), Rack Manager (RM), Power and Management Distribution Unit (PMDU), and Server Rack.

This specification covers block diagram, management sub-system, power management, FPGA Card support, IO connectors, and physical specifications of the Server Motherboard.

3 Background

To conceptualize how the server motherboard fits within server rack, consider the following.

The server motherboard is the computational element of the server. The motherboard includes a full server management solution and supports interfaces to integrated or rear-access 12V Power Supply Units (PSUs).

The Server optionally interfaces to a rack-level Power and Management Distribution Unit (PMDU).

The PMDU provides power to Server and interfaces to the Rack Manager (RM).

The motherboard design provides optimum front-cable access (cold aisle) for external IO such as networking and storage as well as standard PCIe cards. This enables flexibility to support many configurations.

4 Block Diagram

Figure 1 shows the baseline block diagram describing general requirements for the server motherboard.

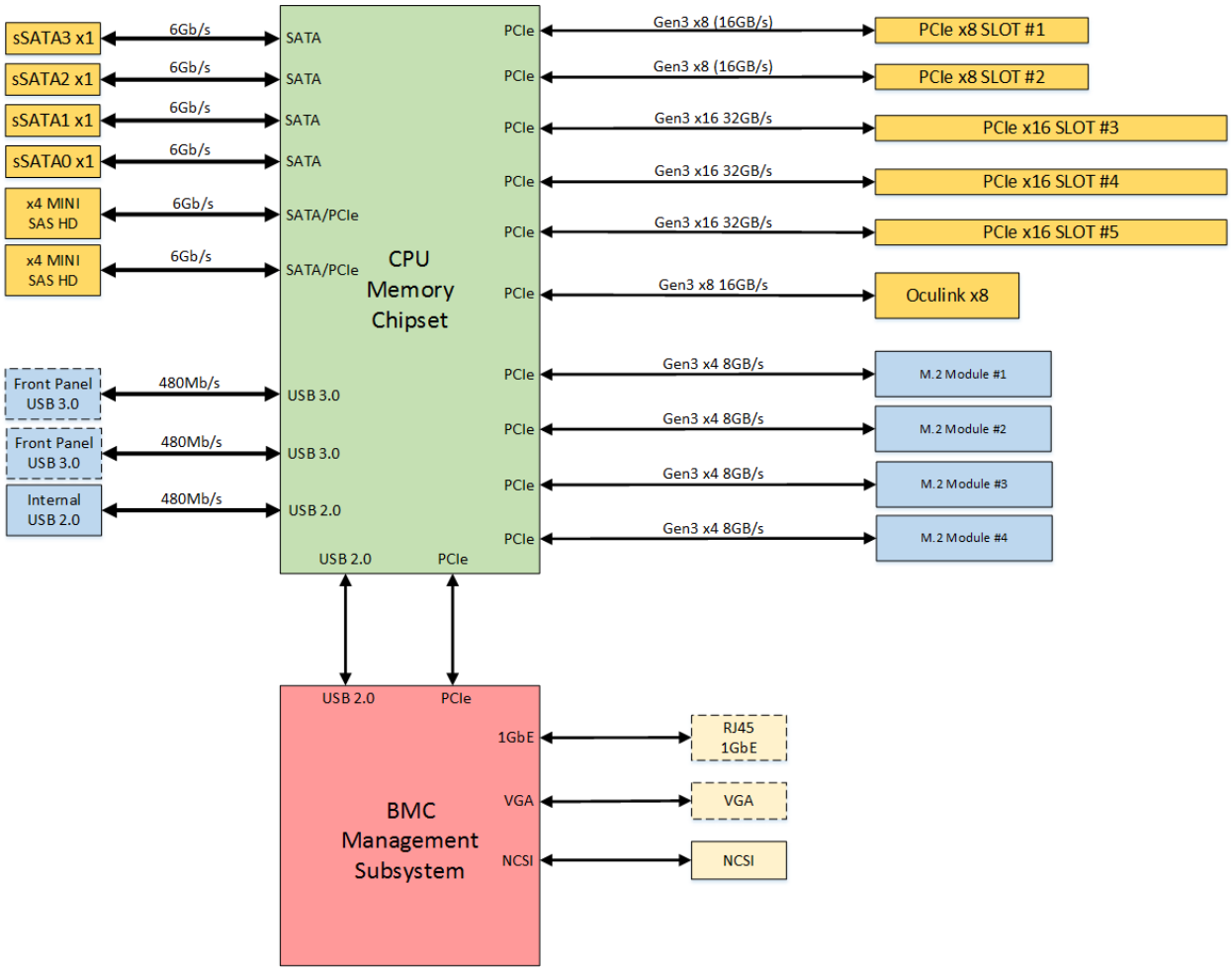


Figure 1. Top Level Block Diagram

Key features of the motherboard include:

- Support for up to 2 CPUs
- Support for up to 32 DIMMs
- Support for up to 12 SATA devices
- Support for up to 3 FHHL PCIe x16 slots
- Support for x8 PCIe cabling (OCuLink)
- Support for up to two PCIe x8 slots each capable of supporting up to two M.2 modules through an interposer board
- Support for up to four M.2 modules via direct-attach to motherboard
- Support for Server Management (AST2500 or equivalent)
- Support for integrated or rear managed PSU(s)
- Support for secure, signed boot
- Support for service and debugging

5 Motherboard Layout

Figure 2 shows an example layout and the approximate location of critical components and connectors. The top of the diagram represents the location of the cold aisle.

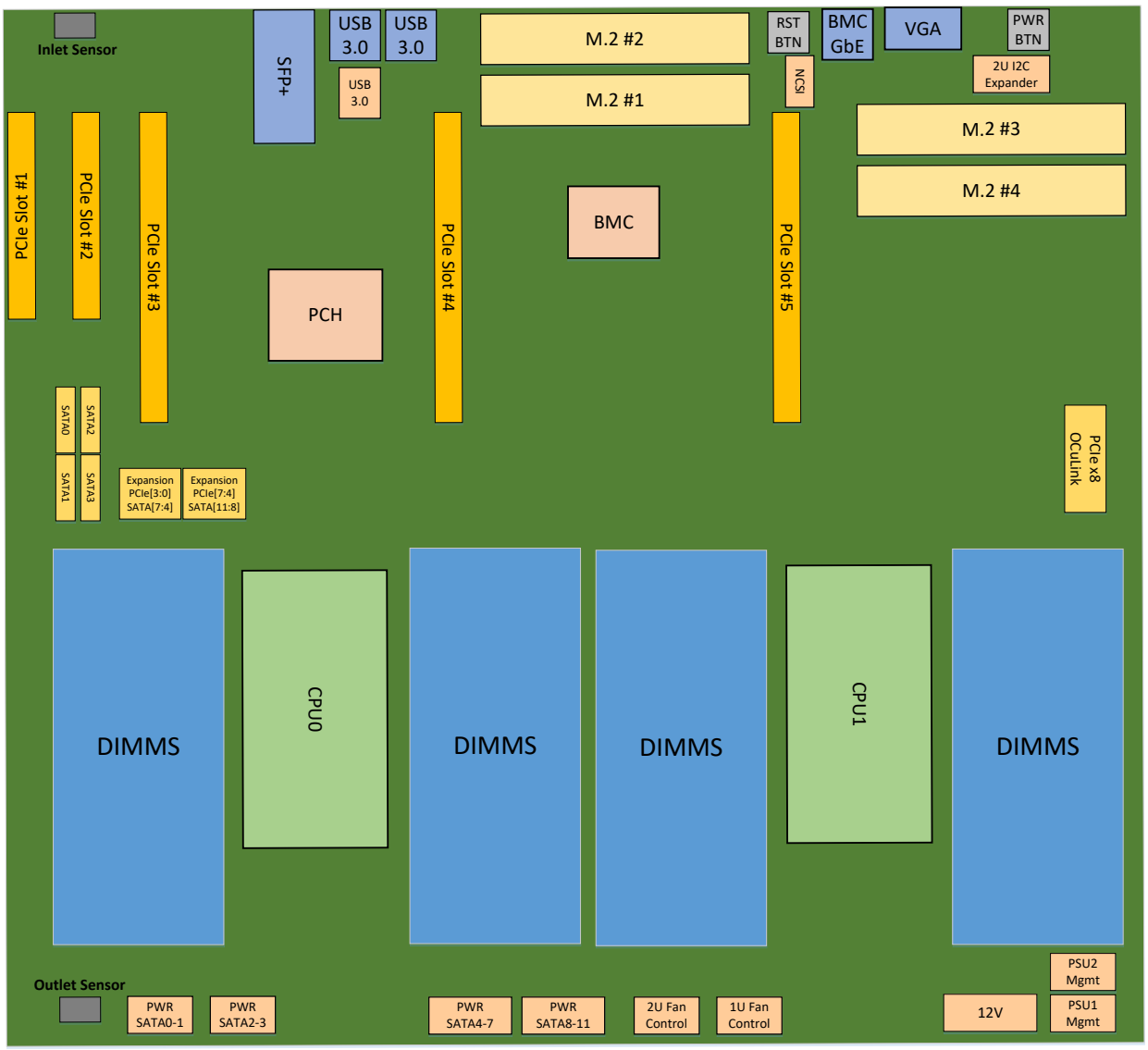


Figure 2. Motherboard Layout

6 Management Subsystem

The Baseboard Management Controller circuitry (BMC) for the Motherboard uses the ASPEED AST2500 or equivalent. This section describes the requirements for management of the motherboard. Primary features include.

- BMC - ASPEED AST2500 (or equivalent)
- BMC dedicated 1GbE LAN for communication with Rack Manager
- Low pin count (LPC) or equivalent connection to the chipset to support in-band management
- Out of band environmental controls for power and thermal management
- FRUID EEPROM for storage of manufacturing data and events (I^2C)
- Thermal sensors for inlet and exhaust temperature monitoring (I^2C)
- Power monitoring through the 12V Hot Swap Controller circuitry (I^2C)
- Service LEDs

Figure 3 shows the management block diagram.

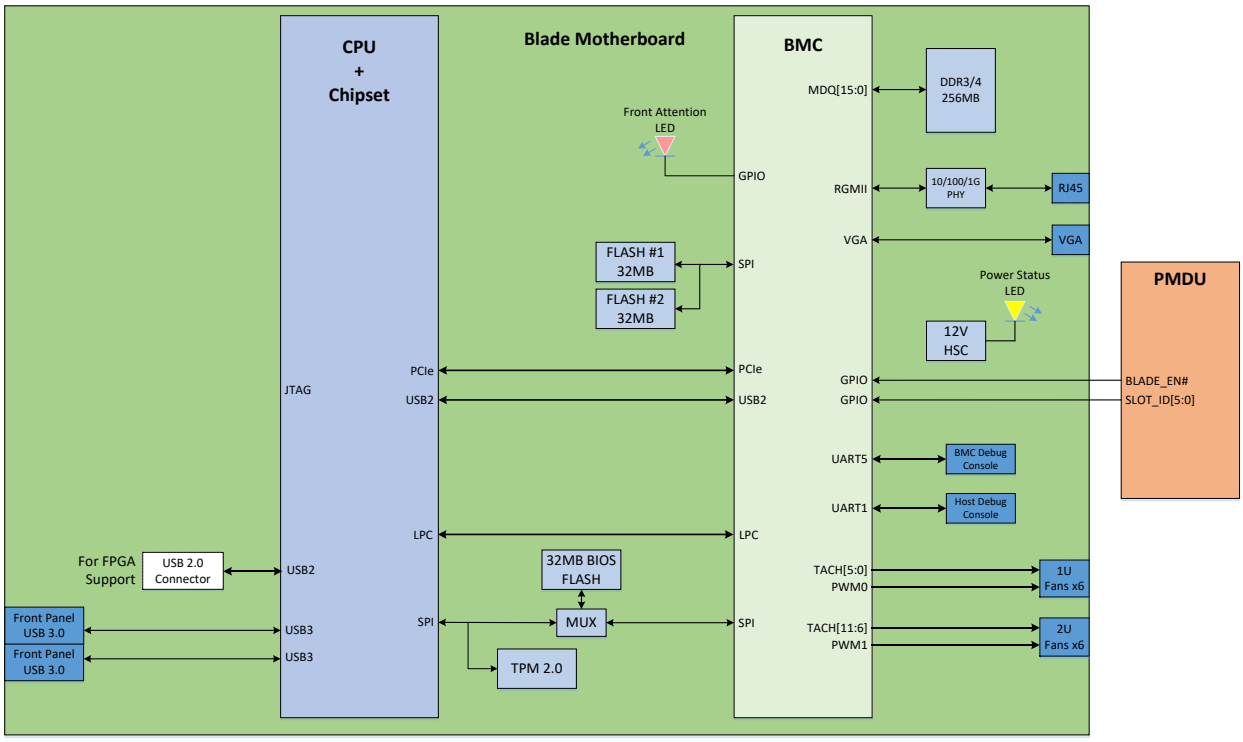


Figure 3. Management Block Diagram

6.1 BMC

The design for the BMC is based on the Aspeed 2500 family. Primary features include:

- Embedded ARM Processor
- Minimum 256MiB of DDR3/4 memory
- Redundant NOR/NAND/SPI flash memory

- I^2C /SMBus
- UART
- LPC Bus Interface
- Over 200 GPIO pins

6.1.1 DRAM

The BMC shall support a minimum of 256MiB of DDR3/4 memory.

6.1.2 BMC Boot Flash

The BMC boots from a flash memory device located on the SPI bus. The device size shall be 256Mb (32MiB) minimum and shall also be used to store FPGA and CPLD recovery images. Recommend using Windbond W25Q256 or equivalent. A secondary device shall be supported to provide BMC recovery. The design shall support a socket for the primary device during preproduction. It is not required to support a socket for the secondary device.

6.1.3 BIOS Flash

The BIOS utilizes one 256Mb (32MiB) Flash BIOS device located on the chipset SPI bus. The device shall be Windbond MPN W25Q256 or equivalent. The BIOS shall be recoverable from the BMC in the event the chipset is inaccessible.

6.1.4 1GbE PHY

The server is managed through a 1GbE PHY connected to the BMC. An RJ45 connector located at the front of the server provides 1GbE connectivity to an external management switch. The PHY shall be Broadcom BCM54612E or equivalent.

6.2 CPU Thermal Monitoring

The BMC shall support a mechanism to query CPU, Memory, and server thermal information to provide optimized fan speed control.

6.3 I^2C

To optimize telemetry gathering for power and thermal management as well as general management of the server assembly, the following functions shall support I^2C access from the BMC.

- All PCIe slots
- All M.2 modules
- Local hot swap controllers
- Power Supplies
- Key voltage regulators (processors and memory)

- Temperature sensors
- FRUID PROM

An example block diagram is shown in Figure 4. Care should be taken to electrically isolate components that are powered from separate power domains, but are located on the same I^2C bus. Note that addresses shown are 8-bit address with the R/W bit as the LSB set to 0 (0xA8=1010100x).

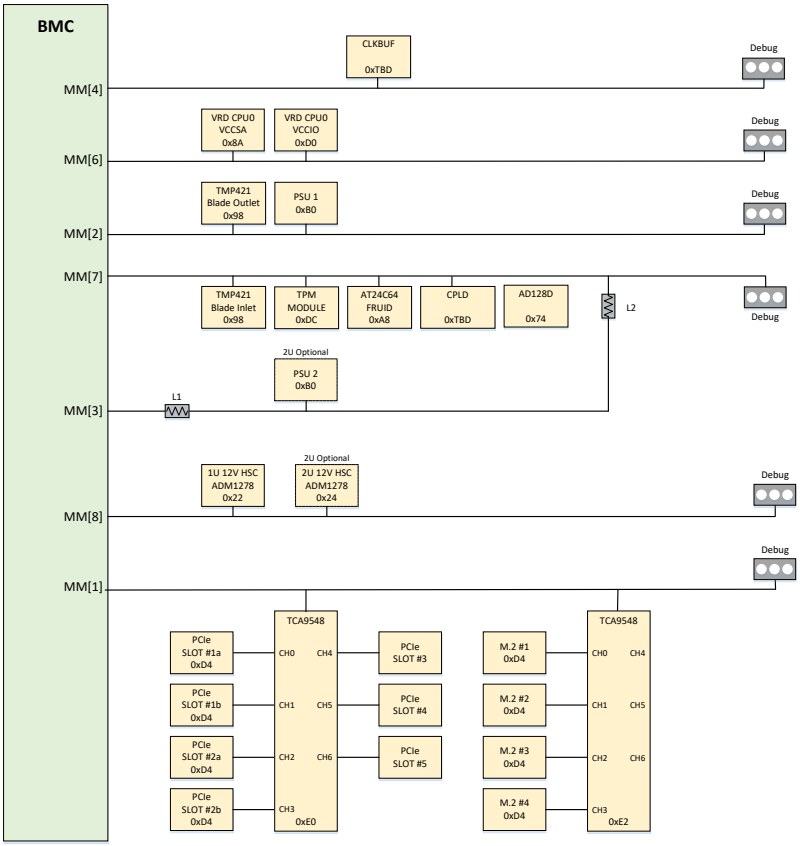


Figure 4. I^2C Block Diagram

6.4 UART

The motherboard shall support two UART headers connected to the BMC for console and debug.

6.5 JTAG Master

The motherboard shall support JTAG programming of programmable logic devices using the BMC's JTAG master controller. The JTAG programming shall be supported to any required CPLDs and a primary PCIe slot designated for FPGA Cards. The board shall contain mux circuitry controlled by the BMC to switch between the two programming paths. A block diagram is shown in Figure 5.

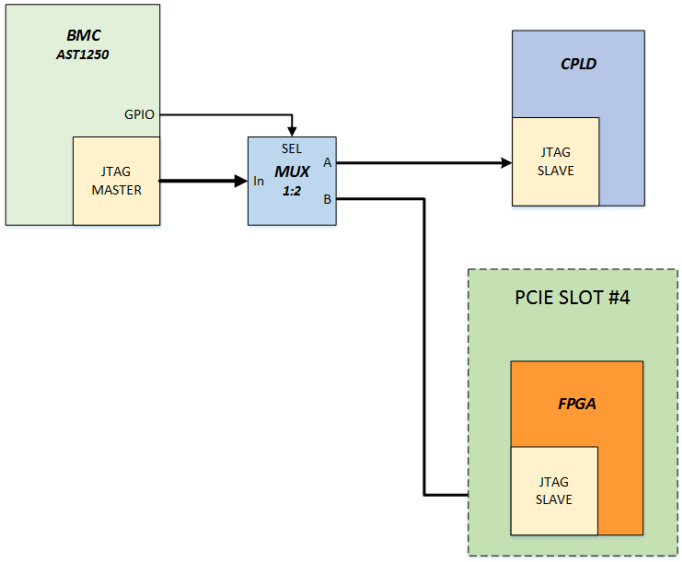


Figure 5. JTAG Programming

6.6 Jumpers

The design shall include appropriate debug jumpers. Recommended jumpers are listed in Table 2. Actual requirements will vary depending on server architecture.

Table 2. Jumpers

Jumper Name	Default Position	Detected By	Function
BMC Disable (default)	High (not installed)	BMC	Disables BMC (sets all pins to High impedance)
BIOS USB Recovery	Low (2,3 short)	BIOS	Enables BIOS recovery via USB image update
BIOS A18 Top Swap	High (1,2 short)	BIOS	Swaps BIOS image by booting from other half of BIOS Flash
Clear CMOS	HIGH (1,2 short)	BIOS	Clears CMOS
Password Clear	High (1,2 short)	BIOS	Clears the password
Manufacturing Mode	Low (not installed)	BIOS	Not supported, used in HVM, placeholder

6.7 Voltage Regulators

Voltage regulators that support I^2C or PMBus should be available to the BMC. This includes CPU and Memory subsystem regulators at a minimum Clock Generators and Buffers

Clock circuitry that supports I^2C should be available to the BMC. Figure 4 above shows generic clock devices. The actual implementation may vary.

6.8 FRUID PROM

The Motherboard shall include a 64Kb serial EEPROM MPN AT24C64 or equivalent for storing manufacturing data.

6.9 Temperature Sensors

The Motherboard shall include I^2C support for a minimum of two temperature sensors, MPN TMP411 or equivalent, for monitoring the inlet and outlet air temperatures of the motherboard. The motherboard shall include provisions to support temperature monitoring of all DIMMs (SPD) and all PCIe slots including M.2s. For accurate temperature reading, care shall be taken to not place these temperature sensors close to component or board heat sources.

6.10 Hot Swap Controllers

The Motherboard shall include I^2C support for two hot swap controllers for power monitoring and power-capping. One controller is located in the 1U space of the motherboard. The other controller is optional and is located in the 2U space accessible to the motherboard by a cable.

6.11 LEDs

The following sections describe the light-emitting diodes (LEDs) used as indicators on the motherboard. Table 3 lists the minimum LEDs required and provides a brief description. Greater detail for some LEDs is included in subsequent sections below. The visible diameter, color (λ) and brightness requirements of the LEDs are TBD. All LEDs shall be visible at the front of the motherboard (cold aisle).

Table 3. LEDs

LED Name	Color	Description
UID LED	Blue	Unit Identification LED
Attention LED	Red	Indicates that Server requires servicing
Power Status LED	Amber/Green	Indicates Power Status of the Server
SATA HDD Activity	Green	Indicates R/W activity to HDDs
Post Code	Green	Indicates the Boot status of the Server (Port 80)
Catastrophic Error	Red	Indicates that a CPU catastrophic error has occurred
BMC Heartbeat	Green	Blinks to indicate BMC is alive
GbE Port 0 Activity	Green	Indicates activity on 10GbE Port 0 (not supported for production)
GbE Port 0 Speed	Green/Orange	Green=high speed, Orange=Low speed (not supported for production)
PSU1 Status LED1 (P2010)	Green	Status LED for PSU1 • Solid Green = AC and DC Power Good • Blinking Green = Battery Power Good
PSU1 Status LED2 (P2010)	Amber	Status LED for PSU1 • Solid Amber = Failure of PSU Phase • Blinking Amber = Failure of 2 PSU Phases
PSU2 Status LED1 (P2010)	Green	Status LED for PSU2 (optional) • Solid Green = AC and DC Power Good

		• Blinking Green = Battery Power Good
PSU2 Status LED2 (P2010)		Status LED for PSU2 (optional) • Solid Amber = Failure of PSU Phase • Blinking Amber = Failure of 2 PSU Phases

6.11.1 UID LED

The motherboard shall support a blue UID (unit ID) LED used to help visually locate a specific server within a datacenter.

6.11.2 Power Status LED

When a server is initially inserted, the Power Status LED shall turn amber if 12V is present at the output of the Hot Swap Controller. This assures that the 12V power is connected and present at the motherboard and that the Hot-swap Controller (HSC) is enabled.

When the server management software turns on the system power (CPU/Memory/PCIe), the Power Status LED turns green. Note that the power status LED may be driven by an analog resistor network tied directly to a power rail, and is not an indication of the health of the server. Table 4 describes the operation of the Power Status LED.

Table 4. Power Status LED Description

LED status	Condition
Off	12V power is absent or PWR_EN# is de-asserted
Solid Amber ON	PWR_EN# is asserted and 12V power output of the Hot Swap Controller is present.
Solid Green ON	Indicates that the management (BMC or IE) is booted and system power is enabled (CPU/Memory/PCIe).

6.11.3 Attention LED

The Attention LED directs the service technicians to the server that requires service. When possible, server diagnostics are used to direct repairs. Alternately, the Microsoft scale-out management software can be used. In both cases, event logs of the repair work are available.

The LED is driven by a single BMC GPIO. Table 5 describes the operation of the Attention LED.

Table 5. Attention LED Description

LED status	Condition
Off	No attention indicated
Solid RED	System needs attention

6.11.4 PSU Status LEDs (Optional)

The server may optionally support 4 PSU status LEDs (2 per PSU). Each PSU is comprised of 2 individual status LEDs indicating the PSU status as shown in Table 3. These LEDs support the WCS P2010 PSU. Standard PSUs may not support external LEDs.

6.12 Fan Control

The motherboard shall support control of twelve 40mm fans located at the rear of the server assembly. Fan control is divided between two connectors enabling two separate fan zones. Each connector supports 12V power, a single PWM, and six TACH signals for controlling up to 6 fans in a single zone.

7 Power Management

The motherboard shall provide a rear connector for interfacing the motherboard to a 12V PSU. The motherboard shall also provide a rear management connector for enabling external control of server power. A block diagram of the interface is shown Figure 6.

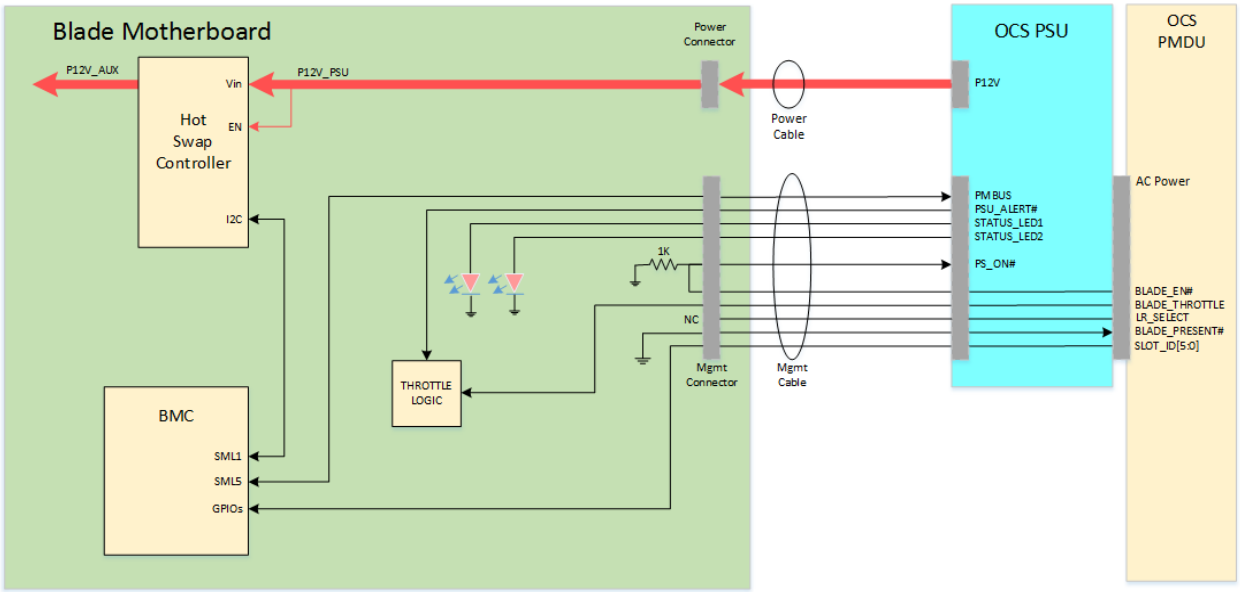


Figure 6. Power Management Block Diagram

7.1 Rack Management

The Rack Manager communicates with the server motherboard through the PMDU. The following describes the management interfaces.

- PWR_EN# - Active low signal used to enable/disable power to the P2010 PSU. A 1K ohm pulldown resistor is used on the motherboard to ensure a default low state (active) if the Rack Manager is not present. This signal connects to the PS_ON# signal of the PSU. When in high state (inactive), this signal disables output power from the P2010 PSU.
- SERVER_PRESENT# - Active low signal used to communicate physical presence of the server to the Rack Manager. This signal should be tied to GND on the motherboard.
- SERVER_THROTTLE - Active high signal used to put the motherboard into a low power (power cap) state. This signal should default low (inactive) if the Rack Manager is not present. This signal is fanned out from the Rack Manager to multiple servers and therefore the circuit design must support electrical isolation of this signal from the motherboard power planes.
- SLOT_ID[5:0] – Identifies the physical rack slot in which the server is installed. ID is hard set by the PMDU. The ID decoding is shown below in Table 6.
- LR_SELECT – Spare signal. Used to differentiate between left and right slots for a dual-node implementation.

Table 6. Slot ID Decode

Slot	SLOT_ID[5:0]	Slot	SLOT_ID[5:0]
Slot 1	000000	Slot 25	100000
Slot 2	000001	Slot 26	100001
Slot 3	000010	Slot 27	100010
Slot 4	000011	Slot 28	100011
Slot 5	000100	Slot 29	100100
Slot 6	000101	Slot 30	100101
Slot 7	001000	Slot 31	101000
Slot 8	001001	Slot 32	101001
Slot 9	001010	Slot 33	101010
Slot 10	001011	Slot 34	101011
Slot 11	001100	Slot 35	101100
Slot 12	001101	Slot 36	101101
Slot 13	010000	Slot 37	110000
Slot 14	010001	Slot 38	110001
Slot 15	010010	Slot 39	110010
Slot 16	010011	Slot 40	110011
Slot 17	010100	Slot 41	110100
Slot 18	010101	Slot 42	110101
Slot 19	011000	Slot 43	111000
Slot 20	011001	Slot 44	111001
Slot 21	011010	Slot 45	111010
Slot 22	011011	Slot 46	111011
Slot 23	011100	Slot 47	111100
Slot 24	011101	Slot 48	111101

7.2 PSU Management

The motherboard shall support management of the P2010 PSU. Below is a description of the signals supported by the PMDU.

- PS_ON# - Active low signal used to enable/disable power to the PSU. This signal is driven by the PWR_EN# signal from the Rack Manager. A 1K ohm pulldown resistor is used on the motherboard to ensure a default low state if the RM is not present.
- PSU_ALERT# - Active low signal used to alert the motherboard that a fault has occurred in the PSU. Assertion of this signal by the PSU shall put the motherboard into a low power (PROCHOT) state. This signal is also connected to the BMC for monitoring of PSU status.
- PMBUS – I^2C interface to the PSU. The BMC uses this signal is used by the BMC to read the status of the PSU.
- STATUS_LED – Controls LED to provide visual indication of a PSU fault.

7.3 Hot Swap Controller

The motherboard shall support a hot swap controller (HSC) for in-rush current protection. The HSC shall include support for the PMBUS interface. Recommend using the ADM1278 or equivalent.

7.4 Power Capping

The motherboard shall enable power capping of the server from different trigger sources. Each of these triggers can be disabled by the BMC. BMC should be able to trigger these events for debugging.

- SERVER_THROTTLE - Throttle signal driven by the Rack Manager.
- PSU_ALERT# - Alert signal driven by the PSU. The PSU will be programmed to assert ALERT# in the event the PSU transitions its power source from AC to battery backup.
- FM_THROTTLE# - Test signal that allows BMC to assert power cap

7.5 Overcurrent Protection

The hot swap controller (HSC) is responsible for detecting a current level that indicates a catastrophic failure of the server. In this event, the HSC should disable 12V to the motherboard typically by disabling the HSC's input FETS.

7.6 M.2 Support

The motherboard shall support M.2 devices with x4 PCIe Gen-3 interfaces (M.2 connector with M Key). These cards can be supported through any of the following methods:

- Standard M.2 connector mounted directly on the motherboard.
- Dual M.2 Interposer Module. PCIe x8 interface described in Section 11.1.
- Quad M.2 Carrier Card. FHHL PCIe Card in standard PCIe format.

For both motherboard and PCIe Card applications, the supported M.2 modules supported are 60mm, 80mm, and 110mm form factors (Type 2260, 2280, and 22110).

7.7 Service Requirements

7.7.1 USB Service Port

The motherboard shall provide two USB 3.0 Type A connectors at the front of the server to enable cold aisle servicing.

7.7.2 LED Visibility

Motherboard LEDs determined to be important for communicating status to service personnel shall be made visible at the front (cold aisle) of the server. This should shall include the following LEDs at a minimum.

- UID LED
- Power Status LED
- Attention LED

8 NVDIMM

The motherboard shall include support for DDR4 NVDIMM with 12V power through the DIMM connector.

9 TPM Module

The Motherboard shall include a connector to support a TPM 2.0 module connected to the PCH chipset SPI bus.

10 FPGA Card Support

The motherboard shall support a Full Height Half Length (FHHL) x16 PCIe form factor FPGA Card. The card installs in a standard PCIe x16 slot. The motherboard shall include a x8 OCuLink connector for

cabling an additional x8 PCIe Link from the motherboard to the FPGA card as well as an internal USB connector to support FPGA debug.

11 Motherboard Interfaces

This section describes the connector interfaces to the motherboard.

11.1 PCIe x8 Connectors

All standard PCIe x8 connectors on the motherboard shall support the dual M.2 riser card. The interface is designed to support a standard PCIe x8 card as well as the M.2 Interposer Module. The M.2 Interposer Module is a custom edge card PCA that supports two M.2 SSD Modules (NGFF form factor cards) in the connectorized SSD Socket 3 format per the PCI Express M.2 Specification. To support two M.2 modules, the PCIe connector interface is altered to support two x4 PCIe Gen3 interfaces as well as the SSD specific signals per the PCIE M.2 specification. Table 7 describes the connector pinout. Signals shall satisfy the electrical requirements of the PCIe Card Electromechanical Specification. The following is a list of pin assignment deviations from that specification needed to support two M.2 modules.

- SUSCLK is assigned to pin A6 replacing JTAG TDI pin. Support for SUSCLK is not required.
- LINKWIDTH is assigned to pin A17 replacing PRSNT#2. Enables auto-detection of 2x4 M.2 Interposer or 1x8 standard PCIe card. The design is not required to support PCIe x1 cards.
- REFCLK2+/- is assigned to pins A32/A33 replacing two Reserved pins.
- SMBCLK2 and SMBDAT2 are assigned to pins A6/A7 replacing TDO and TMS pins.

Table 7. PCIe x8 connector pinout

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK1	SMBus clock	JTAG2	TCK
6	SMDAT1	SMBus data	SUSCLK	Suspend Clk
7	GND	Ground	SMCLK2	SMBus clock
8	+3.3v	+3.3 volt power	SMDAT2	SMBus data
9	JTAG1	+TRST#	+3.3v	+3.3 volt power

10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PGOOD	Powergood
Mechanical Key				
12	CLKREQ#	Request Running Clock	GND	Ground
13	GND	Ground	REFCLK1+	Reference Clock
14	PETP(0)	Transmitter Lane 0,	REFCLK1-	Differential pair
15	PETN(0)	Differential pair	GND	Ground
16	GND	Ground	PERP(0)	Receiver Lane 0,
17	LINKWIDTH	0= 2 x4 1= 1 x8	PERN(0)	Differential pair
18	GND	Ground	GND	Ground
19	PETP(1)	Transmitter Lane 1,	RSVD	Reserved
20	PETN(1)	Differential pair	GND	Ground
21	GND	Ground	PERP(1)	Receiver Lane 1,
22	GND	Ground	PERN(1)	Differential pair
23	PETP(2)	Transmitter Lane 2,	GND	Ground
24	PETN(2)	Differential pair	GND	Ground
25	GND	Ground	PERP(2)	Receiver Lane 2,
26	GND	Ground	PERN(2)	Differential pair
27	PETP(3)	Transmitter Lane 3,	GND	Ground
28	PETN(3)	Differential pair	GND	Ground
29	GND	Ground	PERP(3)	Receiver Lane 3,
30	RSVD	Reserved	PERN(3)	Differential pair
31	PRSNT#2	Presence Detect	GND	Ground
32	GND	Ground	REFCLK2+	Reference Clock
33	PETP(4)	Transmitter Lane 4,	REFCLK2-	Differential pair
34	PETN(4)	Differential pair	GND	Ground
35	GND	Ground	PERP(4)	Receiver Lane 4,
36	GND	Ground	PERN(4)	Differential pair
37	PETP(5)	Transmitter Lane 5,	GND	Ground
38	PETN(5)	Differential pair	GND	Ground
39	GND	Ground	PERP(5)	Receiver Lane 5,
40	GND	Ground	PERN(5)	Differential pair
41	PETP(6)	Transmitter Lane 6,	GND	Ground
42	PETN(6)	Differential pair	GND	Ground
43	GND	Ground	PERP(6)	Receiver Lane 6,

44	GND	Ground	PERN(6)	Differential pair
45	PETP(7)	Transmitter Lane 7,	GND	Ground
46	PETN(7)	Differential pair	GND	Ground
47	GND	Ground	PERP(7)	Receiver Lane 7,
48	PRSNT#2	Presence detect	PERN(7)	Differential pair
49	GND	Ground	GND	Ground

11.2 PCIe x16 Connectors

The PCIe x16 connector interface is designed to support a standard PCIe x16 full-height card. The pinout for supporting PCIe x16 described in Table 8. This interface also supports the PWRBRK# power reduction feature. Note that this signal is declared on pins B12 and B30. This enables support for the feature on existing platforms (B12) and meets the latest PCI SIG definition (B30). For further information, refer to the PCI Express® Card Electromechanical Specification.

Table 8. PCIe x16 connector pinout

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	PWRBRK#	Power Reduction	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock
14	PETP(0)	Transmitter Lane 0,	REFCLK-	Differential pair
15	PETN(0)	Differential pair	GND	Ground
16	GND	Ground	PERP(0)	Receiver Lane 0,
17	PRSNT#2	Presence detect	PERN(0)	Differential pair
18	GND	Ground	GND	Ground

19	PETP(1)	Transmitter Lane 1,	RSVD	Reserved
20	PETN(1)	Differential pair	GND	Ground
21	GND	Ground	PERP(1)	Receiver Lane 1,
22	GND	Ground	PERN(1)	Differential pair
23	PETP(2)	Transmitter Lane 2,	GND	Ground
24	PETN(2)	Differential pair	GND	Ground
25	GND	Ground	PERP(2)	Receiver Lane 2,
26	GND	Ground	PERN(2)	Differential pair
27	PETP(3)	Transmitter Lane 3,	GND	Ground
28	PETN(3)	Differential pair	GND	Ground
29	GND	Ground	PERP(3)	Receiver Lane 3,
30	PWRBRK#	Power Reduction	PERN(3)	Differential pair
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETP(4)	Transmitter Lane 4,	RSVD	Reserved
34	PETN(4)	Differential pair	GND	Ground
35	GND	Ground	PERP(4)	Receiver Lane 4,
36	GND	Ground	PERN(4)	Differential pair
37	PETP(5)	Transmitter Lane 5,	GND	Ground
38	PETN(5)	Differential pair	GND	Ground
39	GND	Ground	PERP(5)	Receiver Lane 5,
40	GND	Ground	PERN(5)	Differential pair
41	PETP(6)	Transmitter Lane 6,	GND	Ground
42	PETN(6)	Differential pair	GND	Ground
43	GND	Ground	PERP(6)	Receiver Lane 6,
44	GND	Ground	PERN(6)	Differential pair
45	PETP(7)	Transmitter Lane 7,	GND	Ground
46	PETN(7)	Differential pair	GND	Ground
47	GND	Ground	PERP(7)	Receiver Lane 7,
48	PRSNT#2	Hot plug detect	PERN(7)	Differential pair
49	GND	Ground	GND	Ground
50	PETP(8)	Transmitter Lane 8,	RSVD	Reserved
51	PETN(8)	Differential pair	GND	Ground
52	GND	Ground	PERP(8)	Receiver Lane 8,
53	GND	Ground	PERN(8)	Differential pair
54	PETP(9)	Transmitter Lane 9,	GND	Ground

55	PETN(9)	Differential pair	GND	Ground
56	GND	Ground	PERP(9)	Receiver Lane 9,
57	GND	Ground	PERN(9)	Differential pair
58	PETP(10)	Transmitter Lane 10,	GND	Ground
59	PETN(10)	Differential pair	GND	Ground
60	GND	Ground	PERP(10)	Receiver Lane 10,
61	GND	Ground	PERN(10)	Differential pair
62	PETP(11)	Transmitter Lane 11,	GND	Ground
63	PETN(11)	Differential pair	GND	Ground
64	GND	Ground	PERP(11)	Receiver Lane 11,
65	GND	Ground	PERN(11)	Differential pair
66	PETP(12)	Transmitter Lane 12,	GND	Ground
67	PETN(12)	Differential pair	GND	Ground
68	GND	Ground	PERP(12)	Receiver Lane 12,
69	GND	Ground	PERN(12)	Differential pair
70	PETP(13)	Transmitter Lane 13,	GND	Ground
71	PETN(13)	Differential pair	GND	Ground
72	GND	Ground	PERP(13)	Receiver Lane 13,
73	GND	Ground	PERN(13)	Differential pair
74	PETP(14)	Transmitter Lane 14,	GND	Ground
75	PETN(14)	Differential pair	GND	Ground
76	GND	Ground	PERP(14)	Receiver Lane 14,
77	GND	Ground	PERN(14)	Differential pair
78	PETP(15)	Transmitter Lane 15,	GND	Ground
79	PETN(15)	Differential pair	GND	Ground
80	GND	Ground	PERP(15)	Receiver Lane 15,
81	PRSNT#2	Hot plug present detect	PERN(15)	Differential pair
82	RSVD#2	Hot Plug Detect	GND	Ground

11.3 PCIe x32 Connector

The PCIe x32 connector interface is designed to support a PCIe x32 full-height card. Use of PCIe x32 is optional for the front I/O slot, and is primarily intended as a future growth targeting slot #4. The interface is comprised of two Samtec HSEC8 connectors: 200 pin MPN DFHSK0FS015 and 60 pin MPN DFHS60FS042. The pinouts for the 200 pin and 60 pin connectors are shown in Table 9 and Table 10 respectively. Key features for this interface includes:

- Supports two PCIe x16 interfaces
- Supports auto-bifurcation (Config ID)
- Supports up to 6 PCIe Clocks
- Supports two SMBus interfaces
- Supports JTAG Interface
- Supports USB 2.0 Interface

Table 9. PCIe x32 Connector Pinout - 200 Pin

Pin	Side A Connector		Side B Connector		Pin
#	Name	Description	Name	Description	#
1	P12V	+12 volt power	P12V	+12 volt power	2
3	P12V	+12 volt power	P12V	+12 volt power	4
5	P12V	+12 volt power	P12V	+12 volt power	6
7	P12V	+12 volt power	P12V	+12 volt power	8
9	P12V	+12 volt power	P12V	+12 volt power	10
11	P12V	+12 volt power	P12V	+12 volt power	12
13	GND	Ground	GND	Ground	14
15	BMC_SMBDAT	SMBus to BMC	BMC_ALERT#	SMBus Alert to BMC	16
17	BMC_SMCLK	SMBus to BMC	SLT_CFG1	Slot Configuration Bit1	18
19	SLT_CFG0	Slot Configuration Bit0	PWRBREAK#	Power Break	20
21	P3V3	+3.3 volt power	P3V3	+3.3 volt power	22
23	P3V3	+3.3 volt power	P3V3	+3.3 volt power	24
25	P3V3_STBY	+3.3 volt stby power	GND	Ground	26
27	PCH_ALERT#	SMBus Alert to PCH	WAKE#	Wake	28
29	PERST#	PCIe Reset	PCH_SMDAT	SMBus to PCH	30
31	GND	Ground	PCH_SMCLK	SMBus to PCH	32
33	CLK_100M_DP<0>	Reference Clock	GND	Ground	34
35	CLK_100M_DN<0>	Differential pair	CLK_100M_DP<1>	Reference Clock	36
37	GND	Ground	CLK_100M_DN<1>	Differential pair	38
39	CLK_100M_DP<2>	Reference Clock	GND	Ground	40
41	CLK_100M_DN<2>	Differential pair	CLK_100M_DP<3>	Reference Clock	42
43	GND	Ground	CLK_100M_DN<3>	Differential pair	44
45	CLK_100M_DP<4>	Reference Clock	GND	Ground	46
47	CLK_100M_DN<4>	Differential pair	CLK_100M_DP<5>	Reference Clock	48
49	GND	Ground	CLK_100M_DN<5>	Differential pair	50
51	P3E_P0_TXP<15>	Transmitter Lane 15,	GND	Ground	52
53	P3E_P0_TXN<15>	Differential pair	P3E_P0_RXP<15>	Receiver Lane 15,	54
55	GND	Ground	P3E_P0_RXN<15>	Differential pair	56
57	P3E_P0_TXP<14>	Transmitter Lane 14,	GND	Ground	58
59	P3E_P0_TXN<14>	Differential pair	P3E_P0_RXN<14>	Receiver Lane 14,	60
61	GND	Ground	P3E_P0_RXP<14>	Differential pair	62
63	RSVD1	Reserved	GND	Ground	64

65	GND	Ground	RSVD2	Reserved	66
67	P3E_P0_TXN<13>	Transmitter Lane 13,	GND	Ground	68
69	P3E_P0_TXP<13>	Differential pair	P3E_P0_RXP<13>	Receiver Lane 13,	70
71	GND	Ground	P3E_P0_RXN<13>	Differential pair	72
73	P3E_P0_TXN<12>	Transmitter Lane 12,	GND	Ground	74
75	P3E_P0_TXP<12>	Differential pair	P3E_P0_RXP<12>	Receiver Lane 12,	76
77	GND	Ground	P3E_P0_RXN<12>	Differential pair	78
79	P3E_P0_TXN<11>	Transmitter Lane 11,	GND	Ground	80
81	P3E_P0_TXP<11>	Differential pair	P3E_P0_RXP<11>	Receiver Lane 11,	82
83	GND	Ground	P3E_P0_RXN<11>	Differential pair	84
85	P3E_P0_TXN<10>	Transmitter Lane 10,	GND	Ground	86
87	P3E_P0_TXP<10>	Differential pair	P3E_P0_RXP<10>	Receiver Lane 10,	88
89	GND	Ground	P3E_P0_RXN<10>	Differential pair	90
91	P3E_P0_TXP<9>	Transmitter Lane 9,	GND	Ground	92
93	P3E_P0_TXN<9>	Differential pair	P3E_P0_RXP<9>	Receiver Lane 9,	94
95	GND	Ground	P3E_P0_RXN<9>	Differential pair	96
97	P3E_P0_TXP<8>	Transmitter Lane 8,	GND	Ground	98
99	P3E_P0_TXN<8>	Differential pair	P3E_P0_RXP<8>	Receiver Lane 8,	100
101	GND	Ground	P3E_P0_RXN<8>	Differential pair	102
103	P3E_P0_TXP<7>	Transmitter Lane 7,	GND	Ground	104
105	P3E_P0_TXN<7>	Differential pair	P3E_P0_RXP<7>	Receiver Lane 7,	106
107	GND	Ground	P3E_P0_RXN<7>	Differential pair	108
109	P3E_P0_TXP<6>	Transmitter Lane 6,	GND	Ground	110
111	P3E_P0_TXN<6>	Differential pair	P3E_P0_RXP<6>	Receiver Lane 6,	112
113	GND	Ground	P3E_P0_RXN<6>	Differential pair	114
115	P3E_P0_TXP<5>	Transmitter Lane 5,	GND	Ground	116
117	P3E_P0_TXN<5>	Differential pair	P3E_P0_RXP<5>	Receiver Lane 5,	118
119	GND	Ground	P3E_P0_RXN<5>	Differential pair	120
121	P3E_P0_TXP<4>	Transmitter Lane 4,	GND	Ground	122
123	P3E_P0_TXN<4>	Differential pair	P3E_P0_RXP<4>	Receiver Lane 4,	124
125	GND	Ground	P3E_P0_RXN<4>	Differential pair	126
127	P3E_P0_TXP<3>	Transmitter Lane 3,	GND	Ground	128
129	P3E_P0_TXN<3>	Differential pair	P3E_P0_RXP<3>	Receiver Lane 3,	130
131	GND	Ground	P3E_P0_RXN<3>	Differential pair	132
133	P3E_P0_TXP<2>	Transmitter Lane 2,	GND	Ground	134
135	P3E_P0_TXN<2>	Differential pair	P3E_P0_RXP<2>	Receiver Lane 2,	136
137	GND	Ground	P3E_P0_RXN<2>	Differential pair	138
139	P3E_P0_TXP<1>	Transmitter Lane 1,	GND	Ground	140
141	P3E_P0_TXN<1>	Differential pair	P3E_P0_RXP<1>	Receiver Lane 1,	142
143	GND	Ground	P3E_P0_RXN<1>	Differential pair	144
145	P3E_P0_TXP<0>	Transmitter Lane 0,	GND	Ground	146
147	P3E_P0_TXN<0>	Differential pair	P3E_P0_RXP<0>	Receiver Lane 0,	148
149	GND	Ground	P3E_P0_RXN<0>	Differential pair	150
151	P3E_P1_TXP<15>	Transmitter Lane 15,	GND	Ground	152
153	P3E_P1_TXP<15>	Differential pair	P3E_P1_RXP<15>	Receiver Lane 15,	154
155	GND	Ground	P3E_P1_RXP<15>	Differential pair	156

157	P3E_P1_TXP<14>	Transmitter Lane 14,	GND	Ground	158
159	P3E_P1_TXN<14>	Differential pair	P3E_P1_RXP<14>	Receiver Lane 14,	160
161	GND	Ground	P3E_P1_RXN<14>	Differential pair	162
163	P3E_P1_TXP<13>	Transmitter Lane 13,	GND	Ground	164
165	P3E_P1_TXN<13>	Differential pair	P3E_P1_RXP<13>	Receiver Lane 13,	166
167	GND	Ground	P3E_P1_RXN<13>	Differential pair	168
169	P3E_P1_TXP<12>	Transmitter Lane 12,	GND	Ground	170
171	P3E_P1_TXN<12>	Differential pair	P3E_P1_RXP<12>	Receiver Lane 12,	172
173	GND	Ground	P3E_P1_RXN<12>	Differential pair	174
175	P3E_P1_TXP<11>	Transmitter Lane 11,	GND	Ground	176
177	P3E_P1_TXN<11>	Differential pair	P3E_P1_RXP<11>	Receiver Lane 11,	178
179	GND	Ground	P3E_P1_RXN<11>	Differential pair	180
181	P3E_P1_TXP<10>	Transmitter Lane 10,	GND	Ground	182
183	P3E_P1_TXN<10>	Differential pair	P3E_P1_RXP<10>	Receiver Lane 10,	184
185	GND	Ground	P3E_P1_RXN<10>	Differential pair	186
187	P3E_P1_TXP<9>	Transmitter Lane 9,	GND	Ground	188
189	P3E_P1_TXN<9>	Differential pair	P3E_P1_RXP<9>	Receiver Lane 9,	190
191	GND	Ground	P3E_P1_RXN<9>	Differential pair	192
193	P3E_P1_TXP<8>	Transmitter Lane 8,	GND	Ground	194
195	P3E_P1_TXN<8>	Differential pair	P3E_P1_RXP<8>	Receiver Lane 8,	196
197	GND	Ground	P3E_P1_RXN<8>	Differential pair	198
199	PRESENT#	Present signal	GND	Ground	200

Table 10. PCIe x32 Connector Pinout - 60 Pin

Pin	Side A Golden Finger		Side B Golden Finger		Pin
#	Name	Description	Name	Description	#
1	GND	Ground	RSVD2	Reserved	2
3	P3E_P1_TXP<7>	Transmitter Lane 7,	GND	Ground	4
5	P3E_P1_TXN<7>	Differential pair	P3E_P1_RXP<7>	Receiver Lane 7,	6
7	GND	Ground	P3E_P1_RXN<7>	Differential pair	8
9	P3E_P1_TXP<6>	Transmitter Lane 6,	GND	Ground	10
11	P3E_P1_TXN<6>	Differential pair	P3E_P1_RXP<6>	Receiver Lane 6,	12
13	GND	Ground	P3E_P1_RXN<6>	Differential pair	14
15	P3E_P1_TXP<5>	Transmitter Lane 5,	GND	Ground	16
17	P3E_P1_TXN<5>	Differential pair	P3E_P1_RXP<5>	Receiver Lane 5,	18
19	GND	Ground	P3E_P1_RXN<5>	Differential pair	20
21	P3E_P1_TXP<4>	Transmitter Lane 4,	GND	Ground	22
23	P3E_P1_TXN<4>	Differential pair	P3E_P1_RXP<4>	Receiver Lane 4,	24
25	GND	Ground	P3E_P1_RXN<4>	Differential pair	26
27	P3E_P1_TXP<3>	Transmitter Lane 3,	GND	Ground	28
29	P3E_P1_TXN<3>	Differential pair	P3E_P1_RXP<3>	Receiver Lane 3,	30
31	GND	Ground	P3E_P1_RXN<3>	Differential pair	32
33	P3E_P1_TXP<2>	Transmitter Lane 2,	GND	Ground	34
35	P3E_P1_TXN<2>	Differential pair	P3E_P1_RXP<2>	Receiver Lane 2,	36

37	GND	Ground	P3E_P1_RXN<2>	Differential pair	38
39	P3E_P1_TXP<1>	Transmitter Lane 1,	GND	Ground	40
41	P3E_P1_TXN<1>	Differential pair	P3E_P1_RXP<1>	Receiver Lane 1,	42
43	GND	Ground	P3E_P1_RXN<1>	Differential pair	44
45	P3E_P1_TXP<0>	Transmitter Lane 0,	GND	Ground	46
47	P3E_P1_TXN<0>	Differential pair	P3E_P1_RXP<0>	Receiver Lane 0,	48
49	GND	Ground	P3E_P1_RXN<0>	Differential pair	50
51	JTAG_TDI	JTAG TDI	GND	Ground	52
53	JTAG_TDO	JTAG TDO	JTAG_TMS	JTAG TMS	54
55	GND	Ground	JTAG_TCK	JTAG TCK	56
57	USB2_DP	USB 2.0	GND	Ground	58
59	USB2_DN	USB 2.0	JTAG_TRST	JTAG Reset	60

11.4 PCIe MiniSAS HD Connectors

The motherboard optionally supports vertical MiniSAS HD connectors for cabling PCIe from the motherboard to PCIe expansion cards. The connector shall support 4 lanes of PCIe and the necessary management signals (clocks, PERST#) to operate as a standalone PCIe interface. The pinout is shown in Table 11.

Table 11. PCIe Cable Connector Pinout

PCIe Cable Connector Pinout		
Pin	**Signal**	**Description**
D9	GND	Ground
D8	TX2-	PCIe Transmit Lane 2
D7	TX2+	PCIe Transmit Lane 2
D6	GND	Ground
D5	TX0-	PCIe Transmit Lane 0
D4	TX0+	PCIe Transmit Lane 0
D3	GND	Ground
D2	SB6	BMC_SMB_CLK
D2	SB5	BMC_SMB_DAT
C1	NC	NC
C2	NC	NC
C3	GND	Ground
C4	TX1+	PCIe Transmit Lane 1
C5	TX1-	PCIe Transmit Lane 1
C6	GND	Ground
C7	TX3+	PCIe Transmit Lane 3
C8	TX3-	PCIe Transmit Lane 3
C9	GND	Ground

B9	GND	Ground
B8	RX2-	PCIe Receive Lane 2
B7	RX2+	PCIe Receive Lane 2
B6	GND	Ground
B5	RX0-	PCIe Receive Lane 0
B4	RX0+	PCIe Receive Lane 0
B3	GND	Ground
B2	GND	GND
B1	PERST#	PERST#
A1	REFCLK+	PCIe Reference Clock
A2	REFCLK-	PCIe Reference Clock
A3	GND	Ground
A4	RX1+	PCIe Receive Lane 1
A5	RX1-	PCIe Receive Lane 1
A6	GND	Ground
A7	RX3+	PCIe Receive Lane 3
A8	RX3-	PCIe Receive Lane 3
A9	GND	Ground

11.5 M.2 Connectors

M.2 connectors are optionally integrated into the motherboard for expansion flash memory. The M.2 connector pinout is shown in Table 12. For more information about the M.2 interface, refer to the PCI Express M.2 Specification.

Table 12. M.2 connector pinout

M.2 Module Standard Pinout					
Pin	**Signal**	**Description**	**Pin**	**Signal**	**Description**
74	3.3V	3.3V Power	75	GND	Ground
72	3.3V	3.3V Power	73	GND	Ground
70	3.3V	3.3V Power	71	GND	Ground
68	SUSCLK(32KHz)	Reduce Power Clock	69	NC	Reserved
66	KEY	Module Key	67	GND	Ground
64	KEY	Module Key	65	KEY	Module Key
62	KEY	Module Key	63	KEY	Module Key
60	KEY	Module Key	61	KEY	Module Key
58	NC	Reserved	59	KEY	Module Key
56	NC	Reserved	57	GND	Ground

54	PEWAKE#	PCIe PME Wake (Open Drain)	55	REFLKCP	PCIe Reference Clock
52	CLKREQ#	Reference Clock Request	53	REFLKCN	PCIe Reference Clock
50	PERST#	PCIe Reset	51	GND	Ground
48	NC	Reserved	49	PETP0	PCIe Transmit Lane 0
46	NC	Reserved	47	PETN0	PCIe Transmit Lane 0
44	ALERT#	SMBus ALERT	45	GND	Ground
42	SMB_DATA	SMBus Data	43	PERP0	PCIe Receive Lane 0
40	SMB_CLK	SMBus Clock	41	PERN0	PCIe Receive Lane 0
38	DEVSLP	Device Sleep	39	GND	Ground
36	NC	Reserved	37	PETP1	PCIe Transmit Lane 1
34	NC	Reserved	35	PETN1	PCIe Transmit Lane 1
32	NC	Reserved	33	GND	Ground
30	NC	Reserved	31	PERP1	PCIe Receive Lane 1
28	NC	Reserved	29	PERN1	PCIe Receive Lane 1
26	NC	Reserved	27	GND	Ground
24	NC	Reserved	25	PETP2	PCIe Transmit Lane 2
22	NC	Reserved	23	PETN2	PCIe Transmit Lane 2
20	NC	Reserved	21	GND	Ground
18	3.3V	3.3V Power	19	PERP2	PCIe Receive Lane 2
16	3.3V	3.3V Power	17	PERN2	PCIe Receive Lane 2
14	3.3V	3.3V Power	15	GND	Ground
12	3.3V	3.3V Power	13	PETP3	PCIe Transmit Lane 3
10	DAS/DSS#	Drive Active Signal (Open Drain)	11	PETN3	PCIe Transmit Lane 3
8	NC	Reserved	9	GND	Ground
6	NC	Reserved	7	PERP3	PCIe Receive Lane 3
4	3.3V	3.3V Power	5	PERN3	PCIe Receive Lane 3
2	3.3V	3.3V Power	3	GND	Ground
			1	GND	Ground

11.6 SATA Cable Ports

The motherboard shall include support for four x1 SATA standard 7-pin connectors. The motherboard optionally supports up to two x4 MiniSAS HD connectors for expansion cabling of up to 8 additional SATA devices (12 total).

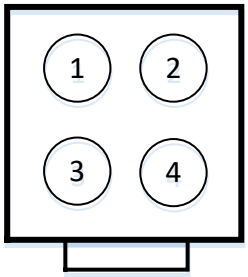
11.7 SATA Power Connector

The motherboard shall optionally include up to two 4-pin Mini-Fit® Jr™ 5566 series power connectors, Molex P/N 39-28-1043 or equivalent for supplying power to up to 4 SATA devices. The motherboard optionally supports additional connectors to provide power to up to an additional 8 SATA devices (12 total). Each connector pin has a maximum 13A current capacity. Table 13 describes the connector pinout. Figure 7 shows a top view of the physical pin numbering.

Table 13. SATA Power Connector

Pin	Signal name	Capacity (in A)
Pin 1 & 2	GND	13A (Black)
Pin 3	12V	9A (Yellow)
Pin 4	5V	9A (Red)

Figure 7. SATA Power Connector Pin Numbering



11.8 SATA Power Expansion Connector

The motherboard shall optionally include up to two 8-pin Mini-Fit® Jr™ 5566 series power connectors, Molex P/N 39-28-1083 or equivalent for supplying power to up to 8 additional SATA devices. Each connector has a maximum 13A current capacity. Table 14 describes the connector pinout.

shows a top view of the physical pin numbering.

Table 14. SATA Power Expansion Connector Pinout

Pin	Signal name	Capacity (in A)
Pin 1-4	GND	13A (Black)
Pin 5,6	12V	9A (Yellow)
Pin 7,8	5V	9A (Red)

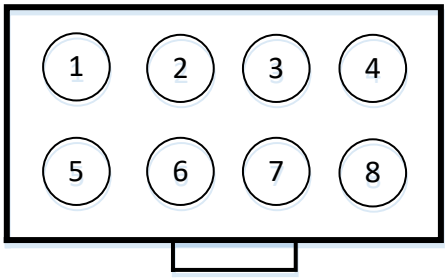


Figure 8. SATA Power Expansion Connector Pin Numbering

11.9 12V Power Connector

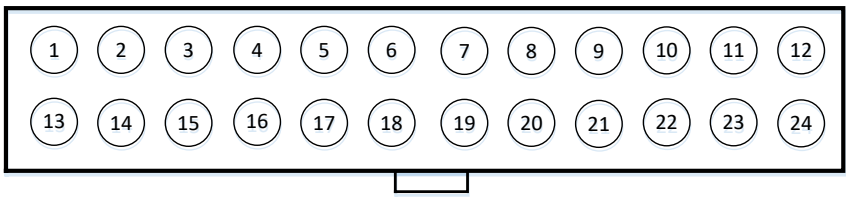
The motherboard shall include a 24-pin Mini-Fit® Jr™ 5569 series power connector, Molex P/N 3930-0240 or equivalent to support 12V cabling from the motherboard to the PSU. The connector shall support 800W. Table 15 describes the connector pinout. Figure 9 shows a top view of the physical pin numbering. For further information, refer to the Project Olympus PSU Specification.

Table 15. 12V Power Connector

Management Connector				
Pin	**Signal**	**I/O**	**Voltage**	**Description**
1	GND	I	0V	GND from PSU
2	GND	I	0V	GND from PSU
3	GND	I	0V	GND from PSU
4	GND	I	0V	GND from PSU
5	GND	I	0V	GND from PSU
6	GND	I	0V	GND from PSU
7	P12V_PSU	I	12V	12V Power from PSU
8	P12V_PSU	I	12V	12V Power from PSU
9	P12V_PSU	I	12V	12V Power from PSU
10	P12V_PSU	I	12V	12V Power from PSU

11	P12V_PSU	I	12V	12V Power from PSU
12	P12V_PSU	I	12V	12V Power from PSU
13	GND	I	0V	GND from PSU
14	GND	I	0V	GND from PSU
15	GND	I	0V	GND from PSU
16	GND	I	0V	GND from PSU
17	GND	I	0V	GND from PSU
18	GND	I	0V	GND from PSU
19	P12V_PSU	I	12V	12V Power from PSU
20	P12V_PSU	I	12V	12V Power from PSU
21	P12V_PSU	I	12V	12V Power from PSU
22	P12V_PSU	I	12V	12V Power from PSU
23	P12V_PSU	I	12V	12V Power from PSU
24	P12V_PSU	I	12V	12V Power from PSU

Figure 9. Mini-Fit Connector Pin Numbering



11.10 Management Connector

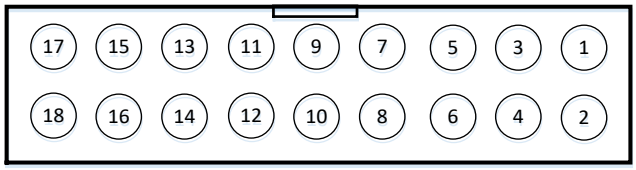
The motherboard shall include a connector for interface management signals from the motherboard to the Rack Manager through a cable to a rear panel connector on the server assembly. The connector for supporting the cable shall be an 18 pin Molex Picoblade™ series connector, Molex part number 87831-1820 or equivalent. Table 16 describes the connector pinout. Figure 10 shows a top view of the physical pin numbering.

Table 16. 1U Management Connector

1U Management Connector				
Pin	**Signal**	**I/O**	**Voltage**	**Description**
1	PWR_EN#	I	3.3V	Enable signal from Rack Manager to HSC on the Server
2	LR_SELECT	I	RS232	Left/Right Node Select
3	SLOT_ID0	I	3.3V	NODE ID from PMDU to the Server
4	SLOT_ID1	I	3.3V	NODE ID from PMDU to Server
5	SERVER_THROTTLE#	I	3.3V	Server Throttle control from Rack Manager
6	PRESENT#	O	3.3V	Indicates Server presence to the Rack Manager

7	I2C _SCL	O	3.3V	I^2C Clock to PSU (PMBus)
8	I2C_SDA	I/O	3.3V	I^2C Data to PSU (PMBus)
9	I2C_GND	I	0V	GND reference for I^2C bus
10	PS_ON#	O	3.3V	Turns on PSU. Pulled low on MB
11	PSU_ALERT#	I	3.3V	I^2C Alert from the PSU
12	PSU_LED0	I	3.3V	PSU LED 0(Green)
13	PSU_LED1	I	3.3V	PSU LED 1(Yellow)
14	SLOT_ID2	I	3.3V	NODE ID from PMDU to Server
15	SLOT_ID3	I	3.3V	NODE ID from PMDU to Server
16	SLOT_ID4	I	3.3V	NODE ID from PMDU to Server
17	SLOT_ID5	I	3.3V	NODE ID from PMDU to Server
18	NC	I	0	No Connect

Figure 10. 1U Management Connector Pin Numbering



11.11 OCuLink x8 Connector

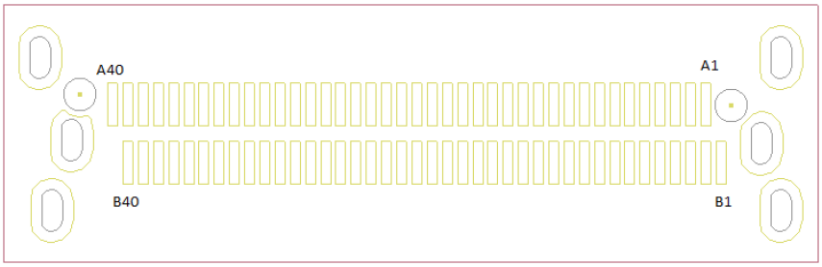
The motherboard shall include a connector for cabling PCIe x8 from the motherboard to the FPGA Card. The connector for supporting the cable shall be an 80-pin vertical Molex Nanopitch™ series connector or equivalent (Molex part number 173162-0334). Table 17 describes the connector pinout. Figure 11 shows a top view of the physical pin numbering.

Table 17. OCuLink x8 Connector Pinout

Row A			Row B		
Pin	**Signal Name**	**Description**	**Pin**	**Signal Name**	**Description**
A1	GND	Ground	B1	GND	Ground
A2	PERp0	PCIe Receive Data to CPU	B2	PETp0	PCIe Transmit Data from CPU
A3	PERn0	PCIe Receive Data to CPU	B3	PETn0	PCIe Transmit Data from CPU
A4	GND	Ground	B4	GND	Ground
A5	PERp1	PCIe Receive Data to CPU	B5	PETp1	PCIe Transmit Data from CPU
A6	PERn1	PCIe Receive Data to CPU	B6	PETn1	PCIe Transmit Data from CPU
A7	GND	Ground	B7	GND	Ground
A8	NC	No Connect	B8	NC	No Connect
A9	NC	No Connect	B9	NC	No Connect
A10	GND	Ground	B10	GND	Ground
A11	NC	No Connect	B11	NC	No Connect

A12	NC	No Connect	B12	CPRSNT#	Cable Present
A13	GND	Ground	B13	GND	Ground
A14	PERp2	PCIe Receive Data to CPU	B14	PETp2	PCIe Transmit Data from CPU
A15	PERn2	PCIe Receive Data to CPU	B15	PETn2	PCIe Transmit Data from CPU
A16	GND	Ground	B16	GND	Ground
A17	PERp3	PCIe Receive Data to CPU	B17	PETp3	PCIe Transmit Data from CPU
A18	PERn3	PCIe Receive Data to CPU	B18	PETn3	PCIe Transmit Data from CPU
A19	GND	Ground	B19	GND	Ground
A20	RSVD	Reserved	B20	RSVD	Reserved
A21	RSVD	Reserved	B21	RSVD	Reserved
A22	GND	Ground	B22	GND	Ground
A23	PERp4	PCIe Receive Data to CPU	B23	PETp4	PCIe Transmit Data from CPU
A24	PERn4	PCIe Receive Data to CPU	B24	PETn4	PCIe Transmit Data from CPU
A25	GND	Ground	B25	GND	Ground
A26	PERp5	PCIe Receive Data to CPU	B26	PETp5	PCIe Transmit Data from CPU
A27	PERn5	PCIe Receive Data to CPU	B27	PETn5	PCIe Transmit Data from CPU
A28	GND	Ground	B28	GND	Ground
A29	NC	No Connect	B29	NC	No Connect
A30	NC	No Connect	B30	NC	No Connect
A31	GND	Ground	B31	GND	Ground
A32	NC	No Connect	B32	NC	No Connect
A33	NC	No Connect	B33	NC	No Connect
A34	GND	Ground	B34	GND	Ground
A35	PERp6	PCIe Receive Data to CPU	B35	PETp6	PCIe Transmit Data from CPU
A36	PERn6	PCIe Receive Data to CPU	B36	PETn6	PCIe Transmit Data from CPU
A37	GND	Ground	B37	GND	Ground
A38	PERp7	PCIe Receive Data to CPU	B38	PETp7	PCIe Transmit Data from CPU
A39	PERn7	PCIe Receive Data to CPU	B39	PETn7	PCIe Transmit Data from CPU
A40	GND	Ground	B40	GND	Ground

Figure 11. OCuLink x8 Pin Numbering



11.12 NCSI Connector

The motherboard shall include a connector for cabling NCSI signals from the motherboard to a NIC. The connector for supporting the cable shall be a 14-pin header connector, Molex part number 87831-1428 or equivalent. Table 18 describes the connector pinout. Figure 12 shows a top view of the physical pin numbering.

Table 18. NCSI Connector

NCSI Connector				
Pin	**Signal**	**I/O**	**Voltage**	**Description**
1	RXER	O	3.3V	Enable signal from Rack Manager to HSC on the motherboard
2	GND	I	0V	Ground
3	TXD1	I	3.3V	Transmit Data from BMC to NIC
4	CLK_50M	I	0V	50Mhz Clock
5	TXD0	I	3.3V	Transmit Data from BMC to NIC
6	GND	I	0V	Ground
7	TXEN	I	3.3V	Transmit Enable from BMC to NIC
8	GND	I	0V	Ground
9	CRSDV	O	3.3V	Receive carrier sense and data valid from NIC to BMC
10	GND	I	0V	Ground
11	RXD1	O	3.3V	Receive Data from NIC to BMC
12	GND	I	0V	Ground
13	RXD0	O	3.3V	Receive Data from NIC to BMC
14	GND	I	0V	Ground

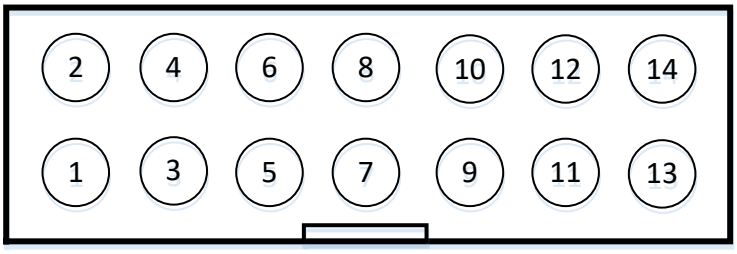


Figure 12. NCSI Connector Pin Numbering

11.13 USB 2.0 Internal Header

The motherboard shall support a header connector for enabling USB 2.0 communication with the FPGA card. The connector shall be TE 440054-4 or equivalent. Table 19 describes the connector pinout. Figure 13 shows a top view of the physical pin numbering.

Table 19. Internal USB Connector

Pin	Signal Name	I/O	Logic	Name/Description
1	P5_USB			5V (500mA max)
2	USB_N	I/O		USB Data
3	USB_P	I/O		USB Data
4	GND			Ground

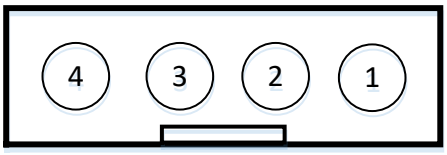


Figure 13. Internal USB Connector Pinout

11.14 Fan Control Connector

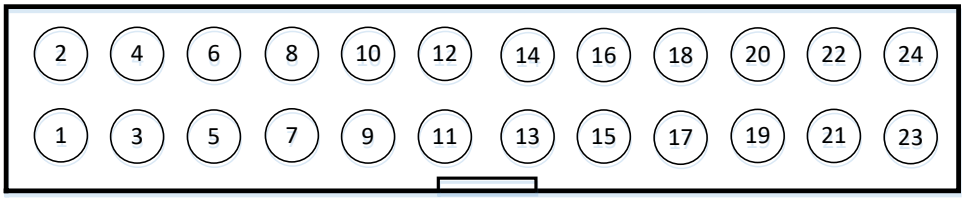
The motherboard shall support two header connectors for enabling fan control. The connector shall be Molex 87831-2420 or equivalent. Table 20 describes the connector pinout. Figure **14** shows a top view of the physical pin numbering.

Table 20. Fan Control Connector

Management Connector				
Pin	**Signal**	**I/O**	**Voltage**	**Description**
1	FAN5_PWM	O	5V	Fan #5 PWM
2	FAN4_PWM	O	5V	Fan #4 PWM
3	FAN5_TACH	I	5V	Fan #5 Tachometer
4	FAN4_TACH	I	5V	Fan #4 Tachometer
5	P12V	O	12V	12V Fan Power
6	P12V	O	12V	12V Fan Power
7	GND	O	0V	Ground
8	GND	O	0V	Ground
9	FAN3_PWM	O	5V	Fan #3 PWM

10	FAN2_PWM	O	5V	Fan #2 PWM
11	FAN3_TACH	I	0V	Fan #3 Tachometer
12	FAN2_TACH	I	3.3V	Fan #2 Tachometer
13	P12V	I	3.3V	12V Fan Power
14	P12V	I	3.3V	12V Fan Power
15	GND	O	0V	Ground
16	GND	O	0V	Ground
17	FAN1_PWM	O	5V	Fan #1 PWM
18	FAN0_PWM	O	5V	Fan #0 PWM
19	FAN1_TACH	I	5V	Fan #1 Tachometer
20	FAN0_TACH	I	5V	Fan #0 Tachometer
21	P12V	O	12V	12V Fan Power
22	P12V	O	12V	12V Fan Power
23	GND	O	0V	Ground
24	GND	O	0V	Ground

Figure 14. Fan Control Connector Pin Numbering



11.15 Connector Quality

The Project Olympus system is designed for use in datacenters with a wide range of humidity. The connectors for these deployments shall be capable of withstanding high humidity during shipping and installation. The baseline for plating DIMMs and PCIe connectors will be 30µ”-thick gold. DIMM connectors shall also include lubricant/sealant applied by the connector manufacturer that can remain intact after soldering and other manufacturing processes. The sealant is required to displace any voids in the connector gold plating.

12 Physical Specification

The motherboard is intended to be deployable in a variety of server mechanical configurations. Figure 15 depicts the dimensions of an example motherboard. The front of the chassis is on the right-hand side. Shown are locations of three PCIe x16 slots on one motherboard as a reference. For detailed mechanical information including mounting hole location and dimensions, please reference the Project Olympus mechanical data package.

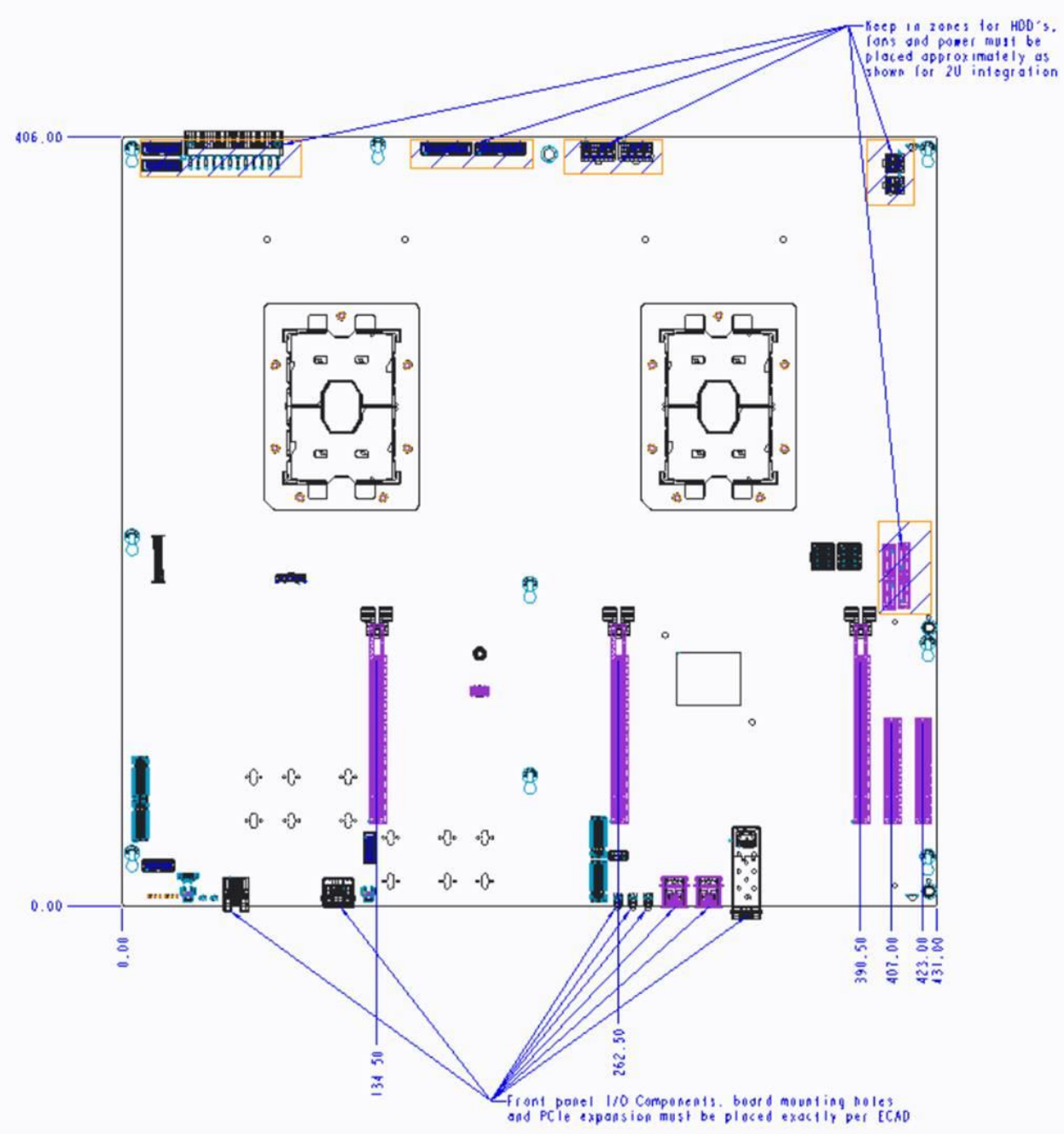


Figure 15. Example Motherboard Drawing

13 Environmental

The server is to be deployed in an environmentally controlled location. The inlet to the server will be exposed to the environment described in Table 21. The server must have the capability to provide full functional operation under the conditions given.

Table 21. Environmental Requirement

Specification		Requirement
Inlet temperature	Operating	• 50°F to 95°F (10°C to 35°C) • Maximum rate of change: 18°F (10°C)/hour • Allowable derating guideline of 1.6°F/1000ft (0.9°C/304m) above 3000 ft.
	Non-operating	• -40°F to 140°F (-40°C to 60°C) • Rate of change less than 36°F (20°C)/hour