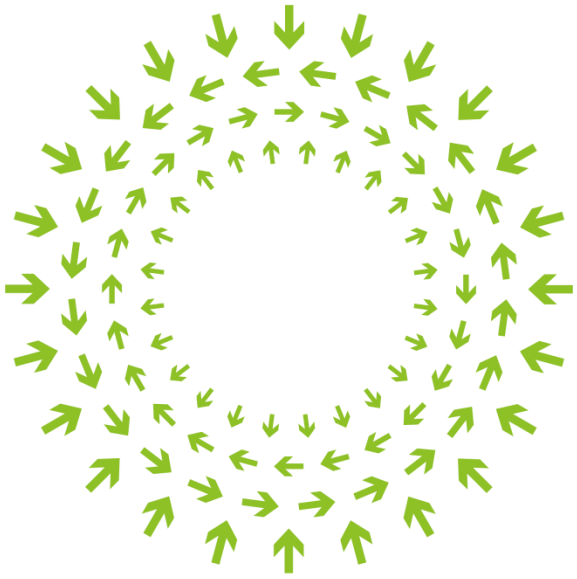

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# Project Olympus Rack Manager Specification

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# Revision History

| Date | Description |
|---|---|
| 2/15/2017 | Version 1.0 |

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# 1 Overview

The M2010 Rack Manager is an ARM processor based board for enabling management of Server Blades and a WCS Rack. It is designed to act as a hot swappable plug in module for a WCS Power and Management Distribution Unit (PMDU) or as part of a separate Rack Management Module for supporting Non WCS racks.

A 3D drawing of the Rack Manager is shown in Figure 1.

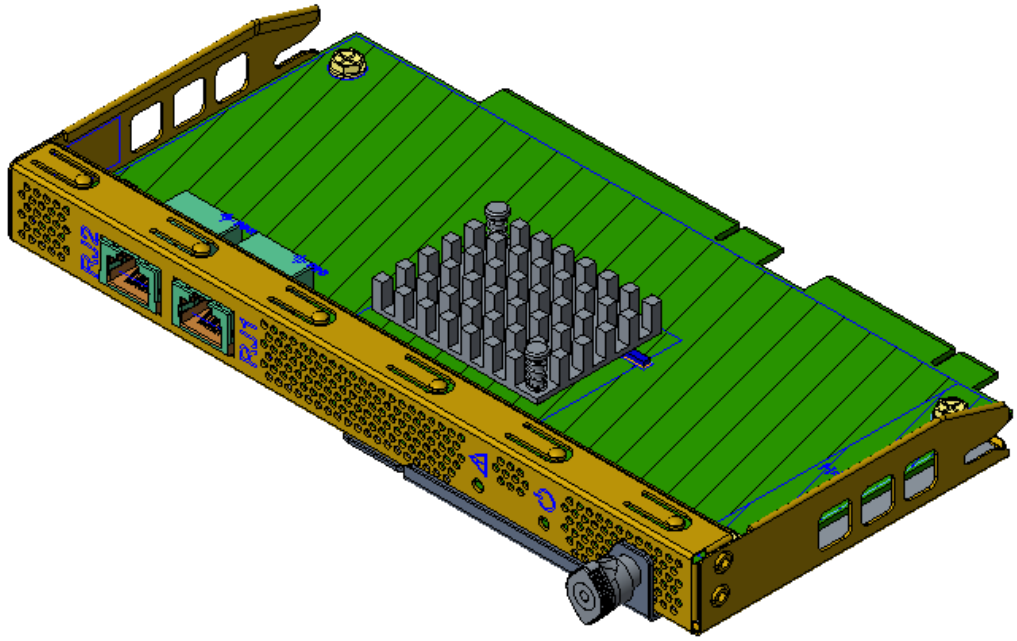


Figure 1. Rack Manager 3D

# 2 Block Diagram

The Rack Manager supports the following primary functional features:

- TI AM4376 ARM Processor
- 2x 1GbE for communication with Data Center and Server Blade management
- 2x UARTs for communication with Data Center Digi and Ethernet Management Switch. 1x Spare UART for Debug or future feature
- Control Signals for power control of blade slots
- Rack AC power monitoring
- Remote AC power control for Rack AC devices
- Remote On/Off control Bootstrap and RM Throttle from Row Manager in MOR
- PCIe x16 and PCIe x8 edge finger connectors for interfacing to the PMDU or other backplanes.

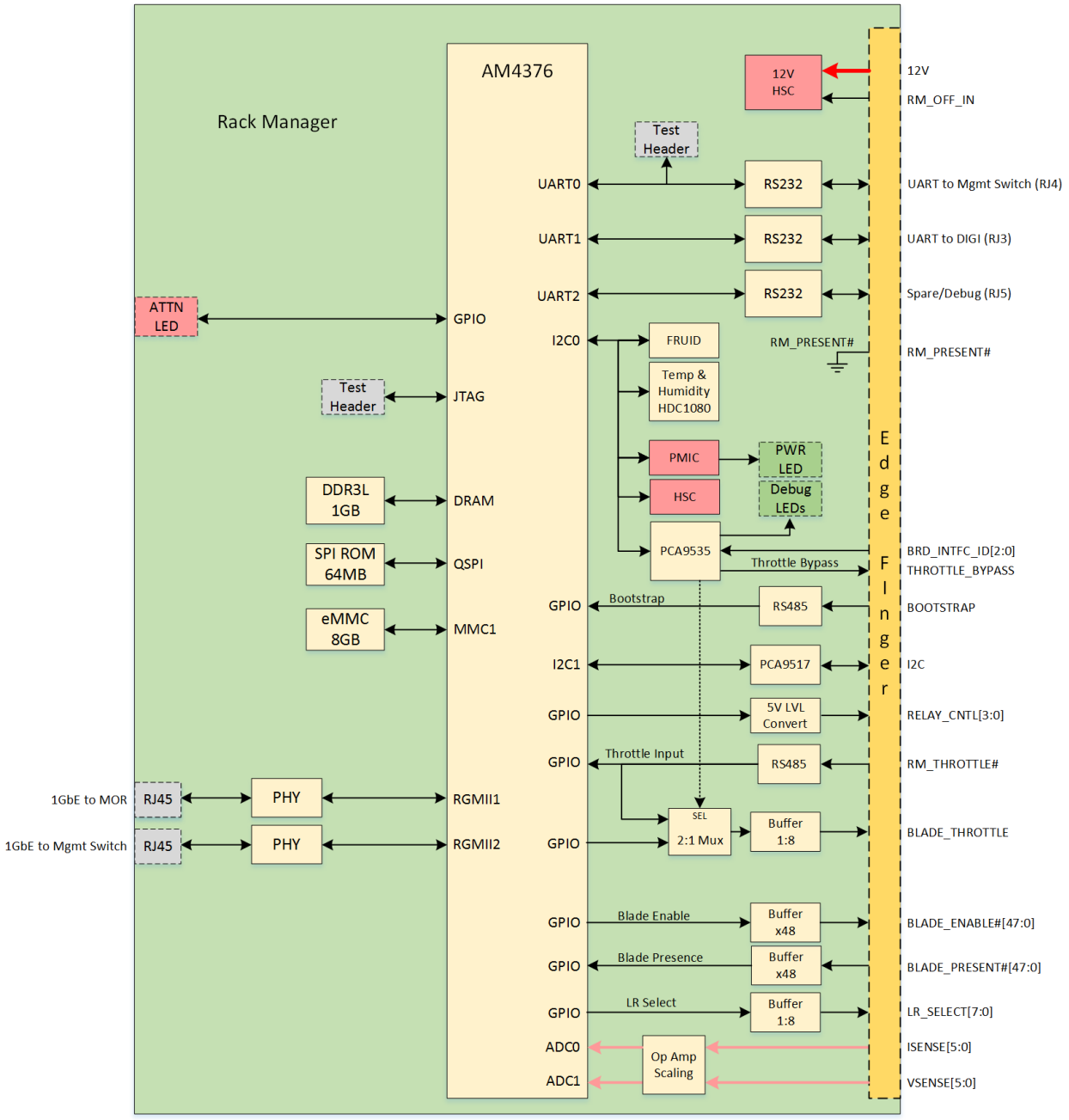



Figure 2. Top Level Block Diagram

# 3 Features

## 3.1 ARM Processor

The Rack Manager shall incorporate the Texas Instruments Sitara ARM Cortex-A9 processor AM4376. A list of key features is shown below. A functional block diagram of the process is shown in Figure 3.

- 32-bit RISC Processor with processing speed up to 1GHz
- 32-bit LPDDR2 (266MHz clock, LPDDR2-533 Data Rate), DDR3, and DDR3L (400MHz clock, DDR3-800 Data Rate) support up to 2GB
- General Purpose Memory Support NAND, NOR, SRAM. GPMC supports up to 512MB address capability with up to 16-bit ECC
- Up to two Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS) with two PRU cores each which is 32-bit RISC processor capable of running at 200MHz
- Internal 32.768-kHz Oscillator, RTC Logic, and 1.1V internal LDO
- Two Gigabit Ethernet MAC (10, 100 and 1000 Ethernet) with integrated switch
- Two Controller Area Network (CAN) ports, six UARTs, two McASPs, five McSPIs (Multichannel Serial Interface Ports up to 48MHz), three I2C ports (master and slave up to 400KHz), one QSPI (up to 48MHz) and one HDQ or 1-wire
- Support Crypto Hardware Accelerators (AES, SHA, RNG, DES and 3DES) and Secure Boot
- Two 12-bit successive Approximation Register(SAR) ADCs, 867K samples per second
- Up to six enhanced high resolution PWM modules
- Up to six banks of General Purpose I/O (GPIO), 32 GPIOs per bank
- 0.65mm ball pitch 491 pin BGA package 17mmx17mm

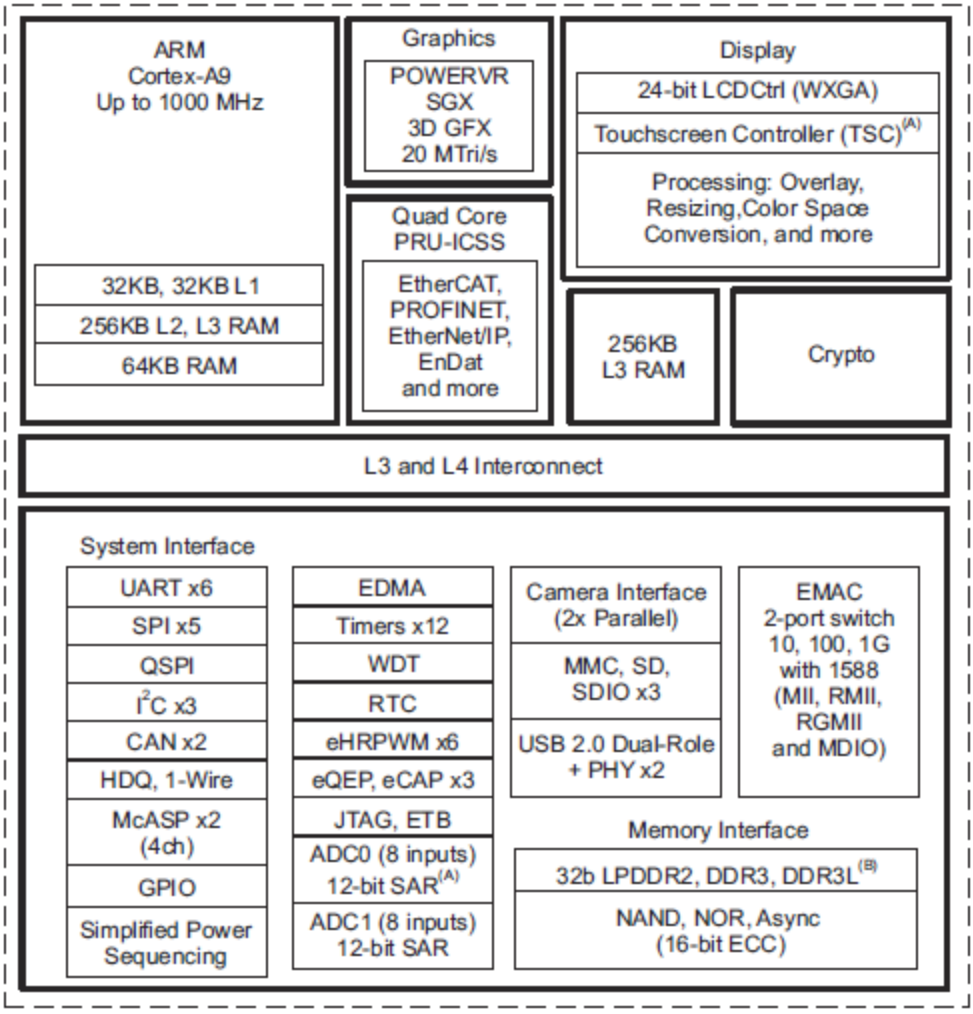



Figure 3. AM4376 Block Diagram

### 3.1.1 Boot Order (SYSBOOT)

The RM shall strap the SYSBOOT pins to enable the following boot order. To enable this, the SYSBOOT[4:0] inputs should be set to 11010b.

1. QSPI
2. eMMC1

The RM shall support a BOOTSTRAP input that when set should enable the following boot order. The board shall contain logic to change SYSBOOT[4:0] to 11100b when the BOOTSTRAP signal is asserted.

1. EMAC1 (network)

## 3.2 DDR3L Memory

The board shall support 1GB of DDR3L Memory. The memory is organized as x32 with two 32M x16 x8 banks DRAM.

## 3.3 NOR Flash

The Rack manager shall support 64MB of QSPI NOR Flash. The memory shall utilize QSPI mode running at 48Mhz.

## 3.4 eMMC Memory

The Rack Manager shall support a minimum of 1 GB of eMMC Memory.

## 3.5 Reset

The Rach Manager shall support two hardware resets.

- Power On Reset to AM4376 - This is driven from the power good signal of the power regulator on the Rack Manger board.
- Watchdog Reset – This is asserted to force a reset of AM4376 when the processor is locked up.

The sequence shall ensure that the output buffers remain disabled until they are enabled as part of the boot process. The circuit also supports override of the BOOTSTAP[2:1] pins to enable altering the boot device.

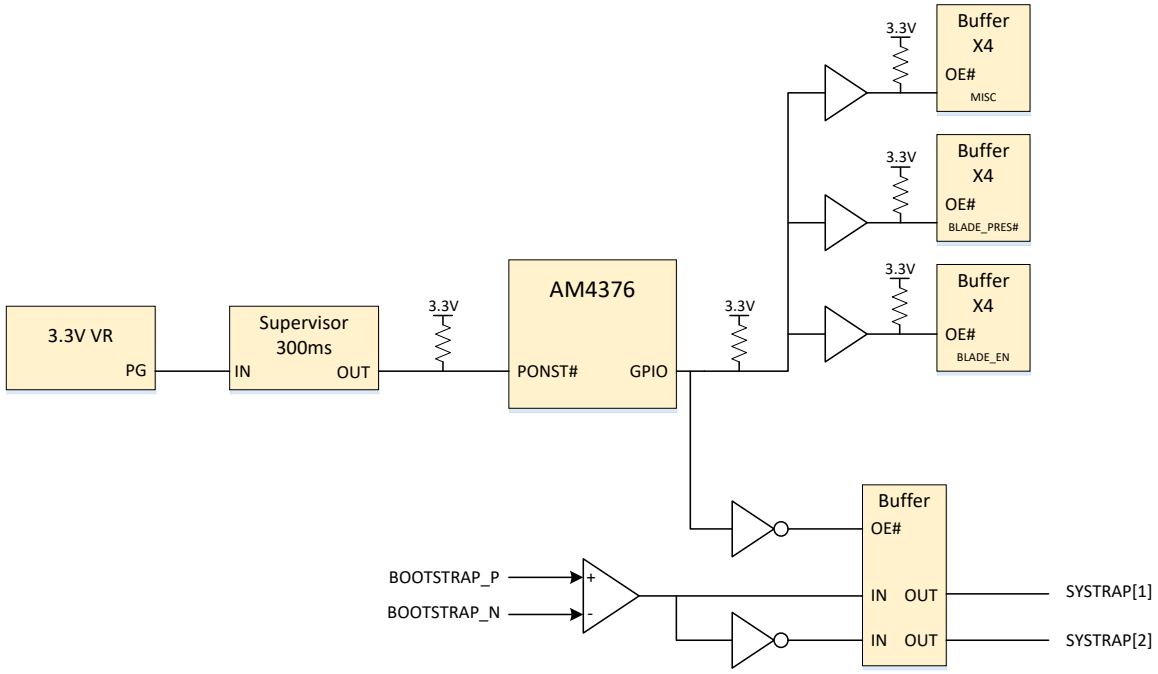



**Figure 4. Reset Block Diagram**

## 3.6 Clocks

The main clock for the processor is derived from a 24-MHz crystal. The AM4376 generates the base clock and subsequent module clocks as needed within the AM4376 processor. A 32-kHz clock for the RTC on the AM4376 is derived from a 32.768-kHz crystal on the board. A 25-MHz crystal is usually required for the clock input of Ethernet PHY

## 3.7 I2C

The Rack Manger shall support two I2C ports sourced from the I2C0 and I2C1 masters in the AM4376. A block diagram of the I2C tree is shown in Figure 5. I2C0 is used to communicated with components located on the Rack Manager. I2C1 is used to communicate with components located off the Rack Manager. The diagram assumes that the Rack Manager is in a standard PMDU configuration showing the FRUID addresses for the PIB and AC-DC Boards. Note that addresses shown are 8-bit address with the R/W bit as the LSB set to 0 (0x48=0100100x). All I2C ports shall support 100Khz operation.

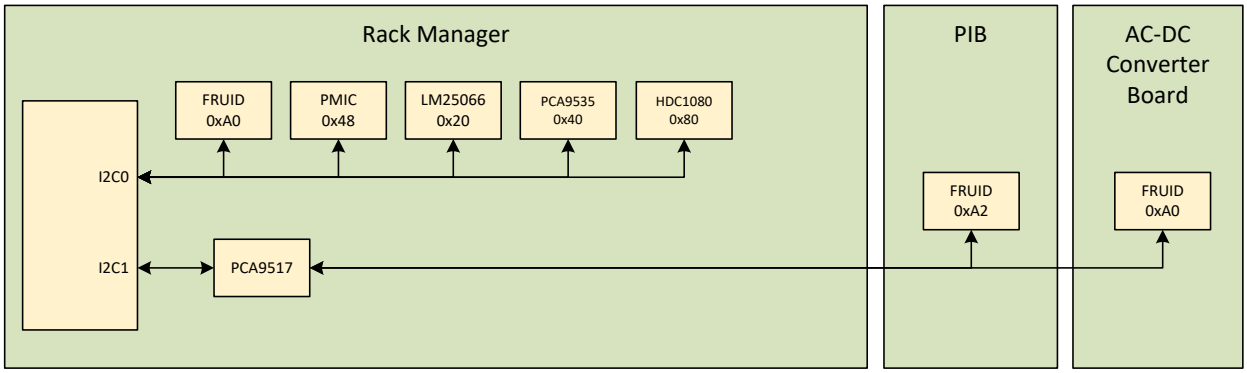



Figure 5. I2C Block Diagram

## 3.8 FRU EEPROM

The Rack Manager shall support a 64Kb FRUID EEPROM for storage of manufacturing data. The device shall be M24128-BWMN6TP or equivalent. Data in the EEPROM will be configured as an IPMI FRU device and fields are defined in the FRU ID Specification for the Rack Manager.

## 3.9 Real Time Clock

The Rack Manager shall support a CR2032 for the real-time clock contained in the AM4376 processor. The battery contains sufficient energy to power the RTC circuitry for a nominal lifetime of 7.5 years.

## 3.10 LEDs

The design shall contain the following LEDs to indicate functional status. The LEDs are listed in Table 1

Table 1. LED Assignments

| LED Name | REF Des | Color | Description |
|---|---|---|---|
| Power LED | LED6 | Green | Indicates all Power Rails are Good |
| Attention | LED5 | Amber | Indicates that a fault has occurred |
| LED[3:0] | LED[4:1] | Green | Status LEDs |

### 3.10.1 Power LED

The Power LED indicates that all the power rails on the Rack Manager are good. The LED shall be visible on the front bulkhead of the assembly.

### 3.10.2 Attention LED

The Attention LED indicates that a fault has been detected on the Rack Manager. The LED shall be controlled by GPIO on the AM4376 and shall be visible on the front bulkhead of the assembly.

### 3.10.3 Status LEDs

The Rack Manager shall support four LEDs to communicate status and debug information. The LEDs shall be driven by GPIOs on the PCA9535. The LEDs shall reside on the PCBA, but are not required to be visible on the bulkhead of the assembly. Functionality is not specified and is subject to change to support development and debug activities.

## 3.11 Blade Control

The Rack Manager shall support I/O for managing the power state of the blade slots. Description of the signals is given below.

### 3.11.1 Blade Presence

The Rack Manager shall support an active low BLADE_PRES# inputs from each of the 48 blade slots for determining the physical presence of a blade within a given slot. The signals shall be available on the GPIOs of the processor. This signal is pulled low to ground through a low impedance resistor on the blade. It should be buffered and pulled high through a high impedance pullup to isolate the Rack Manager from the blade.

### 3.11.2 Blade Enable

The Rack Manager shall support an active low BLADE_EN# output to each of the 48 blade slots for controlling the power state of the blade PSU. The signals shall be available on the GPIOs of the processor. The signal is pulled low to ground on the blade through a 1k resistor to set PSU on as the default state. The Rack Manager shall buffer the signal to isolate the Rack Manager from the blade. The design shall ensure that during hot plug insertion or removal of the Rack Manager, Blade Enable signals shall not be driven high and cause an inadvertent power disable of the blades.

### 3.11.3 Blade Throttle

The Rack Manager shall support throttle control output to each of the 48 blade slots for enabling control of the power throttling function on the blade. The throttle is controlled by the processor based on the RM_THROTTLE# input and the AC Power Monitor function. The processor shall drive a single GPIO for throttle. The board shall contain a buffer to fan out 8 throttle signals to the PMDU. The Rack Manager shall buffer the signal to isolate the Rack Manager from the blade. The design shall ensure that during hot plug insertion or removal of the Rack Manager, BLADE_THROTTLE signals shall not be driven high and cause inadvertent power throttling of the blades.

The board shall contain external logic to enable bypassing of the throttle logic as shown in Figure 6. The bypass (LOCAL_BYPASS) is controlled by an I2C GPIO to ensure that the bypass and buffer OE states are

maintained during boot cycle events. The board shall also support a separate bypass signal (THROTTLE_BYPASS) for enabling throttle bypass circuitry located externally on the ROW PIB when this board is used as part of the Stand-Alone Rack Manager. Both of these signals are pulled down on the PCB so that the default state of the board has bypass disabled.

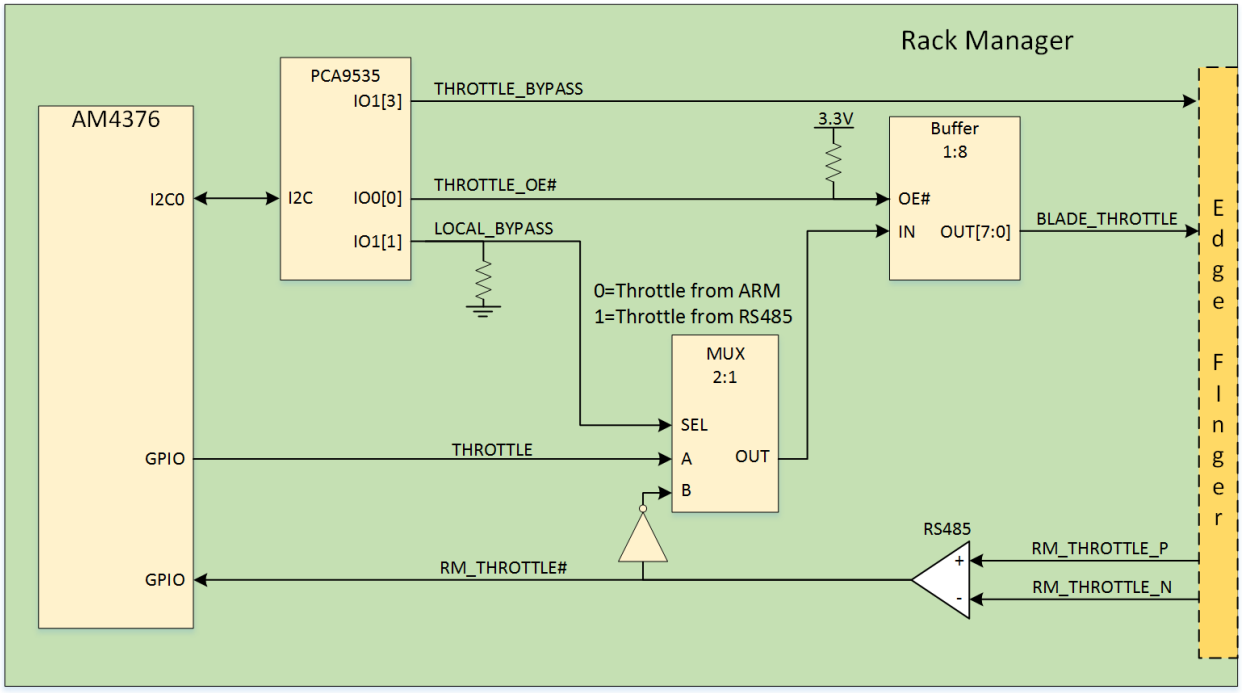



Figure 6. Throttle Block Diagram

### 3.11.4 LR Select

The Rack Manager shall support a select output to each of the 48 blade slots for enabling power control to the left and right entities within a single slot. The processor shall drive a single GPIO. The board shall contain a buffer to fan out 8 select signals to the PMDU.

## 3.12 AC Monitor

The Rack Manager shall support AC power monitoring of the 2 AC feeds to the PMDU. The board receives current and voltage sense inputs from the PIB and shall scale them appropriately for the A/D converters in the processor. The processor is responsible for filtering and interpreting the A/D results to determine the rack power.

## 3.13 Remote Recovery

The Rack Manager contains several features to aid in the remote recovery in the event of a power brownout, processor lockup, or corrupted boot image. These signals are driven from a Row Manager or similar remote device and are cabled to the PMDU or Rack Manager Module (RMM).

### 3.13.1 Remote Bootstrap

The Rack Manager shall support remote setting of the processor's boot. The signal when asserted shall alter the SYSBOOT setting to direct the processor to switch the boot location from the local ROM or Flash to the network enabling remote recovery in the event of a corrupted or blank boot image. Additional information is contained in Section 3.1.1. The design shall ensure that processor boots from the local ROM when the cable is removed.

### 3.13.2 Remote Rack Manager ON/OFF

The Rack Manager shall support a remote power on/off control signal input. The signal shall be 5V and when asserted shall disable power to the 12V HSC. The design shall ensure that the HSC remains on when the cable is inserted or removed.

### 3.13.3 Remote Throttle

The Rack Manager shall support a throttle signal (RM_THROTTLE#) input. When this signal is asserted, the Rack Manager shall assert a throttle output (BLADE_THROTTLE) to all the blades connected to the PMDU. The design shall ensure that throttle output is de-asserted when the cable is removed. The design shall also ensure that throttle control of the blades does not glitch or assert due to insertion of the cable.

### 3.13.4 Rack Manager Present

The Rack Manager shall support a single present signal (RM_PRESENT#). The signal shall be grounded on the blade to indicate physical presence of the Rack Manager to the RMM.

## 3.14 Remote AC Power Control

The Rack Manager shall support power control to external AC relays for remote on/off control of rack AC devices. The board shall support four 5V outputs that interface to the PMDU through the edge finger connectors.

## 3.15 PCB Revision

The Rack Manager shall support reading of a 3-bit PCB revision using GPIOs on the AM4376 processor. Revision shall be set using strapping resistors. The purpose of the ID bits is to communicate to firmware the identity of the Rack Manager in the event that different PCB revisions will require different firmware features to be enabled or disabled. The ID should be incremented with each revision of the PCB.

**Table 2. PCB Revision ID**

| ID | Description |
|---|---|
| 000 | EV |
| 001 | DV |
| 010 | PV |

| | |
|---|---|
| 011 | TBD |
| 100 | TBD |
| 101 | TBD |
| 110 | TBD |
| 111 | TBD |

## 3.16 Board Interface ID

The Rack Manager shall support reading of a 3-bit interface ID using I2C IO expander connecting to the AM4376 processor. The ID bits are received through the PCIe edge finger connector. The purpose of the ID bits is to communicate to firmware the identity of the board mated to the Rack Manager in the event that different interface boards will require different firmware features to be enabled or disabled. ID assignments are shown in Table 3.

**Table 3. Board Interface ID**

| ID | Description |
|---|---|
| 000 | Power Interface Board (PMDU) |
| 001 | Row PIB Board (RMM) |
| 010 | Manufacturing Test Board |
| 011 | TBD |
| 100-111 | TBD |

## 3.17 AM4376 GPIO Summary

Table 4 shows a summary of the AM4376 GPIO usage.

**Table 4. AM4376 GPIO Assignments**

| Signal | # of Signals | GPIOs Used | I/O | Description |
|---|---|---|---|---|
| BLADE_PRESENT# | 48 | 48 | I | Indicates blade installed in slot |
| BLADE_ENABLE# | 48 | 48 | O | Enable/Disables Blade Power |
| BLADE_THROTTLE | 1 | 1 | O | Enables Blade power throttle |
| DC_THROTTLE# | 1 | 1 | I | Throttle Input |
| RELAY_CNTL | 4 | 4 | O | Turns On/Off Relays in AC Cords |
| BUFF_OE# | 1 | 1 | O | Enables I/O Buffers |
| ATTENTION_LED | 1 | 1 | O | Local LED - TBD |
| LR_SELECT | 1 | 1 | O | Selects Left or Right location in Blade Slot |
| Total | | 105 | | |
| Available | | 105 | | |

## 3.18 I2C Expander (PCA9535)

The Rack Manager supports one I2C Expanders for control and reading of selected I/Os. The I/O assignments for each expander are shown in Table 5.

**Table 5. PCA9535 I/O Assignments**

| 0x40 | | PCA9535C | | |
|---|---|---|---|---|
| **Port** | **GPIO** | **I/O** | **Signal** | **Description** |
| 1 | 7 | O | Debug LED 3 | 0=LED On |
| 1 | 6 | O | Debug LED 2 | 0=LED On |
| 1 | 5 | O | Debug LED 1 | 0=LED On |
| 1 | 4 | O | Debug LED 0 | 0=LED On |
| 1 | 3 | O | THROTTLE_BYPASS | 1=Bypass |
| 1 | 2 | I | Board Interface ID 2 | See Section 3.16 |
| 1 | 1 | I | Board Interface ID 1 | See Section 3.16 |
| 1 | 0 | I | Board Interface ID 0 | See Section 3.16 |
| 0 | 7 | I | N/A | N/A |
| 0 | 6 | I | N/A | N/A |
| 0 | 5 | I | N/A | N/A |
| 0 | 4 | I | N/A | N/A |
| 0 | 3 | I | P12VB_GOOD | 1=Good |
| 0 | 2 | I | P12VA_GOOD | 1=Good |
| 0 | 1 | O | LOCAL_BYPASS | 1=Bypass |
| 0 | 0 | O | THROTTLE_OE# | 0=Output Enabled |

## 3.19 UARTS

The Rack Manager shall support 3 RS232 UARTS for interfacing to external devices.

- UART 0 – Intended for communication with Management Switches. Utilizes software flow control and does not require hardware flow control signals.
- UART 1 – Intended for communication with the Data Center Digi device. Utilizes full hardware flow control (RTS, CTS, DSR, DTR).
- UART 2 – Intended for debug and future expansion. Utilizes software flow control and does not require hardware flow control signals.

## 3.20 Power

### 3.20.1 Power Subsystem

The Rack Manager shall receive 12V through the PCIe connector or a separate power connector. The Rack Manager shall utilize a hot swap circuitry to control in-rush current during hot installation of the

board. Power to the hot swap controller can be disabled externally using the RM_OFF_IN signal. Power rails are generated by a Texas Instruments TPS 65218 Power Management IC (PMIC). A block diagram of the power delivery is shown in Figure 7.

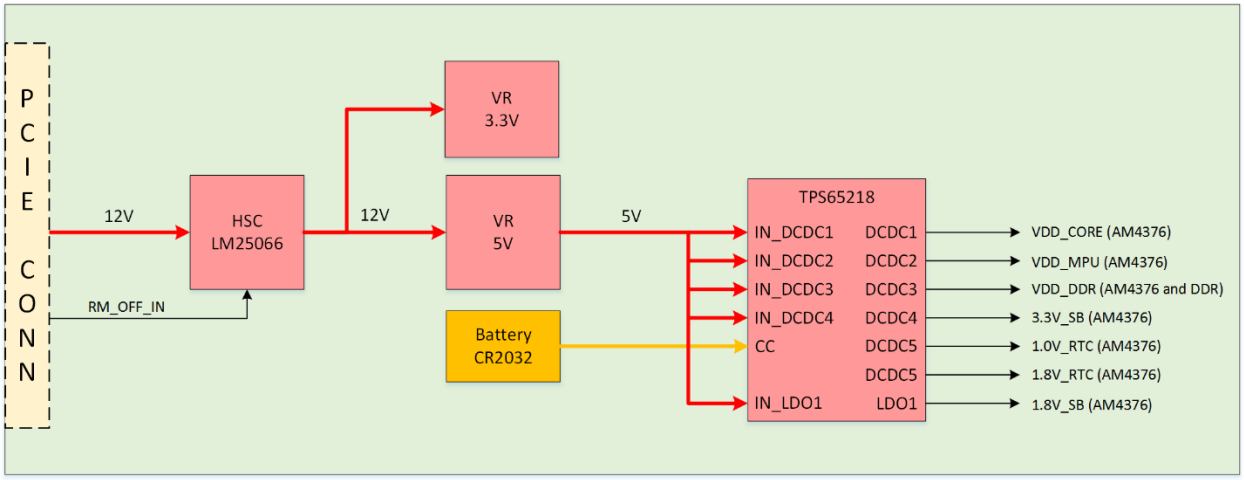


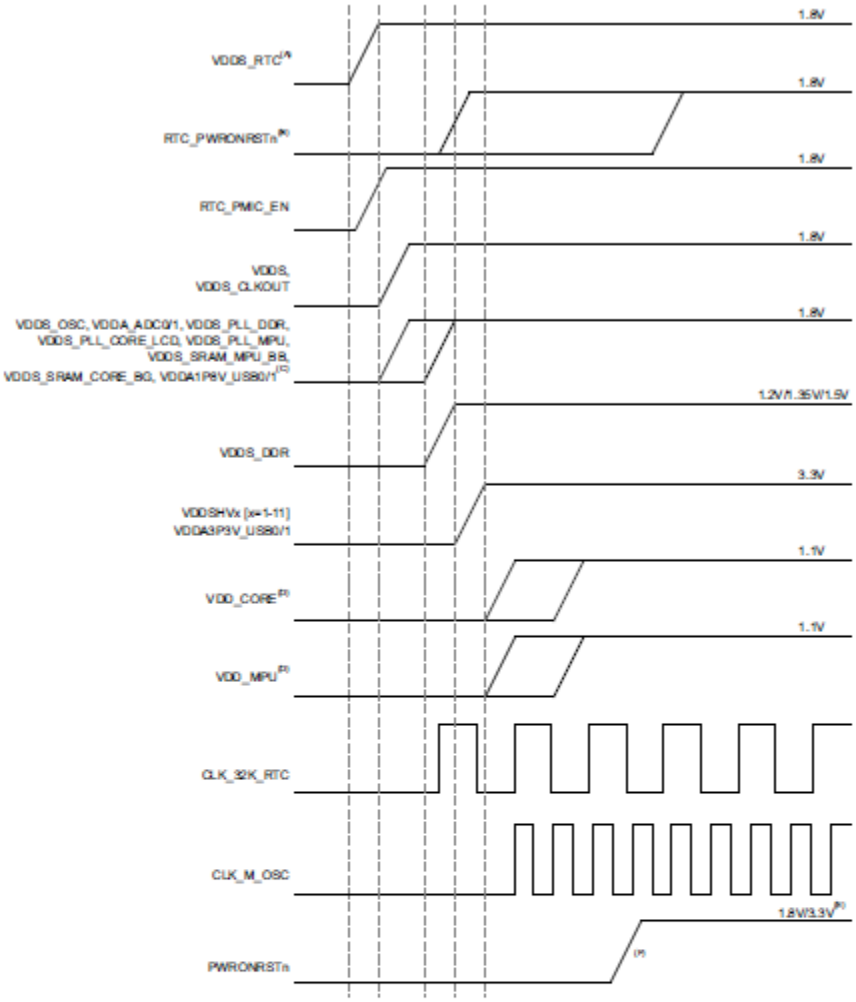

Figure 7. Power Block Diagram

### 3.20.2 Power-up/down Sequence

The power-up sequencing of all voltage rails, clock and reset must meet AM4376 clock and power sequencing requirements as defined by the device datasheet and referenced in Figure 8. The AM4376 requires the following power sequence during power up:

- 1.8-> 1.35V->3.3V->1.1V, Clock->PWRONRSTn

PWRONRSTn should stay low until all power rails and clock are stable.




A. The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC.
If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply. If CAP_VDD_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE.
VDDS_RTC can be ramped independent of other supplies if RTC_PMIC_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE when internal RTC LDO is enabled, there might be a small amount of leakage current on VDD_CORE.

B. RTC_PWRONRSTn should be asserted for at least 1 ms and can be released before the 32-kHz clock is stable.

C. These supplies can be ramped together with VDDS, VDDS_CLKOUT supplies if powered from the same source only. If a USB port is not used, the respective VDDA1P8V_USB may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If a system does not have a 3.3-V supply, the VDDA3P3V_USB may be connected to ground.

D. VDD_MPU and VDD_CORE can be supplied from the same power source if OPPs higher than OPP100 are not used.

E. PWRONRSTn input voltage thresholds are not dependent on VDDSHV3 voltage and the terminal is not fail-safe. PWRONRSTn can accept 1.8-V or 3.3-V input levels when VDDSHV3 is configured as 3.3 V. However, PWRONRSTn can only accept 1.8 V input levels when VDDSHV3 is configured as 1.8 V. For details on this input terminal, see Section 5.7.

F. It is required to hold the PWRONRSTn terminal low until all the supplies have ramped and the input clock CLK_M_OSC is stable.

**Figure 5-4. Power Sequencing with RTC Feature Enabled, All Dual-Voltage IOs Configured as 3.3 V**

Figure 8. Power Up Sequence Diagram

In addition to the power up sequence, it is recommended to limit the maximum slew rate of supplies to be less than 1.0E+5V/s to maintain the safe operating range of the internal ESD protection devices. The following diagram shows the supply ramp slew should be more than 18us for 1.8V supply.

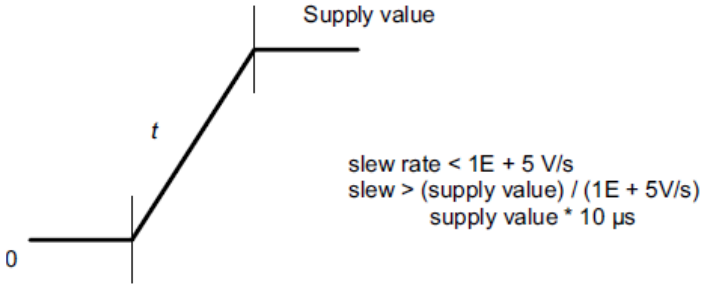



Figure 9. Power Supply Slew Rate Diagram

### 3.20.3 Grounding and Return

The chassis grounding/return is provided to the board from the front bezel assembly through the alignment and mounting holes that secure the motherboard to PSU. The Rack Manager board ground is also tied to the PSU ground through the edge finger connector. Chassis ground and Logic ground are tied together on the board.

### 3.20.4 AC-DC Power Monitoring

The Rack Manager receives two power good signals from the AC-DC Converter board indicating the status of AC to DC 12V converters. The power goods are connected to the PCA9535 I2C expander.

## 3.21 Stackup

The PCB stackup is shown in Figure 10. The board material shall be NPG_170N with OSP surface finish.

To enable visual tracking, the PCB color shall be different for EVT (red), DVT (blue) and PVT (green) builds. PVT build (green) shall be the production PCB color.

| 10-Layer Board Stack-Up (1.6 mm) | | | | |
|---|---|---|---|---|
| Layer Name | Layer Description | Material | Layer Thickness (mil) | Copper Weight (oz) |
| | SOLDER MASK | Solder Mask | 0.50 | |
| Signal1 | SIGNAL | Copper | 1.90 | 0.5 + 1 (plating) |
| | PREPREG | FR4 | 4.00 | |
| GPlane2 | GND | Copper | 1.20 | 1.0 |
| | CORE | FR4 | 4.00 | |
| Signal3 | SIGNAL | Copper | 1.20 | 1.0 |
| | PREPREG | FR4 | 6.50 | |
| GPlane4 | GND | Copper | 1.20 | 1.0 |
| | CORE | FR4 | 4.00 | |
| PPlane5 | SIG / PWR | Copper | 1.20 | 1.0 |
| | PREPREG | FR4 | 12.00 | |
| PPlane6 | PWR / SIG | Copper | 1.20 | 1.0 |
| | CORE | FR4 | 4.00 | |
| GPlane7 | GND | Copper | 1.20 | 1.0 |
| | PREPREG | FR4 | 6.50 | |
| Signal8 | SIGNAL | Copper | 1.20 | 1.0 |
| | CORE | FR4 | 4.00 | |
| GPlane9 | GND | Copper | 1.20 | 1.0 |
| | PREPREG | FR4 | 4.00 | |
| Signal10 | SIGNAL | Copper | 1.90 | 0.5 + 1 (plating) |
| | SOLDER MASK | Solder Mask | 0.50 | |
| Overall Board Thickness w/SM | | | 63.40 | mils Tol: +/-10% |

Figure 10. PCB Stackup

# 4 Connectors

## 4.1 PCIe x16 Goldfinger

The board contains one PCIe x16 Edge Finger connector for interfacing signals from the Rack Manager to the Power Interface Board in the MDU. The pinout is shown in Table 6.

Table 6. PCIe x16 Pinout

| Pin # | Name | I/O | Voltage | Description |
|---|---|---|---|---|
| A1 | GND | I | 0V | GND |
| A2 | GND | I | 0V | GND |
| A3 | BLADE_EN_4_N | O | 3.3V | Blade power enable output |
| A4 | BLADE_EN_3_N | O | 3.3V | Blade power enable output |
| A5 | BLADE_EN_2_N | O | 3.3V | Blade power enable output |
| A6 | BLADE_EN_1_N | O | 3.3V | Blade power enable output |
| A7 | BLADE_EN_5_N | O | 3.3V | Blade power enable output |
| A8 | BLADE_EN_6_N | O | 3.3V | Blade power enable output |
| A9 | BLADE_EN_7_N | O | 3.3V | Blade power enable output |

| | | | | |
|---|---|---|---|---|
| A10 | BLADE_EN_8_N | O | 3.3V | Blade power enable output |
| A11 | GND | I | 0V | GND |
| **Mechanical Key** | | | | |
| A12 | BLADE_EN_12_N | O | 3.3V | Blade power enable output |
| A13 | BLADE_EN_11_N | O | 3.3V | Blade power enable output |
| A14 | BLADE_EN_10_N | O | 3.3V | Blade power enable output |
| A15 | BLADE_EN_9_N | O | 3.3V | Blade power enable output |
| A16 | BLADE_EN_13_N | O | 3.3V | Blade power enable output |
| A17 | BLADE_EN_14_N | O | 3.3V | Blade power enable output |
| A18 | BLADE_EN_15_N | O | 3.3V | Blade power enable output |
| A19 | BLADE_EN_16_N | O | 3.3V | Blade power enable output |
| A20 | GND | I | 0V | GND |
| A21 | BLADE_EN_17_N | O | 3.3V | Blade power enable output |
| A22 | BLADE_EN_18_N | O | 3.3V | Blade power enable output |
| A23 | BLADE_EN_19_N | O | 3.3V | Blade power enable output |
| A24 | BLADE_EN_20_N | O | 3.3V | Blade power enable output |
| A25 | BLADE_EN_24_N | O | 3.3V | Blade power enable output |
| A26 | BLADE_EN_23_N | O | 3.3V | Blade power enable output |
| A27 | BLADE_EN_22_N | O | 3.3V | Blade power enable output |
| A28 | BLADE_EN_21_N | O | 3.3V | Blade power enable output |
| A29 | GND | I | 0V | Ground |
| A30 | BLADE_EN_25_N | O | 3.3V | Blade power enable output |
| A31 | BLADE_EN_26_N | O | 3.3V | Blade power enable output |
| A32 | BLADE_EN_27_N | O | 3.3V | Blade power enable output |
| A33 | BLADE_EN_28_N | O | 3.3V | Blade power enable output |
| A34 | BLADE_EN_32_N | O | 3.3V | Blade power enable output |
| A35 | BLADE_EN_31_N | O | 3.3V | Blade power enable output |
| A36 | BLADE_EN_30_N | O | 3.3V | Blade power enable output |
| A37 | BLADE_EN_29_N | O | 3.3V | Blade power enable output |
| A38 | GND | I | 0V | GND |
| A39 | BLADE_EN_33_N | O | 3.3V | Blade power enable output |
| A40 | BLADE_EN_34_N | O | 3.3V | Blade power enable output |
| A41 | BLADE_EN_35_N | O | 3.3V | Blade power enable output |
| A42 | BLADE_EN_36_N | O | 3.3V | Blade power enable output |
| A43 | BLADE_EN_40_N | O | 3.3V | Blade power enable output |
| A44 | BLADE_EN_39_N | O | 3.3V | Blade power enable output |
| A45 | BLADE_EN_38_N | O | 3.3V | Blade power enable output |
| A46 | BLADE_EN_37_N | O | 3.3V | Blade power enable output |
| A47 | GND | I | 0V | GND |
| A48 | BLADE_EN_41_N | O | 3.3V | Blade power enable output |
| A49 | BLADE_EN_42_N | O | 3.3V | Blade power enable output |

| | | | | |
|---|---|---|---|---|
| A50 | BLADE_EN_43_N | O | 3.3V | Blade power enable output |
| A51 | BLADE_EN_44_N | O | 3.3V | Blade power enable output |
| A52 | BLADE_EN_48_N | O | 3.3V | Blade power enable output |
| A53 | BLADE_EN_47_N | O | 3.3V | Blade power enable output |
| A54 | BLADE_EN_46_N | O | 3.3V | Blade power enable output |
| A55 | BLADE_EN_45_N | O | 3.3V | Blade power enable output |
| A56 | GND | I | 0V | Ground |
| A57 | LR_SELECT0 | O | 3.3V | Left/Right Node Select |
| A58 | LR_SELECT1 | O | 3.3V | Left/Right Node Select |
| A59 | LR_SELECT2 | O | 3.3V | Left/Right Node Select |
| A60 | LR_SELECT3 | O | 3.3V | Left/Right Node Select |
| A61 | LR_SELECT7 | O | 3.3V | Left/Right Node Select |
| A62 | LR_SELECT6 | O | 3.3V | Left/Right Node Select |
| A63 | LR_SELECT5 | O | 3.3V | Left/Right Node Select |
| A64 | LR_SELECT4 | O | 3.3V | Left/Right Node Select |
| A65 | GND | I | 0V | Ground |
| A66 | UART1_TX | O | RS232 | UART 1 RTS |
| A67 | UART1_RTS | O | RS232 | UART1 DTR |
| A68 | UART1_DTR | O | RS232 | UART1 TX |
| A69 | UART1_CTS | I | RS232 | UART1 RX |
| A70 | UART1_DSR | I | RS232 | UART1 DSR |
| A71 | UART1_RX | I | RS232 | UART1 CTS |
| A72 | GND | I | 0V | Ground |
| A73 | UART2_RX | I | RS232 | UART2 RX |
| A74 | UART2_TX | O | RS232 | UART2 TX |
| A75 | GND | I | 0V | GND |
| A76 | I2C1_BUFF1_SDA | I/O | 3.3V | I2C Data |
| A77 | I2C1_BUFF1_SCL | O | 3.3V | I2C Clock |
| A78 | BOARD_INT_ID_0 | I | 3.3V | Board ID |
| A79 | BOARD_INT_ID_1 | I | 3.3V | Board ID |
| A80 | BOARD_INT_ID_2 | I | 3.3V | Board ID |
| A81 | P12V7A_GOOD | I | 3.3V | P12VA Power Good |
| A82 | P12V7B_GOOD | I | 3.3V | P12VB Power Good |
| B1 | GND | I | 0V | GND |
| B2 | GND | I | 0V | GND |
| B3 | BLADE_PRESENT_4_N | I | 3.3V | Blade present |
| B4 | BLADE_PRESENT_3_N | I | 3.3V | Blade present |
| B5 | BLADE_PRESENT_2_N | I | 3.3V | Blade present |
| B6 | BLADE_PRESENT_1_N | I | 3.3V | Blade present |
| B7 | BLADE_PRESENT_5_N | I | 3.3V | Blade present |
| B8 | BLADE_PRESENT_6_N | I | 3.3V | Blade present |

| | | | | |
|---|---|---|---|---|
| B9 | BLADE_PRESENT_7_N | I | 3.3V | Blade present |
| B10 | BLADE_PRESENT_8_N | I | 3.3V | Blade present |
| B11 | GND | I | 0V | GND |
| **Mechanical Key** | | | | |
| B12 | BLADE_PRESENT_12_N | I | 3.3V | Blade present |
| B13 | BLADE_PRESENT_11_N | I | 3.3V | Blade present |
| B14 | BLADE_PRESENT_10_N | I | 3.3V | Blade present |
| B15 | BLADE_PRESENT_9_N | I | 3.3V | Blade present |
| B16 | BLADE_PRESENT_13_N | I | 3.3V | Blade present |
| B17 | BLADE_PRESENT_14_N | I | 3.3V | Blade present |
| B18 | BLADE_PRESENT_15_N | I | 3.3V | Blade present |
| B19 | BLADE_PRESENT_16_N | I | 3.3V | Blade present |
| B20 | GND | I | 0V | GND |
| B21 | BLADE_PRESENT_17_N | I | 3.3V | Blade present |
| B22 | BLADE_PRESENT_18_N | I | 3.3V | Blade present |
| B23 | BLADE_PRESENT_19_N | I | 3.3V | Blade present |
| B24 | BLADE_PRESENT_20_N | I | 3.3V | Blade present |
| B25 | BLADE_PRESENT_24_N | I | 3.3V | Blade present |
| B26 | BLADE_PRESENT_23_N | I | 3.3V | Blade present |
| B27 | BLADE_PRESENT_22_N | I | 3.3V | Blade present |
| B28 | BLADE_PRESENT_21_N | I | 3.3V | Blade present |
| B29 | GND | I | 0V | Ground |
| B30 | BLADE_PRESENT_25_N | I | 3.3V | Blade present |
| B31 | BLADE_PRESENT_26_N | I | 3.3V | Blade present |
| B32 | BLADE_PRESENT_27_N | I | 3.3V | Blade present |
| B33 | BLADE_PRESENT_28_N | I | 3.3V | Blade present |
| B34 | BLADE_PRESENT_32_N | I | 3.3V | Blade present |
| B35 | BLADE_PRESENT_31_N | I | 3.3V | Blade present |
| B36 | BLADE_PRESENT_30_N | I | 3.3V | Blade present |
| B37 | BLADE_PRESENT_29_N | I | 3.3V | Blade present |
| B38 | GND | I | 0V | GND |
| B39 | BLADE_PRESENT_33_N | I | 3.3V | Blade present |
| B40 | BLADE_PRESENT_34_N | I | 3.3V | Blade present |
| B41 | BLADE_PRESENT_35_N | I | 3.3V | Blade present |
| B42 | BLADE_PRESENT_36_N | I | 3.3V | Blade present |
| B43 | BLADE_PRESENT_40_N | I | 3.3V | Blade present |
| B44 | BLADE_PRESENT_39_N | I | 3.3V | Blade present |
| B45 | BLADE_PRESENT_38_N | I | 3.3V | Blade present |
| B46 | BLADE_PRESENT_37_N | I | 3.3V | Blade present |
| B47 | GND | I | 0V | GND |
| B48 | BLADE_PRESENT_41_N | I | 3.3V | Blade power enable output |

| | | | | |
|---|---|---|---|---|
| B49 | BLADE_PRESENT_42_N | I | 3.3V | Blade power enable output |
| B50 | BLADE_PRESENT_43_N | I | 3.3V | Blade power enable output |
| B51 | BLADE_PRESENT_44_N | I | 3.3V | Blade power enable output |
| B52 | BLADE_PRESENT_48_N | I | 3.3V | Blade power enable output |
| B53 | BLADE_PRESENT_47_N | I | 3.3V | Blade power enable output |
| B54 | BLADE_PRESENT_46_N | I | 3.3V | Blade power enable output |
| B55 | BLADE_PRESENT_45_N | I | 3.3V | Blade power enable output |
| B56 | GND | I | 0V | Ground |
| B57 | BLADE_19TO24_THROTTLE | O | 3.3V | Blade Throttle |
| B58 | BLADE_13TO18_THROTTLE | O | 3.3V | Blade Throttle |
| B59 | BLADE_7TO12_THROTTLE | O | 3.3V | Blade Throttle |
| B60 | BLADE_1TO6_THROTTLE | O | 3.3V | Blade Throttle |
| B61 | BLADE_25TO30_THROTTLE | O | 3.3V | Blade Throttle |
| B62 | BLADE_31TO36_THROTTLE | O | 3.3V | Blade Throttle |
| B63 | BLADE_37TO42_THROTTLE | O | 3.3V | Blade Throttle |
| B64 | BLADE_43TO48_THROTTLE | O | 3.3V | Blade Throttle |
| B65 | GND | I | 0V | Ground |
| B66 | RELAY_CNTL_3 | O | 5V | 0 = AC Power enabled to load<br>1 = AC Power disabled to load |
| B67 | RELAY_CNTL_2 | O | 5V | 0 = AC Power enabled to load<br>1 = AC Power disabled to load |
| B68 | RELAY_CNTL_1 | O | 5V | 0 = AC Power enabled to load<br>1 = AC Power disabled to load |
| B69 | RELAY_CNTL_0 | O | 5V | 0 = AC Power enabled to load<br>1 = AC Power disabled to load |
| B70 | GND | I | 0V | GND |
| B71 | UART0_RX | I | RS232 | UART0 RX |
| B72 | UART0_TX | O | RS232 | UART0 TX |
| B73 | RM_PRESENT# | O | 3.3V | Indicates RM is installed. |
| B74 | RM_OFF_IN | I | 5V | Hot Swap Controller disable |
| B75 | THROTTLE_BYPASS | O | 3.3V | Enables throttle to bypass Rack Manager |
| B76 | GND | I | 0V | I2C Data |
| B77 | RM_THROTTLE_RS485_P | I | RS485 | RM Throttle RS485 Input |
| B78 | RM_THROTTLE_RS485_N | I | RS485 | RM Throttle RS485 Input |
| B79 | GND | I | 0V | GND |
| B80 | BOOTSTRAP_RS485_P | I | RS485 | Bootstrap RS485 Input |
| B81 | BOOTSTRAP_RS485_N | I | RS485 | Bootstrap RS485 Input |
| B82 | GND | I | 0V | GND |

## 4.2 PCIe x8 Goldfinger

The board contains one PCIe x8 Edge Finger connector for interfacing signals from the Rack Manager to the Power Interface Board in the PMDU. The pinout is shown in Table 7.

**Table 7. PCIe x8 Pinout**

| Pin # | Name | I/O | Voltage | Description |
|---|---|---|---|---|
| A1 | GND | I | 0V | GND |
| A2 | GND | I | 0V | GND |
| A3 | GND | I | 0V | GND |
| A4 | GND | I | 0V | GND |
| A5 | GND | I | 0V | GND |
| A6 | GND | I | 0V | GND |
| A7 | NC | | | No Connect |
| A8 | P3V3 | O | 3.3V | 3.3V Power Output |
| A9 | P3V3 | O | 3.3V | 3.3V Power Output |
| A10 | P3V3 | O | 3.3V | 3.3V Power Output |
| A11 | P3V3 | O | 3.3V | 3.3V Power Output |
| **Mechanical Key** | | | | |
| A12 | P5V | O | 5V | 5V Power Output |
| A13 | P5V | O | 5V | 5V Power Output |
| A14 | P5V | O | 5V | 5V Power Output |
| A15 | NC | O | | No Connect |
| A16 | AGND | I | 0V | Analog GND |
| A17 | AGND | I | 0V | Analog GND |
| A18 | AC_SOURCE2_N2_VS | I | AC | AC Voltage Sense - Neutral |
| A19 | AC_SOURCE2_S_VS | I | AC | AC Voltage Sense - Line |
| A20 | AGND | I | 0V | Analog GND |
| A21 | AGND | I | 0V | Analog GND |
| A22 | AC_SOURCE2_S_CS2 | I | AC | AC Current Sense - Line |
| A23 | AC_SOURCE2_S_CS1 | I | AC | AC Current Sense - Line |
| A24 | AGND | I | 0V | Analog GND |
| A25 | AGND | I | 0V | Analog GND |
| A26 | AC_SOURCE2_N1_VS | I | AC | AC Voltage Sense - Neutral |
| A27 | AC_SOURCE2_R_VS | I | AC | AC Voltage Sense - Line |
| A28 | AGND | I | 0V | Analog GND |
| A29 | AGND | I | 0V | Analog GND |
| A30 | AC_SOURCE2_T_CS2 | I | AC | AC Current Sense - Line |
| A31 | AC_SOURCE2_T_CS1 | I | AC | AC Current Sense - Line |

| | | | | |
|---|---|---|---|---|
| A32 | AGND | I | 0V | Analog GND |
| A33 | AGND | I | 0V | Analog GND |
| A34 | AC_SOURCE2_N3_VS | I | AC | AC Voltage Sense - Neutral |
| A35 | AC_SOURCE2_T_VS | I | AC | AC Voltage Sense - Line |
| A36 | AGND | I | 0V | Analog GND |
| A37 | AGND | I | 0V | Analog GND |
| A38 | AC_SOURCE2_R_CS2 | I | 0V | AC Current Sense - Line |
| A39 | AC_SOURCE2_R_CS1 | I | 0V | AC Current Sense - Line |
| A40 | GND | I | 0V | GND |
| A41 | GND | I | 0V | GND |
| A42 | GND | I | 0V | GND |
| A43 | GND | I | 0V | GND |
| A44 | GND | I | 0V | GND |
| A45 | GND | I | 0V | GND |
| A46 | GND | I | 0V | GND |
| A47 | GND | I | 0V | GND |
| A48 | GND | I | 0V | GND |
| A49 | GND | I | 0V | GND |
| B1 | P12V_IN | I | 12V | 12V Power Input |
| B2 | P12V_IN | I | 12V | 12V Power Input |
| B3 | P12V_IN | I | 12V | 12V Power Input |
| B4 | P12V_IN | I | 12V | 12V Power Input |
| B5 | P12V_IN | I | 12V | 12V Power Input |
| B6 | NC | | | No Connect |
| B7 | GND | I | 0V | GND |
| B8 | GND | I | 0V | GND |
| B9 | GND | I | 0V | GND |
| B10 | GND | I | 0V | GND |
| B11 | GND | I | 0V | GND |
| **Mechanical Key** | | | | |
| B12 | GND | I | 0V | GND |
| B13 | GND | I | 0V | GND |
| B14 | GND | I | 0V | GND |
| B15 | GND | I | 0V | GND |
| B16 | GND | O | AC | GND |
| B17 | GND | O | AC | GND |
| B18 | AGND | I | 0V | Analog GND |
| B19 | AGND | I | 0V | Analog GND |
| B20 | AC_SOURCE1_N2_VS | I | AC | AC Voltage Sense - Neutral |
| B21 | AC_SOURCE1_S_VS | I | AC | AC Voltage Sense - Line |
| B22 | AGND | I | 0V | Analog GND |

| | | | | |
|---|---|---|---|---|
| B23 | AGND | I | 0V | Analog GND |
| B24 | AC_SOURCE1_S_CS2 | I | AC | AC Current Sense - Line |
| B25 | AC_SOURCE1_S_CS1 | I | AC | AC Current Sense - Line |
| B26 | AGND | I | 0V | Analog GND |
| B27 | AGND | I | 0V | Analog GND |
| B28 | AC_SOURCE1_N1_VS | I | AC | AC Voltage Sense - Neutral |
| B29 | AC_SOURCE1_R_VS | I | AC | AC Voltage Sense - Line |
| B30 | AGND | I | 0V | Analog GND |
| B31 | AGND | I | 0V | Analog GND |
| B32 | AC_SOURCE1_T_CS2 | I | AC | AC Current Sense - Line |
| B33 | AC_SOURCE1_T_CS1 | I | AC | AC Current Sense - Line |
| B34 | AGND | I | 0V | Analog GND |
| B35 | AGND | I | 0V | Analog GND |
| B36 | AC_SOURCE1_N3_VS | I | AC | AC Voltage Sense - Neutral |
| B37 | AC_SOURCE1_T_VS | I | AC | AC Voltage Sense - Line |
| B38 | AGND | I | 0V | Analog GND |
| B39 | AGND | I | 0V | Analog GND |
| B40 | AC_SOURCE1_R_CS2 | I | 0V | AC Current Sense - Line |
| B41 | AC_SOURCE1_R_CS1 | I | 0V | AC Current Sense - Line |
| B42 | GND | I | 0V | GND |
| B43 | GND | I | 0V | GND |
| B44 | GND | I | 0V | GND |
| B45 | GND | I | 0V | GND |
| B46 | GND | I | 0V | GND |
| B47 | GND | I | 0V | GND |
| B48 | GND | I | 0V | GND |
| B49 | GND | I | 0V | GND |

## 4.3 RJ45 GbE Connectors

The Rack Manager shall contain two RJ45 connectors located on the bulkhead of the assembly for cabling 1GbE. The pinout for the connector is shown in Table 8.

**Table 8. RJ45 GbE Pinout**

| Pin # | Signal | I/O | Description |
|---|---|---|---|
| 1 | TX_D1+ | O | Transmit Data + |
| 2 | TX_D1- | O | Transmit Data - |
| 3 | RX_D2+ | I | Receive Data + |
| 4 | BI_D3+ | I/O | Bi-directional Data + |
| 5 | BI_D3- | I/O | Bi-directional Data - |

| | | | |
|---|---|---|---|
| 6 | RX_D2- | I | Receive Data - |
| 7 | BI_D4+ | I/O | Bi-directional Data + |
| 8 | BI_D4- | I/O | Bi-directional Data - |

## 4.4 I2C Debug Header

The board shall include a 3 pin I2C header on all I2C busses. This is a standard 100mil pitch 3-pin header. The pinout should be compatible with standard I2C debug solutions such as Beagle and Aardvark.

# 5 Mechanical Specifications

This specification describes key mechanical elements of the M.2 storage board.

## 5.1 Mechanical Dimensions

Mechanical Dimensions are shown in Figure 11.

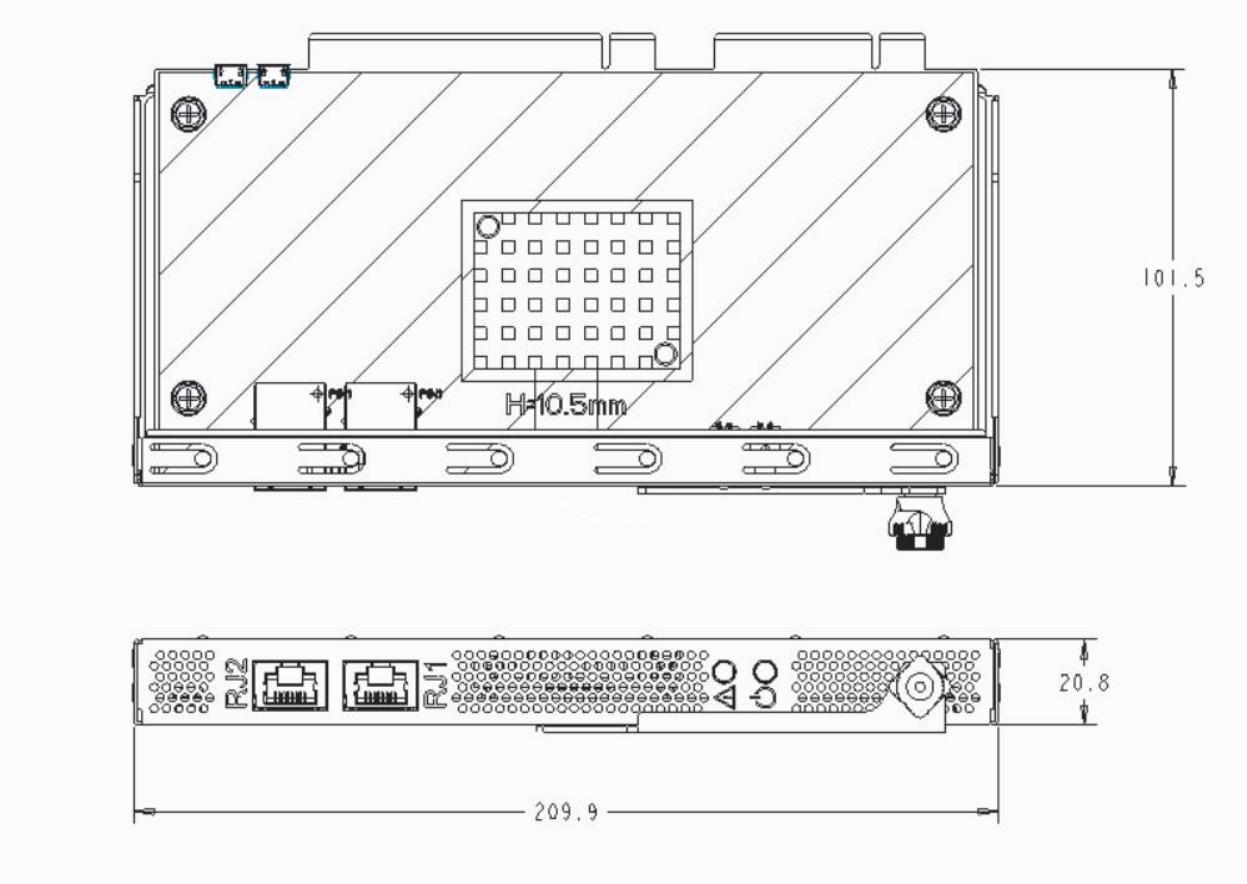



Figure 11. Mechanical Dimensions

## 5.2 Thermal

The solution must operate in a 60 degrees Centigrade environment and must be passively cooled.