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Ultra-Low-Power, I2C Real-Time Clock and Power Management

MAX31331

General Description

The MAX31331 ultra-low power, real-time clock (RTC) is a time-keeping device that consumes nominal 65nA timekeeping current, extending battery life. The MAX31331 supports a wide range of 32.768kHz crystals. A crystal with any capacitive loading (CL) spec can be used, which broadens the pool of usable crystals for this device. This device is accessed through an I^2C serial interface.

The device also features a backup supply pin (VBAT) and automatically switches over to the backup supply (VBAT) when the main supply (VCC) drops below the programmed threshold voltage and the backup supply (VBAT) voltage.

Other features include two time-of-day alarms, interrupt outputs, programmable square-wave output, event detection input with timestamping, and a serial bus timeout mechanism. The 32-byte timestamp registers double as RAM storage. The device features a digital Schmitt trigger input (DIN) which can be used to record timestamps and/or generate an interrupt on the falling/rising edge of the DIN signal. The clock/calendar provides seconds, minutes, hours, day, month, year, and date information. A 1/128 second register is available for a sub-second timestamp resolution. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in 24-hour/12-hour format.

The MAX31331 is available in lead (Pb)-free/RoHS compliant, 12-bump, 1.66mm x 1.26mm WLP with 0.4mm pitch, as well as a 10-pin 3mm x 3mm TDFN package.

The device supports the -40°C to +85°C extended temperature range.

Applications

- Medical
- Wearables
- Portable Instruments
- Telematics
- Industrial
- IOT

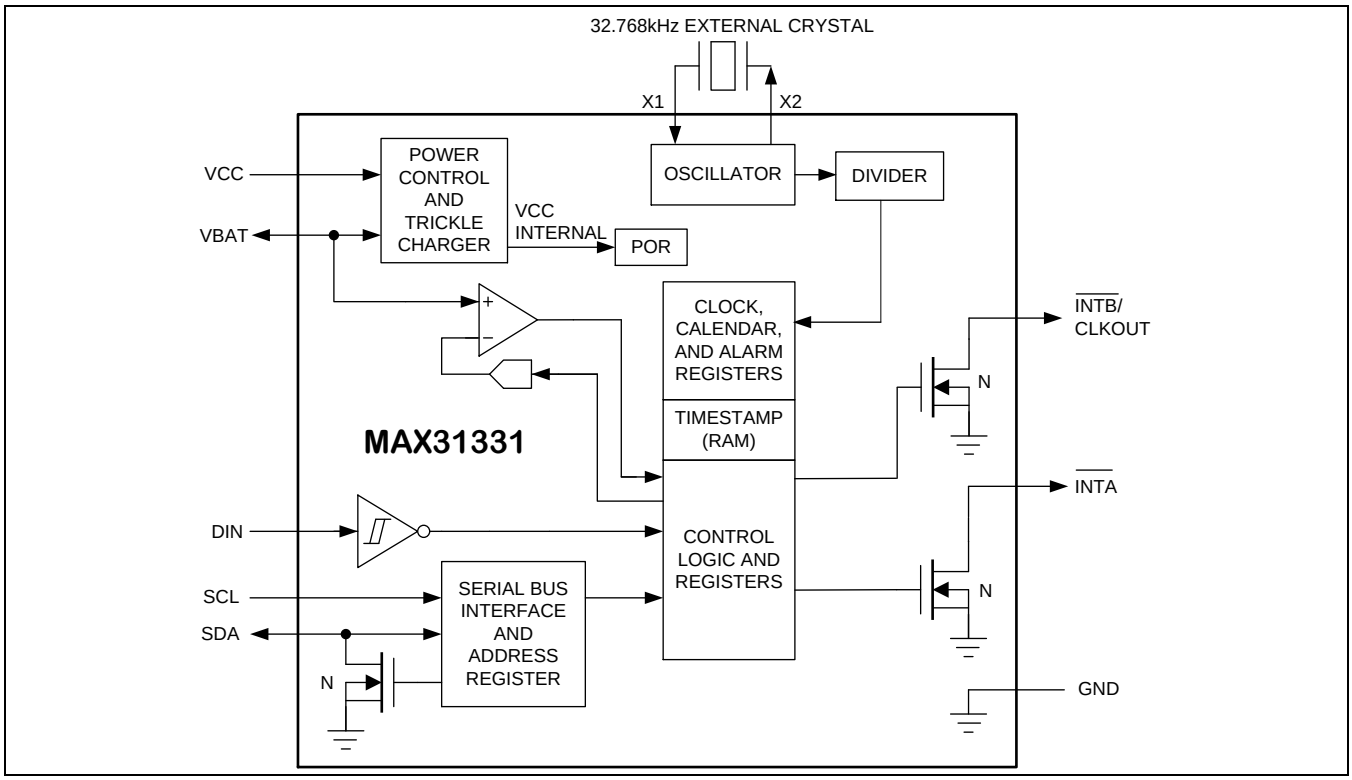
Benefits and Features

- Ultra-Low-Power Extends Run Time
  - 65nA Timekeeping Current
  - 1.1V to 5.5V Timekeeping Voltage Range
  - Automatic Switchover to Backup Supply on Power Fail Event
  - Trickle Charger for External Supercapacitor or Rechargeable Battery
- Small Footprint and Low BOM
  - 1.66mm x 1.26mm 12-bump WLP
  - 3mm x 3mm 10-pin TDFN
  - No External Load Capacitors Required
- Provides Flexibility
  - Wide Range of External Crystals Supported (No External Loading Required)
  - Frequency Correction with <0.5ppm Resolution
  - 1.62V to 5.5V Interface Voltage Range
- Value-added Features for Ease of Use
  - Event Detection with Dedicated Pin
  - Timestamps for Various Events
  - Low Battery Voltage Detection
  - 1/128 Second Register
  - Alarms and Countdown Timer
  - 32-byte User RAM

Ordering Information appears at end of data sheet.

19-101203; Rev 1; 4/22

Simplified Block Diagram



Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground .....-0.3V to +6V

Operating Temperature Range .....-40°C to +85°C

Junction Temperature.....+125°C

Storage Temperature Range ..... -55°C to +125°C

Soldering Temperature (Reflow) ..... 260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12-WLP

PACKAGE CODE	W121P1+1
Outline Number	*21-100554*
Land Pattern Number	Refer to *Application Note 1891*
Four Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	72.82°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

10-TDFN

PACKAGE CODE	T1033+1C
Outline Number	*21-0137*
Land Pattern Number	*90-0003*
Single Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	54°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W
Four Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W

Electrical Characteristics

(VCC = +1.1V to +5.5V,T_A = -40°C to +85°C unless otherwise noted. = Typical values at VCC = +3.0V, T_A = +25°C unless otherwise noted. Limits are 100% tested at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Timekeeping Supply Voltage Range	V_{CC}	(*Note 3*)		1.1		5.5	V
Interface Supply Voltage Range	V_{CCIO}	Full Operation		1.62		5.5	V
Minimum Initial Power-On Voltage	$V_{CC(POR)}$				1.7		V
Timekeeping Current	I_{CCT}	(*Note 4*)	V_{CC} = +1.1V		65	650	nA
			V_{CC} = +3.0V		65	650	
			V_{CC} = +5.5V		70	700	
Maximum Supply Power-Up Slew Rate	T_{VCCR}				5		V/ms
Maximum Supply Switchover Slew Rate	T_{VCCF}				0.5		V/ms
BATTERY BACKUP AND THRESHOLD							
Timekeeping Backup Voltage Range	V_{BAT}			1.1		5.5	V
Power Fail Threshold Voltage	V_{PF}	PFVT = 0			1.55		V
		PFVT = 1			2		
Timekeeping Battery Current	I_{BATT}	(*Note 4*)	V_{BAT} = +1.1V		65	650	nA
			V_{BAT} = +3.0V		65	650	
			V_{BAT} = +5.5V		70	700	
Trickle-Charge Current-Limiting Resistance	R1				3.3		kΩ
	R2				6.4		
	R3				11.3		
Minimum Battery Voltage for V_{CC} to V_{BAT} Switch (Auto Mode)	V_{BAT_SW}	V_{CC} < V_{PF} and V_{CC} < V_{BAT_SW}			1.5		V
SCHMITT TRIGGER INPUT (DIN)							
Logic 1 Input	V_{IH}	(*Note 14*)	V_{CC_INT} = 1.8 to 5.5V	0.7 x V_{CC_INT}		V_{CC_INT} + 0.3	V
			V_{CC_INT} = 1.62V	0.75 x V_{CC_INT}		V_{CC_INT} + 0.3	
Logic 0 Input	V_{IL}	(*Note 14*)	V_{CC_INT} = 1.8 to 5.5V	-0.3		0.3 x V_{CC_INT}	V
			V_{CC_INT} = 1.62V	-0.3		0.25 x V_{CC_INT}	
Input Leakage	I_{LI}			-0.1		+0.1	µA
LOGIC INPUTS AND OUTPUTS							

(VCC = +1.1V to +5.5V,T_A = -40°C to +85°C unless otherwise noted. = Typical values at VCC = +3.0V, T_A = +25°C unless otherwise noted. Limits are 100% tested at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic 1 Input	V_{IH}	VCC = 1.62V	0.75 x V_{CC}		V_{CC} + 0.3	V
		VCC = 1.8V to 5.5V	0.7 x V_{CC}		V_{CC} + 0.3	
Logic 0 Input	V_{IL}	VCC = 1.62V	-0.3		0.25 x V_{CC}	V
		VCC = 1.8V to 5.5V	-0.3		0.3 x V_{CC}	
Input Leakage (SCL)	I_{IL}	V_{CC} ≥ 1.62V	-0.1		+0.1	µA
Output Leakage (SDA, $\overline{INTA}$, $\overline{INTB}$/CLKOUT)	I_O	V_{CC} ≥ 1.62V	-1		+1	µA
Output Logic 0 (SDA, $\overline{INTA}$, $\overline{INTB}$, CLKOUT)	I_{OL}	V_{OL} = +0.4V, V_{CC} ≥ 1.62V	2			mA
AC CHARACTERISTICS (V_{CC} = +1.62V to +5.5V)						
SCL Clock Frequency	f_{SCL}	(*Note 5*)	10		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(*Note 6*)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(*Note 7*, *Note 8*)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	V_{CC} = 3V (*Note 9*)	100			ns
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Minimum Rise Time of Both SDA and SCL Signals	t_{RMIN}	(*Note 10*)		20 + 0.1C_B		ns
Maximum Rise Time of Both SDA and SCL Signals	t_{RMAX}			300		ns
Minimum Fall Time for Both SDA and SCL Signals	t_{FMIN}	(*Note 10*)		20 + 0.1C_B		ns
Maximum Fall Time for Both SDA and SCL Signals	t_{FMAX}			300		ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs

(VCC = +1.1V to +5.5V,T_A = -40°C to +85°C unless otherwise noted. = Typical values at VCC = +3.0V, T_A = +25°C unless otherwise noted. Limits are 100% tested at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Capacitive Load for Each Bus Line	C_B	(*Note 10*)		400		pF
I/O Capacitance	$C_{I/O}$	(*Note 11*)		10		pF
SCL Spike Suppression	t_{SP}	(*Note 11*)		110		ns
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(*Note 12*)		0.5	2	ms
Timeout Interval	$t_{TIMEOUT}$	(*Note 13*)	25		35	ms

Note 1: Limits at -40°C and +85°C are guaranteed by design and characterization; not production tested.

Note 2: Voltage referenced to ground.

Note 3: Timekeeping function is active through this range. I^2C and other I/O functions are not active below $V_{CCIO(min)}$.

Note 4: Specified with I^2C bus inactive. Oscillator (timekeeping function) operational. (CLKOEN = 0).

Note 5: The minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface if SCL is held low for $t_{TIMEOUT}$.

Note 6: After this period, the first clock pulse is generated.

Note 7: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 8: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 9: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250$ns before the SCL line is released.

Note 10: C_B is the total capacitance of one bus line, including all connected devices, in pF.

Note 11: Guaranteed by design; not 100% production tested.

Note 12: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over V_{CC} range.

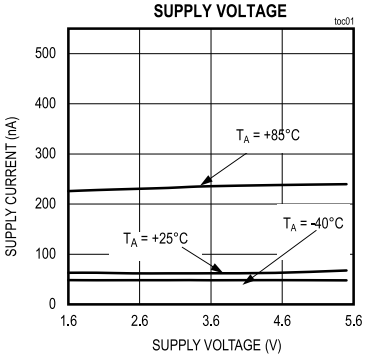
Note 13: The device I^2C interface is in reset state and can receive a new START condition when SCL is held low for at least $t_{TIMEOUTMAX}$. Once the device detects this condition, the SDA output is released. The oscillator must be running for this function to work.

Note 14: V_{CC_INT} is the Active Internal supply. V_{CC_INT} = VBAT when VCC < VPF and VCC < VBAT in auto mode (*Table 1*).

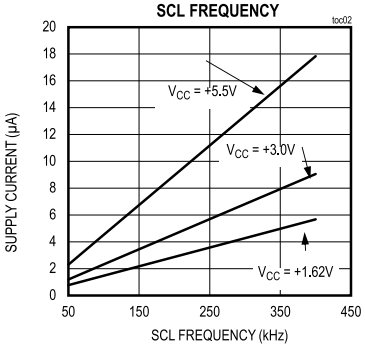
Typical Operating Characteristics

V_{CC} = 3V; T_A = +25°C, unless noted otherwise (T_A = +25°C, unless otherwise noted.)

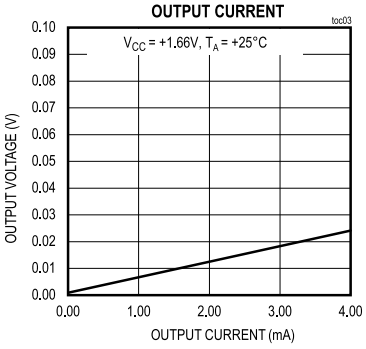
I_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE



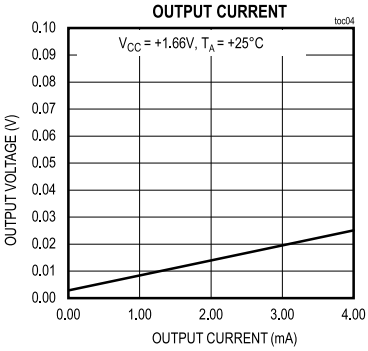
POWER SUPPLY CURRENT vs. SCL FREQUENCY



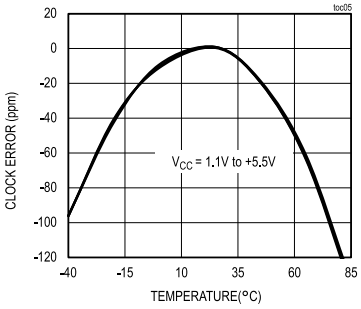
$\overline{INTA}$ OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT



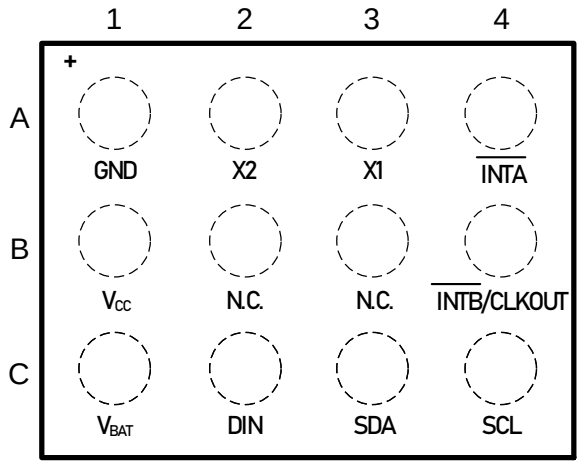
$\overline{INTB}$/CLKOUT OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT



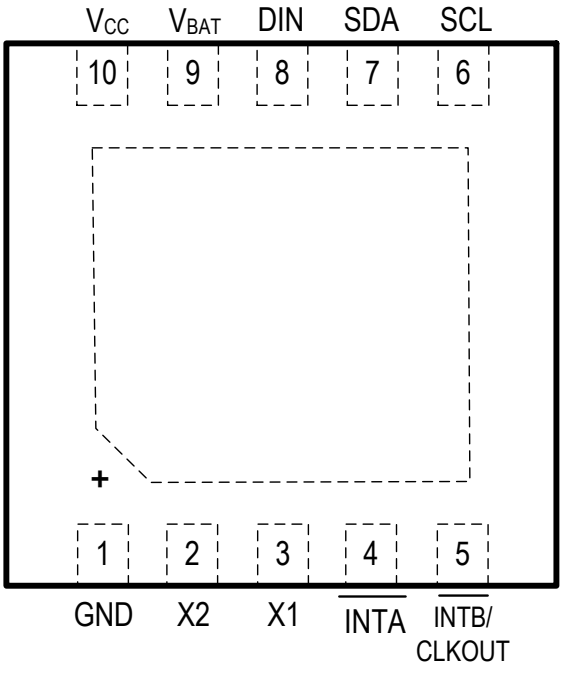
CLOCK ERROR vs. TEMPERATURE



Pin Configuration



12 WLP (1.26mm x 1.66mm)



10-TDFN (3mm x 3mm)

Pin Description

PIN		NAME	FUNCTION
WLP	TDFN		
A1	1	GND	Ground Connection
A2	2	X2	Second Crystal Input for an External 32.768kHz Crystal. See the *Oscillator Circuit and Clock Accuracy* section for recommended external crystal parameters.
A3	3	X1	First Crystal Input for an External 32.768kHz Crystal. See the *Oscillator Circuit and Clock Accuracy* section for recommended external crystal parameters.
A4	4	$\overline{\text{INTA}}$	Active-Low Interrupt Output. This pin is used to output an alarm interrupt. It is an open-drain pin and requires an external pullup resistor. If not used, connect this pin to ground. See *Table 2*.
B4	5	$\overline{\text{INTB}}$/CLK OUT	Square-Wave Clock or Active-Low Interrupt Output. This pin is used to output a programmable square wave or an alarm interrupt signal. This is an open-drain output and requires an external pullup resistor. If not used, connect this pin to ground. See *Table 2*.
C4	6	SCL	Serial-Clock Input. SCL is used to synchronize data movement on the serial interface.
C3	7	SDA	Serial-Data Input/Output. SDA is the input/output pin for the I^2C serial interface. The SDA pin is open-drain and requires an external pullup resistor.
C2	8	DIN	Digital SCHMITT TRIGGER Input. Connect to ground if not used.
C1	9	VBAT	Backup Battery Input and Trickle Charger Output. Connect to GND when backup battery is not used.
B1	10	VCC	Supply Voltage
B2, B3		N.C.	Not Connected.

Detailed Description

Clock/Calendar

The time and calendar information are obtained by reading the appropriate I2C registers. The time and calendar data are set or initialized by writing to the appropriate time/date registers. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The century bit (bit 7 of the Month register) is toggled when the Years register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. A write to any of clock/calendar registers updates the clock/calendar after a 3ms window.

I2C Interface

The I2C interface is guaranteed to operate when VCC is between 1.62V and 5.5V. The I2C interface is accessible whenever VCC is at a valid level. To prevent invalid device operation, the I2C interface should not be accessed when VCC is below +1.62V. The slave address is defined as the seven most significant bits (MSBs) sent by the master after a START condition. The address is 1101000 (or 0xD0, left justified with LSB set to 0). The eighth bit is used to define a write or read operation. If a microcontroller connected to the MAX31331 resets during I2C communication, it is possible that the microcontroller and the MAX31331 could become unsynchronized. In such scenarios, the timeout feature in MAX31331 can be used to reset the I2C slave controller if the SCL is held low for >$t_{TIMEOUT}$. After a loss of communication, if the microcontroller initiates a new I2C transaction, the MAX31331's I2C state machine is reset.

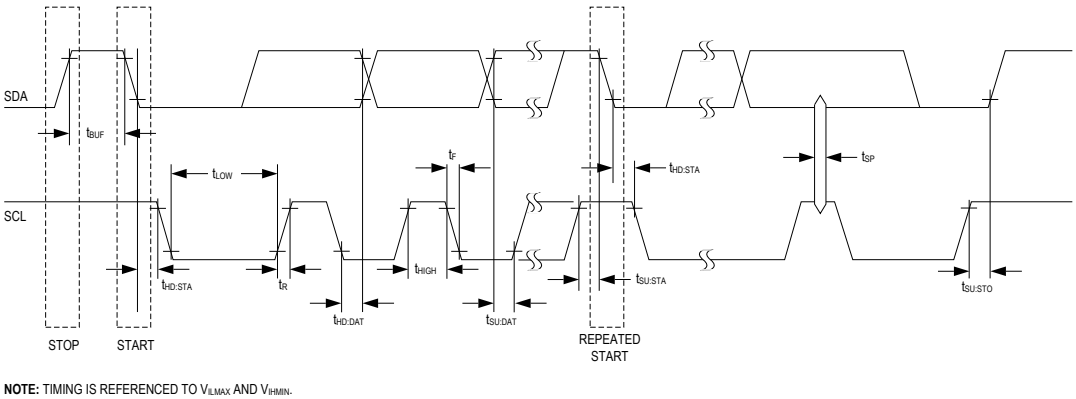


Figure 1. I2C Timing Diagram

Oscillator Circuit and Clock Accuracy

The MAX31331 uses an external 32.768kHz crystal. The oscillator circuit does not require any external components to operate. This also enables the use of many 32.768kHz crystals regardless of the loading (CL) spec. Crystal with minimum Quality Factor of 9000 must be used for sustaining oscillations. After the oscillator is enabled, the startup time of the oscillator circuit is usually less than 1 second.

It is recommended to minimize the trace lengths from the crystal to the X1/X2 pins of MAX31331 and keep them away from any nearby ground plane to minimize the parasitic capacitance. Also, keep any other high-speed clock routings including signal from $\overline{\text{INTB}}$/CLKO pin far away from these X1/X2 pins to reduce coupling effect which can degrade the oscillator signal integrity. *Figure 2* shows the recommended PCB layout for the crystal and oscillator.

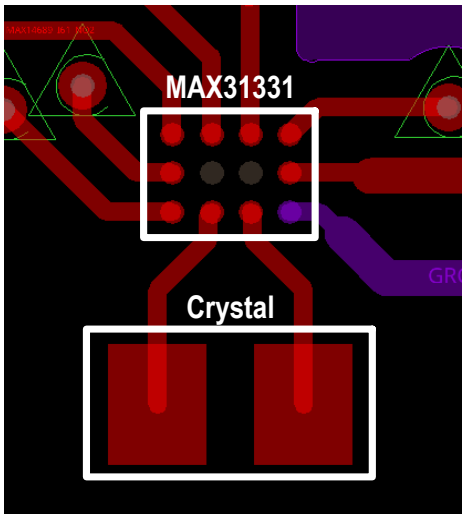


Figure 2. PCB Layout Example

The accuracy of the MAX31331 depends on the parallel resonant frequency of the crystal used, which is typically above the nominal 32.768kHz. The device includes a fractional divider circuit that can correct the typical accuracy close to 0ppm. The MAX31331 is factory-trimmed to ensure a typical accuracy of ±20ppm with the NDK NX2012SA 6pF crystal, which is also used on the MAX31331SHLD evaluation board. As stated above, any other suitable crystal can be used instead. Due to the nature of the oscillator and the nature of quartz blanks inside different crystals, the accuracy observed with other crystals may be off by 10 to 100's of ppm. The MAX31331 provides an option to digitally correct the clock accuracy using the OFFSET_HIGH (1Dh) and OFFSET_LOW (1Eh) registers. These registers enable the user to measure and enter the absolute error. The digital logic then calculates the required compensation and corrects the accuracy with a resolution of 0.477ppm. Follow the steps to measure and correct the clock accuracy on your board.

1. Power on the MAX31331 and write 0x07 to the RTC_CONFIG2 (04h) register to enable the uncorrected 32kHz output clock.
2. Measure the clock frequency on $\overline{\text{INTB}}$/CLKO pin using a frequency counter and record it as MEAS.
3. Calculate uncorrected crystal accuracy in ppm as: ACC = $\frac{(MEAS - 32{,}768) \times 10^6}{32{,}768}$
4. Calculate the offset value as: OFFSET = int{ACC/0.477}.
5. Split the final 16-bit OFFSET value and enter the upper eight bits into the OFFSET_HIGH register and the lower eight bits into the OFFSET_LOW register.
6. The new offset correction starts taking effect after the OFFSET_LOW byte is written.

The new offset correction remains valid as long as there is power source (VCC or VBAT) provided. The offset registers default to a factory-trimmed value at every POR event.

Power Management

The MAX31331 features a backup battery voltage pin (VBAT) in addition to the primary supply voltage pin (VCC). Initial power-up should always be performed on the VCC domain, and this rail is expected to be equal to or higher than VCC(POR) = 1.7V. This ensures a successful power-on-reset (POR) function. If the VCC rail stays below 1.7V (but above 1.62V) during the initial power-up, an external I^2C master can communicate with the MAX31331, but successful operation is not guaranteed because POR was not achieved.

The MAX31331 has a power management function which monitors supply voltage on VCC and backup battery voltage on VBAT, and then determines which source to use as internal supply. There is a PFAIL interrupt flag status bit in the register map to indicate the power fail condition. The VBAT pin should be connected to the backup battery; if there is no backup battery, VBAT should be tied to ground.

Power management control bits PWR_MGMT[1:0] (register 1Ah) are used as follows; for the Power Management Auto and Trickle Charger mode, a “power fail voltage” can be programmed to 1.55V (default) or 2V. MAX31331 switches from the backup battery to the internal power supply if and only if the main supply VCC is lower than both the power fail voltage and the backup battery voltage (and the backup battery voltage is higher than VBAT_SW = 1.5V). Otherwise, VCC remains as the main supply. There is an PFAIL interrupt flag status bit in the STATUS (00h) register that can be used as a power fail flag. The PFAIL interrupt flag monitors the VCC supply and is set when VCC falls below the power fail threshold voltage.

Table 1. Power Management

EN_TRICKLE	VBACK_SEL	MANUAL_SEL	MODE OF OPERATION	
1	x	0	**Power Management Auto and Trickle Charger On**	
			Supply Condition	Active Supply
			VCC < VPF, VCC < VBAT	VBAT
			VCC < VPF, VCC > VBAT	VCC
			VCC > VPF, VCC < VBAT	VCC
			VCC > VPF, VCC > VBAT	VCC
1	0	1	Power Management Manual and Trickle Charger On Active Supply = VCC	
1	1	1	Power Management Manual and Trickle Charger On Active Supply = VBAT for VBAT > VCC	
0	x	0	**Power Management Auto and Trickle Charger Off**	
			Supply Condition	Active Supply
			VCC < VPF, VCC < VBAT	VBAT
			VCC < VPF, VCC > VBAT	VCC
			VCC > VPF, VCC < VBAT	VCC
			VCC > VPF, VCC > VBAT	VCC
0	0	1	Power Management Manual and Trickle Charger Off Active Supply = VCC	
0	1	1	Power Management Manual and Trickle Charger Off Active Supply = VBAT for VBAT > VCC	

Trickle Charger

The trickle charger is for charging an external super capacitor or a rechargeable battery. The maximum charging current can be calculated as follows:

IMAX = (VCC − VD − VBAT)/R

Where VD is the diode voltage drop, VBAT is the voltage of the battery being charged, and R is the resistance selected in the charging path. As the battery charges, the battery voltage increases and the voltage across the charging path decreases. Therefore, the charging current also decreases.

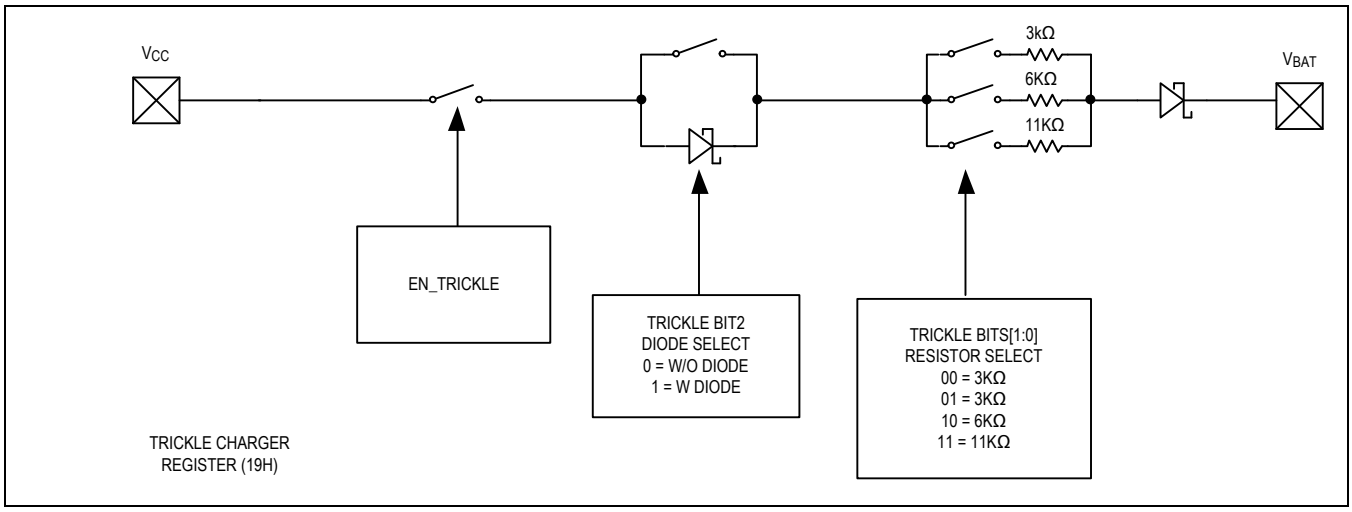


Figure 3. Trickle Charger

Interrupt Status and Outputs

When an interrupt is asserted, a corresponding status bit in STATUS (00h) register becomes “1”, and an interrupt output transitions from High to Low. The interrupt status bit and output can be cleared by reading the STATUS (00h) register. See *Table 2* for interrupt configurations.

Table 2. Interrupt Modes

ENCLKO	$\overline{\text{INTA}}$	CLKOUT/$\overline{\text{INTB}}$
0	$\overline{\text{INTA}}$: Alarm2, Timer, Power Fail (PFAIL), Digital interrupt (DIN)	$\overline{\text{INTB}}$: Alarm1
1	$\overline{\text{INTA}}$: Alarm1, Alarm2 Timer, Power Fail (PFAIL), Digital interrupt (DIN)	CLKOUT

Alarms

The MAX31331 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 0Fh–14h. Alarm 2 can be set by writing to registers 15h–17h. The alarms can be programmed by the A1IE and A2IE bits in INT_EN register to activate the INT output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers and bit 6 of Alm1_mon register are mask bits (*Table 2*). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day, date, month, and year alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. *Table 3* and *Table 4* show the possible settings. Configurations not listed in the table result in illogical operation. The DY_DT_MATCH bit (bit 6 of the alarm day/date registers) controls whether the alarm value stored in bits 0–5 of that register represents the day of the week or the date of the month. If DY_DT_MATCH is written to logic 0, the alarm is the result of a match with date of the month. If DY_DT_MATCH is written to logic 1, the alarm is the result of a match with day of the week.

Table 3. Alarm 1 Settings

DY/DT	ALARM 1 REGISTER MASK BITS (BIT 7)						ALARM RATE
	A1M6	A1M5	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	1	1	Alarm once a second
X	1	1	1	1	1	0	Alarm when seconds match
X	1	1	1	1	0	0	Alarm when minutes and seconds match
X	1	1	1	0	0	0	Alarm when hours, minutes, and seconds match
0	1	1	0	0	0	0	Alarm when dates, hours, minutes, and seconds match
0	1	0	0	0	0	0	Alarm when months, dates, hours, minutes, and seconds match
0	0	0	0	0	0	0	Alarm when years, months, dates, hours, minutes, and seconds match
1	1	1	0	0	0	0	Alarm when days, hours, minutes, and seconds match

Table 4. Alarm 2 Settings

DY/DT	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	Alarm once per minute (00 seconds of every minute)
X	1	1	1	Alarm when minutes match
X	1	1	0	Alarm when hours and minutes match
X	1	0	0	Alarm when dates, hours, and minutes match
0	0	0	0	Alarm when days, hours, and minutes match
1	0	0	0	Alarm when days, hours, and minutes match

Countdown Timer

The MAX31331 features a countdown timer with a pause function. The timer can be configured by writing into registers TIMER_CONFIG (06h) and TIMER_INIT (19h). The TIMER_INIT register should be loaded with the initial value from which the timer would start counting down. The TIMER_CONFIG register allows these configuration options:

- Select the frequency of the timer using the TFS[1:0] field.
- Start/stop the timer using the TE (Timer Enable) bit.
- Enable/disable the timer repeat function using the TRPT bit. This function reloads and restarts the timer with the same init value once it counts down to zero.
- Pause/resume the countdown at any time when the timer is enabled using the TPAUSE bit (explained as follows).

The timer can be programmed to assert the INT output (see *Table 5*) whenever it counts down to zero. This can be enabled/disabled using the TIE bit in register INT_EN register (01h).

The TPAUSE bit is only valid when TE = 1. This bit must be reset to 0 whenever TE is reset to 0.

Table 5 highlights the steps for various use cases involving TE and TPAUSE.

Typical use cases:

- Countdown timer without pause: Step 1 → Step 2 → Step 1 and so on
- Countdown timer with pause: Step 1 → Step 2 → Step 3a → Step 3b → Step 1 and so on

Table 5. Countdown Timer Sequence

SEQUENCE	TE	TPAUSE	ACTION
Step 1	0	0	Countdown timer is reset, and ready for next countdown operation. Timer_init can be programmed in this state.
Step 2	1	0	Countdown timer starts counting down from the value programmed in Timer_init.
Step 3a (Optional)	1	1	Countdown timer is paused, and is ready to start counting down when TPAUSE is programmed back to '0'. Contents of the countdown timer are preserved in this state.
Step 3b If 3a is true	1	0	Countdown timer is brought out of pause state, and starts counting down from the paused value.
	0	1	Not allowed

Timestamps

The MAX31331 can record and store timestamps when triggered by specific events. Up to four timestamps can be stored in the four banks of timestamp registers (TS0, TS1, TS2, and TS3). Each TS bank contains seven registers for date/time information and one TSx_Flags register to indicate which event triggered this timestamp.

The MAX31331 can be configured to record timestamps on these events:

- Rising/falling edge (configurable) on DIN pin
- Supply switch from VCC to VBAT
- Supply switch from VBAT to VCC
- VBAT voltage drops below VBATLOW level (2V)

The part can either be configured to record only the first four timestamps and not record any subsequent events (TSOW = 0, *Figure 4*) or to keep recording every configured event and only keep the four latest events by overwriting the oldest event each time (TSOW = 1, *Figure 5*).

All the configuration related to timestamps can be found in the TIMESTAMP_CONFIG (05h) register. To start recording timestamps, the TSVLOW, TSPWM, TSDIN, TSOW bits need to be configured as desired and the TSE (timestamp enable) bit should be set to 1. The timestamp banks can be read through I2C by accessing the corresponding register address. The TSR bit can be used to reset all the timestamp banks to 0 and start recording new timestamps again (if TSE = 1). When the timestamp functionality is not used (TSE = 0), all 32 bytes of timestamp registers can be used as user RAM. After setting TSE = 0, write TSR = 1 to ensure RAM functionality.

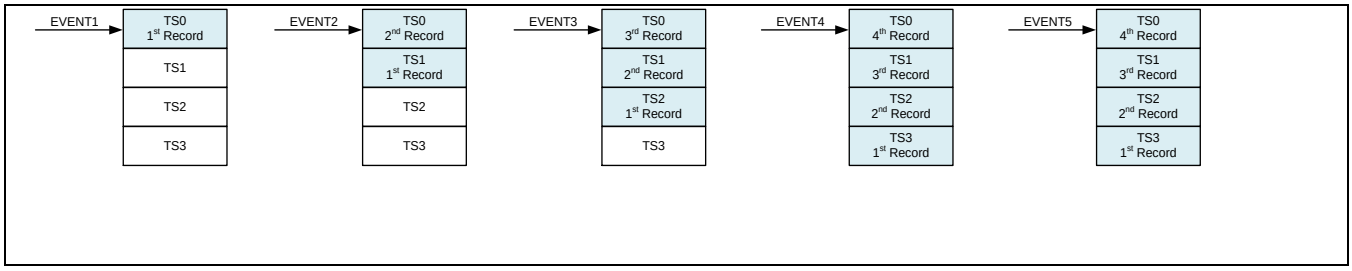


Figure 4. Timestamps with TSOW = 0

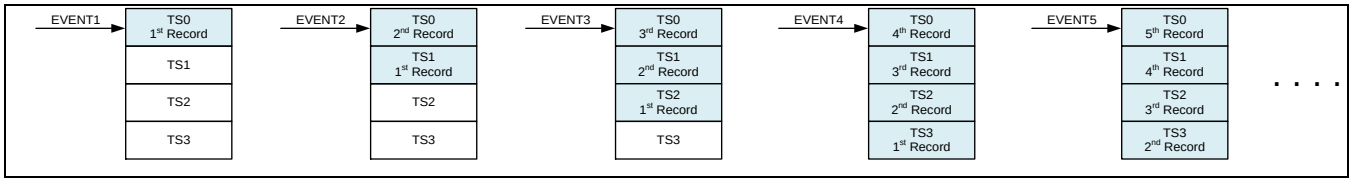


Figure 5. Timestamps with TSOW = 1

Applications Information

Power Supply Decoupling

To achieve the best results when using the device, decouple the VCC and/or VBAT power supplies with 0.1µF and/or 1.0µF capacitors. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance which improves performance and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Using Open-Drain Outputs

The $\overline{INTA}$ and $\overline{INTB}$/CLKO outputs are open-drain and therefore require an external pullup resistor to realize logic-high output levels. Pullup resistor values around 10kΩ are typical.

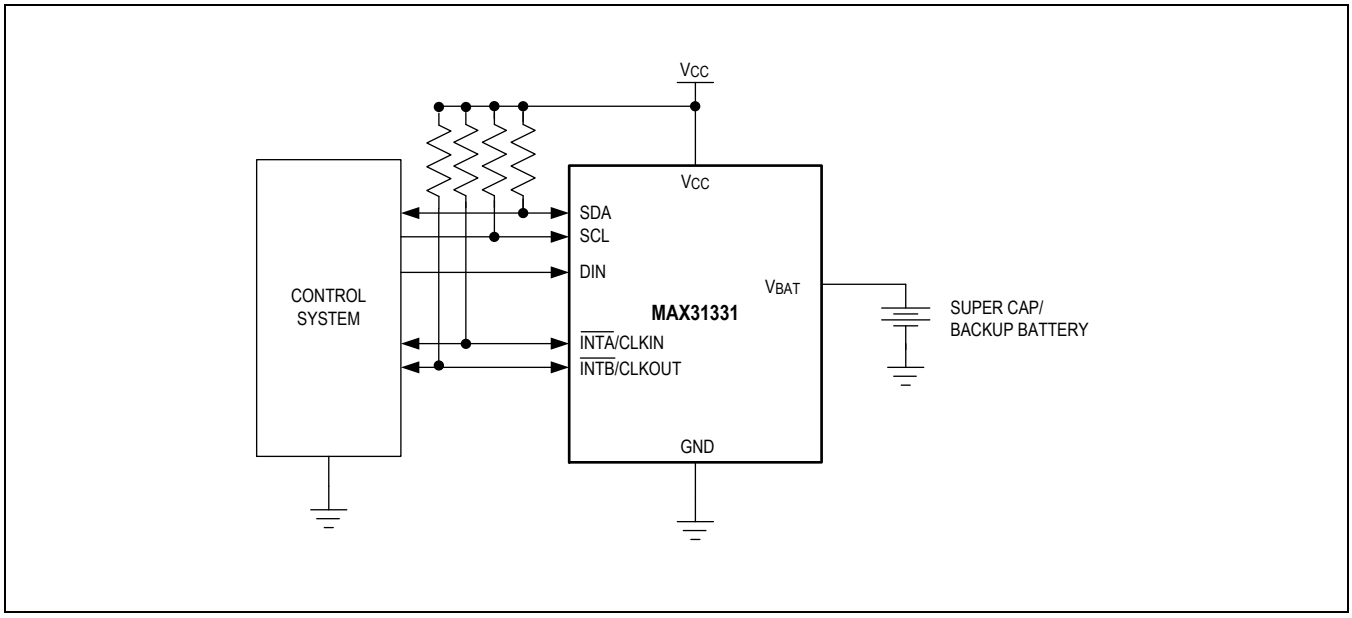
Battery Leakage Current

When the MAX31331 switches from V_{CC} to V_{BAT} supply, the DIN pin buffer internally operates on the V_{BAT} supply rail. If this pin is externally connected to an intermediate voltage level (between 0.7V and V_{BAT} - 0.7V), then there is a high leakage current (tens of microamperes) on the V_{BAT} supply. This scenario can occur when the system V_{CC} rail is discharging and the MAX31331 has switched to V_{BAT} supply, but the DIN pin is pulled up to the V_{CC} rail. Set EN_IO = 0 in RTC_CONFIG1 (03h) register to ensure that the DIN pin is disabled before switching the main supply to V_{BAT} to minimize the leakage current. The DIN pin is automatically enabled when the MAX31331 switches back to V_{CC} supply. Alternatively, the DIN pin can be pulled up to V_{BAT} instead of V_{CC} to ensure minimal negligible leakage when running on V_{BAT}.

SDA and SCL Pullup Resistors

SDA is an open-drain output and requires an external pullup resistor to realize a logic-high level. Because the device does not use clock cycle stretching, a master using either an open-drain output with a pullup resistor or CMOS output driver (push-pull) could be used for SCL.

Typical Application Circuits



Register Map

RC31_REGS

ADDRESS	NAME	MSB							LSB
RTC_REG									
0x00	STATUS[7:0]	PSDECT	OSF	PFAIL	VBATLOW	DIF	TIF	A2F	A1F
0x01	INT_EN[7:0]	–	DOSF	PFAILE	VBATLOWIE	DIE	TIE	A2IE	A1IE
0x02	RTC_RESET[7:0]	–	–	–	–	–	–	–	SWRST
0x03	RTC_CONFIG1[7:0]	–	EN_IO	A1AC[1:0]		DIP	–	I2C_TIMEOUT	EN_OSC
0x04	RTC_CONFIG2[7:0]	–	–	–	–	–	ENCLKO	CLKO_HZ[1:0]	
0x05	TIMESTAMP_CONFIG[7:0]	–	–	TSVLOW	TSPWM	TSDIN	TSOW	TSR	TSE
0x06	TIMER_CONFIG[7:0]	–	–	–	TE	TPAUSE	TRPT	TFS[1:0]	
0x07	SECONDS_1_128[7:0]	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
0x08	SECONDS[7:0]	–	SEC_10[2:0]			SECONDS[3:0]			
0x09	MINUTES[7:0]	–	MIN_10[2:0]			MINUTES[3:0]			
0x0A	HOURS[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
0x0B	DAY[7:0]	–	–	–	–	–	DAY[2:0]		
0x0C	DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x0D	MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x0E	YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x0F	ALM1_SEC[7:0]	A1M1	A1_SEC_10[2:0]			A1_SECONDS[3:0]			
0x10	ALM1_MIN[7:0]	A1M2	A1_MIN_10[2:0]			A1_MINUTES[3:0]			
0x11	ALM1_HRS[7:0]	A1M3	–	A1_HR_20_AM_PM	A1_HR_10	A1_HOUR[3:0]			
0x12	ALM1_DAY_DATE[7:0]	A1M4	A1_DY_DT_MATCH	A1_DATE_10[1:0]		A1_DAY_DATE[3:0]			
0x13	ALM1_MON[7:0]	A1M5	A1M6	–	A1_MONTH_10	A1_MONTH[3:0]			

ADDRESS	NAME	MSB							LSB
0x14	ALM1_YEAR[7:0]	A1_YEAR_10[3:0]				A1_YEAR[3:0]			
0x15	ALM2_MIN[7:0]	A2M2	A2_MIN_10[2:0]			A2_MINUTES[3:0]			
0x16	ALM2_HRS[7:0]	A2M3	–	A2_HR_20_AM_PM	A2_HR_10	A2_HOUR[3:0]			
0x17	ALM2_DAY_DATE[7:0]	A2M4	A2_DY_DT_MATCH	A2_DATE_10[1:0]		A2_DAY_DATE[3:0]			
0x18	TIMER_COUNT[7:0]	TIMER_COUNT[7:0]							
0x19	TIMER_INIT[7:0]	TIMER_INIT[7:0]							
0x1A	PWR_MGMT[7:0]	–	–	–	–	–	–	VBACK_SEL	MANUAL_SEL
0x1B	TRICKLE_REG[7:0]	–	–	–	–	TRICKLE[2:0]			EN_TRICKLE
0x1D	OFFSET_HIGH[7:0]	COMPWORD[15:8]							
0x1E	OFFSET_LOW[7:0]	COMPWORD[7:0]							
TS_RAM_REG									
0x20	TS0_SEC_1_128[7:0]	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
0x21	TS0_SEC[7:0]	–	SEC_10[2:0]			SEC[3:0]			
0x22	TS0_MIN[7:0]	–	MIN_10[2:0]			MIN[3:0]			
0x23	TS0_HOUR[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
0x24	TS0_DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x25	TS0_MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x26	TS0_YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x27	TS0_FLAGS[7:0]	–	–	–	–	VLOWF	VBATF	VCCF	DINF
0x28	TS1_SEC_1_128[7:0]	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
0x29	TS1_SEC[7:0]	–	SEC_10[2:0]			SEC[3:0]			
0x2A	TS1_MIN[7:0]	–	MIN_10[2:0]			MIN[3:0]			
0x2B	TS1_HOUR[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			

ADDRESS	NAME	MSB							LSB
0x2C	TS1_DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x2D	TS1_MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x2E	TS1_YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x2F	TS1_FLAGS[7:0]	–	–	–	–	VLOWF	VBATF	VCCF	DINF
0x30	TS2_SEC_1_128[7:0]	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
0x31	TS2_SEC[7:0]	–	SEC_10[2:0]			SEC[3:0]			
0x32	TS2_MIN[7:0]	–	MIN_10[2:0]			MIN[3:0]			
0x33	TS2_HOUR[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
0x34	TS2_DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x35	TS2_MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x36	TS2_YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x37	TS2_FLAGS[7:0]	–	–	–	–	VLOWF	VBATF	VCCF	DINF
0x38	TS3_SEC_1_128[7:0]	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
0x39	TS3_SEC[7:0]	–	SEC_10[2:0]			SEC[3:0]			
0x3A	TS3_MIN[7:0]	–	MIN_10[2:0]			MIN[3:0]			
0x3B	TS3_HOUR[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
0x3C	TS3_DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x3D	TS3_MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x3E	TS3_YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x3F	TS3_FLAGS[7:0]	–	–	–	–	VLOWF	VBATF	VCCF	DINF

Register Details

STATUS (0x0)

Interrupt Status Register

BIT	7	6	5	4	3	2	1	0
Field	PSDECT	OSF	PFAIL	VBATLOW	DIF	TIF	A2F	A1F
Reset	0b0	0b1	0b0	0x0	0b0	0b0	0b0	0b0
Access Type	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
PSDECT	7	Main supply source indication. This bit is not cleared after successful I²C read.	0x0: Device is running on VCC 0x1: Device is running on VBAT
OSF	6	Oscillator stop flag. This bit is not cleared after successful I²C read.	0x0: Oscillator is running (or DOSF = 1) 0x1: Oscillator has stopped.
PFAIL	5	Power Fail interrupt flag. This bit is cleared automatically after successful I²C read.	0x0: No power fail condition on V_{CC} 0x1: There is a power fail condition on V_{CC}. After an initial power fail condition occurs, if the condition does not persist, this bit can only be cleared by reading the Status register.
VBATLOW	4	VBAT Low interrupt flag. This bit is cleared automatically after successful I²C read.	0x0: VBAT > 2V 0x1: VBAT < 2V
DIF	3	Digital (DIN) interrupt flag. This bit is cleared automatically after successful I²C read.	0x0: DIN interrupt is not triggered. 0x1: DIN interrupt is trigerred.
TIF	2	Timer interrupt flag. This bit is cleared automatically after successful I²C read.	0x0: Countdown timer is still running. 0x1: Countdown timer elapses (COUNT = 0).
A2F	1	Alarm2 interrupt flag. This bit is cleared automatically after successful I²C read.	0x0: RTC time doesn't match the Alarm2 registers. 0x1: RTC time matches the Alarm2 registers.
A1F	0	Alarm1 Interrupt flag. This bit cleared automatically after successful I²C read.	0x0: Set to zero when RTC time doesn't match to alarm1 register. 0x1: Set to 1 when RTC time matches the alarm1 register. When this is set to 1, and A1IE = 1, an interrupt will be generated on pin INTA/INTB.

INT_EN (0x1)

Interrupt Enable Register

BIT	7	6	5	4	3	2	1	0
Field	–	DOSF	PFAILE	VBATLOWIE	DIE	TIE	A2IE	A1IE
Reset	–	0b0	0b0	0x0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DOSF	6	Disable oscillator flag	0x0: Allow the OSF to indicate the oscillator status. 0x1: Disable the oscillator flag, irrespective of the oscillator status.

BITFIELD	BITS	DESCRIPTION	DECODE
PFAILE	5	Power fail Interrupt enable	0x0: Enable PFAIL flag and interrupt 0x1: Disable PFAIL flag and interrupt
VBATLOWIE	4	VBAT Low interrupt enable	0x0: Disable VBAT Low flag and interrupt 0x1: Enable VBAT Low flag and interrupt
DIE	3	Digital (DIN) interrupt enable	0x0: Disable DIN flag and interrupt 0x1: Enable DIN flag and interrupt
TIE	2	Timer interrupt enable	0x0: Disable Timer flag and interrupt 0x1: Enable Timer flag and interrupt
A2IE	1	Alarm2 interrupt enable	0x0: Disable Alarm2 flag and interrupt 0x1: Enable Alarm2 flag and interrupt
A1IE	0	Alarm1 interrupt enable	0x0: Disable Alarm1 flag and interrupt 0x1: Enable Alarm1 flag and interrupt

RTC_RESET (0x2)

RTC Software Reset Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SWRST
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
SWRST	0	Active high software reset bit	0x0: Device is in normal mode. 0x1: Resets the digital block and the I^2C programmable registers except for RAM registers and RTC_reset.SWRST. Oscillator is disabled.

RTC_CONFIG1 (0x3)

RTC Configuration Register 1

BIT	7	6	5	4	3	2	1	0
Field	–	EN_IO	A1AC[1:0]		DIP	–	I2C_TIMEOUT	EN_OSC
Reset	–	0b1	0x0		0b0	–	0b1	0b1
Access Type	–	Write, Read	Write, Read		Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_IO	6	Disables DIN pin when running on VBAT. No effect when running on VCC. Disabling DIN when running	0x0: Disables DIN pin when running on VBAT. 0x1: Enables DIN pin when running on VBAT.

BITFIELD	BITS	DESCRIPTION	DECODE
		on VBAT ensures that there is no leakage current when 0.7V < VCC < VBAT - 0.7V and active supply = VBAT. No leakage is seen on SDA, SCL since they are powered by the VCC rail directly.	
A1AC	5:4	Alarm1 Auto Clear	0x0: Alarm1 flag and interrupt can only be cleared by reading Status register through I^2C 0x1: Alarm1 flag and interrupt are cleared ~10ms after assertion 0x2: Alarm1 flag and interrupt are cleared ~500ms after assertion 0x3: Alarm1 flag and interrupt are cleared ~5s after assertion. This option should not be used when Alarm1 is set to OncePerSec repetition rate.
DIP	3	Digital (DIN) interrupt polarity	0x0: Interrupt triggers on falling edge of DIN input. 0x1: Interrupt triggers on rising edge of DIN input.
I2C_TIMEOUT	1	I^2C timeout enable	0x0: Disables I^2C timeout 0x1: Enables I^2C timeout
EN_OSC	0	Active-high enable for the crystal oscillator	0x0: Disable oscillator 0x1: Enable oscillator

RTC_CONFIG2 (0x4)

RTC Configuration Register 2

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	ENCLKO	CLKO_HZ[1:0]	
Reset	–	–	–	–	–	0b0	0x3	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ENCLKO	2	CLKOUT enable	0x0: Sets $\overline{INTB}$/CLKOUT pin as $\overline{INTB}$ (interrupt). Alarm1 interrupt occurs on $\overline{INTB}$ pin. 0x1: Sets $\overline{INTB}$/CLKOUT pin as CLKO (clock output). Alarm1 interrupt occurs on $\overline{INTA}$ pin.
CLKO_HZ	1:0	Set output clock frequency on $\overline{INTB}$/CLKOUT pin	0x0: 1 Hz 0x1: 64 Hz 0x2: 1.024 kHz 0x3: 32kHz (uncompensated)

TIMESTAMP_CONFIG (0x5)

Timestamp Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	TSVLOW	TSPWM	TSDIN	TSOW	TSR	TSE
Reset	–	–	0x0	0b0	0b0	0b1	0x0	0b0

Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read, Pulse	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TSVLOW	5	Record Timestamp on VBATLOW detection	0x0: Disable 0x1: Enable
TSPWM	4	Record Timestamp on power supply switch (VCC ↔ VBAT)	0x0: Disable 0x1: Enable
TSDIN	3	Record Timestamp on DIN transition. Polarity controlled by DIP bitfield in RTC_Config1 register.	0x0: Disable 0x1: Enable
TSOW	2	Timestamp Overwrite	0x0: 4 Timestamps are recorded (TS0 → ... → TS3). Latest timestamp is always stored in the TS0 bank. Further TS trigger events do not record timestamps. Reset TS block using TSR bit to clear all timestamps and start recording new TS again. 0x1: More than four timestamps are recorded by overwriting oldest timestamp. Latest timestamp is always stored in the TS0 bank; earliest timestamp is stored in the TS3 bank. Reset using TSR bit to clear all timestamps and start recording again.
TSR	1	Timestamp Registers Reset	0x0: No effect 0x1: All Timestamp registers are reset to 0x00. If TSE = 1, timestamp recording starts again.
TSE	0	Timestamp Enable	0x0: Timestamp function disabled. All Timestamp registers can be used as user RAM. Timestamp block needs to be reset using TSR bit if these registers are used as user RAM. 0x1: Timestamp function enabled.

TIMER_CONFIG (0x6)

Countdown Timer Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	TE	TPAUSE	TRPT	TFS[1:0]	
Reset	–	–	–	0b0	0b0	0b1	0b00	
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TE	4	Timer enable. Also see TPAUSE field for additional information.	0x0: Timer is reset. New timer countdown value (Timer_Init) can be programmed in this state. Note: In this state, ensure TPAUSE is also programmed to 0, if TPAUSE was set to 1 earlier. 0x1: Timer starts counting down from the value programmed in Timer_Init.
TPAUSE	3	Timer Pause. This field is valid only when TE = 1. When TE is programmed to 0, this field must also be reset to 0.	0x0: Timer continues to count down from the paused count value as per programming. 0x1: Timer is paused, and the count value is retained. When this bit is reset back to 0, count down continues from the paused value.

BITFIELD	BITS	DESCRIPTION	DECODE
TRPT	2	Timer repeat mode. Controls the timer interrupt function.	0x0: Countdown timer halts once it reaches zero 0x1: Countdown timer reloads the value from the Timer_Init register upon reaching zero and restarts counting.
TFS	1:0	Timer frequency selection	0x0: 1024 Hz 0x1: 256 Hz 0x2: 64 Hz 0x3: 16 Hz

SECONDS_1_128 (0x7)

1/128 Seconds Register

BIT	7	6	5	4	3	2	1	0
Field	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
_1_2s	6	
_1_4s	5	
_1_8s	4	
_1_16s	3	
_1_32s	2	
_1_64s	1	
_1_128s	0	

SECONDS (0x8)

Seconds Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SECONDS[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	RTC seconds in multiples of 10
SECONDS	3:0	RTC seconds value

MINUTES (0x9)

Minutes Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MINUTES[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	RTC minutes in multiples of 10
MINUTES	3:0	RTC minutes value

HOURS (0xA)

Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION	DECODE
F_24_12	6	Sets RTC in 12-hr or 24-hr format	0x0: 24 hour format (Hours counts from 0-23) 0x1: 12 hour format (Hours counts from 1-12)
HR_20_AM_PM	5	In 12 hr format, this works as the AM/PM indicator. In 24 hr format, it is the RTC hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format. 0x1: Indicates PM in 12-hr format.
HR_10	4	RTC hours in multiples of 10 (BCD)	
HOUR	3:0	RTC hours value (BCD)	

DAY (0xB)

Day Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DAY[2:0]		
Reset	–	–	–	–	–	0b001		
Access Type	–	–	–	–	–	Write, Read, Dual		

BITFIELD	BITS	DESCRIPTION
DAY	2:0	RTC days

DATE (0xC)

Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	DATE_10[1:0]		DATE[3:0]			
Reset	–	–	0b00		0x1			
Access Type	–	–	Write, Read, Dual		Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	RTC date in multiples of 10 (BCD)
DATE	3:0	RTC date (BCD)

MONTH (0xD)

Month Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0b0	–	–	0b0	0x1			
Access Type	Write, Read, Dual	–	–	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION	DECODE
CENTURY	7	Century bit	0x0: Year is in 21st century 0x1: Year is in 22nd century

BITFIELD	BITS	DESCRIPTION	DECODE
MONTH_10	4	RTC month in multiples of 10 (BCD)	
MONTH	3:0	RTC months (BCD)	

YEAR (0xE)

Year Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	YEAR_10[3:0]				YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read, Dual				Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	RTC year multiples of 10 (BCD)
YEAR	3:0	RTC years (BCD)

ALM1_SEC (0xF)

Alarm1 Seconds Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M1	A1_SEC_10[2:0]			A1_SECONDS[3:0]			
Reset	0b0	0b000			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M1	7	Alarm1 mask bit for seconds
A1_SEC_10	6:4	Alarm1 seconds in multiples of 10
A1_SECONDS	3:0	Alarm1 seconds

ALM1_MIN (0x10)

Alarm1 Minutes Configuration Register

BIT	7	6	5	4	3	2	1	0

Field	A1M2	A1_MIN_10[2:0]	A1_MINUTES[3:0]
Reset	0b0	0b000	0x0
Access Type	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
A1M2	7	Alarm1 mask bit for minutes
A1_MIN_10	6:4	Alarm1 minutes in multiples of 10
A1_MINUTES	3:0	Alarm1 minutes

ALM1_HRS (0x11)

Alarm1 Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M3	–	A1_HR_20_AM_PM	A1_HR_10	A1_HOUR[3:0]			
Reset	0b0	–	0b0	0b0	0x0			
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A1M3	7	Alarm1 mask bit for hours	
A1_HR_20_AM_PM	5	In 12 hr format, this works as the AM/PM indicator. In 24 hr format, it is the Alarm1 hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format. 0x1: Indicates PM in 12-hr format.
A1_HR_10	4	Alarm1 hours in multiples of 10	
A1_HOUR	3:0	Alarm1 hours	

ALM1_DAY_DATE (0x12)

Alarm1 Day/Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M4	A1_DY_DT_MATCH	A1_DATE_10[1:0]		A1_DAY_DATE[3:0]			
Reset	0b0	0b0	0b00		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A1M4	7	Alarm1 mask bit for day/date	
A1_DY_DT_MATCH	6		0x0: Alarm when date match 0x1: Alarm when day match
A1_DATE_10	5:4	Alarm1 date in multiples of 10	
A1_DAY_DATE	3:0	Alarm1 day/date	

ALM1_MON (0x13)

Alarm1 Month Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M5	A1M6	–	A1_MONTH_10	A1_MONTH[3:0]			
Reset	0b0	0b0	–	0b0	0x0			
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M5	7	Alarm1 mask bit for month
A1M6	6	Alarm1 mask bit for year
A1_MONTH_10	4	Alarm1 months in multiples of 10
A1_MONTH	3:0	Alarm1 months

ALM1_YEAR (0x14)

Alarm1 Year Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1_YEAR_10[3:0]				A1_YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
A1_YEAR_10	7:4	Alarm1 year in multiples of 10

BITFIELD	BITS	DESCRIPTION
A1_YEAR	3:0	Alarm1 years

ALM2_MIN (0x15)

Alarm2 Minutes Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A2M2	A2_MIN_10[2:0]			A2_MINUTES[3:0]			
Reset	0b0	0b000			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A2M2	7	Alarm2 mask bit for minutes
A2_MIN_10	6:4	Alarm2 minutes in multiples of 10
A2_MINUTES	3:0	Alarm2 minutes

ALM2_HRS (0x16)

Alarm2 Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A2M3	–	A2_HR_20_AM_PM	A2_HR_10	A2_HOUR[3:0]			
Reset	0b0	–	0b0	0b0	0x0			
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A2M3	7	Alarm2 mask bit for hours	
A2_HR_20_AM_PM	5	In 12 hr format, this works as the AM/PM indicator. In 24 hr format, it is the Alarm2 hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format. 0x1: Indicates PM in 12-hr format.
A2_HR_10	4	Alarm2 hours in multiples of 10	
A2_HOUR	3:0	Alarm2 hours	

ALM2_DAY_DATE (0x17)

Alarm2 Day/Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A2M4	A2_DY_DT_MATCH	A2_DATE_10[1:0]		A2_DAY_DATE[3:0]			
Reset	0b0	0b0	0b00		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A2M4	7	Alarm2 mask bit for day/date	
A2_DY_DT_MATCH	6	This bit selects alarm when day match or date match.	0x0: Alarm when date match 0x1: Alarm when day match
A2_DATE_10	5:4	Alarm2 date in multiples of 10	
A2_DAY_DATE	3:0	Alarm2 day/date	

TIMER_COUNT (0x18)

Countdown Timer Value Register

BIT	7	6	5	4	3	2	1	0
Field	TIMER_COUNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TIMER_COUNT	7:0	Count down timer current count value. The current timer value can be read by reading this register.

TIMER_INIT (0x19)

Countdown Timer Initialization Register

BIT	7	6	5	4	3	2	1	0
Field	TIMER_INIT[7:0]							
Reset	0x00							

Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION
TIMER_INIT	7:0	Count down timer initial value. The timer is loaded with the contents of this register when it reaches zero in repeat mode.

PWR_MGMT (0x1A)

Power Management Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VBACK_SEL	MANUAL_SEL
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VBACK_SEL	1	Backup battery select. Require D_MANUAL_SEL = 1 for this bit to have effect. V_{BAT} can only be selected when $V_{CC} < V_{BAT}$.	0x0: Use V_{CC} as supply. 0x1: Use V_{BAT} as supply.
MANUAL_SEL	0	When this bit is low, input control block decides which supply to use. When this bit is high, user can manually select V_{BACKUP} as supply only when V_{CC} is lower than V_{BACKUP}.	0x0: Circuit decides whether to use V_{CC} or V_{BAT} as supply. 0x1: User decides whether to use V_{CC} or V_{BAT} as supply by setting D_VBAT_SEL bit.

TRICKLE_REG (0x1B)

Trickle Charger Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	TRICKLE[2:0]			EN_TRICKLE
Reset	–	–	–	–	0x0			0b0
Access Type	–	–	–	–	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TRICKLE	3:1	Sets the charging path for trickle charger.	0x0: 3kΩ in series with a Schottky diode 0x1: 3kΩ in series with a Schottky diode 0x2: 6kΩ in series with a Schottky diode 0x3: 11kΩ in series with a Schottky diode 0x4: 3kΩ in series with a diode and Schottky diode 0x5: 3kΩ in series with a diode and Schottky diode

BITFIELD	BITS	DESCRIPTION	DECODE
			0x6: 6kΩ in series with a diode and Schottky diode 0x7: 11kΩ in series with a diode and Schottky diode
EN_TRICKLE	0	Trickle charger enable.	0x0: Trickle charger disabled 0x1: Trickle charger enabled

OFFSET_HIGH (0x1D)

Offset Configuration Register High

BIT	7	6	5	4	3	2	1	0
Field	COMPWORD[15:8]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COMPWORD	7:0	Compensation Words (2's complement) provides the option to digitally tune the oscillator output frequency by applying correction pulses. It can be used for accuracy tuning, aging offset, or temperature compensation. Resolution = 0.477ppm If there is no write to these bits, the factory trim values are used instead.

OFFSET_LOW (0x1E)

Offset Configuration Register Low

BIT	7	6	5	4	3	2	1	0
Field	COMPWORD[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COMPWORD	7:0	Compensation Words (2's complement) provides the option to digitally tune the oscillator output frequency by applying correction pulses. It can be used for accuracy tuning, aging offset, or temperature compensation. Resolution = 0.477ppm If there is no write to these bits, the factory trim values are used instead.

TS0_SEC_1_128 (0x20)

BIT	7	6	5	4	3	2	1	0

Field	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	Write, Read	Write, Read	Write, Read, Dual	Write, Read	Write, Read	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
_1_2s	6	
_1_4s	5	
_1_8s	4	RTC seconds in multiples of 10
_1_16s	3	
_1_32s	2	
_1_64s	1	
_1_128s	0	RTC seconds value

TS0_SEC (0x21)

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SEC[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	RTC seconds in multiples of 10
SEC	3:0	RTC seconds in multiples of 10

TS0_MIN (0x22)

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MIN[3:0]			
Reset	–				0x0			
Access Type	–	Write, Read			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	
MIN	3:0	RTC seconds in multiples of 10

TS0_HOUR (0x23)

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION	DECODE
F_24_12	6	Sets RTC in 12-hr or 24-hr format	0x0: 24 hour format (Hours counts from 0-23) 0x1: 12 hour format (Hours counts from 1-12)
HR_20_AM_PM	5	In 12 hr format, this works as the AM/PM indicator. In 24 hr format, it is the RTC hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format. 0x1: Indicates PM in 12-hr format.
HR_10	4	RTC hours in multiples of 10 (BCD)	
HOUR	3:0	RTC seconds in multiples of 10	

TS0_DATE (0x24)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DATE_10[1:0]		DATE[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read		Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	
DATE	3:0	RTC seconds in multiples of 10

TS0_MONTH (0x25)

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0x0	–	–	0x0	0x0			
Access Type	Write, Read	–	–	Write, Read	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
CENTURY	7	
MONTH_10	4	
MONTH	3:0	RTC seconds in multiples of 10

TS0_YEAR (0x26)

BIT	7	6	5	4	3	2	1	0
Field	YEAR_10[3:0]				YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	
YEAR	3:0	RTC seconds in multiples of 10

TS0_FLAGS (0x27)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VLOWF	VBATF	VCCF	DINF
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VLOWF	3	Indicates if this Timestamp was triggered by VLOW detection	0x0: Not triggered by VLOW detection 0x1: Triggered by VLOW detection

BITFIELD	BITS	DESCRIPTION	DECODE
VBATF	2	Indicates if this Timestamp was triggered by VCC → VBAT switch	0x0: Not triggered by VCC → VBAT switch 0x1: Triggered by VCC → VBAT switch
VCCF	1	Indicates if this Timestamp was triggered by VBAT → VCC switch	0x0: Not triggered by VBAT → VCC switch 0x1: Triggered by VBAT → VCC switch
DINF	0	Indicates if this Timestamp was triggered by DIN transition	0x0: Not triggered by DIN 0x1: Triggered by DIN

TS1_SEC_1_128 (0x28)

BIT	7	6	5	4	3	2	1	0
Field	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	Write, Read	Write, Read	Write, Read, Dual	Write, Read	Write, Read	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
_1_2s	6	
_1_4s	5	
_1_8s	4	RTC seconds in multiples of 10
_1_16s	3	
_1_32s	2	
_1_64s	1	
_1_128s	0	RTC seconds value

TS1_SEC (0x29)

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SEC[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	RTC seconds in multiples of 10
SEC	3:0	RTC seconds in multiples of 10

TS1_MIN (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MIN[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	
MIN	3:0	RTC seconds in multiples of 10

TS1_HOUR (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION	DECODE
F_24_12	6	Sets RTC in 12-hr or 24-hr format	0x0: 24 hour format (Hours counts from 0-23) 0x1: 12 hour format (Hours counts from 1-12)
HR_20_AM_PM	5	In 12 hr format, this works as the AM/PM indicator. In 24 hr format, it is the RTC hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format. 0x1: Indicates PM in 12-hr format.
HR_10	4	RTC hours in multiples of 10 (BCD)	
HOUR	3:0	RTC seconds in multiples of 10	

TS1_DATE (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DATE_10[1:0]		DATE[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read		Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	
DATE	3:0	RTC seconds in multiples of 10

TS1_MONTH (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0x0	–	–	0x0	0x0			
Access Type	Write, Read	–	–	Write, Read	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
CENTURY	7	
MONTH_10	4	
MONTH	3:0	RTC seconds in multiples of 10

TS1_YEAR (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	YEAR_10[3:0]				YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	

BITFIELD	BITS	DESCRIPTION
YEAR	3:0	RTC seconds in multiples of 10

TS1_FLAGS (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VLOWF	VBATF	VCCF	DINF
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VLOWF	3	Indicates if this Timestamp was triggered by VLOW detection	0x0: Not triggered by VLOW detection 0x1: Triggered by VLOW detection
VBATF	2	Indicates if this Timestamp was triggered by VCC → VBAT switch	0x0: Not triggered by VCC → VBAT switch 0x1: Triggered by VCC → VBAT switch
VCCF	1	Indicates if this Timestamp was triggered by VBAT → VCC switch	0x0: Not triggered by VBAT → VCC switch 0x1: Triggered by VBAT → VCC switch
DINF	0	Indicates if this Timestamp was triggered by DIN transition	0x0: Not triggered by DIN 0x1: Triggered by DIN

TS2_SEC_1_128 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	Write, Read	Write, Read	Write, Read, Dual	Write, Read	Write, Read	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
_1_2s	6	
_1_4s	5	
_1_8s	4	RTC seconds in multiples of 10
_1_16s	3	
_1_32s	2	

BITFIELD	BITS	DESCRIPTION
_1_64s	1	
_1_128s	0	RTC seconds value

TS2_SEC (0x31)

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SEC[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	RTC seconds in multiples of 10
SEC	3:0	RTC seconds in multiples of 10

TS2_MIN (0x32)

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MIN[3:0]			
Reset	–				0x0			
Access Type	–	Write, Read			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	
MIN	3:0	RTC seconds in multiples of 10

TS2_HOUR (0x33)

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			

Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION	DECODE
F_24_12	6	Sets RTC in 12-hr or 24-hr format	0x0: 24 hour format (Hours counts from 0-23) 0x1: 12 hour format (Hours counts from 1-12)
HR_20_AM_PM	5	In 12 hr format, this works as the AM/PM indicator. In 24 hr format, it is the RTC hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format. 0x1: Indicates PM in 12-hr format.
HR_10	4	RTC hours in multiples of 10 (BCD)	
HOUR	3:0	RTC seconds in multiples of 10	

TS2_DATE (0x34)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DATE_10[1:0]		DATE[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read		Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	
DATE	3:0	RTC seconds in multiples of 10

TS2_MONTH (0x35)

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0x0	–	–	0x0	0x0			
Access Type	Write, Read	–	–	Write, Read	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
CENTURY	7	
MONTH_10	4	
MONTH	3:0	RTC seconds in multiples of 10

TS2_YEAR (0x36)

BIT	7	6	5	4	3	2	1	0
Field	YEAR_10[3:0]				YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	
YEAR	3:0	RTC seconds in multiples of 10

TS2_FLAGS (0x37)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VLOWF	VBATF	VCCF	DINF
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VLOWF	3	Indicates if this Timestamp was triggered by VLOW detection	0x0: Not triggered by VLOW detection 0x1: Triggered by VLOW detection
VBATF	2	Indicates if this Timestamp was triggered by VCC → VBAT switch	0x0: Not triggered by VCC → VBAT switch 0x1: Triggered by VCC → VBAT switch
VCCF	1	Indicates if this Timestamp was triggered by VBAT → VCC switch	0x0: Not triggered by VBAT → VCC switch 0x1: Triggered by VBAT → VCC switch
DINF	0	Indicates if this Timestamp was triggered by DIN transition	0x0: Not triggered by DIN 0x1: Triggered by DIN

TS3_SEC_1_128 (0x38)

BIT	7	6	5	4	3	2	1	0
Field	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	Write, Read	Write, Read	Write, Read, Dual	Write, Read	Write, Read	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
_1_2s	6	
_1_4s	5	
_1_8s	4	RTC seconds in multiples of 10
_1_16s	3	
_1_32s	2	
_1_64s	1	
_1_128s	0	RTC seconds value

TS3_SEC (0x39)

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SEC[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	RTC seconds in multiples of 10
SEC	3:0	RTC seconds in multiples of 10

TS3_MIN (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MIN[3:0]			
Reset	–				0x0			
Access Type	–	Write, Read			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	
MIN	3:0	RTC seconds in multiples of 10

TS3_HOUR (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION	DECODE
F_24_12	6	Sets RTC in 12-hr or 24-hr format	0x0: 24 hour format (Hours counts from 0-23) 0x1: 12 hour format (Hours counts from 1-12)
HR_20_AM_PM	5	In 12 hr format, this works as the AM/PM indicator. In 24 hr format, it is the RTC hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format. 0x1: Indicates PM in 12-hr format.
HR_10	4	RTC hours in multiples of 10 (BCD)	
HOUR	3:0	RTC seconds in multiples of 10	

TS3_DATE (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DATE_10[1:0]		DATE[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read		Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	
DATE	3:0	RTC seconds in multiples of 10

TS3_MONTH (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0x0	–	–	0x0	0x0			
Access Type	Write, Read	–	–	Write, Read	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
CENTURY	7	
MONTH_10	4	
MONTH	3:0	RTC seconds in multiples of 10

TS3_YEAR (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	YEAR_10[3:0]				YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	
YEAR	3:0	RTC seconds in multiples of 10

TS3_FLAGS (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VLOWF	VBATF	VCCF	DINF
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VLOWF	3	Indicates if this Timestamp was triggered by VLOW detection	0x0: Not triggered by VLOW detection 0x1: Triggered by VLOW detection
VBATF	2	Indicates if this Timestamp was triggered by VCC → VBAT switch	0x0: Not triggered by VCC → VBAT switch 0x1: Triggered by VCC → VBAT switch
VCCF	1	Indicates if this Timestamp was triggered by VBAT → VCC switch	0x0: Not triggered by VBAT → VCC switch 0x1: Triggered by VBAT → VCC switch
DINF	0	Indicates if this Timestamp was triggered by DIN transition	0x0: Not triggered by DIN 0x1: Triggered by DIN

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX31331EWC+	-40°C to +85°C	12-WLP
MAX31331EWC+T	-40°C to +85°C	12-WLP
MAX31331TETB+	-40°C to +85°C	10-TDFN
MAX31331TETB+T	-40°C to +85°C	10-TDFN

+Denotes a lead(Pb)-free/ROHS-compliant package

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/22	Release for Market Intro	—
1	4/22	Updated TDFN part numbers in *Ordering Information* table	48

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