

Cross Band Transponder (XBT)

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Date of Last Edit: 12 March 2024

High Level Needs (from Jonathan's email)

- Start with:
 - Single signal path
 - VHF voice signal transponded as a UHF voice signal
- Could be a SDR w/digital radio chip
- Could be analog
- Fit onto a CubeSat board
 - Ideally 2" x 2" area
- Radiation tolerant
 - Avoid CMOS

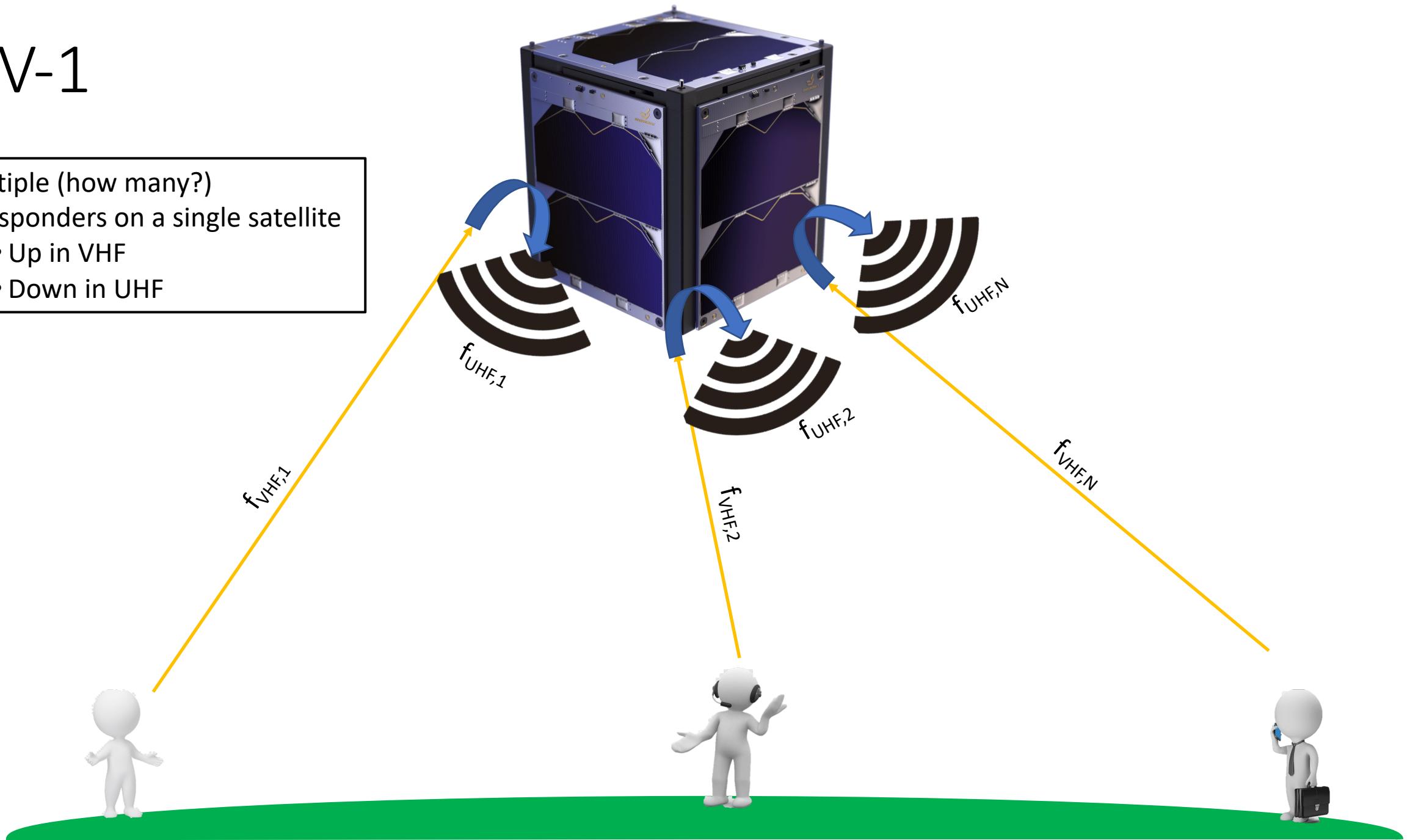
Goals

- Multiple transponders on a single satellite
 - I.e., multiple up frequencies with multiple down frequencies
- Low SWaP-C
- Other desired capabilities?
 - Brainstorm session to build a “wish list”

Concept of Operations (CONOPS)

OV-1

- Multiple (how many?) transponders on a single satellite
 - Up in VHF
 - Down in UHF

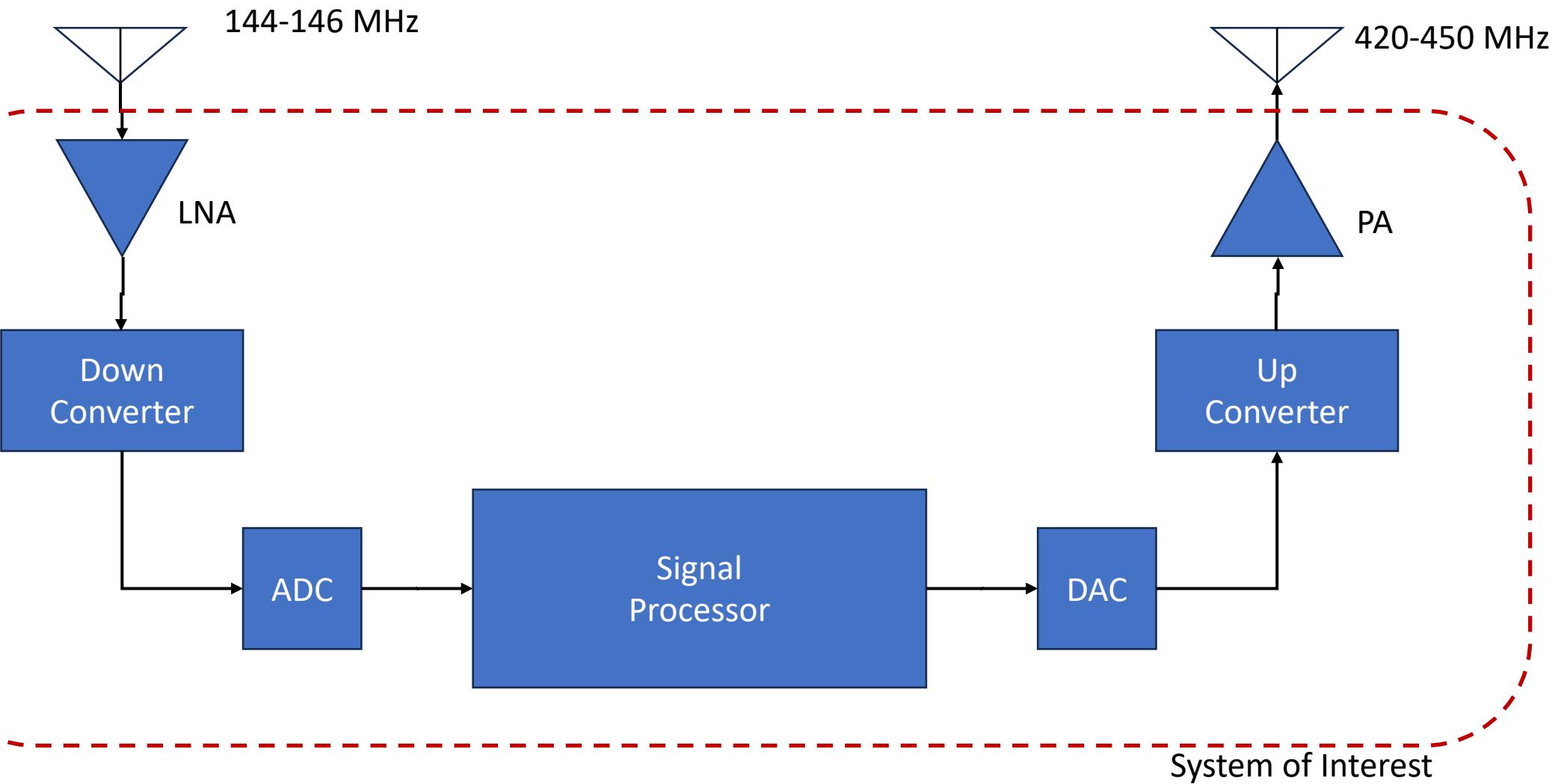


CONOPS

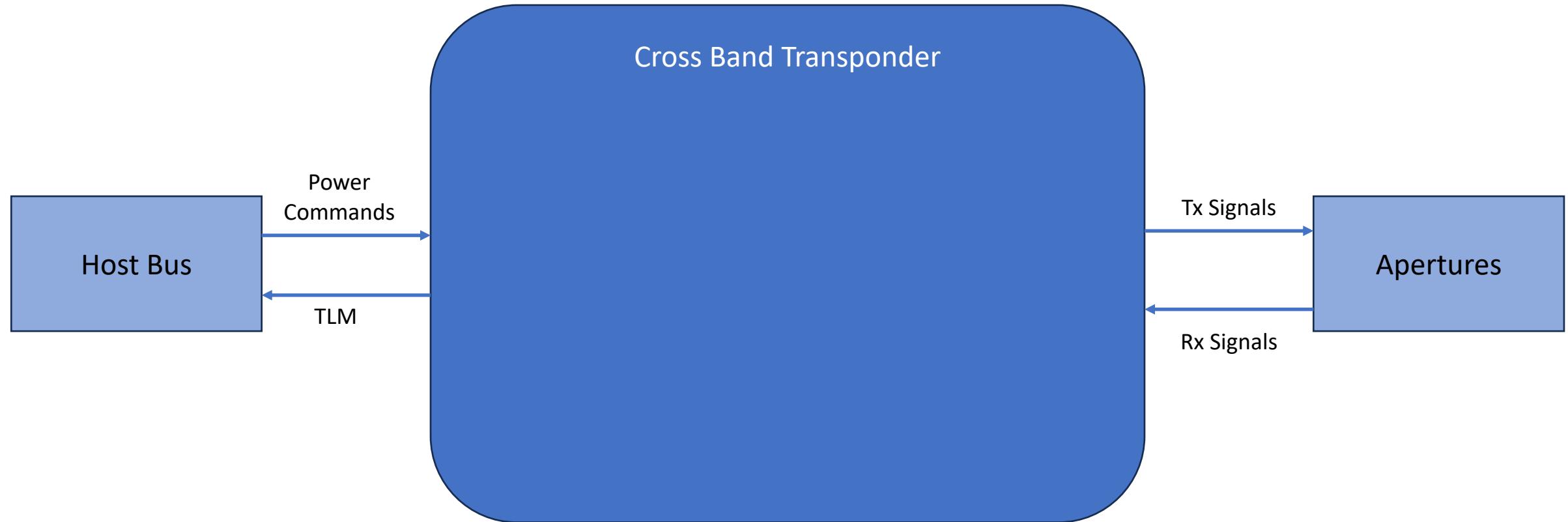
- Main mission:
 - Receive TBD number of VHF signals from aperture
 - Amplify/filter/condition incoming signals for processing
 - Process signals
 - Filter/condition/amplify outgoing signal
 - Transmit UHF signals to aperture
- Other Use Cases:
 - SOH, failure recovery
 - Store and forward?
 - Software updates
 - Different/new/etc. modes

Architecture

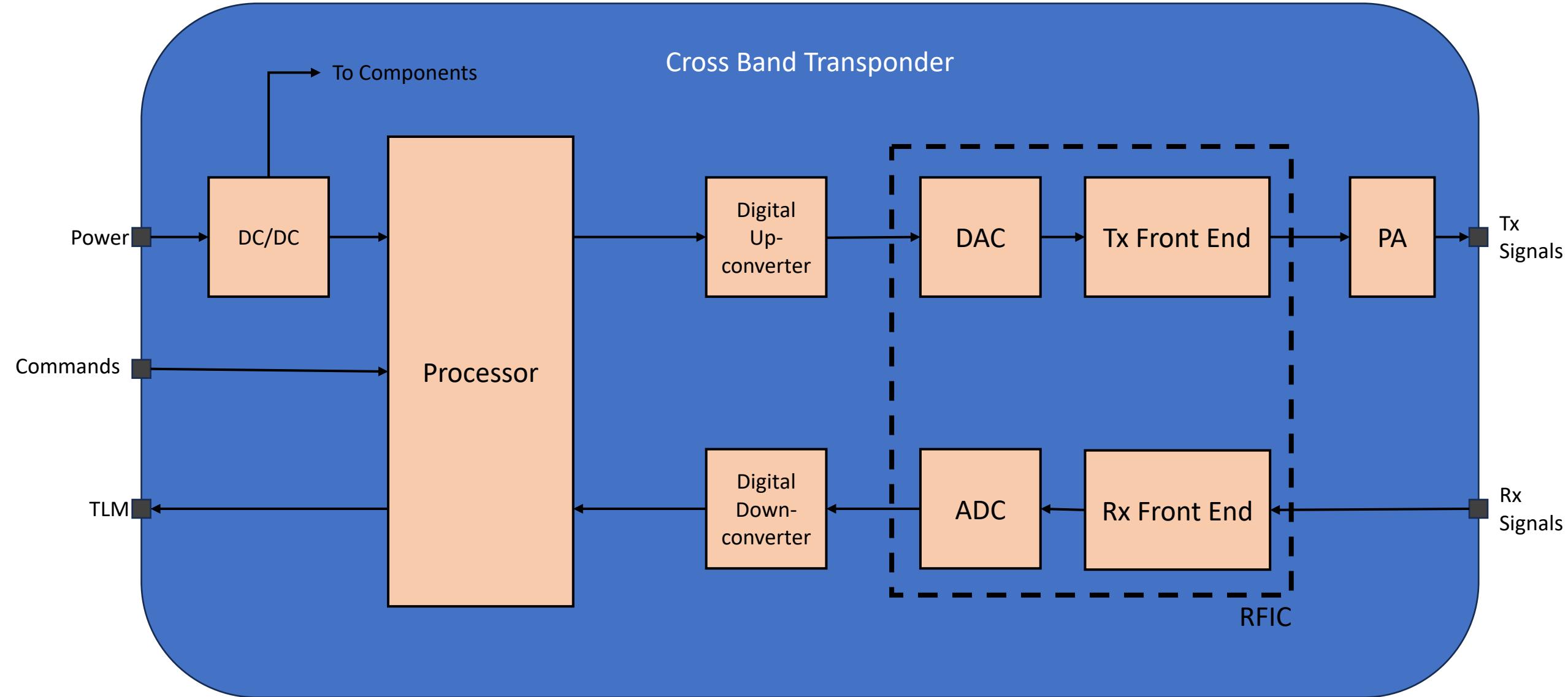
High-Level Block Diagram



Context Diagram



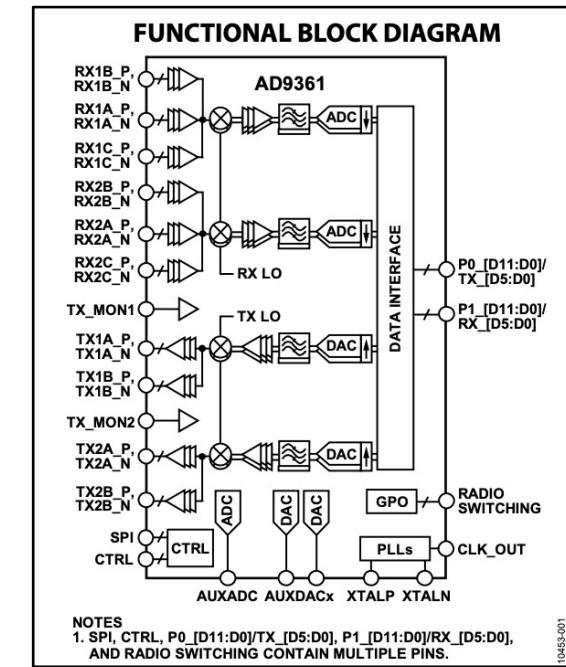
Will the Bus have a comm system for TLM D/L or will the XBT be used?



Reference signal: needed?
(probably) → internal or external?

RFIC

- Functionality needed:
 - Analog receive
 - Amplify
 - Mix with LO to IF
 - ADC
 - DAC
 - Mix with LO to RF
 - Analog transmit
- Baseline: Analog Devices AD9361
 - 12-bit DAC and ADC's
 - TX: 47 MHz to 6.0 GHz, RX: 70 MHz to 6.0 GHz
 - Other options?



From AD9361 Data Sheet

Processor

- Functionality needed:
 - Demodulate signal
 - Shift signal
 - What else..??

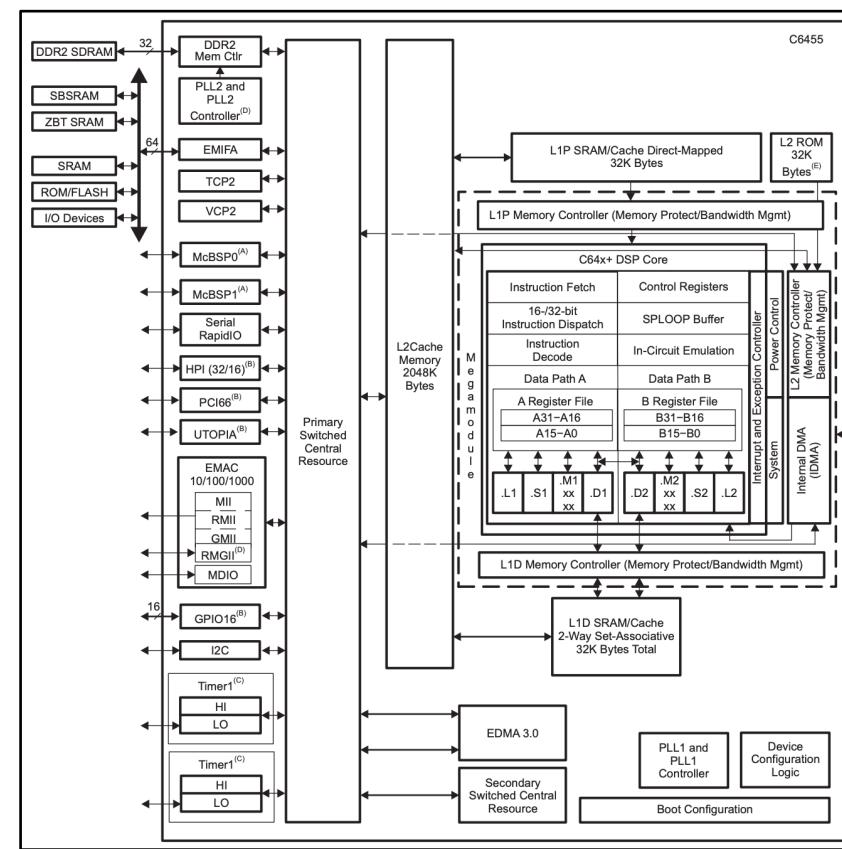
Notes/Questions/Observations:

Processor Exploration – scratch the ASCENT itch

- Prompted a variety of LLM's to brainstorm low power processor options:
 - TI Tiva C Series
 - STMicroelectronics STM32F7 Series
 - Microchip Technology PIC32MX Series
 - NXP Semiconductors i.MX6 Series
 - Espressif Systems ESP32/ESP8266
 - **TI TMS320C6000 Series → see follow-on slide**
 - Xilinx Zynq UltraScale+ MPSoC
 - Analog Devices ADSP-SC58x/ADSP-2158x
 - Microchip dsPIC33CH
 - Renesas R-Car V3H

Processor Option (1 of n)

- TI TMS320C6000 Series
 - High performance DSP w/low power
 - Very Long Instruction Word (VLIW) → efficient parallel processing
 - E.g., TMS320C6455BCTZA
 - -40C to 90C
 - 1 GHz clock rate
 - \$291.15 and 43 in stock (DigiKey)
 - Evaluation board: TMDXEV6455
 - \$1,895.52 and 1 in stock (DigiKey)
 - Radiation-hardened version available → SMJ320C6701-SP



Processor Option (2 of n)

- WIP

Power Amplifier (PA)

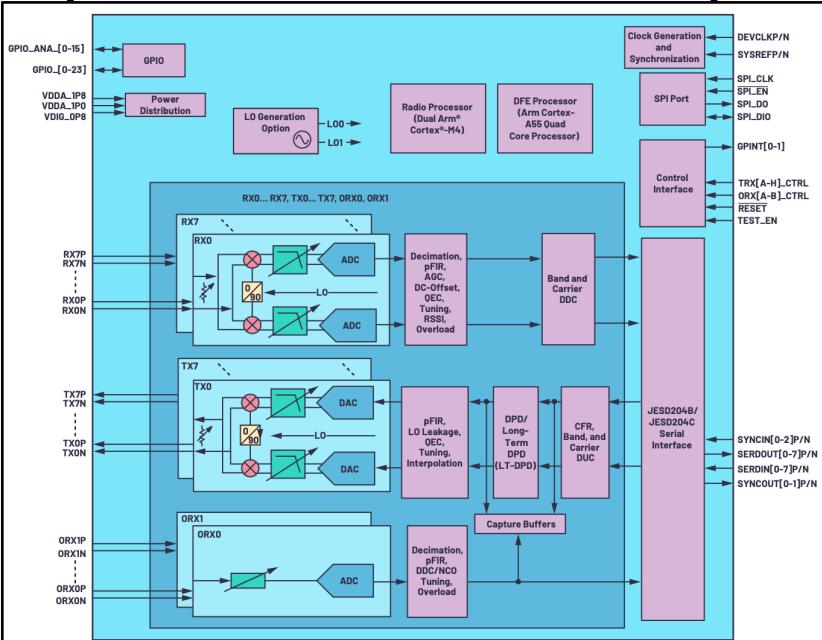
Functions → Form:

- Amplify the RF signal

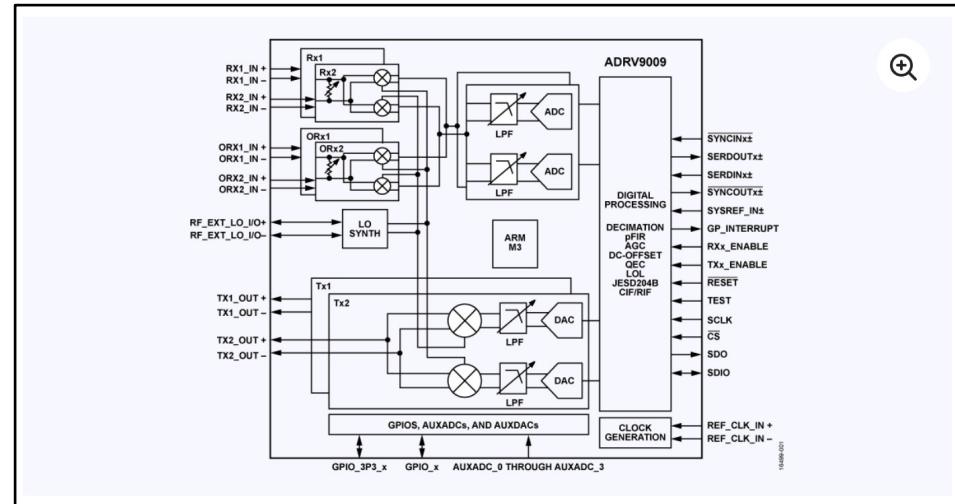
Notes/Questions/Observations:

- What power is required to close the link?
 - Frequency, aperture, altitude dependent?

Other Potential Components to Explore



ADRV904x Block Diagram



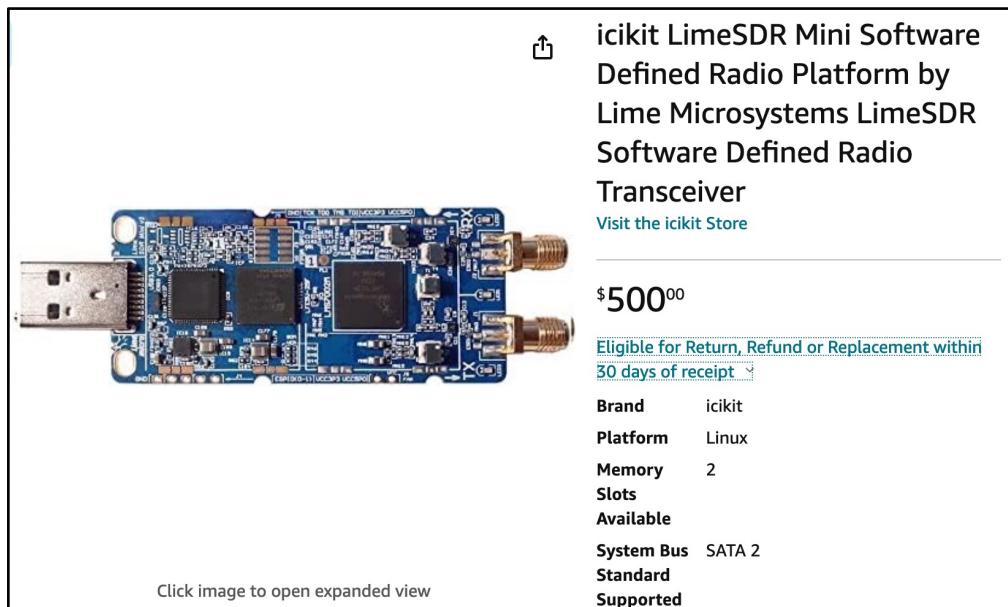
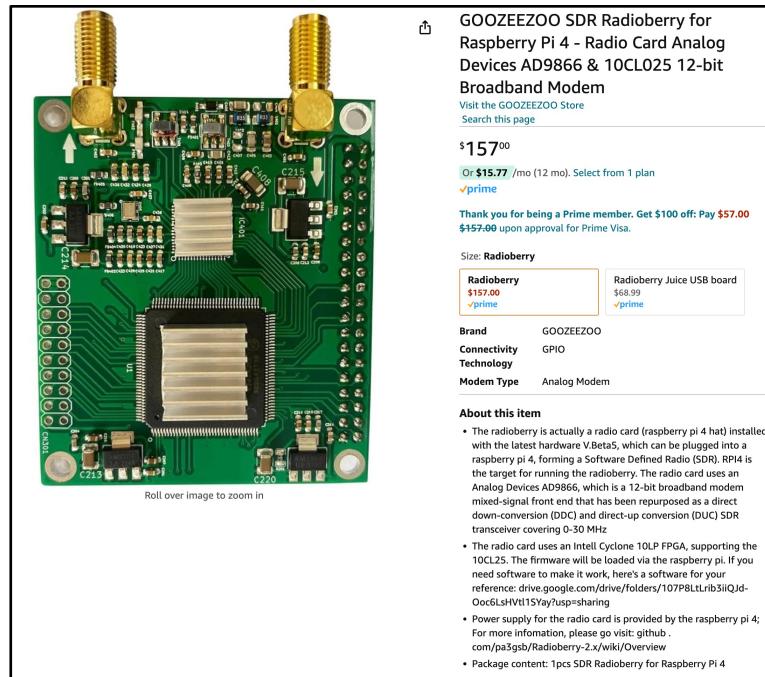
Acronyms

Acronym	Definition
ADC	Analog to Digital Conversion
COTS	Commercial Off The Shelf
D/L	Downlink
DAC	Digital to Analog Conversion
DC	Direct Current
FM	Frequency Modulation
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
PA	Power Amplifier
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
Rx	Receive
SDR	Software Defined Radio
TLM	Telemetry
Tx	Transmit
U/L	Uplink
XBT	Cross Band Transponder

Prototyping

Early Prototyping Ideas

- Potential Options:
 - Radioberry w/Raspberry Pi (and required converters)
 - LimeSDR
 - Others?
- Purpose: Exploration on non-flight COTS parts to gain confidence/experience while going through conceptual design



Backup

Assumptions

#	Title	Assumption
1	Input Power	A single source of power will be received from the bus Conversion and distribution of power is a function of the XBT
2		
3		
4		
5		
6		
7		
8		

High-Level Questions

#	Question	Response
1	Are there any desired additional capabilities that we can enhance with a digital design or a SDR design?	
2		
3		
4		
5		
6		
7		
8		

Requirements(-ish)

Design-y Questions

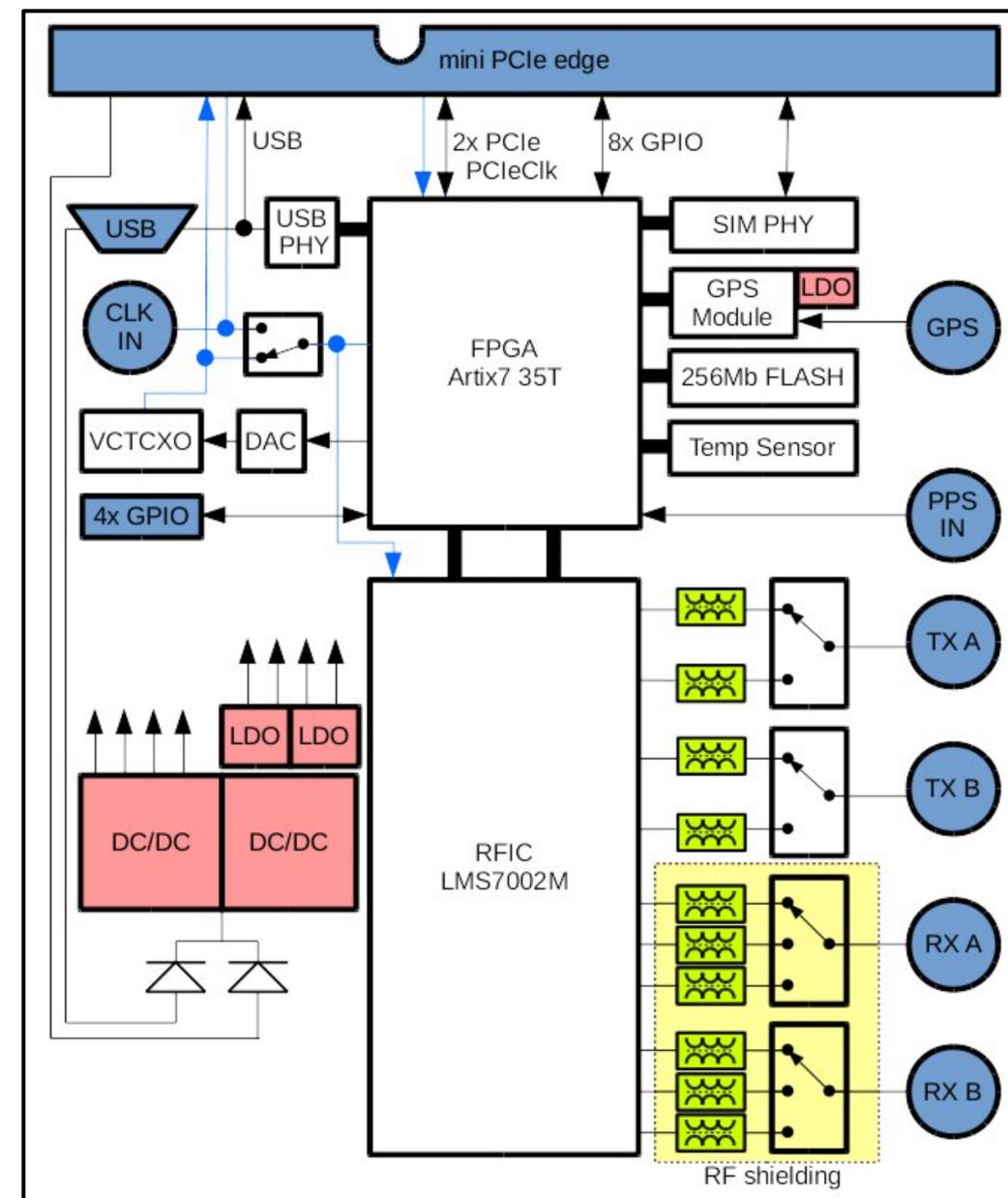
#	Question	Response
1	What TLM is typically collected?	
2	How many signals?	
3	What is a good power draw to shoot for?	
4	Are reference signals (e.g., PPS, 50 MHz) available from the bus or should they be accounted for on the XBT?	
5		
6		
7		
8		

SDR

- Fairwaves
- XTRX

Features & Specifications

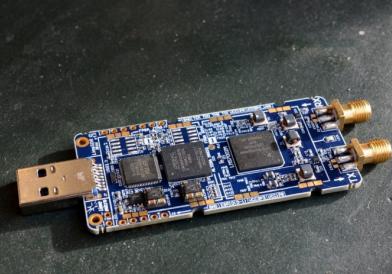
- **RF Chipset:** Lime Microsystems LMS7002M FPRF
- **FPGA Chipset:** Xilinx Artix 7 35T
- **Channels:** 2 × 2 MIMO
- **Sample Rate:** ~0.2 MSPS to 120 MSPS SISO / 90 MSPS MIMO
- **Tuning Range:** 30 MHz - 3.8 GHz
- **Rx/Tx Range:**
 - 10 MHz - 3.7 GHz
 - 100 kHz - 3.8 GHz with signal level degradation
- **PCIe Bandwidth:**
 - PCIe x2 Gen 2.0: 8 Gbit/s
 - PCIe x1 Gen 2.0: 4 Gbit/s
 - PCIe x1 Gen 1.0: 2 Gbit/s
- **Reference Clock:**
 - Frequency: 26 MHz
 - Stability: <10 ppb stability after GPS/GNSS lock, 500 ppb at start up
- **Form Factor:** full-size Mini PCIe (30 × 51 mm)
- **Bus Latency:** <10 µs, stable over time
- **Synchronization:** synchronize multiple XTRX boards for massive MIMO
- **GPIO:**
 - FPC Edge Connector: four lines (usable as two diff-pairs)
 - Mini PCIe Reserved Pins: eight lines (including two diff-pairs, 1pps input, 1pps output, TDD switch control, and three LEDs)
- **Accessories:**
 - Antennas + Cables
 - USB 3 Adapter with Aluminium Enclosure
 - PCIe x2 + Front End Adapter
 - PCIe Octopack



Source: <https://www.crowdsupply.com/fairwaves/xtrx>

SDR

- Lime Microsystems took over the XTRX (?)
- Additional Options:

<p>LimeSDR Mini</p> <p>The LimeSDR Mini board is a highly cost-optimised hardware platform for high-performance digital and RF designs</p> 	<p>LimeSDR QPCle</p> <p>Double the capacity (4x4 MIMO) of the original LimeSDR PCIe, this board is at the heart of the LimeNET Core and, by extension, the LimeNET Base Station.</p> 
<p>LimeSDR</p> <p>LimeSDR is a low cost, open source, apps-enabled (more on that later) software defined radio (SDR) platform that can be used to support just about any type of wireless communication standard.</p> 	<p>LimeSDR PCIe</p> <p>PCIe variant of the original LimeSDR.</p> 

Source: <https://limemicro.com/products/boards/>

SDR

- AntSDR E200

- **RF Chipset:** Analog Devices AD9363 / AD9361
- **FPGA Chipset:** AMD/Xilinx ZYNQ7020
- **Channels:** 2 x 2 MIMO
- **Sample Rate:** 200 kS/s - 61.44 MS/s
- **Tuning Range:** AD9363: 325 MHz - 3.8 GHz, AD9361: 70 MHz - 6 GHz
- **RF bandwidth:** AD9363: 200 KHz - 20 MHz, AD9361: 200 KHz - 56 MHz
- **RF Transmit Power:** Up to 10 dBm
- **Flash Memory:** 1x QSPI 256 Mb flash memory for firmware
- **RAM:** 512 MB DDR3
- **Clock System:** 40M VCXO and PPS/10M Reference clock input
- **Connectivity:**
 - 2x SMA and 2x U.FL connectors
 - 1x Gigabit Ethernet
 - 1x Micro SD card slot
 - FPGA JTAG connector for external JTAG programmer/debugger
 - 8x PL GPIO interfaces

