

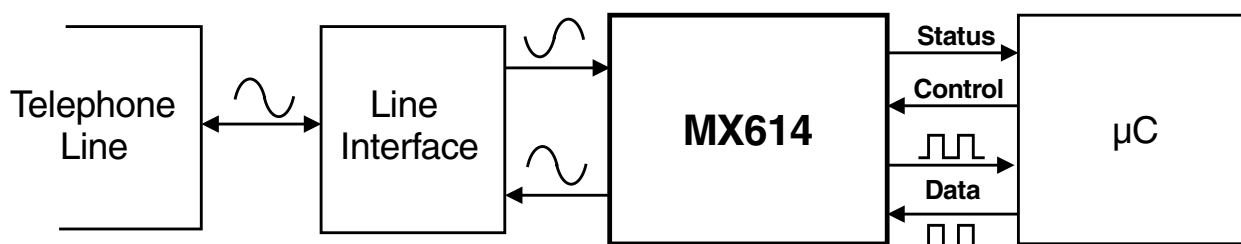
### PRELIMINARY INFORMATION

#### Features

- 1200bps - 1800bps half duplex Bell 202 Compatible Modem
- Optional 1200bps Data Retiming Facility can eliminate external UART
- Optional 5bps and 150bps Back Channel
- Optional Line Equalization

#### Applications

- Low Voltage Operation (3.3V to 5.0V)
- Low Power Operation  
1mA typ. @ 3.3V Operating Mode  
1 $\mu$ A typ. Zero-Power Mode
- Standard 3.58MHz Xtal/Clock
- Telephone Telemetry Applications



The MX614 is a low voltage, low power CMOS integrated circuit designed for the reception or transmission of asynchronous 1200bps data. This device is compatible with Bell 202 type systems. The MX614 supports 5bps and 150bps 'back channel' operation. Asynchronous data rates up to 1818bps are also supported.

The MX614 provides an optional Tx and Rx data retiming function which can eliminate, based on user preference, the need for a UART in the associated  $\mu$ C when operating at 1200bps. An optional line equalizer has been incorporated into the receive path and is controlled by an external logic level.

The MX614 may be used in a wide range of telephone telemetry systems. A very low current "Zero Power Mode (1 $\mu$ A typ.) and an operating current of 1mA typ. @  $V_{DD} = 3.3V$ , make the MX614 ideal for portable, terminal and line powered applications. A standard 3.58MHz Xtal/Clock is required and the device operates from a 3.0V to 5.5V supply.

The MX614 is available in 24-pin TSSOP (MX614TN), 16-pin SOIC (MX614DW) and 16-pin PDIP (MX614P) packages.

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## 1. Block Diagram

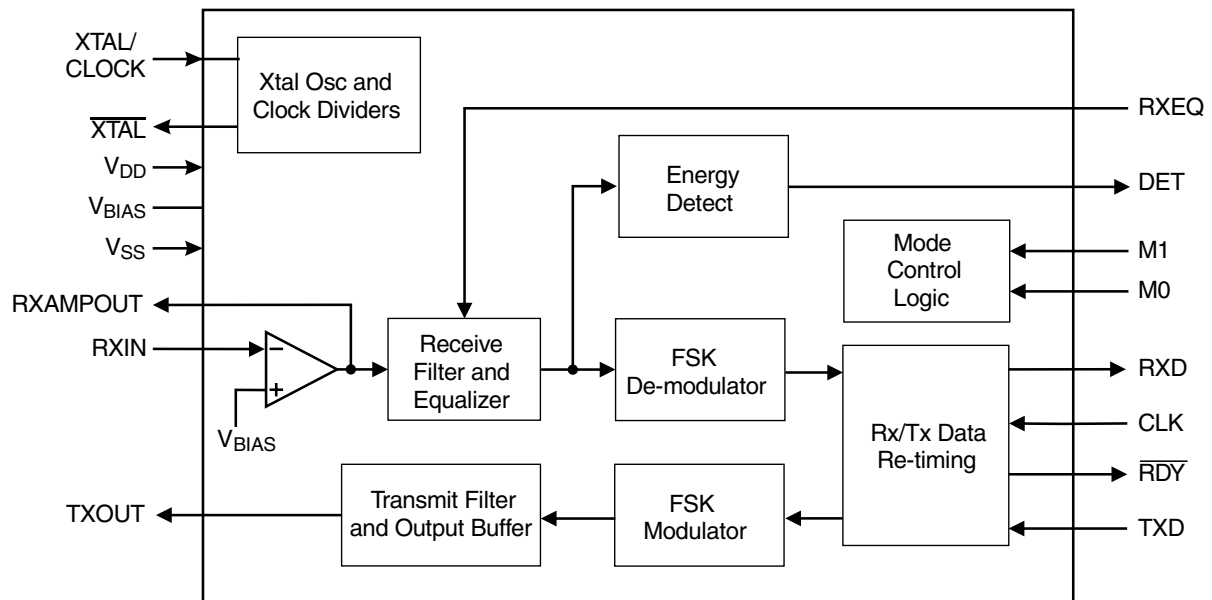
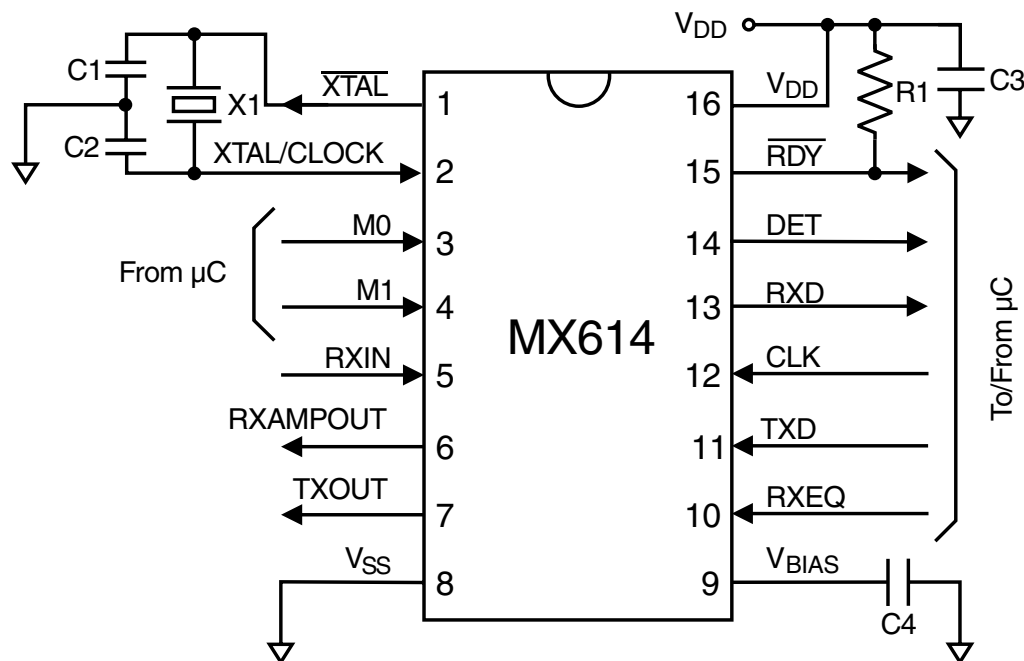


Figure 1: Block Diagram

## 2. Signal List

Pin No.		Signal		Description
P, DW	TN	Name	Type	
1	1	XTAL	output	Output of the on-chip Xtal oscillator inverter.
2	2	XTAL/CLOCK	input	Input to the on-chip Xtal oscillator inverter.
3	5	M0	input	A logic level input for setting the mode of the device. See section 4.2
4	6	M1	input	A logic level input for setting the mode of the device. See section 4.2
5	7	RXIN	input	Input to the Rx input amplifier.
6	8	RXAMPOUT	output	Output of the Rx input amplifier
7	11	TXOUT	output	Output of the FSK generator.
8	12	V <sub>SS</sub>	Power	Negative supply (ground).
9	13	V <sub>BIAS</sub>	output	Internally generated bias voltage, held at V <sub>DD</sub> /2 when the device is not in 'Zero-Power' mode. Should be bypassed to V <sub>SS</sub> by a capacitor mounted close to the device pins.
10	14	RXEQ	input	A logic level input for enabling/disabling the equalizer in the receive filter. See section 4.4
11	17	TXD	input	A logic level input for either the raw input to the FSK Modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. See section 4.9
12	18	CLK	input	A logic level input which may be used to clock data bits in or out of the FSK Data Retiming block.
13	19	RXD	output	A logic level output carrying either the raw output of the FSK Demodulator or re-timed characters depending on the state of the M0, M1 and CLK inputs. See section 4.8
14	20	DET	output	A logic level output of the on-chip Energy Detect circuit.
15	23	RDY	output	"Ready for data transfer" output of the on-chip data retiming circuit. This open-drain active low output may be used as an Interrupt Request/Wake-up input to the associated $\mu$ C. An external pull-up resistor should be connected between this output and V <sub>DD</sub> .
16	24	V <sub>DD</sub>	Power	Positive supply. Levels and thresholds within the device are proportional to this voltage. Should be bypassed to V <sub>SS</sub> by a capacitor mounted close to the device pins.
	3, 4, 9, 10, 15, 16, 21, 22	N/C		No internal connection

### 3. External Components



R1		100k $\Omega$	$\pm 5\%$
C1 C2		18pF	$\pm 10\%$
C3		0.1 $\mu$ F	$\pm 10\%$
C4		0.1 $\mu$ F	$\pm 10\%$
X1	Note 1	3.579545MHz	

**Figure 2: Recommended External Components for Typical Application**

#### External Components Notes

- IMPORTANT:** This device is capable of detecting and decoding small amplitude signals. To achieve this  $V_{DD}$  and  $V_{BIAS}$  decoupling and protecting the receive path from extraneous in-band signals are very important. It is recommended that the decoupling capacitors be placed so that connections between them and the device pins are as short as practicable e.g.  $\leq 1$  inch from device pins. A ground plane protecting the receive path will help attenuate interfering signals
- A crystal frequency of 3.579545MHz  $\pm 0.1\%$  is required for correct FSK operation. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of  $V_{DD}$  peak-peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

## 4. General Description

### 4.1 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the MX614 is determined by a 3.579545MHz clock signal present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL/CLOCK input. If supplied from an external source, C1, C2 and X1 should not be fitted.

The on-chip oscillator is turned off in the 'Zero-Power' mode.

If the clock is provided by an external source which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by MX614 as well as generating undefined states of the RXD, DET and RDY outputs.

### 4.2 Mode Control Logic

The MX614's operating mode is determined by the logic levels applied to the M0 and M1 input pins:

M1	M0	Rx Mode	Tx Mode	Data Retime <sup>[1]</sup>
0	0	1200bps	150bps	Rx
0	1	Off	1200bps	Tx
1	0	1200bps	Off / 5bps	Rx
1	1	'Zero-Power'		-

[1] If enabled

**Note:** On applying power to the device, the mode must be set to 'ZP', i.e. M0 = '1', M1 = '1', until V<sub>DD</sub> has stabilized.

In the 'Zero-Power' (ZP) mode, power is removed from all internal circuitry. When leaving the 'ZP' mode there must be a delay of 20ms before any Tx data is passed to, or Rx data read from the device to allow the bias level, filters, and oscillator to stabilize.

### 4.3 Rx Input Amplifier

This amplifier is used to adjust the received signal to the correct amplitude for the FSK receiver and Energy Detect circuits (see section 5.1).

### 4.4 Receive Filter and Equalizer

The Receive Filter and Equalizer section is used to attenuate out of band noise and interfering signals, especially the locally generated transmit tones which might otherwise reach the 1200bps FSK Demodulator and Energy Detector circuits. This block also includes a switchable equalizer section. When the RXEQ pin is low, the overall group delay of the receive filter is flat over the 1200bps frequency range. If the RXEQ pin is high the receive filter's typical overall group delay will be as shown in Figure 3.

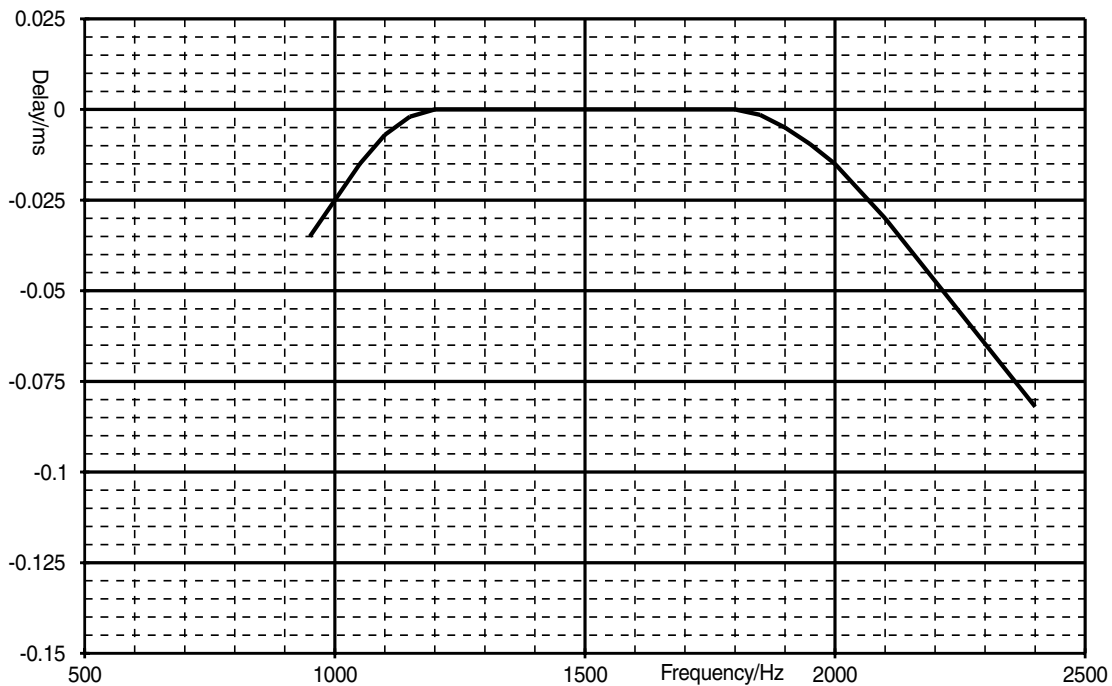


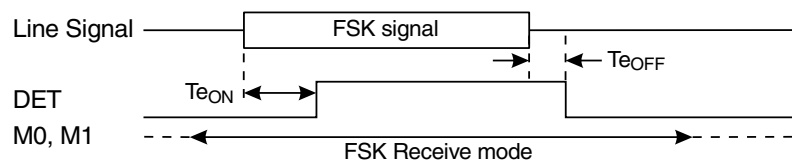
Figure 3: Rx Equalizer Group Delay (RXEQ = '1') wrt 1700Hz

## 4.5 Energy Detector

This block operates by measuring the level of the signal at the output of the Receive Filter, and comparing it against a preset threshold.

The DET output will be set high when the level has exceeded the threshold for a sufficient period of time. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note that this circuit may also respond to non-FSK signals such as speech.



See section 6.1 for definitions of  $T_{eON}$  and  $T_{eOFF}$

Figure 4: FSK Level Detector Operation

## 4.6 FSK Demodulator

This block converts the 1200bps FSK input signal to a logic level received data signal which is output via the RXD pin as long as the Data Retiming function is not enabled (see section 4.8). This output does not depend on the state of the DET output.

When the Rx 1200bps mode is 'Off' or in 'ZP' the DET and RXD pins are held low.

Note that in the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data. For this reason it is advised that the RXD pin is read only when data is expected.

## 4.7 FSK Modulator and Transmit Filter

These blocks produce a tone according to the TXD, M0 and M1 inputs as shown in the table below, assuming data retiming is not being used:

M1	M0	TXD = 0	TXD = 1
1	1	-	-
1	0	0Hz <sup>[1]</sup>	387Hz
0	0	487Hz	387Hz
0	1	2200Hz	1200Hz

Note: [1] TXOUT held at approx.  $V_{DD}/2$ .

When modulated at the appropriate baud rates, the Transmit Filter and associated external components (see section 5.1) limit the FSK out of band energy sent to the line in accordance with Figure 5 and Figure 6, assuming that the signal on the line is at -6dBm or less.

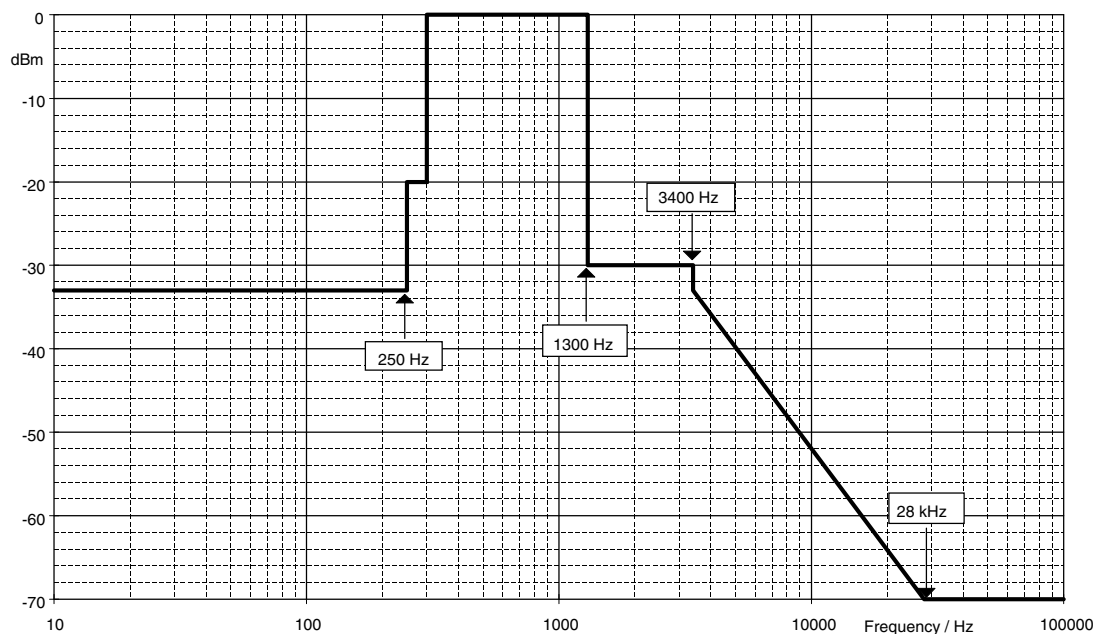


Figure 5: Tx limits at 5bps and 150bps rate



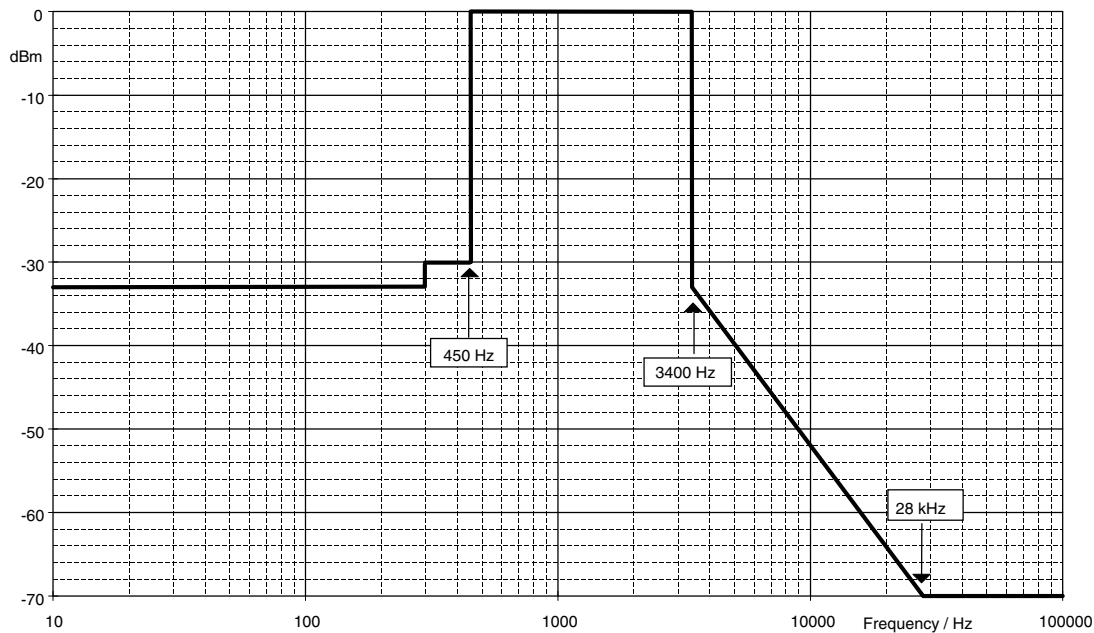


Figure 6: Tx limits at 1200bps rate

#### 4.8 Rx Data Retiming

This function may be used when the received data consists of 1200bps asynchronous characters, each character consisting of one start bit followed by a minimum of 9 formatted bits as shown in the table below.

**Note: Rx Data Retiming is not supported for data rates exceeding 1212bps.**

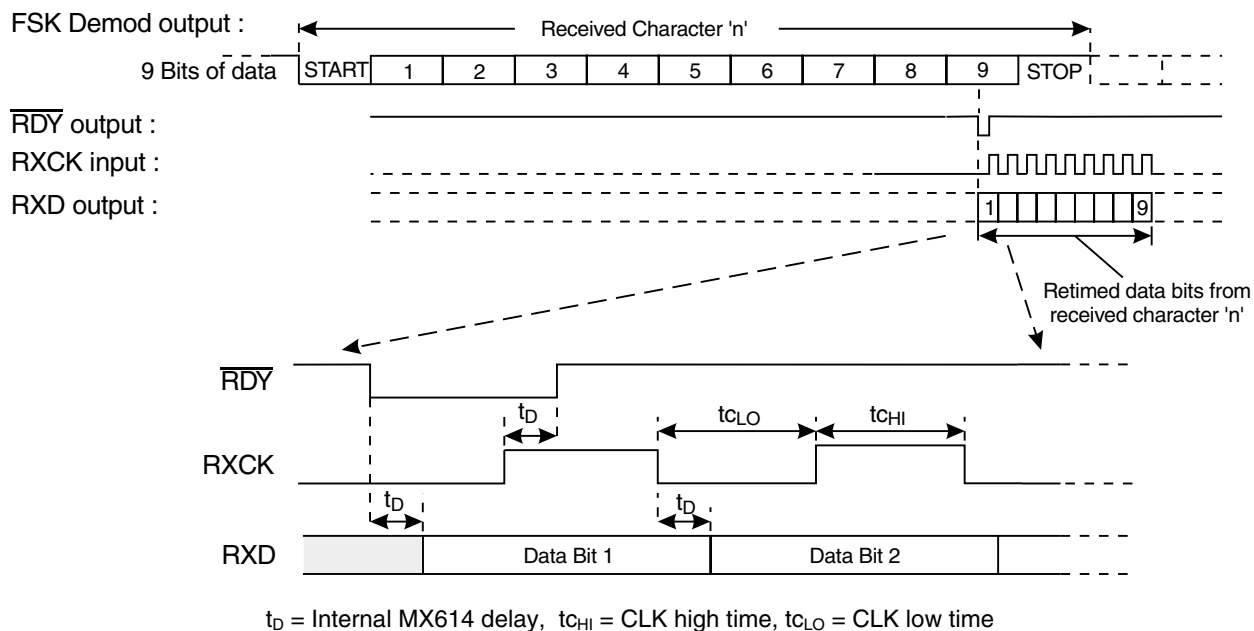
Data bits	Parity bits	Stop bits
7	0	$\geq 2$
7	1	$\geq 1$
8	0	$\geq 1$
8	1	$\geq 1$
9	0	$\geq 1$

The Data Retiming block, when enabled in receive mode, extracts the first 9 bits of each character following the start bit from the received asynchronous data stream, and presents them to the  $\mu\text{C}$  under the control of strobe pulses applied to the CLK input. The timing of these pulses is not critical and they may easily be generated by a simple software loop. This facility removes the need for a UART in the  $\mu\text{C}$  without incurring an excessive software overhead.

The receive retiming block consists of two 9-bit shift registers, the input of the first is connected to the output of the FSK demodulator and the output of the second is connected to the RXD pin. The first register is clocked by an internally generated signal that stores the 9 received bits following the timing reference of a high to low transition at the output of the FSK demodulator. When the 9th bit is clocked into the first register these 9 bits are transferred to the second register, a new stop-start search is initiated and the CLK input is sampled. If the CLK input is low at this time the  $\overline{\text{RDY}}$  pin is pulled low and the first received bit is output on the RXD pin. The CLK pin should then be pulsed high 9 times, the first 8 high to low transitions will be used by the device to clock out the bits in the second register. The  $\overline{\text{RDY}}$  output is cleared the first time the CLK input goes high. At the end of the 9th pulse the RXD pin will be connected to the FSK demodulator output.

So to use the Data Retiming function, the CLK input should be kept low until the  $\overline{\text{RDY}}$  output goes low; if the Data Retiming function is not required the CLK input should be kept high at all times.

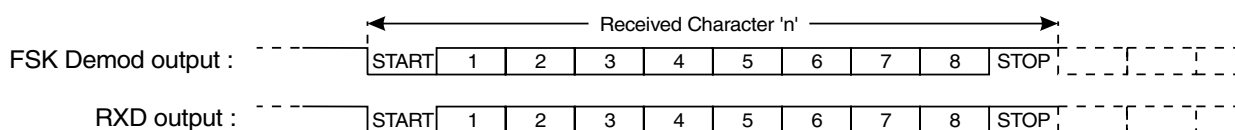
The only restrictions on the timing of the CLK waveform are those shown in Figure 7 and the need to complete the transfer of all nine bits into the  $\mu\text{C}$  within the time of a complete character at 1200bps. See Section 6.2 for Timing specifications.



**Figure 7: FSK Operation with Rx Data Retiming**

Note that, if enabled, the Data Retiming block may interpret speech or other signals as random characters.

If the Data Retiming facility is not required, the CLK input to the MX614 should be kept high at all times. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the  $\overline{\text{RDY}}$  output will not be activated by the FSK signal. This case is illustrated by the example in Figure 8.



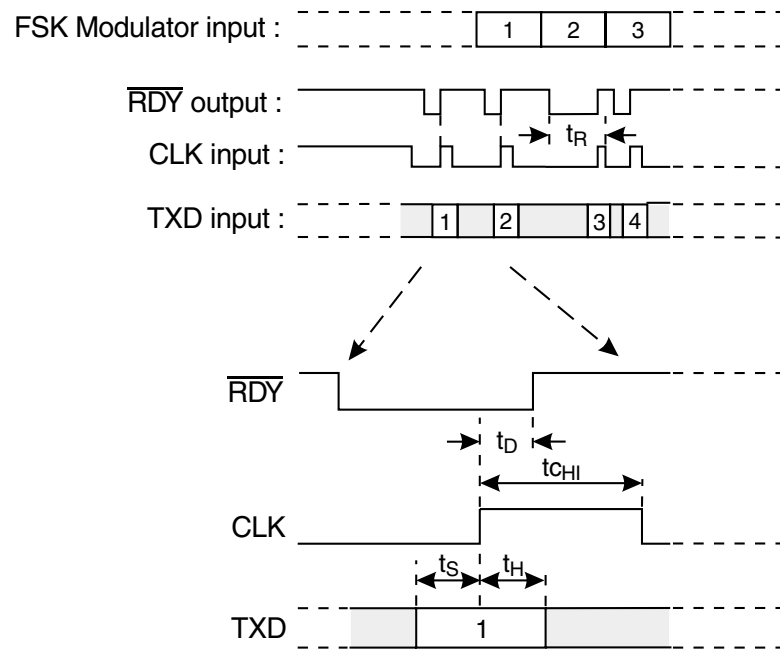
**Figure 8: FSK Operation without Rx Data Retiming (CLK always high)**

## 4.9 Tx Data Retiming

The Data Retiming block, when enabled in 1200bps transmit mode, requires the controlling  $\mu\text{C}$  to load one bit at a time into the device by a pulse applied to the CLK input. The timing of this pulse is not critical and it may easily be generated by a simple software loop. This facility removes the need for a UART in the  $\mu\text{C}$  without incurring an excessive software overhead. **Note: Tx Data Retiming is not supported for data rates exceeding 1212bps.**

The Tx re-timing circuit consists of two 1-bit registers in series, the input of the first is connected to the TXD pin and the output of the second feeds the FSK modulator. The second register is clocked by an internally generated 1200Hz signal and when this occurs the CLK input is sampled. If the CLK input is high the TXD pin directly controls the FSK modulator, if the CLK input is low the FSK modulator is controlled by the output of the second register and the  $\overline{\text{RDY}}$  pin is pulled low. The  $\overline{\text{RDY}}$  output is reset by a high level on the CLK input pin. A low to high change on the CLK input pin will latch the data from the TXD input pin into the first register ready for transfer to the second register when the internal 1200Hz signal next occurs.

So to use the retiming option the CLK input should be held low until the  $\overline{\text{RDY}}$  output is pulled low. When the  $\overline{\text{RDY}}$  pin goes low the next data bit should be applied at the TXD input and the CLK input pulled high and then low within the time limits set out in Figure 9. See Section 6.2 for Timing specifications.

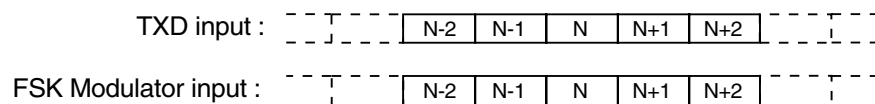


$t_D$  = Internal MX614 delay,  $t_R$  =  $\overline{\text{RDY}}$  low to CLK going low,  $t_S$  = data set up time  
 $t_{CH}$  = CLK high time,  $t_H$  = data hold time

**Figure 9: FSK Operation with Tx Data Retiming**

To ensure synchronization between the controlling device and the MX614 when entering Tx retiming mode the TXD pin must be held at a constant logic level from when the CLK pin is first pulled low to the end of loading in the second retimed bit. Similarly when exiting Tx retiming mode the TXD pin should be held at the same logic level as the last retimed bit for at least 2 bit times after the CLK line is pulled high.

If the data retiming facility is not required, the CLK input to the MX614 should be kept high at all times. The asynchronous data to the FSK modulator will then be connected directly to the TXD input pin. This is illustrated in Figure 10 and will also be the case when transmitting 5bps or 150bps data which has no retiming option.



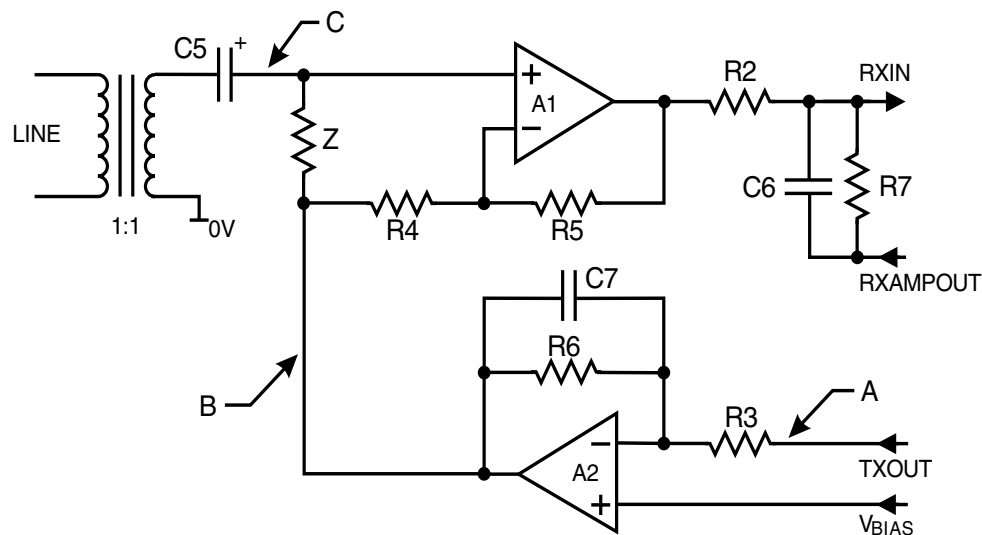
**Figure 10: FSK Operation without Tx Data Retiming (CLK always high)**

## 5. Application

### 5.1 Line Interface

The signals on the telephone line are not suitable for direct connection to the MX614. A Line Interface circuit is required to:

- Provide high voltage and dc isolation
- Attenuate the Tx signal present at the Rx input
- Provide the low impedance drive necessary for the line
- Filter the Tx and Rx signals



R2	See Notes		±1%,
R3	See Notes		±1%,
R4-R7		100kΩ	±1%,
C5		22μF	±20%
C6		100pF	±10%
C7		330pF	±10%

**Figure 11: Line Interface Circuit**

**Line Interface Notes:**

1. The components 'Z' between points B and C should match the line impedance.
2. Device A2 must be able to drive 'Z' and the line.
3. R2: For optimum results R2 should be set so that the gain is  $V_{DD}/5.0$ , i.e.  $R2 = 100k\Omega$  at  $V_{DD} = 5.0V$ , rising to  $150k\Omega$  at  $V_{DD} = 3.3V$ .
4. R3: The levels in dB (relative to a  $775mV_{RMS}$  signal) at 'A', 'B' and 'C' in the line interface circuit are:

$$\begin{aligned} \text{Level at 'A'} &= 20\text{Log}(V_{DD}/5) \\ \text{" 'B'} &= \text{'A'} + 20\text{Log}(100k\Omega/R3) \\ \text{" 'C'} &= \text{'B'} - 6 \end{aligned}$$

Example:

$V_{DD}$	'A'	R3	'B'	'C'
3.3V	-3.6dB	100k $\Omega$	-3.6dB	-9.6dB
5.0V	0dB	150k $\Omega$	-3.5dB	-9.5dB

## 6. Performance Specification

### 6.1 Electrical Performance

#### Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply ( $V_{DD} - V_{SS}$ )	-0.3	7.0	V
Voltage on any pin to $V_{SS}$	-0.3	$V_{DD} + 0.3$	V
Current into or out of and pins			
$V_{DD}$	-30	30	mA
$V_{SS}$	-30	30	mA
Any other pins	-20	20	mA
<b>DW / PDIP Packages</b>			
Total Allowable Power Dissipation at $T_{AMB} = 25^{\circ}\text{C}$		800	mW
Derating above $25^{\circ}\text{C}$		13	mW/ $^{\circ}\text{C}$ above $25^{\circ}\text{C}$
Storage Temperature	-55	125	$^{\circ}\text{C}$
Operating Temperature	-40	85	$^{\circ}\text{C}$

#### Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply ( $V_{DD} - V_{SS}$ )		3.0	5.5	V
Operating Temperature		-40	85	$^{\circ}\text{C}$
Xtal Frequency	1	3.575965	3.583125	MHz

#### Operating Limits Notes:

1. A crystal frequency of  $3.579545\text{MHz} \pm 0.1\%$  is required for correct FSK operation.

## Operating Characteristics

For the following conditions unless otherwise specified:

$V_{DD} = 3.3V$  at  $T_{AMB} = 25^{\circ}C$

Xtal Frequency =  $3.579545MHz \pm 0.1\%$  0dBV corresponds to  $1.0V_{RMS}$

Tx and Rx data rates = 1200bps.

	Notes	Min.	Typ.	Max.	Units
<b>DC Parameters</b>					
$I_{DD}$ (M0 = '1', M1 = '1')	1, 2		1.0		$\mu A$
$I_{DD}$ (M0 or M1 = '0') at $V_{DD} = 3.0V$	1		1.0	1.25	mA
$I_{DD}$ (M0 or M1 = '0') at $V_{DD} = 5.0V$	1		1.7	2.5	mA
Logic '1' Input Level		70%			$V_{DD}$
Logic '0' Input Level				30%	$V_{DD}$
Logic Input Leakage Current ( $V_{IN} = 0$ to $V_{DD}$ ), Excluding XTAL/CLOCK Input		-1.0		1.0	$\mu A$
Output Logic '1' Level ( $I_{OH} = 360\mu A$ )		$V_{DD} - 0.4$			V
Output Logic '0' Level ( $I_{OL} = 360\mu A$ )				0.4	V
$\overline{RDY}$ Output 'off' State Current ( $V_{OUT} = V_{DD}$ )				1.0	$\mu A$
<b>FSK Demodulator</b>					
Bit Rate	3	0	1200	1818	Baud
Mark (Logical '1') Frequency		1188	1200	1212	Hz
Space (Logical '0') Frequency		2178	2200	2222	Hz
Valid Input Level Range	4, 5	-40.0		-8.0	dBV
Maximum Twist (Mark Level wrt Space Level)		$\pm 6.0$			dB
Acceptable Signal to Noise Ratio	6	20.0			dB
Level Detector 'On' Threshold Level	4			-40.0	dBV
Level Detector 'Off' to 'On' Time (Figure 4 $T_{eON}$ )				25.0	ms
Level Detector 'On' to 'Off' Time (Figure 4 $T_{eOFF}$ )		8.0			ms
<b>FSK Retiming</b>					
Acceptable Rx Data Rate		1188	1200	1212	Baud
Tx Data Rate		1194		1206	Baud
<b>FSK Modulator</b>					
TXOUT Level Driving $\geq 40k\Omega$ load	7	-3.2	-2.2	-1.2	dBV
Twist (Mark Level wrt Space Level)		-2.0	0	2.0	dB
<b>Tx 1200bps (M1 = '0', M0 = '1').</b>					
Bit Rate	3	0	1200	1818	Baud
Mark (Logical '1') Frequency		1197		1203	Hz
Space (Logical '0') Frequency		2196		2204	Hz
<b>Tx 150bps (M1 = '0', M0 = '0').</b>					
Bit Rate		0	150	152	Baud
Mark (Logical '1') Frequency		385		389	Hz
Space (Logical '0') Frequency		485		489	Hz
<b>Tx 5bps (M1 = '1', M0 = '0').</b>					
Bit Rate		0	5.0	5.1	Baud
Mark (Logical '1') Frequency		385		389	Hz

	Notes	Min.	Typ.	Max.	Units
Space (Logical '0') Frequency	8		0		Hz
<b>Input Amplifier</b>					
Impedance (RXIN Pin)	9	10.0			MΩ
Voltage Gain	9		500		V/V
<b>XTAL/CLOCK Input</b>					
'High' Pulse Width	10	100			ns
'Low' Pulse Width	10	100			ns

**Operating Characteristics Notes:**

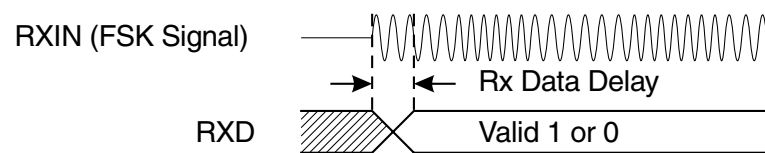
1. Not including any current drawn from the MX614 pins by external circuitry other than X1, C1 and C2.
2. TXD, RXEQ and CLK inputs at  $V_{SS}$ , M0 and M1 inputs at  $V_{DD}$ .
3. Tested at 1200bps.
4. Measured at the Rx Input Amplifier output (pin RXAMP0UT) for 1200Hz and  $V_{DD}= 5.0V$ . The internal threshold levels are proportional to  $V_{DD}$ . To cater for other supply voltages or different signal level ranges the voltage gain of the Rx Input Amplifier should be adjusted by selecting the appropriate external components as described in section 5.1.
5. Best 1818bps performance is achieved when the minimum Input Level is  $\geq -32dBV$ .
6. Flat noise in 200 - 3200Hz band.
7. At  $V_{DD}= 5.0V$ . ( $-2.2dBV$  is equivalent to 0dBm ref. 775mV<sub>RMS</sub> into 600Ω.)
8. TXOUT held at approximately  $V_{DD}/2$ .
9. Open loop, small signal low frequency measurements.
10. Timing for an external input to the XTAL/CLOCK pin.

## 6.2 Timing

Data and Mode Timing	Notes	Min.	Typ.	Max.	Units
Rx Data Delay (RXIN to RXD)	1, 5		2.55		ms
Tx Delay Data (TXD to TXOUT)	1, 6		0.1		ms
Mode change delay ZP to Tx or Rx	2			20	ms
Mode change delay Tx1200 to Rx1200	2			4.0	ms
Mode change delay Rx1200 to Tx1200	2			0.2	ms
$t_D$ = Internal MX614 delay	3, 4			1	$\mu$ s
$t_{CH}$ = CLK High time	3, 4	1			$\mu$ s
$t_{CL}$ = CLK low time	3	1			$\mu$ s
$t_R$ = RDY low to CLK going low	4			800	$\mu$ s
$t_S$ = Data Set-up time	4	1			$\mu$ s
$t_H$ = Data Hold time	4	1			$\mu$ s

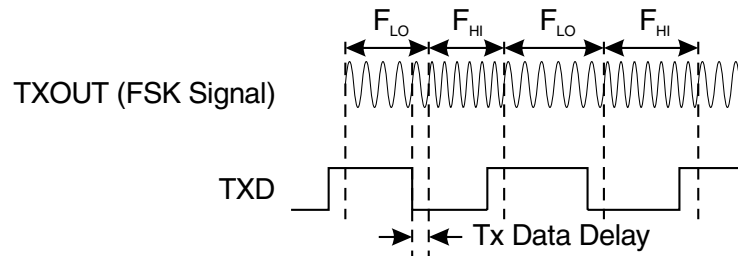
### Timing Notes

1. When data retiming is not enabled.
2. Delay from mode change to reliable data at TXOUT or RXD pins.
3. Reference Figure 7.
4. Reference Figure 9.
5. Reference Figure 12.
6. Reference Figure 13.



Note: M0 and M1 are preset and stable.

**Figure 12: RXIN to RXD Delay time**



Note: M0 and M1 are preset and stable.  $F_{LO}$  and  $F_{HI}$  are the two FSK signaling frequencies.

**Figure 13: TXD to TXOUT Delay time**



## 6.3 Packaging

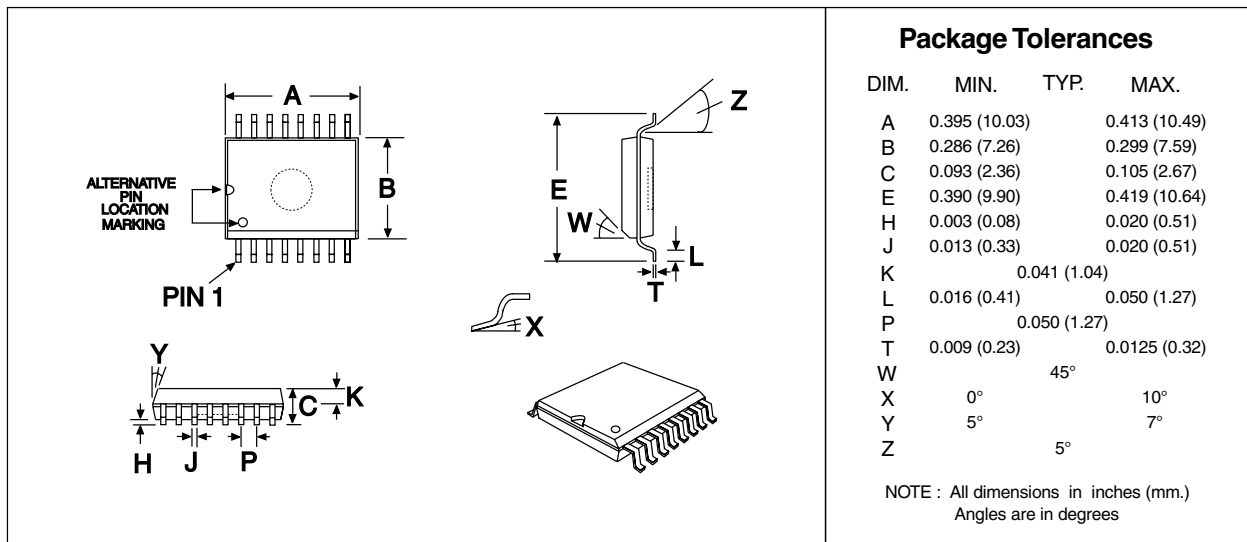


Figure 14: 16-pin SOIC Mechanical Outline: *Order as part no. MX614DW*

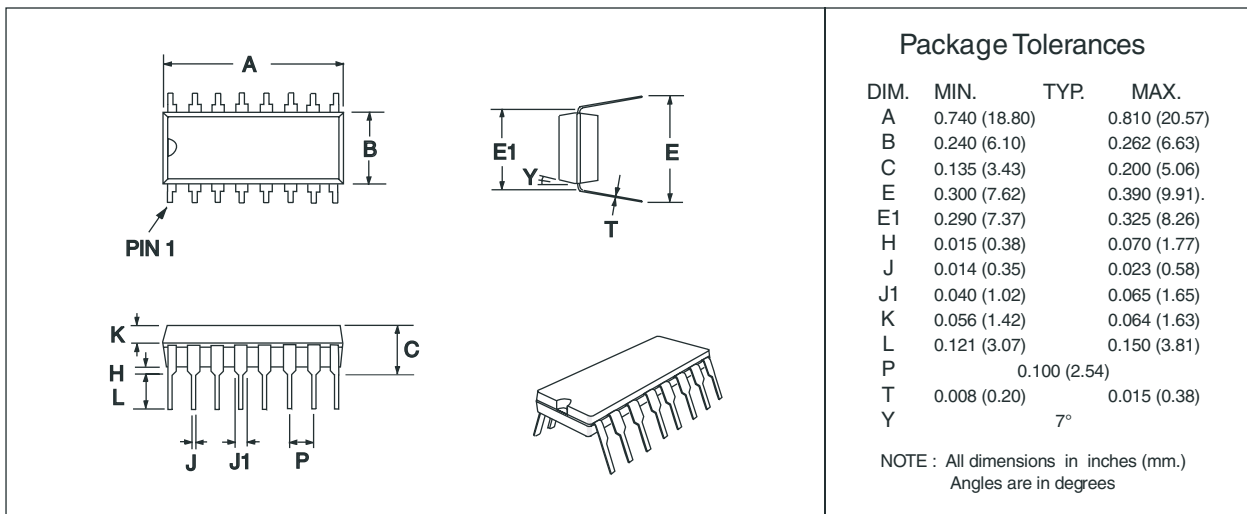
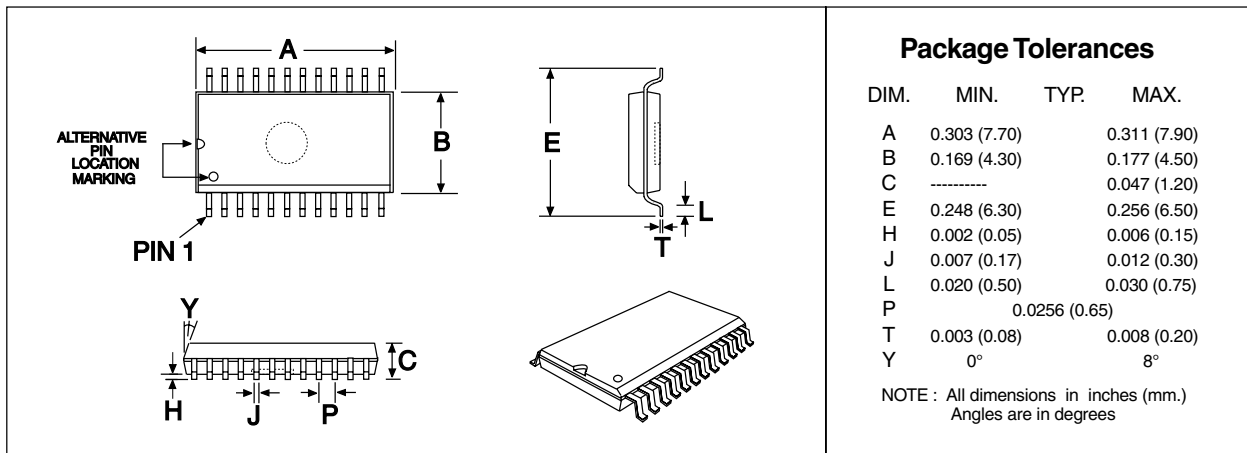


Figure 15: 16-pin PDIP Mechanical Outline: *Order as part no. MX614P*



**Figure 16 : 24-pin TSSOP Mechanical Outline: Order as part no. MX614TN**

## CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc (*Consumer Microcircuits Limited (UK)*, *MX-COM, Inc (USA)* and *CML Microcircuits (Singapore) Pte Ltd*) have undergone name changes and, whilst maintaining their separate new names (*CML Microcircuits (UK) Ltd*, *CML Microcircuits (USA) Inc* and *CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.

These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

### CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

### CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the '**MX-COM**' textual logo is being replaced by a '**CML**' textual logo.

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