

Quad 2-Input NAND Gates in bare die form

Rev 1.0 07/02/19

Description

74HC00 provides x4 independent 2-input NAND gates performing the Boolean function Y = $\overline{A \cdot B}$ or Y = $\overline{A} + \overline{B}$. The device is fabricated using a 2.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power. Internal circuitry comprises of 3 stages and includes buffered output for high noise immunity and stability. Device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Features:

Output Drive Capability: 10 LSTTL Loads

■ Low Input Current: 1µA

Outputs directly interface CMOS, NMOS and TTL

Operating Voltage Range: 2V to 6V

Function compatible with 74LS00

High Noise Immunity CMOS process.

Ordering Information

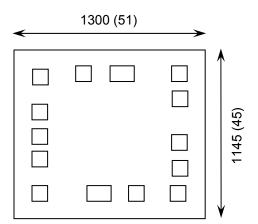
The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54HC00

Die Dimensions in µm (mils)



Supply Formats:

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Mechanical Specification

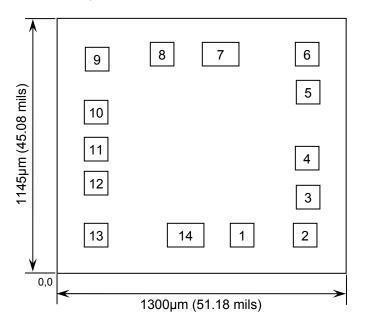
Die Size (Unsawn)	1300 x 1145 51 x 45	µm mils	
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils	
Top Metal Composition	Al 1%Si 1.1μ	m	
Back Metal Composition	N/A – Bare Si		





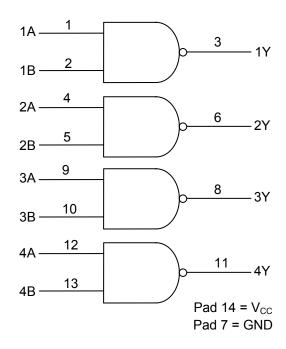
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Pad Layout and Functions



COORDINATES MARKED IN DIE PASSIVATION FOR ORIENTATION

Logic Diagram



PAD	FUNCTION	COORDIN	ATES (mm)
FAD	FUNCTION	X	Y
1	1A	0.132	0.443
2	1B	0.132	0.126
3	1Y	0.315	0.129
4	2A	0.485	0.128
5	2B	0.802	0. 129
6	2Y	0.981	0.129
7	GND	0.981	0.504
8	3Y	0.981	0.807
9	3A	0.971	1.105
10	3B	0.722	1.115
11	4Y	0.551	1.115
12	4A	0.331	1.115
13	4B	0.132	1.105
14	V _{CC}	0.132	0.65
CON	NECT CHIP BA	CK TO V _{CC} C	R FLOAT

Function Table

INP	INPUTS					
Α	В	Υ				
L	L	Н				
L	Н	Н				
Н	L	Н				
Н	Н	L				
	H = High level (steady state) L = Low level (steady state)					





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V _{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V _{IN}	-0.5 to V _{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V _{OUT}	-0.5 to V _{CC} +0.5	V
DC Input Current	I _{IN}	±20	mA
DC Output Current, per pad	I _{OUT}	±25	mA
DC Supply Current, V _{CC} or GND, per pad	I _{CC}	±50	mA
Power Dissipation in Still Air ²	P _D	750	mW
Storage Temperature Range	T _{STG}	-65 to 150	°C

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages referenced to GND)

•					
PARAMETER	SYMBOL		MIN	MAX	UNITS
Supply Voltage	V _{CC}		2	6	V
DC Input or Output Voltage	V_{IN} , V_{OUT}		0	V _{CC}	V
Operating Temperature Range	T _J		0	+85	°C
		V _{CC} = 2V	0	1000	
Input Rise or Fall Times	t _r , t _f	V _{CC} = 4.5V	0	500	ns
		$V_{CC} = 6.0V$	0	400	

^{3.} This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \le (V_{IN} \text{ or } V_{OUT}) \le V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{cc}	CONDITIONS		UNITS		
	OTHEOL	V CC	CONDITIONS	25°C	85°C	FULL RANGE⁴	Oitilo
Minimum High-Level Input Voltage		2.0V	.,	1.5	1.5	1.5	
	V _{IH}	3.0V	$V_{OUT} = 0.1V \text{ or}$ $V_{CC} - 0.1V$	2.1	2.1	2.1	V
	VIH [4.5V	I _{OUT} ≤ 20μA	3.15	3.15	3.15	V
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage		2.0V		0.5	0.5	0.5	
	V	3.0V	$V_{OUT} = 0.1V \text{ or}$	0.9	0.9	0.9	V
	V _{IL}	4.5V	V _{CC} -0.1V I _{OUT} ≤ 20µA	1.35	1.35	1.35	V
		6.0V	1001 = 20 p. (1.8	1.8	1.8	





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DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{cc}	CONDITIONS	CONDITIONS		TS	LIMITS
	STWIDOL	▼ CC	CONDITIONS	25°C	85°C	FULL RANGE ⁴	UNITS
		2.0V	\/ -\/ or\/	1.9	1.9	1.9	V
		4.5V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 20 \mu A$	4.4	4.4	4.4	
		6.0V	1.0011 = = 0	5.9	5.9	5.9	
Minimum High-Level Output Voltage	V _{OH}	3.0V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 2.4 \text{mA}$	2.48	2.34	2.34	
		4.5V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 4.0 \text{mA}$	3.98	3.84	3.84	V
			6.0V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 5.2 \text{mA}$	5.48	5.34	5.34
	2.0	2.0V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 20 \mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V	1.0011 = 201.	0.1	0.1	0.1	
Maximum Low-Level Output Voltage	V _{OL}	3.0V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 2.4 \text{mA}$	0.26	0.33	0.33	
, ,		4.5V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 4.0 \text{mA}$	0.26	0.33	0.33	V
		6.0V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 5.2 \text{mA}$	0.26	0.33	0.33	
Maximum Input Leakage Current	I _{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Leakage Current	I _{cc}	6.0V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	1	10	10	μA

^{4.} 0°C ≤ T_J ≤ +85°C

AC Electrical Characteristics⁵

PARAMETER SYI	SYMBOL	V _{cc} CONDIT	CONDITIONS		LIMITS		
	OTIMBOL	• 66	CONDITIONS	25°C	85°C	FULL RANGE⁴	UNITS
Maximum Propagation Delay, Input A or B to Output Y		2.0V		75	95	95	
	t t	3.0V	$C_{L} = 50pF,$	30	40	40	ns
	t _{PLH} , t _{PHL}	4.5V	4.5V	$t_r = t_f = 6$ ns	15	19	19
(Figure 1,2)		6.0V		13	16	16	
Maximum Output Rise		2.0V		75	95	95	
and Fall Time, Any Output (Figure 1,2)	<u> </u>	3.0V	$C_{L} = 50pF,$	27	32	32	ns
	t _{TLH} , t _{THL}	4.5V	$t_r = t_f = 6$ ns	15	19	19	113
		6.0V		13	16	16	

^{5.} Not production tested in die form, characterized by chip design and tested in package.





AC Electrical Characteristics Continued⁵

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PARAMETER	SYMBOL	Voc	V _{cc} CONDITIONS		LIMIT	S	UNITS
17tto tille 12tt	01111202	• 66		25°C	85°C	FULL RANGE⁴	00
Maximum Input Capacitance	C _{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate ⁶	C _{PD}	-	$T_A = 25^{\circ}C,$ $V_{CC} = 5.0V$		TYPIC	AL	pF

^{6.} Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveform

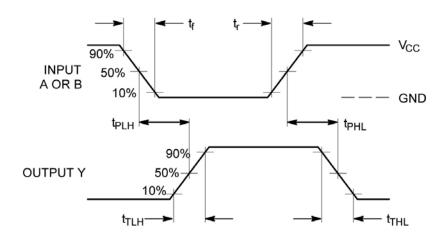
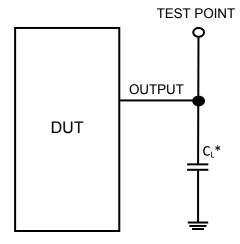


Figure 1 - Propagation Delay & Output Transition Time

Test Circuit



^{*} Includes all probe and jig capacitance

Figure 2

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