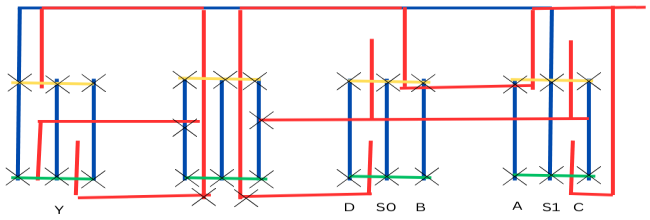
Introduction

A 4:1 multiplexer is a digital circuit that selects one of four input signals and forwards it to a single output line based on a 2-bit select code. In this project, Microwind is used to design layout of 4:1mux and analyse its timing, output voltages and working. The implementation can be done using either CMOS or pass gate technology. Pass gate based circuit helps reduce number of transistors, thus area and cost, and it can also achieve higher speeds due to the simpler structure and lower capacitance. CMOS based circuit is less susceptible to noise and voltage variations and is efficient in terms of power dissipation.

Optimized Boolean Equation

$$Y = \overline{S_1 S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$

Stick Diagram



Green: n-diffusion

Red: polysilicon

Blue: metal

Yellow: p-diffusion

Black: contact areas

V_{OL} Levels

In a 4:1 mux, V_{OL} level is constant as only one path is complete for current flow at any given time. Thus when selected input is low, it can be around 0.4 V. This works whenever the NMOS network conducts, that means any one of $\overline{S_1 S_0} I_0$, $\overline{S_1} S_0 I_1$, $S_1 \overline{S_0} I_2$, $S_1 S_0 I_3$ has to conduct, resulting three resistances in series in NMOS network. The statuses of the corresponding selection line transistors and input transistor has to be "ON" or "1". Other paths may have one or more "OFF" transistors.

For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance?

The input pattern that gives the lowest output resistance when the output is low is when the selected input is 0. This can any one of A, B, C, D depending on the selection lines.

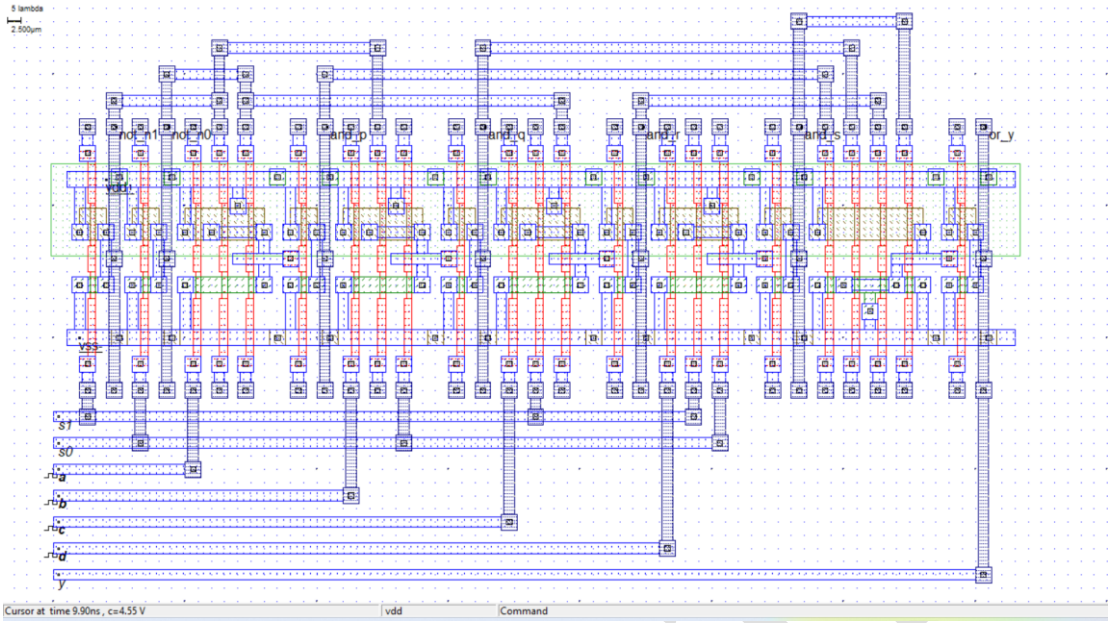
Considering given value of 20 kΩ for each transistor, it will be around 15 kΩ. This value is obtained by considering 3 transistors in series and one transistor in parallel for the inversion.

For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that resistance?

The input pattern that gives the lowest output resistance when the output is high is when the selected input is 1. This can any one of A, B, C, D depending on the selection lines.

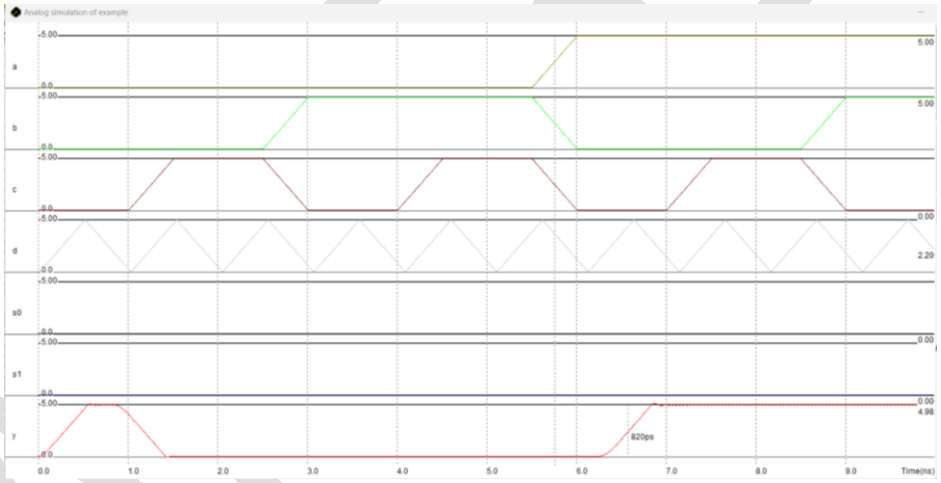
Considering given value of 20 kΩ for each transistor, it will be around 15 kΩ. This value is obtained by considering 3 transistors in series and one transistor in parallel for the inversion.

Microwind Layout

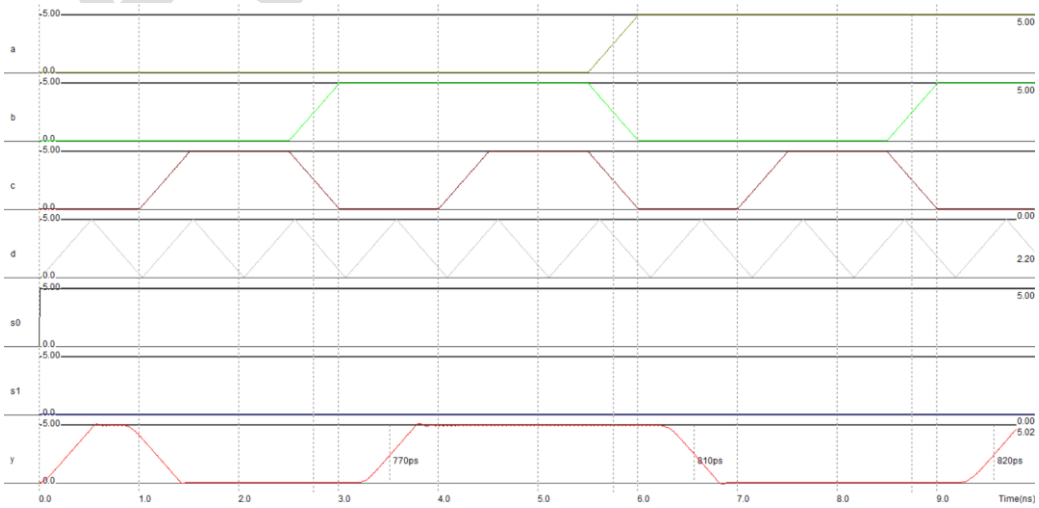


Simulations

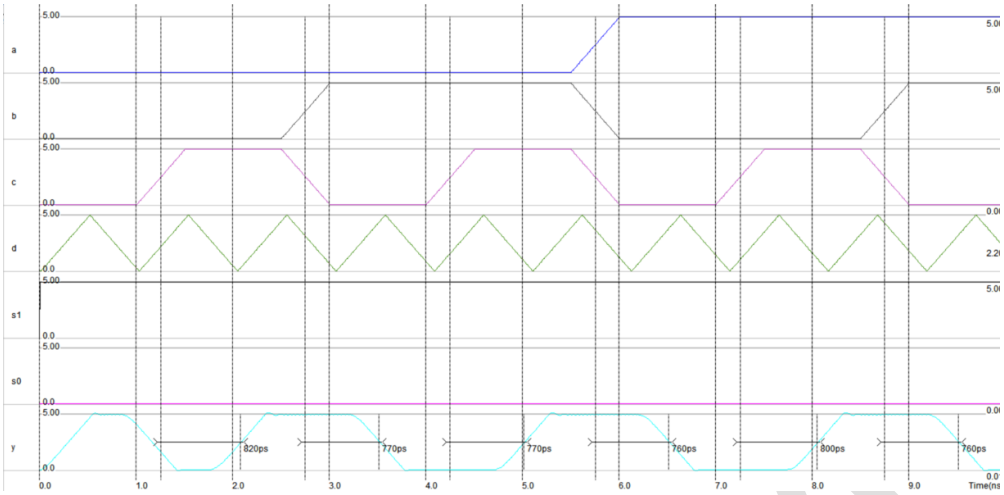
Case I: Input A, for $S_0 = 0$ and $S_1 = 0$



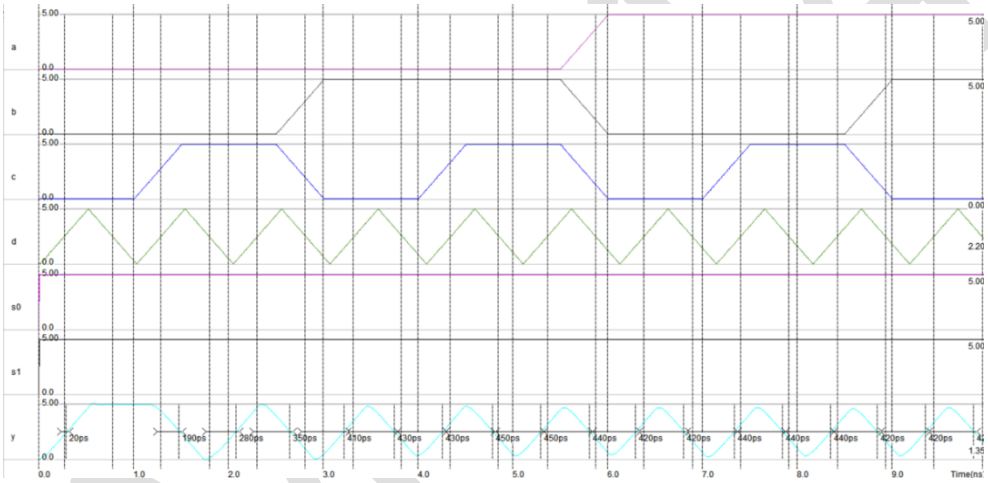
Case II: Input B, for $S_0 = 1$ and $S_1 = 0$



Case III: Input C, for $S_0 = 0$ and $S_1 = 1$



Case IV: Input D, for $S_0 = 1$ and $S_1 = 1$



Rise time, Fall time, Propagation delay

Case	Rise time	Fall time	Propagation delay
I	456 ps	456 ps	820 ps
II	520 ps	540 ps	810 ps
III	470 ps	450 ps	770 ps
IV	510 ps	490 ps	420 ps

Applications

- Data Selection: Selecting data from multiple sources based on a control signal.
- Address Decoding: Decoding memory addresses to select specific memory locations.
- Data Routing: Routing data between different parts of a digital system.
- Data Multiplexing: Combining multiple data streams into a single data stream.

Conclusion

This project successfully designed and simulated a 4:1 multiplexer using Microwind. The design process involved creating the circuit schematic using basic logic gates and then translating it into a physical layout. This involved stick diagram, structural HDL code and final layout. The simulation results validated the functionality of the 4:1 MUX, demonstrating its ability to select one of four input

signals based on the control signals. The layout design adhered to the specific technology node's design rules, ensuring manufacturability. Future work could involve exploring different implementation techniques, such as transmission gate-based designs, to optimize performance and area.

References

[1] S.-M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits Analysis and Design," McGraw-Hill International Editions, Boston, USA, 2nd Edition, 2003

[2] M. Morris Mano, R. Kime, "Logic and Computer Design Fundamentals," Pearson Education, 2nd edition, 2001