



(	)	Preliminary Specifications
(✓	)	Final Specifications

Module	15.6" (15.55") FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B156HAN07.1 (H/W:0A)
Note ( 🗭 )	LED Backlight with driving circuit design

Customer	Date
Checked & Approved by	Date
	7.00
Note: This Specification change without notice	

Approved by	Date				
Buffy Chen	<u>2018 05 18</u>				
Prepared by	Date				
<u>Brenda Lu</u>	<u>2018/05/18</u>				
NBBU Marketing Division AU Optronics corporation					

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# **Record of Revision**

Ve	rsion and Date	Page	Old description	New Description	Remark
1.0	2018/05/18	All		Final Spec	



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# **Product Specification**

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# 1. Handling Precautions

- Since front polarizer is easily damaged, pay attention not to scratch it.
- Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.





## 2. General Description

B156HAN07.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x 1080(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B156HAN07.1 is designed for a display unit of notebook style personal computer and industrial machine.

## 2.1 General Specification

Items	Unit	Specificatio	ns			
Screen Diagonal	[mm]	394.9				
Active Area	[mm]	344.16 x 193	.59			
Pixels H x V		1920 x 3(RGB) x 1080				
Pixel Pitch	[mm]	0.17925 x 0.1	7925			
Pixel Format		R.G.B. Vertic	cal Stripe	<b>*</b>		
Display Mode		Normally Blo	ack			
White Luminance (ILED= 25 mA) (Note: ILED is LED current)	[cd/m²]	300 typ. (5 p 255 min. (5 p		<b>U</b> ,		
Luminance Uniformity		1.25 max. (5	points)			
Contrast Ratio		800:1 typ				
Response Time	[ms]	9 Tvp				
Nominal Input Voltage VDD	[Volt]	+3.3 min				
Power Consumption	[Watt]	7.8 W				
Weight	[Grams]	370 max.				
Discription Circ			Min.	Тур.	Max.	
Physical Size w/ Bracket		Length	359.00	359.50	360.00	
w/ blucker	[mm]	Width	223.30	223.80	224.30	
Thicknessss	[ICIII]	Thicknessss	3.2 max			
Electrical Interface	<b>&gt;</b>	4 Lane eDP	1.4			
Glass Thickness	[mm]	0.4				
Surface Treatment		Anti Glare				
Support Color		16.7M colors	s ( RGB 8-bit	. )		
Temperature Range Operating Storage (Non-Operating)	[°C]	0 to +50 -20 to +60				
RoHS Compliance		RoHS Comp	liance			

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# 2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25% (Room Temperature) :

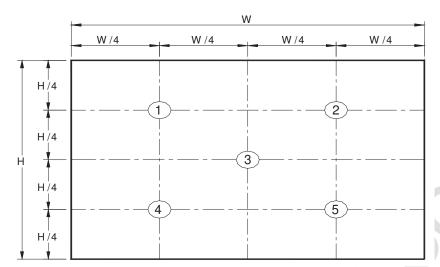
Item		Symbol	Conditions	Min.	Тур.	Max.	Unit	Note
White Luminance ILED=25 mA			5 points average	255	300	-	cd/m²	1, 4, 5.
Viewing Ar	o clo	Θ <sub>R</sub> ΘL	Horizontal (Right) CR = 10 (Left)	80 80	85 85	-	degree	
viewing Ai	igi <del>e</del>	Ψн Ψι	Vertical (Upper) CR = 10 (Lower)	80 80	85 85	-		4, 9
Luminance Un	iformity	δ <sub>5P</sub>	5 Points	-	-	1.25		1, 3, 4
Luminance Un	iformity	<b>δ</b> 13P	13 Points	-	-	1.60		2, 3, 4
Contrast Ro	atio	CR		-	800	_		4, 6
Cross tal	k	%			<b>\</b>	4		4, 7
Response Time		T <sub>RT</sub>	Rising + Falling	-	9	13		4,8
Response T	ime	T <sub>G</sub> to G			7		msec	8
	Red	Rx		0.612	0.642	0.672		
		Ry		0.308	0.338	0.368		
Color /	Green	Gx		0.292	0.322	0.352		
Chromaticity	Green	Gy	CIE 1931	0.581	0.611	0.641		
Coodinates		Bx		0.123	0.153	0.183		4
	Blue	Ву		0.016	0.046	0.076		
	VA (1-11-	Wx		0.283	0.313	0.343		
	White	Wy		0.299	0.329	0.359		
NITCO	) ITCC				70			

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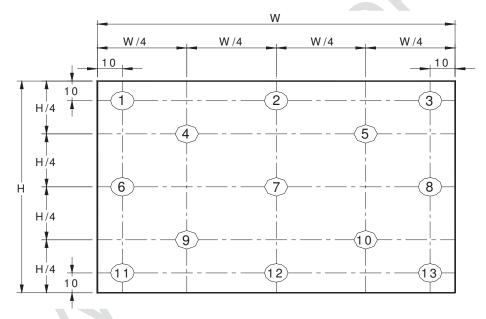


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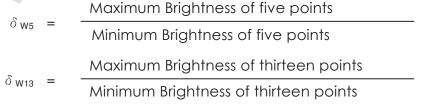
Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

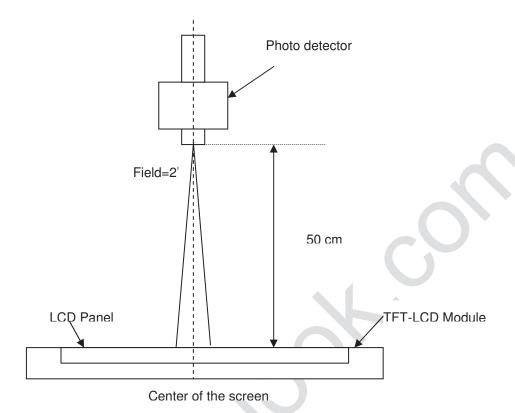


Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the



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**Note 5**: Definition of Average Luminance of White (Y<sub>L</sub>):

Measure the luminance of gray level 63 at 5 points,  $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$ L (x) is corresponding to the luminance of the point X at Figure in Note (1).

#### **Note 6**: Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

Brightness on the "White" state Contrast ratio (CR)= Brightness on the "Black" state

## Note 7: Definition of Cross Talk (CT)

$$CT = | YB - YA | / YA \times 100 (\%)$$

#### Where

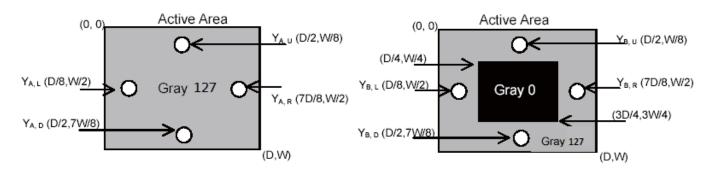
YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)



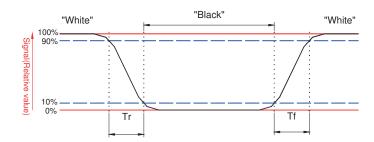
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Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



The gray to gray response time is defined as the following table.

Gray Layal to G	roy Loyal	Target gray level					
Gray Level to Gray Level		L0	L63	L127	L191	L255	
	L0						
	L63						
Start gray level	L127						
	L191						
	L255						

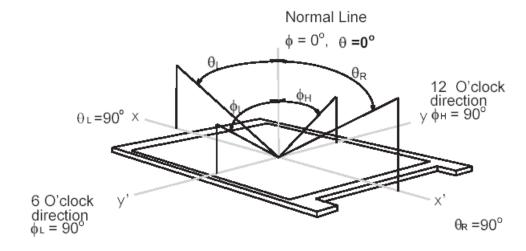
 $T_{GTG\_typ}$  is the total average time at rising time and falling time of gray to gray.

## Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.







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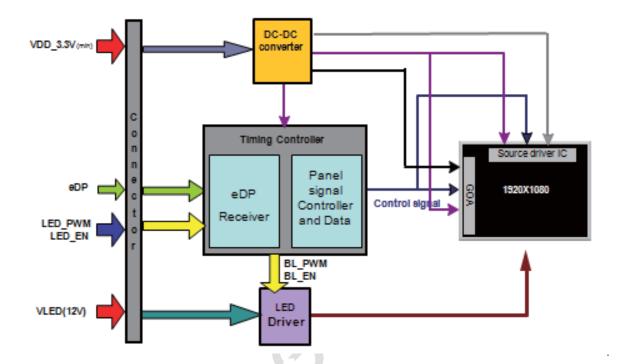




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# 3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 40 Pin (One CH/connector Module)



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# 4. Absolute Maximum Ratings

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An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Item Symbol		Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

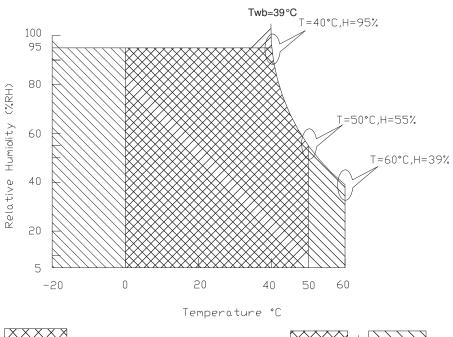
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range

Storage Range

 $+ \bigcirc$ 



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#### 5. Electrical Characteristics

#### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

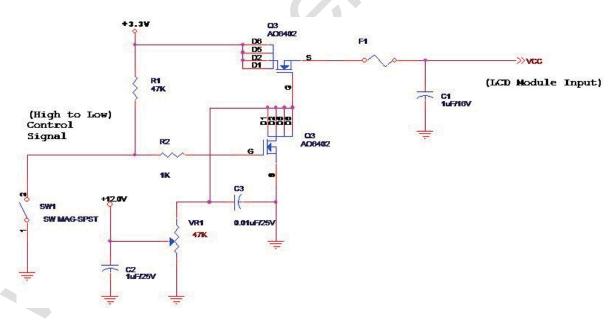
Input power specifications are as follows;

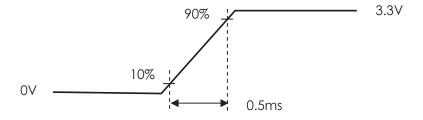
Symble	Parameter	Min	Тур	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.3	-	3.6	[Volt]	Max 1.3A
PDD	VDD Power	-	2.0	3.6	[Watt]	Note 1
IDD	IDD Current	-	-	1090	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	<b>*</b>

Note 1: PDD(typ)@ mosaic pattern Maximum Power; PDD(Max)@ R/G/B pattern Maximum Power

IDD(Max)=PDD(Max) / VDD(Min)

Note 2: Measure Condition





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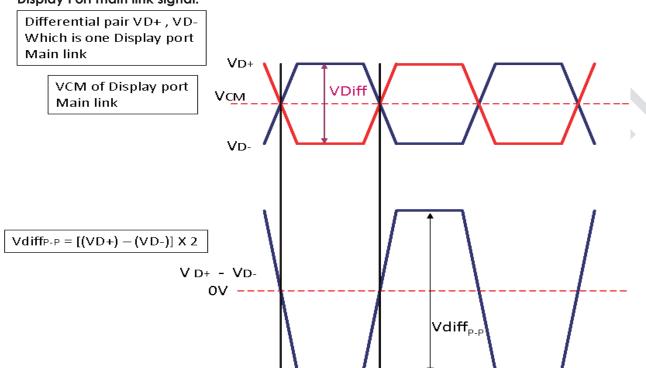


# 5.1.2 Signal Electrical Characteristics

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Signal electrical characteristics are as follows;

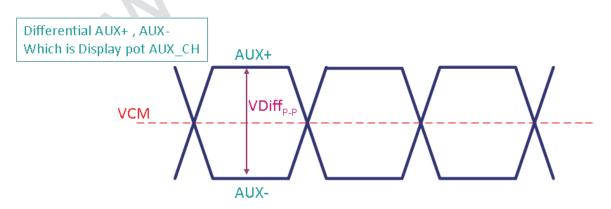
## Display Port main link signal:



	Display port main link				
		Min	Тур	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff <sub>P-P</sub>	Peak-to-peak Voltage at a receiving Device	75		1320	mV

Follow as VESA display port standard V1.4

## Display Port AUX\_CH signal:



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	Display port AUX_CH				
		Min	Тур	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff <sub>P-P</sub>	AUX Peak-to-peak Voltage at a receiving Device	270		800	mV

Follow as VESA display port standard V1.3

## Display Port VHPD signal:

	Display port VHPD				
		Min	Тур	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	V

Follow as VESA display port standard V1.3



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# **Product Specification**

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# 5.2 Backlight Unit

## 5.2.1 LED characteristics

Parameter	Symbol	Min	Тур	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	5.8	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	- Hour (Ta=25°C), Not		(Ta=25°C), Note 2 I <sub>F</sub> =25 mA

Note 1: Calculator value for reference PLED = VF (Normal Distribution) \* IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

# 5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Тур	Max	Units	Remark
LED Power Supply	VLED	7.0	12.0	21.0	[Volt]	
LED Enable Input High Level	VLED_EN	2.5	-	3.6	[Volt]	
LED Enable Input Low Level	7225_21	-	-	0.5	[Volt]	Define
PWM Logic Input High Level	VPWM_EN	2.5	-	3.6	[Volt]	Define as Connector
PWM Logic Input Low Level		-	-	0.5	[Volt]	Interface (Ta=25°C)
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5		100	%	

Note 1: Recommend system pull up/down resistor no bigger than 10kohm





# 6. Signal Interface Characteristic

# 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

	I						15	20	1
1st Line	R G B	R G B		R	G	В	R	G	В
	' '	'							
1080th Line	R G B	R G B	. (2)	R	G	В	R	G	В





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## **6.2 Integration Interface Requirement**

## **6.2.1 Connector Description**

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	STM or compatible
Type / Part Number	MSAK24025P40 or compatible
Mating Housing/Part Number	I-PEX 20453-040T-11 or compatible

## 6.2.2 Pin Assignment

PIN NO	Symbol	Function
1	NC	NO Connect
2	H_GND	High Speed Ground
3	Lane3_N	Comp Signal Lane3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Comp Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Comp Signal Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Comp Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Ch.
16	AUX_CH_N	Comp Signal Auxiliary Ch.
17	H_GND	High Speed Ground
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	LCD_Self_Test	LCD Panel Self Test Enable
23	ICD GND	I CD logic and driver around





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24	LCD GND	LCD logic and driver ground
25	LCD GND	LCD logic and driver ground
26	LCD GND	LCD logic and driver ground
27	HPD	HPD signale pin
28	BL_GND	Backlight_ground
29	BL_GND	Backlight_ground
30	BL_GND	Backlight_ground
31	BL_GND	Backlight_ground
32	BL_Enable	Backlight On / Off
33	BL PWM DIM	System PWM signal Input
34	NC	NC
35	NC	NC
36	BL_PWR	Backlight power
37	BL_PWR	Backlight power
38	BL_PWR	Backlight power
39	BL_PWR	Backlight power
1		

No Connect (Reserved for CM)

Note1 : start from right side

NC

40

 ${\tt Note 2: Input \ signals \ shall \ be \ low \ or \ High-impedance \ state \ when \ VDD \ is \ off.}$ 







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# **6.3 Interface Timing**

For normal display, interface timings should match the 1920x1080 /144Hz manufacturing guide line timing.

Parar	neter	Symbol	Min.	Тур.	Max.	Unit
Frame	e Rate	-	-	144	-	Hz
Clock fre	equency	1/TClock	-	368.14	-	MHz
	Period	T <sub>V</sub>	-	1222	-	
Vertical	Active	<b>T</b> VD		1080		<b>T</b> Line
Section	Blanking	T∨B	-	142	-	
	Period	T <sub>H</sub>	-	2092	-	
Horizontal	Active	<b>T</b> HD		1920		<b>T</b> Clock
Section	Blanking	<b>T</b> HB	-	172	-	

Note 1: The above is as optimized setting

Note 2: The maximum clock frequency = (1920+B)\*(1080+A)\*144=368,14MHz



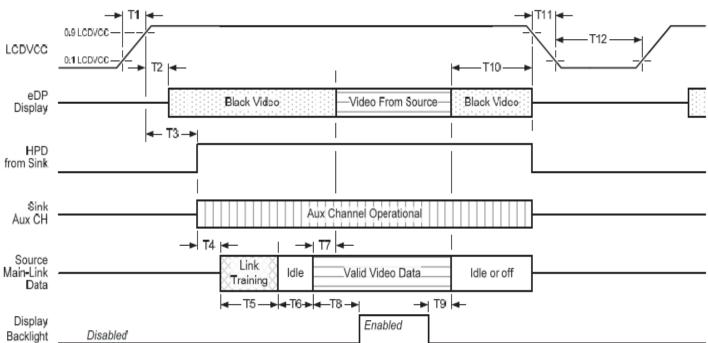


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6.4 Power ON/OFF Sequence

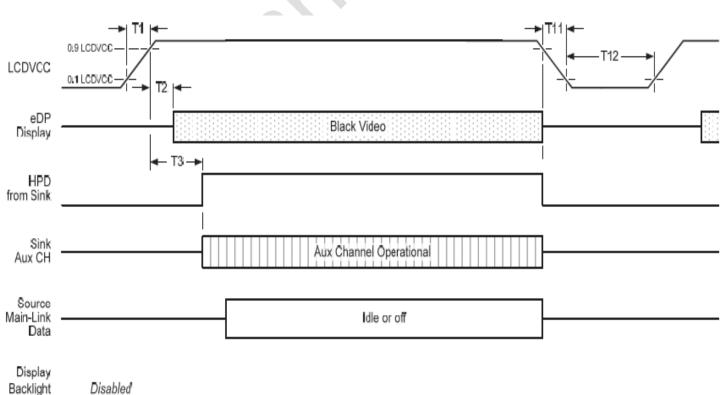
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

## Display Port panel power sequence:



#### Display port interface power up/down sequence, normal system operation

## Display Port AUX\_CH transaction only:



Display port interface power up/down sequence, AUX\_CH transaction only





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Display Port panel power sequence timing parameter:

Timing	Description	Don't be	Limits			Natas
parameter	Description	Reqd. by	Min.	Тур.	Max.	Notes
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
Т2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
Т3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
Т5	link training duration	source				dependant on source link to read training protocol.
Т6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
Т7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
Т8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
Т9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

**Note1:** The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

- -upon LCDVDD power on (with in T2 max)-when the "Novideostream\_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
- -when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

**Note 2:** The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

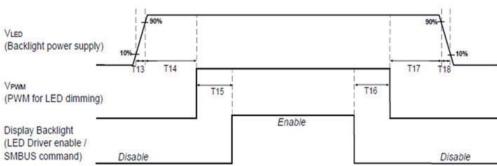
**Note 3:** The sink must support AUX\_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX\_CH transaction with the time specified within T3 max.



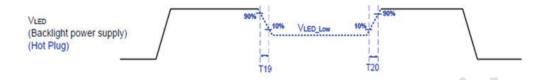


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## Display Port panel B/L power sequence timing parameter:



Note: When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	
T15	10	200
T16	10	=
T17	10	-
T18	0.5	10
T19	1*	
T20	1*	. 9

Seamless change: T19/T20 = 5xT<sub>PWM</sub>\*

\*T<sub>PWM</sub>= 1/PWM Frequency





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# 7. Panel Reliability Test

## 7.1 Vibration Test

## **Test Spec:**

Test method: Non-Operation

Acceleration: 1.5 G

• Frequency: 10 - 500Hz Random

• Sweep: 30 Minutes each Axis (X, Y, Z)

#### 7.2 Shock Test

#### **Test Spec:**

Test method: Non-Operation

Acceleration: 220 G , Half sine wave

Active time: 2 ms

Pulse: X,Y,Z .one time for each side

## 7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta=0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 250h	
Thermal Shock Test	Ta=-20°C(30min) ~60°C(30min), 100cycles condition.	
ESD	Contact : ±8 KV	Note 1
	Air: ±15 KV	

**Note1:** According to EN 61000-4-2, ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

nventory and accessory: Www.panelook.com

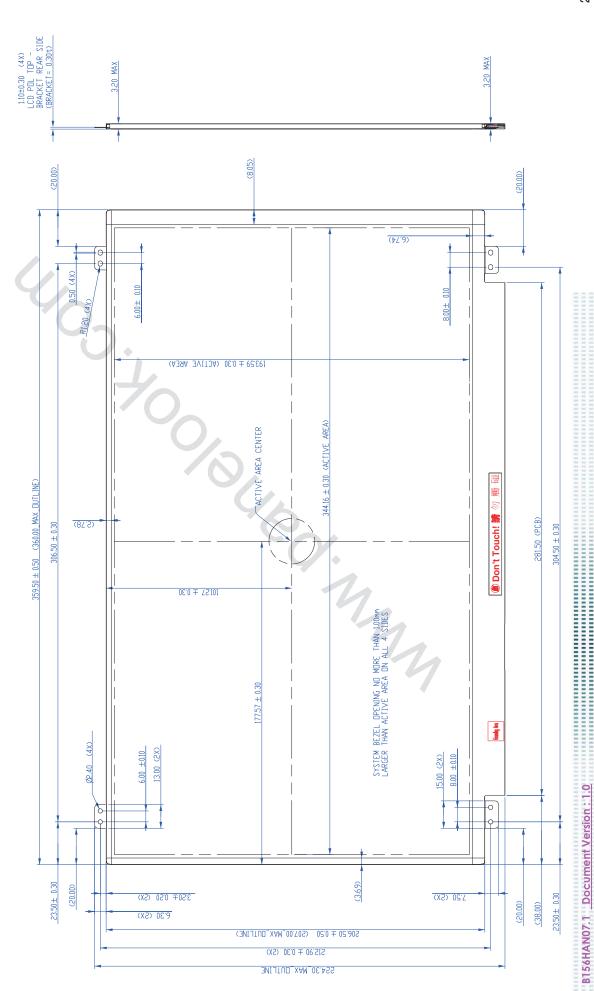
屏庫:全球液晶屏交易中心



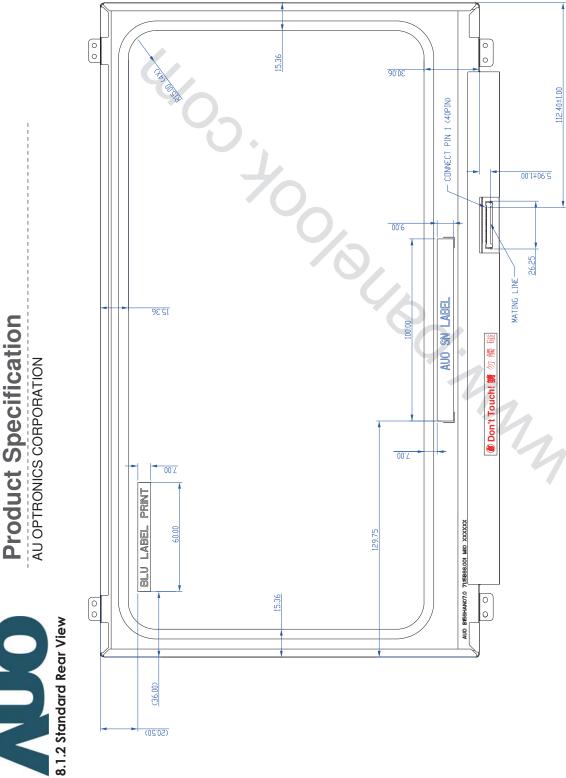
# **Product Specification**

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- 8. Mechanical Characteristics
- 8.1 LCM Outline Dimension
  - 8.1.1 Standard Front View



(50.50)





9. Shipping and Package

9.1 Shipping Label Format

Manufactured MM/WW Model No: B156HANØ7.1 **AU Optronics** 

MADE IN CHINA(\$01)

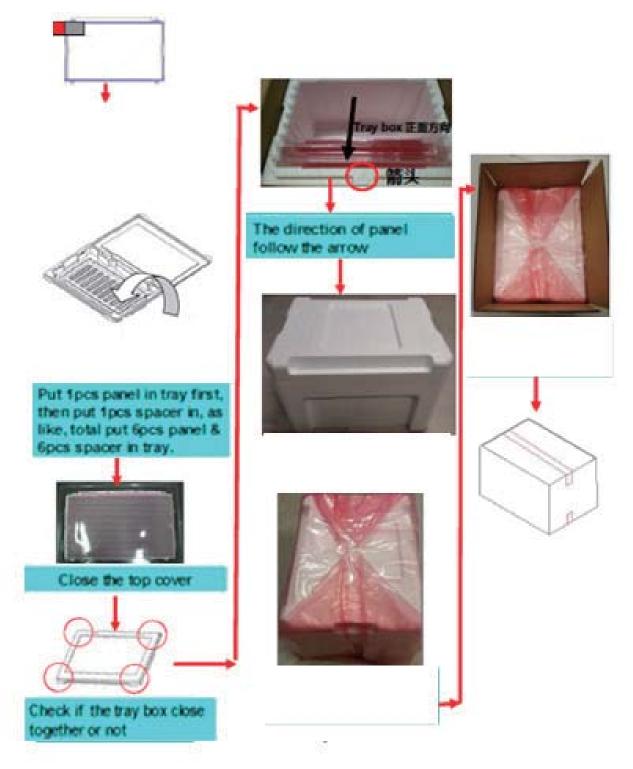






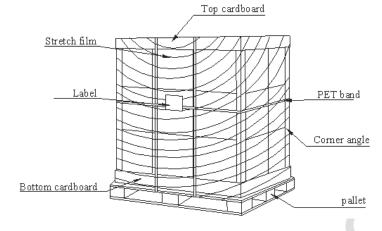


# 9.2 Carton Package





# 9.3 Shipping Package of Palletizing Sequence







# 10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	111111111	255	
02		FF	111111111	255	
03		FF	111111111	255	
04		FF	111111111	255	
05		FF	111111111	255	
06		FF	111111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	ED	11101101	237	
0B	hex, LSB first	71	01110001	113	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	10	00010000	16	
11	Year of manufacture	1B	00011011	27	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	Video input def. (digital I/P, non-TMDS, CRGB)	A5	10100101	165	
15	Max H image size (rounded to cm)	22	00100010	34	
16	Max V image size (rounded to cm)	13	00010011	19	
17	Display Gamma (=(gamma*100)-100)	78	01111000	120	
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	02	00000010	2	
19	Red/green low bits (Lower 2:2:2:2 bits)	6A	01101010	106	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	75	01110101	117	
1B	Red x (Upper 8 bits)	A4	10100100	164	
1C	Red y/ highER 8 bits	56	01010110	86	
1D	Green x	52	01010010	82	
1E	Green y	9C	10011100	156	
1F	Blue x	27	00100111	39	
20	Blue y	0B	00001011	11	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	

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29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B	Ĭ i	01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	CE	11001110	206	
37	Pixel Clock/10000 USB	8F	10001111	143	
38	Horz active Lower 8bits	80	10000000	128	
39	Horz blanking Lower 8bits	AC	10101100	172	
3A	HorzAct:HorzBlnk Upper 4:4 bits	70	01110000	112	
3B	Vertical Active Lower 8bits	38	00111000	56	
3C	Vertical Blanking Lower 8bits	8E	10001110	142	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	40	01000000	64	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	A5	10100101	165	
41	Horz‖ Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	58	01011000	88	
43	Vertical Image Size Lower 8bits	C1	11000001	193	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border (zero for internal LCD)	00	00000000	0	
46	Vertical Border (zero for internal LCD)	00	00000000	0	
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24	
48	Pixel Clock/10,000 (LSB)	CE	11001110	206	
49	Pixel Clock/10,000 (MSB)	8F	10001111	143	40Hz frame rate
4A	Horizontal Addressable Pixels, lower 8 bits	80	10000000	128	
4B	Horizontal Blanking Pixels, lower 8 bits	AC	10101100	172	
4C	H Pixels, upper nibble : H Blanking, upper nibble	70	01110000	112	
4D	Vertical Addressable Lines, lower 8 bits	38	00111000	56	
4E	Vertical Blanking Lines, lower 8 bits	3A	00111010	58	
4F	V lines, upper nibble : V blanking, upper nibble	47	01000111	71	
50	Horizontal Front Porch, lower 8 bits	30	00110000	48	
51	Horizontal Sync Pulse, lower 8 bits	20	00100000	32	
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	A5	10100101	165	
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0	
54	Horizontal Image Size in mm, lower 8 bits	58	01011000	88	
55	Vertical Image Size in mm, lower 8 bits	C1	11000001	193	
56	H Image Size, upper nibble : V Image Size, upper nibble	10	00010000	16	
57	Horizontal Border	00	00000000	0	

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58	Vertical Border	00	00000000	0	
59	Bit Encode Sync Information	18	00011000	24	
	DC				
5A	HTOTAL	00	00000000	0	
5B	НА	00	00000000	0	
5C		00	00000000	0	
5D	HBL	00	00000000	0	
5E	HFP	00	00000000	0	
5F	HFPe	00	00000000	0	
60	HBP	00	00000000	0	
61	НВ	00	00000000	0	
62	HSO	00	00000000	0	nVDPS
63	HS	00	00000000	0	Reserved 00
64	VTOTAL	00	00000000	0	
65	VA	00	00000000	0	
66	VBL	00	00000000	0	
67	VFP	00	00000000	0	
68	VBP	00	00000000	0	
69	VB	00	00000000	0	
6A	VSO	00	00000000	0	
6B	VS	00	00000000	0	
6C	Detail Timing Description #4	00	00000000	0	
6D	Flag	00	00000000	0	
6E	Reserved	00	00000000	0	
6F	For Brightness Table and Power Consumption	02	00000010	2	
70	Flag	00	00000000	0	Header
71	PWM % [7:0] @ Step 0	10	00010000	16	
72	PWM % [7:0] @ Step 5	36	00110110	54	
73	PWM % [7:0] @ Step 10	FF	11111111	255	
74	Nits [7:0] @ Step 0	0F	00001111	15	
75	Nits [7:0] @ Step 5	3C	00111100	60	
76	Nits [7:0] @ Step 10	96	10010110	150	Brightness Table
77	Panel Electronics Power @ 32x32 Chess Pattern =	24	00100100	36	
78	Backlight Power @ 60 nits =	14	00010100	20	
79	Backlight Power @ Step 10 =	33	00110011	51	
7A	Nits @ 100% PWM Duty =	96	10010110	150	Power Consumption
7B	Flag	20	00100000	32	
7C	Flag	20	00100000	32	
7D	Flag	20	00100000	32	
7E	Extension Flag	00	00000000	0	
7F	Checksum	1C	00011100	28	

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