Introduction to Digital Systems
Part III (Sequential Components)
2021/2022

Sequential Logic Fundamentals
and Basic Circuits

Arnaldo Oliveira, Augusto Silva, Iouliia Skliarova

Lecture Contents

- Sequential logic circuits fundamentals
  - Motivation and concepts
- Sequential logic basic circuits (memory elements built with ordinary gates and feedback loops)
  - S-R Latch
  - D Latch
  - D Flip-flop

Figures and most content extracted from: John F. Wakerly, "Digital Design – Principles and Practices", 4 ed., Pearson – Prentice Hall, 2006 (chapter 7). Reading chapter 7 (4th ed.) or chapter 10 (5th ed.) is highly recommended.

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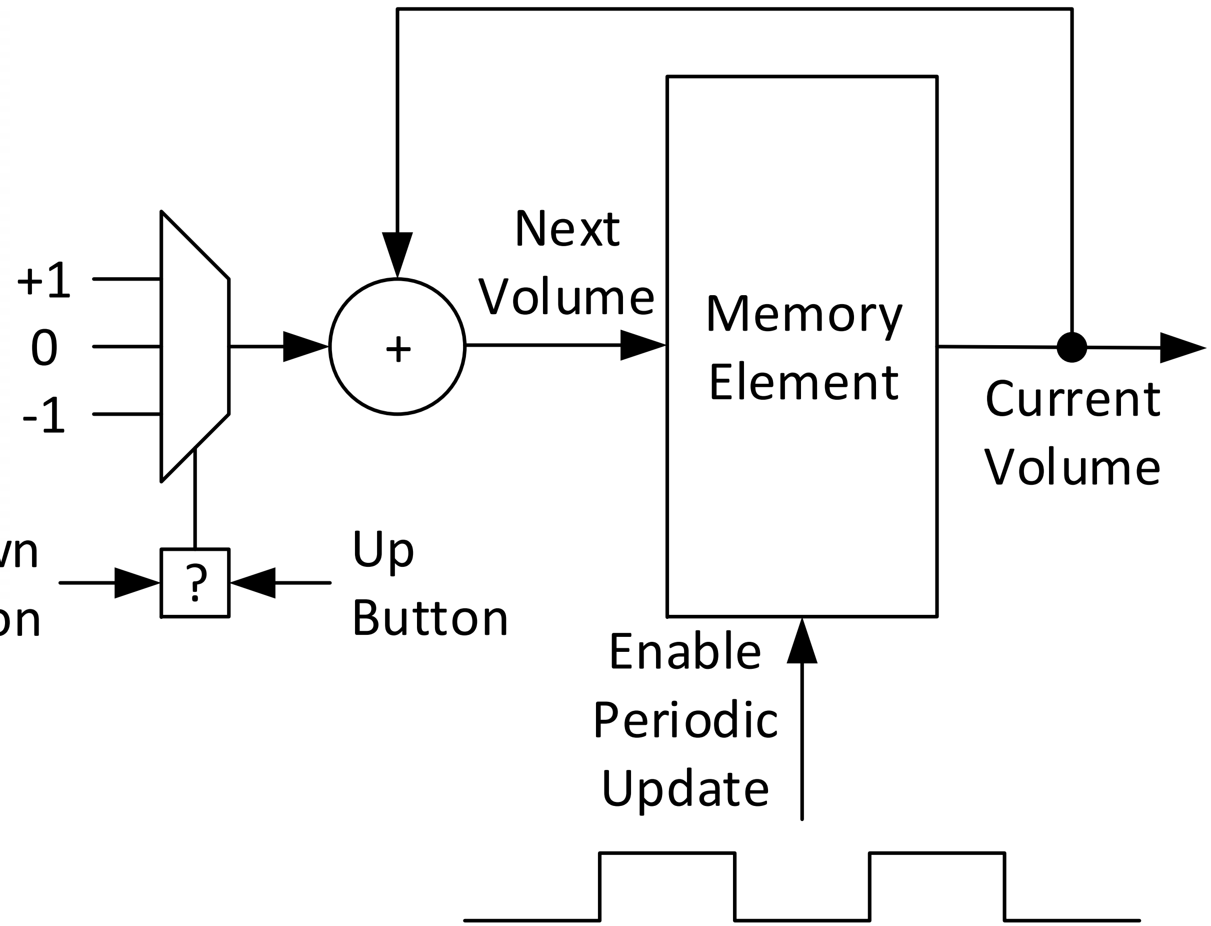
Sequential Circuit Example

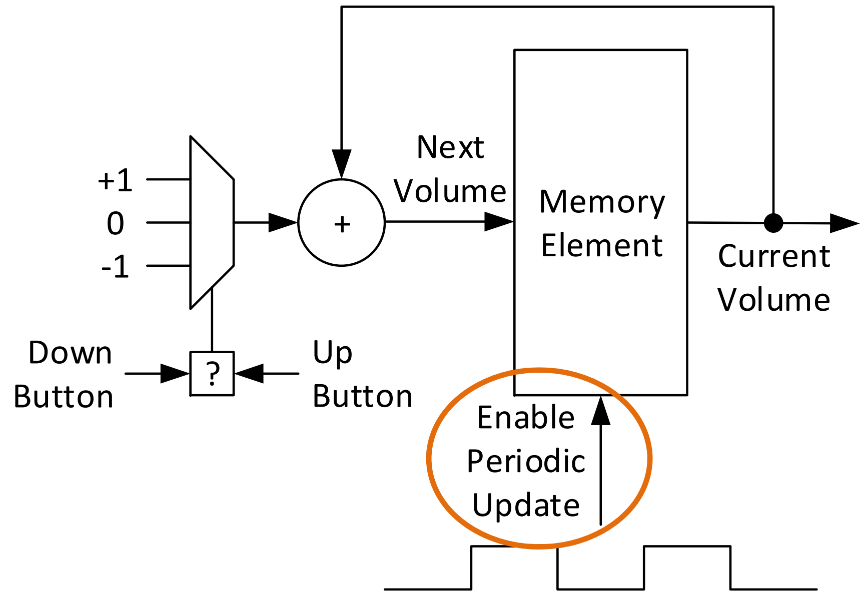


Introduction

- **Combinatorial** logic circuit
  - Is one whose outputs depend only on its current inputs
- **Sequential** logic circuit
  - Is one whose outputs depend not only on its current inputs, but also on the past sequence of inputs, possibly far back in time
- **State** of a sequential circuit
  - Is a collection of state variables whose values at any one time contain all the information about the past, necessary to account for the circuit's future behavior
- N-bit state variable: 2^N maximum number of states

Clock Signals

- State changes of most sequential circuits occur at times specified by a free-running clock signal
- Active high / active low clock signals



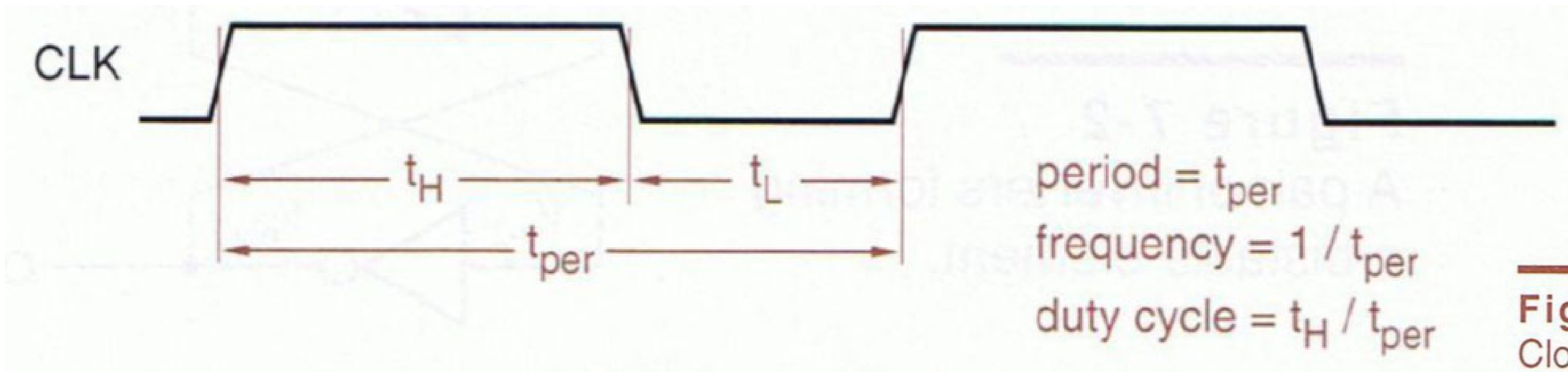
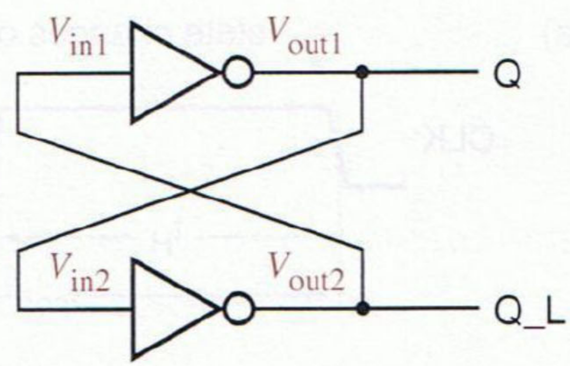


Figure 7-1
Clock signals:

Bistable Element (Basic Structure)

- No inputs and therefore no way of controlling or changing its state (random set at power up)
- Only illustrative but serves the basis for more complex and useful memory elements

Figure 7-2
A pair of inverters forming a bistable element.



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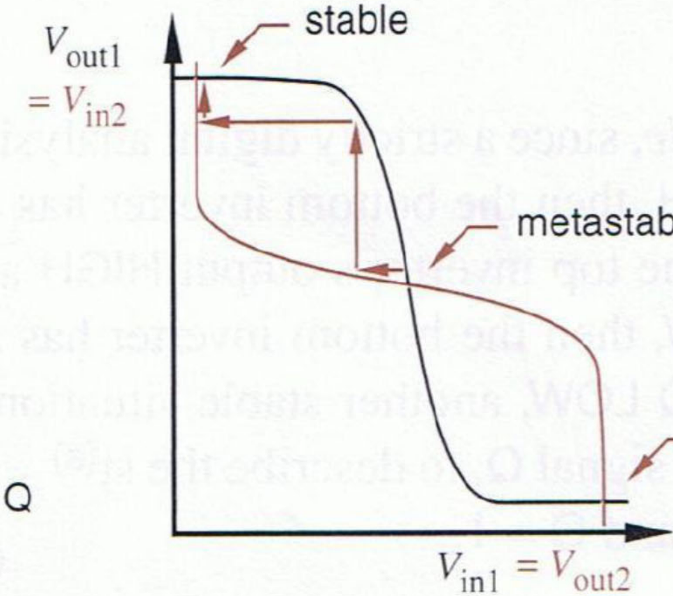
Bistable Element (Analog Analysis)

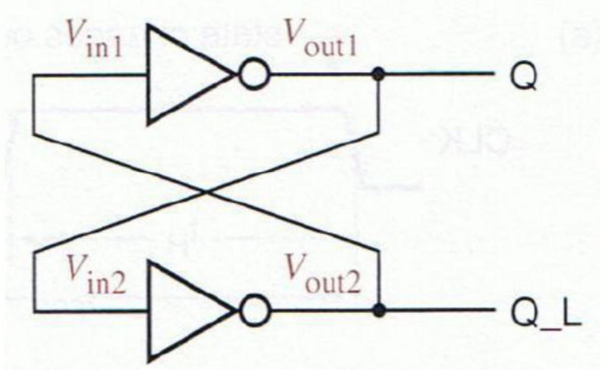
Figure 7-3
Transfer functions for inverters in a bistable feedback loop.



Transfer function:

$V_{out1} = T(V_{in1})$

$V_{out2} = T(V_{in2})$

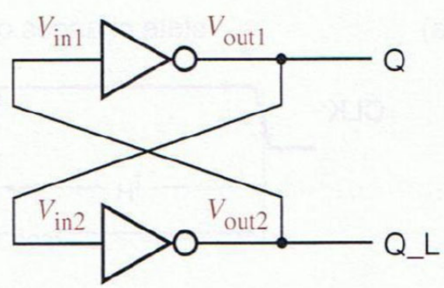


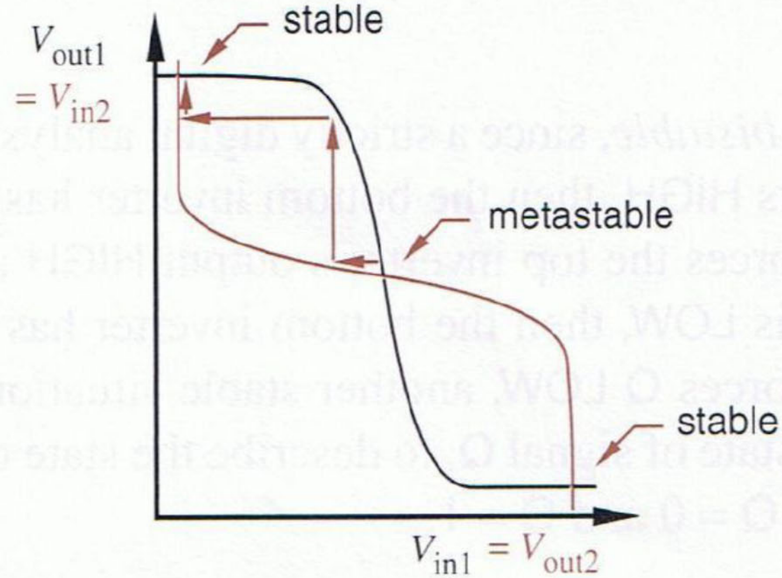
$$
\begin{aligned}
V_{in1} &= V_{out2} \\
&= T(V_{in2}) \\
&= T(V_{out1}) \\
&= T(T(V_{in1}))
\end{aligned}
$$

3 equilibrium points: 2 stable and 1 metastable

Metastability

Figure 7-3
Transfer functions for inverters in a bistable feedback loop.





Transfer function:

$$V_{out1} = T(V_{in1})$$

$$V_{out2} = T(V_{in2})$$

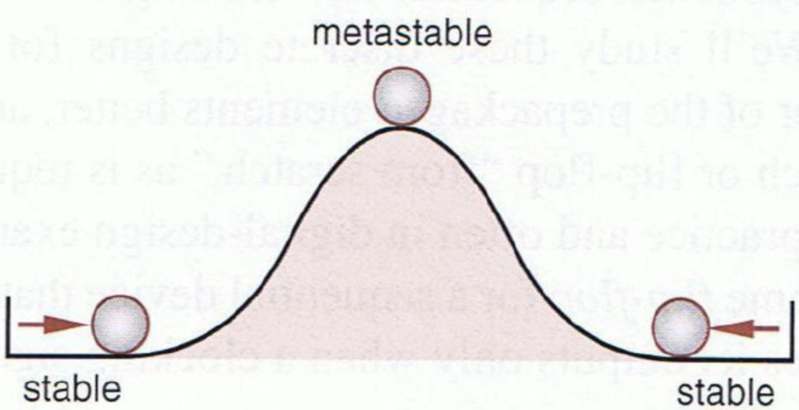
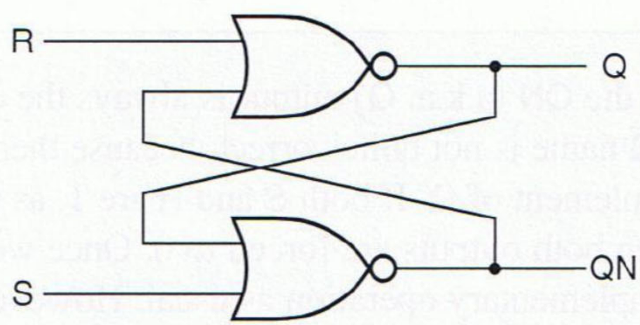


Figure 7-4
Ball and hill analogy for metastable behavior.

Effects of noise and circuit impairments on metastability

S-R Latch
(Structure and Function Table)

(a)



(b)

S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

Figure 7-5
S-R latch: (a) circuit design using NOR gates; (b) function table.

S-R Latch
(Operation/Timing Diagrams)

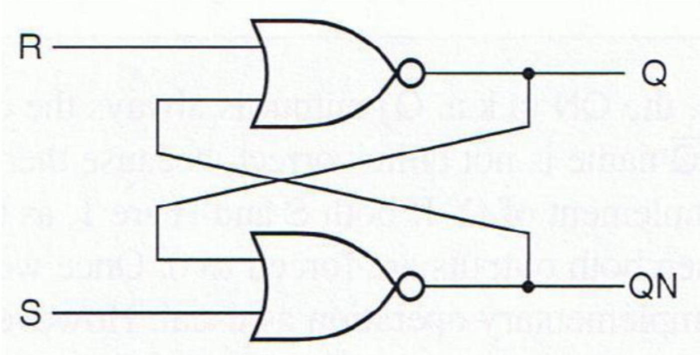
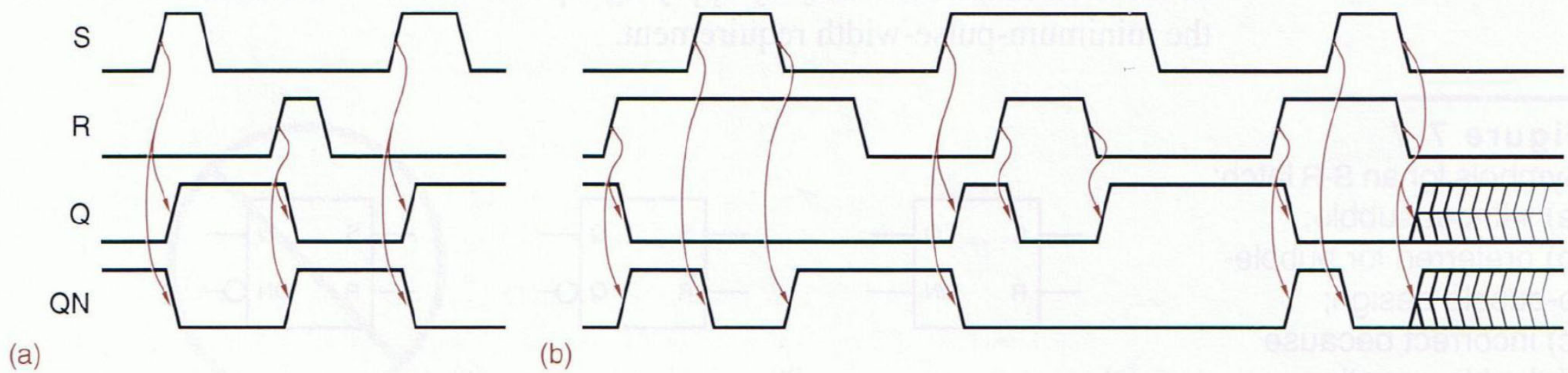


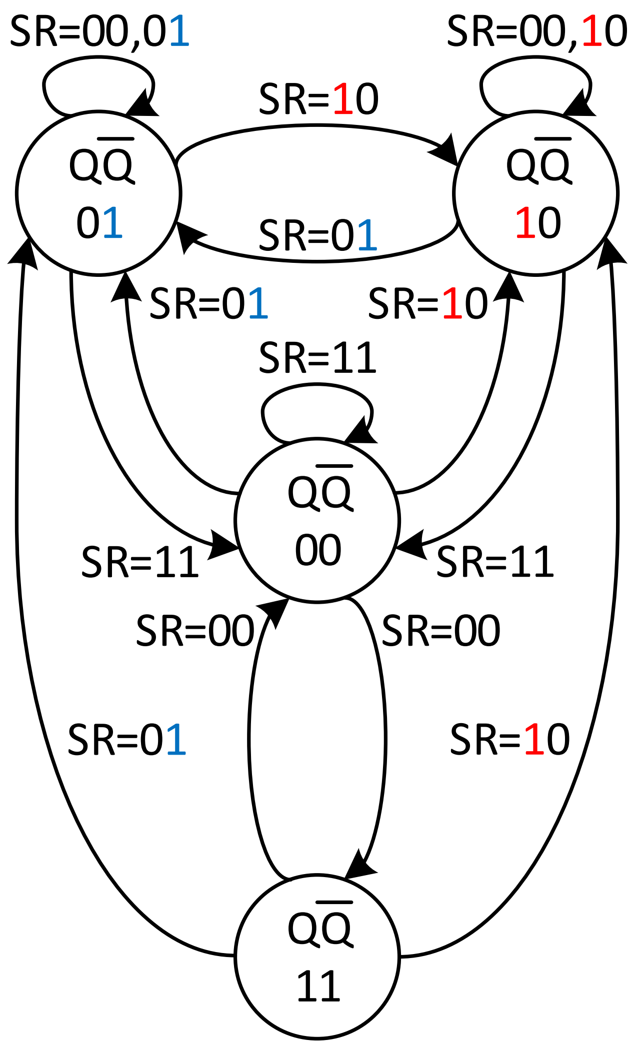
Figure 7-6 Typical operation of an S-R latch: (a) "normal" inputs; (b) S and R asserted simultaneously.

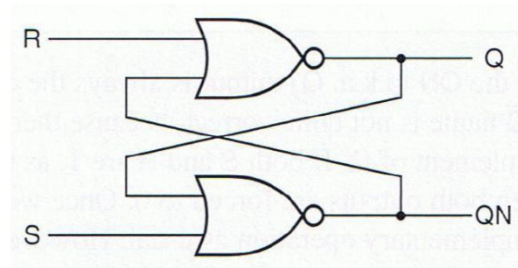


S-R Latch

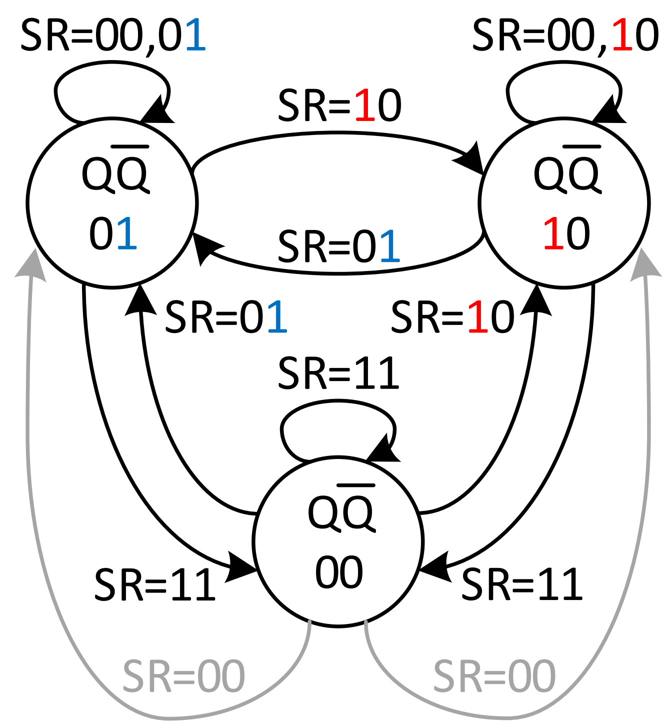
(State Diagram)

Theoretical



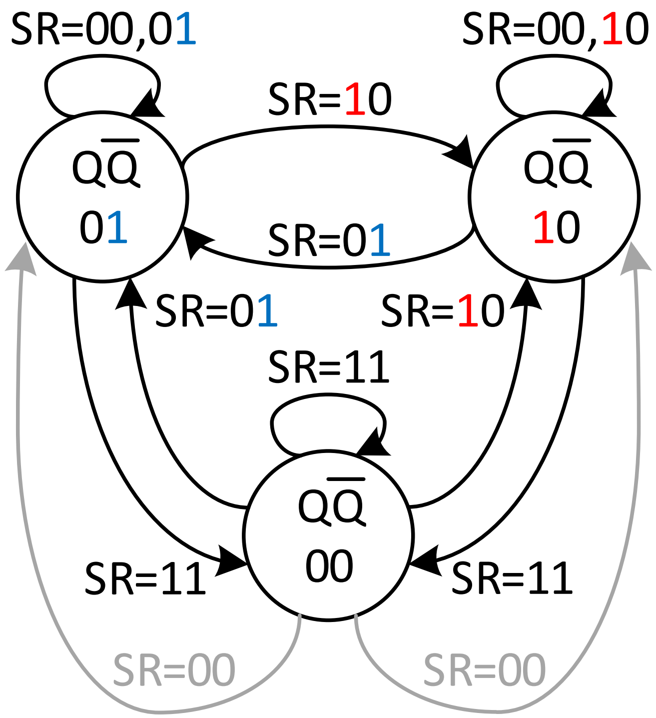


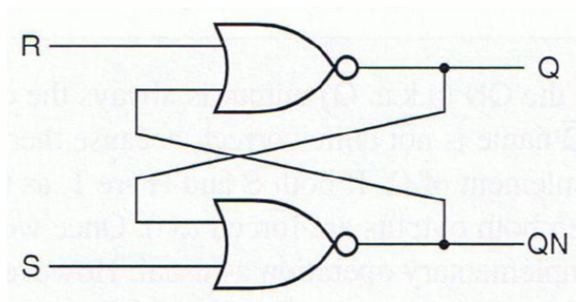
Real



S-R Latch
(Characteristic Equation)

Real



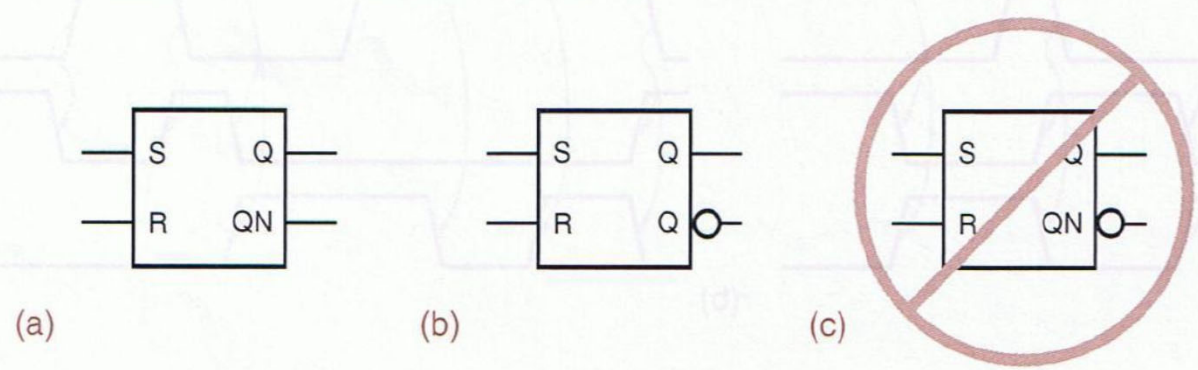


Q \ SR	00	01	11	10
0	0	0	X	1
1	1	0	X	1

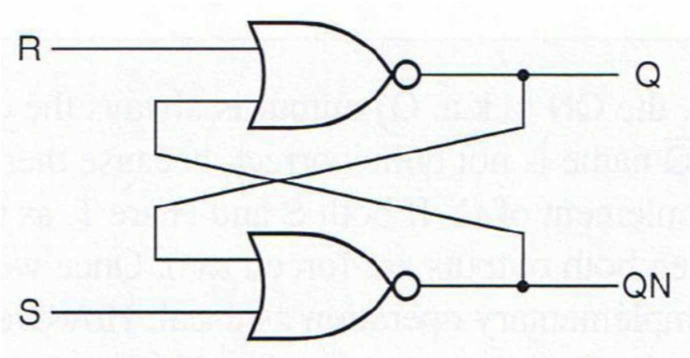
$Q^{+} = S + Q.\overline{R}$

S-R Latch (Symbol)

Figure 7-7
Symbols for an S-R latch:
(a) without bubble;
(b) preferred for bubble-to-bubble design;
(c) incorrect because of double negation.



S-R Latch (Timing Parameters)



- t_{pLH} – propagation time LOW-to-HIGH
- t_{pHL} – propagation time HIGH-to-LOW
- $T_{pw(min)}$ – minimum pulse width

Non-determinism/metastability due to violation of $T_{pw(min)}$

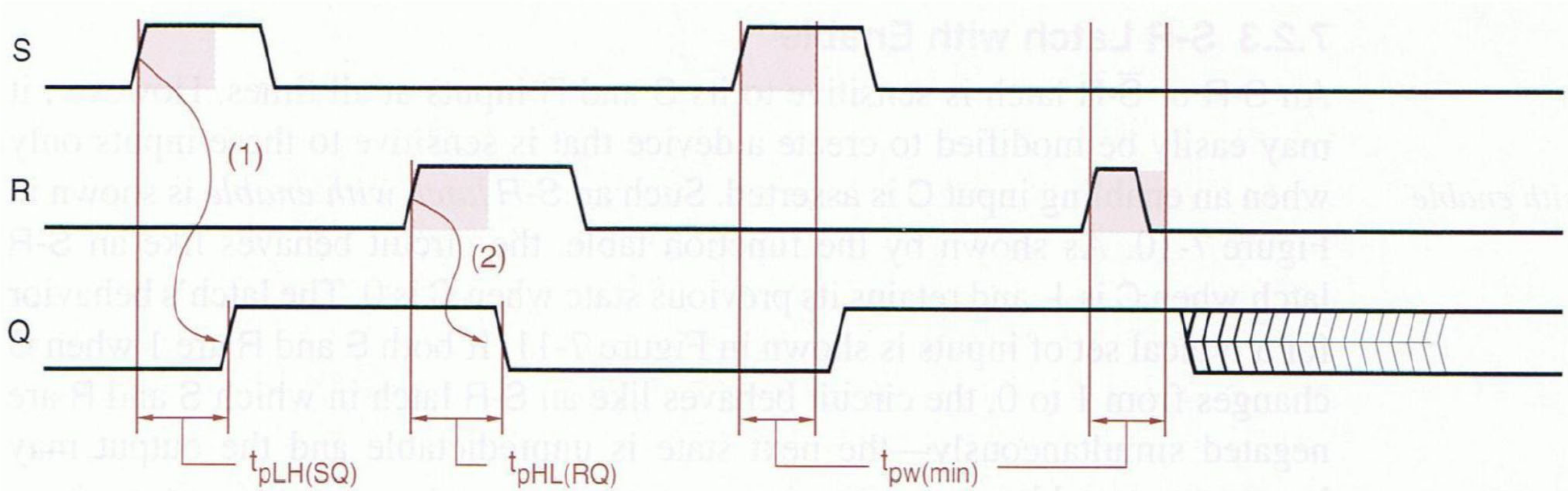
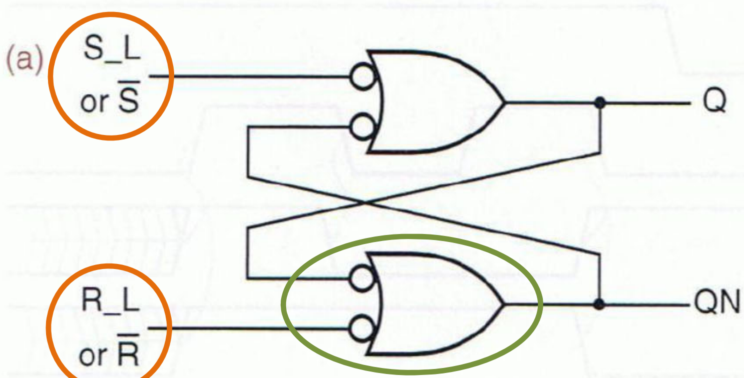
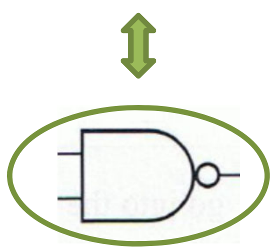


Figure 7-8 Timing parameters for an S-R latch.

S-R Latch (with NAND Gates)

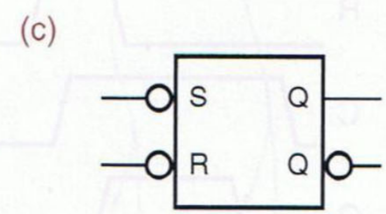
Figure 7-9 $\overline{S}$-$\overline{R}$ latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.





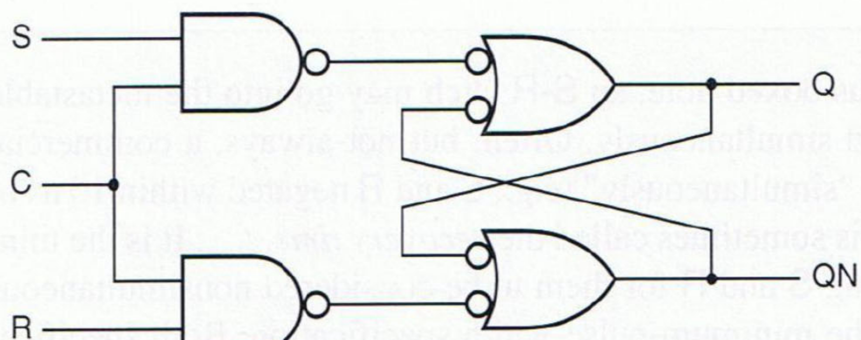
(b)

S_L	R_L	Q	QN
0	0	1	1
0	1	1	0
1	0	0	1
1	1	last Q	last QN



S-R Latch with Enable (C)

(a)



(b)

S	R	C	Q	QN
0	0	1	last Q	last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
x	x	0	last Q	last QN

(c)

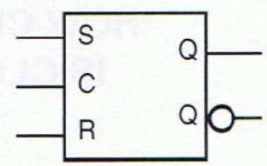


Figure 7-10 S-R latch with enable: (a) circuit using NAND gates; (b) function table; (c) logic symbol.

S-R Latch with Enable (Operation)

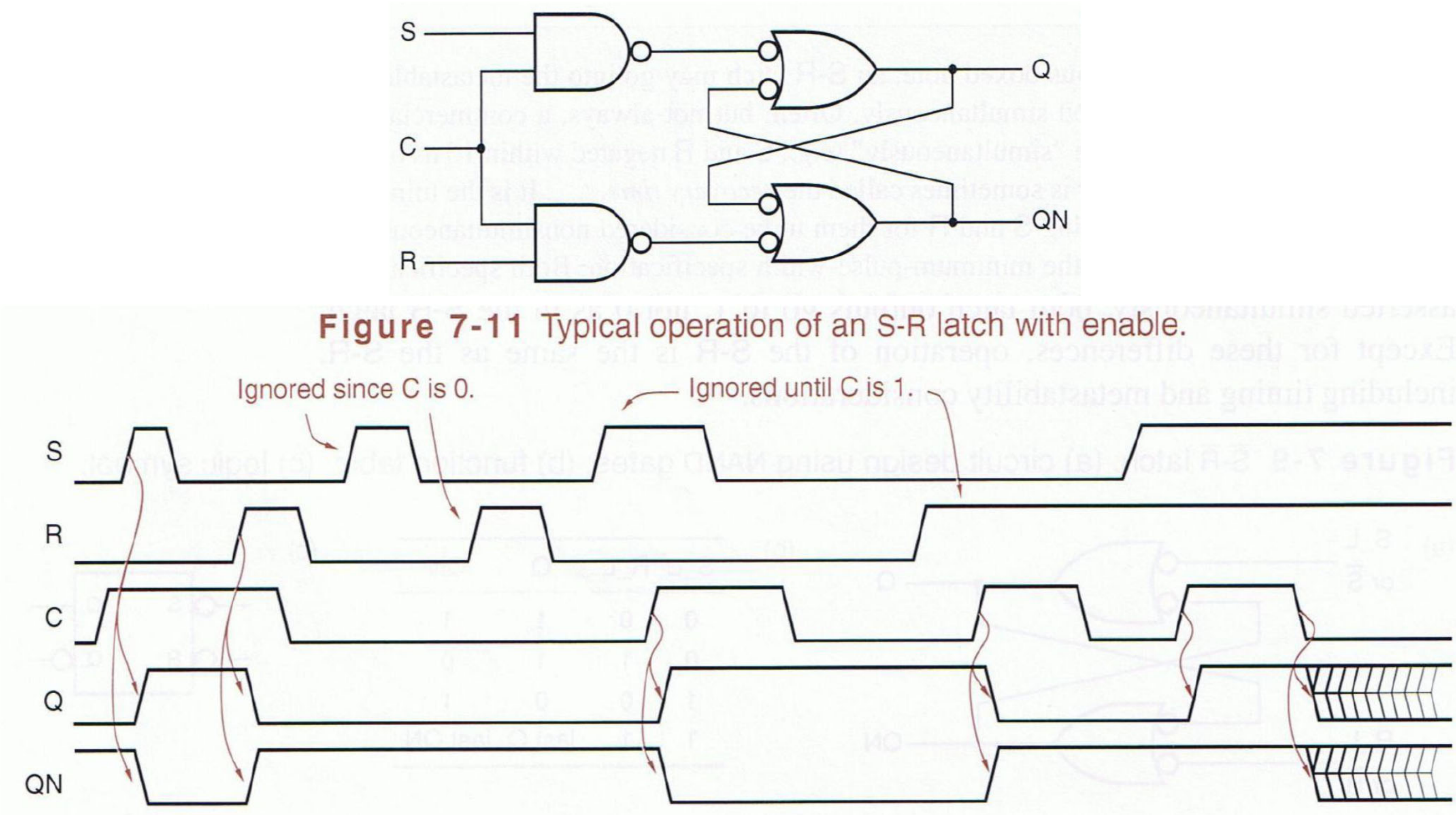
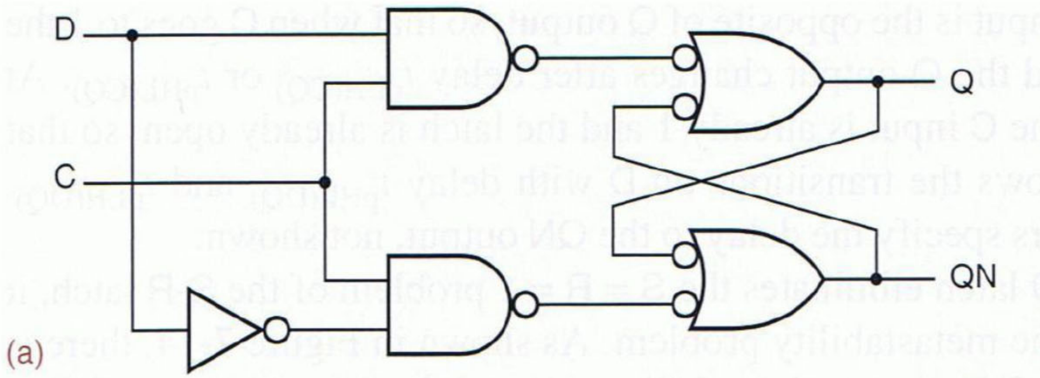


Figure 7-11 Typical operation of an S-R latch with enable.

D Latch (Structure and Operation)



(b)

C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	last Q	last QN

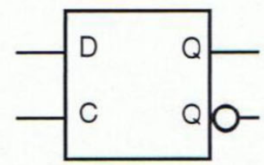


Figure 7-12 D latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.

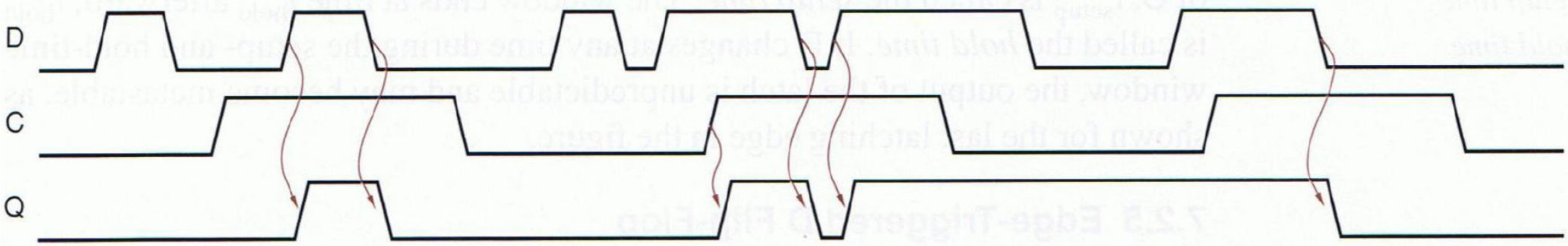
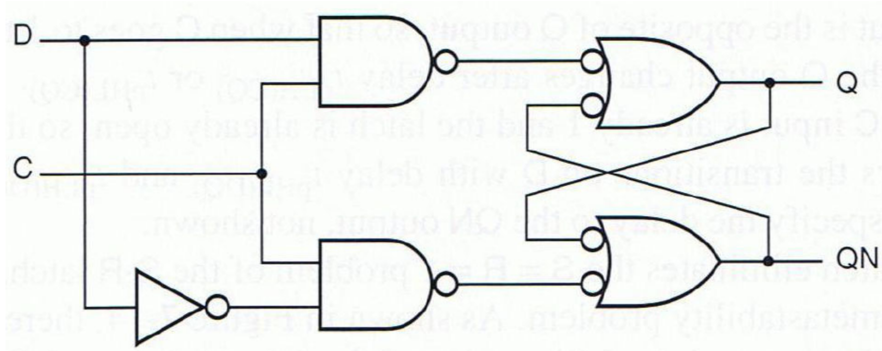
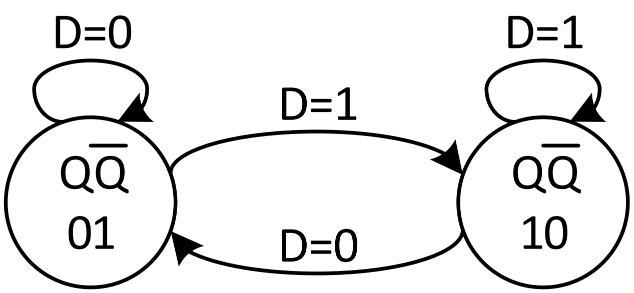


Figure 7-13 Functional behavior of a D latch for various inputs.

D Latch
(State Diagram and Characteristic Equation)

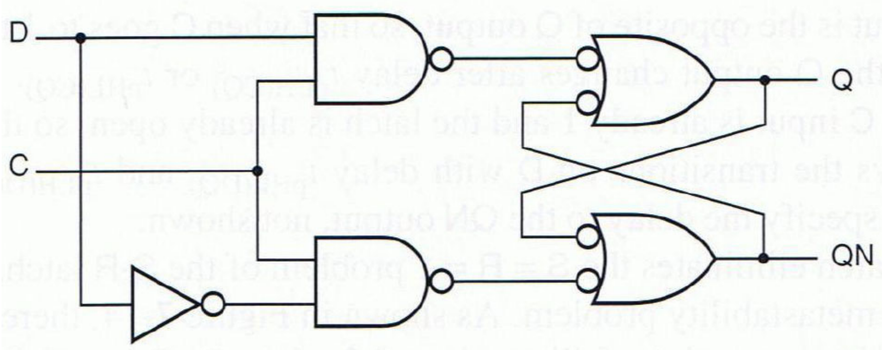




Q \ D	0	1
0	0	1
1	0	1

$Q^{+} = D$

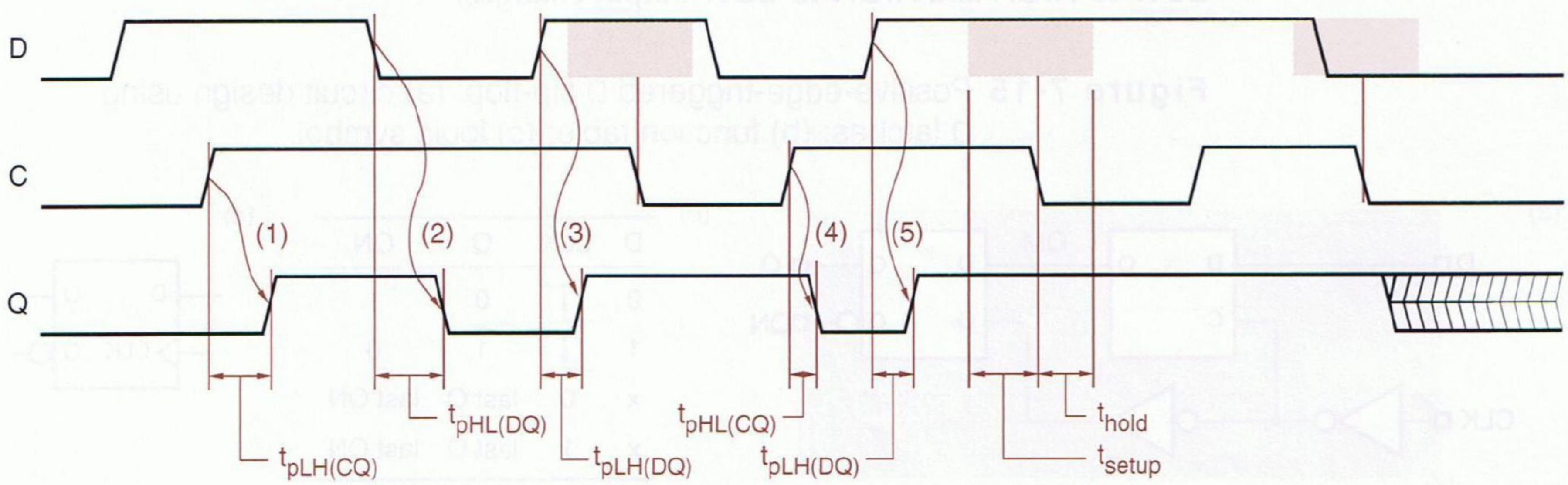
D Latch (Timing Parameters)



- t_{pLH} – propagation time LOW-to-HIGH
- t_{pHL} – propagation time HIGH-to-LOW
- t_{setup} – setup time
- t_{hold} – hold time

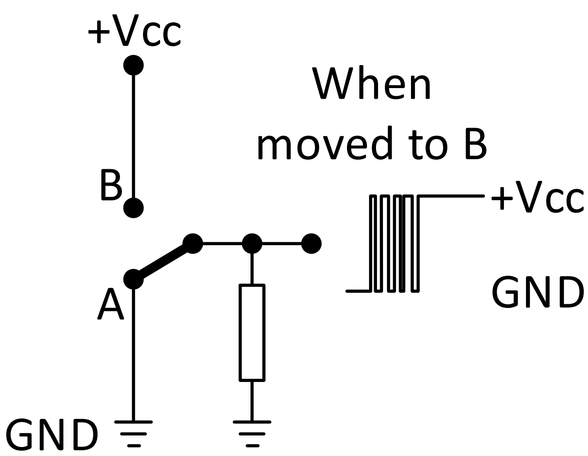
Non-determinism/metastability due to violation of t_{setup} and/or t_{hold}

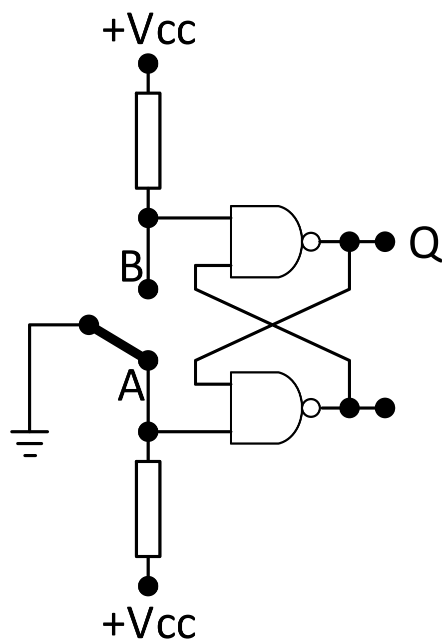
Figure 7-14 Timing parameters for a D latch.

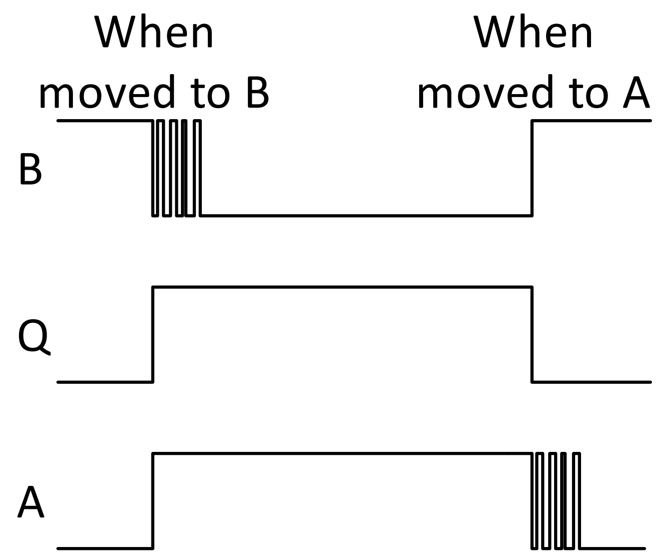


Application Example of an S-R Latch

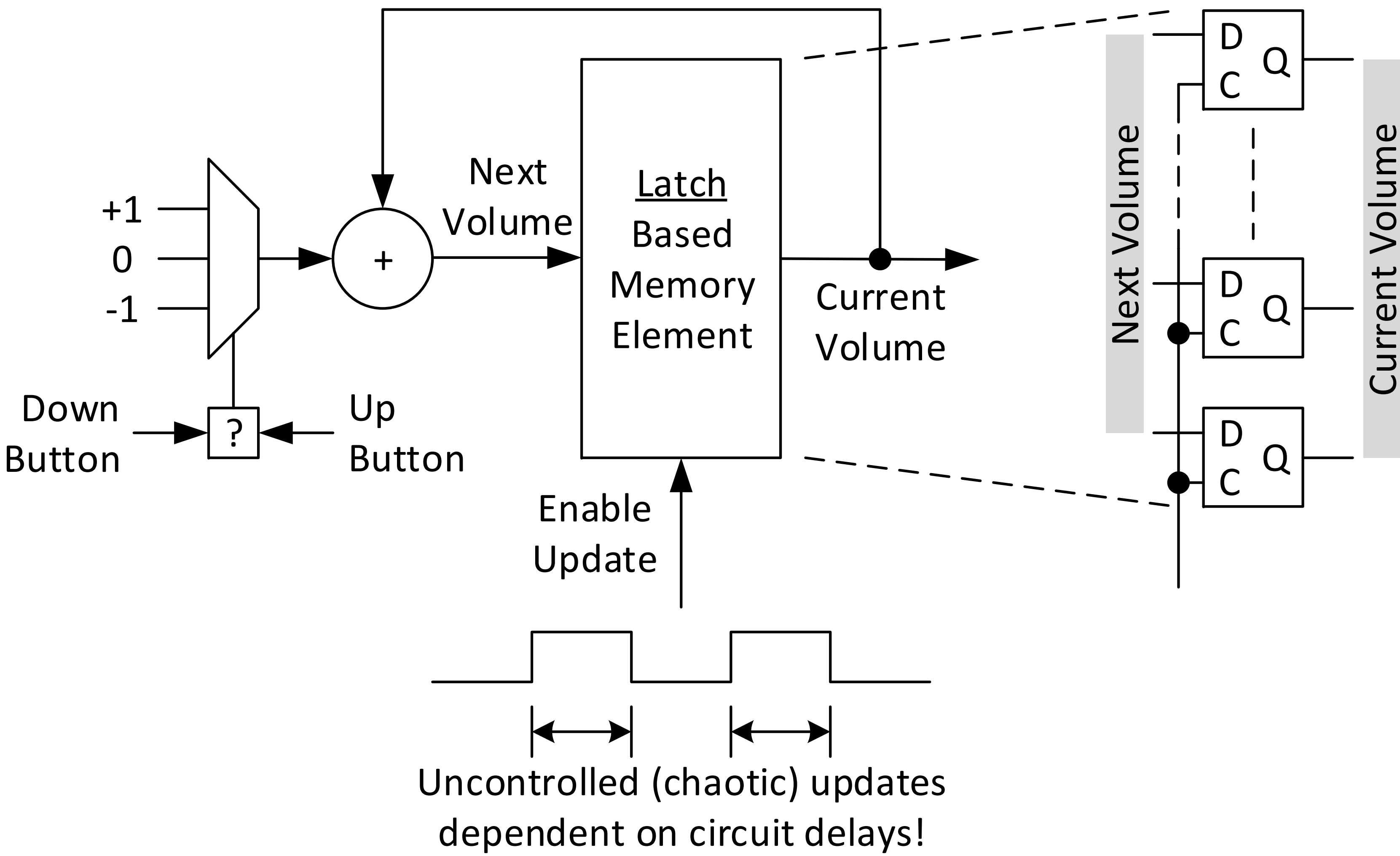
Debounce mechanical switches



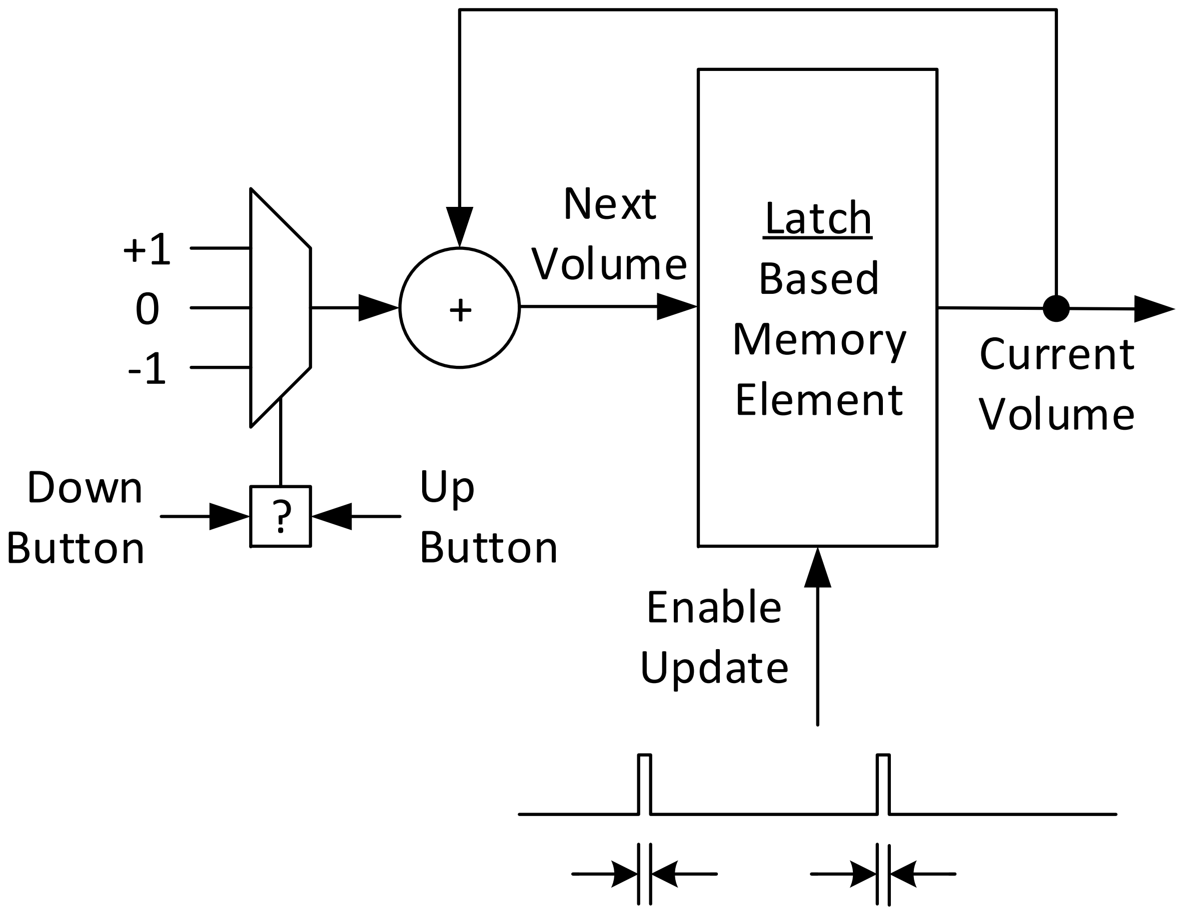




Latch Limitations/Issues

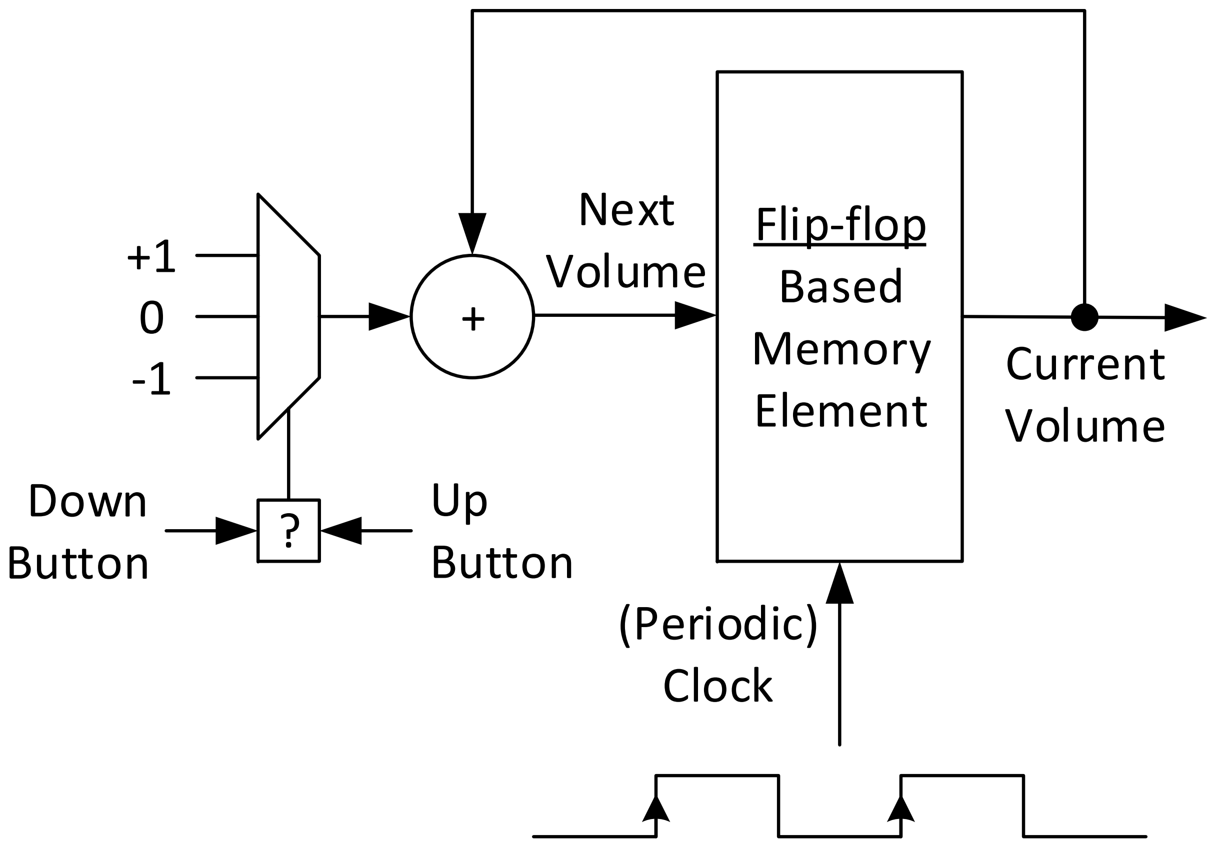


Possible Solution? Unfeasible!



Very narrow enable pulses?
Very difficult to implement!

A Feasible Solution



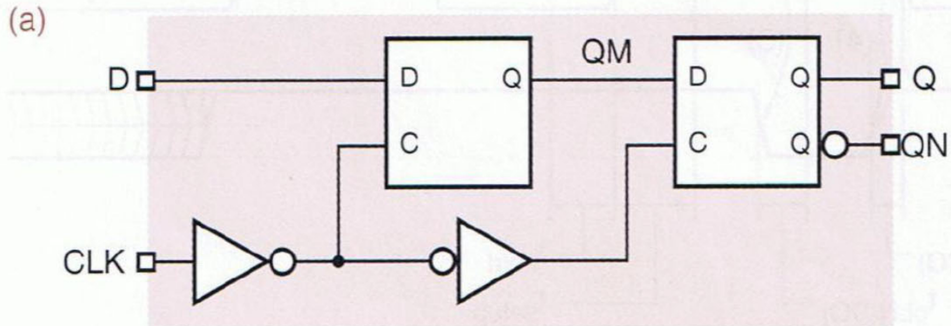
Periodic updates triggered by one of the edges (rising or falling) of a clock signal

Positive-edge-triggered D Flip-flop

- Latches are not used frequently but are a building block for flip-flops

Figure 7-15 Positive-edge-triggered D flip-flop: (a) circuit design using D latches; (b) function table; (c) logic symbol.

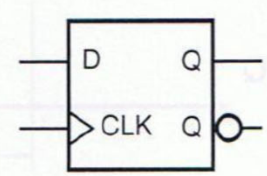
(a)



(b)

D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

(c)



Clock Signals (revisited)

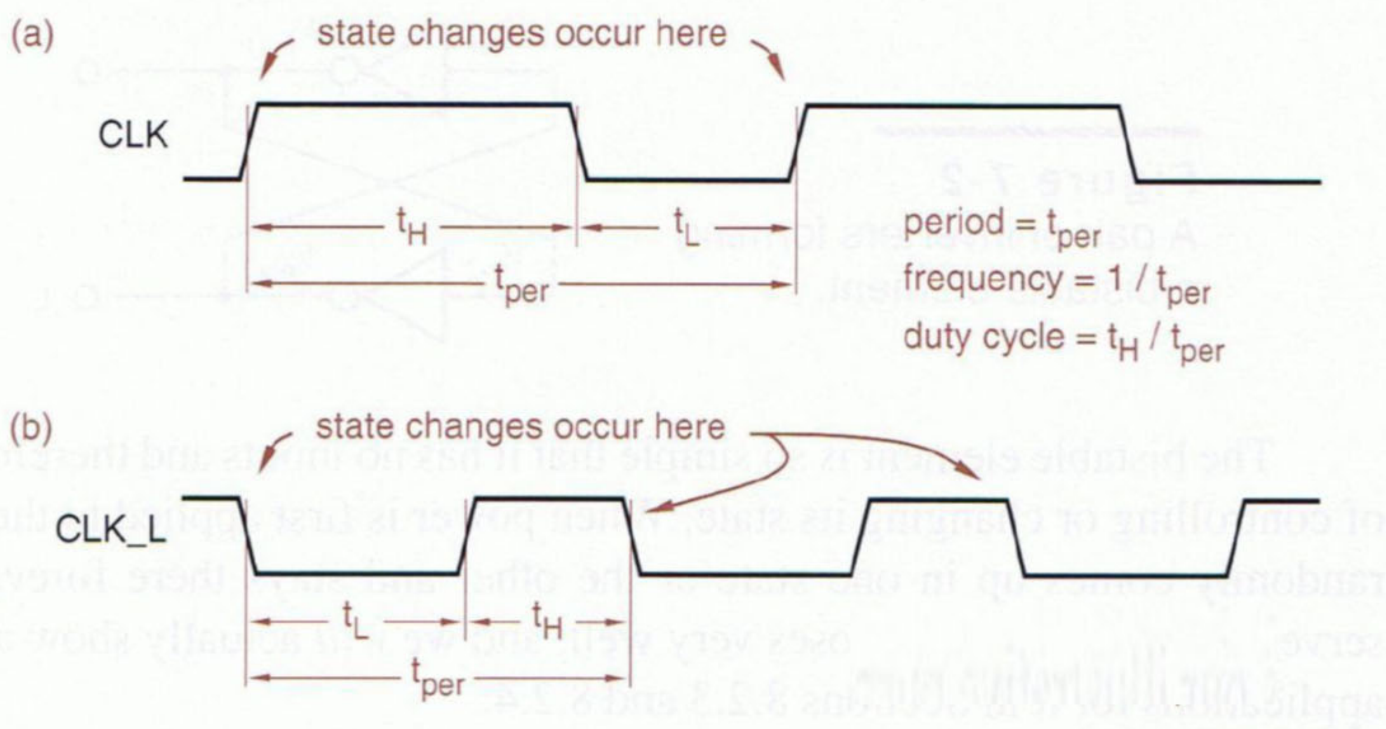


Figure 7-1
Clock signals:
(a) active high;
(b) active low.

Positive-edge-triggered D Flip-flop (Functional Behavior / Operation)

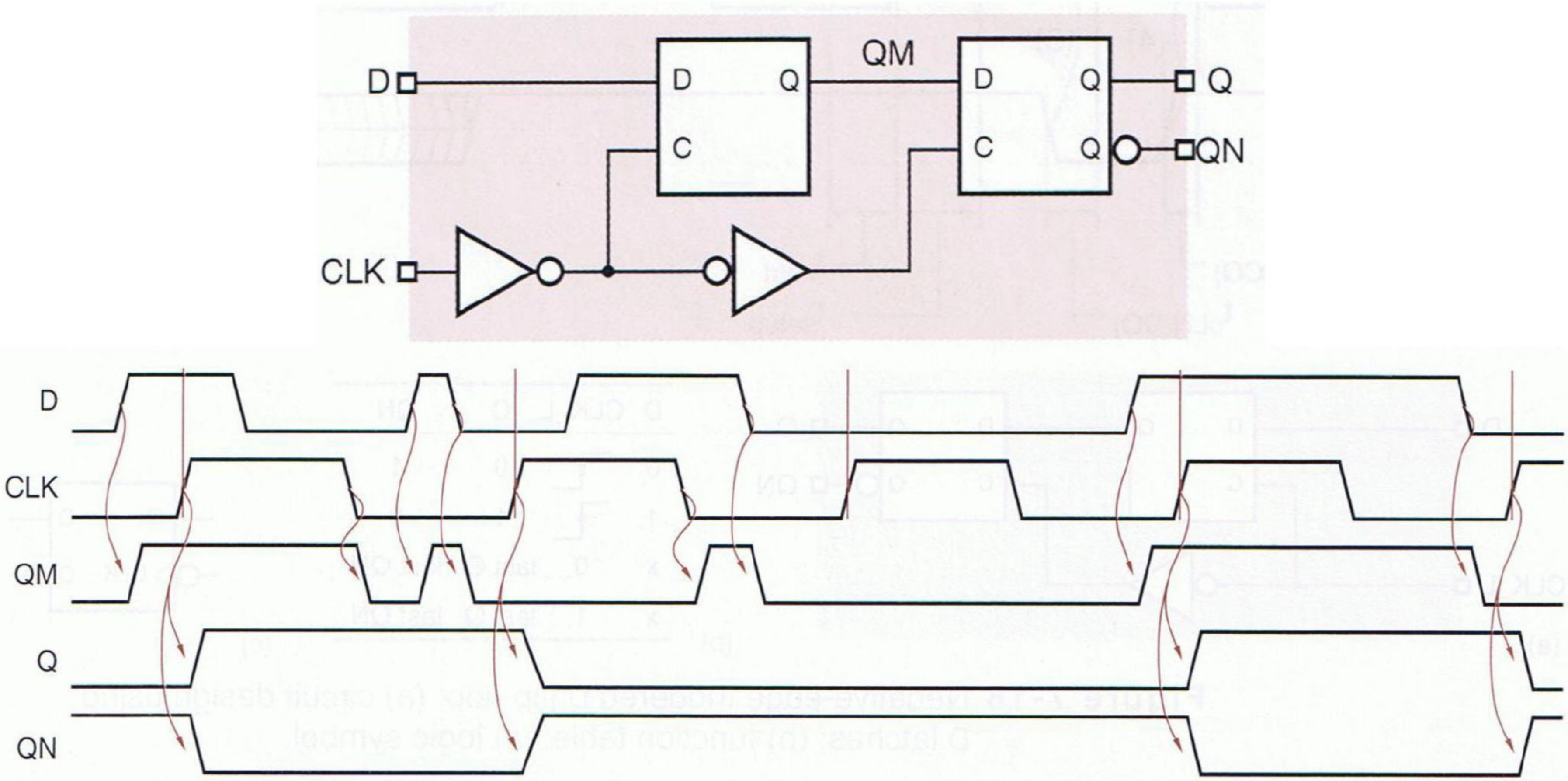
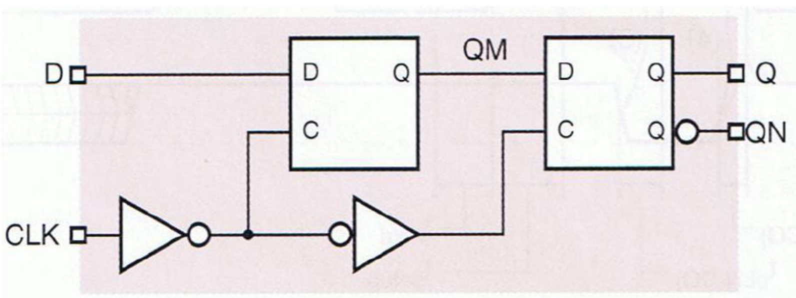


Figure 7-16 Functional behavior of a positive-edge-triggered D flip-flop.

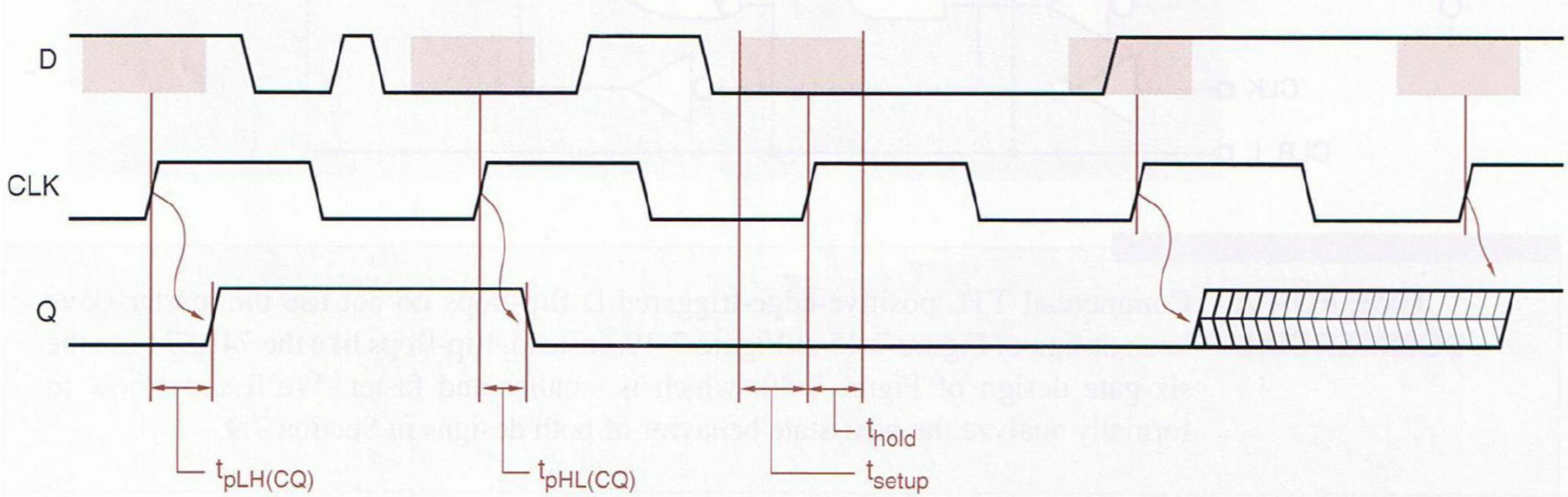
Positive-edge-triggered D Flip-flop (Timing Behavior)



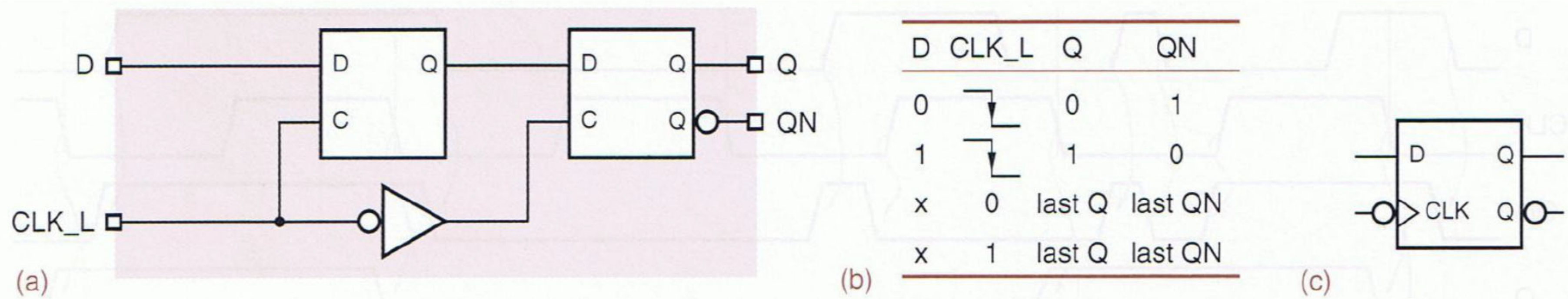
- t_{pLH} – propagation time LOW-to-HIGH
- t_{pHL} – propagation time HIGH-to-LOW
- t_{setup} – setup time
- t_{hold} – hold time

Non-determinism/metastability due to violation of t_{setup} and/or t_{hold}

Figure 7-17 Timing behavior of a positive-edge-triggered D flip-flop.



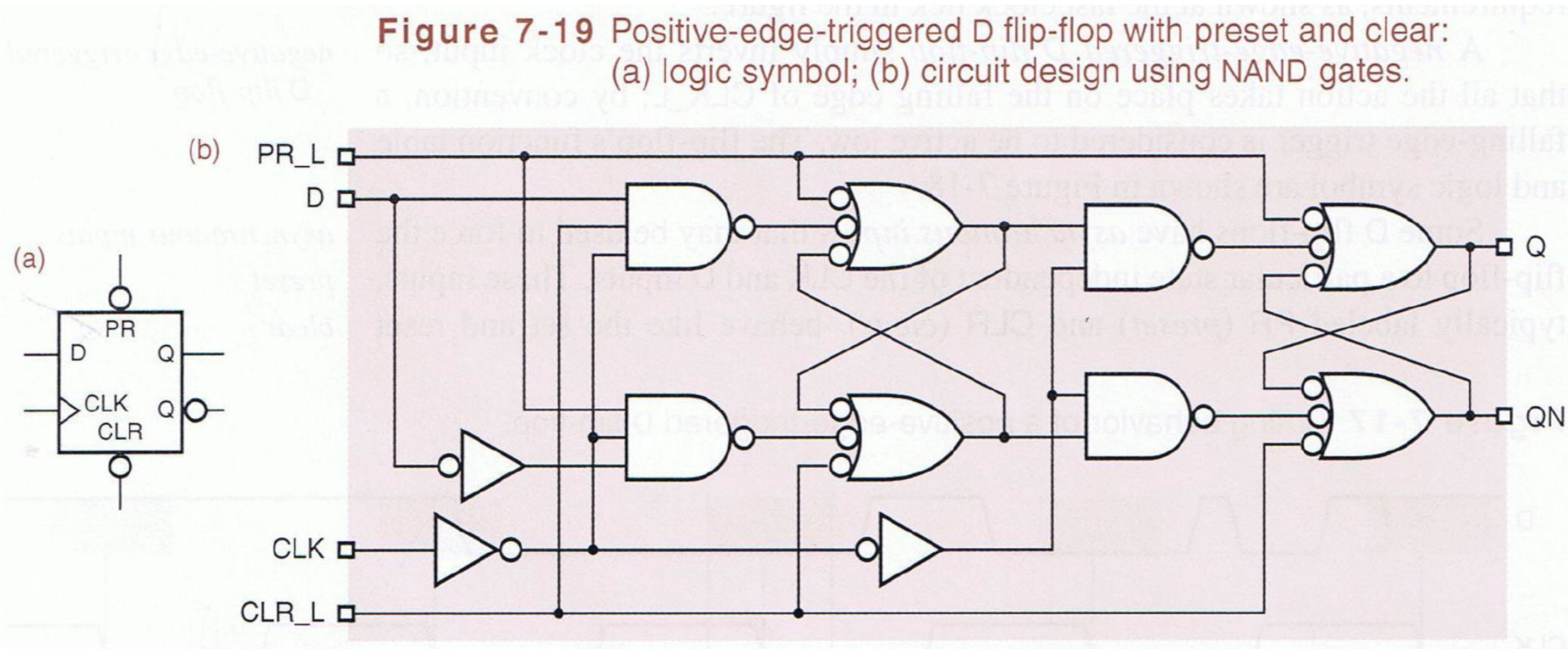
Negative-edge-triggered D Flip-flop



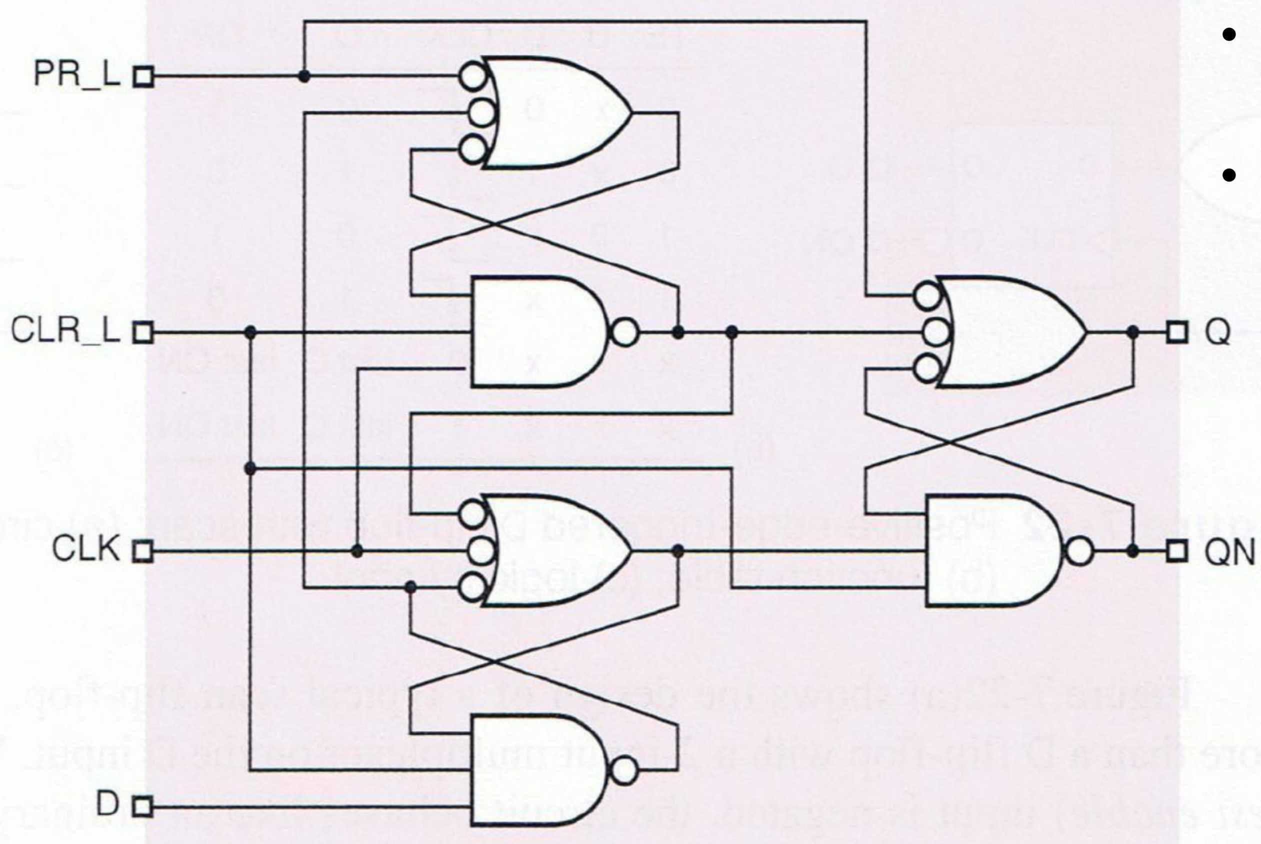
D	CLK_L	Q	QN
0	$\downarrow$	0	1
1	$\downarrow$	1	0
x	0	last Q	last QN
x	1	last Q	last QN

Figure 7-18 Negative-edge triggered D flip-flop: (a) circuit design using D latches; (b) function table; (c) logic symbol.

Positive-edge-triggered D Flip-flop with Preset and Clear



Positive-edge-triggered D Flip-flop (7474 Commercial Integrated Circuit)



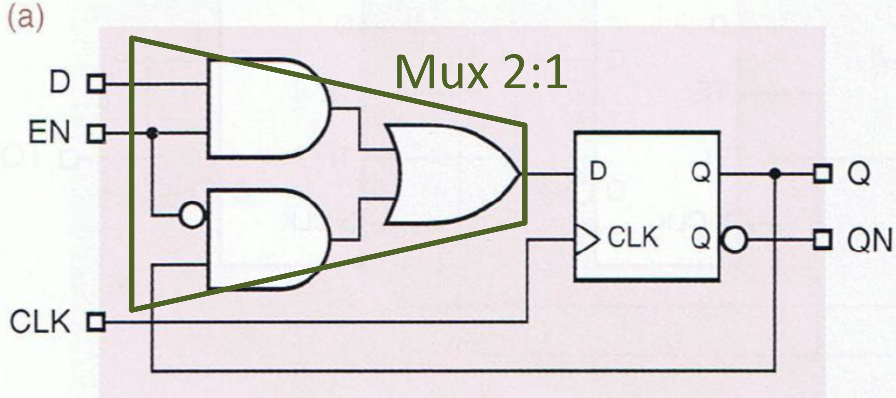
- 6 gates instead of 8 gates + inverters
- To be analyzed later…

Figure 7-20
Commercial circuit for a positive-edge-triggered D flip-flop such as 74LS74.

Positive-edge-triggered D Flip-flop with Enable

Figure 7-21 Positive-edge-triggered D flip-flop with enable: (a) circuit design; (b) function table; (c) logic symbol.

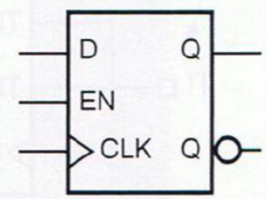
(a)



(b)

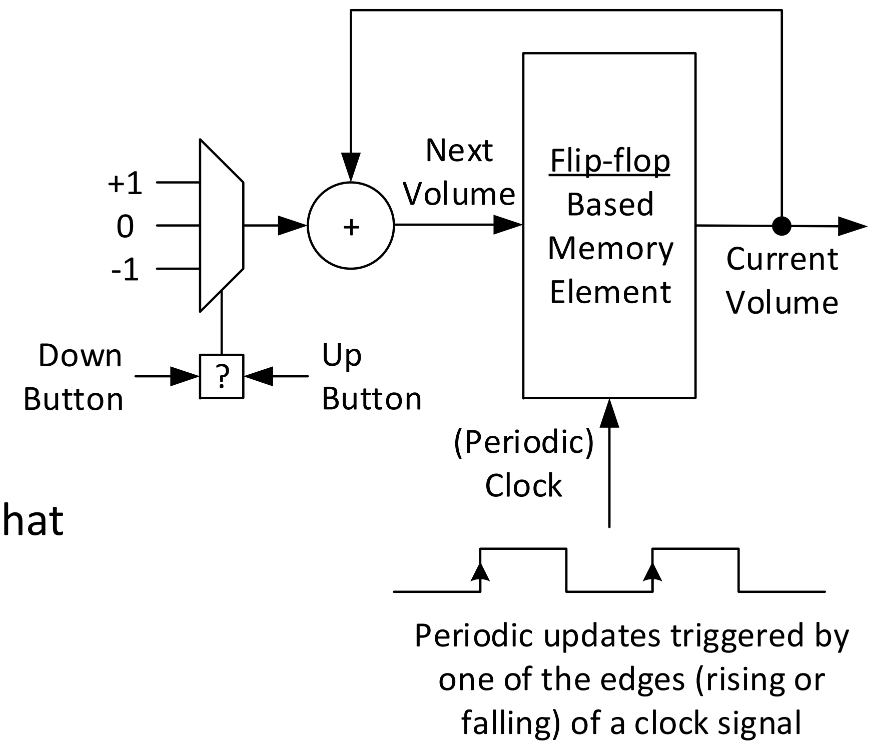
D	EN	CLK	Q	QN
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	last Q	last QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN

(c)



Exercise

- Design the complete logic diagram of the volume control system based on positive-edge-triggered D Flip-flops with enable (assume 16 levels of volume).
- Component budget
  - Flip-flops
  - Adder
  - Mux 2:1
  - Logic gates



- From the usability point of view, what could be the clock frequency?
- How to force a predefined volume level (e.g. half scale) at power up?

Conclusion

- At the end of this lecture and corresponding lab, it is fundamental to know and understand the structure, operation and timing behavior of basic sequential logic circuits (latches and flip-flops)
- Plan for the next lectures
  - Analysis of sequential circuits (Finite State Machines) and timing aspects
  - Synthesis of sequential circuits (Finite State Machines)
  - Standard sequential circuits
    - Registers and shift registers
    - Counters
  - Iterative vs. sequential circuits

Reading chapter 7 (4th ed.) or chapter 10 (5th ed.) of *John F. Wakerly, "Digital Design – Principles and Practices", Pearson – Prentice Hall*, is highly recommended.

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