EECS119 - VLSI - Project 4

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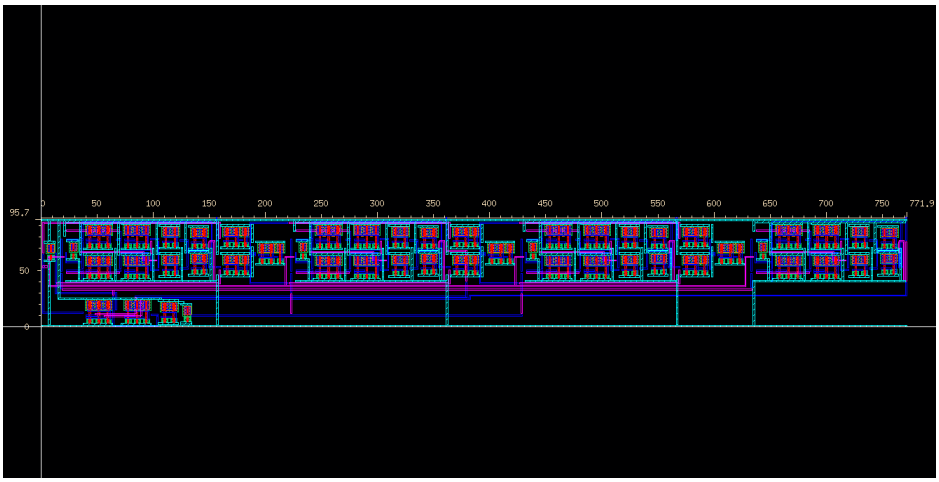

0.1 Introduction

For this project, a Binary Coded Decimal (BCD) up/down counter was constructed using a standard cell approach. An approach using JK flip flops was chosen as this was a popular counter architecture. The up/down circuit was found in [1] and was modified by using JK flip flops with a reset and additional reset logic that became asserted when the counter output was 1010 (10).

0.2 Design Parameters

Like in the previous project, the transistor parameters were: $L_n = L_p = 1.5\mu m$, $W_n = 3\mu m$, $W_p = 6\mu m$.

0.3 Logic Gates

Five gates were necessary to implement the higher level blocks: NOT, AND, OR, 2-NAND and 3-NAND. The first three gates were slightly altered since the previous project (smaller area and metal 3 used for V_{dd} and Gnd).

0.3.1 Inverter layout

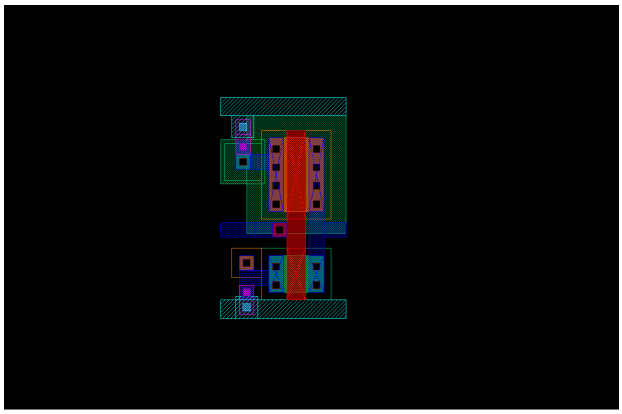

Figure 1: Inverter layout.

0.3.2 AND gate layout

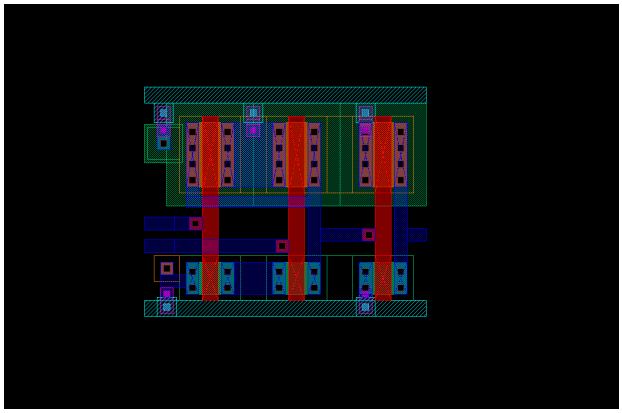

Figure 2: AND gate layout.

0.3.3 OR gate layout

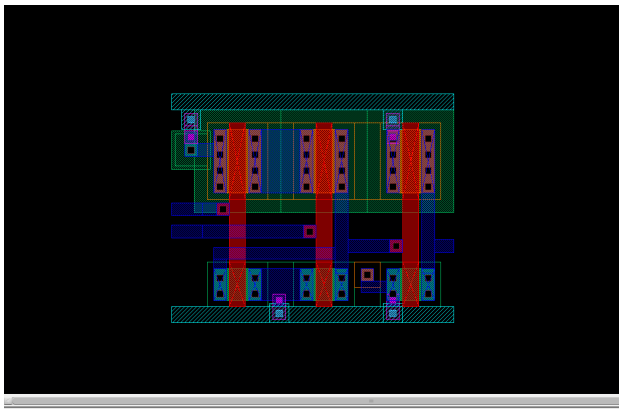

Figure 3: AND gate layout.

0.3.4 2-input NAND gate layout

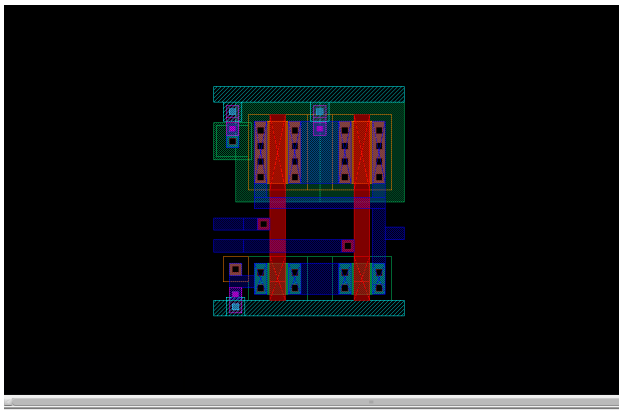

Figure 4: 2 input NAND gate layout.

0.3.5 3-input NAND gate layout

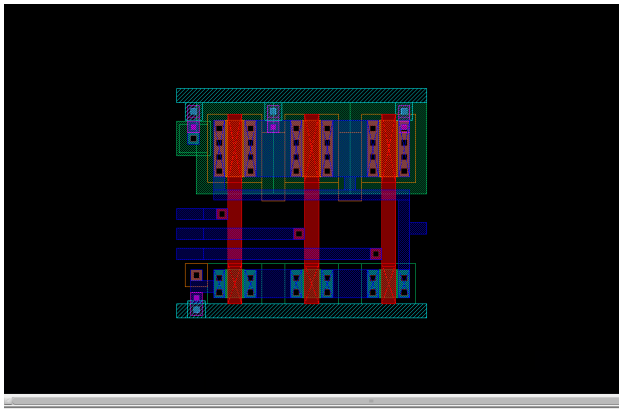

Figure 5: 3 input NAND gate layout.

0.4 JK Flip Flop

The JK flip flop design was based on schematic from [2] with four 3-input NAND gates and 4 2-input NAND gates. However the original schematic did not have set or reset inputs, which were added.

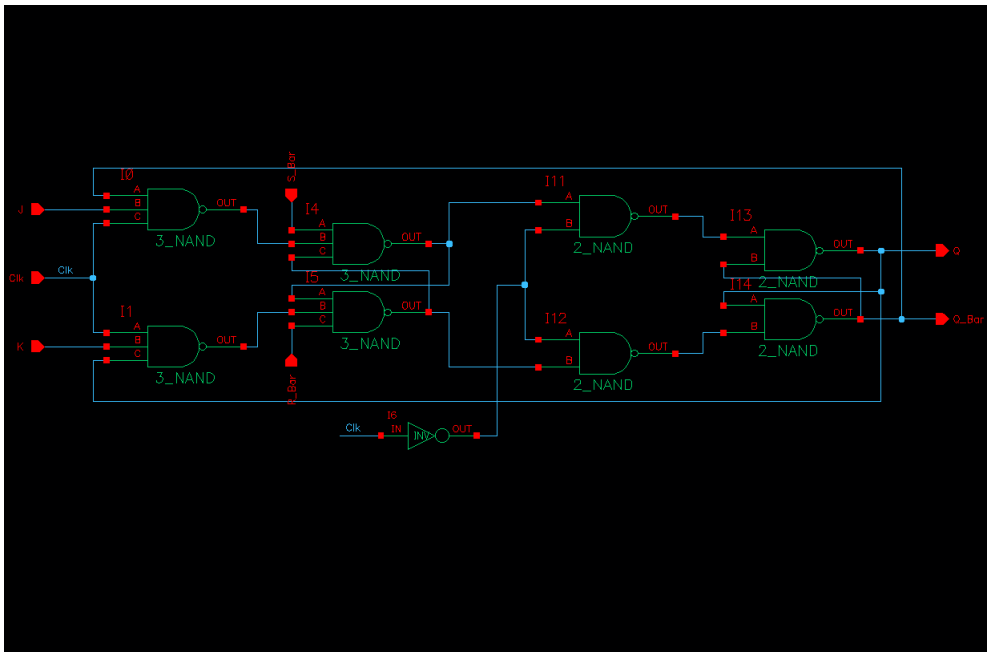

Figure 6: JK flip flop schematic.

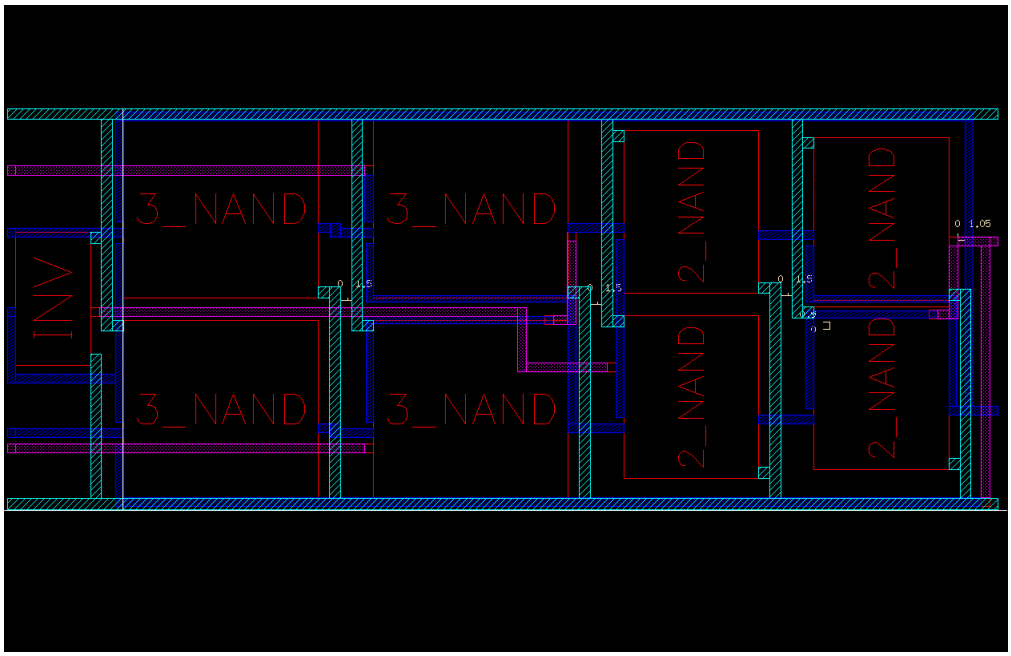

Figure 7: JK flip flop layout.

0.5 BCD Up/Down Counter

The design of the BCD counter that could increment and decrement was simplified significantly with the modified logic gate standard cells. The total area of the counter was $772\mu m$ by $96\mu m$ or $74,000\mu m^2$

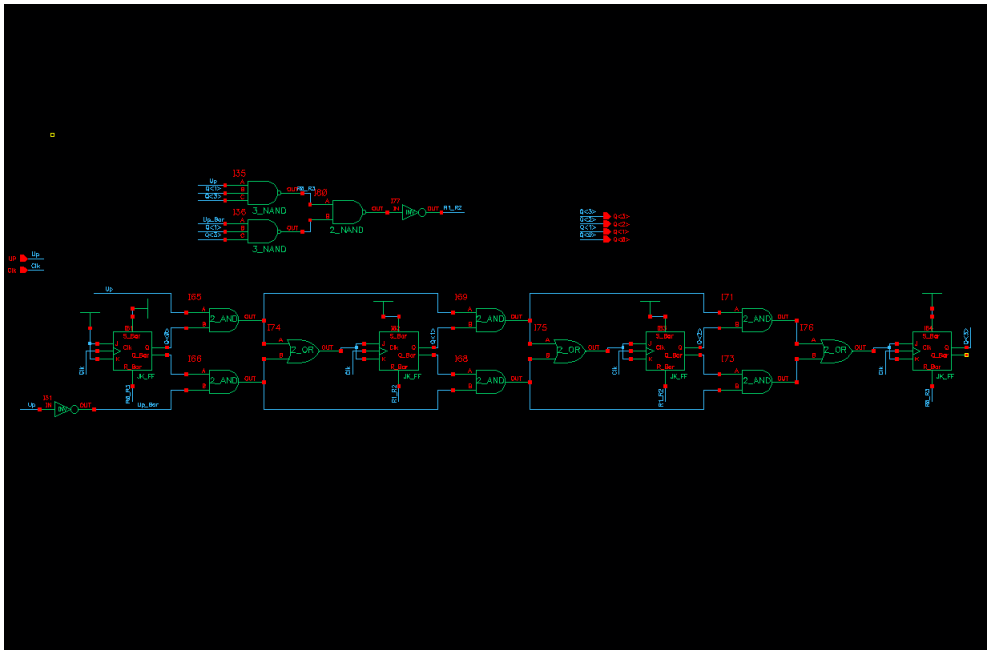

Figure 8: BCD up/down counter schematic.

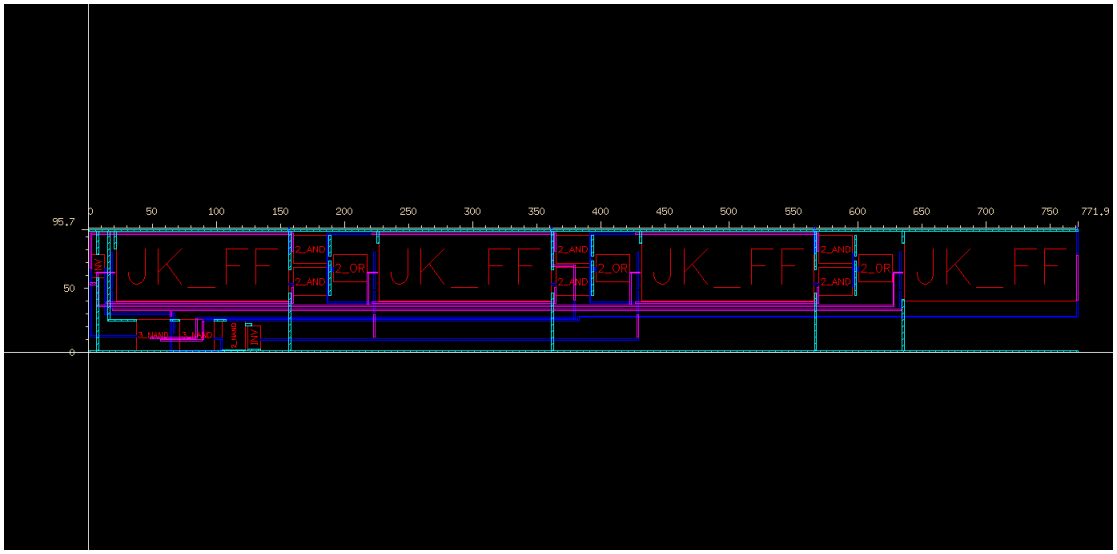

Figure 9: BCD up/down counter layout without the transistors shown.

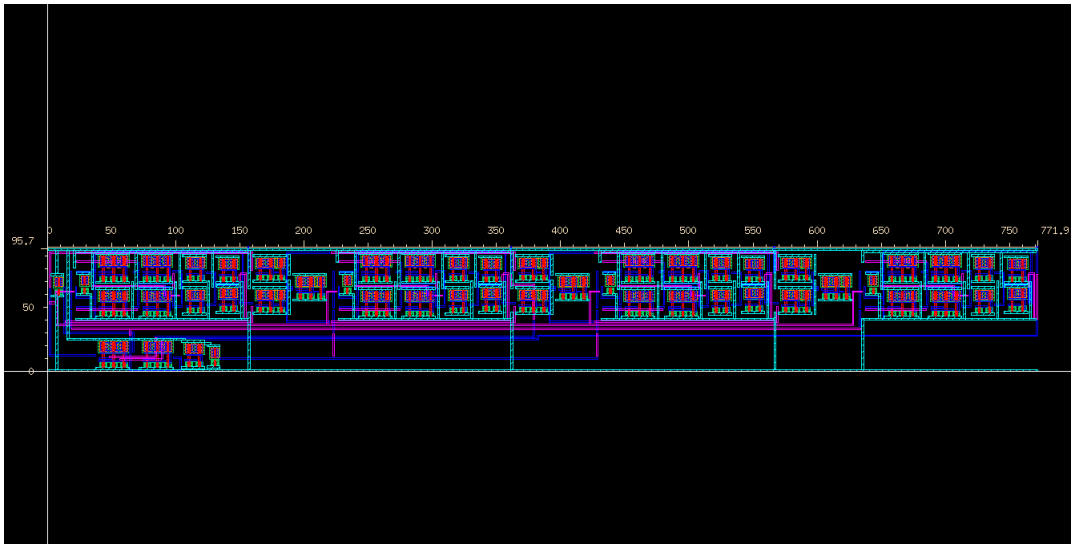

Figure 10: BCD up/down counter complete layout.

0.6 Simulation

The counter layout had successfully passed the DRC and LVS tests.

0.6.1 DRC

```
DRC started.......Thu Dec  7 10:52:24 2017
    completed ....Thu Dec  7 10:52:24 2017
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "BCD_Counter_JK layout"   *********
   Total errors found: 0
```

Figure 11: Design Rule Checker result.

0.6.2 LVS check

File Edit View Help cāden

```
@(#)$CDS: LVS version 6.1.6 09/01/2015 15:36 (sjfnl125) $

Command line: /ecelib/linware/cadence/ic616/tools.lnx86/dfII/bin/32bit/LVS -dir /users/ugrad/2017/fall/amiroshn/eecs119/LVS
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /users/ugrad/2017/fall/amiroshn/eecs119/LVS/layout/netlist
       count
         125            nets
         8              terminals
         121            pmos
         121            nmos

    Net-list summary for /users/ugrad/2017/fall/amiroshn/eecs119/LVS/schematic/netlist
       count
         125            nets
         8              terminals
         121            pmos
         121            nmos


    Terminal correspondence points
    N122      N17       Clk
    N121      N15       Q<0>
    N120      N22       Q<1>
    N119      N12       Q<2>
    N117      N23       Q<3>
    N124      N18       UP
    N118      N1        gnd!
    N123      N0        vdd!

Devices in the rules but not in the netlist:
       cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
       un-matched                 0       0
       rewired                    0       0
       size errors                0       0
       pruned                     0       0
       active                   242     242
       total                    242     242
```

Figure 12: LVS match confirmation popup.

0.6.3 Testbench schematic

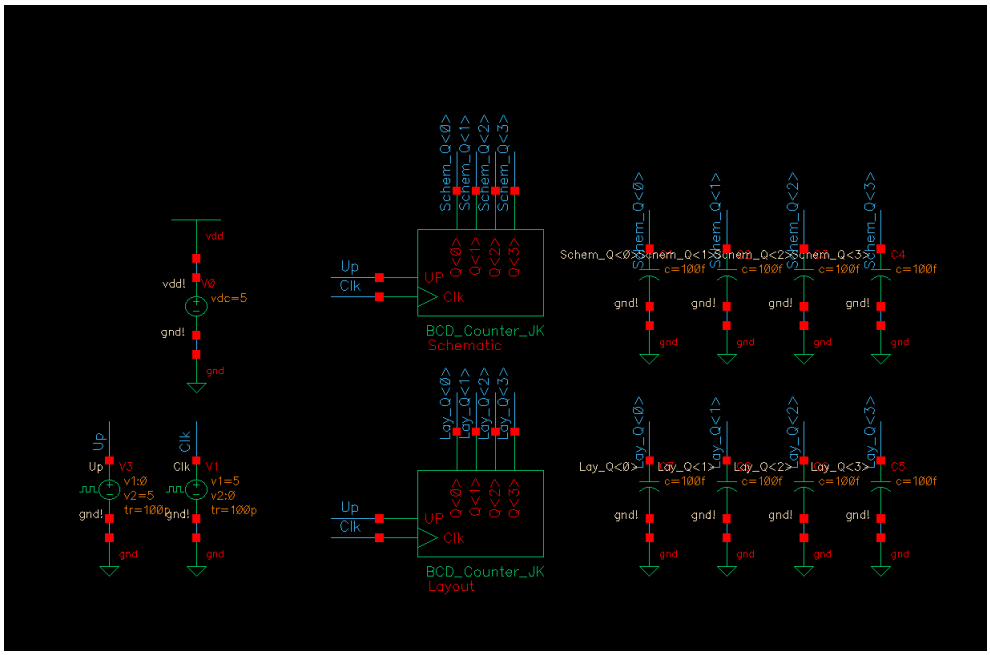

Figure 13: Testbench schematic for the BCD up/down counter.

0.6.4 Waveforms

Several cases were tested with transient analysis using ADE L.

Schematic and layout comparison

Firstly, both the schematic and layout were tested for correct functionality (counting up and down depending on the value of the "Up" input).

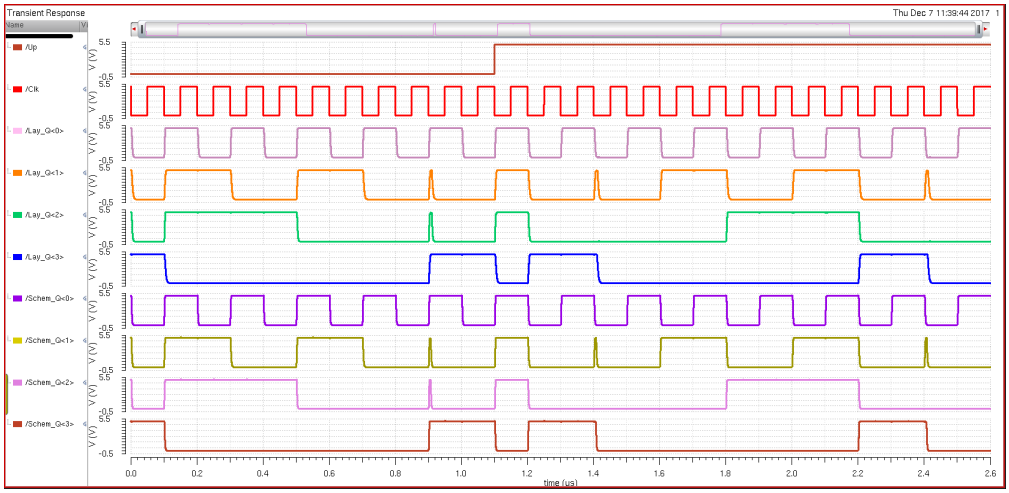

Figure 14: Schematic and layout test result waveforms

Layout with Up=1

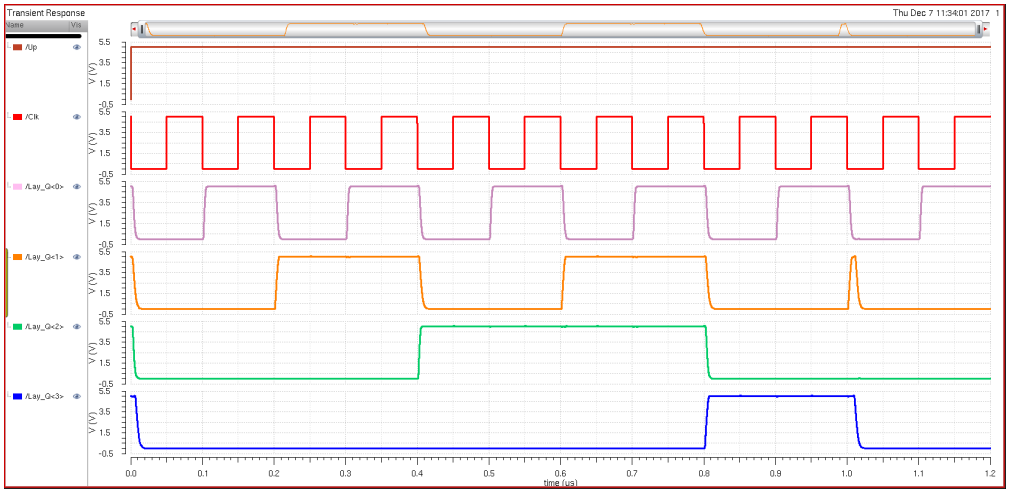

Figure 15: Layout test showing incrementing behaviour.

Layout with Up=0

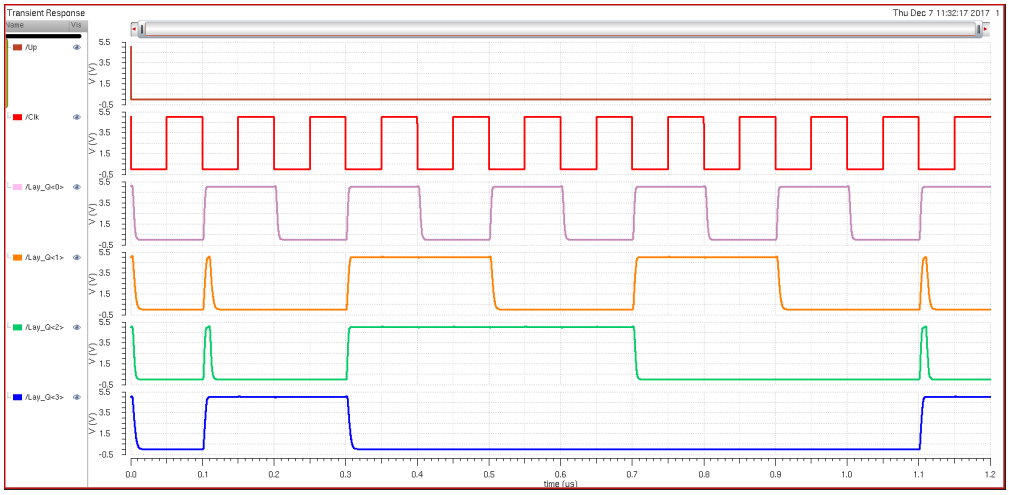

Figure 16: Layout test showing decrementing behaviour.

The counter had successfully passed the test with $Up = 1$ and $Up = 0$ (incrementing and decrementing) as well as reseting if decrementing from 0 or incrementing past 9.

Bibliography

[1] TECHNICAL ARTICLES, Synchronous Counters, https://www.allaboutcircuits.com/textbook/digital/chpt-11/synchronous-counters/

[2] ElectronicsTutorials, JK Flip Flop and the Master-Slave JK Flip Flop Tutorial, http://www.electronics-tutorials.ws/sequential/seq_2.html