

# Tutorial-5: Shift Instructions

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[ 1 ]

## ARM Shift Operations

- There are **NO** explicit shift operations in ARM.
- Instead, shift operations are incorporated in all data processing as an option.



[ 4 ]

## Shift Instructions

- What can you do with shifting:
  - Multiply by power of 2
  - Divide by power of 2
  - rearrange the bits of a word
  - access bits in a specific location of a word



[ 2 ]

## Four Classes of Shift Instructions

- Two basic shifts: left and right
- 4 flavors (classes) :
  - Logical Shift
  - Arithmetic Shift
  - Rotate
  - Rotate through carry
- The different classes are determined by what we **shift in**.



[ 5 ]

## Shift Right vs. Shift Left

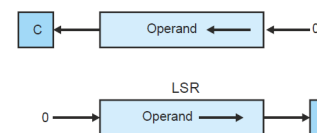
Source	After shift Left	After shift Right
00110011	0110011 <b>0</b>	<b>0</b> 0011001
11110011	1110011 <b>0</b>	<b>0</b> 1111001
10000001	0000001 <b>0</b>	<b>0</b> 1000000



[ 3 ]

## Logical Shift

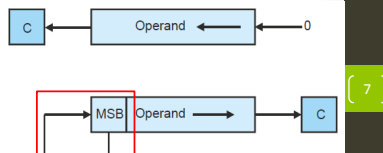
- a zero is shifted in and the bit shifted out is copied to the carry bit of the condition code register.



[ 6 ]

## Arithmetic Shift

- The sign of a two's complement number is preserved. How?
- $11001010_2 = -54$  (in two's complement)
- After Shift Right:
  - $11001010_2$  (i.e., -54)  $\rightarrow$   $11100101_2$  (i.e., -27)



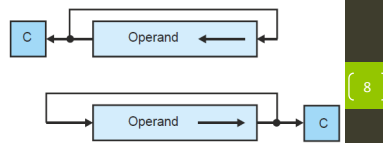
## Example-1: Logical Shift

- We have a list of unsigned numbers.
- Divide them by 4 in an **efficient way** and sum them up.
- Example:

Number		Number/4	CumSum	CumSum (hex)
12	4	3	3	0x3
8	4	2	5	0x5
4	4	1	6	0x6
16	4	4	10	0xA
12	4	3	13	0xD
Sum		13		0xD

## Rotate Shift

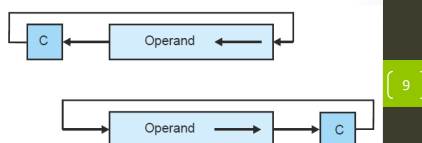
- the bit shifted out is copied into the bit vacated at the other end
- no bit is lost during a rotate



## Example-1: Logical Shift

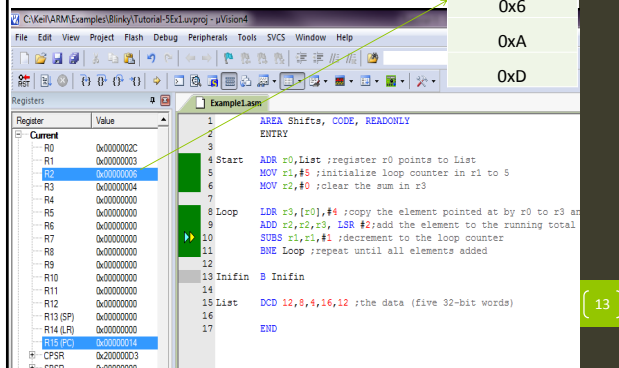
## Rotate Through Carry

- Similar to Rotate Shift
- The carry bit is treated as part of the word to be shifted



## Example-1: Logical Shift

## Example-1: Logical Shift



Registers:

Register	Value
R0	0x00000024
R1	0x00000005
R2	0x00000000
R3	0x00000004
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000014
CPSR	0x20000003
SPSR	0x00000000

Assembly Code:

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List; register r0 points to List
5 MOV r1, #5; initialize loop counter in r1 to 5
6 MOV r2, #0; clear the sum in r3
7
8 Loop LDR r3, [r0], #4; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, LSR #2; add the element to the running total
10 SUBS r1, r1, #1; decrement to the loop counter
11 BNE Loop; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, 16, 12; the data (five 32-bit words)
16
17 END

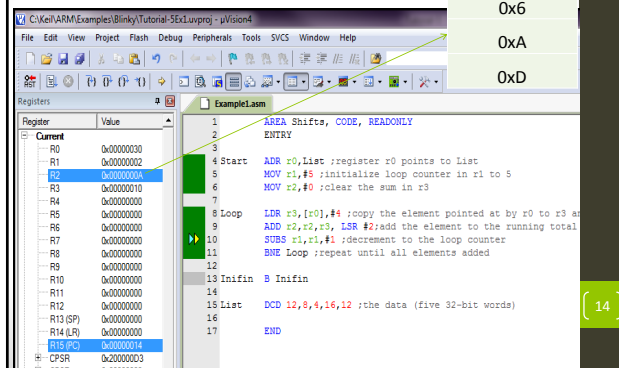
```

## Example-2: Logical Shift

- We have a list of unsigned numbers.
- Multiply them by 4 in an **efficient way** and sum them up.
- Example:

Number		NumberX4	CumSum	CumSum (hex)
12	4	48	48	0x30
8	4	32	80	0x50
4	4	16	96	0x60
16	4	64	160	0xA0
12	4	48	208	0xD0
Sum		208		0xD0

## Example-1: Logical Shift



Registers:

Register	Value
R0	0x00000024
R1	0x00000005
R2	0x00000000
R3	0x00000004
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000014
CPSR	0x20000003
SPSR	0x00000000

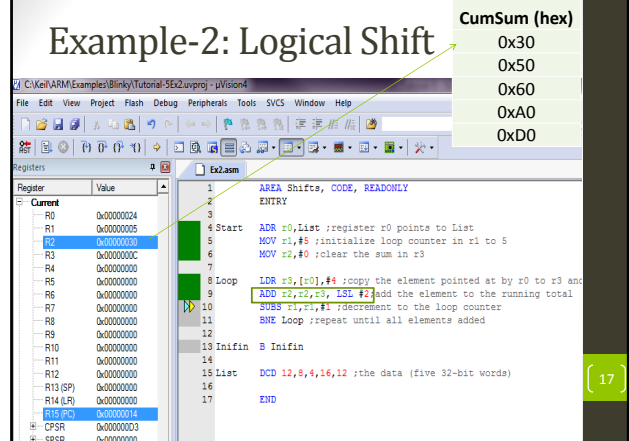
Assembly Code:

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List; register r0 points to List
5 MOV r1, #5; initialize loop counter in r1 to 5
6 MOV r2, #0; clear the sum in r3
7
8 Loop LDR r3, [r0], #4; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, LSR #2; add the element to the running total
10 SUBS r1, r1, #1; decrement to the loop counter
11 BNE Loop; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, 16, 12; the data (five 32-bit words)
16
17 END

```

## Example-2: Logical Shift



Registers:

Register	Value
R0	0x00000024
R1	0x00000005
R2	0x00000000
R3	0x00000004
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000014
CPSR	0x20000003
SPSR	0x00000000

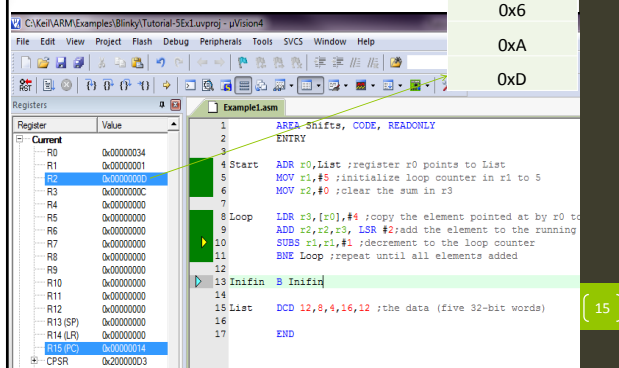
Assembly Code:

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List; register r0 points to List
5 MOV r1, #5; initialize loop counter in r1 to 5
6 MOV r2, #0; clear the sum in r3
7
8 Loop LDR r3, [r0], #4; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, LSR #2; add the element to the running total
10 SUBS r1, r1, #1; decrement to the loop counter
11 BNE Loop; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, 16, 12; the data (five 32-bit words)
16
17 END

```

## Example-1: Logical Shift



Registers:

Register	Value
R0	0x00000024
R1	0x00000005
R2	0x00000000
R3	0x00000004
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000014
CPSR	0x20000003
SPSR	0x00000000

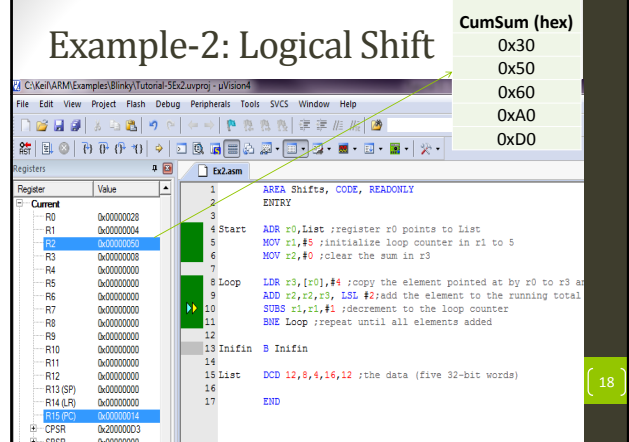
Assembly Code:

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List; register r0 points to List
5 MOV r1, #5; initialize loop counter in r1 to 5
6 MOV r2, #0; clear the sum in r3
7
8 Loop LDR r3, [r0], #4; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, LSR #2; add the element to the running total
10 SUBS r1, r1, #1; decrement to the loop counter
11 BNE Loop; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, 16, 12; the data (five 32-bit words)
16
17 END

```

## Example-2: Logical Shift



Registers:

Register	Value
R0	0x00000024
R1	0x00000005
R2	0x00000000
R3	0x00000004
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000014
CPSR	0x20000003
SPSR	0x00000000

Assembly Code:

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List; register r0 points to List
5 MOV r1, #5; initialize loop counter in r1 to 5
6 MOV r2, #0; clear the sum in r3
7
8 Loop LDR r3, [r0], #4; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, LSR #2; add the element to the running total
10 SUBS r1, r1, #1; decrement to the loop counter
11 BNE Loop; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, 16, 12; the data (five 32-bit words)
16
17 END

```

## Example-2: Logical Shift

CumSum (hex)  
0x30  
0x50  
0x60  
0xA0  
0xD0

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0,List ;register r0 points to List
5 MOV r1,#5 ;initialize loop counter in r1 to 5
6 MOV r2,#0 ;clear the sum in r3
7
8 Loop LDR r3,[r0],#4 ;copy the element pointed at by r0 to r3 and
9 ADD r2,r2,r3,LSL #2;add the element to the running total
10 SUBS r1,r1,#1 ;decrement to the loop counter
11 BNE Loop ;repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12,8,4,16,12 ;the data (five 32-bit words)
16
17 END
  
```

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## Example-3: Logical Shift

- We have a list of unsigned numbers.
- Divide them by 4 in an **efficient way** and sum them up.
- Example:

Number		Number/4	CumSum	CumSum (hex)
12	4	3	3	0x3
8	4	2	5	0x5
4	4	1	6	0x6
-16	4	-4	2	0x2
12	4	3	5	0x5
Sum	5			0x5

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## Example-2: Logical Shift

CumSum (hex)  
0x30  
0x50  
0x60  
0xA0  
0xD0

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0,List ;register r0 points to List
5 MOV r1,#5 ;initialize loop counter in r1 to 5
6 MOV r2,#0 ;clear the sum in r3
7
8 Loop LDR r3,[r0],#4 ;copy the element pointed at by r0 to r3 and
9 ADD r2,r2,r3,LSL #2;add the element to the running total
10 SUBS r1,r1,#1 ;decrement to the loop counter
11 BNE Loop ;repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12,8,4,16,12 ;the data (five 32-bit words)
16
17 END
  
```

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## Example-3: Logical Shift

0x3  
0x5  
0x6  
0x2  
0x5

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0,List ;register r0 points to List
5 MOV r1,#5 ;initialize loop counter in r1 to 5
6 MOV r2,#0 ;clear the sum in r3
7
8 Loop LDR r3,[r0],#4 ;copy the element pointed at by r0 to r3 and
9 ADD r2,r2,r3,LSL #2;add the element to the running total
10 SUBS r1,r1,#1 ;decrement to the loop counter
11 BNE Loop ;repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12,8,4,16,12 ;the data (five 32-bit words)
16
17 END
  
```

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## Example-2: Logical Shift

CumSum (hex)  
0x30  
0x50  
0x60  
0xA0  
0xD0

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0,List ;register r0 points to List
5 MOV r1,#5 ;initialize loop counter in r1 to 5
6 MOV r2,#0 ;clear the sum in r3
7
8 Loop LDR r3,[r0],#4 ;copy the element pointed at by r0 to r3 and
9 ADD r2,r2,r3,LSL #2;add the element to the running total
10 SUBS r1,r1,#1 ;decrement to the loop counter
11 BNE Loop ;repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12,8,4,16,12 ;the data (five 32-bit words)
16
17 END
  
```

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## Example-3: Logical Shift

0x3  
0x5  
0x6  
0x2  
0x5

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0,List ;register r0 points to List
5 MOV r1,#5 ;initialize loop counter in r1 to 5
6 MOV r2,#0 ;clear the sum in r3
7
8 Loop LDR r3,[r0],#4 ;copy the element pointed at by r0 to r3 and
9 ADD r2,r2,r3,LSL #2;add the element to the running total
10 SUBS r1,r1,#1 ;decrement to the loop counter
11 BNE Loop ;repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12,8,4,16,12 ;the data (five 32-bit words)
16
17 END
  
```

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## Example-3: Logical Shift

Registers:

Register	Value
R0	0x0000002C
R1	0x00000003
R2	0x00000004
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000000
CPSR	0x20000003
SPSR	0x00000000

Assembly Code (Ex3.asm):

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3
9 ADD r2, r2, r3, LSR #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END

```

Shift Amount: 0x2

## What did you do wrong?

- Should use arithmetic shift right on signed numbers



## Example-3: Logical Shift

Registers:

Register	Value
R0	0x00000030
R1	0x00000002
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000000
CPSR	0x20000003
SPSR	0x00000000

Assembly Code (Ex3.asm):

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3
9 ADD r2, r2, r3, LSR #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END

```

Shift Amount: 0x2

## Example-3: Arithmetic Shift

Registers:

Register	Value
R0	0x00000024
R1	0x00000005
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000000
CPSR	0x20000003
SPSR	0x00000000

Assembly Code (Ex3.asm):

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3
9 ADD r2, r2, r3, ASR #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END

```

Shift Amount: 0x2

## Example-3: Logical Shift

Registers:

Register	Value
R0	0x00000034
R1	0x00000001
R2	0x00000005
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000000
CPSR	0x20000003
SPSR	0x00000000

Assembly Code (Ex3.asm):

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3
9 ADD r2, r2, r3, LSR #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END

```

Shift Amount: 0x2

## Example-3: Arithmetic Shift

Registers:

Register	Value
R0	0x00000028
R1	0x00000004
R2	0x00000005
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000000
CPSR	0x20000003
SPSR	0x00000000

Assembly Code (Ex3.asm):

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3
9 ADD r2, r2, r3, ASR #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END

```

Shift Amount: 0x2

### Example-3: Arithmetic Shift

Registers: R0=0x00000000, R1=0x00000003, R2=0x00000006, R3=0x00000004, R4=0x00000000, R5=0x00000000, R6=0x00000000, R7=0x00000000, R8=0x00000000, R9=0x00000000, R10=0x00000000, R11=0x00000000, R12=0x00000000, R13(SP)=0x00000000, R14(LR)=0x00000000, CPSR=0x20000003, SPSP=0x00000000.

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, ASR #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END

```

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### Example-4: Logical Shift

- We have a list of numbers.
- Multiply them by 4 in an **efficient way** and sum them up.
- Example:

Number		NumberX4	CumSum	CumSum (hex)
12	4	48	48	0x30
8	4	32	80	0x50
4	4	16	96	0x60
-16	4	-64	32	0x20
12	4	48	80	0x50
Sum		80		0x50

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### Example-3: Arithmetic Shift

Registers: R0=0x00000030, R1=0x00000002, R2=0x00000000, R3=0xFFFFFFFF, R4=0x00000000, R5=0x00000000, R6=0x00000000, R7=0x00000000, R8=0x00000000, R9=0x00000000, R10=0x00000000, R11=0x00000000, R12=0x00000000, R13(SP)=0x00000000, R14(LR)=0x00000000, CPSR=0x20000003, SPSP=0x00000000.

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, ASR #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END

```

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### Example-4: Logical Shift

Registers: R0=0x00000024, R1=0x00000005, R2=0x00000030, R3=0x00000000, R4=0x00000000, R5=0x00000000, R6=0x00000000, R7=0x00000000, R8=0x00000000, R9=0x00000000, R10=0x00000000, R11=0x00000000, R12=0x00000000, R13(SP)=0x00000000, R14(LR)=0x00000000, CPSR=0x20000003, SPSP=0x00000000.

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, LSL #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END

```

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### Example-3: Arithmetic Shift

Registers: R0=0x00000034, R1=0x00000001, R2=0x00000000, R3=0x00000000, R4=0x00000000, R5=0x00000000, R6=0x00000000, R7=0x00000000, R8=0x00000000, R9=0x00000000, R10=0x00000000, R11=0x00000000, R12=0x00000000, R13(SP)=0x00000000, R14(LR)=0x00000000, CPSR=0x20000003, SPSP=0x00000000.

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, ASR #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END

```

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### Example-4: Logical Shift

Registers: R0=0x00000028, R1=0x00000004, R2=0x00000030, R3=0x00000000, R4=0x00000000, R5=0x00000000, R6=0x00000000, R7=0x00000000, R8=0x00000000, R9=0x00000000, R10=0x00000000, R11=0x00000000, R12=0x00000000, R13(SP)=0x00000000, R14(LR)=0x00000000, CPSR=0x20000003, SPSP=0x00000000.

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, LSL #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END

```

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## Example-4: Logical Shift

Registers:

Register	Value
R0	0x0000002C
R1	0x00000003
R2	0x00000060
R3	0x00000004
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000000
CPSR	0x20000003
SPSR	0x00000000

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, LSL #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END
  
```

Memory addresses: 0x30, 0x50, 0x60, 0x20, 0x50

## No ASL in ARM

- There's no ASL (Arithmetic Shift Left) in ARM.
- It's safe to use LSL instead (both are identical)



## Example-4: Logical Shift

Registers:

Register	Value
R0	0x0000002C
R1	0x00000002
R2	0x00000000
R3	0xFFFFFFFF
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000014
CPSR	0x20000003
SPSR	0x00000000

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, LSL #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END
  
```

Memory addresses: 0x30, 0x50, 0x60, 0x20, 0x50

## What we learned so far

- To multiply numbers, we should use:
  - LSL: Logical Shift Left
  - There's no arithmetic shift left
- To divide numbers, we should use:
  - ASR: Arithmetic Shift right
  - Logical Shift Left will give wrong results**



## Example-4: Logical Shift

Registers:

Register	Value
R0	0x00000034
R1	0x00000001
R2	0x00000000
R3	0x0000000C
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000014
CPSR	0x20000003
SPSR	0x00000000

```

1 AREA Shifts, CODE, READONLY
2 ENTRY
3
4 Start ADR r0, List ; register r0 points to List
5 MOV r1, #5 ; initialize loop counter in r1 to 5
6 MOV r2, #0 ; clear the sum in r3
7
8 Loop LDR r3, [r0], #4 ; copy the element pointed at by r0 to r3 and
9 ADD r2, r2, r3, LSL #2 ; add the element to the running total
10 SUBS r1, r1, #1 ; decrement to the loop counter
11 BNE Loop ; repeat until all elements added
12
13 Inifin B Inifin
14
15 List DCD 12, 8, 4, -16, 12 ; the data (five 32-bit words)
16
17 END
  
```

Memory addresses: 0x30, 0x50, 0x60, 0x20, 0x50

## Example-6: Rotate Shift

- Assume a person wants to send a secure number to another person.
- They agree to use rotate shift to encrypt the message



secure  
message  
delivery

## Example-6: Rotate Shift

- Assume the message sent is the number: 12
- Assume the mutually agreed key is: 5



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## Example-6: Rotate Shift-Encoder

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## Example-6: Rotate Shift-Encoder

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## Example-6: Rotate Shift-Encoder

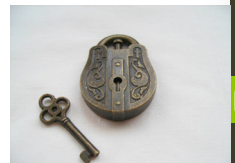
47

## Example-6: Rotate Shift-Encoder

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## Example-5: Rotate Shift

- After Encoding
- $12 \rightarrow 0x60000000 (1610612736)_{10}$



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## Example-5: Rotate Shift

- Now, we will design the decoder to decrypt the message
- We used ROR.
  - So, we should use ROL.
- Problem. No ROL, in ARM
- How can we solve this?



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## Example-5: Rotate Shift Decoder

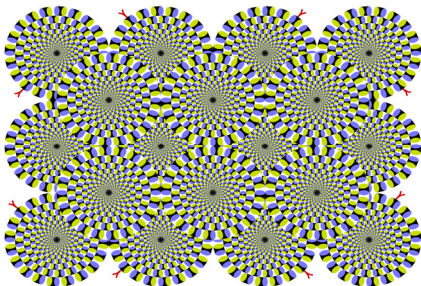
```

1 AREA Cryptography, CODE, READONLY
2 ENTRY
3
4 Endc MOV r0, #1610612736 ;register r0 points to message to be decoded
5 MOV r1, #5 ;our key
6 MOV r2, r0, ROR #27;Rotate the number (Decode it)
7
8 Inifin B Inifin
9
10 END
  
```

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## Example-5: Rotate Shift

- 1 ROL =  $32-1 = 31$  ROR
- 5 ROL =  $32-5 = 27$  ROR



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## Example-5: Rotate Shift Decoder

```

1 AREA Cryptography, CODE, READONLY
2 ENTRY
3
4 Endc MOV r0, #1610612736 ;register r0 points to message to be decoded
5 MOV r1, #5 ;our key
6 MOV r2, r0, ROR #27;Rotate the number (Decode it)
7
8 Inifin B Inifin
9
10 END
  
```

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## Example-5: Rotate Shift Decoder

```

1 AREA Cryptography, CODE, READONLY
2 ENTRY
3
4 Endc MOV r0, #1610612736 ;register r0 points to message to be decoded
5 MOV r1, #5 ;our key
6 MOV r2, r0, ROR #27;Rotate the number (Decode it)
7
8 Inifin B Inifin
9
10 END
  
```

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## Example-5: Rotate Shift Decoder

```

1 AREA Cryptography, CODE, READONLY
2 ENTRY
3
4 Endc MOV r0, #1610612736 ;register r0 points to message to be decoded
5 MOV r1, #5 ;our key
6 MOV r2, r0, ROR #27;Rotate the number (Decode it)
7
8 Inifin B Inifin
9
10 END
  
```

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## Example-5: Rotate Shift

- After Decoding:
  - $0x60000000 (1610612736)_{10} \rightarrow 0x0000000C (12)_{10}$



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## Summary

- Two basic: left and right shifts
- 4 flavors (classes) :
  - Logical Shift (Good for: unsigned): LSL and RSL
  - Arithmetic Shift (Good for: signed) :ASR, No LSR
  - Rotate (Good for: cryptography): ROR, No ROL
  - Rotate through carry (Good for: large numbers): RRX, No RLX



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