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Design Guide for High-Speed Controlled Impedance Circuit Boards

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2215 Sanders Road, Northbrook, IL 60062-6135
Tel. 847.509.9700 Fax 847.509.9798
www.ipc.org

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Developed by the IPC Controlled Impedance Task Group (D-21c) of the High Speed/High Frequency Committee (D-20) of IPC

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Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
2215 Sanders Road
Northbrook, Illinois
60062-6135
Tel 847 509.9700
Fax 847 509.9798

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Acknowledgment

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High Speed/High Frequency Committee

Chair
Thomas Bresnan
R&D Circuits

IPC Controlled Impedance Task Group

Chair
Nicholas G. Paulter
NIST

Technical Liaisons of the IPC Board of Directors

Nilesh S. Naik
Eagle Circuits Inc.

Sammy Yi
Flextronics International

IPC Controlled Impedance Task Group

Frank Y. S. Bai, Taiwan Printed Circuit Association

Amit Bhardwaj, Polar Instruments (AP) Pte. Ltd.

Robert J. Black, Northrop Grumman Corporation

Gary Brist, Intel Corporation

Ronald J. Brock, NSWC - Crane

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Byron Case, L-3 Communications

Christine R. Coapman, Delphi Delco Electronics Systems

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Zane K. Emstad, GE Electromaterials

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Margie Hillsman, GE Transportation Systems

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Thomas E. Kemp, Rockwell Collins

Robert J. Konsowitz, Flextronics

Dana Korf, Sanmina

P. Douglas Lyle, Advanced Glassfiber Yarns LLC

Bob Neves, Microtek Laboratories

Deepak K. Pai, C.I.D.+, General Dynamics-Advanced Information

John Reynolds, Rogers Corporation

Roberta Ross, Taconic Advanced Dielectric Division

Joseph Samrani, Northrop Grumman

Lowell Sherman, Defense Supply Center Columbus

Ken Taylor, Polar Instruments

G. Robert Traut, Rogers Corporation

Nicholas R. Watts, Intel Corporation

Philip R. Wellington, L-3 Communications

Steve Zimmer, Coretec Inc.

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1 SCOPE

This guide is intended to be used by circuit designers, packaging engineers, printed board fabricators, and procurement personnel so that all may have a common understanding of each other's area.

The goal in packaging is to transfer a signal from one device to one or more other devices, through a conductor. High-speed designs are defined as designs in which the interconnecting properties affect circuit performance and require unique consideration.

The term ''high-speed'' as applied to logic or digital designs needs clarification in its usage. The three most common interpretations of high-speed are as follows. (1) High-speed as a reference to the rate of change of signal amplitude with time (frequently called the edge rate of a pulse) constitutes the most important usage. The edge rate puts the greatest performance demand on interconnecting structures. (2) High-speed as a reference to the data transmission rate (bits or bytes per second) is often used to describe the ''speed'' of a system. However, high data rates can be achieved with parallel bus architectures that do not necessarily require improved performance of an interconnecting structure. (3) High-speed as a reference to the speed (distance per unit time) of a signal propagating between devices has the smallest usage and, in many cases, is not important to the application.

Controlled impedance is the maintenance of some specified tolerance in the characteristic impedance of an interconnect line (transmission line) that is used to connect different devices on a circuit. Controlled impedance is often a design consideration for high-speed digital or high-frequency analog circuits. However, the reverse is not true, that is, high-speed digital or high-frequency analog circuit designs may not need to consider controlled impedance. The purpose of this document is to help the designer understand when controlled impedance should be considered in his/her circuit design and to describe concepts important to controlled impedance design.

2 APPLICABLE DOCUMENTS

The following standards contain provisions which, through reference in this text, constitute provisions of this document. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

2.1 IPC[1]

IPC T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-356 Bare Substrate Electrical Test Data Format

IPC-TM-650 Test Methods Manual[2]

2.5.5.7 11/92 Characteristic Impedance of Lines on Printed Boards by TDR

IPC-2220 Design Standard Series

IPC-2251 Design Guidelines for the Packaging of High Speed Electronic Circuits

IPC-2252 Design and Manufacture Guide for RF/Microwave Circuit Boards

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4103 Specification for Base Materials for High Speed/High Frequency Applications

References, if presented at the end of a section, provide a more comprehensive treatment of the subject of that section.

3 ENGINEERING DESIGN OVERVIEW

Packaging of electronic equipment has traditionally been an area for mechanical considerations. However, today's packaging designs are becoming more complex because of the faster switching speeds and higher input/output densities available from today's electronic technologies. To take maximum advantage of device density and speed, designers must pay much more attention to problems of electromagnetic wave propagation phenomena associated with transmission of high-speed pulsed/switched signals within the system. New design disciplines and design strategies are needed. Controlled impedance circuit boards are a part of this strategy.

Interconnection and the packaging of electronic components primarily has been the domain of mechanical designers who were concerned with such factors as weight, volume, power, and form factor, and when interconnections

1. www.ipc.org
2. Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.htm).

were specified in to/from wire listing or net lists. Electrical signals were routed with only a few concerns, namely, that electrical continuity was maintained between points, that conductors had sufficient copper for the required current carrying capacity, and that sufficient clearance was maintained between conductors to prevent voltage breakdown in the insulator. Aside from providing a good electrical path, the electrical performance of the signal was not a major concern.

Advances in digital integrated circuits have introduced new devices that have extremely fast switching times and that are housed in high density microelectronic packages. To optimize system performance, these devices require a wiring technology that supports high density interconnection and, at the same time, provides superior electrical performance.

With recent advances in semiconductor processing technology, the output impedance of Complimentary Metal-Oxide Semiconductor (CMOS) devices are approaching that of Emitter-Coupled Logic (ECL) devices (5 Ω to 6 Ω) and can switch from one logic level to the other, a voltage swing of 5 V, in a 50 Ω environment, in as little as 1 ns. These fast level transitions demand all of the concern normally given the GaAs and ECL logic families.

3.1 Device Selection Device technology options include Transistor-Transistor Logic (TTL), Schottky TTL, CMOS, ECL and GaAs. Each technology has its own set of power requirements, operating temperature ranges, input-output (I/O) densities, input impedances, output impedances, signal threshold levels, noise sensitivities, response times and output pulse rise/fall times. Many circuit designs will have mixed technology where both Surface Mount Technology (SMT) and through-hole packaging are used to connect TTL, CMOS and ECL logic devices on a given circuit. These circuits may consist of interconnect lines with different widths (and, therefore, different characteristic impedance values), one width for each logic family on the circuit, or they may consist of a single width interconnect line that is designed to be within the performance margins of all the logic families on the circuit.

Chips can be individually mounted on a large board or assembled into small boards or multichip modules that are then mounted onto large boards. Large systems may require several large board assemblies with additional levels of interconnect between the boards. Noise, timing, and signal degradation will accompany transitions from one packaging level to the next because of mismatches in circuit impedance.

The electrical connections to the board can be of a variety of configurations ranging from pins that will insert into plated-through holes in the board, as in dual in-line packages, to a series of lands for surface mount devices. Requirements for component packaging are dependent on many factors including space, economics, electrical performance and reliability, as well as the predominant packaging style of the assembly. The components must be provided in a style that is compatible with the assembly processes used to manufacture the printed board assembly.

The component package must be considered when designing for high speed. In passive components, the primary factor that affects signal quality will be the lead length because leads provide additional inductance and capacitance that affect signal propagation and switching transients. To minimize these effects, the leads should be as short as possible. Surface mount devices can provide almost leadless packages which can be mounted directly to the interconnecting substrate.

Note: Manufacturer component data sheets often do not provide information on the parasitic values of package leads. These parameters are important to designers where high-speed signal propagation and noise are issues.

Active devices, components such as integrated circuits, are often offered in several package designs. In the past, Dual In-Line Packages (DIPs), using either plastic or ceramic substrates, have been the dominant package style. These packages typically are the largest packages and provide the poorest high speed operating environment due to their lead configuration. The next best package style for high-speed performance and high density circuitry is the surface mount package. Surface mount packages are the dominate package style in use today and are offered in a variety of package configurations/styles such as (Small Outline Integrated Circuits) SOICs, (Plastic Leaded Chip Carriers) PLCCs, Plastic Quad Flat Packages (PQFPs) or Thin Small Outline Packages (TSOPs). These packages will typically have lower lead capacitance and inductance than DIPs.

To obtain the optimum performance from the device, the die can be directly mounted to the substrate using either the Chip-on-Board (COB), Flip Chip, Chip Scale Package (CSP), Tape Automated Bonding (TAB), Ball Grid Array (BGA), Pin Grid Array (PGA) or similar approach. These mounting strategies offer an optimum approach since they minimize lead capacitance and inductance and improve package reliability and high-volume production capability. However, as with all mounting strategies, the quality and reliability of the interconnection for the application must be determined.

3.2 Interconnection

3.2.1 Connectors Interconnections may cause troubles in high speed application because of the impedance discontinuities that exist between the connector and the board and/or between the connector and the cable. At high frequencies, even changes in the geometries within a connector may cause discontinuities. If a continuous uniform

impedance environment is not provided, the propagating signal will reflect at the impedance discontinuities and this will result in degradation of signal integrity.

Many board-to-board connector systems are not designed for use in high-speed applications, and will degrade signal integrity if used in a high-speed board. Furthermore, the impedance of board-to-board connections are often not matched to the characteristic impedance of the signal conductors on the board themselves, and this causes further signal degradation. However, for high-speed circuits and systems, which typically use a 50 Ω impedance environment, high-bandwidth 50 Ω board-to-board connectors are readily available.

There are two primary approaches to reduce the impedance discontinuity caused by interconnect systems. The first approach is to provide a connector style such that the pinouts can be arranged to provide a good signal path. For nondifferential signals, the electrical reference for the active signal line is the closest reference plane connection, which is either a voltage or ground plane. Nondifferential signal conductors rely on controlled geometries and nearby reference planes for impedance control. Therefore, signal pin quality, reference pin quality and their location control the electrical performance of the connection. To optimize the electrical performance of the connection, reference pins must be added to reduce the problems associated with an insufficient number of reference pins, such as poor shielding, inadequate ground reference, and increased reactance. As a ''rule of thumb,'' a 3:1 signal pin to reference (ground or voltage) pin ratio is sufficient.

The second approach to reduce the impedance discontinuity is to modify the connector to minimize the magnitude of the discontinuity between boards. This can be achieved by shortening the pin length or by adding a reference ground plane within the connector.

Board mounted coaxial connectors are frequently used when only a few signal lines are connected to a circuit board or where signal isolation and/or signal integrity is critical.

3.2.2 Cables Discrete coaxial connectors and cables are sometimes used because they can couple high speed, high frequency signals to a circuit board with little signal degradation. A coaxial cable controls signal propagation speed, reduces crosstalk, lowers noise pick-up, and provides an excellent impedance match, particularly at higher frequencies. Discrete coaxial cables have been used with discrete wire boards for unique, high-speed applications. An optical cable can also be used with discrete wired boards for high frequency signals and for better signal isolation. Unique and specialized boards may require coaxial cables for the ultimate EMI control. Another consideration is discrete wiring boards have a lower I/O density and a higher fabrication cost than conventional boards.

3.3 Printed Board and Printed Board Assemblies Component placement is a critical factor in the design of high-speed systems. The effects of unsuitable placement can be significant and include concerns in the following areas:

a. *Crosstalk Management* Crosstalk between conductive lines and/or devices is affected by the location of one device (and its corresponding interconnects) relative to another.

b. *Impedance Control* Whether or not an interconnect needs to be considered a transmission line will depend on, for one, the length of the interconnect between devices.

c. *Power Distribution* Not all power planes are available across the entire board.

d. *Time Delays Between Circuits*

e. *Thermal Management*

3.3.1 Board Design The number of signal layers in multilayer boards will be influenced by the density of interconnections within the board as well as the effect of crosstalk or coupling between signal lines. Crosstalk control may require placing additional dielectric layers or metal planes between signal layers and/or increased spacing between conductors on a given signal layer. However, the increased spacing decreases interconnect density.

The use of diagonal routing in addition to orthogonal routing on the same wiring layers may allow greater circuit density per layer and also increase possible placement geometries. The increase in possible placement geometries may help to increase circuit density and lower crosstalk.

A close relationship exists between interconnect design and circuit performance in high-speed digital circuits. This interdependence previously was noticeable only in the very highest performance computers and was ignored in low speed signal applications. However, due to increasing logic speeds, this interdependence now imposes new design rules, restrictions and process controls on products as ordinary as personal computers.

To meet the performance requirements of high speed digital circuits, the design of today's multilayer printed board must accommodate the requirements for:

a. Propagation delay.

b. Transmission line reflectance.

c. Signal loss.

d. High density interconnections.

e. Crosstalk.

f. Controlled impedance.

To achieve the design requirements, the designer must start by controlling the characteristic impedance of the transmission lines, which, in turn, minimizes reflections from lines that are properly terminated.

Controlled impedance conductors on boards can be used for signal interconnections between devices. For a given transmission line design (microstrip, stripline, etc.), the characteristic impedance can be controlled by the dielectric thickness, conductor thickness, conductor width, and relative permittivity (dielectric constant) of the substrate. These design and material parameters also affect signal propagation. Choosing a dielectric with a lower relative permittivity, ε_r, (see 3.4.2) results in faster signal propagation, but requires increasing the conductor width to maintain a given characteristic impedance value. Solder masks and conformal coatings also affect the characteristic impedance of external (on the surface of the board) transmission lines, as well as the effective relative permittivity (see 3.4.2.2). The type, thickness, and cure process of the solder mask, as well as the conductor thickness and width, affect the characteristic impedance of the transmission line.

Signal paths should be managed such that the system timing requirements are met. If it is desired to minimize signal losses, shorter paths are typically preferred. Even if it were possible to make a circuit capable of switching with infinite speed, the interconnection material would limit the performance of the systems because of the frequency dependent characteristics of the materials in the interconnect (see 3.4.2.1).

Space constraints, the number and complexity of interconnections, power distribution, and cost of manufacture are some factors that should be considered when determining the number of layers in a circuit board. The thickness of dielectric layers, the composition and thickness of ground/voltage plane layers, the dielectric, conductor width/thickness and the overall circuit length will impact electrical performance. The width and thickness of the conductor and the number of layers have an effect on manufacturing costs. The manufacturing costs include direct material cost, cost of fabrication, reduced yield, etc. Consequently, design options may need to be considered to provide flexibility in selecting the materials, fabrication processes, etc. that reduce manufacturing cost without sacrificing performance. For example, the manufacturing cost of a printed board may be prohibitively expensive if a dielectric with unique electrical properties, ideal for the given application, (such as low ε_r or low $\tan\delta$ (see 3.4.4) for high-speed low-loss signal propagation) is used but may be within budget if another dielectric and a slight design modification are used.

3.4 Performance Requirements Electromagnetic wave propagation theory must be considered in evaluating the performance of high-speed interconnects and circuit substrates. High-speed is characterized by the fast rise time of an electrical pulse, such as those pulses used in digital circuits. As the rise time of the pulse decreases, the frequency bandwidth (see 3.4.5) of the pulse increases and the digital circuit board looks increasingly like a high speed analog circuit.

3.4.1 Power Distribution System Both AC and DC power must be distributed in a circuit. Losses will occur in this power distribution circuit and, therefore, it must be designed to minimize power loss (which may result in heating or electromagnetic interference) and/or accommodate losses so that devices receive the required power. Losses in the power distribution may be grouped into two major categories, conductive losses (AC and DC) and dielectric (AC) losses.

3.4.1.1 DC Power Distribution The DC power distribution system extends from the conductors starting at the output of the power supply and ending at the input of each device. For systems with many circuit boards and supplies, a simulation of the interaction of each component is desirable to verify and assist the design effort. The voltage drop between any two points on a copper plane is determined by multiplying the maximum load current by the plane sheet resistance. When necessary, model analysis is used to determine the voltage drop between each integrated circuit location.

3.4.1.2 AC Power Distribution High-speed switching devices require equally high-speed changes in the electrical current delivered to their power inputs. If several high-speed devices are switched simultaneously, the power distribution system is required to meet the current delivery demands for all the high-speed devices simultaneously while still maintaining its voltage. This requirement demands low inductance connections to the devices from the power supply and high supply capacitance for each voltage in the system. At very high speeds, the impedance of the power supply is too high to supply the switching currents. As a result, the switching currents must be supplied by capacitors close to the devices. For higher speed circuits, capacitors are too slow and the currents must be supplied by the capacitance associated with the power and ground planes (the interplane capacitance) of the board.

The AC power distribution system must provide a low impedance, low inductance path to current flow, especially for high-speed signals. Furthermore, the power system must provide the switching current to the devices without lowering the supply voltage below the required minimum device level. These requirements are achieved by charge stored in discrete capacitors located on the board and near devices and charge stored in the interplane capacitance.

The AC system can be divided into three elements based on their frequency bandwidth. The element with the lowest frequency bandwidth is that consisting of the bulk IC decoupling capacitors. The next element is that consisting of localized high-frequency decoupling capacitors, and the highest frequency element is the capacitance associated with the power-to-ground spacing.

Bulk decoupling capacitors have the lowest bandwidth and are recharged by the power supply. The current associated with this element is higher than the current associated with the other elements.

The next element consists of discrete capacitors connected to the leads of the devices on the board. These capacitors may be useful with signal bandwidths up to 200 MHz or so. When these local capacitors discharge their current into the device, they are quickly recharged from energy stored in slower discharging bulk capacitors, thereby making them ready for their next discharge. These localized capacitors affect the highest frequency components of the current. The reactive impedance associated with these capacitors and their connections to the device, the switching transient impedance, is the cause of ground and/or V_{CC} bounce (see 3.4.14.5).

Decoupling capacitors must provide sufficient current for the devices to operate, including the high peak currents required during device switching. When the stored energy on the board is insufficient to power all the devices on the board, capacitors are placed near the devices for localized energy storage. In this case, the capacitors, and not the power planes, provide the immediate power required by the device for operation. These capacitors are connected between the power and ground planes. Capacitors having a range of capacitance values should be used to ensure that the input impedance of the power system is low over a large frequency range. Since discrete capacitors have an inductance and a resistance associated with them, they will have a resonance at which their impedance is lowest. Therefore, to obtain a power system impedance that is low over a large frequency range requires that many different capacitance values be used. Furthermore, to minimize inductance, it is good practice to use several capacitors to obtain the required capacitance value instead of one large capacitor. Decoupling capacitors also reduce overall system noise (see 3.4.15.1).

The highest bandwidth element is provided by the ground-to-power plane capacitance. These planes also provide a low inductance path to the device, which is important for signal integrity and electromagnetic emissions issues. The spacing between the power and ground planes gives the designer another parameter to vary in the design of their circuit. For example, by reducing the spacing between the ground and power planes, the local capacitance can be increased and the impedance and inductance decreased.

3.4.2 Relative Permittivity (Dielectric Constant) The relative permittivity, ε_r, of a material is defined as the ratio of the permittivity of the material to the permittivity of free space, ε_0, which has a value of 8.854×10^{-12} F/m. The permittivity of a material is a complex value given by:

$$\varepsilon = \varepsilon' + j\varepsilon'' \qquad [3\text{-}1]$$

where $j = \sqrt{-1}$ and $\varepsilon = \varepsilon_r\varepsilon_0$. In this document we will use the real part of the permittivity to represent the permittivity.

Dielectric constant is the term in common use in industry even though the ''dielectric constant'' varies with several parameters such as material composition, frequency, substrate orientation, temperature, etc.

The relative permittivity (ε_r) of the dielectric of an interconnecting structure will affect electrical performance. The value of ε_r is used in the design of the interconnect to ensure that the interconnect meets the characteristic impedance, capacitance, and propagation time requirements of the system. 3.4.6.2 and 3.4.7 describe the effects of ε_r on characteristic impedance and signal propagation. Considerations for measuring the effective relative permittivity (see 3.4.2.1) are described in 3.4.3.

3.4.2.1 Factors Affecting Relative Permittivity Factors that influence the relative permittivity of a given material include material composition, frequency, temperature, and water absorption. In addition, if the material is a composite, that is, a reinforced laminate, the value of ε_r may vary enormously as the relative amount of the constituents varies, which also may change after curing. The effects of the type of glass reinforcement and percent resin content for FR4 materials can be observed from the curves shown in Figure 3-1.

The data shown in Figure 3-1 are representative of different types of FR4 and is only used to show trends. More accurate values of $\varepsilon_{r,FR4}$ should be obtained from the material supplier. Although Figure 3-1 shows values of $\varepsilon_{r,FR4}$ for various frequencies, material suppliers commonly provide a value of $\varepsilon_{r,FR4}$ that was measured at 1 MHz using capacitance methods.

3.4.2.1.1 Frequency Effects All materials exhibit frequency dependent dielectric properties. Substrates that are compositionally anisotropic, such as glass-fabric-reinforced epoxies (such as FR-4), will more than likely be dielectrically anisotropic (depending on the materials of the composition). This anisotropic behavior is dependent on the orientation of the electric field vector of the propagating electromagnetic signal with respect to the substrate axes.

3.4.2.2 Effective Relative Permittivity The effective relative permittivity, $\varepsilon_{r,eff}$, is the relative permittivity that is experienced by an electrical signal transmitted along a conductive path. The $\varepsilon_{r,eff}$ is dependent on the permittivities of all the materials that affect the propagation of the pulse on a transmission line and on the geometry of the transmission line. The $\varepsilon_{r,eff}$ may not be dielectrically isotropic, such as in some fiber-reinforced materials (such as FR4) and many crystalline materials. $\varepsilon_{r,eff}$ may deviate from by ε_r 10% or more.

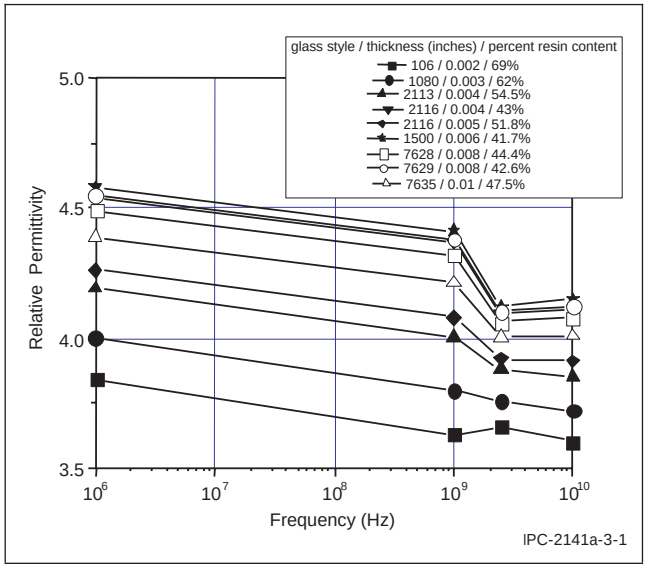

Figure 3-1 Relative permittivity of FR4 as a function of frequency for different glass reinforcement and percent resin content. The data used to generate these curves has been provided by Park/Nelco.

3.4.3 Measuring Effective Relative Permittivity As stated in 3.4.2.1, the value of ε_r is dependent on a variety of parameters, including material composition, temperature, humidity, and frequency. Consequently, the electrical measurements used to acquire ε_r and $\varepsilon_{r,eff}$ should be performed under conditions that are similar to that of the final application.

An experimental value of $\varepsilon_{r,eff}$ may be obtained using a Time Domain Reflectometry (TDR) technique (see Section 9) or by measuring the propagation delay (see 3.4.10.1) for a known length of transmission line and then calculating a value for $\varepsilon_{r,eff}$.

Material suppliers typically quote values of ε_r at 1 MHz, determined using capacitance methods performed at 1 MHz. However, calculations of Z_0 of transmission lines fabricated on FR4 substrates will more closely agree with TDR measurements if the value of ε_r used in the calculations was obtained from measurements at frequencies greater than 1 GHz. This is because TDR bandwidths are typically greater than 1 GHz.

Frequency domain methods are also used to determine $\varepsilon_{r,eff}$ In this case, the measurement frequencies should be selected such that the dielectric parameters obtained provide a precise prediction of the electrical characteristics of the finished printed board at its design frequencies. To extract ε_r from $\varepsilon_{r,eff}$, models describing the electrical behavior of the transmission line as a function of geometry and materials must be used.

If $\varepsilon_{r,eff}$ is not dielectrically isotropic, it may be necessary to measure the electrical characteristics of the material in two orthogonal directions that are parallel to the plane of the board. These directions should be chosen to maximize the differences in the observed electrical characteristics of the material.

3.4.4 Loss tangent (tanδ, or dissipation factor) The loss tangent is the ratio of the imaginary part of ε, ε'', to the real part of ε, ε':

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} \qquad [3\text{-}2]$$

The loss tangent describes the energy absorbed by the dielectric. Losses in the dielectric contribute to pulse attenuation (see 3.4.7.1) and degrade pulse rise times.

3.4.5 Bandwidth For a pulse, the bandwidth is the frequency at which the power spectrum has decreased to a given fraction of the magnitude of a reference frequency. Typically, the reference frequency is DC and the fraction is about 0.71 (or -3 dB). Since the performance characteristics of transmission lines in a printed board are often measured by time-domain reflectometry (TDR), it is necessary that the frequency bandwidth of the TDR system exceeds that of the signal propagating in the circuit. For example, the bandwidth of a TDR having a rise time of 100 ps is 3.5 GHz and should not be used to determine circuit properties for a 10 GHz application. (3.4.5.1 briefly describes frequency domain and time domain representations of a signal.) Some degradation of the rise time of the TDR pulse will occur in transmission through the test fixture and this reduces measurement bandwidth. To determine the bandwidth of the pulse, the following approximation is used:

$$BW = \frac{0.35}{t_r} \qquad [3\text{-}3]$$

where t_r is the fastest of the pulse rise or fall times and is typically calculated as the interval between the instants the pulse crosses its 10% and 90% amplitude values. Signal rise times and bandwidths are dependent on device technology (see Table 3-1).

The data provided in Table 3-1 were obtained from data sheets and manuals published in 2001 and 2002. Because this information changes often, the manufacturers should be consulted for more accurate data. Table 3-1 provides a typical range of pulse rise times, bandwidths, and critical line lengths for the indicated logic family. However, rise time will be dependent on other parameters, such as technology (for example, Schottky, low-power Schottky, etc. for the TTL family), supply voltage, and load impedance.

3.4.5.1 Frequency and Time Domain Representations Frequency domain representations of time signals are commonly used to show the frequencies contained in that signal. The frequency domain representations often provide

Table 3-1 Typical Data for Some Logic Families (critical line length is described in 3.4.9)

Logic Family	Typical Rise/ Fall Time(ns)		Band-width (MHz)	Critical Electrical Length in FR-4 at Fastest Rise/Fall Time				Output Drive Current (mA)		Logic Input Threshold (V)		Typical Buffer Prop. Delay (ns)
				Microstrip		Stripline						
	Rise	Fall		inch	cm	inch	cm	I_{OL}	I_{OH}	V_{IL}	V_{IH}	
AGP	0.350	0.450	1000	0.63	1.60	0.50	1.27	20	-12	1.12	1.52	1.5
BiCMOS 74ABT	1.6	1.4	250	2.5	6.3	2.0	4.9	64	-32	1.1	1.9	3.6
BiCMOS 74BCT	0.700	0.700	500	1.24	3.15	0.98	2.49	64	-15	0.8	2.0	2.5
BICMOS 74LVT	2.7	2.8	130	4.80	12.2	3.8	9.8	64	-32	1.3	1.7	4.1
CMOS 74AC	1.7	1.5	233	2.7	6.8	2.1	5.3	24	-24	2.2	3.0	7.5
CMOS 74ACT	1.7	1.5	233	2.7	6.8	2.1	5.3	24	-24	0.4	2.1	10.0
CMOS 74ACQ	2.4	2.4	146	4.3	10.8	3.4	8.4	24	-24	2.3	2.9	9.5
CMOS 74ACTQ	2.5	2.4	146	4.3	10.8	3.4	8.4	24	-24	1.2	2.0	7.0
CMOS 74AHCT	2.4	2.4	146	4.3	10.8	3.4	8.4	24	-15	0.8	2.0	7.0
CMOS 74C	35.0	25.0	14	44.4	112.5	35	87.5	12	-14	0.7	3.5	70.0
CMOS 74FCT	1.5	1.2	292	2.1	5.4	1.7	4.2	64	-15	0.8	2.0	3.1
CMOS 74HC	3.6	4.1	97	6.4	16.2	5.0	12.6	6	-6	2.3	2.4	25.0
CMOS 74HCT	4.6	3.9	90	6.9	17.6	5.5	13.7	6	-6	1.3	1.4	25.0
CMOS 74LCX	2.9	2.4	146	4.3	10.8	3.4	8.4	24	-24	1.3	1.8	6.5
CMOS 74LV	3.0	3.0	116	5.3	13.5	4.2	10.5	8	-8	0.9	2.3	7.5
CMOS 74LVQ	3.5	3.2	109	5.7	14.4	4.5	11.2	12	-12	1.6	1.7	9.5
CMOS 74LVX	4.8	3.7	95	6.6	16.7	5.2	13.0	4	-4	1.4	1.7	12.0
CMOS 74VHC	4.1	3.2	109	5.7	14.4	4.5	11.2	8	-8	2.1	2.8	8.5
CMOS 74VCX	2.0	2.0	175	3.6	9.0	2.8	7.0	24	-24	0.8	2.2	2.5
CTT	0.600	0.750	583	1.07	2.70	0.84	2.10	8	-8	1.3	1.7	2.0
ECL 10K	2.2	2.2	159	3.9	9.9	3.1	7.7	50	-50	-1.7	-0.95	2.0
ECL 10KH	1.7	1.7	206	3.0	7.7	2.4	6.0	50	-50	-1.7	-0.95	1.0
ECL 100K	0.600	0.600	583	1.07	2.70	0.84	2.10	50	-50	-1.5	-0.90	0.800
ECL 300K	0.500	0.500	700	0.89	2.25	0.7	1.25	50	-50	-1.7	-0.95	1.55
ECL (E)	0.375	0.375	933	0.67	1.69	0.53	1.31	50	-50	3.3	4.0	0.300
LVPECL (EP)	0.110	0.110	3182	0.20	0.50	0.15	0.39	50	-50	1.6	2.4	0.160
LVPECL (LVEL)	0.220	0.220	1591	0.39	0.99	0.31	0.77	50	-50	1.6	2.4	0.300
PECL (EL)	0.225	0.225	1556	0.40	1.01	0.32	0.79	50	-50	3.3	4.0	0.250
RSECL (SiGe)	0.030	0.030	11700	0.06	0.14	0.04	0.11					
GaAs	0.300	0.100	3500	0.18	0.45	0.14	0.35	30	-30	0.8	2.0	0.250
GTL	1.2	1.2	292	2.1	5.4	1.7	4.2	40	-40	0.75	0.85	3.0
GTL+	0.300	0.300	1167	0.53	1.35	0.42	1.05	40	-40	0.80	1.20	3.0
HSTL	0.620	0.220	1591	0.39	0.99	0.31	0.77	8~48	-8~48	0.75	0.85	1.7
LVDS	0.300	0.300	1167	0.53	1.35	0.42	1.05	3.5	-3.5	1.07	1.41	2.0
SSTL	0.330	0.510	1060	0.59	1.50	0.46	1.17	8~20	-8~20	1.30	1.70	1.8
TTL 74	8.0	5.0	70	8.9	22.5	7	17.5	16	-15	0.8	2.0	20.0
TTL 74ALS	2.3	2.3	152	4.1	10.4	3.2	8.1	24	-15	0.8	1.6	10.0
TTL 74AS	2.1	1.5	233	2.7	6.8	2.1	5.3	64	-15	0.5	1.9	6.2
TTL 74F	2.3	1.7	206	3.0	7.7	2.4	6.0	64	-15	0.9	1.8	6.5
TTL 74FR	2.1	1.5	233	2.7	6.8	2.1	5.3	64	-15	0.6	2.2	3.9
TTL 74H	7.0	7.0	50	12.4	31.5	9.8	24.5	20	-0.25	0.8	2.0	15.0
TTL 74L	35.0	30.0	12	53.3	135.0	42.0	105.0	2	-0.4	0.8	2.0	35.0
TTL 74LS	15.0	10.0	35	17.8	45.0	14.0	35.0	24	-15	0.8	1.8	18.0
TTL 74S	2.5	2.0	175	3.6	9.0	2.8	7.0	64	-15	0.8	1.8	6.0

insight into the periodicity of a signal and are easier to use than time domain representations. For example, for a sinusoidally varying signal, it is more convenient to represent the signal as a kroneker delta in the frequency domain than as a series of continuous values, the sinewave.

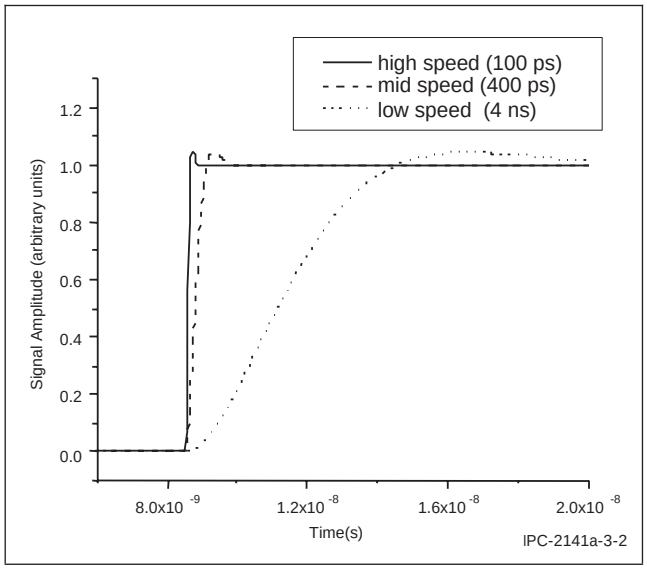

Figure 3-2 Step-like Waveforms. Transition duration values are shown in parenthesis.

A signal commonly encountered in circuits is a rectangular pulse, which may be used for clock signals and data. Figure 3-2 shows three different pulses, each with a different transition duration (or rise time). The higher the bandwidth of the pulse, the shorter is its transition duration (see 3.4.5).

To represent a time domain signal in the frequency domain (or vice versa), mathematical operators, called transforms, are used. The most commonly-used transform is the Fourier transform. The Fourier transform exploits the periodicity of a signal to generate the frequency domain representation, the spectrum, of that signal. The spectrum can be presented as either a complex number (real and imaginary parts) or as magnitude and phase. Each frequency component of the spectrum has a unique real and imaginary part (or magnitude and phase). The continuous Fourier transform of a continuous signal is given by:

$$H(f) = \int_{t=0}^{\infty} h(t)e^{-j2\pi f t}dt$$

$$= \int_{t=0}^{\infty} f(t)[\cos(2\pi f t) - j\sin(2\pi f t)]dt$$

$$= a(f) - jb(f) \qquad [3\text{-}4]$$

where *h(t)* is the signal, and *H(f)* is the Fourier transform of the signal. The magnitude and phase are derived from the real and imaginary parts. The magnitude spectrum, *M(f)*, is found from:

$$M(f) = \sqrt{a^2(f) + b^2(f)} \qquad [3\text{-}5]$$

and the phase spectrum, $\theta(f)$, from:

$$\theta(f) = \tan^{-1}\left(\frac{b(f)}{a(f)}\right) \qquad [3\text{-}6]$$

As mentioned in 3.4.5, the bandwidth is typically defined as the frequency at which the power spectrum drops to -3 db relative to the DC power. Figure 3-3 shows the power spectrum of the pulses related to those shown in Figure 3-2. (To avoid showing unnecessary spectral artifacts, like oscillatory behavior, the spectrum shown in Figure 3-3 are actually the spectra of the derivatives of the pulses shown in Figure 3-2.).

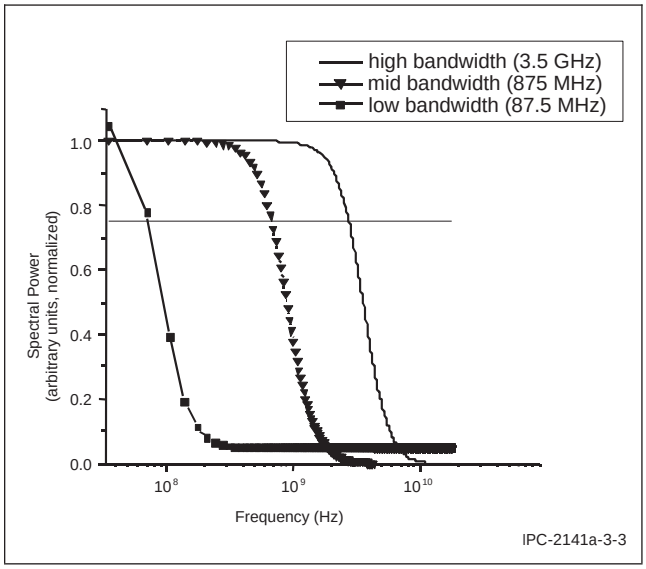

Figure 3-3 Spectra of the derivatives of the waveforms shown in Figure 3-2.

3.4.6 Capacitive Line Versus Transmission Line Environment Conductors can behave either as lumped elements (resistance, inductance or capacitance) or as distributed elements (transmission lines) depending on the length of the conductors relative to the frequencies of the signal propagating along the conductor (see 3.4.9). At low frequencies, a signal path on a circuit board may be represented electrically as a capacitance in parallel with a resistance. However, as the frequency is increased, this approach of lumped circuit modeling is no longer accurate and signal paths must be regarded as transmission lines. The analysis required to determine if the conductor behaves like a transmission line can be performed in either the frequency or the time domain. However, the critical point to remember for digital signals is that it is the pulse rise time, and not the rate at which the device is clocked, that is the key determining factor. The clock rate is limited by the rise time, thus the faster the rise time is, the faster the clock frequency may be. The critical design parameters and requirements will depend on the purpose of the line.

3.4.6.1 Capacitive Line The purpose for a capacitive line is to store charge and it is short in length. The charging time of the capacitive line and, consequently, the voltage on this line, depends on the current. The propagation time of the short capacitive line is usually less than the rise time of the digital pulse traveling on the line. Consequently, reflections from the ends of the transmission line can add to the signal, thereby degrading the pulse integrity. Specifically, because the line is so short, the reflections cause the rise time of the pulse to broaden. This broadening effect can be described equivalently as the result of a lumped element RC filter, where R is given by the load impedance and C is given by the capacitance of the transmission line and other elements connected to the line. The impedance of the lumped element line can be calculated as a resistance in series with an inductance and a shunt capacitance:

$$Z_{0,L} = \sqrt{R_L^2 + \frac{\omega^2 L^2}{(1-\omega^2 LC)^2}} \qquad [3\text{-}7]$$

where R_L,L, and C represent the lumped resistance, inductance, and capacitance for a given length of line.

3.4.6.2 Transmission Line For transmission lines, the design intent is to provide a known and common impedance environment that facilitates impedance matching to the devices populating a printed wiring board. Impedance matching is necessary to ensure the integrity of high-speed logic pulses. Discontinuities in impedance are the source of reflections that will degrade the integrity of the digital pulse and these discontinuities occur at the terminations (ends) of the transmission lines or at physical discontinuities in the transmission line. The characteristic impedance, Z_0, of a uniform continuous transmission line is given by:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \qquad [3\text{-}8]$$

where R, L, G, and C are the resistance, inductance, conductance, and capacitance of the transmission line per unit length, ω is the angular frequency, $\omega = 2\pi f$, and f is frequency. R and L are functions of the conductor properties (conductivity and permeability) and transmission line geometry. R and L are also frequency dependent because the penetration of the current into the conductors is frequency dependent: R increases with frequency and L decreases with frequency. L decreases to a limit because L is actually the sum of an internal self inductance, L_i, and an external self inductance, L_e, where L_e is fixed but L_i decreases as the penetration of the current into the conductor decreases. G and C are functions of the dielectric properties (permittivity) and the geometry of the transmission line. G and C may be a function of frequency but this dependence is a consequence of a frequency-dependent permittivity. Usually the permittivity is constant over the frequency range that the circuit operates so that C is also constant. Typically $G < \omega C$ and is ignored. Although Z_0 is a complex value (contains a real and an imaginary part), it is sometimes approximated as a real value from the following ideal approximation:

$$Z_{0,I} = \sqrt{\frac{L}{C}} \qquad [3\text{-}9]$$

A more accurate approximation to the magnitude of the characteristic impedance of the transmission line is obtained by using a second-order Taylor series expansion of Z_0 (equation [3-8]) with $G = 0$:

$$Z_0 \approx \sqrt{\frac{L}{C}}\left(1 + \frac{R^2}{8\omega^2 L^2}\right) \qquad [3\text{-}10]$$

From these last two equations for the characteristic impedance, we can see that Z_0 increases if L increases or if C decreases.

Characteristic impedance is important in high speed printed wiring boards for several reasons. First, the amount of current that is required to drive a conductor depends on Z_0 via Ohm's law, which is: $V = IZ_0$. Second, in high speed systems with impedance mismatches along the signal path, reflections will occur. Reflections not only reduce the amount of power reaching the receiver, but may also cause ringing (noise) along the circuit. These forms of signal degradation can cause systems to malfunction due to missing data pulses (from attenuation drop out) or spurious data pulses (from reflection noise).

The resistivity of the conductor, typically copper, does not contribute significantly to the high speed circuit impedance because the conductivity of most practical conductors is high and the operating frequencies are high (therefore, $R << \omega L$).

For controlled impedance conductor interconnections, the electrical and dielectric properties of the board materials have increased importance and greater care must be taken with the design and termination of the circuit.

3.4.7 Propagation in a Transmission Line The propagation of an electromagnetic wave in a uniform continuous transmission line is described by its propagation function, $\Gamma(\omega)$, which is given by:

$$\Gamma(\omega) = e^{-\gamma(\omega)L} \qquad [3\text{-}11]$$

where ω is the angular frequency, L is the propagation distance, and $\gamma(\omega)$ is the propagation coefficient give by:

$$\gamma(\omega) = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha(\omega) + j\beta(\omega) \qquad [3\text{-}12]$$

where $\alpha(\omega)$ and $\beta(\omega)$ are the attenuation (or loss) and phase functions of the transmission line.

3.4.7.1 Attenuation Attenuation is a critical parameter for preserving the integrity of a signal propagating in the transmission line and for the performance of high-speed circuits. High-speed electronic systems generate and require fast transition (risetime, falltime) electrical pulses. These systems may respond unpredictably to pulses having transitions slower than a critical duration or amplitudes less than a critical voltage. Because attenuation in the transmission line is a frequency dependent phenomenon, attenuation may cause the pulse transition to increase to a value greater than some critical value thereby causing the circuit to malfunction. Attenuation will also cause the pulse amplitude to decrease.

Losses in a transmission line are given by:

$$\alpha = \alpha_c + \alpha_d + \alpha_r \qquad [3\text{-}13]$$

Where α_c, α_d, and α_r are the conductor, dielectric, and radiative losses. Signal attenuation and distortion in a uniform continuous transmission line are caused by resistive losses in the conductors and dissipative losses in the dielectric. The effects of signal attenuation and distortion can best be understood if the pulse is described as consisting of many frequency components, a spectrum (see 3.4.5.1). The faster the pulse transition, the higher the frequency content of the pulse's spectrum. For the low frequency spectral components of the signal, the resistive losses are described by the DC resistance of the conductor. The DC losses affect pulse amplitude. For the high frequency components, the resistive losses are dependent on the penetration of the current into the conductors, which is a function of the metal conductivity and the frequency; these losses are called skin-effect losses. Skin effect losses increase with increasing frequency. The skin effect loss is also increased by rough conductor surfaces; the rough-surfaced conductors effectively have a longer electrical path length than a smooth-surfaced conductor.

The dissipative losses of the signal in the dielectric increase with increasing frequency for a constant loss tangent. Consequently, the higher frequency components of the signal will experience greater dielectric losses and thus cause the transition duration of the pulse to increase.

For an example of loss in a transmission line, consider a stripline structure. The dielectric contribution, α_d, to the attenuation is not affected by signal line width. The attenuation, in dB/m, due to dielectric losses is given by (2, Equation 7):

$$\alpha_d = 8.68589\pi\frac{f}{c}\sqrt{\varepsilon_r}\tan\delta \qquad [3\text{-}14]$$

where c is the speed of light. From this equation, it can be seen that the dielectric loss increases with increasing frequency and increasing loss tangent. The conductor losses are dependent on the penetration of the electrical current into the conductors. The attenuation in the conductors, α_c, is complicated for planar structures (see IPC-2252), but it is proportional to the surface resistivity. For smooth conductors the surface resistivity in ohms/square is given by:

$$R_s = \sqrt{\frac{\pi f\mu}{\sigma}} \qquad [3\text{-}15]$$

Corrections to this equation for surface roughness should be made (see IPC-2252), especially for high frequencies where the surface roughness approaches the skin depth. The skin depth is the depth into a conductor for which e^{-1} of the current associated with a propagating electromagnetic signal is flowing (see IPC-2252). The skin depth becomes less as frequency increases and so resistive loss also increases. The skin depth, δ, is given by:

$$\delta = \frac{1}{\sqrt{\pi f\mu\sigma}} \qquad [3\text{-}16]$$

where μ is the magnetic permeability of the conductor and σ is the electrical conductivity of the conductor. Since α_c is proportional to R_S, α_c will increase with increasing frequency, decreasing conductivity, and/or increasing permeability.

3.4.7.2 Dispersion Dispersion occurs when the propagation speed (see 3.4.7.3) changes with frequency. The propagation speed is affected by frequency through a frequency dependence in the relative permittivity of the dielectrics of the transmission line. Dispersion will cause the transition of the pulse to broaden and this broadening may cause the circuit to malfunction.

3.4.7.3 Propagation Speed Propagation speed is the speed at which an electromagnetic wave propagates in a given medium. For a transmission line, the propagation speed is affected by the effective permittivity (see 3.4.2.2). From Maxwell's equations, it can be shown that the propagation speed, v, for a signal in a transmission line is:

$$v = \frac{c}{\sqrt{\varepsilon'_{r,eff}}} \qquad [3\text{-}17]$$

where c is the speed of light in a vacuum ($3\text{x}10^8$ m/s) and $\varepsilon'_{r,eff}$ is the real part of the effective relative permittivity. The propagation speed of a pulse in a transmission line is affected by the frequency-dependent phase and attenuation characteristics of the transmission line. The attenuation (see 3.4.7.1) is caused by conductor, dielectric, and radiative losses in the transmission line. The phase response is affected by the permittivities of the dielectrics.

The propagation speed is important, for example, in determining the delays in a transmission line and differences in

these delays, the skew (see 3.4.14.1). 4.2 lists equations for several transmission line configurations from which the propagation speed of the transmission line can be calculated.

Signal (pulse or sinusoidal) propagation speed is also affected by the surface roughness of the conductors. Surface roughness of the conductor increases the effective path length that a signal must propagate and, thereby, increases the signal propagation time for a given length of conductor (1).

Pulse propagation speeds in transmission lines may appear different for different device technologies. However, this apparent difference in propagation speed is a consequence of several factors. For one, the device technologies are limiting the bandwidth (see Table 3-1) and, thus, the propagating frequencies of the pulse. Secondly, a given transmission line structure (such as microstrip or strip line), will exhibit frequency dependent attenuation (see 3.4.7.1) and dispersion (see 3.4.7.2), both of which will cause the pulse transition to increase. Lastly, propagation speed is typically defined from the propagation delay (see 3.4.10.1) which may be affected by broadening of the pulse transition caused by attenuation and dispersion.

3.4.8 Critical Signal Speed The critical signal speed is related to the signal rise time, not the clock frequency. The bandwidth of a digital system is determined by the leading edge of the pulse (which has the shortest transition time). This edge must be permitted to rise (or fall) as quickly as possible. High speed signals have bandwidths in the 100 MHz to 1 GHz range, corresponding to rise/fall times ranging between 3.5 ns to 350 ps (see 3.4.5). The general rule is that transmission line effects (wave effects) become an important design consideration when the length of the interconnection (including conductors and plated-through holes) approaches some fraction of the wavelength (see 3.4.9) of the -3 dB frequency of the signal's power spectrum. The wavelength at a given frequency can be obtained using:

$$\lambda = \frac{v}{f} \qquad [3\text{-}18]$$

where λ is wavelength. Successful controlled impedance design requires the use of materials where ε_r is relatively constant over the 100 MHz to 1 GHz frequency range. Table 3-1 shows the rise times for some families of the ICs. For example, ECL has a 0.45 ns rise time and this rise time corresponds to a 3 dB frequency bandwidth of 777 MHz.

3.4.9 Critical Line Length The critical length is the length above which a conductor exhibits the characteristics of a transmission line, that is, when propagation effects of the conductor should be considered. The critical length, a parameter widely cited within the printed board wiring community, is determined from the rise time of the pulse and the propagation speed of the pulse in the transmission line. The critical length can be determined in different ways. For example, using the effective permittivity of the transmission line, the pulse propagation speed in the transmission line can be estimated (see 3.4.7.3). From this speed, the electrical length of the transmission line is calculated from the product of the pulse rise time, t_r, and the pulse propagation speed, v, where v is defined in 3.4.7.3 and t_r is described in 3.4.5. The critical length is then defined as being a multiple of electrical lengths ($t_r v$). Typically the critical length is between $2t_r v$ and $10t_r v$, where $10t_r v$ is a conservative value.

For a general ''rule of thumb,'' if the line length is less than $3t_r v$, then the line should be treated as a lumped (or discrete) circuit element. Similarly, for a general ''rule of thumb,'' if the line length is greater than $3t_r v$, then the line should be treated as a distributed circuit element (or transmission line).

An alternative, but less commonly used definition of critical line length is based on the wavelength of the 3 dB frequency, λ_{3dB}, which is the frequency at which the power spectrum of the pulse has dropped -3 dB relative to its DC power. The critical line length, in this case, is equal to $0.5\lambda_{3dB}$. Any circuit conductor greater than or equal to $0.5\lambda_{3d}B$ is considered a transmission line.

For conductors longer than the critical length, reflections from a mismatched load impedance may be received back at the source after the pulse has reached its maximum value; this may lead to false triggering of a device. For conductors shorter than the critical length, reflected pulses are received back at the source before the pulse has reached its maximum value. Therefore, any modification of the pulse shape will only be to the leading edge, which is less likely to produce false device triggering.

3.4.10 Propagation Time Propagation time is the time it takes a signal to travel from node to another node along a given interconnect. Propagation time is in units of seconds. For a system to perform correctly at high speeds, controlled propagation time between nodes may be required. Adjustments in the propagation time of the line may be achieved by controlling the length of the line from source to load. As shown in sec. 3.4.7.3, the real part of the effective relative permittivity affects the propagation speed. Because propagation delay (see 3.4.10.1) is the reciprocal of propagation speed, the effective permittivity affects propagation time and delay. In some situations, ε'_r will be dependent on the orientation of the electric field of the propagating pulse with respect to the material axes (such as FR4). To calculate the propagation speed for a specific conductor, the equation in 3.4.7.3 must be used where ε'_r is replaced by

$\varepsilon'_{r,eff}$, where $\varepsilon'_{r,eff}$ is the effective relative permittivity, which was described in 3.4.2.2.

The measurement of propagation time in a transmission line may be affected by frequency-dependent attenuation (see 3.4.7.1), dispersion (see 3.4.7.2), and pulse amplitude attenuation. Dispersion and frequency-dependent attenuation typically will cause the rise time of the pulse to increase with propagation distance in a transmission line and this in turn will cause an observed increase in propagation time. Pulse amplitude attenuation will affect propagation time calculations if a fixed amplitude is used as a reference level. For example, if the input pulse has an amplitude of 2 V, the reference level is chosen to be 1 V, and after propagation in the transmission line the pulse amplitude is reduced to 1.5 V, an erroneous increase in propagation time may be computed.

3.4.10.1 Propagation Delay Propagation delay is the time it takes a pulse to travel a given length of transmission line (that is, propagation delay is the propagation time per unit length), typically given in units of ps/cm. Because the propagation time is directly proportional to the square root of $\varepsilon'_{r,eff}$, so is the propagation delay.

3.4.11 Signal Loading Effects When a conductor is connected to several loads (devices), signal loading must be considered. When connected in serial fashion and where the impedance of the load is low or a near match to the characteristic impedance of the line, there will be a decrease in signal amplitude as each load is reached. High impedance loads relative to the line impedance will result in a smaller decrease in amplitude. An impedance-matched load at the end signal line may be necessary to prevent a reflection that could send an aberrant pulse (resulting in a false triggering) on the line

Radial or star connections to loads may result in complex reflections from the open ends of each line that add to each other. This method of connecting should be avoided in high speed design.

3.4.12 Crosstalk Crosstalk is the transfer (coupling) of energy between conductors by mutual inductance and/or capacitance. In crosstalk, the energy from an active line becomes superimposed on a passive line (also called a quiet line, victim line, or a receptor conductor), leading to spurious switching and circuit dropouts. Crosstalk is a result of the electromagnetic fields of the signal propagating on the active line extending outward to and enveloping the quiet line. The magnitude of coupling to the passive line is dependent on the length over which the fields envelop the passive line and the magnitude of those fields.

The terms ''near end'' and ''far end'' are used to indicate the direction of signal propagation on a line. The near end refers to the signal originating end, and the far end refers to the signal receiving end. The coupled signals that travel toward the far end of the line constitute forward crosstalk, and the coupled signals that travel back to the near end constitute backward crosstalk. The crosstalk coupling coefficients found in references differentiate between the forward and backward coefficients.

The coupling to the passive line by capacitive effects causes a low level replica of the active signal to be sent to both the far and near ends of the passive line, with the same polarity as the active signal. The coupling due to the inductive effects also sends signals to both the near and the far ends of the passive line, but the signal observed at the far end is inverted (reversed polarity) relative to that of the active signal. The signals from the both inductive and capacitive crosstalk sum at the far and near ends of the passive line. Consequently, backward crosstalk is the sum of the inductive and capacitive coupling, whereas forward crosstalk is the difference between the two signals. Forward crosstalk is usually smaller than backward crosstalk. Backward crosstalk reaches a maximum in short parallel runs and is of major concern in circuit design.

The magnitude of the coupled signal decreases with shorter parallel line segments, wider line separations, thinner dielectrics, and longer pulse rise times. Conductors that are parallel for long lengths either on the same signal plane or on adjacent signal planes are susceptible to induced crosstalk. A passive line can also run parallel for short distances to several other lines. If a certain combination and timing of pulses occurs, this combination can induce a signal on the passive line that is equal in amplitude to the active signal. Thus, there are design requirements that state that the crosstalk between lines be kept below some specified level.

Typically, crosstalk is a concern when high-speed devices are used because of their fast rise time. Mixing logic families may also cause problems because of the mixture of various voltage swings, noise margins, and logic levels. An example would be mixing Schottky TTL and ECL logic families. The concern here is coupling from the TTL signals to the ECL conductors. Since TTL switches 3 volts and the ECL family has only a 100 mV DC noise margin, significant undesired coupling can occur to an ECL device in a TTL circuit.

3.4.13 Termination of Nets Termination of nets may be necessary to satisfy signal integrity, timing, and voltage requirements of drivers and receivers and impedance matching. Terminations prevent reflections of the propagating pulse by either providing an impedance match for the transmission line at the device I/O port or by absorbing the energy reflected from the device I/O port. Common termination types are detailed in the following paragraphs and are shown in Figure 3-4.

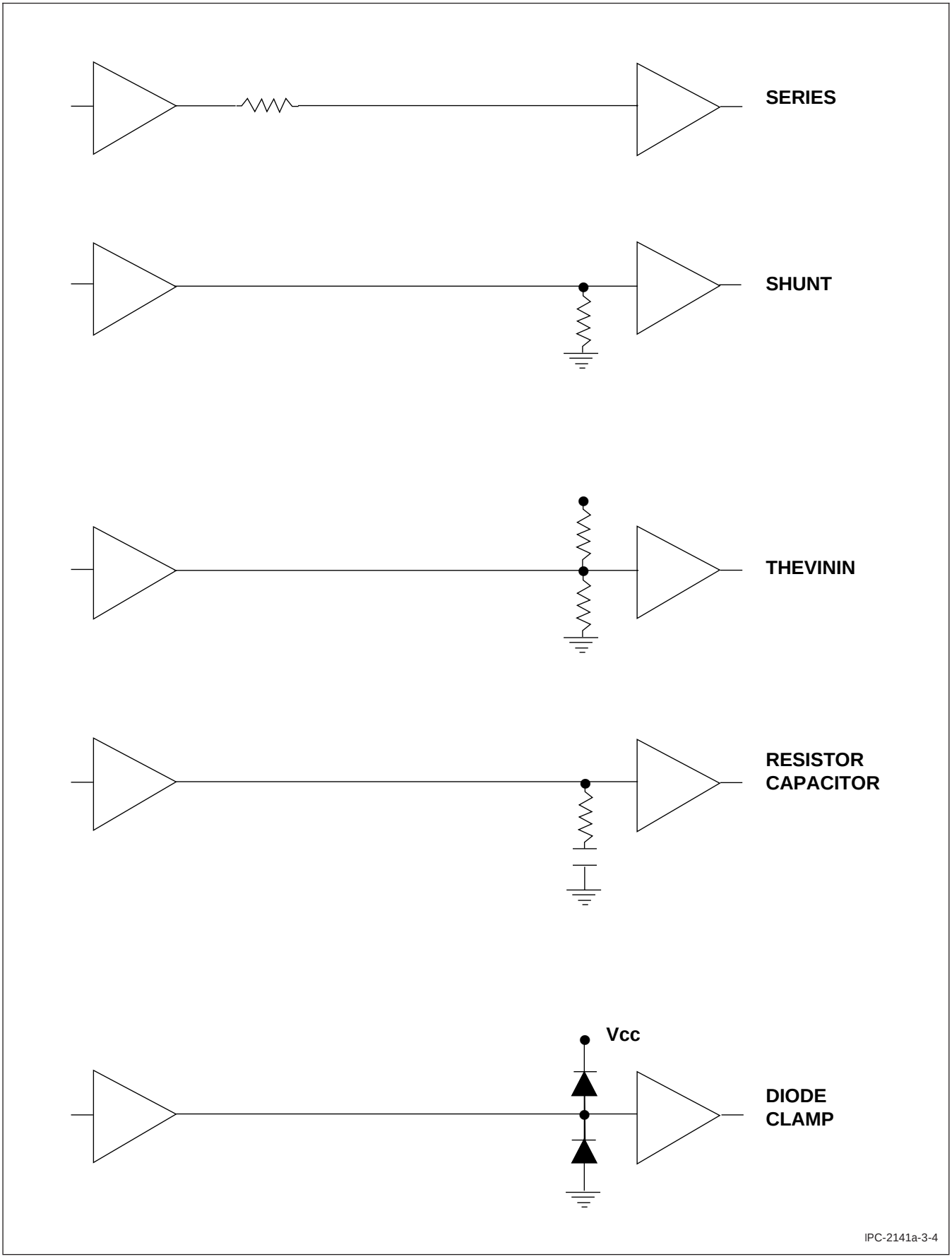

Figure 3-4 Termination of Nets

Series resistor terminations use a resistor in series between the driver and the line and are most commonly used to match the net to the driver impedance. A series termination controls overshoot, requires only one component and consumes little power, but can effect pulse rise time and/or fall time. To be most effective, the series resistor must be placed as close as possible to the driver. The driver series resistance plus that of the termination resistor should equal the interconnect characteristic impedance.

Shunt terminations connect the end of a net to the ground. A serial chain load with a driver is a typical application. The resistance value of the termination resistor must match the impedance value of the net impedance. Shunt terminations will exhibit small reflection coefficients, provide easy routing of distributed loads, and do not cause changes in propagation delay relative to the designed values.

Thevinin terminations are resistor dividers that are usually connected to voltage and ground at the end of the net. As with the shunt termination, there is no change in the designed propagation delay. With the Thevinin termination, a defined DC bias is established on the line by choice of resistor values, and switching of the entire applied voltage occurs at the load. This termination consumes more power than other terminations described here, requires two components, and effects the DC offsets for the high and low logic states.

Resistor capacitor terminations, called AC terminators, are placed at the load end of the net. These terminations control overshoot and spiking, consume no DC power, and filter high-frequency components of the signal. The value of the resistor is matched to the impedance of the transmission line and the capacitance value must be chosen so that its impedance is nominally zero at frequencies exceeding the 3 dB attenuation bandwidth of the pulse.

A diode clamp termination can be either pulled up by V_{cc}, pulled to ground, or both. The effect is to limit the magnitude of the overshoot and undershoot values (see 3.4.14.2). Diode clamps do not terminate nets and are the more expensive solution to a reflection problem.

3.4.14 Additional Signal Integrity Issues In addition to the above signal integrity issues, other effects may have to be considered in high speed/high frequency design. Some of these are skew, overshoot, ring back, threshold violations, and coupling due to simultaneous switching.

3.4.14.1 Skew Skew is a timing problem and is caused by different delays among a group of pulses that should nominally arrive at a given node at the same instant but do not. Skew may cause timing errors in the circuit. As an example, clocks and their timing relationship to clock-synchronized devices may be affected by skew. Skew can be affected by conductor impedance, differing conductor lengths, power supply variation, device tolerances and load capacitance of inputs.

3.4.14.2 Overshoot and Undershoot Overshoot refers to signal voltages that exceed V_{cc} and undershoot refers to signal voltages that are less than the reference (typically ground) potential. Devices in a circuit have varying tolerance to overshoot and undershoot and the designs of the interconnecting structures should take device requirements into consideration. Overshoot can be controlled by different schemes external to the devices by some of the termination methods discussed in 3.14.11.

3.4.14.3 Ring Back Ring back occurs when the rising edge of a logic transition meets or exceeds the logic threshold and then recrosses the threshold before settling. This can be caused by mismatch (such as in input vs output device impedance, input vs output signal risetime, input vs output signal amplitude) of logic drivers and receivers, poor termination techniques and impedance mismatch of the net to the devices.

3.4.14.4 Threshold Threshold violations are caused when a pulse does not reach the voltage threshold level for an input device. Weak drivers or poor terminations are often the cause of this problem although it can also be caused by device drivers with a large risetime to pulse width ratio.

3.4.14.5 V_{cc}/Ground Bounce Simultaneous switched outputs may be inductively coupled between V_{cc} and ground. This coupling may affect the risetime and falltime of pulses generated by an output device and, consequently, affect the switching instant of an input device. Without adequate electrical models of the V_{cc} and ground layouts and of the package, accurate simulation of V_{cc} and ground bounce is difficult. Provision for low inductance connections using wider conductors helps to reduce the inductive effects.

3.4.15 Noise

3.4.15.1 Switching Noise When devices are switching, current is either drawn from or passed to the power supply through the power/ground paths. When this current has high frequency components, the self inductance of the leads and traces become significant, leading to transient or switching noise. These transients are caused by the inductance of the power/ground loop and the layout must be designed to reduce this inductance as much as possible.

A common technique to reduce switching noise is the use of decoupling capacitors that serve to provide the required current from a point closer to the IC than the power supply. When this is done, the positioning of the capacitor is important. If the capacitor leads are too long, the self

inductance becomes too high and unwanted switching of adjacent circuits occur. The decoupling on boards is normally achieved with discrete capacitors that are closely positioned near the device and are connected to power and ground with short interconnect lengths.

The most effective way to minimize the effects of lead inductance in a circuit is to choose component packages with very short leads and then to connect them into the power and ground planes with the shortest possible path. The best technique is to use a via at the component land that is connected directly to the power or ground planes.

3.4.15.2 Other Parasitic Noise Multilayer boards have advantages over double sided boards in that the power/ground planes in multilayer boards are continuous planes of metallization. Consequently, multilayer boards offer a lower RF impedance to the spurious currents and improved current distribution compared to a single layer board. The current loop is significantly reduced in multilayer boards compared to single layer boards because the current path is bounded by the length of the signal line and the distance to the power/ground planes. For further improvements in multilayer designs, signal lines in adjacent signal layers can be run orthogonally thus reducing the crosstalk due to the small crossover area between conductors. Continuous power and ground layers will also serve to isolate noisy signal conductors by shielding their emissions.

3.4.15.3 Noise Budget/Noise Margin The noise budget of a device is the variation in the system DC and AC voltages for which the device can still operate within specifications. There are two primary components of the noise budgets. The first is the DC power supply noise of each integrated circuit, and the second is the device logic signal AC noise budget.

Each logic device connects to a voltage and a ground return. The system power distribution has finite AC and DC voltage drops between the power supply and component. Also the power supply has a designated operating tolerance. The primary parameters that are included for the noise margin are:

a. Power supply variation
b. Reflections
c. Ground bounce
d. Ground offsets
e. Thermal offsets
f. Crosstalk
g. Ground IR drop
h. Reference accuracy
i. Terminator noise

The noise budget also includes reflections, coupling noise, and ground bounce in the power leads.

References

1. C.S. Chang and A.P. Agrawal, ‘‘Fine line thin dielectric circuit board characterization,’’ Proceedings of Electronic Components and Technology Conference, 1994.
2. S.B.Cohn, ‘‘Problems in strip transmission lines,’’ IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-3, March 1955, pp. 119-126.

4 DESIGN OF CONTROLLED IMPEDANCE CIRCUITS

There are many considerations in high-speed circuit design. It is the job of the circuit designer to understand the system specifications and weigh the alternatives to provide the simplest, most cost effective, most reliable solution for meeting those specifications, including the selection of the best printed wiring or discrete wiring board features. In cases where high speed signals are present, the signal conductors may need to be considered as transmission lines. This means, as a minimum, that the designer must specify the characteristic impedance, Z_0, of those lines. Since transmission lines should be terminated into its characteristic impedance to avoid signal degradation, a designer may also provide for termination.

The tolerance and value of the termination resistors must be chosen to match the Z_0 of the transmission line and other circuit design requirements. The following should be considered:

a. Terminating each signal line increases circuit density and complexity.
b. Placement of the termination resistors should be made so that signals travel the shortest path from source (driver) to load (termination).
c. Circuit board technology must be capable of controlling impedance.
d. Minimum component-to-component spacing may eliminate the need for controlled impedance lines but may increase etch density.

Placing high-speed components close together may reduce the need for using transmission line and thus reduce crosstalk problems. However, this may also result in thermal management problems and in increasing the number of layers required to produce a wiring board with the same number of I/O. Increasing the spacing between devices will reduce the thermal problems but could increase crosstalk and impedance restrictions.

Circuit impedance is important in board design for several reasons. First, the amount of current that a circuit element (driver) will need depends upon Z_0. This is taken into account in the design of ICs and can affect how many receivers may be placed along the circuit (see 3.4.11 on signal loading effects). Furthermore, in high-speed systems, any impedance mismatch experienced by a signal propagating along the transmission line will cause reflections. These

reflections not only reduce the amount of power reaching the receiver, but also may cause ringing along the circuit.

In high-speed circuits, because the propagation time of the pulse along the signal conductor is greater than transition duration (rise or fall time) of the pulse, the impedance experienced by the pulse is not affected by the termination until it reaches the termination. The effect of the resistivity of the conductor material (typically copper) is not significant for typical conductor widths and thicknesses but may be a concern as the frequency bandwidth of the propagating pulses increases and as the width of the signal conductors decreases. Both of these effects are a result of the fact that the ratio of driving voltage to current flow (V/I = impedance) is established before the signal reaches the end of the circuit.

4.1 Unbalanced Line Configurations Unbalanced transmission lines are also called uncoupled transmission lines or, more commonly, single-ended transmission lines. Unbalanced lines consist of one signal line and either one or two ground (reference) planes. Diagrams of two types of unbalanced transmission line configurations are shown in Figure 4-1, the microstrip and stripline configurations. These are the most commonly used unbalanced line configurations.

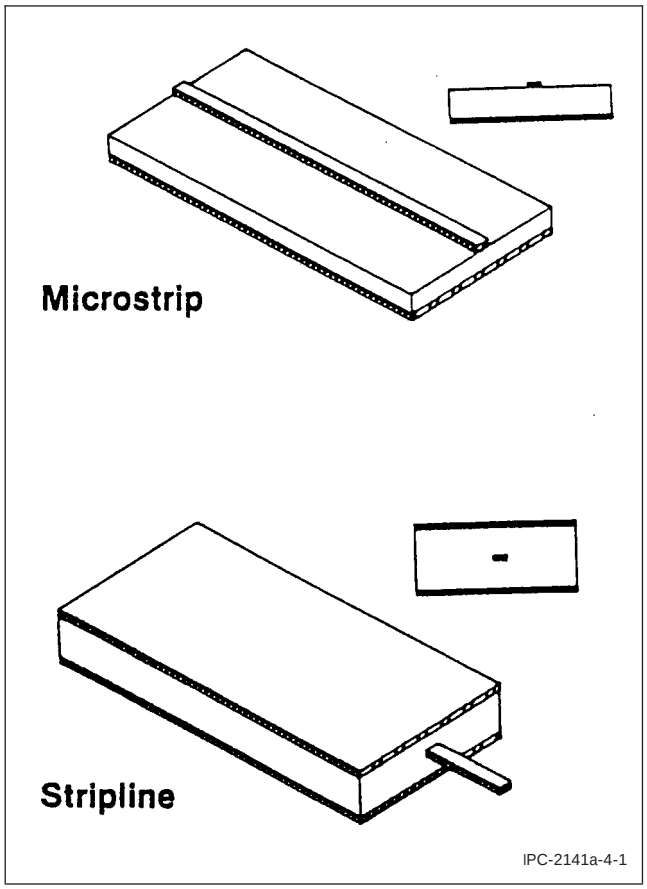

Figure 4-1 Diagrams of two types of unbalanced transmission line configurations.

The electrical diagram for an unbalanced transmission line in a circuit is shown in Figure 4-2. A single conductor is the most common way to make connections between two devices. A single conductor can connect the source of one device to the load of another device, as shown in Figure 4-2. If these are high speed devices, the conductor should be a controlled impedance interconnection. Unbalanced transmission lines have one signal conductor and a common return path, usually a power or ground plane. Since the signal conductor cross-section is different than the return (plane) conductor, this case is called an unbalanced line. This can be a coax line, an unshielded twisted pair, or a printed circuit board in either a microstrip or stripline configuration. In an ideal stripline, the signal line is precisely centered between the two reference planes; in practice, however, this situation rarely occurs and the signal line is offset.

The unbalanced lines considered here and their geometries are shown in Figure 4-3. Descriptions of the most commonly used types of unbalanced lines, microstrip and stripline, is also given.

4.1.1 Microstrip A microstrip line consists of a signal conductor separated from a ground or reference plane that is at least 100 times the width of the signal line. The signal and ground are separated by a layer of dielectric. In the simplest case, the signal conductor sits on the surface of an outer dielectric layer and is otherwise surrounded by air ($\varepsilon_{r,air}$ = 1.0) or a solder mask material on its top and edges.

A special case of a microstrip transmission line is the embedded microstrip line where the line is buried some distance beneath the surface of the board and is surrounded by a solid dielectric. The buried microstrip has a single reference plane that is separated from the signal conductor by a layer of dielectric. One case of the buried microstrip is where outer layer circuitry is covered by solder mask material. However, the solder mask is relatively thin and if the electric field extends beyond the solder mask and into the air, then the effect of air must also be considered. The discrete wire board is another example of an embedded microstrip construction. In this case, the discrete wire is embedded in a dielectric and encapsulated by additional solid dielectric.

4.1.2 Stripline A stripline consists of a signal line that is embedded in solid dielectric between two reference planes. As in the case of microstrip, the width of the reference planes should be much greater than that of the signal line. There are two variations of the stripline configuration, one where the stripline is centered between the reference planes and another where the stripline is not centered. In this case, the influences of the two reference planes on the signal line are not equal, but are proportional to the distances that separate them from the signal line. Discrete wire boards are often constructed in stripline configurations where one or

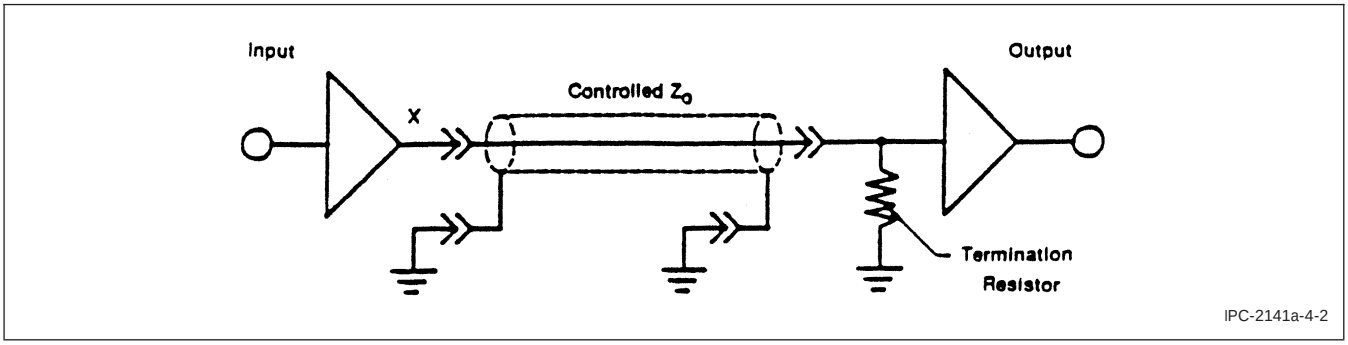

Figure 4-2 Circuit schematic showing unbalanced transmission line.

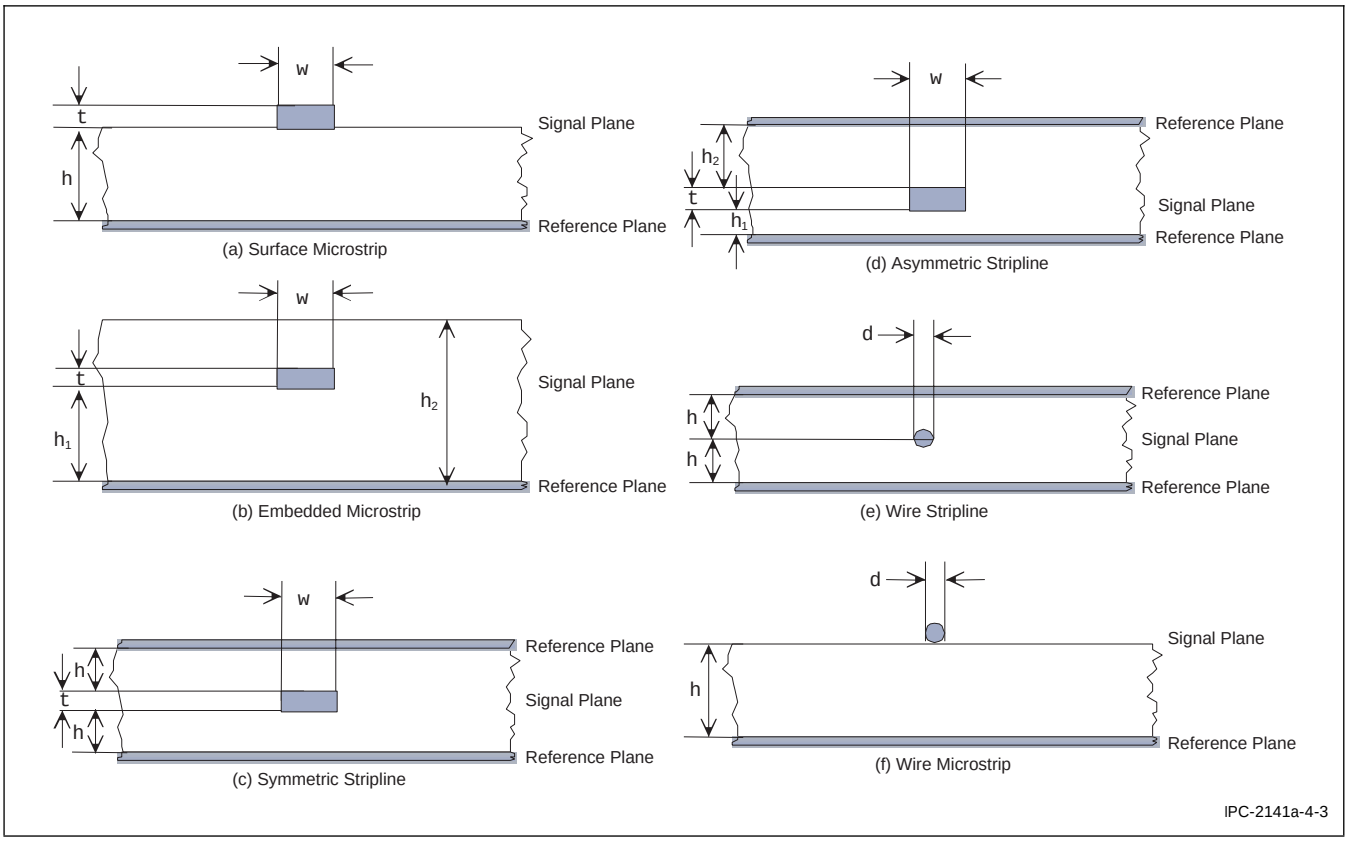

Figure 4-3 Typical unbalanced line configurations.

more wiring layers are embedded in solid dielectric sandwiched between two reference planes.

Designs for both controlled capacitance and impedance use calculations to predict the capacitance of a conductor as well as its characteristic impedance. The equations, which are given below for some unbalanced line configurations, are based on empirical work and are unique for different configurations.

4.2 Unbalanced Line Equations Z_0 is the impedance, given in Ohms. Unbalanced line configurations are shown in Figure 4-3. Although equations are useful in predicting transmission line characteristics, it is recommended that electromagnetic (em) field solving software be used to predict transmission line properties of structures that will actually be fabricated. This is because the equations do not accurately describe the complicated structure of a printed wiring board transmission line. For example, the dielectric constant of the materials below, above, and at the sides of the conductors for any transmission line structure may be different. Equations presently do not have the ability to address this situation whereas em field solvers do. Also, the width of the conductor is typically described as having a rectangular cross section. In practice, however, the cross section is usually trapezoidal. Although corrections to transmission line equations do exist to accommodate for trapezoidally shaped cross sections, this situation is more accurately solved with em field solvers than with equations. Deviation of the transmission line cross section from rectangular increases as the metal thickness increases.

Note: The IPC maintains a noncomprehensive list of signal integrity software vendors on its website at www.ipc.org. These vendors provide programs used for signal integrity analysis and controlled impedance.

4.2.1 Capacitance per Unit Length The capacitance per unit length for any of these transmission line structures can be approximated using the propagation time per unit length (reciprocal of propagation speed) for an ideal representation of the given structure. The propagation speed in a given transmission line is given in 3.4.7.3. This speed is also proportional to the phase function described in 3.4.7. For an ideal structure, the speed computed from the phase function is:

$$\nu = \frac{1}{\sqrt{LC}} \quad [4\text{-}1]$$

Equating this with the equation in 3.4.7.3 gives:

$$\nu = \frac{1}{\sqrt{LC}} = \frac{c}{\sqrt{\varepsilon_{r,eff}}} \quad [4\text{-}2]$$

where c is the speed of light. Multiplying [4-2] by the characteristic impedance for an ideal transmission line (see 3.4.6.2) and then solving for C gives:

$$C = \frac{\sqrt{\varepsilon_{r,eff}}}{cZ_{0,l}} \quad [4\text{-}3]$$

4.2.2 Surface Microstrip, Figure 4-3(a) The characteristic impedance, $Z_{0,surf}$, is (1,2):

$$Z_{0,surf} = \frac{\eta_0}{2\sqrt{2\pi}\sqrt{\varepsilon_{r,eff}+1}} \ln\left\{1+4\frac{h}{w'}\left[4\left(\frac{14\varepsilon_{r,eff}+8}{11\varepsilon_{r,eff}}\right)\frac{h}{w'} + \sqrt{16\left(\frac{14\varepsilon_{r,eff}+8}{11\varepsilon_{r,eff}}\right)^2\left(\frac{h}{w'}\right)^2 + \frac{\varepsilon_{r,eff}+1}{2\varepsilon_{r,eff}}\pi^2}\right]\right\} \quad [4\text{-}4]$$

where η_0 is the wave impedance of free space, w' is the effective signal line width:

$$w' = w + \frac{t}{\pi}\ln\left\{\frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2 + \left(\frac{t}{w\pi + 1.1t\pi}\right)^2}}\right\}\left(\frac{\varepsilon_{r,eff}+1}{2\varepsilon_{r,eff}}\right) \quad [4\text{-}5]$$

and

$$\varepsilon_{r,eff} = \left\{\frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left\{\sqrt{\frac{w}{w+12h}} + 0.04\left(1-\frac{w}{h}\right)^2\right\} \quad \frac{w}{h}<1\right\}$$

$$\varepsilon_{r,eff} = \left\{\frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\sqrt{\frac{w}{w+12h}} \quad \frac{w}{h}\geq 1\right\} \quad [4\text{-}6]$$

where w is the width of the signal line, t is the thickness of the signal line, h is the separation between the signal line and the reference plane, and ε_r is the relative permittivity of the substrate material. The accuracy of these equations is better than ± 2% (1,2). For more accuracy, the effect of conductor thickness should be considered (3).

4.2.3 Embedded Microstrip, Figure 4-3(b) The effect of embedding the signal line in a single dielectric is to modify [4-4] using a modified $\varepsilon_{r,eff}$ (2):

$$Z_{0,embedd} = Z_{0,surf}\frac{1}{\sqrt{e^{-2b/h} + \frac{\varepsilon_r}{\varepsilon_{r,eff}}\left(1-e^{-2b/h}\right)}} \quad [4\text{-}7]$$

where

$$b = h_2 - h_1 \quad [4\text{-}8]$$

4.2.4 Symmetric Stripline, Figure 4-3(c) As was the case for microstrip transmission line, the Z_0 of stripline is also dependent on the ratio of the conductor width and separation between the signal and ground planes. The are two commonly used set of equations for $Z_{0,SS}$ of a symmetric stripline.

4.2.4.1 Formula Set 1 From (2) is:

$$Z_{0,SS} = \frac{\eta_0}{2\pi\sqrt{\varepsilon_r}}\ln\left\{1+\frac{8h}{\pi w'}\left[\frac{16h}{\pi w'} + \sqrt{\left(\frac{16h}{\pi w'}\right)^2 + 6.27}\right]\right\} \quad [4\text{-}9]$$

where

$$w' = w + \frac{t}{\pi}\ln\left\{\frac{e}{\sqrt{\left(\frac{t}{4h+t}\right)^2 + \left(\frac{\pi t}{4(w+1.1t)}\right)^m}}\right\} \quad [4\text{-}10]$$

and

$$m = \frac{6h}{3h+t} \quad [4\text{-}11]$$

According to (2), the errors for this set of formulas is less then 1.5%.

4.2.4.2 Formula Set 2 Can be further broken down into two cases, one for a narrow signal conductor and one for a wide signal conductor. For the narrow signal conductor, that is for $w/b < 0.35$, the appropriate formula for the characteristic impedance, $Z_{0,ss,t-2}$, is (4,5):

$$Z_{0,ss,t-2} = \frac{60}{\sqrt{\varepsilon_r}}\ln\left(\frac{4b}{\pi D}\right) \quad [4\text{-}12]$$

where

$$b = 2h + t \quad [4\text{-}13]$$

and

$$D = \frac{w}{2}\left\{1+\frac{t}{\pi w}\left[1+\ln\left(\frac{4\pi w}{t}\right)\right]+0.551\left(\frac{t}{w}\right)^2\right\} \quad [4\text{-}14]$$

Equation [4-12] is based on a circular wire approximation wherein the width of the signal conductor is so small relative to the other dimensions of the transmission line that the signal conductor can be approximated as a round wire (see 4.2.6). This equation is valid for $t/b \leq 0.25$ and $t/w \leq 0.11$ (4).

For the wide signal conductor, that is for $w/b \geq 0.35$, the appropriate formula for the characteristic impedance, $Z_{0,ss,w\text{-}2}$ is (4,5):

$$Z_{0,ss,w-2} = \frac{94.15}{\left(\frac{w/b}{1-t/b}+\frac{\theta}{\pi}\right)} \quad [4\text{-}15]$$

where

$$\theta = \left(\frac{2b}{b-t}\right)\ln\left(\frac{2b-t}{b-t}\right)-\left(\frac{t}{b-t}\right)\ln\left[\frac{2bt-t^2}{(b-t)^2}\right] \quad [4\text{-}16]$$

The stated error in Equations [4-12] and [4-16] is less than 1.3%, and the worst case error is at $w/b = 0.35$ (5).

4.2.5 Asymmetric Stripline, Figure 4-3(d) The $Z_{0,AS}$ for an asymmetric stripline is given by (2):

$$Z_{0,AS} = \frac{1}{\varepsilon_r}\left[Z_{0,SS}\left(\varepsilon_r = 1,\ b=h_1+h_2+t\right)-\Delta Z_{0,air}\right] \quad [4\text{-}17]$$

where $Z_{0,SS}(\varepsilon_r=1,b=h_1+h_2+t)$ is the $Z_{0,SS}$, see Equation [4-9], with air as the dielectric and having total thickness, b, equal to h_1+h_2+t; $\Delta Z_{0,\text{air}}$ is:

$$\Delta Z_{0,air} = 0.0325\pi Z_{0,air}^2\left(0.5-\frac{1}{2}\frac{2h_1+t}{h_1+h_2+t}\right)^{2.2}\left(\frac{t+w}{h_1+h_2+t}\right)^{2.9} \quad [4\text{-}18]$$

where h_1 is the distance between the signal line and the lower reference plane, h_2 is the distance between the signal line and the upper reference plane, and

$$Z_{0,air} = 2\left[\frac{Z_{0,SS}(\varepsilon_R=1,b=h_1)Z_{0,SS}(\varepsilon_R=1,b=h_2)}{Z_{0,SS}(\varepsilon_R=1,b=h_1)+Z_{0,SS}(\varepsilon_R=1,b=h_2)}\right] \quad [4\text{-}19]$$

where $Z_{0,SS}(\varepsilon_r=1,b=h_1)$ is the $Z_{0,SS}$ see Equation [4.9], with air as the dielectric and having total thickness, b, equal to h_1; and $Z_{0,SS}(\varepsilon_r=1,b=h_2)$ is the $Z_{0,SS}$ with air as the dielectric and total thickness, b,equal to h_2.

4.2.6 Wire Stripline, Figure 4-3(e) The Z_0 of a transmission line consisting of a circular signal conductor having a diameter d and centered between parallel ground planes separated by a distance h is (4):

$$Z_0 = \frac{\eta_0}{2\pi\sqrt{\varepsilon_r}}\ln\left(\frac{4h}{\pi d}\right) \quad [4\text{-}20]$$

This equation is accurate to within 1% for $d \leq h/2$ (4).

4.2.7 Wire Microstrip, Figure 4-3(f)

$$Z_0 = \frac{\eta_0}{2\pi\sqrt{\varepsilon_{r,eff}}}\cosh^{-1}\left(\frac{2h}{d}\right) \quad [4\text{-}21]$$

where d is the wire diameter and h is the separation between the wire and the ground (reference) plane, and $\varepsilon_{r,eff}$ is given by (4-6). To compute $\varepsilon_{r,\text{eff}}$ using Equation [4-6], d is obtained from (2):

$$\frac{d}{w} = 0.5008+1.0235x-1.023x^2+1.1564x^3-0.4749x^4 \quad [4\text{-}22]$$

where

$$x = \left\{\frac{t}{w} \quad w \geq t\right\}$$

$$x = \left\{\frac{w}{t} \quad w < t\right\} \quad [4\text{-}23]$$

4.3 Balanced Line Configuration Balanced transmission lines are also called coupled transmission lines or, more commonly, differential transmission lines. These structures contain two signal conductors in their design. High performance digital systems use balance lines, also called differential configurations, to provide better noise immunity and improved timing. The differential configuration (Figure 4-4 depicts two commonly used differential structures) has different controlled impedance calculations and measurement techniques compared to the more common unbalanced line. A balanced transmission line has two signal conductors usually accompanied by a reference plane or a cable shield, and is most often used to transmit differential signals. The geometrical and electrical relationship between the two signal lines and the common reference are ideally the same, and this is why it is called a balanced line. However, the two lines are usually slightly different in geometry or in their relationship to the reference plane. As with unbalanced line configurations, it is recommended that electromagnetic field solvers be used to predict transmission line characteristics (see 4.2).

An electrical schematic showing a circuit using a balanced transmission line is provided in Figure 4-5. The true signal and its logical complement are connected to the load. High

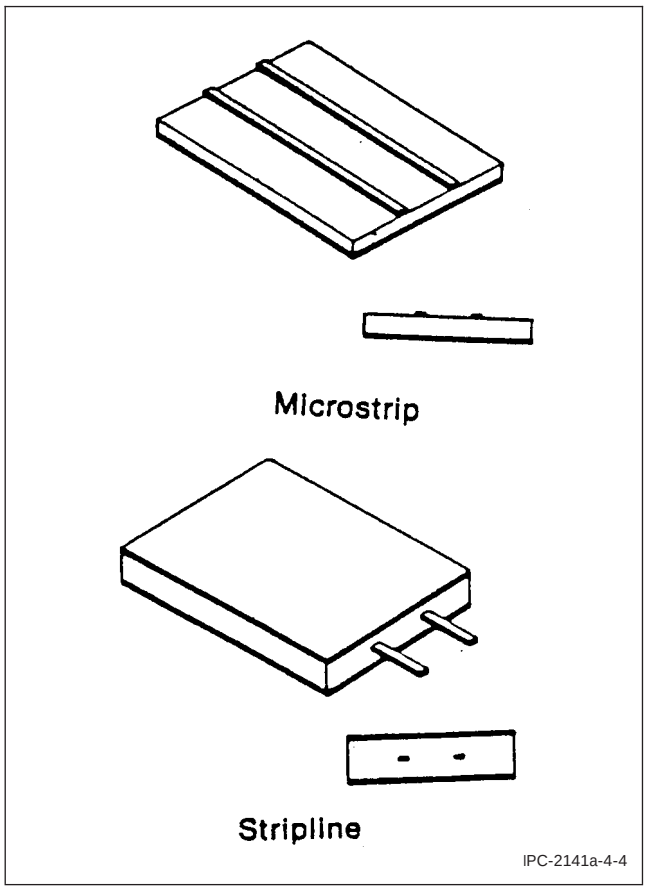

Figure 4-4 Balanced line structure.

speed devices typically use controlled impedance transmission lines, which can be achieved with a twisted wire pair within a metallic shield, a pair of coaxial lines, or two signal lines in a planar environment, as shown in Figure 4-4. The cross-sections of typical transmission lines used for differential connections are shown in Figure 4-6.

There are advantages to the differential connection. If the signal conductors carrying the complementary signals are in close proximity to each other, then when these signals are switched, the radiated fields generated will cancel each other thus reducing electromagnetic interference (EMI). Furthermore, because the receiver is seeing the differential voltage between the two signal conductors, the common mode noise is ignored by the receiver. The disadvantage of the balanced line is that two signal paths are required and that each signal path must be matched for characteristic impedance and time delay (or electrical length). ECL devices provide true and complementary output, but CMOS and TTL logic do not, except line drivers.

The three configurations, edge-coupled surface microstrip, edge-coupled stripline, and broadside-coupled stripline are shown in Figure 4-6 and the equations in the following section. Because these equations are based on a model that may not accurately represent every circuit, it is strongly recommended that manufacturers empirically verify results by characterizing their own process and designs.

Testing of and test configuration for differential transmission lines is covered in 9.4.5.

4.3.1 Even Versus Odd Mode Propagation When a transmission line structure contains two signal lines, there are two possible propagation modes, the even mode and the odd mode. The even mode describes the case when the two propagating signals, one on each of the two signal lines, are identical in amplitude as a function of time. That is, the amplitude of the two signals are equal (same magnitude and same polarity) and exhibit zero delay. Zero delay means that identical features on the two signals occur at the same instant and on the same location on their respective signal lines. In practice, this is achieved by connecting both signal lines to the same connection of a signal source. In the even mode, the electric fields are directed as shown in the top sketch of Figure 4-7.

The other mode of propagation, the odd mode, describes the case when the signals propagating on the two signal lines are of equal amplitude, opposite polarity, and exhibit zero delay. The field lines for the odd mode of propagation are shown in the lower sketch of Figure 4-7. The odd mode is achieved by driving the two signal lines differentially, that is, by driving the two signals lines with signals of equal amplitude but opposite polarity.

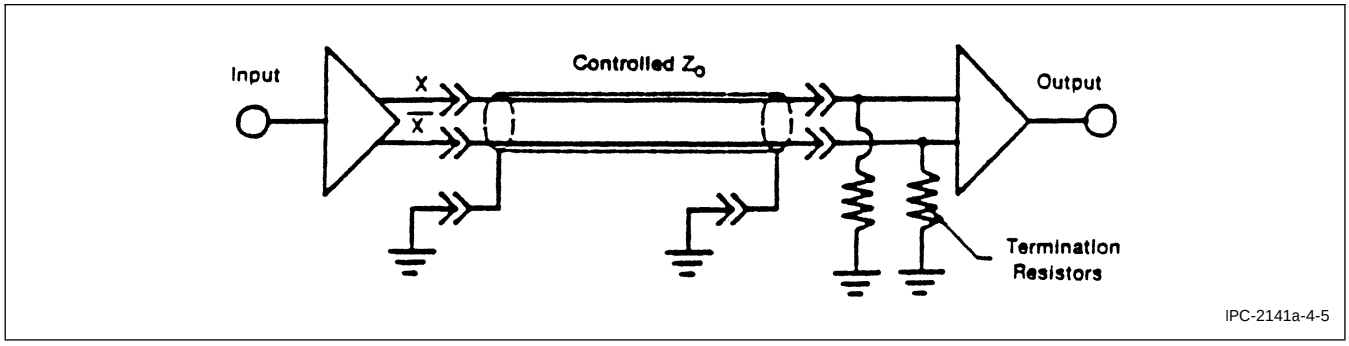

Figure 4-5 Circuit schematic showing balanced transmission line.

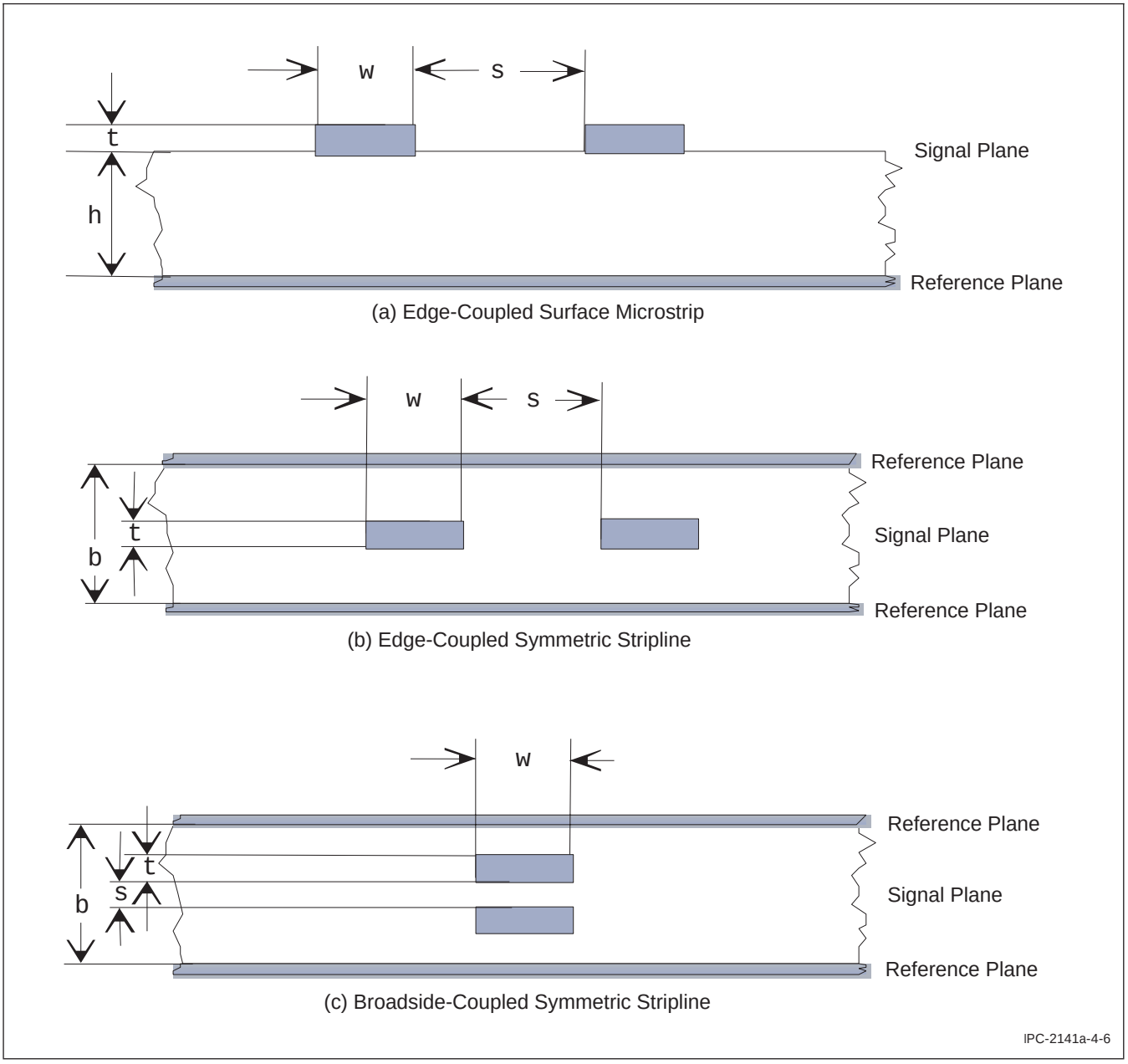

Figure 4-6 Cross-sections of typical balanced line configuration.

4.3.2 Even Mode, Odd Mode, Common Mode, and Differential Mode Impedances The even mode impedance is the impedance of one of the two signal lines of a balanced transmission line when the two signal lines are driven by a common signal. Similarly, the odd mode impedance is the impedance of one of the two signal lines when the two signal lines are driven differentially. The capacitance is greater and inductance lower for a balanced transmission line that is driven differentially than if it is driven otherwise. Consequently, the characteristic impedance is lower for the odd mode of propagation than it is for the even mode of propagation or for a single-end transmission line of similar construction to the balanced line. The propagation velocity may also be different for the odd mode and even mode in a balanced structure and for a single-end transmission line. For example, in surface microstrip using geometries and materials identical to that used in a balanced structure, the even mode impedance of a balanced design is greater than that for a single-ended design and the propagation velocity is less than that for a single-ended design, and the odd mode impedance of a balanced design is less than that for a single-ended design and the propagation velocity is greater than that for a single-ended design.

The common mode impedance is the parallel combination of the even mode impedances of the two signal lines. The differential impedance is the series combination of the odd mode impedances of the two signal lines. Consequently, the differential impedance will typically be greater than the

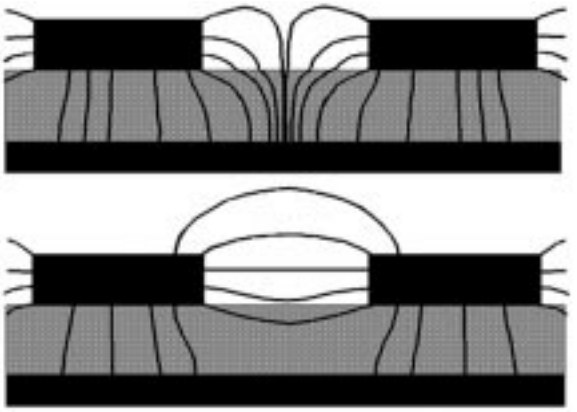

Figure 4-7 Electric field lines for even (top) and odd (bottom) modes of propagation in a balanced transmission line. The two smaller black rectangles in each sketch represent the two signal lines and the long black rectangle represents the reference plane.

common mode impedance or the impedance of a single-end transmission line of similar construction.

4.4 Balanced Line Equations Configurations for balanced lines considered here are shown in Figure 4-6. The specific formulas for calculating Z_0 of the balanced line configurations exist in various forms, some of which are not in agreement. Research is currently underway to resolve these differences by means of both mathematical study and sample verification. IPC maintains a noncomprehensive list of signal integrity software vendors that provide methods for computing Z_0 of balanced lines on their website at www.ipc.org.

4.4.1 Edge-Coupled Surface Microstrip The equation for the odd mode impedance, $Z_{0,o}$ for this structure, shown in Figure 4-6(a), is (2,6):

$$Z_{0,o}(0) = \frac{Z_0(0)\sqrt{\frac{\varepsilon_{r,eff}(0)}{\varepsilon_{r,ett,o}(0)}}}{1 - \frac{Z_0(0)}{\eta_0}\sqrt{\varepsilon_{r,eff}(0)Q_{10}}} \quad [4\text{-}24]$$

where

$Z_0(0)$ is given by equation [4-4],
$\varepsilon_{r,eff}(0)$is given by equation [4-6],

$$\varepsilon_{r,eff,o}(0) = \left[0.5(\varepsilon_r+1) + a_0(u,\varepsilon_r) - \varepsilon_{r,eff}(0)\right] e^{-c_0 g^{d_0}} + \varepsilon_{r,eff}(0) \quad [4\text{-}25]$$

with

$$a_0(u,\varepsilon_r) = 0.7287\left[\varepsilon_{r,eff}(0) - 0.5(\varepsilon_r+1)\right]\left(1 - e^{-0.179u}\right) \quad [4\text{-}26]$$

$$c_0 = b_0(\varepsilon_r) - \left[b_0(\varepsilon_r) - 0.207\right]e^{-0.414u} \quad [4\text{-}27]$$

$$b_0(\varepsilon_r) = \frac{0.747\varepsilon_r}{0.15+\varepsilon_r} \quad [4\text{-}28]$$

$$d_0 = 0.593 + 0.694e^{-0.562u} \quad [4\text{-}29]$$

and

$$u = \frac{w}{h} \quad [4\text{-}30]$$

Q_{10} is (2,6):

$$Q_{10} = \frac{1}{Q_2}\left(Q_2Q_4 - Q_5e^{\left[\ln(u)Q_6u^{-Q_9}\right]}\right) \quad [4\text{-}31]$$

where

$$Q_1 = 0.8695u^{0.194} \quad [4\text{-}32]$$

$$Q_2 = 1 + 0.7519g + 0.189g^{2.31} \quad [4\text{-}33]$$

$$Q_3 = 0.1975 + \left[16.6 + \left(\frac{8.4}{g}\right)^6\right]^{-0.387} + \frac{1}{241}\ln\left[\frac{g^{10}}{1+\left(\frac{g}{3.4}\right)^{10}}\right] \quad [4\text{-}34]$$

$$Q_4 = \frac{2Q_1}{Q_2\left[e^{-g}u^{Q_3} + (2 - e^{-g})\,u^{-Q_3}\right]} \quad [4\text{-}35]$$

$$Q_5 = 1.794 + 1.14\ln\left(1 + \frac{0.638}{g + 0.517g^{2.43}}\right) \quad [4\text{-}36]$$

$$Q_6 = 0.2305 + \frac{1}{281.3}\ln\left[\frac{g^{10}}{1+\left(\frac{g}{5.8}\right)^{10}}\right] + \frac{1}{5.1}\ln(1 + 0.598g^{1.154}) \quad [4\text{-}37]$$

$$Q_7 = \frac{10 + 190g^2}{1 + 82.3g^3} \quad [4\text{-}38]$$

$$Q_8 = e^{\left[-6.5 - 0.95\ln(g) - \left(\frac{g}{0.15}\right)^5\right]} \quad [4\text{-}39]$$

$$Q_9 = \ln(Q_7)\left(Q_8 + \frac{1}{16.5}\right) \quad [4\text{-}40]$$

and

$$g = \frac{s}{h} \quad [4\text{-}41]$$

4.4.2 Edge-Coupled Symmetric Stripline The equation for the odd mode impedance, $Z_{0,o}$ for this structure, shown in Figure 4-6(b), is (2,7), for $s/t \geq 5.0$:

$$Z_{0,o}\left(\frac{w}{b},\frac{t}{b},\frac{s}{b}\right)=\left\{\frac{1}{Z_0\left(\frac{w}{b},\frac{s}{b}\right)}-\frac{C_f'\left(\frac{t}{b}\right)}{C_f'(0)}\left[\frac{1}{Z_{0,o}\left(\frac{w}{b},0,\frac{s}{b}\right)}-\frac{1}{Z_0\left(\frac{w}{b},0\right)}\right]\right\}^{-1} \quad [4\text{-}42]$$

and for $s/t \leq 5.0$ is (2,7):

$$Z_{0,o}\left(\frac{w}{b},\frac{t}{b},\frac{s}{b}\right)=\left\{\frac{1}{Z_{0,o}\left(\frac{w}{b},0,\frac{t}{b}\right)}+\left[\frac{1}{Z_{0,o}\left(\frac{w}{b},0,\frac{s}{b}\right)}-\frac{1}{Z_0\left(\frac{w}{b},0\right)}\right]-\frac{2}{377\varepsilon}\left(C_f'\left(\frac{t}{b}\right)-C_f'(0)-\frac{\varepsilon}{s}\right)\right\}^{-1} \quad [4\text{-}43]$$

where

$Z_0(w/b,t/b)$ is given by equation [4-9],
Z_0(w/b,t/b) is the characteristic impedance for transmission lines having zero-thickness conductors (see (2,7)),

$$C_f'\left(\frac{t}{b}\right)=\frac{0.0885\varepsilon_r}{\pi}\left\{\frac{2b}{b-t}\ln\left(\frac{2b-t}{b-t}\right)-\left(\frac{2b-t}{b-t}\right)\ln\left[\frac{b^2}{(b-t)^2}-1\right]\right\} \quad [4\text{-}44]$$

and

$$C_f'(0)=\frac{0.0885\varepsilon_r}{\pi}2\ln 2 \quad [4\text{-}45]$$

4.4.3 Broadside-Coupled Symmetric Stripline The equation for the odd mode impedance, $Z_{0,o}$ for this structure, shown in Figure 4-6(c), is (2,8,9):

$$Z_{0,o}=\frac{293.9}{\sqrt{\varepsilon_r}}\frac{s}{b}\frac{1}{\tanh^{-1}(k)} \quad [4\text{-}46]$$

where k is the solution of:

$$\frac{w}{b}=\frac{1}{\pi}\left[\ln\left(\frac{1+R}{1-R}\right)-\frac{s}{b}\ln\left(\frac{k+R}{k-R}\right)\right] \quad [4\text{-}47]$$

and

$$R=\sqrt{\frac{k(kb-s)}{b-ks}} \quad [4\text{-}48]$$

According to (2), this equation is nearly exact for $w/s \geq 0.35$, and is more accurate for substrates with large values of ε_r.

4.5 Controlled Impedance Design Rules

4.5.1 Effect of External and Device Impedance When considering a controlled impedance/high speed design, the components and external I/O cables often determine the allowable values of transmission line impedance. For example, if a coaxial cable is used as the external I/O cable, the characteristic impedance (Z_0) of the board interconnects (transmission lines) will be constrained by the characteristic impedances of standard coaxial cables, which have values of 50 Ω, 75 Ω, and 93 Ω. Also, impedance values of components are often in the range of 50 Ω to 85 Ω, and this puts another constraint on the Z_0 of the board interconnects.

4.5.2 Material Properties and Transmission Line Geometry The range of widths for transmission line conductors is generally in the range of 0.076 mm to 0.76 mm [0.003 in to 0.03 in], which limits interconnect design options. Dielectric thicknesses also restrict the choices for the physical design of the transmission line. The range of relative permittivity of the dielectric is also fairly narrow, 2.9 to 4.7. Although more exotic materials may be used for very high frequency applications, economics dictate the use of more conventional material for the bulk of consumer and commercial applications.

4.5.3 High Impedance High impedance values in the board require narrow lines and/or thick dielectrics, split planes, or lower dielectric constant materials. However, practical printed circuit board fabrication limits, for example, 0.051 mm [0.002 in] for line width and dielectric thickness, limit how high of an impedance can be achieved. Discrete wiring boards offer an alternative to achieve high density interconnects with high impedance values and that are within practical board physical constraints. However, discrete wiring technology has a limited source of supply and this may restrict large volume production.

4.5.4 Impedance Design Considerations The following are design considerations for achieving controlled impedance interconnects.

a. *Conductor Cross Section* – Conductors, particularly on outer layers, are sensitive to width variations caused by plating and etching uniformity. Wider lines decrease impedance values whereas narrower lines increase it.

b. *Type of Transmission Line Structure* – For a given value of ε_r, spacing, and conductor width, impedance values will be greater for a microstrip than for a stripline.

c. *Relative Permittivity,* ε_r – Higher ε_r results in a lower impedance value while increasing propagation time.

d. *Dielectric Separation Between Signal and Ground* – Impedance decreases as separation decreases.

4.5.5 Secondary Controlled Impedance Design Factors

a. Use the thinnest copper possible that still satisfies the

other design requirements. Impedance decrease slightly as the copper thickness increases. This is a result of the increased edge capacitance for thicker transmission lines. However, as the thickness of the conductor decreases below 0.018 mm ([0.007 in], or ''1/2-oz'' copper) so does the reliability of the board, especially on thick (≥ 2.54 mm [0.10 in] thick) boards.

b. Keep controlled impedance conductors and reference planes, that are located on the same surface, far enough from each other to prevent coupling. A rule of thumb is that this spacing should be the greater of six times the widest signal conductor width or six times the ground to signal spacing.

c. The current return for high-speed signal is typically the reference plane(s) closest to the signal line. For microstrip, the reference plane is the plane immediately below the signal line and, for stripline, they are the planes immediately above and below the signal line. The return current should not encounter any partitions (voids or breaks) in the reference plane(s). Partitions in the reference plane may cause additional noise in the circuit, increase generated EMI, and increase plane impedance.

d. Critical signal conductors should be incorporated in an embedded microstrip or a stripline configuration.

e. If possible, avoid board constructions that approach fabrication limits, such as those using narrow conductors or thick boards because they are difficult to make, reduce reliability, and increase cost.

f. Use different line widths for each controlled impedance value on each signal layer.

g. Allow for the effects of solder mask in surface microstrip line design.

h. Allow the fabricator to adjust the board construction within design constraints, to meet the impedance requirements for the proposed line width and material sets.

i. If possible, do not use cross-hatched power or ground planes as this increases plane impedance.

j. Best results are obtained with no more than two signal planes between adjacent reference (ground or power) planes.

k. If two signal lines are located between adjacent reference planes, the signal lines in these planes should be routed orthogonally.

4.6 Crosstalk Guidelines Crosstalk is discussed in 3.4.12. Several guidelines can be used to control crosstalk. The most common techniques of reducing crosstalk effects in high density circuits are as follows (see IPC-2251):

a. Group common logic families together in the same area. Restrict signal conductors for each logic family to those areas.

b. Terminate controlled impedance conductors to reduce reflections.

c. Place components close together to minimize conductor lengths and the extent of parallel running lines.

d. Reduce the signal to ground separation.

e. Isolate noise emitters such as clocks, high speed communications I/O and high speed bus interconnect on separate layers with power/ground separators or in isolated area of the board.

f. Higher impedance transmission lines are more susceptible to crosstalk than low impedance lines.

g. High signal levels induce more crosstalk than low signal levels.

h. The use of guard lines between adjacent signal lines on the same plane will reduce crosstalk between these adjacent lines. The guard lines should be used in conjunction with the reference (ground and not power) plane of the signal line and be connected to this reference plane using vias. These via connections should be made at several places along the length of the guard line but, in the least, should be made at the ends of the guard line.

4.6.1 Crosstalk Implementation The impact on circuit board design due to implementation of the crosstalk rules will include:

a. Requirement of multiple power and ground planes.

b. Added complexity due to dense component placement.

c. Selective signal routing criteria.

These can greatly increase complexity and place limitations on the available circuit board technology.

In general, a board is populated as densely as possible with chip devices to minimize the size of the board and reduce signal propagation time between these devices. The result is that conductors are placed close to each other. The designer must then resort to multilayer or discrete wiring boards to handle the high interconnect density and the crossovers in the wiring plan.

4.7 Design Guidelines for Controlled Impedance Test Structures The following are rules for designing transmission line test structures that can be used in time-domain reflectometry (TDR) measurements and analysis. These test structures or interconnects (which are transmission lines) may be placed within the functional area of the board or within test coupons. (A coupon is a section of the board that is designated for test structures and is removed from the panel after board fabrication is completed). Although it is preferable to measure the performance of functional interconnects whenever possible, measuring specifically-designed test interconnects may be necessary when physical access to test points on the functional interconnect is not available or if the design of the functional interconnect

does not allow sufficient resolution for the test equipment used.

4.7.1 Purpose of Test Coupon Test interconnect design seeks to ideally emulate the electromagnetic properties, specifically the characteristic impedance, of the functional interconnect (the transmission line connecting devices on a board). However, differences between the characteristics of test and functional interconnects will exist, especially for test interconnects located in panel coupons (that is, outside of the functional area). Issues that can affect this lack of measurement correlation between functional and test interconnects include higher circuit densities in the functional interconnect area that cause different coupling compared to the test interconnects, etching variations, laminate thickness and dielectric material variations, via effects, ground plane effects, open versus shorted interconnects, and plating thickness variations.

When testing the test interconnect for the first time, a comparison between the test interconnect and the functional interconnect should be made. This comparison provides a correlation between the test and functional interconnects and should include the average, minimum, and maximum impedance values of a statistically significant sample size. This comparison is done to ensure that if the test interconnect does not accurately emulate the electromagnetic characteristics of the functional interconnect that it is intended to represent, then the at least there is a known correlation between the behavior of the test and functional interconnects.

The number of signal planes that require impedance control will vary with each functional board design. It is recommended that there be at least one test transmission line for each impedance controlled signal layer.

4.7.2 Test Interconnect Placement The ability to correlate impedance values derived from measurements taken of test interconnects to impedance values on functional interconnects is directly related to the proximity of the test interconnect to the functional interconnect. The closer the test and functional interconnects, the more likely the material properties and transmission line geometries will be the same. The placement of test interconnects on the board or panel should be analyzed for each board design and be based on the impedance tolerance and practicality of the layout. When deciding on the best test interconnect placement, consider the following placement priorities:

a. Inside the functional area of board
b. At the edge of the board but outside the functional circuit area
c. Outside of the board area and at the center or edge of the panel.

If coupons are placed in all the locations listed above, a comparison between a statistically significant sample set taken from each location over time can yield data that will relax placement requirements without reducing confidence in test results.

4.7.3 Test Interconnect Geometry The test interconnects should use the same line width, conductor thickness, and be located in the same dielectric environment (permittivity and thickness) as the functional interconnects being compared. Spacing between conductor pairs on differential test interconnects should also match that of the functional interconnects. If edge coupons are used and previous studies have shown that conductors at the edge of the panel etch differently from those in functional panel areas, then a compensation factor may be needed to adjust the impedance measurement for this difference.

4.7.3.1 Test Interconnect Length The length of the test interconnect required to determine its characteristic impedance is dependent on the resolution of the test equipment. Test interconnects should nominally be 15 cm [6 in] long. Longer test interconnects occupy more board or panel area. Moreover, the effect of conductor and dielectric losses in long interconnects may cause errors in the calculated impedance values. For short interconnects, the rise time of the TDR system may be too slow to allow existence of the constant-valued regions in the TDR waveform (see Section 9) that are necessary in computing characteristic impedance.

4.7.3.2 Transmission Line Termination Transmission lines are best utilized for test if they are terminated at both ends by a plated-through hole (PTH). Having one PTH termination, instead of two, reduces the size of the test interconnect area in the situation when more than one signal plane is to be tested (see 4.7.5). If two PTH terminations are provided, then either end of the transmission line may be contacted with the TDR probe. Additionally, for the dual PTH termination design, DC resistance/capacitance measurements could be taken on test interconnects, thereby providing an additional diagnostic tool in the event of an out-of-specification condition.

4.7.3.3 Contact Land The contact land should comprise a PTH and contact pad (see Figure 4-7). The PTH should be of consistent dimensions to ensure repeatability and reliability of the tests for the given measurement equipment. For example, different hole sizes and land pitches may each behave different electrically and this difference may affect the results of the measurement. Ideally, hole and pad size should be the same as those of functional interconnects but a practical issue of operator ability to hand probe should be considered. The nominal hole diameter is 0.9 mm [0.036 in] and surface land is 1.5 mm [0.060 in]. Reference contact lands should be square to aid in visual identification.

4.7.3.4 Contact Land Pitch The center-to-center distance between the signal and reference lands of the test

interconnect should be consistent to simplify probing requirements and ensure measurement repeatability and reproducibility.

4.7.3.4.1 Single-Signal Conductor Transmission Line The single-signal conductor transmission line is also known as the single-ended and asymmetrical structure (see Figure 4-8). The probing area should consist of one contact land (see 4.7.3.4.2) each for the signal line and reference/ground plane/line of the test interconnect. A contact pitch that is consistently used allows the use of one type of probe and this ensures more repeatable probing of the test interconnects.

4.7.3.4.2 Differential Transmission Line This structure is also known as the symmetrical or balanced structure. The probing area is best designed for testing if it contains four contact lands, one contact land for each of the two signal conductors in the differential pair and two contact lands connected to the reference plane(s) (see Figure 4-8). The use of two reference lands minimizes probe ground loop inductance and the associated ringing in the TDR waveform.

4.7.3.5 Orientation If possible, the contact land orientation (placement of the contact land of the signal line relative to the contact land of the reference plane, both of the same test interconnect) should be the same for all test interconnects to reduce operator fatigue due to probe rotation requirements. Consistency with orientation will also reduce test cost and time and cost of automatic measurement systems.

4.7.4 Test Interconnect Routing

a. The test interconnects should only be routed over/under contiguous ground/voltage planes. Care should be taken to ensure that test interconnects do not extend into PTH clearance areas. Special care should also be taken when using split planes.

b. The test interconnects should be kept at least six times the width of the signal conductor or 2.5 mm [0.100 in], whichever is greater, from any PTHs and any other interconnect on the same plane. All conductive material (such as, copper nomenclature, copper thieving, etc.) should be kept at least 2.5 mm [0.100 in] from each test interconnect.

c. Where possible test interconnects should be straight.

4.7.5 Nomenclature Labeling of the test interconnect contact lands on at least one surface layer is important for operator identification during manual probing operations. The label should minimally contain information about which signal layer the test interconnect is modeling (for example, L1, S3, etc.). If one signal plane is expected to contain more than one impedance level, than the contact lands should be additionally labeled with the expected impedance value (for example, L1/55, L1/28, as shown in Figure 4-9). Labeling of the contact land for differential

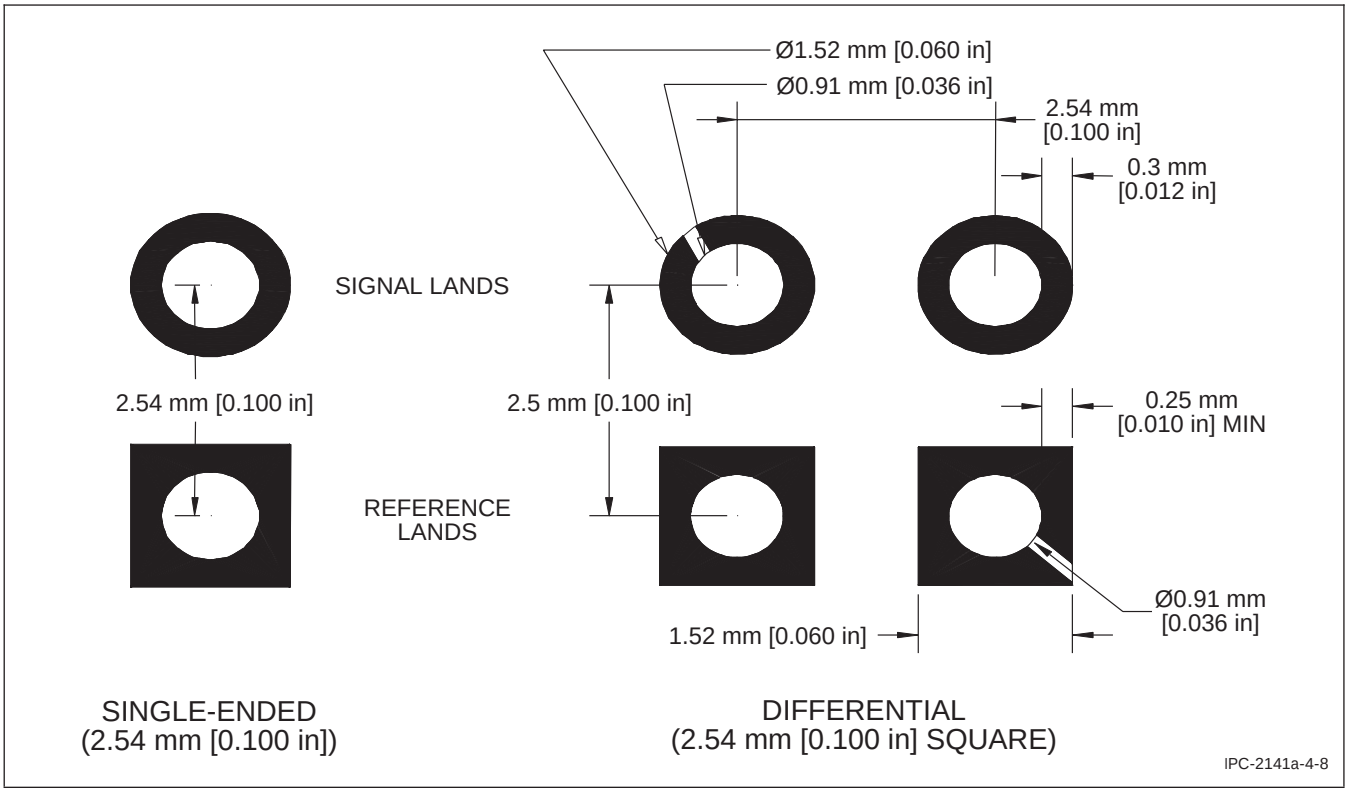

Figure 4-8 Impedance test interconnect contact pad geometry and drilled hole size. All dimensions are reference.

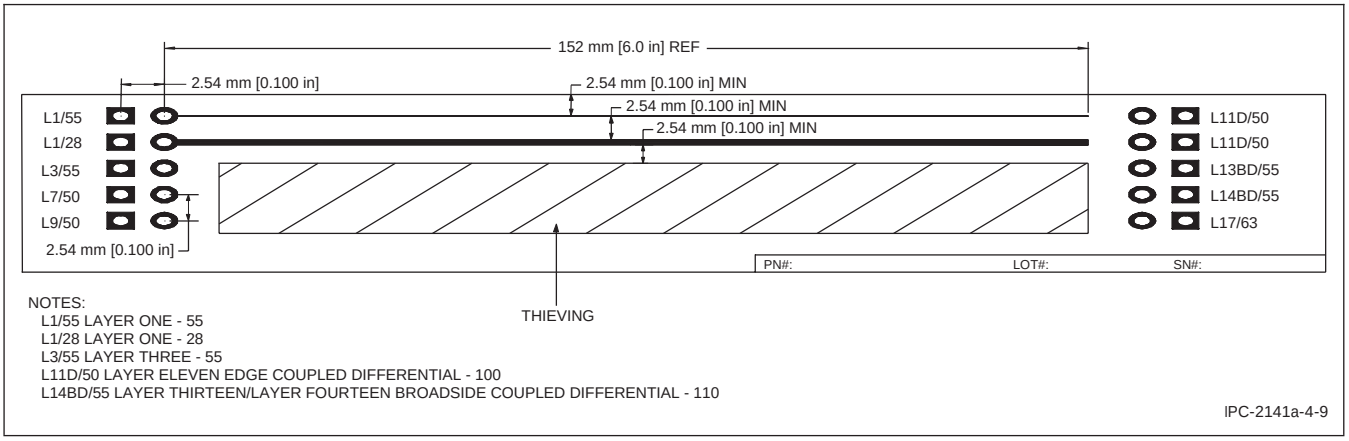

Figure 4-9 Impedance coupon design. All dimensions are reference.

traces should clearly indicate the matched pair. Nomenclature should preferably be etched in copper and be spaced a minimum of at least six times the width of the signal conductor (of the test interconnect) or 2.5 mm [0.100 in], whichever is greater, from the test interconnect area. Where practical, both terminations of the test interconnect should be marked.

4.7.6 Additional Guidelines for Testing Panel Coupons Test interconnects may be contained within one or more panel coupons. It is recommended that there be at least one coupon per board on the panel as long as it does not adversely affect panel utilization. With this configuration, the following additional design guidelines listed in this section apply. More than one coupon may be necessary on a board to ensure uniformity. Also, more test interconnects may be required than can fit inside one test coupon. In that case, more than one test coupon will be necessary.

4.7.6.1 Reference and Ground Planes All reference planes existing in the coupon are to be connected together within the coupon area and be independent of those planes in functional circuit area.

4.7.6.2 Surface Condition The panel test coupons shall have the same surface plating and use the same solder mask requirements as the functional circuit board.

4.7.6.3 Thieving Differences in circuit density between the inside of a panel coupon and the functional area may produce surface plating differences. In order to compensate for these differences, thieving (the use of nonterminated copper structures, such as planes, pads, and/or traces adjacent to test lines) may be used. Ensure all thieving structures are kept at least six times the width of the signal conductor (of the test interconnect) or 2.5 mm [0.100 in], whichever is greater, from each test interconnect.

4.7.6.4 Serialization Coupons can be provided with an area for the marking of part number, lot/date code, and serial number.

4.8 Decoupling/Capacitor Guidelines Decoupling is discussed in the IPC-2251.

4.8.1 Decoupling Capacitance Decoupling capacitors provide current to devices on the board when the power supply cannot respond quickly enough. High-speed switching devices may require a combination of several low to high frequency capacitors to meet their current requirements (see 3.4.12). A single capacitance value or capacitor type typically cannot provide the broadband current requirements of high-speed switching devices.

4.8.1.1 Transient Capacitance Consideration The transient capacitance is used to provide the charge required to drive the signal line of the transmission line during the high-speed switching transient. The switching transient typically contains the highest speed content of the signal but requires the least amount of current. In very high-speed devices, it may be necessary to build the decoupling capacitance into the package to minimize the lead inductance between the capacitance and the device. If that is not possible, the transient capacitance must be located as close as possible to the device. If sufficient energy is not available to drive the transmission line during the switching transient, the signal transition will be degraded.

4.8.1.2 Line Charging Capacitance Line charging capacitance provides current to the devices for charging the signal line of the transmission line after the device has been switched. This charging current must be maintained until the signal on the transmission line has reached its quiescent state. If insufficient current is provided to the device, the signal transition will be degraded.

Two types of line charging capacitance are required: one for capacitive lines and one for transmission lines. Capacitive line charging requires a relatively slower charging rate than a transmission line, but must provide more current. A transmission line requires a slower but typically longer pulse, than the capacitive line, to keep the line charged until all of the reflections subside.

4.8.1.3 Low Frequency (Bulk) Capacitance Low frequency capacitance is often termed bulk capacitance. This capacitance is used to recharge power planes and higher frequency charging capacitors and to provide switching current to lower frequency requirements.

4.8.2 Capacitor Model Capacitors with shorter leads provide current faster because their lead inductance is much smaller. In high-speed designs, changing the decoupling capacitors from leaded to leadless SMT capacitors can dramatically increase the circuit performance.

4.8.3 Decoupling/Capacitor Design Rules The following is a list of considerations for design of decoupling and capacitors.

a. Provide a capacitor network for the board comprised by a parallel arrangement of high and low frequency capacitances. An electrolytic capacitor with high storage capacity is typically used for the low speed requirements and a ceramic capacitor for high frequency requirements.
b. Provide local decoupling capacitors at each device. Larger devices with higher current demands may require more than one capacitor, such as clock drivers and line drivers.
c. Use wider conductors for power and ground connections to reduce high frequency coupling. For decoupling SMT devices, connect the device to the capacitor with wide conductors.
d. Use short or wide connections to power and ground pins to reduce inductive effects of the connection.
e. For power and ground, use large surface area conductive planes in which multiple via connections are used to contact devices on the board. This reduces the inductive effects of narrow reference planes and too few vias.
f. Distribute decoupling proportionally on the board to supply the current required by the devices.
g. For optimum performance, connect capacitor terminals and device leads directly to power planes.
h. The capacitance between the power and ground planes may also be used to provide decoupling. This type of decoupling will typically be used in high-speed boards.

4.9 EMI Considerations in Design Layout

4.9.1 Reasons for Considering EMI in Design Layout The requirements for EMI are generally dictated by regulatory agencies. Accordingly, a product must meet the requirements for radiated and conducted emissions, and /or radiated and conducted susceptibility limits before that product may be marketed or sold in that country. Some of those regulatory agency requirements are FCC Class A/B, EN 55022 Class A/B, VCCI Class 1/2, MIL-STD-461D, etc. Other reasons for considering EMI in a layout include proper operation when the board is placed adjacent to other boards in a card rack, electrically noisy environments, etc. Care must be exercised that EMI layouts do not conflict with safety regulatory agency requirements (high ground leakage currents from capacitors). The active components on a PCB generate EMI, and this EMI can generally be controlled to acceptable levels through source suppression practices in the layout. System level EMI layout (casework for EMI containment, interface cable partitioning, etc.) is beyond the scope of this document.

Many of the EMI layout practices described below are inter-related and all of them should be considered.

4.9.2 Pulse Transition Rates and Times To provide products with higher speed performance, clock and data rates must increase. To provide faster clock and data rates, the transition times (rise and/or fall times) of the clock and data pulses need to be shorter to accommodate the required logic set-up and hold timing for proper logic operation. As mentioned in Section 3.4.5, the highest frequency components in the spectrum of a digital pulse are related to the transition times (rise time or fall time) of the pulse. With some output structures, the rise and fall times are equal. Generally, however, one of these times is faster than the other, and both are modified by the length of the signal path, loading, and driver technology.

As transition times on active devices decrease, the requirement for attention to EMI layout practices increases. EMI layout practices may include controlling component placement, signal line termination, signal line routing, plane partitioning, crosstalk management, power decoupling, and shielding. When considering EMI layout, transition rates are the primary concern.

4.9.3 Suggested EMI Layout Practices The following sections suggest ways in which EMI layouts may be included in a product.

4.9.3.1 Controlling Component Placement Controlling the physical placement of the component is necessary to partition fast transition rate generators (that is, high-speed devices, such as clock drivers) away from the board edge. A good practice is to place given logic families together as a functional group. Place cable interface drivers near their associated I/O connector. Avoid mixing logic families in the same plane partition (TTL with ECL or TTL with GTL). Plan ahead for short routes, a rough placement diagram may indicate where small schematic changes (gate or pin swapping) will dramatically improve the layout. Clock oscillators and clock distribution (clock trees) should be placed close together to preserve the transition rate of the pulse and confine EMI energy.

4.9.3.2 Signal Line Termination A properly terminated signal line emits less EMI and is less susceptible to EMI. Care should be exercised so that all signal lines on which the propagating pulse has a fast transition rate (almost all signal lines are in this category) are properly terminated into their respective impedance. A nonterminated line will generate a reflection, which if not controlled, radiates, couples to adjacent traces, contaminates plane partitions, and couples to interface or power cables that exit the product enclosure and cause EMI test or susceptibility failures.

It is best to insure that the I/O Interface cabling impedance matches the driver impedance and that the receiver is properly terminated. Cable shields should be properly terminated to contain EMI emissions.

4.9.3.3 Signal Line Routing Proper routing of signal lines is very important. As a trace is routed, the designer must realize that the signal line will reference one or two reference planes. These planes may be power or ground planes and provide the return current path for the signal line. The planes become part of the impedance for the trace and concentration of the return current needs to be considered. Large address or data busses generate greater current density in the return planes than do random control traces. It should be noted that, when routed voltages are used, they also have return current paths. Signal lines should not reference different voltage planes or routed voltage traces than the driver, for example, 5 V signal lines should not reference a -2 V, -5.2 V, -12 V, or a +12 V routed voltage trace or plane. Transition noise or power supply noise from the other voltage may cause problems.

Routing of signal lines for clocks and fast transition rate signals should be between reference planes (such as in striplines) to provide EMI shielding and to control noise coupling to them. Extra line spacing from these lines to other signal lines should be used to prevent coupling between these lines. Routing clocks on outside layers (microstrips) for long distances should be avoided. General guidelines identified elsewhere in this document should be used to avoid stubs and other signal integrity effects which may cause EMI levels to increase.

Routing signal lines across voids in partitions should be avoided if possible because an alternate return current path will result which, depending on the trace length, may cause EMI problems. Routing of traces under sensitive circuitry like op-amps, PLLs and loop filter components, synthesizer chips, video clock generators, radio frequency (RF) devices, etc., should be avoided.

Avoid routing lines for fast transition rate signals near the PCB edge as it may be difficult to provide a return path near the PCB route border. As a rule of thumb, the reference planes for the signal line should extend 1.5 to 2 times the width of the signal line on either side of the signal line to provide an adequate return current reference. This rule may need to be adjusted to accommodate larger voltage swings or faster transition times.

Lines that provide power to active devices should be as short as possible and as wide as possible (within assembly soldering guidelines) to insure a low inductance (impedance) source for the device.

4.9.3.4 Plane Partitioning It is often necessary to partition the power or ground planes to manage voltage and ground distribution. Copper planes may be partitioned (split into more than one section) to provide TTL and ECL voltages or grounds, etc. Other plane partitions that may be considered are partitioning GTL from TTL (to keep the lower level GTL signals in a quiet area), TTL from ECL (for logic family isolation), TTL from analog (to keep high-speed TTL pulses away from op-amp high impedance sensitive circuitry), TTL from video (to prevent excessive noise on the video signal), etc.

Partitions of unlike planes should not overlap each other. For example, a TTL ground plane partition on one layer should not be placed above or below an ECL voltage plane partition on an adjacent layer. If not, this will cause coupling between planes that may cause EMI and signal integrity problems.

It is best to keep plane inductance as low as possible to insure the current demands can be met with low voltage drops to all devices. Decoupling will help with instantaneous current demands.

4.9.3.5 Crosstalk Management Crosstalk occurs when signal lines are placed in close enough proximity to each other that a signal on one line couples onto an adjacent line. The magnitude of crosstalk is based on the fastest transition rate of the pulse, the impedances of the lines (field coupling to the nearest plane), loading, and the length of the coupling. Crosstalk problems can be difficult to locate and are best solved by avoiding them in the layout. It is best to identify the signal lines that have the faster transition rates (clocks, strobes, etc.) and plan for extra spacing between them and all other lines. Routing high-speed signal lines on outside layers should be avoided because crosstalk increases on an outside layer due to the existence of only one reference plane for field containment.

Crosstalk can occur between signal lines and the I/O Interface lines that exit the enclosure, and this coupling may cause EMI limit failures or EMI susceptibility problems.

4.9.3.6 Power Decoupling All digital packages should have high frequency decoupling capacitors to insure that there is sufficient energy for high-speed drivers (see 3.4.1.2). The number of high frequency decoupling capacitors required is dependent on power and ground pin distribution, drive requirements, predicted noise environment,

and board space limitations. Consult the manufacturer or data books for the decoupling requirements for each device. Without high frequency decoupling, many of the switching currents will remain on the planes or power /ground line (if they are long) and cause EMI and functional problems.

High frequency decoupling capacitors should be placed as close to the power and ground pins as possible. Placing high frequency decoupling capacitors directly under the power and ground pins of the device but on the opposite side of the PCB works best.

Bulk low frequency decoupling capacitors store energy for charging the high frequency decoupling capacitors and provide reduced plane inductance for the PCB.

Bulk low frequency decoupling and high frequency decoupling should be provided close to the power input connector for all voltages. This provides clean power for the PCB and reduces any EMI that could couple to the power cabling.

Clock oscillators, clock drivers, PLL power and grounds, some I/O drivers, on-card power inverters, etc., should have a pi filter power source. The pi filter is usually constructed of a high frequency decoupling capacitor and low frequency bulk decoupling capacitor on the power side of a ferrite bead (for isolation), and a high frequency decoupling capacitor(s) (for transition and quiescent current demands) on device side of the side of the ferrite bead. Be sure the ferrite bead will handle the current without saturation. Ferrite bead impedance decreases with increased current.

4.9.3.7 Shielding Shielding, like partitioning, reduces radiated emissions and susceptibility of the product. Local shielding can provide both isolation from the emission of another circuit and prevent interference from other circuitry. A shield may be a metal fence, via fence, metal cover, guard bands around sensitive signal lines, chassis ground layers on the outsides of the PCB, etc.

RF circuitry is typically shielded by metal covers because many of the signal lines may be surface microstrips. Surface microstrip may radiate or have noise coupled into them, thus causing circuit performance problems.

Guard bands are ground lines that surround a signal line to provide isolation from other signal lines on the same layer or adjacent layers. The guard band is typically wide and grounded by vias periodically to keep it at ground potential. If guard bands are used, the guard band should be placed the proper distance from the signal line to preserve the transition rate of the propagating pulse (too close a placement will slow the transition rate). A guard band, if not kept at ground potential at the frequency of interest, may electromagnetically couple to adjacent traces. Sometimes it is better to use wider spacing between signal lines than to use a guard band.

A chassis ground on the outside layers of a PCB, if properly grounded to the chassis, provides EMI containment. A good connection to the chassis is essential and you may want to place a power or ground layer directly below the chassis ground layer for signal isolation. This may or may not be a good option with RF boards depending on the grounding arrangements of the system.

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5 DESIGN FOR MANUFACTURING

5.1 Process Rules in CAD The predominate tool used in the design of high speed, high frequency circuits, is computer-aided design (CAD) system. The CAD system can be used to specify conductor width, conductor spacing, and plating thieves (small isolated squares that allow uniform plating across the panel), all of which can be contained within a CAD data base. During the design stages, the widths of conductors in a net are specified to ensure that the transmission lines in the nets have either the correct characteristic impedance (Z_0) or capacitance (C_0) values.

Routing software allows the designer to control PCB conductor spacing and lengths (in both net nodes and for entire net lengths), to specify matched net lengths and minimum net lengths using concurrent orthogonal and diagonal routing and other rules driven routing specifics. Conductor separation in all axes is specified to ensure that nets have proper spacing relative to other nets for minimum noise and crosstalk.

5.2 Design Complexity and Correlation to Cost The design of high speed logic boards can be very simple, such as in microwave stripline or microstrip structures, or it can be very complex, as in a high performance, multilayer circuit board. Material selection and the degree of design complexity will impact the cost.

The following are some of the cost drivers for controlled impedance/controlled capacitance boards:

a. Smaller impedance/capacitance tolerance ranges than typical manufacturing processes will allow. The tolerance range for controlled impedance manufacturing processes is normally around ± 10%.

b. Specifying parameters that cause suppliers to control both physical and electrical measurements, such as specifying both the thickness of the dielectric layers and Z_0 for that layer.

c. Insisting on multiple Z_0 and/or C_0 values for the same layer. This will result in increased scrap because one Z_0 and/or C_0 value may be within an acceptable range while another value may be outside of that range. In most cases, the supplier will need to sort through the fabricated boards select those board that meet this criteria. Consequently, yield will be decreased.

d. Not allowing the supplier to make adjustments that better fits within their process capabilities, such as adjusting conductor width, dielectric thickness, or laminate choice.

6 DATA DESCRIPTION

Data should include the construction details on a layer by layer basis as well as the design data from the CAD system. Combined, the complete detail of the board fabrication should include the nominal values as well as the tolerances. Physical parameters as well as material properties should be included in the description.

6.1 Details of Construction The values and tolerances of the following design, material, and performance parameters should be included in the data:

a. Conductor width (for each line width and Z_0 requirement on that layer).

b. Conductor Z_0 or C_0 (for each line width and Z_0 requirement on that layer).

c. Conductor thickness.

d. Material type (including laminate, copper and surface finish).

e. Relative permittivity.

f. Dielectric thickness.

g. Solder mask type and thickness.

h. Layer diagram.

6.1.1 Controlled Construction When design and material parameters are specified, they control the construction of the board. The values and tolerances of the following design and material parameters should be provided (for each layer if applicable):

a. Dielectric thickness.

b. Finished copper thickness.

c. Material type.

d. Relative permittivity.

e. Solder mask type and thickness.

f. Conductor width and spacing.

g. Layer diagram including overall thickness.

By specifying these parameters, the board construction and the performance is controlled by normal construction parameters and their resultant tolerances. Conformance is verified by cross sectional analysis of the manufactured panel having the required physical dimensions, and not by measurements of the electrical properties of patterned structures (such as transmission lines) on the board. Controlled Z_0 values or C_0 values are not the criteria for acceptance.

6.1.2 Controlled Performance - Controlled Capacitance or Controlled Impedance Controlled Z_0 or C_0 is another method for defining board construction. In this case, the design and material parameters are referenced (nominal) and the values and tolerances of performance parameters are measured. The performance parameters are:

a. Controlled impedance in ohms or controlled capacitance in pf.

b. Propagation delay in picoseconds.

c. Layer diagram including overall thickness.

6.2 Isolation of Data by Net Class (Noise, Timing, Capacitance, and Impedance) Identification of nets by class or logical net names in either the net list or the CAD/CAM data base can allow specific conductors to be treated separately from the other conductors. As an example, two conductors, one that is specified as a ''noise susceptible'' conductor and another as a ''noise generating'' conductor, may have special physical spacing rules applied. Nets used for a particular class of logic, ECL for example, could be isolated to a certain signal layer. Controlled impedance conductors should be assigned a unique conductor code

(plotted width or aperture) so that they are treated separately from other conductors.

Different CAD systems and their routers should code or tag nets to accomplish routing and layer isolation strategies. By utilizing the features of the CAD system, high speed circuit design can be enhanced to meet design requirements.

6.3 Electrical Performance In addition to meeting the predicted performance criteria, printed wiring board designs must be manufacturable. Performance tradeoffs versus cost tradeoffs factor into the choice for optimum system design. Yields at manufacture are even greater contributors to cost than the obvious costs of raw materials and fabrication. For this reason, designers should be familiar with the materials available, their properties, capabilities, and tolerances, and have a good understanding of the process capabilities and tolerances that impact the performance and manufacturing yield of their boards.

The development of a close working relationship with the engineering design group and board fabricator is of benefit to avoid prototype iterations that are costly and time consuming. Designing ''based on previous experience'' is certainly valid, but may be limited and not take full advantage of advances in both materials and fabrication. The development of a relationship with in-house materials and manufacturing groups or outside industry sources is advisable.

Electrical performance parameters should be established so that the appropriate measurements can be performed. For example, ε_r varies with frequency, therefore, the measured values of ε_r should reflect the operating frequency range of the circuit or the rise time of the devices used in the circuit. Critical clock lines should have a length constraint consistent with skew requirements. Transmission line Z_0 values should match the input impedance of the devices (chip set) and the Z_0 of I/O lines should match that of the connector/cable system. Noise levels should also be within the noise margins of the devices.

7 MATERIALS

7.1 Resin Systems The resin systems used for circuit board laminates are classified into two basic categories: thermosetting and thermoplastic. Thermosetting resins are cross-linked matrices of smaller, polymeric units that once cured do not remelt. The polar nature of thermosetting materials generally causes them to have a higher relative permittivity, loss tangent (dissipation factor), and moisture absorption than the thermoplastic materials. The cross-linked structure of the thermosets generally provides better dimensional and thermal expansion characteristics than the thermoplastics. Moisture absorption becomes an issue because the relative permittivity of water is high (approximately 75) compared to that of these resin systems. Relatively small changes in environmental humidity may drastically impact circuit performance (because of a change in the capacitance of the printed wiring board transmission line) and, thus, require strict environmental controls. Furthermore, the relative permittivity and loss tangent of each unique resin system is dependent on temperature and operating frequency.

7.2 Reinforcements Various reinforcements, supports, and/or fillers are incorporated into resin systems to enhance the physical and/or electrical properties of the composite laminate. A typical example is the incorporation of woven E-glass into a resin to enhance dimensional stability and reduce the X-Y coefficient of thermal expansion (CTE). Fillers may be added to modify the relative permittivity and/or to exclude resin and thereby reduce the overall CTE in X, Y, and Z dimensions.

7.3 Prepregs, Bonding Layers and Adhesives These are various thermosetting and thermoplastic materials that are used to form a multilayer board through a lamination process. Prepregs are woven glass supported resins in their B-stage, which is a partially cured state. They are used to create the dielectric spacing between layers and are cured or cross-linked during the lamination process. This is the typical method of producing multilayer boards. Other methods include the use of thermoplastic bonding layers that are fusion bonded to the other layers during lamination by reflowing the bonding layers at their melting point. In flexible board technology, thin unsupported thermoplastic bonding films and thermosetting adhesive films are used in lamination where the dielectric is already provided by the base material.

7.4 Frequency Dependence Figure 3-1 and Section 3.4.2 describe the effect of material properties on the characteristic impedance of transmission lines. As described in that section, the resin and the reinforcement and/or fillers used for the laminate are key to the relative permittivity of the laminated material. Knowing the value and tolerance of the relative permittivity of the material supplied by the laminator will help to predict the probability that a given design will perform within the desired specifications.

8 FABRICATION

A general understanding of the capabilities of board fabrication technologies and the realistic, achievable tolerances in manufacture is critical to the successful implementation of designs. Areas of particular interest are the effect of manufacturing processes on board and circuit design attributes (or variables). Knowing the fabrication techniques and tolerances from the start will help the designer predict the probability that a given design will perform within the desired specifications.

8.1 General Generally, printed boards are custom components and cannot be treated in the same manner as

commercially-off-the-shelf components. Similarly, the printed board fabrication process is unique for each fabricator. Any comments or advice given in this document must, therefore, be modified to suit individual circumstances. The following are considerations to be taken into account:

a. Relative permittivity (ε_r). Reinforced, supported, and filled materials are a composite of materials having different ε_r values. The ε_r value of the composite material (see 3.4.2) will exhibit variations unless the proportions of the contributing materials are strictly controlled. The ε_r of the nonreinforced materials should be invariant as these are generally uniform, isotropic materials.

b. Dielectric spacing (thickness). Changes in the resin content will impact both thickness and relative permittivity. Thickness uniformity among materials will vary with the technology and the level of process control employed by the laminate manufacturer. It is further impacted by choice of prepreg, bonding layers, film, and lamination conditions.

c. Prepreg. Cured prepreg thickness and ε_r after lamination may vary with pressing conditions. For calculation purposes, the designer should consider the ε_r and thickness of a prepreg after the lamination cycle and account for any differences in ε_r that may exist between the prepreg and other layers.

d. Conductor width and spacing. Conductor width and spacing will be impacted by artwork, imaging, copper foil thickness, etching, and plating.

e. Conductor geometry. Conductor geometry may be influenced by imaging technique, cleaning, etching, and plating, particularly on outer layers where undercut in thick foils with narrow lines will create trapezoidal cross-sections.

8.1.1 Data Electronic data is the preferred data format and is usually transmitted via modem or high speed internet connection. To enhance production the design rules employed during layout can be electronically compared to the relevant design rules in the host database library. Design rule check is a normal part of the preproduction engineering process. Each layer will be identified by a unique file identity number (see IPC-2511 and IPC-D-356).

8.1.2 Pattern Generation and Transfer The patterned structures (typically conductors) on a board are obtained through a process starting with the generation of the design or artwork, then transferring the design to the board, and finally forming a pattern onto the metal plane of the board. For guidance on artwork and design considerations, including compensating dimensions for process effects, see 8.4.1 and IPC-2252.

8.1.3 Machined Features Machined features include plated-thru holes, nonplated holes, slots, pockets, and relief cuts. Dimensioning and tolerancing of machined features are extremely important to each printed circuit board design. For guidance on machined features, see IPC-2252.

8.2 Preproduction Processes The salient preproduction processes are shown in Figure 8-1.

8.2.1 Artwork Verification See 8.1.1 and 8.1.2 and references cited therein.

8.2.2 Panelization This is the stage where PCB images are step and repeated and robber bars and test coupons, are added to the manufacturing panel. (Robber bars, also called plating thieves, are metal lines or patterns added to the panel to improve current plating uniformity across the panel.) Electronic data is manipulated for panelization and can be rotated and/or mirrored to assist copper plating current distribution and/or edge connections, for subsequent gold plating, to the panel boundary. During this stage, the orientation of the panel providing for its maximum usage and any preferential process requirements for reflow or assembly should be considered.

8.2.3 Tooling Tooling information is obtained from the electronic data. The tooling is specific to the fabricator and may include pinning locations and coupons that are located outside the finished board outline area.

8.2.4 Photoplotting The photographic film used in the photoplotter should be stabilized prior to use. Panelized electronic data is down loaded to a photoplotter, where the light sensitive film is exposed. (Panelized data contains all the information required to produce boards from the panel. This information includes repeats of a given board design and/or multiple board designs.) The exposed film is then developed. The systems used in photoplotting are usually automated. They use a magazine/cartridge film feeder in the plotter and the film is automatically transferred to an auto feed developer. Plotting and developing are normally carried out in a controlled clean room environment.

8.2.5 Artwork Inspection All artwork, or its electronic graphical representation, should be checked prior to use. It is the manufacturers' responsibility to ensure that the production phototools are suitable to attain the physical and electrical characteristics of the end product. The following list identifies some of the criteria/parameters to be checked:

a. All layers present and correctly oriented.

b. Each layer is uniquely identified.

c. Contrast between clear and opaque areas.

d. Registration/scale.

e. Geometry definition.

f. Inclusions/pin holes.

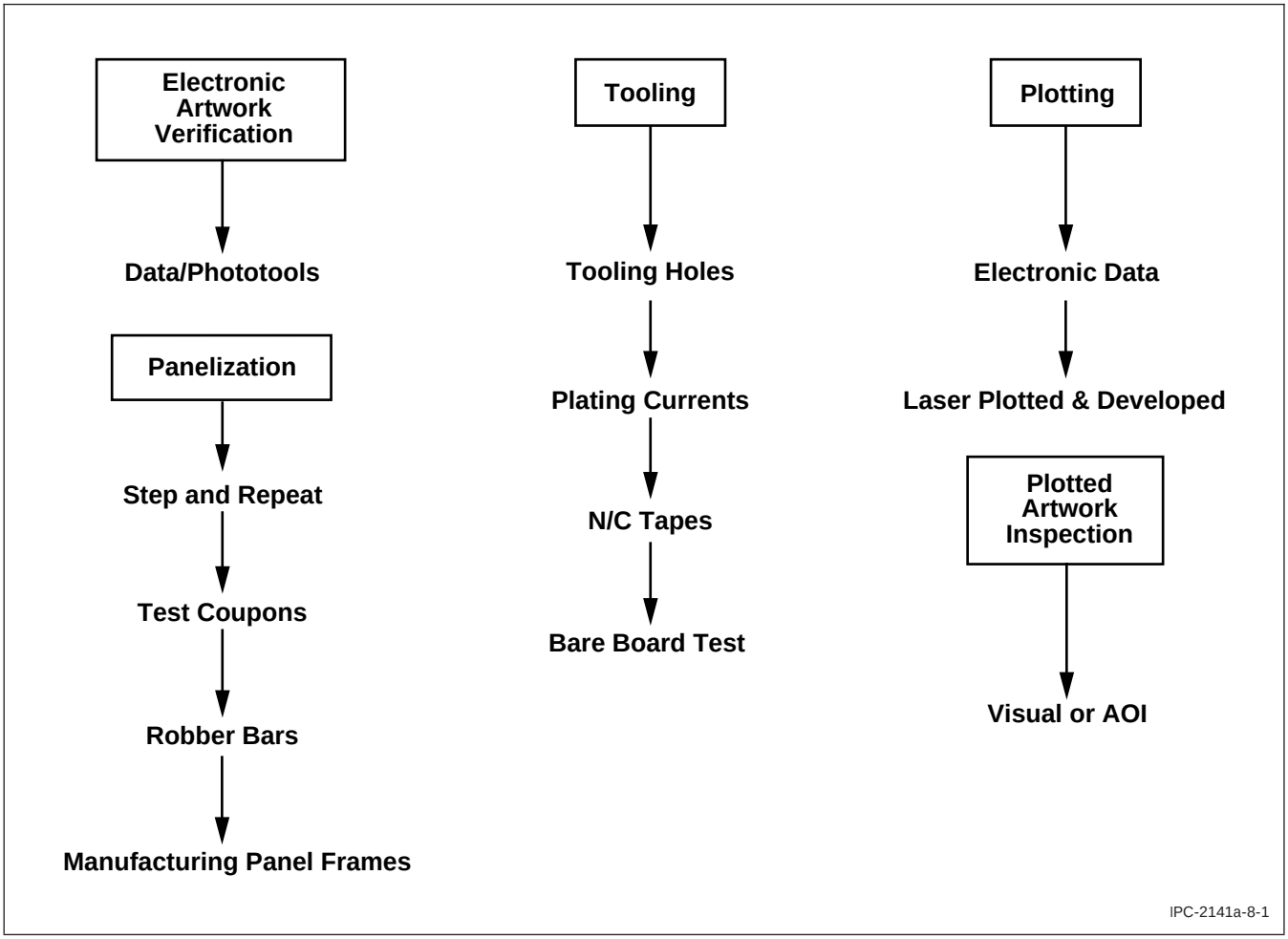

Figure 8-1 Flow Chart of Preproduction Processes.

g. Land/hole ratio.

h. Conductor/land clearances (gap width).

i. Annular clearances for ground and planes.

The above list is not exhaustive but should be used in conjunction with the relevant customer detail specification.

8.3 Production Processes An example flowchart of the processes employed in the fabrication of a typical multilayer printed board is shown in Figure 8-2. Critical processes for controlled impedance are boxed. Many variations of these processes can be employed to produce a variety of rigid multilayer configurations and surface finishes used today.

8.3.1 Processing Considerations The use of statistical process control (SPC) is advantageous in the fabrication of printed boards. Processes monitored by SPC methods can achieve minimum process variation and provide consistent characteristic impedance (Z_0) control. Process capability indices should be established for all critical processes. (See IPC-9191 for details.).

8.3.2 Laminate, Expose & Develop Cores Conductor edge profile is critical to characteristic impedance control. The presence of residual copper or photoresist should be avoided.

8.3.3 Innerlayer Etching The effects of over-etch or under-etch on Z_0 can be demonstrated by substituting changes in conductor width into one of the many formulae for calculating Z_0. The degree of over- and under-etch, the etch factors, and its effect on the fabricated board are the responsibility of the printed board fabricator but must be considered in the design so that the spacing between and width of the conductors is correct after etching.

8.3.4 Scan (AOI) Automated optical inspection (AOI) will detect imperfections in the conductor uniformity, widths, and clearances that may affect impedance performance. For example, depending on the designed line width, a 50 µm line width anomaly (nick or protrusion) could prove unacceptable in a circuit working at very high frequencies. The designer should include in his fabrication drawing any critical controlled line width or spacing

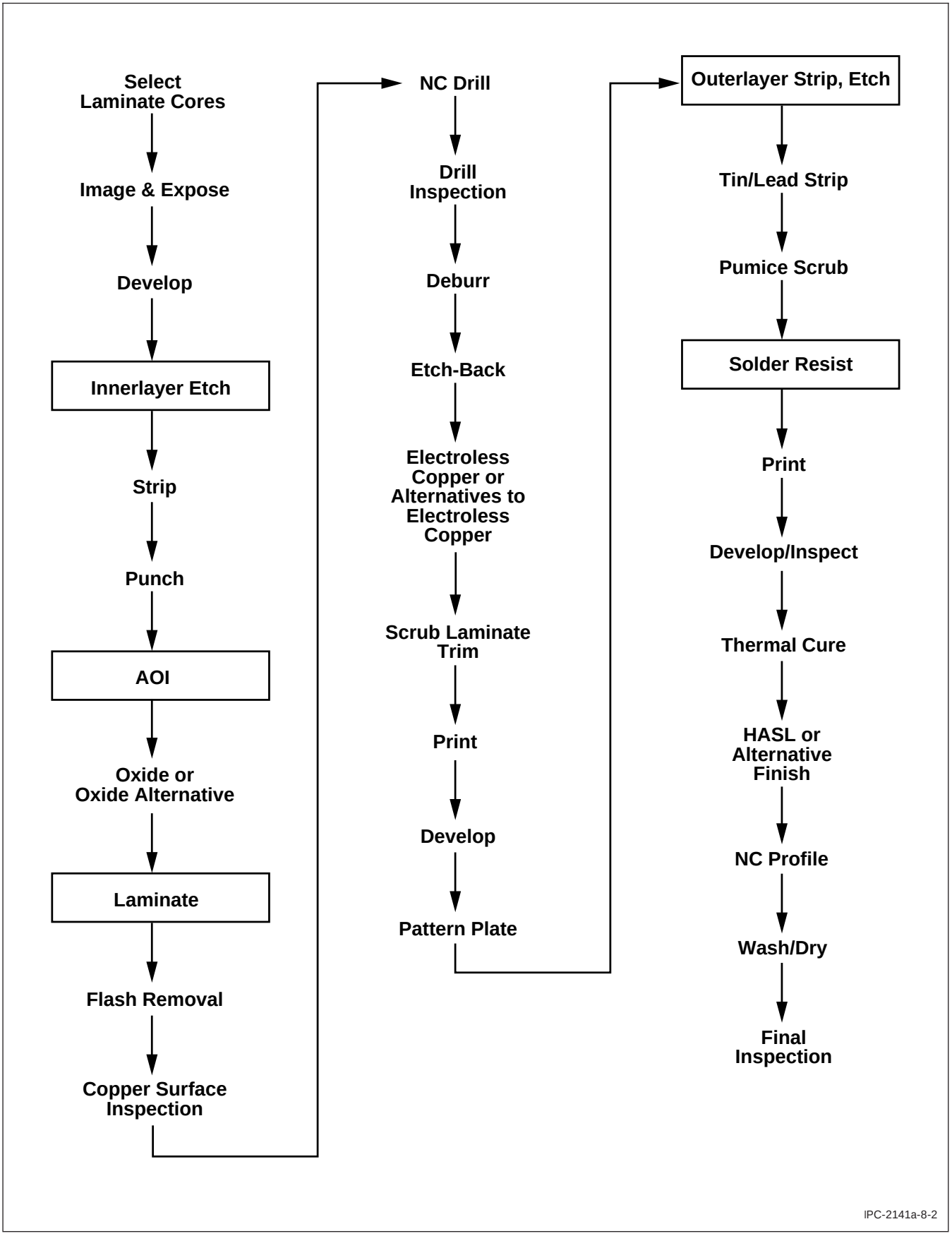

Figure 8-2 Production Process Flow Chart.

requirements above and beyond standard acceptance criteria contained in the applicable fabrication conformance specifications.

8.3.5 Lamination Final pressed thickness, retained resin content, and ε_r are influenced by prepreg panel resin flow characteristics. These characteristics can vary depending on choice of lamination equipment and techniques. The printed board fabricator must verify that the specified ε_r values and tolerances are achievable for their lamination process and that they can be maintained.

8.3.6 Numerically Controlled (NC) Equipment Most drilling, routing and milling equipment is typically controlled by numerical data supplied to the machine controller electronically. The format of the data is dictated by the capability of the controller and the equipment used. Most fabricators can use the data generated by computer-aided-design (CAD) software to drive their equipment directly or, if necessary, convert the CAD data to a format that can be accepted by their equipment. There are various data formats adopted by the electronics industry to facilitate transfer and use of data.

8.3.7 Hole Formation Drilled hole diameter and land hole ratio affect Z_0. Where high speed signals are routed via two or more impedance structures, the inherent capacitance of the via holes may affect the measured impedance. However, this effect is typically small and is dependent on the design of the transmission lines. To minimize this effect, via holes should feature as small a drill / pad diameter as possible. Ground to via hole clearance lands should be as large as possible. Although these are mainly design considerations, the capability of the fabricator to routinely achieve the design should be established.

8.3.8 Routing (NC Profile) Parts (printed wiring boards) are usually cut from the larger board or a panel by CNC routing. This approach requires at least two internal nonplated tooling holes. Tooling hole diameters must be large enough to permit precise registration of the panel to the router.

8.3.9 Dimensional Inspection Dimensions of machined features can be verified using a variety of inspection tools such as pin gages, calipers, micrometers, depth gages, etc. Almost all fabrication facilities have either automatic inspection equipment or manual equipment fitted with precision digital readout devices.

8.3.10 Electrolytic (Pattern) Plate Good design practice should result in a plating current density that is as uniform as possible across the board. When the design permits, the fabricator should be allowed to add plating thieves (robber bars) within the board area. Overplating, resulting in wider conductors, is more detrimental to controlled impedance than an increase in conductor thickness. The overplating-induced conductor widening becomes more of a problem as conductor widths and/or conductor-to-conductor spacings decrease. The use of panel plating or a combination of panel and pattern plating may prove a good compromise for some designs.

8.3.11 Outer Layer Strip, and/or Etch Stripping and etching processes are critical since any residue will destroy line definition.

8.3.12 Solder Mask Solder mask is only a consideration for surface microstrip structures. The material may be considered to be a boundary layer. The printed board fabricator should determine in advance the ε_r values for each solder mask type and thicknesses offered. These need to be taken into consideration when modeling for Z_0. Conformal coatings should also be considered in the same manner. The degree of cure of surface coatings will also have a minimal effect on overall performance.

8.4 Impact of Defects at High Frequencies It is common for limited numbers of defects in printed boards to be permitted where their distribution and prevalence is known. Examples include defects in conductors and spurious copper. Printed boards that feature controlled impedance must be virtually defect-free when judged against traditional criteria. The use of SPC is the only economic means of ensuring a consistently compliant product.

The influence of material properties upon impedance control should be understood (see 3.4.2, 3.4.4., 3.4.7), and the construction of the laminate specified.

8.4.1 Copper

8.4.1.1 General The nature and condition of the copper (plated, rolled, annealed) will affect Z_0 of a transmission line (see 3.4.7). At higher frequencies, the skin effect (see 3.4.7.1) affects signal propagation in the conductor. Surface roughness (see 3.4.7.3) is also a consideration for the propagation of high-speed signals.

8.4.1.2 Conductor Cross-Section The cross-section profile (such as, trapezoidal for inner layers, undercut for outer layers) of the conductor will influence the distribution of the electrical field around the conductor and currents in the conductor. Manufacturers attempt to provide as close to straight wall profiles as possible to control conductor line width. The conductor shape, by itself, typically has a small effect on Z_0.

8.4.1.3 Pin-Holes Defects commonly allowed or permitted in conventional printed wiring boards could create problems for controlled impedance boards. Although the

conductor shape, in most circumstances, has a small effect on Z_0, at very high frequencies these anomalies could cause undesirable electrical performance. The designer should include in his fabrication drawing any critical controlled line width, spacing, or conductor edge requirements above and beyond standard acceptance criteria contained in the applicable fabrication conformance specifications.

8.4.1.4 Spurious Copper Spurious copper affects the distribution of the electrical field along the conductor, the current distribution in the conductor, and the value of Z_0 near the location of the spurious copper.

8.4.1.5 Copper Thickness Copper foils with a nominal thickness greater than 17 µm [670 µin] are consistently supplied thinner than the nominal thickness. This reduces costs for the material supplier, but should be taken into account by the printed board designer who may be using inaccurate values to compute Z_0 and current carrying capacity. Foils with nominal thickness of 17 µm or less are typically supplied with thicknesses closer to the nominal thickness. Variation in conductor thickness will modify Z_0 slightly.

8.4.1.6 Surface Preparations The smoother surfaces provided by low-profile copper foils have not been found to affect Z_0 requirements. Changing from existing foil treatment to those required for low-profile copper could reduce peel strengths. Consequently, the affect of any change in the foil used must be carefully considered.

8.4.2 Substrate

8.4.2.1 General The difference between localized and global defects and effects should be identified and corrective action taken.

8.4.2.2 Dielectric Constant (Relative Permittivity, ε_r) Relative permittivity of a material is dependent on a variety of parameters (see 3.4.2). For a composite material, ε_r is also strongly affected by the ε_r of all the constituent materials (see 3.4.2.1). When trying to ascertain the effect of ε_r on Z_0, equations specific to the transmission line structure (microstrip, strip line, etc.) must be used (see Section 4).

8.4.2.3 Loss Tangent The dielectric loss, tanδ, (see 3.4.4) of a substrate affects its use at high frequencies. Ceramic materials have a high ε_r and low tanδ, which makes them suitable for high-frequency, low loss applications. For low loss materials, tanδ typically does not have a large effect on the electrical characteristics of the transmission lines. At very high frequencies, however, tanδ could be a significant concern to the board designer because of increased dielectric losses (see 3.4.4).

8.4.2.4 Laminate Consistency Laminate suppliers will consistently press their products to the same standard. Any changes in glass styles or resin systems must be discussed beforehand with the printed board fabricator.

Relative permittivity (see 3.4.2) tolerance is usually within ± 10%. Material thickness tolerance is generally ± 10%, but the thickness repeatability can be held to much tighter tolerances if necessary. For more information on material specifications, see IPC-4101 and IPC-4103.

8.4.2.5 Prepreg Prepreg is the B-stage bond sheets used to ''glue'' or bond the multilayer boards together. Where prepreg is used, the etched copper conductors will become impressed into the prepreg during the lamination process, thus resulting in an effective thinning of the prepreg. This reduction in the thickness of prepreg in the laminate must be considered when calculating the conductor separation, and will depend upon:

a. Conductor width.

b. Copper thickness.

c. Resin content of prepregs.

d. Type of glass composition.

8.4.2.6 Inclusions Conductive inclusions in the laminate should be considered as spurious copper. Nonconductive inclusions will locally modify ε_r of the substrate, and their effect on the electrical performance of the board will depend on their location, size, and prevalence.

8.4.2.7 Voids This type of defect, in common with delamination and crazing, will also affect ε_r to a degree determined by location, size, and prevalence. Delamination should not be accepted.

8.4.2.8 Resin Flow and Content The properties of the resin will have an effect upon the performance of the printed board. Suppliers of substrate materials typically experience little difficulty in producing single ply glass cores. Tighter thickness control (< ± 10% of nominal thickness) than typical can be achieved, without compromising product quality, by using single plies that contain less resin in the structure. However, the higher glass-to-resin ratio causes the laminate to have a higher ε_r value, which may be undesirable for many applications.

8.5 Data Description

8.5.1 Type of CAD Data All data for controlled impedance designs is supplied in a digital format. The data can be provided in a variety of formats, but electronic data files with embedded apertures are preferred.

8.5.2 Customer Interface Designers should interface with the printed board fabricator from the start of a project and a ''design for manufacture'' philosophy should be

encouraged. Critical controlled impedance conductors must be identified. Agreements should be made defining parameters that can be varied, and the amount of variation that is tolerable. The designed PCB should target achievable design parameters that can be supported by fabrication suppliers based on anticipated production quantities.

9 TIME DOMAIN REFLECTOMETRY TESTING

9.1 Description of Time-Domain Reflectometry Time-domain reflectometry (TDR) is a method for measuring the change in electrical impedance along a conductive path, typically the signal path or line in a circuit. In TDR, this impedance change is manifested as a reflection in the pulse that was generated by the TDR unit and delivered to the signal line. Reflections in this propagating pulse occur when the pulse experiences an impedance discontinuity.

The TDR system contains a pulse generator and a sampler (see Figure 9-1). Typically, the pulse generator and sampler are contained within a common module, however, this is not necessary. For example, in certain circumstances a commercially-available TDR may not provide adequate accuracy when measuring the characteristic impedance of low impedance (<20 Ω) line (see 9.7). The TDR waveform is usually acquired using an equivalent-time sampling process. The pulse generated by the TDR contains two states, a low or base state followed by a high state. The first transition between these two states is fast and is the one observed in a TDR waveform. The second transition occurs much later than the first transition and is usually not observed in a TDR waveform.

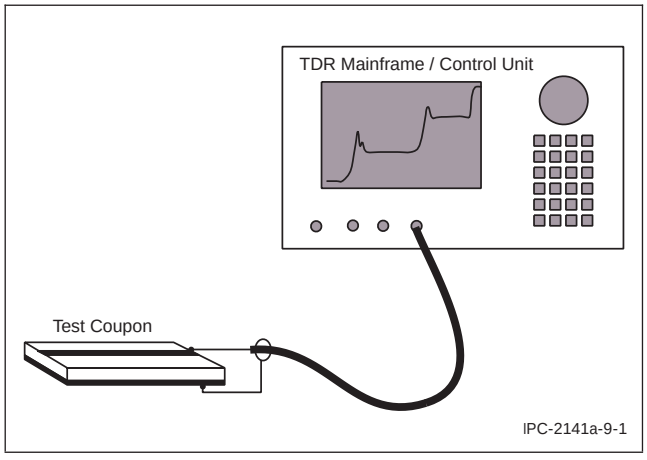

Figure 9-1 TDR System.

The pulse generated by the TDR unit, the incident pulse, is measured by the TDR sampler as it propagates away from TDR pulse generator and toward the output connector of the TDR (see Figure 9-2). The pulse is then launched onto the circuit connected to the TDR unit. If this pulse, now called the incident pulse, encounters an impedance discontinuity, a reflection will occur. The impedance discontinuity can occur at the TDR/circuit interface or anywhere

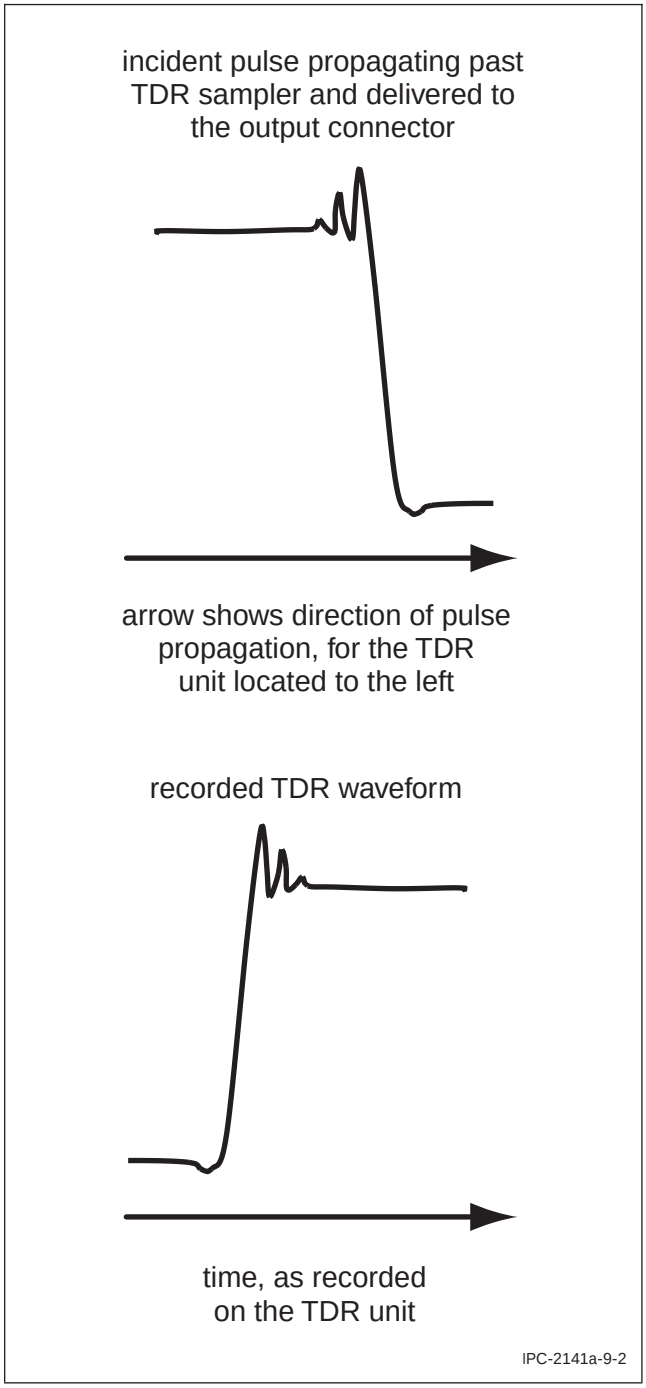

Figure 9-2 Pulse generated and sampled by TDR unit. This is the pulse that is launched onto the TDR output connector. The arrow in the figure on the left depicts the direction of propagation of the pulse, assuming the TDR unit is to the left. The arrow in the figure on the right shows the time axis of the recorded TDR waveform.

along the signal line. The pulse reflected from the impedance discontinuity will propagate away from the discontinuity and back toward the TDR (see Figure 9-3). This reflected pulse is also measured by the TDR sampler, consequently, the TDR waveform is the sum of the incident and reflected pulses, where the reflected pulses have been delayed relative to the incident pulse (see Figure 9-4). The

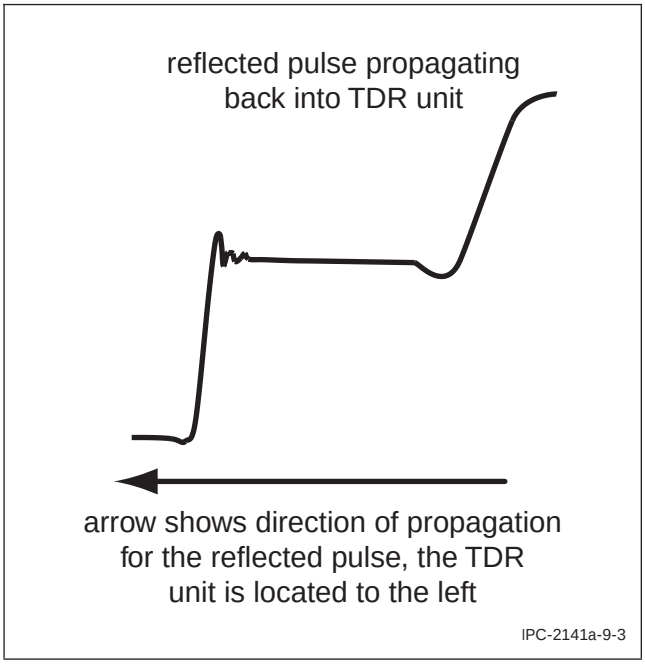

Figure 9-3 Pulse reflected from an impedance discontinuity and traveling back toward the TDR unit. The arrow indicates the direction of propagation (compare Figure 9-2, left side). The reflected pulse is positive in this example because the reflection coefficient at the impedance discontinuity is greater than 0.

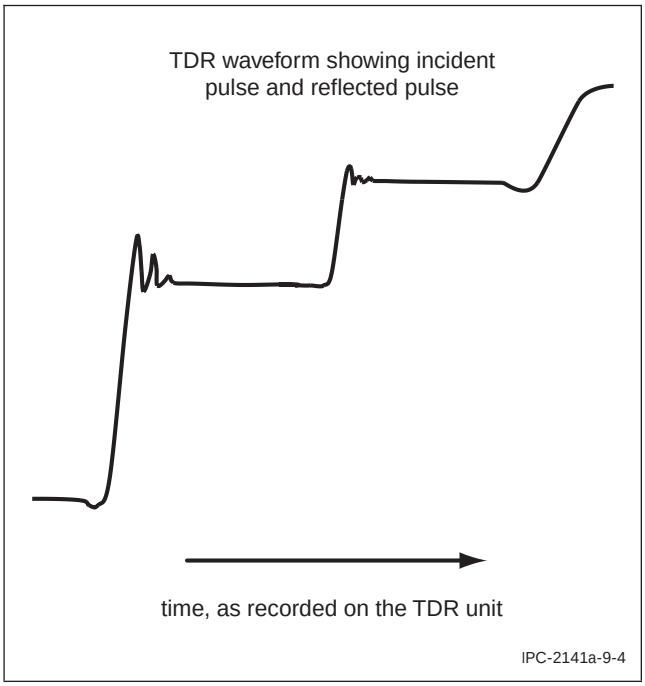

Figure 9-4 TDR waveform showing incident and reflected pulses. The reflected and incident pulses add. Because the incident pulse is a step, the reflected positive reflected pulse appears to sit on top of the high state of the incident pulse.

delay is caused by the length of circuit that the reflected pulse has traveled before it is measured. The spectral content of the reflected pulses is different from that of the incident pulse because of additional propagation losses and the fact that the reflection coefficient of the discontinuity is a function of frequency (contains both magnitude and phase information).

An impedance change may occur between two circuits even if the two circuits have nominally the same impedance. This impedance change is a result of geometric differences, albeit slight, between the two circuits. This occurs, for example, when connecting two 50 Ω lines together. It is for this reason that precision coaxial connectors are recommended when high accuracy measurements are required. Connectors and cables should be inspected at regular intervals to insure that they are not damaged and contributing to any changes in the TDR waveform.

The TDR waveform can be given as a voltage-vs-time (V(t)), reflection coefficient (ρ)-vs-time (ρ(t)), or as Z_0-vs-time waveform ($Z_0(t)$). The basic information is V(t), and from this ρ(t) and then $Z_0(t)$ can be obtained.

9.1.1 Mathematics of TDR Waveform The TDR waveform, as mentioned above, is the result of the addition of the incident pulse with the reflected pulse(s). If the pulse generated by the TDR unit is given by *p(t),* then the reflected pulse, *d(t),* is given by *p(t)*r(t),* where *r(t)* is the reflection function for the impedance discontinuity and the ''*'' indicates a convolution. This is also written as:

$$d(\tau) = \int_{t=0}^{\infty} p(t)r(\tau - t)dt \qquad [9\text{-}1]$$

where *p(t)*is zero for t < 0. Equation [9-1] is the convolution integral and is represented by the ''*.'' In the frequency domain, this convolution is the product of the spectrum of *p(t), P(f),* and the spectrum of *r(t), R(f)*:

$$D(f) = P(f)R^*(f) \qquad [9\text{-}2]$$

where *D(f)* is the spectrum of the reflected pulse and the asterisk denotes the complex conjugate.

The TDR signal, *w(t),* is the result of the cross-correlation of the sum of *p(t)* and *d(t)* with the impulse response of the sampler, *s(t),* which is given by:

$$w(\tau) = \int_{t=0}^{\infty} [p(t) + d(t)]s(\tau + t)dt \qquad [9\text{-}3]$$

where *d(t)*is zero for t < 0. In the frequency domain this becomes:

$$W(f) = [P(f)+D(f)]S(f) = P(f)[1+R^*(f)]S(f) \qquad [9\text{-}4]$$

The TDR waveform is the acquired TDR signal and is a discretized (in both time and amplitude) replica of the signal given in [9-3].

The transition duration (risetime, falltime) of a pulse is typically used to approximate the bandwidth of that pulse (see 3.4.5). The transition duration of the TDR signal is often approximated by a root-sum-of-squares rule (see 9.3.1.1.1) using the transition durations of the generated pulse, the reflection function, and the sampler effective step response.

9.2 Uses of TDR TDR is used to measure the reflection of pulse signals from impedance discontinuities in an electrical circuit. Typically, TDR is used to determine Z_0 of a transmission line by measuring the reflection caused by the impedance discontinuity at the TDR/transmission line interface. From this reflected signal and knowledge of the TDR impedance, Z_0 of the attached transmission line can be calculated. However, this is only the most common use of TDR. TDR can also be used, for example, to measure the input impedance of terminations and loads and to profile the impedance of a signal line in a populated or unpopulated circuit board. Furthermore, from the reflected signal, different characteristics or properties of a transmission line can be computed. For example, with additional information, the dielectric properties of the insulator of the printed wiring board can be computed. The TDR can also be used in quality control applications by observing changes in a group of TDR waveforms taken from samples (coupons) of a given lot or from different lots of a particular circuit design.

9.2.1 Computation of Characteristic Impedance The computation of Z_0 of the transmission line is based on the existence in the TDR waveform of nominally steady-state (constant) amplitude regions. These constant-valued regions correspond to the reflections of a step-like pulse from nominally uniform impedances. The amplitude of the constant-valued regions is dependent on Z_0 of the transmission line relative to the impedance of the TDR. The duration of the constant-valued region is dependent on the round trip propagation time of the pulse in that transmission line. Typically only one such region exists because of the limited duration of the waveform epoch and the length of the transmission line. This region is located between the transition caused by the reflection at the TDR/transmission line interface and that at the transmission line/termination interface, and is user defined. This region is shown in Figure 9-5 as the region between the lines labeled ''start of Z_0 computation region'' and ''end of Z_0 computation region.'' This portion should ideally have zero slope (that is, be flat, see 9.3.1.4), contain no aberrations (see 9.3.1.3), and have minimal noise (see 9.3.1.5). From this nominally flat region, Z_0 of the transmission line can be computed. The transmission line termination may be an open circuit.

9.2.1.1 Example of Z_0 Computation, Integrated Reference The following is an example of the computation of Z_0 assuming the voltage values corresponding to the reference and unknown impedances are contained within the same TDR waveform (see Figure 9-5). In this situation, the reference is obtained by having the reference impedance connected between the TDR unit and the transmission line under test. The Z_0 of the transmission line can be determined from:

$$Z_0 = \frac{1+\rho}{1-\rho} Z_{REF} = \frac{1+\frac{V_{refl}}{V_{in}}}{1-\frac{V_{refl}}{V_{in}}} Z_{REF} = \frac{V_{in}+V_{refl}}{V_{in}-V_{refl}} Z_{REF}$$

$$= \frac{(V_1 - V_0) + (V_2 - V_1)}{(V_1 = V_0) - (V_2 - V_1)} Z_{REF}$$

$$= \frac{V_2 - V_0}{2V_1 - V_0 - V_2} Z_{REF} \qquad [9\text{-}5]$$

where ρ is the reflection coefficient at the TDR/transmission line interface and Z_{REF} is the impedance of the TDR unit. Typical TDR systems provide ρ directly and it is not necessary for the user to compute ρ from the measured voltage levels.

9.2.1.2 Example of Z_0 Computation, Separated Reference The following is an example of the computation of Z_0 assuming the voltage values corresponding to the reference and unknown impedances are not contained within the same TDR waveform. In this measurement procedure, the transfer line that will connect the PCB transmission line to the TDR unit is first characterized relative to the reference (typically an air line). Next, the PCB transmission line is connected to the TDR using the transfer line and a waveform acquired. This results in two waveforms, both similar to that shown in Figure 9-5, from which Z_0 of the transmission line is calculated. Effectively, two equations such as shown below are obtained, one for the transfer line and one for the PCB transmission line. The transfer line equation is:

$$Z_L = \frac{V_{2,R} - V_{0,R}}{2V_{1,R} - V_{0,R} - V_{2,R}} Z_{REF} \qquad [9\text{-}6]$$

where Z_L is the characteristic impedance of the transfer line that will be used to connect the PCB transmission line to the TDR unit and the subscript ''R'' denotes that the measurements were taken with the reference line connecting the transfer line to the TDR unit. The Z_0 of the PCB transmission line is then computed from:

$$Z_0 = \frac{V_{2,TL} - V_{0,TL}}{2V_{1,TL} - V_{0,TL} - V_{2,TL}} Z_L$$

$$Z_0 = \frac{V_{2,TL} - V_{0,TL}}{2V_{1,TL} - V_{0,TL} - V_{2,TL}} \quad \frac{V_{2,R} - V_{0,R}}{2V_{1,R} - V_{0,R} - V_{2,R}} Z_{REF} \qquad [9\text{-}7]$$

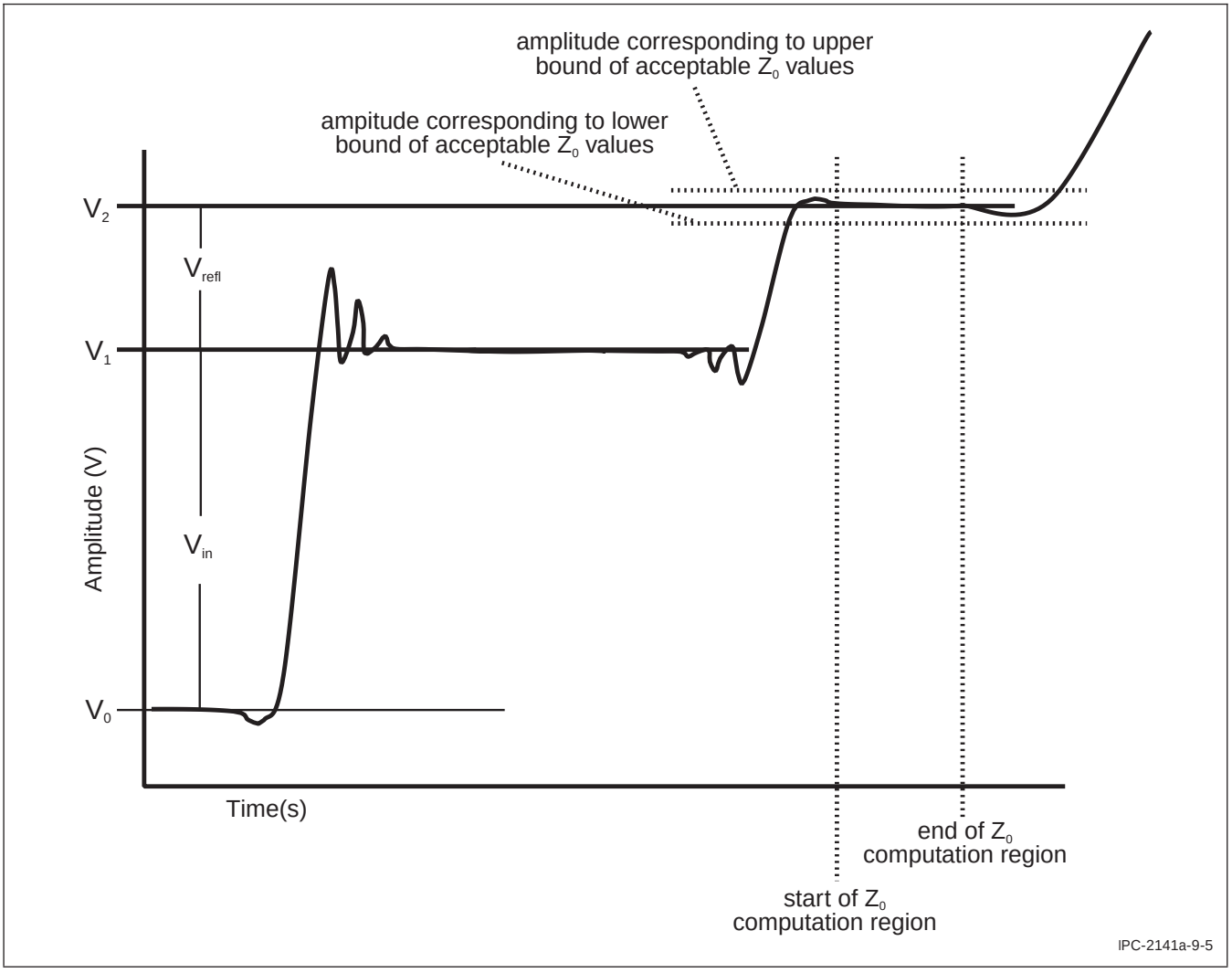

Figure 9-5 TDR waveform of a positive reflection.

where the subscript ''TL'' refers to the measurement with the PCB transmission line connected, via the transfer line, to the TDR unit.

9.2.2 Comparison to Other Methods Network analyzers, which use frequency domain methods, can also be used to obtain material or transmission line performance parameters. Most frequency domain methods use nominally monotonic signals (single-frequency sinusoids). When frequency domain information of a PCB is desired, for example the complex effective relative permittivity of a transmission line as a function of frequency, it would be best to use frequency domain tools. This is because the signal to noise as a function of frequency is much better for frequency-domain methods than it is for time-domain methods. However, to observe variations in impedance as a function of time (or equivalently, as a function of distance along the signal line) it is best to use time-domain methods, such as TDR. Although network analyzers can also provide this information by utilizing digital signal processing techniques, it may not be as accurate as TDR for this application because of the difficulty in representing the frequency content of a pulse and the necessary reconstruction of a pulse from magnitude and phase spectra. Moreover, network analyzers are much more expensive than TDR systems.

Other methods, such as micro-sectioning and capacitance testing of boards measure only some of the parameters influencing Z_0 of a transmission line. They also fail to show any variation in Z_0 of the transmission line over its length.

9.3 TDR System Description The TDR system contains, in addition to the TDR unit, all the necessary interface or interconnecting components that provide electrical connection between the TDR system and the device or circuit under test. This device under test is typically a transmission line.

9.3.1 System Components and Their Requirements

9.3.1.1 TDR Unit The TDR unit or head consists of a pulse generator and sampler integrated on the same circuit. The primary considerations for the TDR unit are step

response transition duration or bandwidth, pulse amplitude, pulse and sampler aberrations and settling, amplitude noise, and timebase errors.

9.3.1.1.1 Bandwidth and Transition Duration The bandwidth of the TDR unit, approximated by $0.35/t_r$ (see 3.4.5), should be much greater than that of the TDR waveform or the information desired, otherwise the effect of the TDR unit must be deconvolved from the measured TDR waveform. The effect of the response time, $t_{d,TDR}$, of the TDR unit ($t_{d,TDR}$ includes both pulser and sampler contributions) on the transition duration, $t_{d,meas}$, of the measured TDR waveform can be approximated using

$$t_{d,meas} = \sqrt{t_{d,TDR}^2 + t_{d,TL}^2} \qquad [9\text{-}8]$$

where $t_{d,TL}$ is transition duration of the effective step response of the transmission line. Ideally, $t_{d,meas}$ should be dominated by $t_{d,TL}$. If $t_{d,TDR}$ is one tenth or less of $t_{d,TL}$, then the effect of $t_{d,TDR}$ on $t_{d,meas}$ is negligible (less than 0.5 %) and $t_{d,meas}$ is primarily determined by $t_{d,TL}$. How much error is acceptable is dependent on the particular user requirements. This error can be approximated using a power series approximation of [9-8]:

$$t_{d,meas} = t_{d,TL}\sqrt{1+\Delta^2}$$

$$\approx t_{d,TL}\left(1+\frac{\Delta^2}{2}\right) \qquad [9\text{-}9]$$

where $t_{d,TDR} = \Delta t_{d,TL}$. For our previous example, $\Delta < 0.1$, so the effect of $t_{d,TDR}$ on $t_{d,meas}$ is less than 0.5%.

The transition duration of the TDR response function and the pulse propagation velocity in the transmission line are also important in determining the length of the transmission line that is to be tested. The length of this transmission line should be greater than the critical line length (see 3.4.9) otherwise reflections from the ends of the transmission line may affect the flatness of the region in the TDR waveform that will be used to compute Z_0 of the transmission line (see 9.2.1). Typically, the transition duration of a high-speed TDR system is around 15 ps.

9.3.1.1.2 Pulse Amplitude The generated pulse should have sufficient amplitude so that the reflected pulse can be easily observed above the noise (see 9.3.1.5). This means that the pulse amplitude must also be great enough to account for any losses in propagation in the transfer line or any other line connecting the TDR unit to the transmission line under test. Typically, the amplitude of pulses from TDR units is in the range from 0.2 V to 0.25 V.

9.3.1.1.3 Pulse and Sampler Aberrations Aberrations are the oscillations and spurious signal components caused by unwanted reflections and the electrical structure of the pulse generator and sampler. Most if not all pulse generators and samplers exhibit some type of aberrations in their outputs or responses, mostly after fast transients. If these aberrations are within the region of the TDR waveform that will be used to compute Z_0 of the transmission line (see 9.2.1), they can cause a bias and increased uncertainty in the computed Z_0 value. Aberrations may also be reduced or filtered by the frequency-dependent attenuation of cables.

9.3.1.1.4 Pulse and Sampler Settling Settling describes how well a pulse or response to a pulse achieves a steady-state value. As mentioned in 9.2.1, the Z_0 of the transmission line is computed from the voltage values of the steady-state regions of the TDR waveform. If these regions do not settle quickly to some nominal value but instead either drift up or down relative to the nominal value, an error in the calculated value of Z_0 will occur. This error is due to a bias in the voltage value or reflection coefficient value of the steady-state region, which in turn will cause a bias in the computed value of Z_0. Settling errors may be caused by, for example, frequency-dependent losses in the conductors (see 3.4.7.1, and is commonly called the ''skin effect'') and pulser and/or sampler circuit relaxation (resistor-inductor-capacitor, or RLC, response).

9.3.1.1.5 Amplitude Resolution, Gain, and Noise These effects, except for noise, are primarily sampler properties. Noise can come from the pulser, radiated electromagnetic interference, and the sampler circuit. Typically the noise can be averaged to a value less than 0.5 mV rms (root-mean-square). Since the typical TDR pulse has an amplitude > 0.2 V, this provides a peak signal to rms noise greater than 400:1.

The absolute gain of the sampler is not critical since TDR waveforms will be used in a ratiometric or comparative way. However, gain linearity is important. Typically, the gain linearity of high-speed samplers is one least significant bit (LSB). For a sampler using a 12 bit analog-to-digital converter (ADC) with a ± 2 V input, the gain linearity error will be less than 1 mV.

The amplitude resolution should be sufficient to provide the desired accuracy to compute Z_0 of the transmission line. One way to examine the effect of amplitude resolution and noise on the uncertainty, μ_{Z_0}, *in* Z_0 is to perform an uncertainty analysis. Using the equation from 9.2.1.1, μ_{Z_0} can be derived and is:

$$u_{Z_0} = \frac{2Z_{REF}}{(2V_1-V_0-V_2)^2}\sqrt{(V_2-V_1)^2\,u_{V_0}^2+(V_0-V_2)^2\,u_{V_1}^2+(V_1-V_0)^2\,u_{V_2}^2}$$

$$\sqrt{+\frac{1}{Z_{REF}^2}(V_2-V_0)^2(2V_1-V_0-V_2)^2\,u_{Z_{REF}}^2} \qquad [9\text{-}10]$$

The uncertainty in voltage levels will be primarily caused by noise, therefore, $\mu_{V_0} = \mu_{V_1} = \mu_{V_2} = \sigma_n$, where σ_n is the standard deviation of the noise. As an example, let $\mu_{Z_{REF}}$ = 0 Ω, V_0 = 0 V, V_1 = 0.25 V, V_2 = 0.3 V, (this corresponds to the reflection from a 75 Ω line, reflection coefficient = 0.2), and Z_{REF} = 50 Ω. For these values, $\mu_{Z_0} \approx 984\ \Omega/V\ \mu_V$. If the impedance tolerance is 10%, this tolerance can be related to uncertainties in voltage levels by:

$$\frac{u_{Z_0}}{Z_0} \approx \frac{984 u_v}{Z_{REF}} \frac{2V_1 - V_0 - V_2}{V_2 - V_0} \approx 13V u_v \leq 0.05 \qquad [9\text{-}11]$$

Therefore, μ_V must be less than about 0.004 V if the impedance is to be within about 10% of 75 Ω. The value 0.05 is used instead of 0.1 to accommodate extreme values, as will be shown in the next example. Let V_0 = 0.004 V, V_1 = 0.246 V, and V_2 = 0.304 V, which gives the largest value for V_{refl} and the smallest for V_{in}. These values give a reflection coefficient of approximately 0.24 and a Z_0 of 81.5 into a 50 Ω system, which is an 8.7% error in the target impedance of 75 Ω.

This example shows that the desired impedance tolerance is dependent on the target impedance relative to the reference impedance, signal noise, and the amplitude resolution of the measurement.

9.3.1.1.6 Timebase Settings and Errors The timebase should be set so that the sampling interval, δt, does not affect the measurement bandwidth. Based on the discussion in 9.3.1.1.1, this means that $\delta t < 0.1\ t_{d,TDR}$. If frequency domain analysis will be performed on the TDR waveform, then at least 10 samples should be contained within the transition of the pulse. Any fewer sample points may cause aliasing in the spectrum of the TDR waveforms. The spectrum may be necessary for computing certain transmission line characteristics.

Timebase errors (unequal sampling intervals, given by δt_i, i = 1, 2, ...*N*, where *N* is the number of samples in the TDR waveform) are not critical for steady-state characteristic impedance measurements and may not be an issue for propagation delay or impedance profiling measurements. The deviation of δt_i from δt is typically fairly small, $(\delta t - \delta t_i) < 0.1\delta t$ and, therefore, will not affect the accuracy of these TDR measurements. However, the circuitry used to provide the timebase is reset periodically and, at the instant the timebase is reset, the timebase error may be on the order of several picoseconds, that is, $\delta t_{reset} > m\delta t$, where *m* is an integer. These reset-based timebase errors may cause errors in impedance profiling and propagation delay measurements.

Timebase delay drift, for consistency, should be no more than 100 ps between any measurements. For propagation delay or impedance profiling it will be necessary to ensure that the delay drift is measured and taken into account.

9.3.1.1.7 Other Parameters

a. Offset drift will not affect pulse amplitude unless the drift occurs while the TDR waveform is acquired, which is not likely.

b. *Time Jitter* – Jitter effectively acts as a low-pass filter and, consequently, reduces system bandwidth. However, root-mean-square (rms) jitter is typically less than 2 ps (95% confidence interval) for commercially-available high-speed TDR systems. The effect of jitter on the measurement system response time or bandwidth can be calculated as described in 9.3.1.1.1.

9.3.2 Cables High quality (low insertion loss, low propagation loss) 50 Ω coaxial cables should be used to minimize reflections from the cable and to minimize the attenuation of the high frequency components of the incident and reflected pulses. The additional reflections caused by a poor cable connector may add spurious components to the region of the TDR waveform that will be used to compute transmission line parameters (see 9.2.1).

The cable has a step response with associated transition duration. The effect of the cable on the measurement system response time can be approximated by adding the square of the cable transition duration to that of the rest of the system components (similar to that shown in 9.3.1.1). High loss and/or long cables have longer transition durations than low loss and/or short cables, consequently high loss and/or long cables will reduce the effective bandwidth of the TDR system.

9.3.3 Connectors The connectors used should be precision quality or metrology quality connectors, have the same characteristic impedance of the TDR system, have the same form as the TDR connection (such as SMA, 3.5 mm [0.138 in], etc.), and have a bandwidth nominally greater than that of the desired information. Precision connectors have tighter geometric tolerances than that of regular connectors. This greater precision reduces the magnitude of reflections at the connector interfaces. Furthermore, some connectors, even connectors claimed to be high-bandwidth, contain ferromagnetic metals in their construction. These metals reduce the skin depth at any given frequency, and this has been observed to affect the settling behavior of electrical pulses. If this settling error is significant and it is not taken into account, it may cause errors in the analysis of a TDR waveform.

9.3.4 Probes The probes have the same requirements as the cables and connectors. In addition, the probe must be designed to provide a high-bandwidth electrical contact to the contact pads on the test structure (coupon). The probe must also be designed to efficiently launch the pulse onto the transmission line.

SMA connectors are commonly used to make probes. The SMA connector that is used should provide low-loss and

repeatable electrical connections to the test coupon. For a more consistent probe contact, a spring loaded coaxial probe may be used.

9.3.5 Test Fixtures Test fixtures are used to improve measurement repeatability. The fixture provides a way of holding both the probe and the coupon in a consistent manner and accurately registered to each other. To achieve this, the fixture should contain tooling holes to orient the printed wiring board or coupon relative to the probe and to support the printed wiring board so that the transmission line being tested is not contacting or in close proximity to any materials that could affect its propagation or impedance characteristics. The fixture ideally should contain a manual or computer-controlled positioner for placing the probe anywhere in a plane above and parallel to that of the coupon. The fixture should also have a vertically-moving spring-loaded mechanism for making reliable and repeatable contact between the probe and the coupon.

9.4 TDR Operation

9.4.1 Operating Procedures The operating procedures should be well documented and should include all cautionary statements regarding instrumentation damage and factors affecting measurement quality. The operating procedures should be tested to ensure that they accurately describe the actual waveform acquisition and data analysis processes. Operating procedures must be updated to reflect new equipment and changes in measurement protocols.

9.4.2 Test Considerations

9.4.2.1 Automation Use of software for automated instrument set-up and calibration is recommended. This usage ensures that the test system is correctly and consistently configured for testing. In addition, it can calibrate the system on every test, thereby minimizing the effects of instrument drift.

9.4.2.2 Standardization A standard test procedure for acquiring the TDR waveforms and methods for calculating the characteristic impedance from the TDR waveform should be agreed upon. The equations used in the computation of the Z_0 may be incorporated into the system software.

The region in the TDR waveform from which the Z_0 of the PCB transmission line is to be obtained (see 9.2.1) should be defined in the system set-up. This region should be chosen so as not to include the impedance variations normally seen at the probe/transmission line interface and the transmission line/termination interface. Typically, these excluded regions correspond to the ends of the transmission line and are each approximately 20% of the transmission line length.

The degree of standardization depends on the use of the TDR data. If the TDR data will be used primarily at one location for quality control, then almost any TDR system, transmission line, probe, and test fixture design and analysis method will do, as long as they are implemented consistently. On the other hand, if a comparison with other laboratories is the intent, then more standardization is required. The most repeatable and reproducible measurements will be those where the following are defined: TDR system general design, TDR system performance requirements, data acquisition and analysis procedures, transmission line design, probe design, and test fixture design.

9.4.2.3 Electrostatic Discharge (ESD) Protection TDR instrumentation is very sensitive to damage from ESD. Therefore, it is recommended that some form of ESD protection be used. Some TDR systems have internal limiting diodes to prevent ESD damage but higher performance systems usually require an external static isolation unit. Test procedure should include instructions for an operator using proper grounding techniques, such as wrist or heel ground straps.

9.4.2.4 Factors that can Affect Measurement Quality The following factors have been found to adversely affect the quality of TDR measurements on controlled impedance PCBs:

a. Incorrect set-up and calibration of instrumentation.
b. Different test methods and methods and equations of calculating Z_0.
c. Variation in the manual selection of the TDR region used to calculate Z_0.
d. Quality of impedance reference.
e. Poor or intermittent contact during testing.
f. Accidental reversal of signal and ground connections.
g. Contact of coupon with external material, including operator fingers.
h. Variations in manual probing technique.
i. Variations in ambient temperature and humidity.

9.4.3 Operator Requirements Many existing TDR systems are highly complicated and require highly skilled staff to correctly set up, calibrate, and perform measurements with them. In addition, test procedures are often long and complicated. This problem can be addressed by using specialized software for automatic instrument set up and calibration. Once a test set-up has been stored, all the operator need do is select that test and execute it. The software sets up the instrument, calibrates it, performs the test, and displays the result. A display of impedance versus time or distance along the signal line can be provided, including the mean, standard deviation, minimum and maximum impedance values. The PCB can be passed or failed according to

whether its impedance is within tolerance over the selected interval or distance (see 9.3.7). This approach requires minimal operator skill once the software is correctly installed.

The operator must understand the test equipment being used for the test as well as its calibration procedure. In the case of programmable test equipment, an understanding of the program used for measurement is desirable. Board construction and its relationship to controlled impedance is also desirable

9.4.4 Test Example, Unbalanced Transmission Line The following Figure 9-6 provides a schematic of how an unbalanced line is connected to the TDR unit for measurement.

9.4.5 Test Example, Balanced Transmission Line Balanced transmission lines, or differential impedance structures, and measurements are becoming more important because of their improved signal to noise ratio compared to single-ended lines. The main difference between differential and single-ended TDR is that differential structures require pulsing and sampling on two lines instead of one (see Figures 9-6 and 9-7).

Three methods exist for testing differential impedance, a true differential and two single-ended methods. In true differential TDR, two very closely matched pulses of opposite polarity are simultaneously transmitted down balanced conductors, one polarity pulse per conductor, and applied to two different conductors (signal lines) on the test coupon (see Figure 9-5). The reflections from these signal lines are monitored on a sampler, one sampler for each signal line. Valid differential measurements can also be achieved using single-ended TDR methods, where one pulse generator with two samplers or, alternatively, one pulse generator with one sampler is used. These two methods make individual measurements on each conductor and then mathematically combine the results to calculate the resulting differential impedance. Simultaneous connections are made to both conductors in these two methods despite the fact that either only one is receiving a pulse or only the reflection from one is being measured.

9.4.6 Pass/Fail Testing Pass/fail testing may be achieved by checking that the impedance is within a given tolerance of its nominal value over the selected region of the TDR waveform (see 9.2.1). The mean and standard deviation of measured impedance within the selected region should be recorded. An example is shown in Figure 9-5 where the horizontal lines labeled ''upper bound of acceptable Z_0 values'' and ''lower bound of acceptable Z_0 values'' are the tolerance limits within which the PCB transmission line impedance must fall to be acceptable. The tolerance limits are user specified.

9.4.7 Test Information The following list of information should be contained within a TDR test packet.

a. General information
   1. TDR (or sampler/generator) manufacturer, model number, serial number.
   2. Operator name.
   3. Date and time of test.
   4. Temperature, mean and standard deviation (if available).

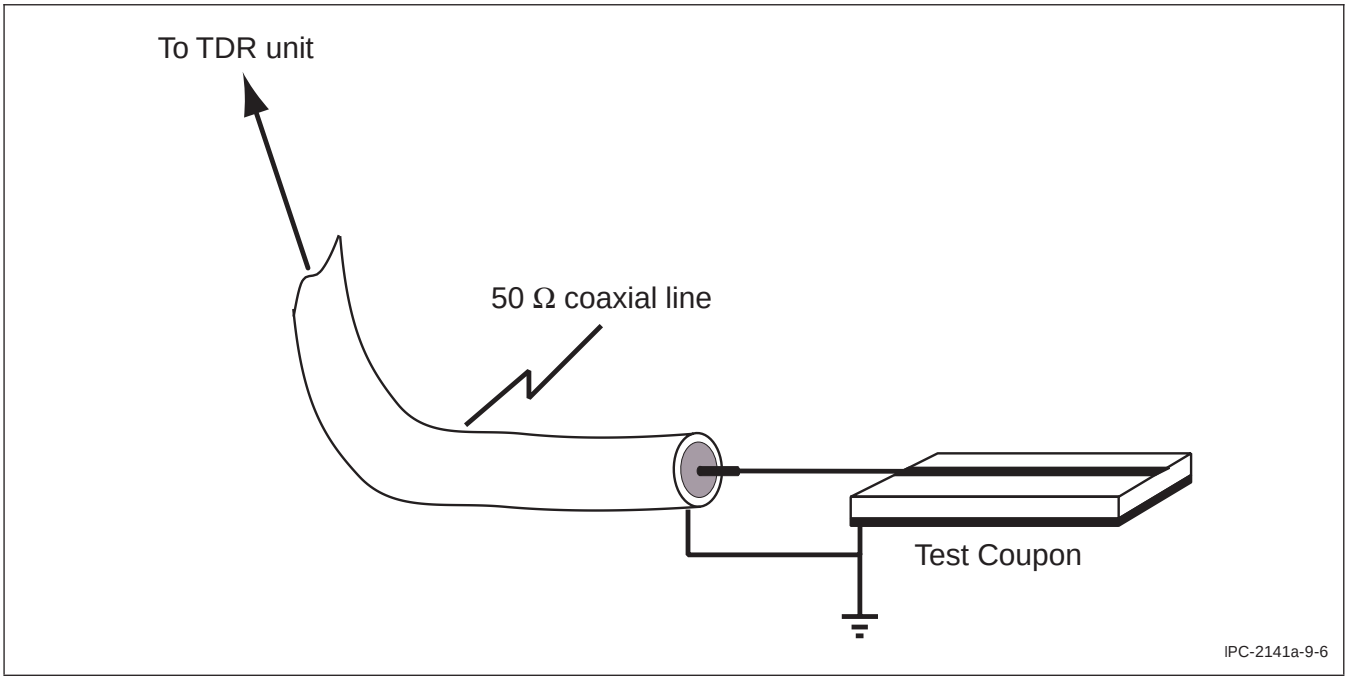

Figure 9-6 Depiction of coupon connection for unbalanced transmission line.

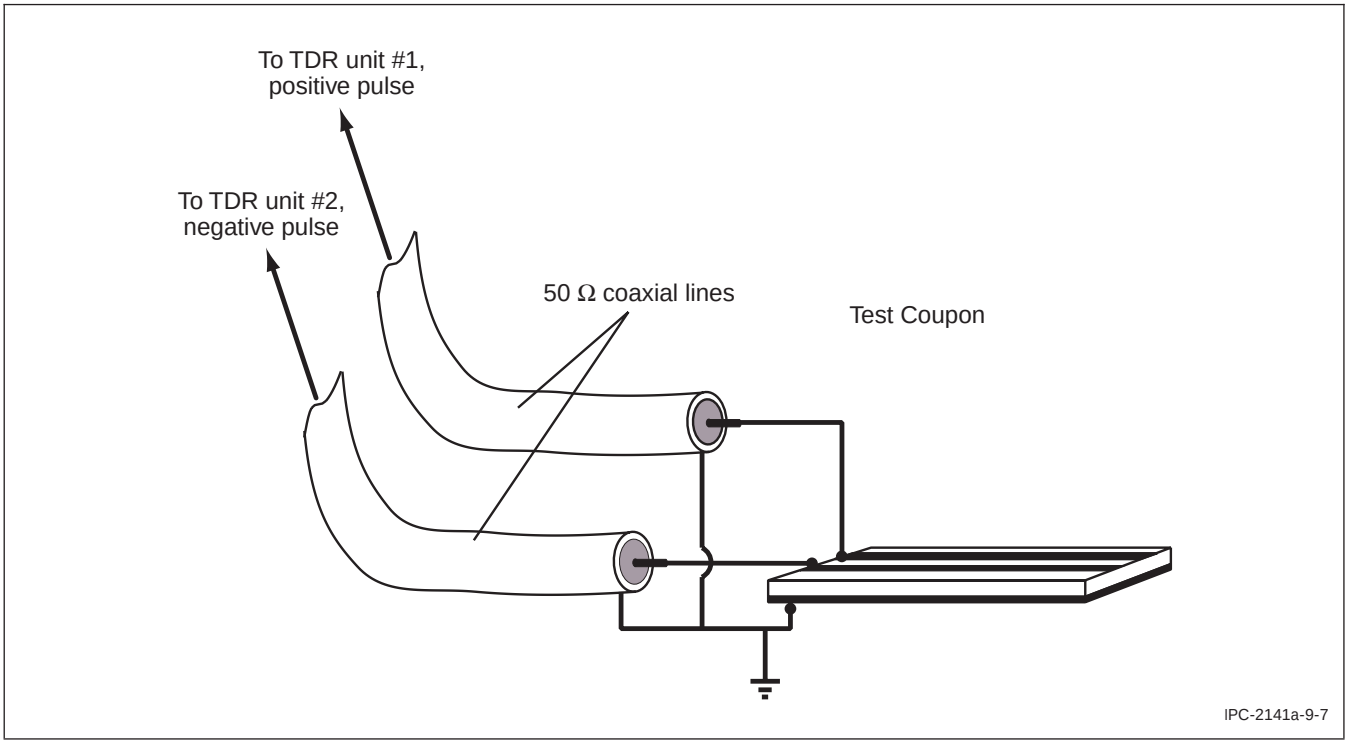

Figure 9-7 TDR testing of differential lines.

5. Relative humidity, mean and standard deviation (if available).
6. Calibration dates of instrumentation.
7. Test pattern name or description.

b. Vertical (amplitude) settings.
   1. Offset.
   2. Gain (typically in volts/division).

c. Horizontal (timebase) settings.
   1. Delay.
   2. Timebase setting (typically in time units/division).
   3. Record length (number of samples in a waveform).

d. Trigger (if externally triggered).
   1. Manufacturer, model number, serial number (if not pulse generator).
   2. Slope.
   3. Sensitivity.
   4. Repetition rate.

e. Other
   1. Filters.
   2. Bandwidth.
   3. Number of averages.

9.5 Test Structure A number of different controlled impedance structures may be used for testing. These structures may be divided into microstrip and stripline configurations and also into single ended and differential signal paths (see Section 4). The design of the transmission line should represent the properties being examined. For example, if the property is the impedance of the line, then the line should not contain tees, 90° bends, line width changes, or anything else that may affect the characteristic impedance of the line. Furthermore, the length of the line must be greater than the critical line length (see 3.4.9). However, if the property of interest is the reflection of a via, bend, etc., then these components must be included in the design of the test structure.

If it is not practical to test the functional transmission lines (that is, a transmission line interconnecting two or more devices), then it may be possible to incorporate additional nonfunctional transmission lines into the board that emulate the electromagnetic behavior of the functional lines. It is important that these nonfunctional lines emulate as closely as possible the electromagnetic behavior of the functional lines and also have suitable test points at each end.

Alternatively, additional transmission lines (test coupons) that are not integrated into the PCB may be used. These test coupons should also emulate as closely as possible the electromagnetic behavior of the functional lines on the PCB. One advantage of a test coupon is that it may be made to fit a standard test fixture and it is available for future testing or comparisons with other laboratories.

Coupons may either be process related or design related. The former will consist of conductors of the appropriate impedance on each controlled impedance layer. Design related coupons may incorporate other circuit features such

as 90° bends and via holes to assess the effect of these on the overall impedance.

9.5.1 Standard Test Coupon It is recommended that a standard design for test coupons be adopted. This design should define the geometries of the transmission lines and coupon, probe pattern, and fixturing holes. This information will allow development of custom fixturing to maximize measurement repeatability and reproducibility.

Testing coupons in a custom fixture that uses spring loaded coaxial probes is recommended to reduce errors in measurement.

9.6 TDR Calibration The TDR system should be calibrated regularly using appropriate calibration artifacts and a log of the calibration results maintained. The TDR should be calibrated by attaching the calibration artifact to the TDR and measuring the signal reflected from the TDR/artifact interface. The calibration procedure is performed similar to an ordinary TDR measurement except that in the analysis of the TDR waveform, the goal is compute the impedance of the TDR unit and not the impedance of the circuit connected to the TDR unit.

9.6.1 Calibration Artifacts High quality coaxial air lines provide the best impedance references. The characteristic impedance of the air line is computed from the geometry of the transmission line and the properties of the dielectric (air) using well known equations for the characteristic impedance of coaxial lines. The accuracy of the geometric measurements is good enough to provide an uncertainty (95% confidence level) in the computed impedance of a 50 Ω air line of ± 0.5 Ω. This characteristic impedance value, however, assumes ideal electrical conductors (that is, the conductivity of the metals is infinite). Consequently, the characteristic impedance of these air lines is not constant with frequency. These air lines should be checked periodically against national standards.

A well-characterized reference coupon with a number of conductors of known characteristic impedance may also be useful for comparison of different test systems and as a test for correct instrument operation.

Although high quality terminations are commercially available, they are not suitable as a broadband impedance reference. The primary reason is that the standing wave ratio (SWR) values of these terminations can range from 1.1 to 1.25 over the frequency range of interest. This SWR range corresponds to an impedance uncertainty in a 50 Ω system of approximately ± 5 Ω at an SWR of 1.1 to ± 12 Ω at an SWR of 1.25.

9.7 Alternative TDR Design As mentioned in 9.1, commercially-available TDR systems may not have adequate measurement accuracy to allow accurate determinations of Z_0 of low-Z_0 transmission lines. In this case, it will be necessary to separate the TDR sampler and pulse generator (see Figure 9-8). The electrical characteristics of the separated pulse generator and sampler will be the same as that described for the integrated system (see 9.3.1). The reference impedance for the measurements is inserted between the pulse generator and sampler. The test coupon is then attached to the open end of the reference line. Reflections will be observed just as in commercially-available TDR systems. The methods of computing the Z_0 of the test coupon transmission line will be the same as that described in 9.2.1.

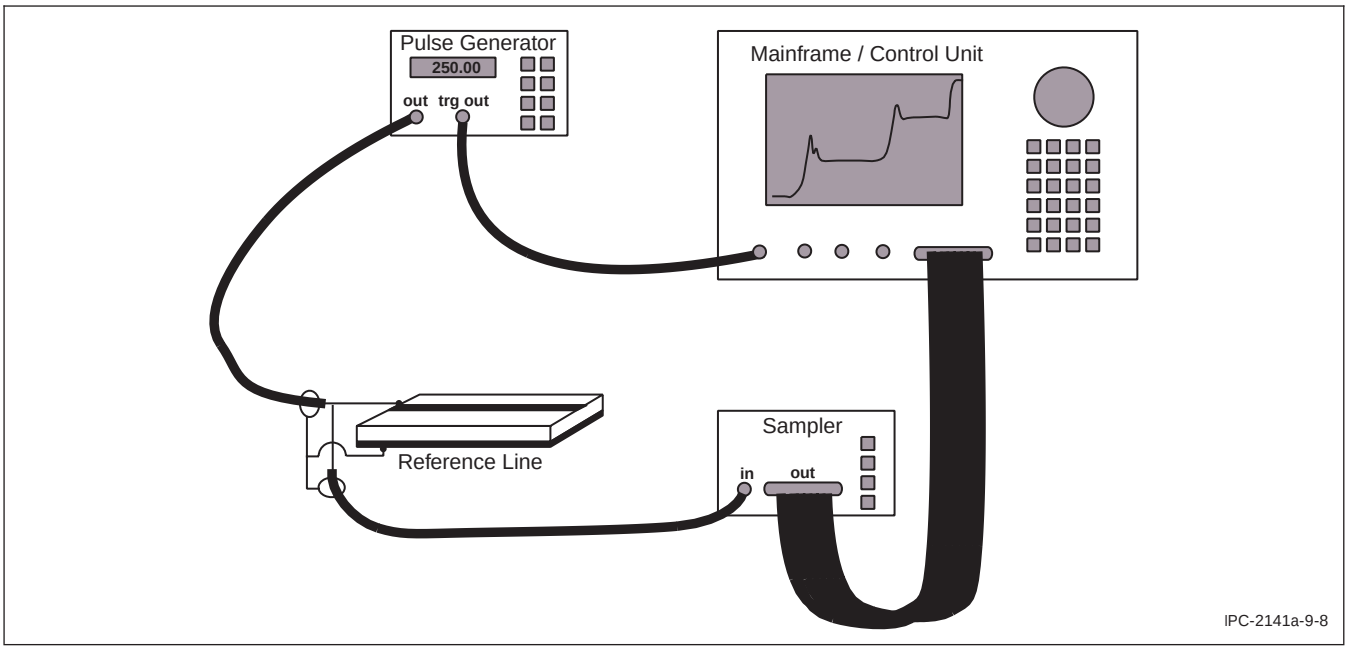

Figure 9-8 Sketch of layout of alternative TDR system.

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Document(s) to which this term applies: _____

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The referenced paragraph number has proven to be:

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