BTS–III(15)–11.16–1510 Reg. No. | | | | | | | | |

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B.Tech. Degree III Semester Examination November 2016

CS 15-1302 LOGIC DESIGN

(2015 Scheme)

Time : 3 Hours Maximum Marks : 60

PART A

(Answer *ALL* questions)

(10 × 2 = 20)

I. (a) Convert $(63.25)_{10}$ to Hexa decimal and octal.

(b) State De-Morgans theorem.

(c) Express the Boolean function $F = A + B'C$ as a sum of minterms.

(d) Differentiate between combinational and sequential circuits.

(e) Design a 4 × 16 decoder constructed two 3 × 8 decoder.

(f) Implement a full adder using ONE 3 input decoder and gates.

(g) Write short notes on triggering of flip flops.

(h) Write a short note on excitation tables.

(i) Draw the PLA block diagram and explain its features.

(j) Write the features of CMOS logic devices.

PART B

(4 × 10 = 40)

II. Simplify the following Boolean function into (i) sum-of-products form and (ii) product-of-sums form $F(A,B,C,D)=\Sigma(0,1,2,5,8,9,10)$.

OR

III. Prove the theorems of Boolean algebra by using postulates.

IV. Explain the design procedure of combinational circuit with an example that converts the BCD to Excess-3 code.

OR

V. Implement the following function using a multiplexer
$F(A,B,C,D)=\Sigma(1,3,4,11,12,13,14,15)$

VI Design a 4 bit ripple counter using JK flip flop.

OR

VII. Design and explain a 4 bit asynchronous up-down binary counter.

VIII. Write short notes on (i) Fan in and Fan out (ii) Propogation delay (iii) Noise margin.

OR

IX. Compare TTL and CMOS logic families.

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