BTS–III(R/S)–02-22-0003 Reg. No. | | | | | | | | |

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B.Tech. Degree III Semester Regular/Supplementary Examination February 2022

CS 19-202-0302 LOGIC DESIGN

(*2019 Scheme*)

Time: 3 Hours Maximum Marks: 60

PART A

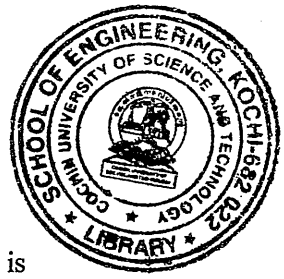
(Answer *ALL* questions)

(8 × 3 = 24)

I. (a) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction:

(i) X - Y and

(ii) Y - X by using 2's complements.



(b) Show that the dual of the exclusive-OR is equal to its complement.

(c) Design a 4 x 16 decoder using two 3 x 8 decoders.

(d) Design a 4 bit shift register with serial input and serial output.

(e) A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory for the following codes.

(i) 000011101010

(ii) 101110000110

(iii) 101111110100

(f) What are the basic differences between PROM, PLA and PAL?

(g) Define the following and provide the values of each for ECL and CMOS logic.

(i) Fan out

(ii) Propagation delay

(iii) Noise margin.

(h) Tabulate the truth table for an 8 * 4 ROM that implements the Boolean functions.

$A(x, y, z) = \Sigma(0, 3, 4, 6)$

$B(x, y, z) = \Sigma(0, 1, 4, 7)$

$C(x, y, z) = \Sigma(1, 5)$

$D(x, y, z) = \Sigma(0, 1, 3, 5, 7)$

PART B

(4 × 12 = 48)

II. (a) Simplify the following expression using the K-Map method by finding essential prime implicants. (6)

$F(A, B, C, D) = \Sigma(5, 6, 7, 12, 14, 15)$

$d(A, B, C, D) = \Sigma(3, 9, 11)$

(b) Implement the Boolean function $F = xy + x'y' + y'z$ (6)

(i) With OR and inverter gates only

(ii) With AND and inverter gates only

(iii) With NOR and inverter gates only.

OR

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III. (a) Simplify the following Boolean function into (6)

(i) sum-of-products form
(ii) product-of-sums forms.

$F(A, B, C, D) = \sum (0, 1, 2, 5, 8, 9, 10)$

(b) Simplify the following Boolean function using the Quine McCluskey method. (6)

$F(A, B, C, D) = \sum (2, 3, 4, 5, 6, 7, 9, 11, 12, 13)$

IV. (a) Implement the following four Boolean expressions with three half adders: (6)

$D = A \oplus B \oplus C$
$E = A'BC + AB'C$
$F = ABC' + (A' + B')C$
$G = ABC$

(b) Implement the following Boolean function with a multiplexer (6)

$F(A, B, C, D) = \sum (0, 2, 5, 8, 10, 14)$

OR

V. (a) What is Carry Propagation delay? Design a 4- bit binary parallel adder with look ahead carry generator. (6)

(b) Design a code converter that converts a decimal digit from 8,4,-2,-1 code to BCD. (6)

VI. (a) Design a synchronous counter using T flip-flops which counts the following repeated binary sequence: 0,1,2,4,6. Derive a suitable self-correcting method for invalid states. (6)

(b) Design a BCD ripple counter using JK flip-flops. (6)

OR

VII. (a) Draw the logic diagram of a four-bit binary ripple counter. Show that a BCD ripple counter can be constructed from this counter with asynchronous clear and a NAND gate. (6)

(b) Design a 4 bit ring counter. How does it differ from a Johnson counter ? (6)

VIII. (a) Design a PLA circuit to implement the functions (6)

$F1 = A'B + AC + A'BC$
$F2 = (AC + AB + BC)'$

(b) What is meant by address multiplexing? With a neat diagram, illustrate how address multiplexing is done for a 64K DRAM. (6)

OR

IX. (a) Draw circuit of an TTL NAND gate and explain the operation. (7)

(b) Compare the performances of CMOS and TTL logic. (5)

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