BTS-V(SS)-09-22-1082 Reg. No. | | | | | | | | |

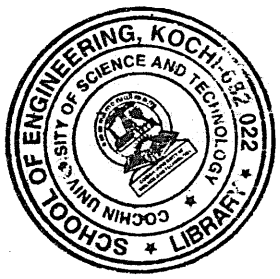
C

B.Tech. Degree V Semester Special Supplementary Examination September 2022

CS 19-202-0505 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

(2019 *Scheme*)

Time: 3 Hours Maximum Marks: 60



Course Outcomes

On successful completion of the course, the students will be able to:

CO1: Familiarize 32bit, 64bit and multi core architectures.
CO2: Compare the features of various microprocessors.
CO3: Learn the architecture and programming with 8O51 microcontroller.
CO4: Explain the basic architecture and features of PIC microcontrollers.
CO5: Develop microcontroller programs.
CO6: Familiarize basics of interfacing.

Bloom's Taxonomy Levels (BL): L1 – Remember, L2 – Understand, L3 – Apply, L4 –Analyze, L5 – Evaluate, L6 – Create

PO – Programme Outcome

PART A

(Answer *ALL* questions)

			(8 × 3 = 24)	Marks	BL	CO	PO
I.	(a)	Explain the real mode of operation of 80386 processor.		3	L2	1	1,2
	(b)	Compare 80386 and 80486 microprocessors.		3	L2	2	1,2
	(c)	Discuss on power reduction techniques in multicore architectures.		3	L1	1	1,2,4
	(d)	Explain Flat memory model and Segmented memory model.		3	L2	1	1,2,4
	(e)	Explain the different types of interrupts in 8051 microcontrollers.		3	L2	3	2
	(f)	Discuss on the pin configuration of 8051 microcontrollers.		3	L2	3	1,3
	(g)	Explain power up set mechanism of PIC16F84A.		3	L1	4	1,3
	(h)	Discuss on PIC16F84A ports.		3	L2	4	1,3

PART B

(4 × 12 = 48)

II.	(a)	Explain the register organization of 80386.	6	L2	1	1
	(b)	Explain how Super scalar architecture is effectively implemented in Intel Pentium microprocessor.	6	L1	1	1
		OR				
III.	(a)	Explain the segmentation and paging mechanism of 80386.	6	L1	1	1
	(b)	List the features of Pentium III processors.	6	L2	1	1
IV.	(a)	With a neat diagram, explain 64-bit processor execution environment.	6	L2	1	1,3,4
	(b)	Discuss on Intel Skylake microarchitectures.	6	L1	1	1,3,4
		OR				
V.	(a)	Explain Operand addressing in Intel 64-bit processors.	6	L2	1	1,3,4
	(b)	Discuss on basic program execution registers in IA-32 architecture.	6	L1	1	1,3,4

(P.T.O.)

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			Marks	BL	CO	PO
VI.	(a)	Draw and explain the architecture of 8051 microcontrollers.	7	L2	3	1,3,4
	(b)	Explain how 8051 interfacing with DAC.	5	L3	6	1,3,4
		OR				
VII.	(a)	Explain how 8051 interfacing with stepper motor.	5	L3	6	1,3,4
	(b)	Explain the instruction set in 8051 microcontrollers.	7	L2	3	1,3,4
VIII.	(a)	Explain the status register of PIC16F84A microcontroller.	5	L1	4	1,3
	(b)	Discuss the addressing modes in PIC16F84A microcontroller.	7	L2	4	1,3
		OR				
IX.	(a)	Draw and explain the architecture of PIC16F84A.	7	L2	4	1,3
	(b)	Draw data memory map of PIC16F84A microcontroller.	5	L1	4	1,3

Bloom's Taxonomy Levels
L1 = 33.3%, L2 = 58.33%, L3 = 8.3%

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