AMRITA VISHWA VIDYAPEETHAM
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19AIE113
Introduction to Electronics

Digital Clock using Clock Signal

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Acknowledgement

We would like to express our special thanks of gratitude to our teacher (Dr Jyothish Sir) who gave us the golden opportunity to do this wonderful project on the topic (Digital Clock using Clock Signal), which also helped us in doing a lot of research and we came to know about so many new things. We are thankful for the opportunity given.

Declaration

We declare that the Submitted Report is our original work and no values and context of it have been copy-pasted from anywhere else. We take full responsibility, that if in future, the report is found invalid or copied, the last decision will be of the Faculty concerned. Any form of plagiarism will lead to the disqualification of the report.

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Aim

Generating a clock signal for driving a digital clock and demonstrating the working of the digital clock. Building the design of a digital clock that ticks each second and goes up to 1 hour using the FF of your choice. It can be either an asynchronous or synchronous circuit. Generate square waves using a transistor-based Schmitt trigger circuit and use it as the clock signal.

Introduction

The design, implementation, and modelling of a clock that can display seconds, minutes, and 24-hour timing have been discussed. Logic gates and synchronous decade counters were used in the architectural design. The basic clock frequency signal (in hertz) that drives the clock was generated by frequency division of the desired clock pulse utilising a clock voltage source from the simulator. The digital circuit was implemented and simulated in Falstad.

Components Used

- Input Signal (AC)
- Schmitt Trigger
- Mod-10 Counter
- Mod-6 Counter
- AND gate
- 7 Segment Decoder
- 7 Segment Display

Roles of each component

Input Signal (AC)

Acts as a source of voltage to the circuit.

Schmitt Trigger

Helps in controlling the duty cycle of the input signal and also converts it from an analogue signal to the digital ones.

Mod-10 Counter

A binary counter which counts from 0-9.

Mod-6 Counter

A binary counter which counts from 0-6.

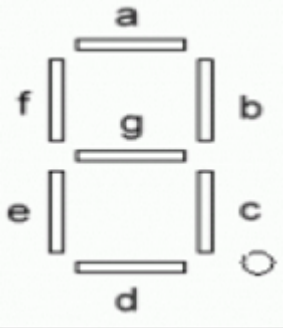
AND gate

Used to provide a connection to the successive counter based on the present counters count limit.

7 Segment Decoder

Takes the input from the binary Mod counter and outputs 7 segments where each of them is responsible for each line in the following diagram in we aim7 segment display.

7 Segment Display



This works based on the inputs given from the 7 segment decoder and lightens up each segment based on the outputs of the decoder.

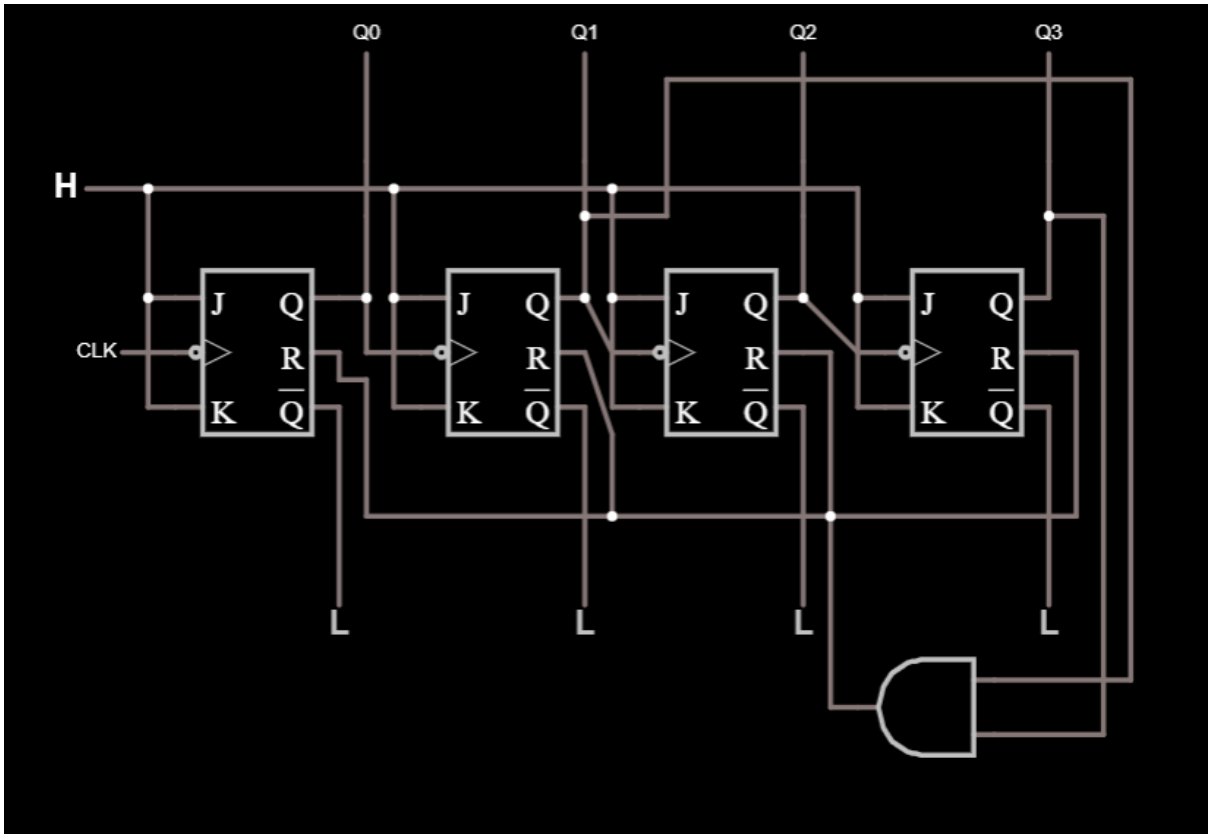
Theory

Sub Circuits

1. Mod-10 Counter
2. Mod-6 Counter
3. 7 Segment Decoder

Mod-10 Counter

Circuit Diagram

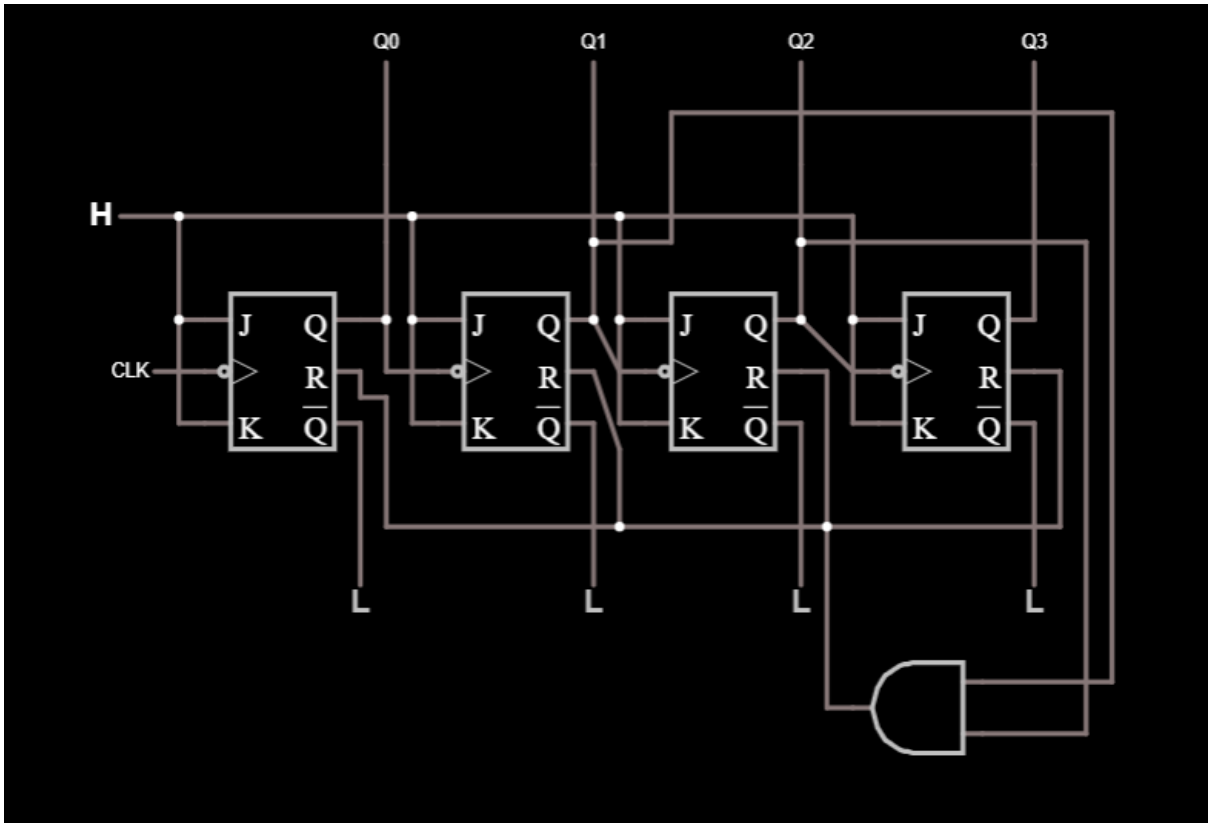


Working

The whole circuit works on a single clock signal that is given to the first JK flip flop. The subsequent flip flops work based on the outputs of the preceding JK flip flops. In this way, it goes all the way from 0000 to 1111. Since, we aim to build a Mod-10 counter, i.e. a counter which counts from 0 to 9. So, after it reaches 9, we need a logic to reset the whole circuit. Hence, we are identifying when the circuit reaches there and resetting the whole circuit to start from 0 again. So, this works as an infinite loop and stops only if there is an interrupt from the user's end.

Mod-6 Counter

Circuit Diagram

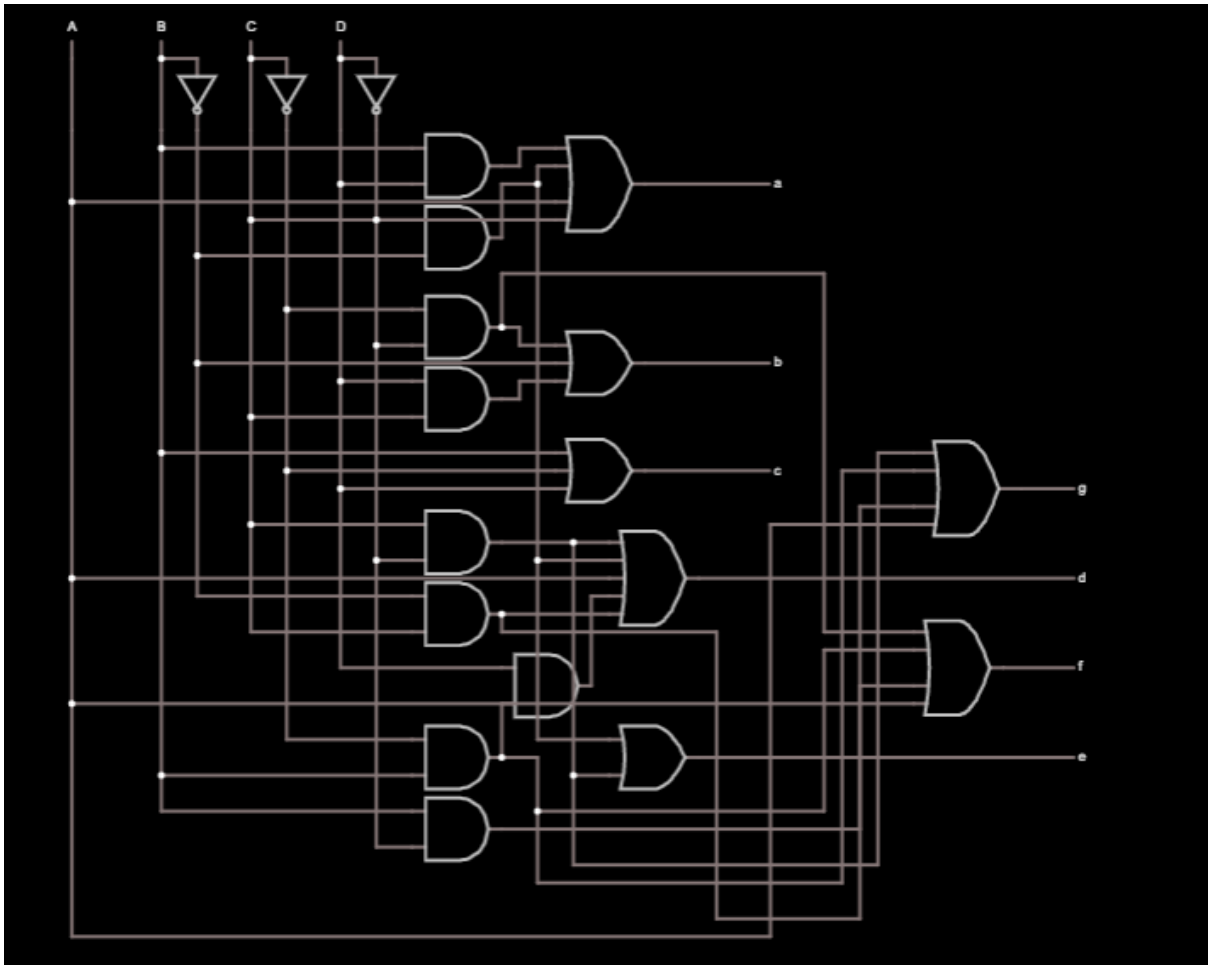


Working

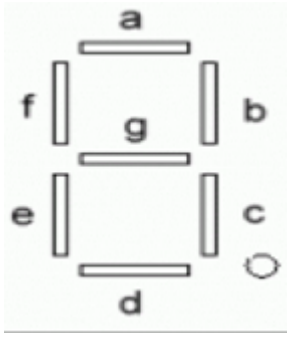
The whole circuit works on a single clock signal that is given to the first JK flip flop. The subsequent flip flops work based on the outputs of the preceding JK flip flops. In this way, it goes all the way from 0000 to 1111. Since, we aim to build a Mod-6 counter, i.e. a counter which counts from 0 to 5. So, after it reaches 5, we need a logic to reset the whole circuit. Hence, we are identifying when the circuit reaches there and resetting the whole circuit to start from 0 again. So, this works as an infinite loop and stops only if there is an interrupt from the user's end.

7 Segment Decoder

Circuit Diagram



Working



This is a 7 segment display, we connect the output of our 7 segment decoder to this to show the desired output. We can understand this by taking an example. So, if we need to display 0, except g (in the above diagram), every other bit should lighten up, i.e. in terms of electronics, we say that every other bit is high. So, when this happens, we can see a 0 forming there. In this way, we take the binary input and give the correspondence to these 7 bits to show the output in hexadecimal format in the 7 segment display.

Truth Table

A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

K-map Simplifications
Representing all segments in canonical form

Sum-of-Product form

$$a = F_1(A,B,C,D) = \Sigma(0,2,3,5,7,8,9)$$
$$b = F_2(A,B,C,D) = \Sigma(0,1,2,3,4,7,8,9)$$
$$c = F_3(A,B,C,D) = \Sigma(0,1,3,4,5,6,7,8,9)$$
$$d = F_4(A,B,C,D) = \Sigma(0,2,3,5,6,8)$$
$$e = F_5(A,B,C,D) = \Sigma(0,2,6,8)$$
$$f = F_6(A,B,C,D) = \Sigma(0,4,5,6,8,9)$$
$$g = F_7(A,B,C,D) = \Sigma(2,3,4,5,6,8,9)$$

Final expressions

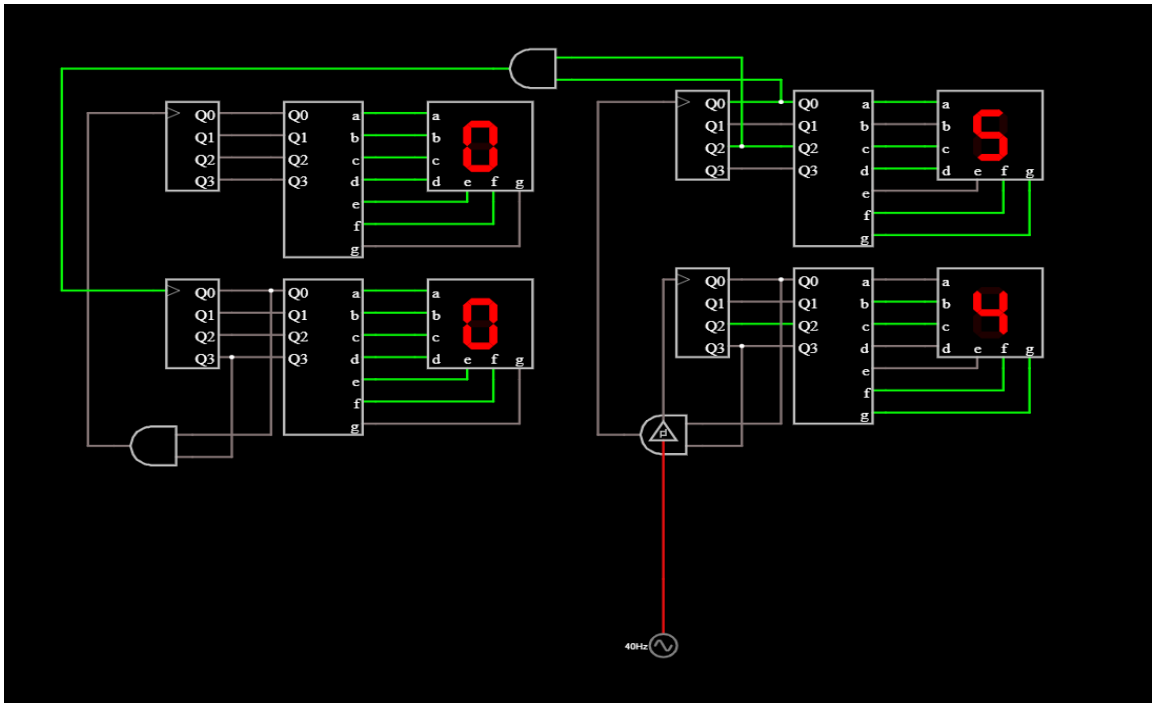
$$a = A + C + BD + \underline{B}\,\underline{D}$$
$$b = \underline{B} + \underline{CD} + CD$$
$$c = B + \underline{C} + D$$
$$d = \underline{B}\,\underline{D} + C\underline{D} + B\underline{C}D + \underline{B}C + A$$
$$e = \underline{BD} + C\underline{D}$$
$$f = A + \underline{CD} + B\underline{C} + B\underline{D}$$
$$g = A + B\underline{C} + \underline{B}C + C\underline{D}$$

Procedure:

Our main objective is to create a timer that adds up to an hour and display it. We used 2 Mod-10 counters to count the one place of several seconds and minutes and 2 Mod-6 counters to count the 10th place of seconds and minutes.
Now, we take specific bits based on how much we want to count and connect them with the AND gate. The output of this AND gate will be connected to the clock pin of the successive counter i.e which counts after the present counter.
In this way, we restrict our counters to a certain count after which it gets reset. After all these connections, we connect our counter's output to a 7 segment decoder which helps the binary bits to hexadecimal output and then we connect it to a 7 segment display to display our output.
Finally, we can use an AC signal as a clock input and we are using a Schmitt trigger to control the duty cycle of the input, which gives us control over the delay of the clock compared to our normal clock.

Circuit Diagram:

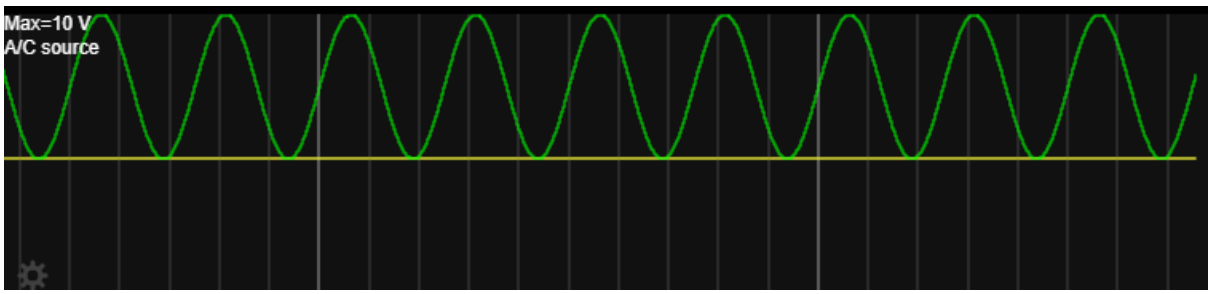
Click here to access the simulation



Results

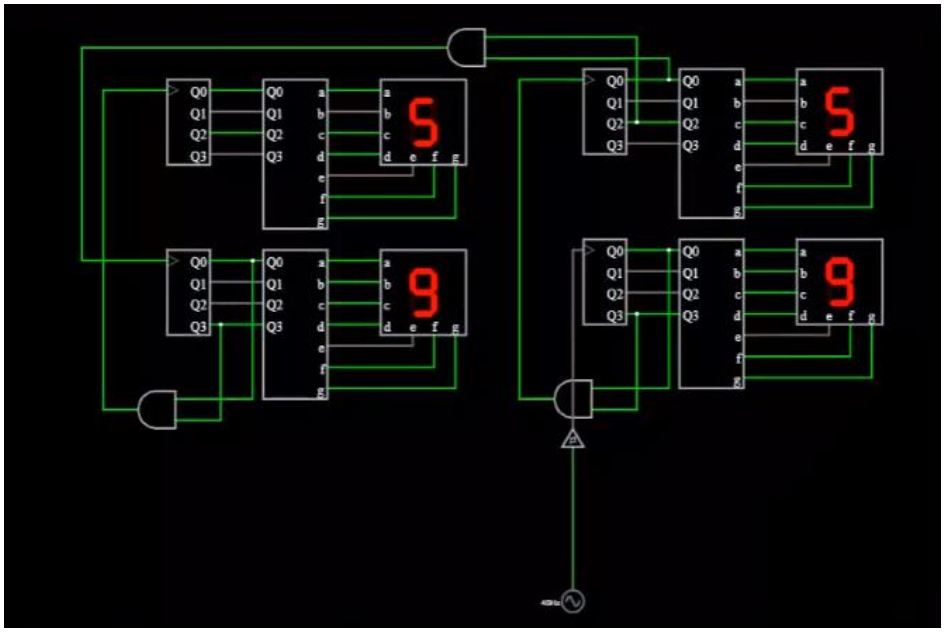
Waveforms

Input Signal



Schmitt Trigger Output

Clock Output



Inference

- We learnt the working of a Digital Clock which can take many kinds of noisy inputs and give out the correct time.
- We learnt the real-world applications of Schmitt Trigger.
- We learnt to apply the usage of decoders and counters in the real world.

Conclusion

- Usage of simple and cost-free basic chips was enough to build the whole circuit.
- Not only up to 1 hour, but we can extend it to 24 hours just by replicating the same logic.

References

- Materials provided by Dr Jyothish Lal Sir
- “Design, Implementation and Simulation of 24h Digital Clock Circuit Design”-Shaswat Satapathy, Shivani Singh, and Bidyashree Rout.

Contributions

1. Anirudh Edpuganti - Logic implementation of Mod 6 and 10 Counters
2. Rishekesan - Logic Analysis and overall model idea
3. Shreya - Report and Theory of Segment Decoder
4. Bhoomika - Logic implementation of Segment Decoder
5. Gokul - PPT and Theory of Mod Counters