

# CMOS Scaling : Era of Transition Metal Dichalcogenides

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# Introduction to TMDs

- Graphene as channel material posed challenges
  - (1) **Zero bandgap**  $\implies$  Switching off was an issue
  - (2) **Bandgap engineering**  $\implies$  Reduced mobility
- Transition Metal Chalcogenides (TMDs)
  - (1) Compounds with formula  $MX_2$
  - (2) M is transition metal (Groups IV, V and VI)
  - (3) X is chalcogenide (Group XVI)

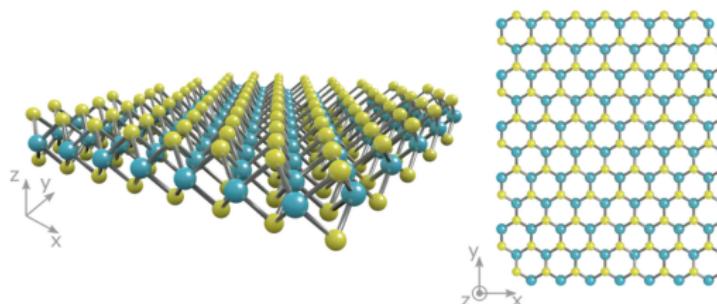


Figure: MoS<sub>2</sub> : Structure <sup>1</sup>

# TMDs : Properties

Favourable for Ultra scaled CMOS

- (1) Ultra thin Si films have degraded mobility ( $\approx 150 \text{ cm}^2/\text{Vs}$ )
- (2) Monolayer thickness  $< 1 \text{ nm} \implies$  High electrostatic control
- (3) Bandgaps similar to Si
- (4) No dangling bonds  $\implies$  cleaner interface

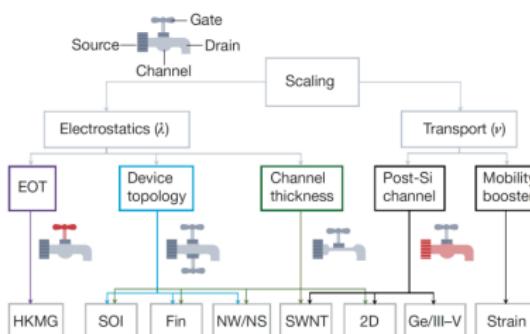


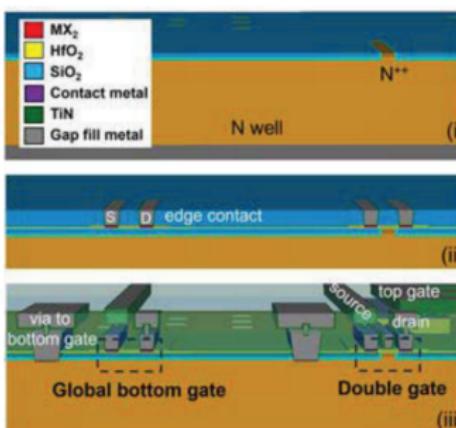
Figure: The future transistors <sup>2</sup>

<sup>2</sup>Cao, W., Bu, H., Vinet, M. et al. The future transistors. Nature 620, 501–515 (2023)

# TMDs : Fabrication\*

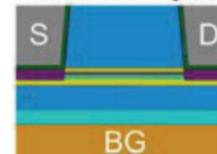
Single Layer planar devices (Intel, 2023 IEDM)  
2D channel deposition using MOCVD

- Starting Si wafer
- Blanket well implantation
- Local Si bottom gate formation, bottom gate degenerate doping (i)
- Bottom dielectric deposition
- 2D channel deposition
- Top dielectric deposition and active patterning
- Trench edge contact formation (ii)
- Trench top gate formation
- Via to back gate formation
- Via and pad formation (iii)



## Device Configurations

Global bottom gate



Double gate



Figure: Single Layer planar devices <sup>3</sup>

<sup>3</sup>Exploring manufacturability of novel 2D channel material 300 mm wafer-scale 2D NMOS & PMOS using MoS<sub>2</sub>, WS<sub>2</sub>, & WSe<sub>2</sub>, C. Dorow, et al., IEDM 2023

# TMDs : Fabrication

Monolayer-MoS<sub>2</sub> Stacked Nanosheet (TSMC, 2023 IEDM)  
2D channel deposited using CVD/film transfer

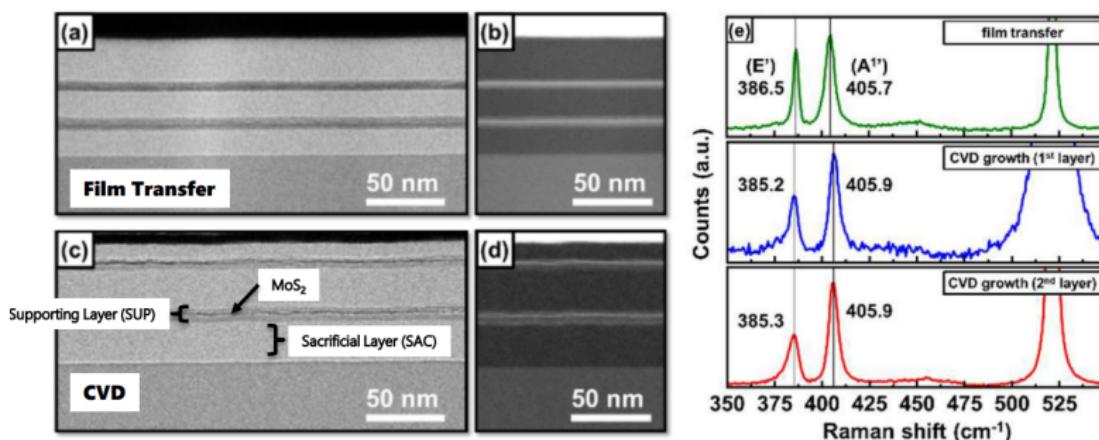


Figure: Monolayer-MoS<sub>2</sub> Stacked Nanosheet <sup>4</sup>

<sup>4</sup>Y. -Y. Chung et al., "Monolayer-MoS<sub>2</sub> Stacked Nanosheet Channel with C-type Metal Contact," 2023 International Electron Devices Meeting (IEDM),

# TMDs : Fabrication

## Bottom-up methods

- Molecular Beam Epitaxy (MBE) : Slow process
- Physical Vapor Deposition (PVD) : Multilayer films
- Chemical Vapor Deposition (CVD) : Best outcomes

## Challenges for CMOS compatible process

- High quality epitaxial growth of TMD at <450 °C for FEOL
- Low temperature Interfacial Layer deposition ‘
- Better choices for sacrificial/supporting layer without impacting TMD layer during etch

# Mobility

Typical mobility of CVD grown  $\text{MOS}_2 \approx 40 \text{ cm}^2/\text{Vs}$   
 $2.5 \text{ nm thick Si} \approx 150 \text{ cm}^2/\text{Vs}$

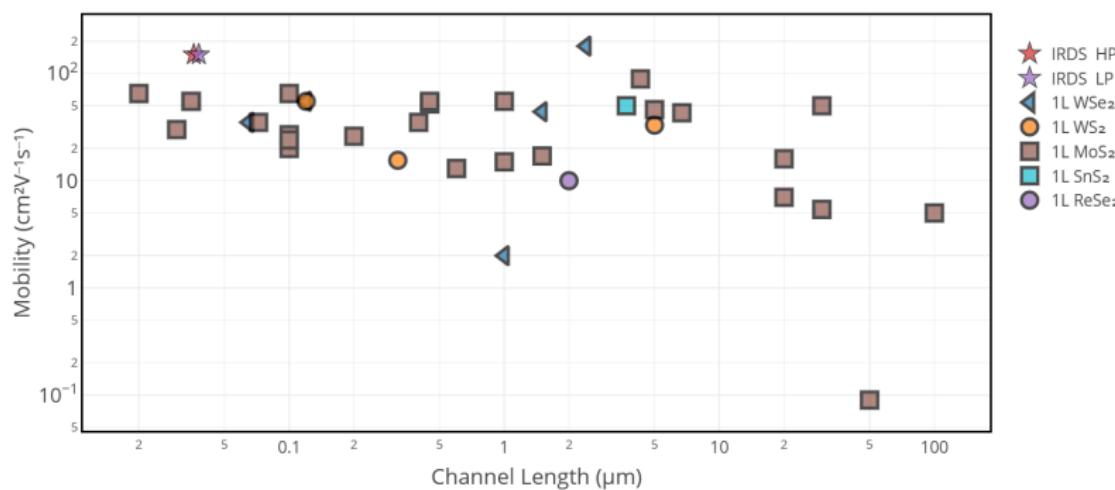


Figure: Mobility in TMDs <sup>5</sup>

<sup>5</sup>C.J. McClellan, S.V. Suryavanshi, C.D. English, K.K.H. Smithe, C.S. Bailey, R.W. Grady, E. Pop , "2D Device Trends," Accessed on: 04/20/2025

# Contact Resistance

Slightly higher Schottky barrier than a metal/Si contact  
Contact resistance is a strong function of gate bias

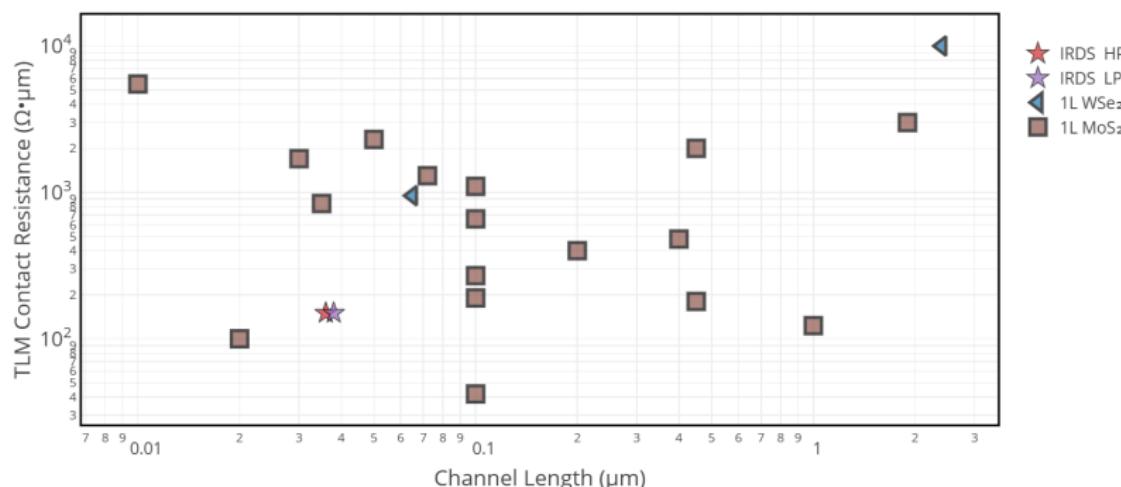


Figure: Contact Resistance <sup>6</sup>

<sup>6</sup>C.J. McClellan, S.V. Suryavanshi, C.D. English, K.K.H. Smithe, C.S. Bailey, R.W. Grady, E. Pop , "2D Device Trends," Accessed on: 04/20/2025

# Gate Stack Defects\*

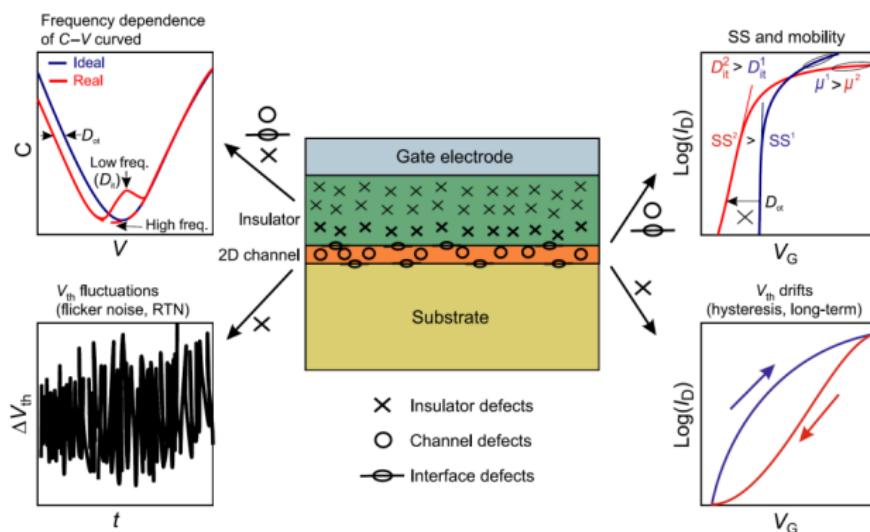


Figure: Gate Stack Defects <sup>7</sup>

<sup>7</sup> Illarionov, Y.Y., Knobloch, T., Jech, M. et al. Insulators for 2D nanoelectronics: the gap to bridge. Nat Commun 11, 3385 (2020)

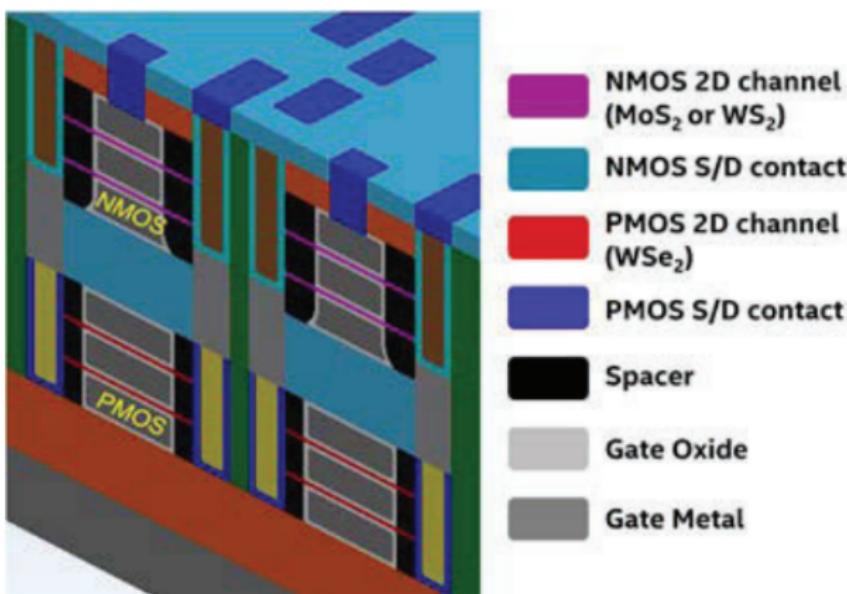
# Exploring manufacturability of novel 2D channel material 300 mm wafer-scale 2D NMOS & PMOS using MoS<sub>2</sub>, WS<sub>2</sub>, & WSe<sub>2</sub>

C. Dorow, et al. (Intel, IMEC IEDM 2023)

# Proposed Structure (2D Nano-sheet CFETs)

First work on scaling 2D materials to 300mm

- Highly scaled gate lengths
- More channels per stack



# Device Fabrication

- Evaluate Transistors  $\Rightarrow$  Planar process
- Two types of devices
  - (1) Global Bottom Gate ( $EOT_{BG} = 50\text{-}62 \text{ nm}$ )
  - (2) Double Gate ( $EOT_{\text{combined}} = 2.2 \text{ nm}$ )

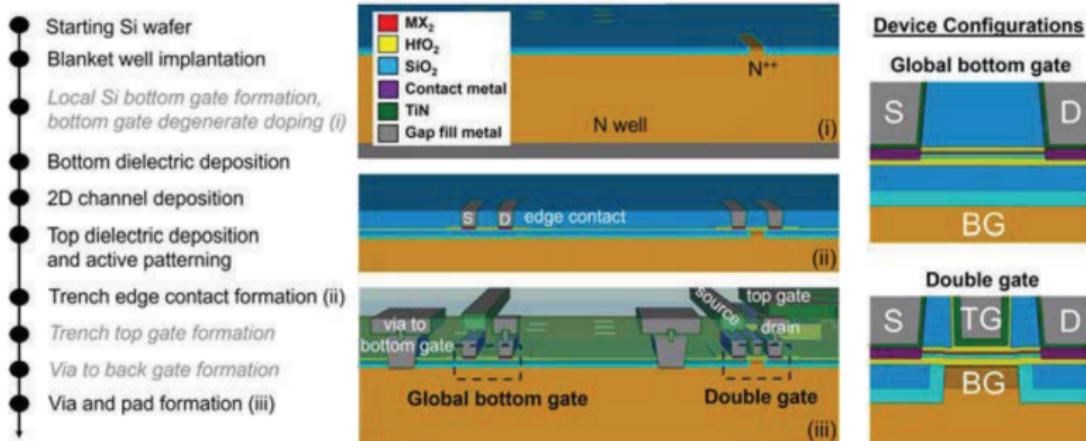


Figure: Process Flow to test transistors

# TMD Deposition

- Direct Deposition using MOCVD
- Advantages over ALD
  - Incompatible for direct growth on amorphous substrates
  - Difficult to scale to 300 mm
- Two types of grains
  - **Small Grain (SG)**  $\approx 100 \text{ nm}$
  - **Large Grain (LG)**  $\approx 1 \mu\text{m}$

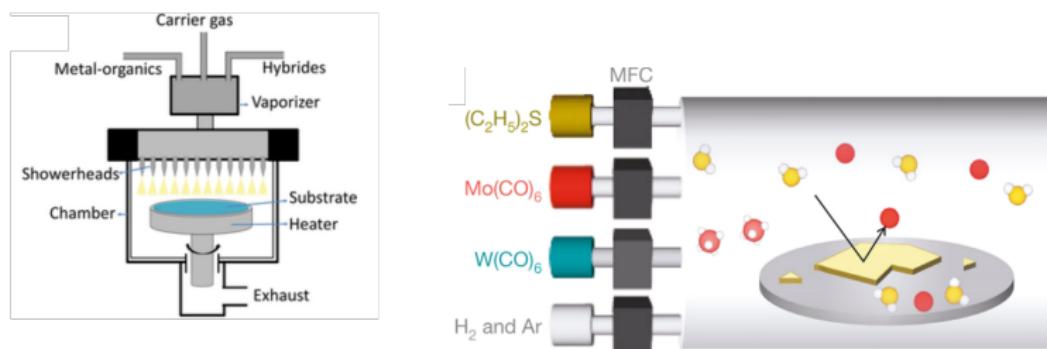
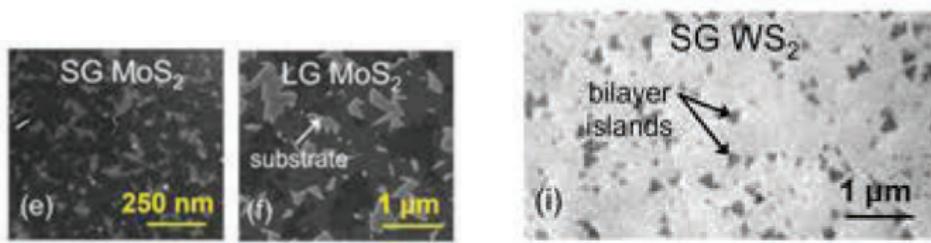


Figure: MOCVD

300 mm 2D NMOS

- **Candidates** : MoS<sub>2</sub>, WS<sub>2</sub>
  - **Contacts** : Ti
  - SG MoS<sub>2</sub> has lower mobility, higher SS compared to SG WS<sub>2</sub>  
    ⇒ Higher defects due to smaller grain size



**Figure:** Grain size : (a) MoS<sub>2</sub> (b) WS<sub>2</sub>

## NMOS Metrology : $I_{MAX}$ vs $L_{channel}$ , $R_c$ extraction

- SG MoS<sub>2</sub> shows higher current due to lower R<sub>c</sub>

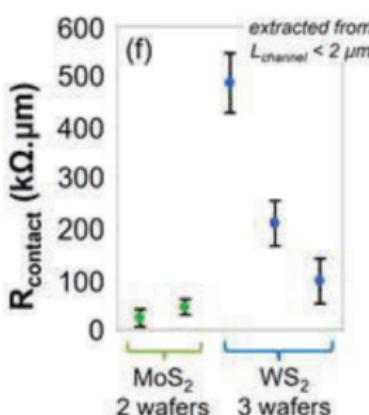
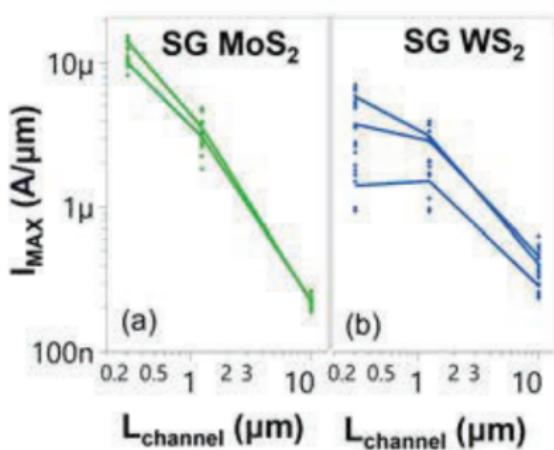
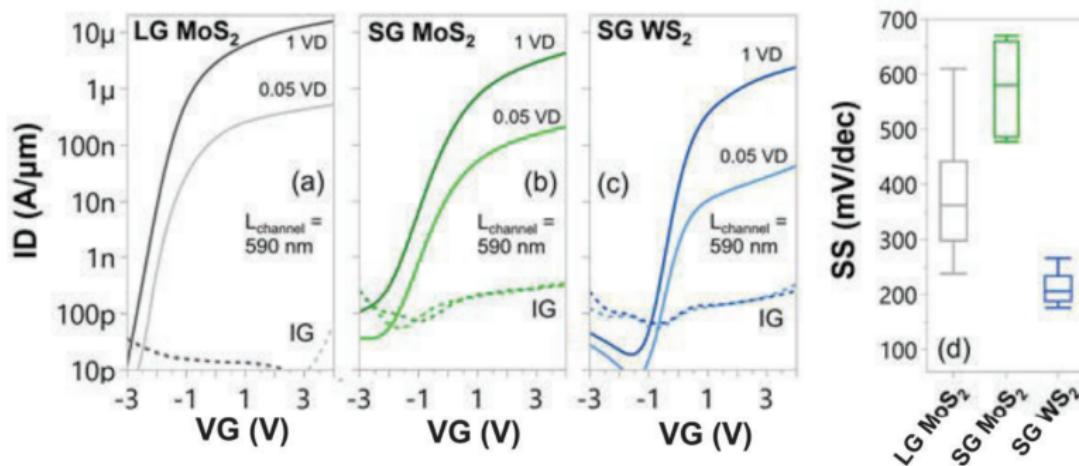


Figure: (a) IDVG Curve (b)  $R_c$  Curve

NMOS Metrology : IDVG Curves

- Increasing grain size improves NMOS performance  
     $\Rightarrow$  Lower defectivity due to better crystallinity of LG films
  - $\mu_{LG} \approx 4 \times \mu_{SG}$



## Figure: LG vs SG

# NMOS Metrology : $I_{MAX}/I_{MIN}$ vs $L_{channel}$ curve

- $I_{MAX}$  upto 10x larger for LG over SG

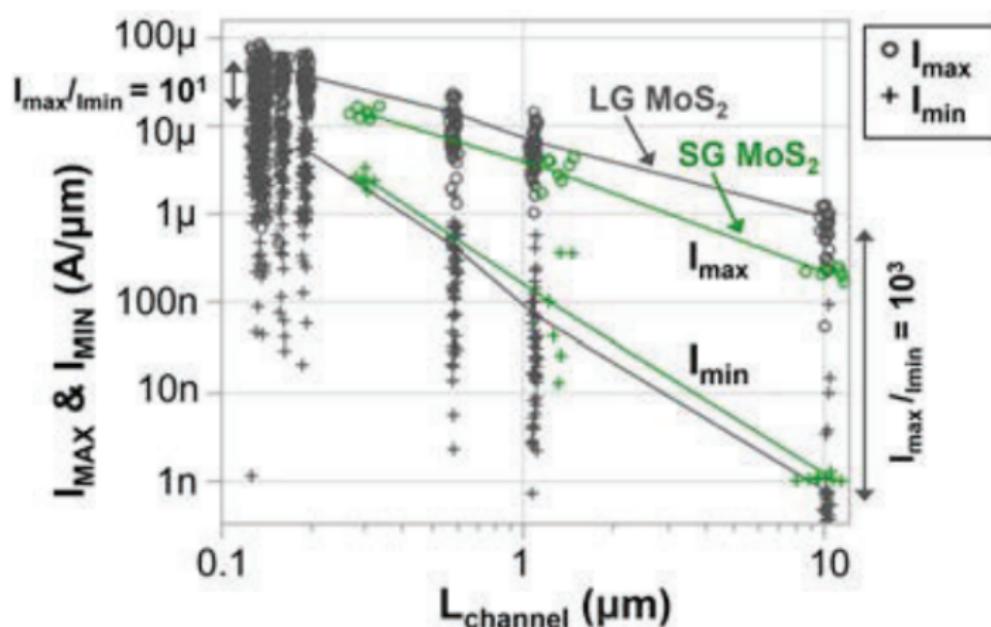


Figure:  $I_{MAX}/I_{MIN}$  vs  $L_{channel}$

300 mm PMOS

- Candidates : WSe<sub>2</sub>
  - Contacts : Ru
  - $I_{LG} \approx 5 \times I_{SG}$
  - $\mu_{LG} \approx 30 \text{ cm}^2/\text{Vs}$

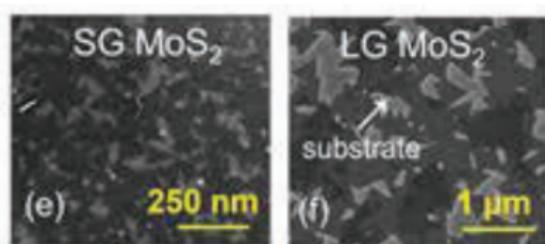


Figure: Grain Size : WSe<sub>2</sub>

## PMOS Metrology : IDVG curves

- Increasing grain size improves PMOS performance

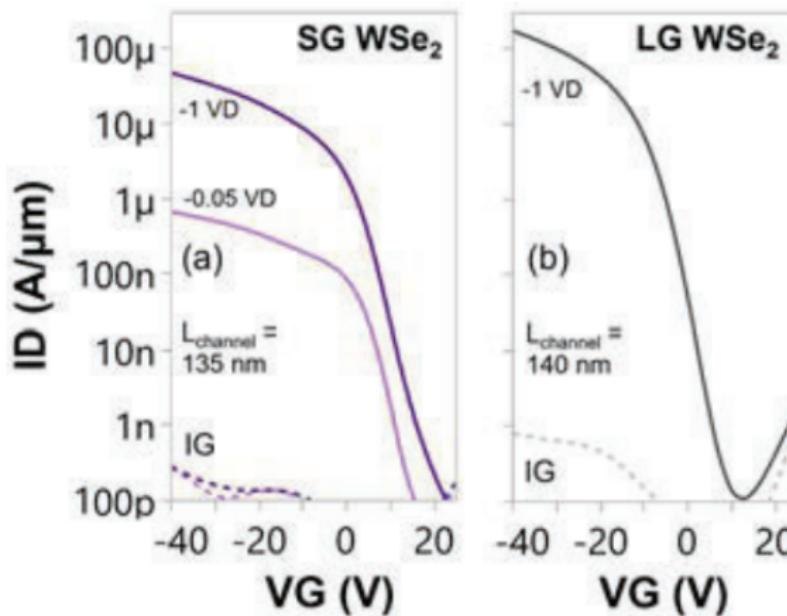


Figure: PMOS : IDVG curves

# PMOS Metrology : IDVG curves

- Thinner channels show  $I_{off} \leq 20 \text{ pA}/\mu\text{m}$  and lower DIBL

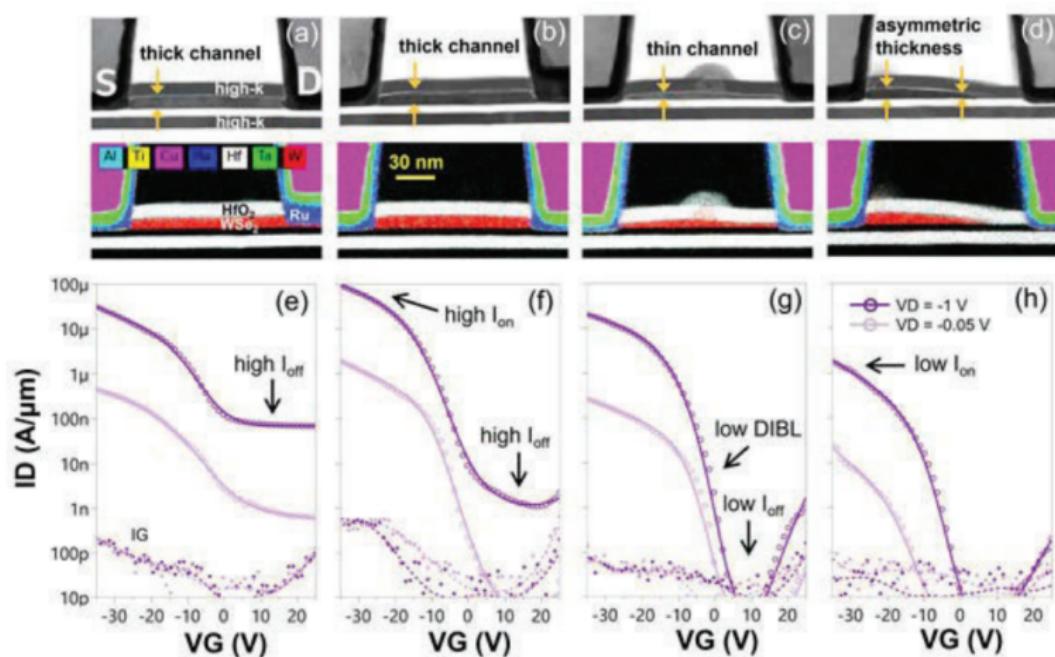
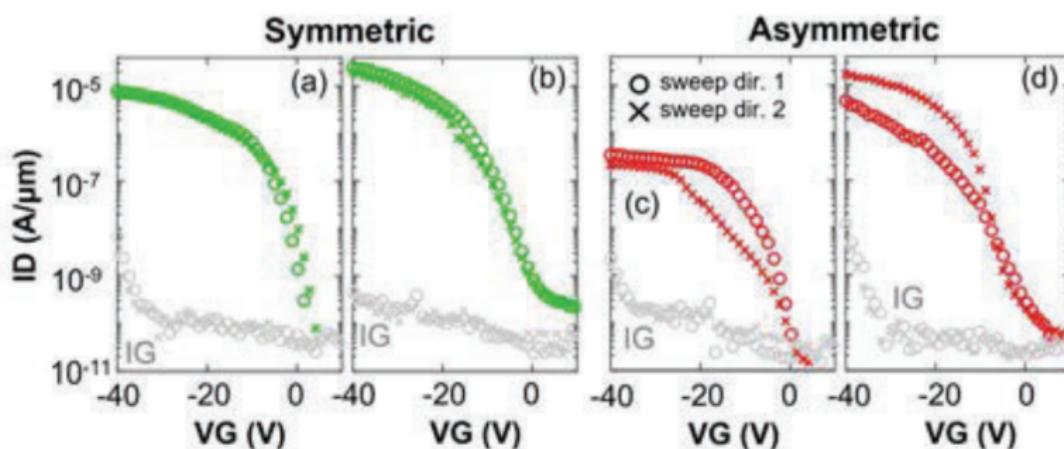


Figure: PMOS : IDVG curves

PMOS Metrology : Symmetric vs Asymmetric

- Switching S/D shows two types of behaviour
    - (1) **Symmetric** : Fully continuous uniform 2D films
    - (2) **Asymmetric** : Difference in 2D layer width



**Figure:** Symmetric S/D vs Asymmetric S/D

# PMOS Metrology : Ambipolar Behaviour

- Alternate Candidate : SG WS<sub>2</sub> shows ambipolar behaviour with  $I < 100 \text{ nA}/\mu\text{m}$

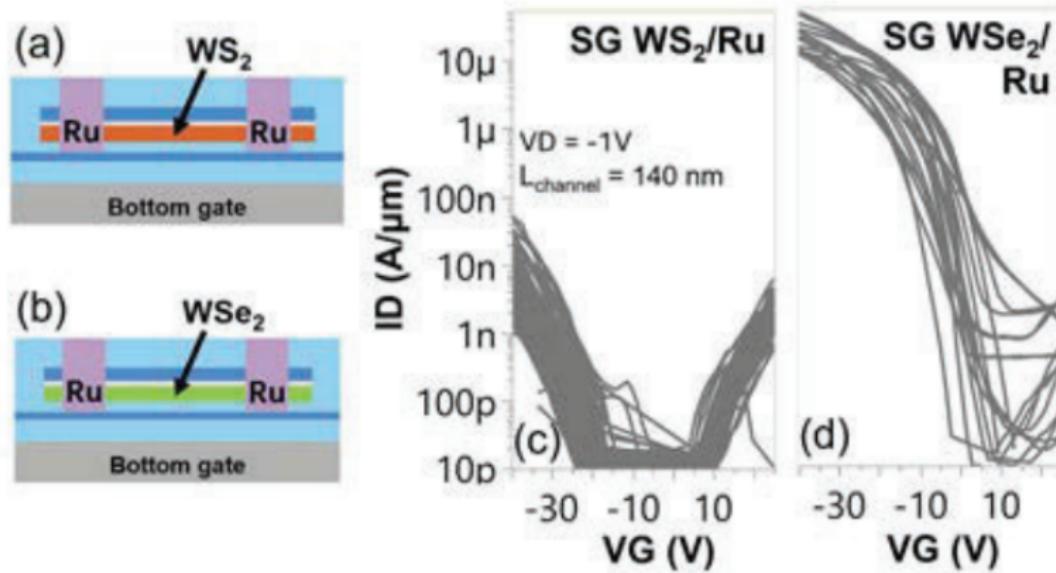


Figure: Ambipolar Behaviour of WS<sub>2</sub>

# PMOS Metrology : $I_{MAX}/I_{MIN}$ vs $L_{channel}$ curve

- Higher  $I_{MAX}$  for LG over SG

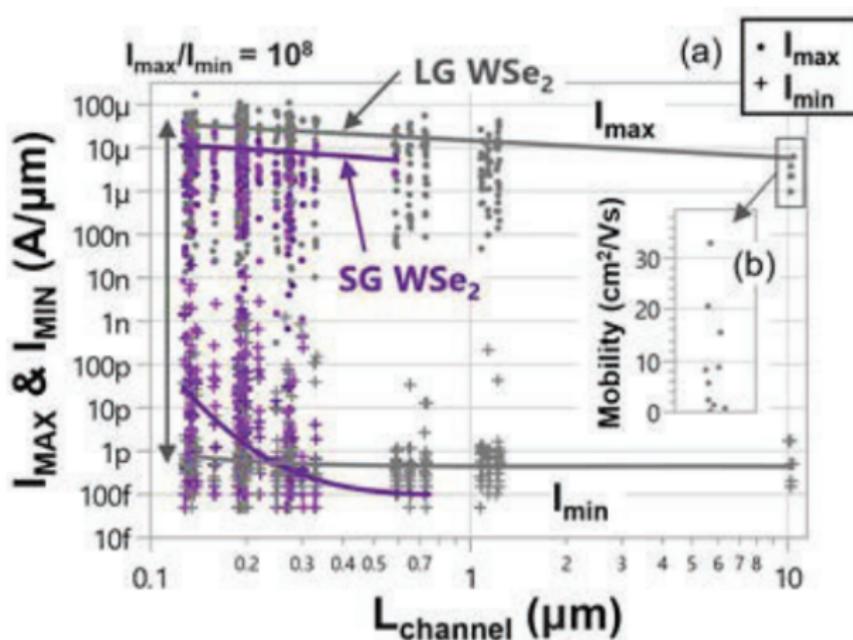


Figure: PMOS Metrology :  $I_{MAX}/I_{MIN}$  vs  $L_{channel}$

## Bias Temperature Instability (BTI)

- MoS<sub>2</sub> - Large degradation
  - WS<sub>2</sub> - Worst behaviour
  - WSe<sub>2</sub> - low NBTI (good for PMOS)
  - **Difference in BTI**
    - (1) Different band offsets
    - (2) Different interactions with top AlO

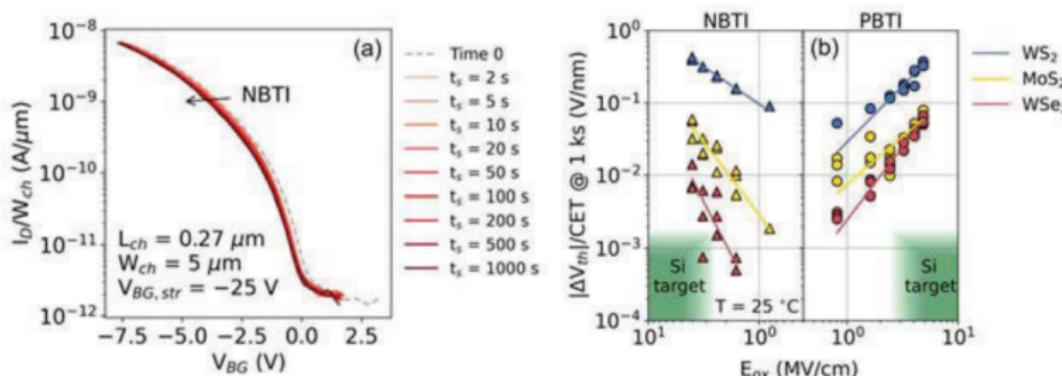


Figure: (a) NBTI measurement (b) NBTI vs PBTI

# Conclusion

- First look at 300mm TMD candidates
- Simplified direct deposition of TMD
- **Going Forward :**
  - (1) Uniform single crystal growth
  - (2) Specialized processes to enhance gate oxide nucleation
  - (3) Atomic etching to integrate thin layers

## Conclusion

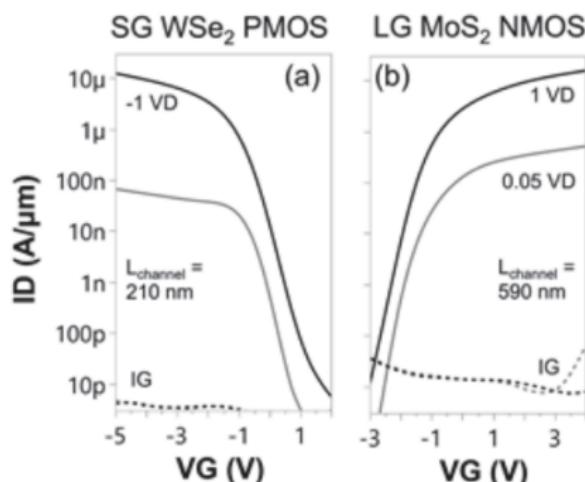


Fig. 15. (a) PMOS local bottom gate device with SG WSe<sub>2</sub>. (b) NMOS double gate device with LG MoS<sub>2</sub>.

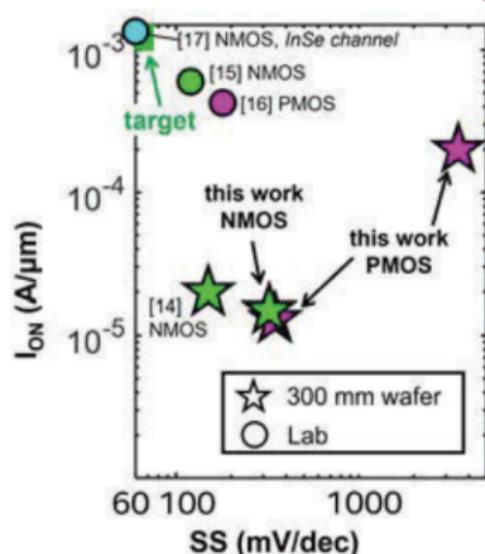


Fig. 16. Benchmark of 2D NMOS and PMOS, 300 mm and lab scale.

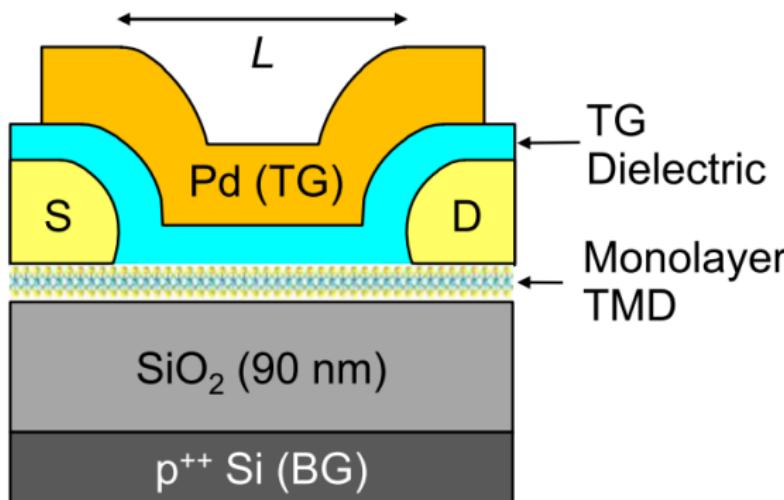
# Achieving 1-nm-Scale Equivalent Oxide Thickness Top-Gate Dielectric on Monolayer Transition Metal Dichalcogenide Transistors With CMOS-Friendly Approaches

Jung-Soo Ko, Alexander B. Shearer, Sol Lee,  
Kathryn Neilson, Marc Jaikissoon, Kwanpyo Kim,  
Stacey F. Bent, Eric Pop and Krishna C. Saraswat

## Proposed Structure

This paper discusses two techniques to achieve 1 nm EOT

- (1) Using an Si seed crystal
  - (2) ALD of  $\text{AlO}_x$



**Figure:** Cross-Section Schematic of dual-gated TMD

## Si Seed Layer Deposition

- (1) CVD of TMDs on 90 nm SiO<sub>2</sub>

  - MoS<sub>2</sub> at 750°C
  - WSe<sub>2</sub> at 850°C

(2) XeF<sub>2</sub> dry etch  $\Rightarrow$  Active region patterning

(3) Electron beam evaporation of Au and Pd  $\Rightarrow$  S/D Deposition

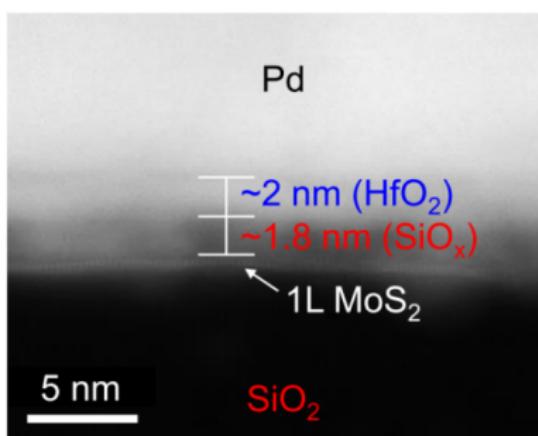
(4) Electron-beam evaporation  $\Rightarrow$  Si seed layer deposition

(5) Oxidation : Si  $\rightarrow$  SiO<sub>2</sub>

(6) ALD of HfO<sub>2</sub>

(7) Pd deposition  $\Rightarrow$  Top gate deposition

Figure: Gate Stack Deposition



## Figure: Gate Stack Deposition

# IDVG Curve : 0.7 nm Si seed

- (1)  $V_{TG} = 0 \implies$   
Unipolar behaviour
- (2)  $V_{TG} = V_{BG} \implies$   
Ambipolar behaviour
- (3) Suboptimal band alignment  
of WSe<sub>2</sub> with SiO<sub>x</sub>  
 $\implies$  Hysteresis

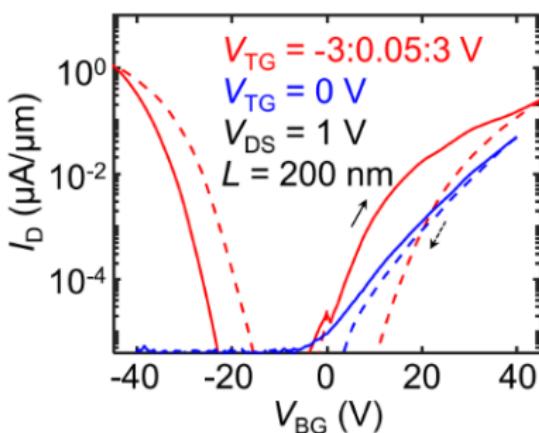
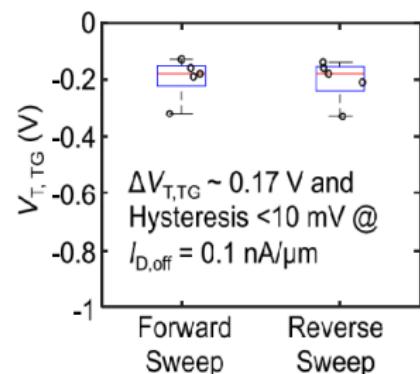
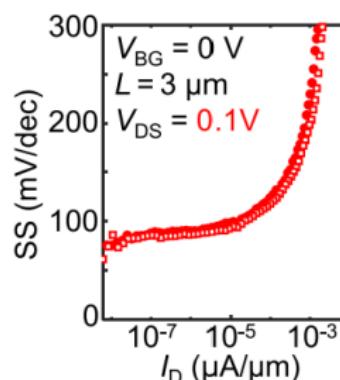
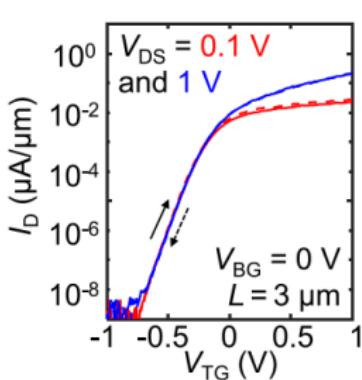


Figure: IDVG curve

### IDVG Curve : 0.2 nm Si seed

- $\frac{I_{ON}}{I_{OFF}} > 10^7$
  - Negligible hysteresis and low  $\sigma V_T$
  - $SS_{min} \approx 70 \text{ mV/dec}$
  - EOT  $\approx 0.9 \text{ nm}$



**Figure:** (a) IDVG (b) SS (c)  $\sigma_{V_T}$

IDVG : 6 nm Al<sub>2</sub>O<sub>x</sub> + 6 nm HfO<sub>2</sub>

- Direct ALD of Alumina ( $\text{AlO}_x$ ) at 100 °C  
**Precursors :** Tetraethylalumnum (TEA) and  $\text{H}_2\text{O}$
  - 6 nm  $\text{AlO}_x$  + 6 nm  $\text{HfO}_2$  shows
    - (1) Negligible defect density
    - (2) Negligible hysteresis

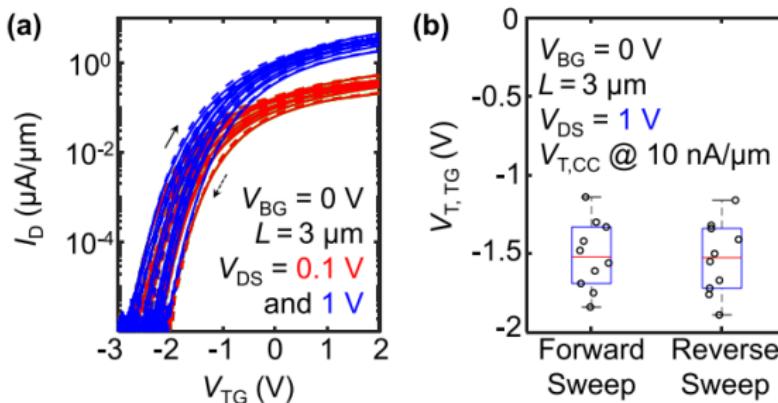


Figure: (a) IDVG for IDVG : 6 nm AlO<sub>x</sub> + 6 nm HfO<sub>2</sub>  
 (b)  $V_T$  variation

IDVG : 3 nm AlO<sub>x</sub> + 6 nm HfO<sub>2</sub>

- High ON/OFF ratio ( $> 10^6$ )
  - Negligible hysteresis

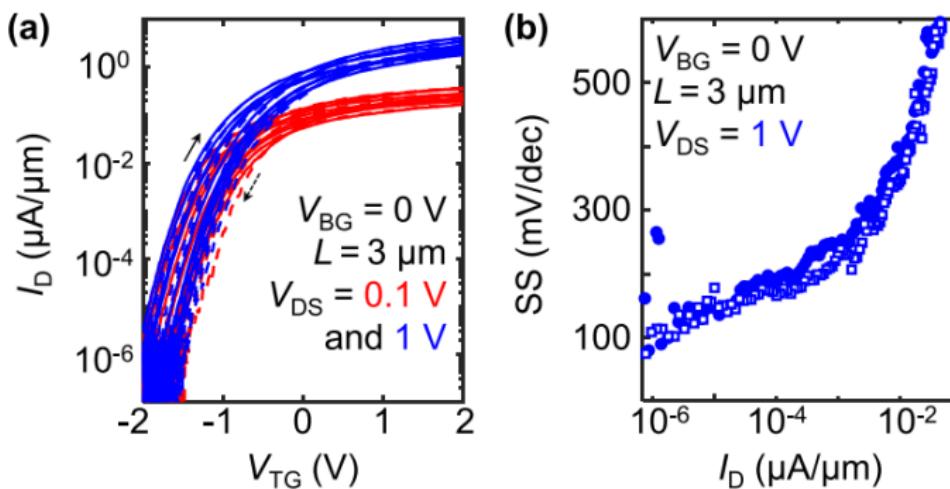


Figure: (a) IDVG curve (b) SS

# IDVG : 1.5 nm AlO<sub>x</sub> + 6 nm HfO<sub>2</sub>

- SS<sub>min</sub> of 80 mV/dec at 300 K

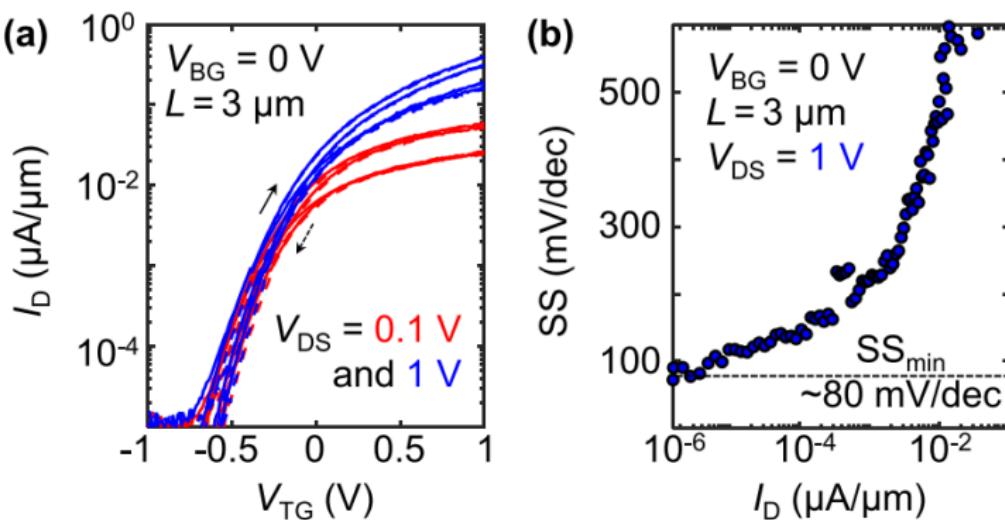


Figure: (a) IDVG curve (b) SS

## $V_T$ behaviour

## Change in Threshold Voltage

- (1) Si seed thickness  $\downarrow \Rightarrow V_T \downarrow$   
 (2) AlO<sub>x</sub> thickness  $\downarrow \Rightarrow V_T \uparrow$

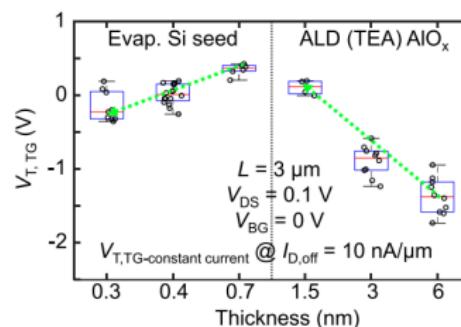
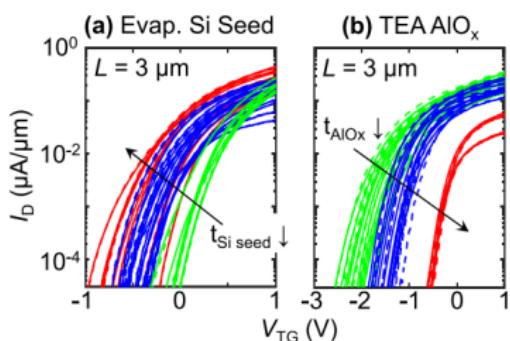


Figure:  $V_T$  variation

EOT Estimation : 1.5 nm AlO<sub>x</sub> + 6 nm HfO<sub>2</sub>

- Obtain  $I_D$  vs  $V_{TG}$  for different  $V_{BG}$
  - Plot  $V_{T,TG}$  vs  $V_{BG}$
  - $|Slope| = \frac{C_{BOX}}{C_{TOX}}$
  - Estimated EOT  $\approx 1.06$  nm
  - $SS_{min} \approx 80$  mV/dec

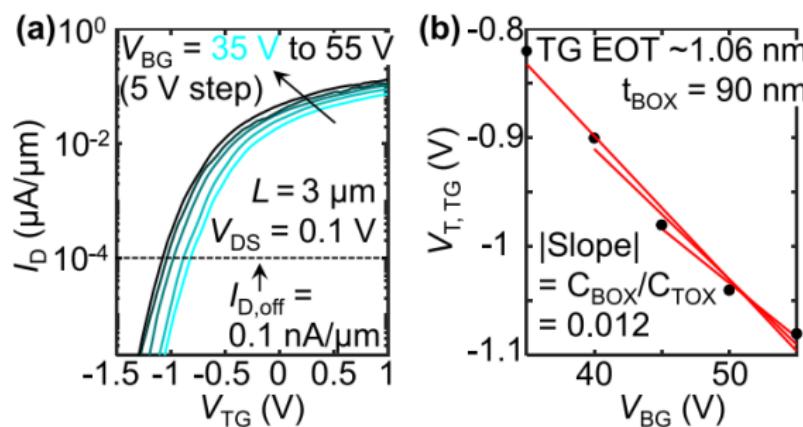


Figure: (a) IDVG curve (b) EOT estimation

# EOT Estimation : 0.2 nm Si seed + 6 nm HfO<sub>2</sub>

Estimated EOT  $\approx 0.9$  nm

Top gate leakage current density  $\approx 2 \mu\text{A}/\text{cm}^2$

SSmin  $\approx 70$  mV/dec

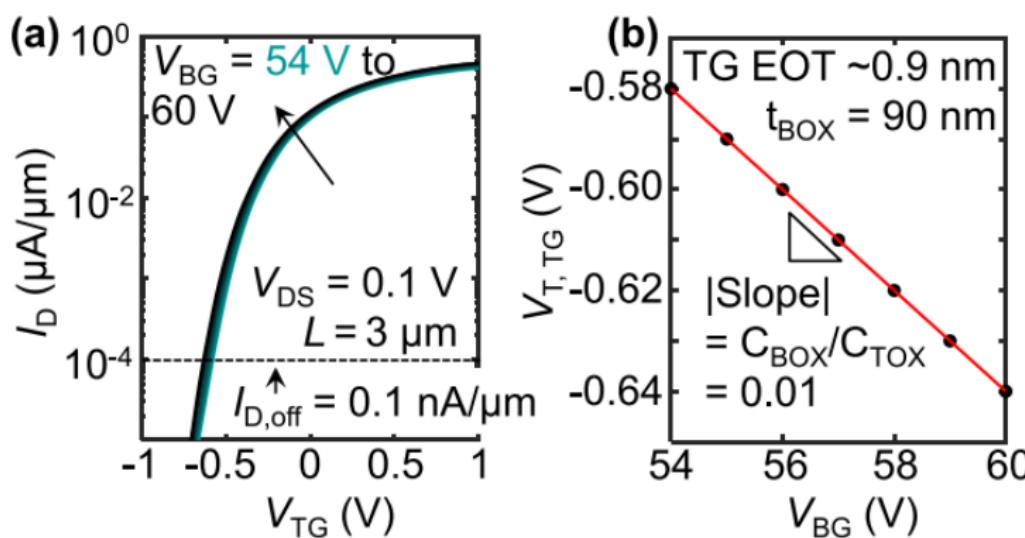
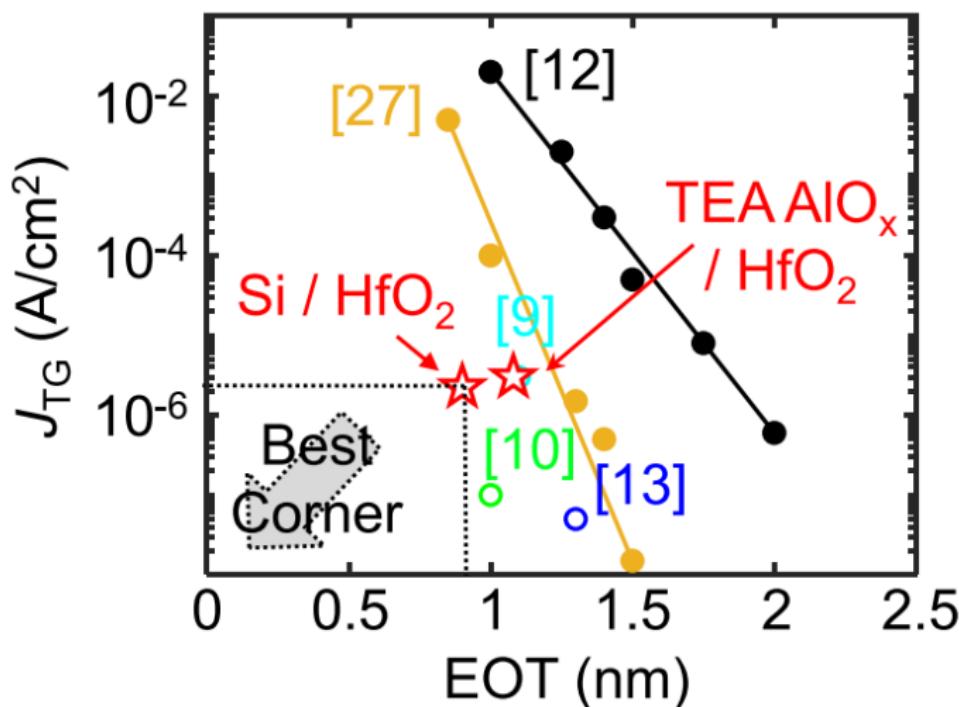


Figure: (a) IDVG curve (b) EOT estimation

# Benchmarking

Benchmarking was done on top-gate leakage current density



# Conclusion

**With Si seed,**

- (1) EOT  $\approx 0.9$  nm
- (2) SS  $\approx 70$  mV/dec
- (3) Top gate leakage current density  $2 \mu\text{A}/\text{cm}^2$

**With AlO<sub>x</sub>,**

- (1) EOT  $\approx 1$  nm
- (2) SS  $\approx 80$  mV/dec
- (3) Top gate leakage current density  $3 \mu\text{A}/\text{cm}^2$

**In summary, the paper successfully demonstrates**

- (1) 1 nm EOT with low leakage current and good SS
- (2) Process flow compatible with industry standards

# Future of 2D TMDs

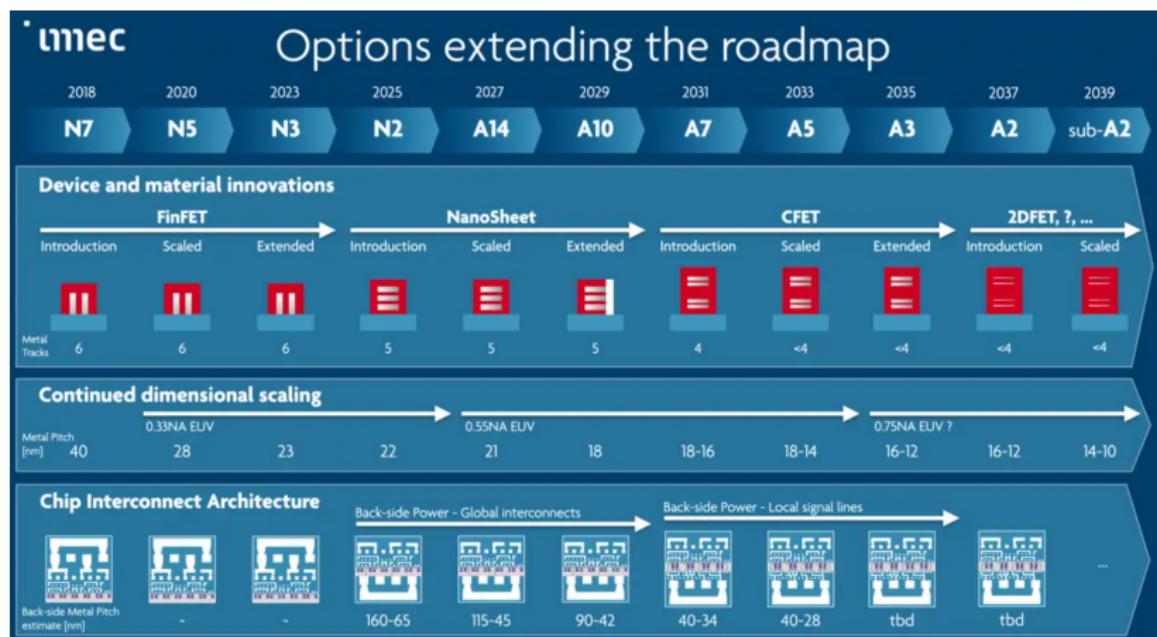


Figure: Reference : IMEC<sup>8</sup>

<sup>8</sup>Introducing 2D-material based devices in the logic scaling roadmap