EE5320 : Analog IC Design
Jan - May 2024
Assignment 8

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Table showing OPAMP Parameters

Parameter	Value
Supply Voltage (Vdd)	1.8 V
Vss	0 V
Common Mode Bias (Vcm)	0.9 V
Length of all transistors (L)	0.3 μm
Width of all transistors (W)	1 μm
Multipliers for MOSFETs	
m00	2 (specified in the Question)
m01	1.63
m0	40
m1 = m2 = m5 = m6	57
m3 = m4 = m7 = m8	16
m11 = m13	65
m12 = m14	200
m0x	40
m3x = m4x	5
mc0	24
mc1 = mc2	10
mc3 = mc4	13
Bias current (I00)	10 μA
VB56	600 mV
VB78	900 mV
Ad = As (for all MOSFETs)	0.36 pm^2
Pd = Ps (for all MOSFETs)	2.72 μm

Simulation Temperature	100 ℃
Rcm	100 kΩ
Cc	1 pF
Ccm	3 pF
Ccmx	0 pF
gm1	1.1 mS
gm11	9.4 mS
Ri, Rf	19 kΩ, 285 kΩ
RL	1205.719 Ω
CL	24 pF
k	15
Closed Loop Bandwidth (fB)	11 MHz

Table showing Simulation Results

Parameter	**Obtained Value**
Closed Loop DC Gain	23.505 dB (= 14.97)
Closed Loop 3-dB Bandwidth	13.7113 MHz
Unity Loop Gain Frequency	8.668 MHz
Phase Margin	78.0105 degrees
Integrated RMS Output Noise Voltage	1.84951 mV
Opamp Open Loop DC Gain	78.627 dB (= 8537.879)
Positive Slew Rate	45.262 V/μs
Negative Slew Rate	51.228 V/μs
HD3	-63.5769 dB
Supply Voltage	1.8 V
Current Consumption	2.707 mA
Power Consumption	4.8726 mW
Input Swing Limit	[-122.45 mV, 116.62 mV]
Output Swing Limit	[-1.49 V, 1.5185 V]
Unity Loop Gain Frequency (CMFB2)	19.9526 MHz
Phase Margin (CMFB2)	72.01739 degrees

Table showing VDSAT results for all the MOSFETs used

Component	Observed VDSAT	Required VDSAT
M0	253.7 mV	250 mV
M1	143.5 mV	150 mV
M2	143.5 mV	150 mV
M3	145.2 mV	150 mV
M4	145.2 mV	150 mV
M5	135.9 mV	150 mV
M6	135.9 mV	150 mV
M7	134.2 mV	150 mV
M8	134.2 mV	150 mV
M00	255.1 mV	250 mV
M01	147.6 mV	150 mV
M11	240.4 mV	250 mV
M12	265 mV	250 mV
M13	240.4 mV	250 mV
M14	265 mV	250 mV

VB56 and VB78 are picked such that 50mV swing limit is permitted as described in the Assignment.

Table showing Noise Contribution results

Noise Summary - percentage contribution to noise	
Ri	79.7 %
Rf	5.31 %
First stage of the OPAMP (fn + id noise)	14.96 %
Second stage of the OPAMP	0 %
RL	0 %

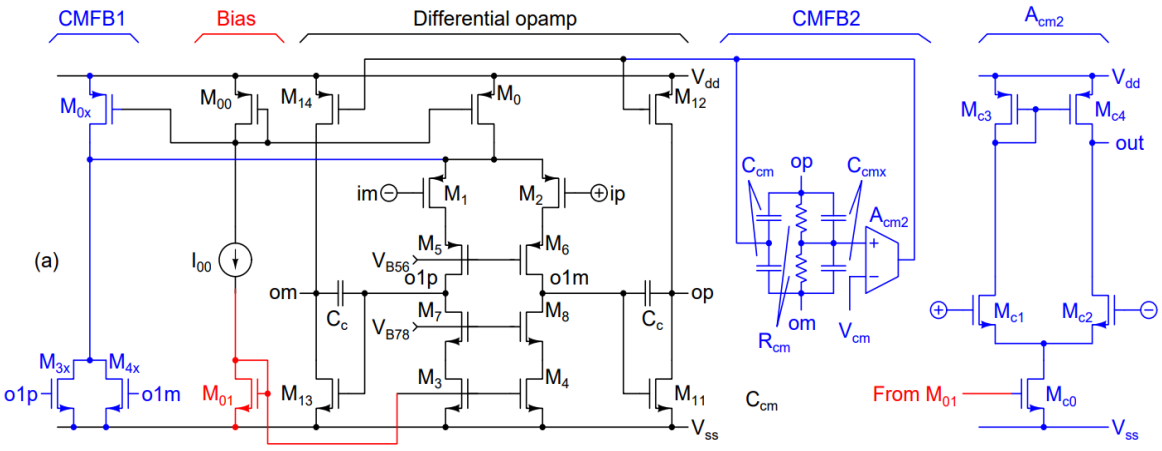
As expected, the noise from the resistors is the maximum, followed by the first stage. The second stage and the load resistor do not contribute to the overall noise. Noise has been integrated from 10 KHz to 100 MHz and results are presented.

Table showing Individual Noise Contribution results

Component Name	Contribution to Noise
Ri (both combined)	39.86 + 39.84 = 79.7
kRi (both combined)	2.66 + 2.65 = 5.31
M4	4.32 + 1.65 = 5.97 (Flicker + Thermal)
M3	4.31 + 1.64 = 5.95 (Flicker + Thermal)
M2	1.46 + 0.05 = 1.51 (Thermal + Flicker)
M1	1.46 + 0.05 = 1.51 (Thermal + Flicker)
M7	0.00
M8	0.00
M5	0.01
M6	0.01
M00	0.00
M01	0.00
M0	0.00
M11	0.00
M12	0.00
M13	0.00
M14	0.00
MC0	0.00
MC1	0.00
MC2	0.00
MC3	0.00
MC4	0.00
M0x	0.00
M3x	0.00
M4x	0.00
Rcm	0.00
RL	0.00

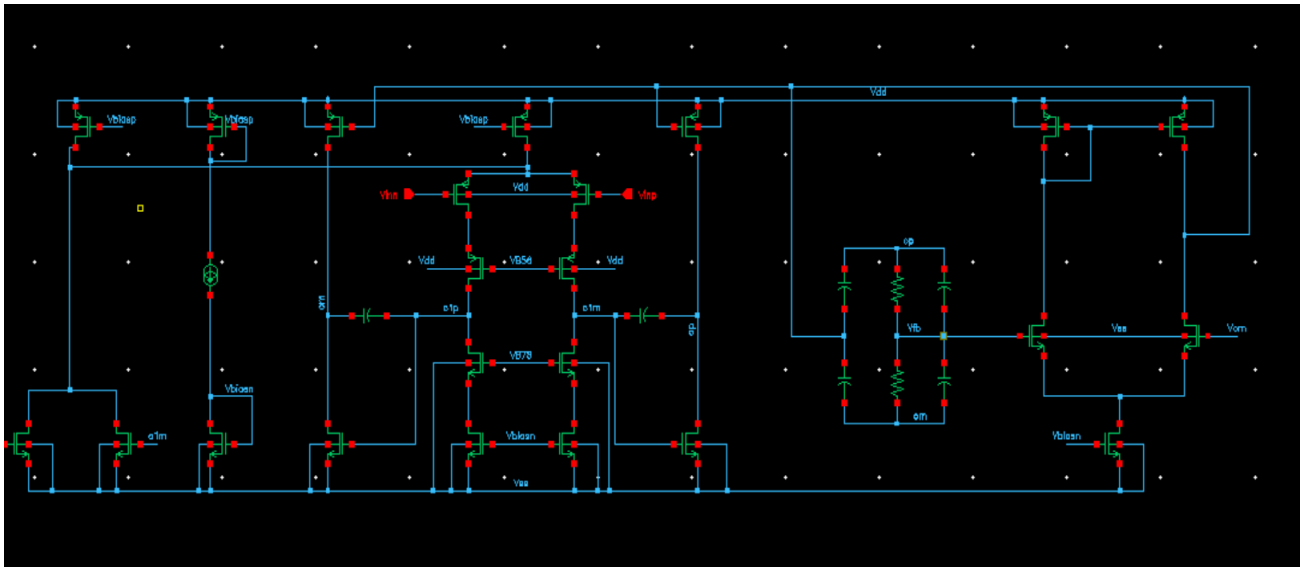
Note : The above are with respect to the MOSFET numbering as in the problem definition.

Circuit Diagram of the Fully Differential Opamp



The first stage is a telescopic cascode stage. A pMOS differential pair in the first stage and an nMOS common-source amplifier in the second stage is used in the design. Each of the two stages has a common mode feedback circuit of its own. CMFB1 is the Common Mode Feedback Circuit for the first stage. CMFB2 is the Common Mode Feedback Circuit for the second stage.

Schematic



The above schematic has been used for the Fully Differential Opamp and the simulator used is Cadence Virtuoso.

3. **Plots (for the inverting amplifier)** :

a. Loop Gain Magnitude and Phase

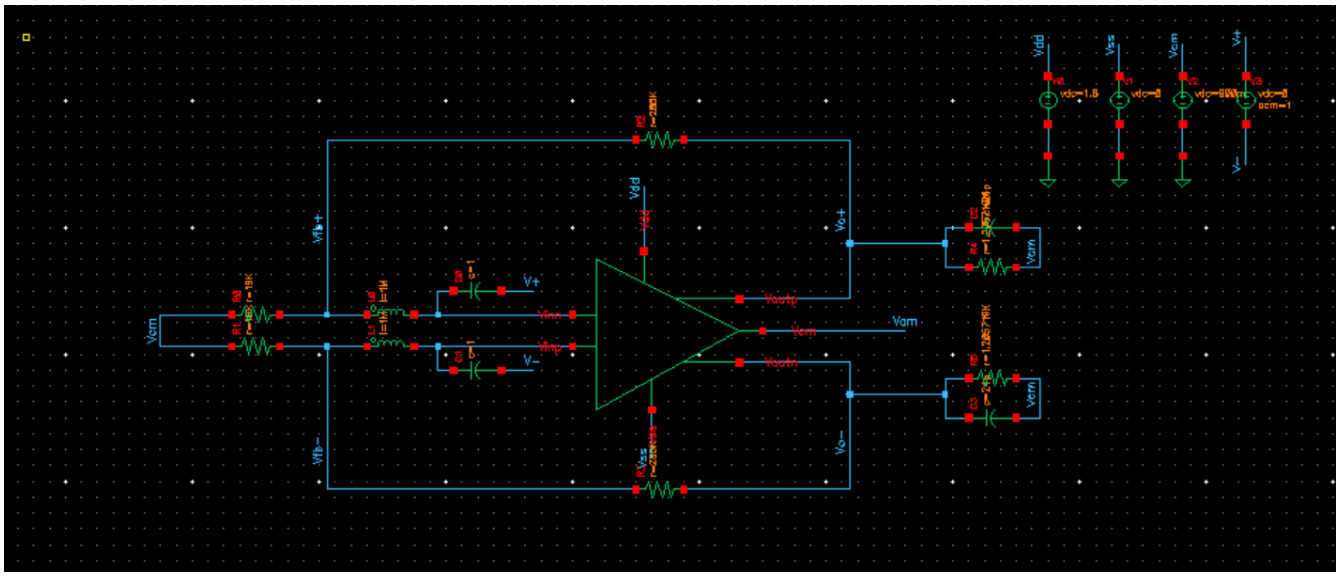


Fig 1 : Loop Gain Test Bench Schematic

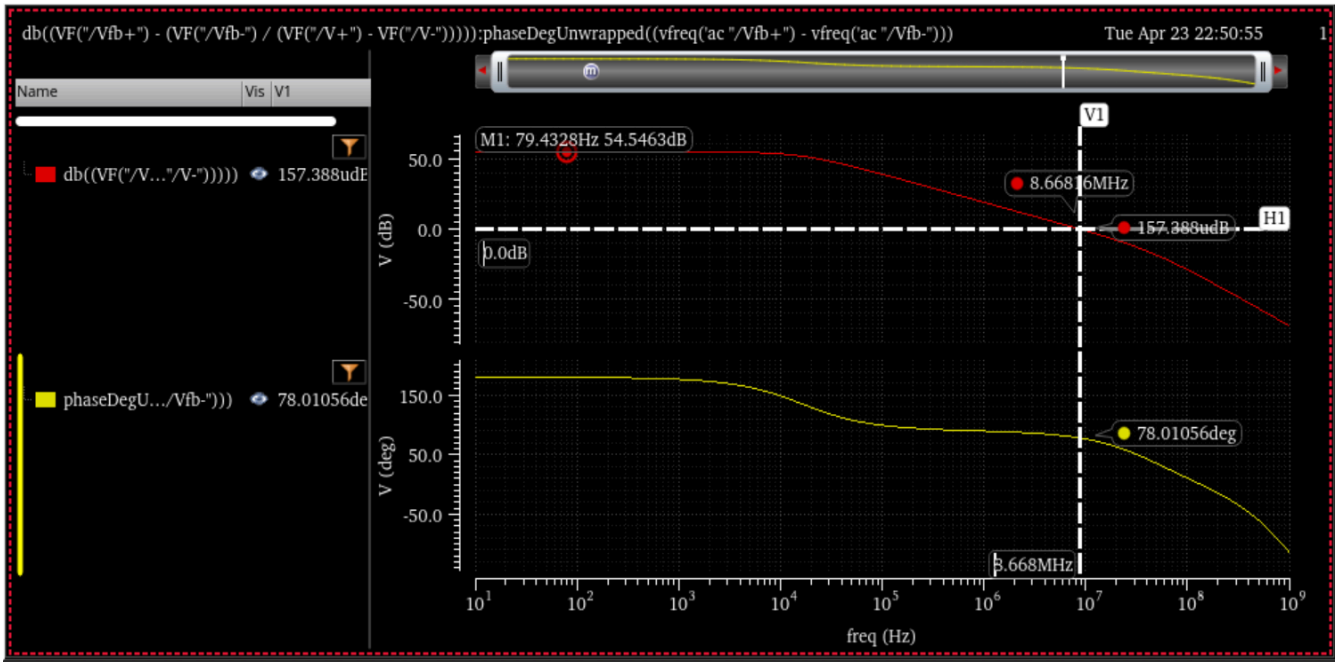


Fig 2 : Loop Gain Magnitude and Phase Plot

The observed unity loop gain frequency is close to 8.668 MHz and the phase margin at this frequency is equal to 78.0105 degrees. The DC loop gain magnitude is 54.5436 dB.

b. Closed Loop DC gain and 3-dB bandwidth

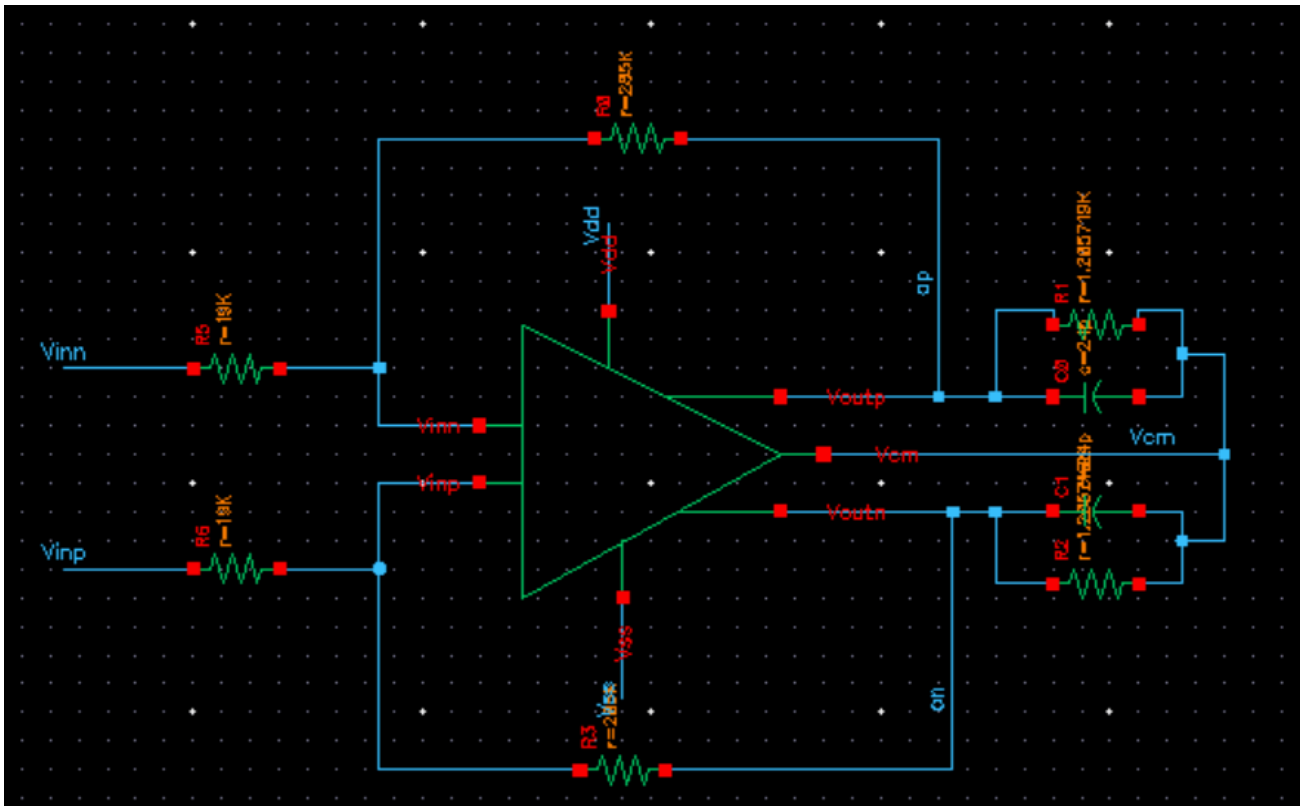


Fig 3 : Closed Loop DC Test Bench Schematic

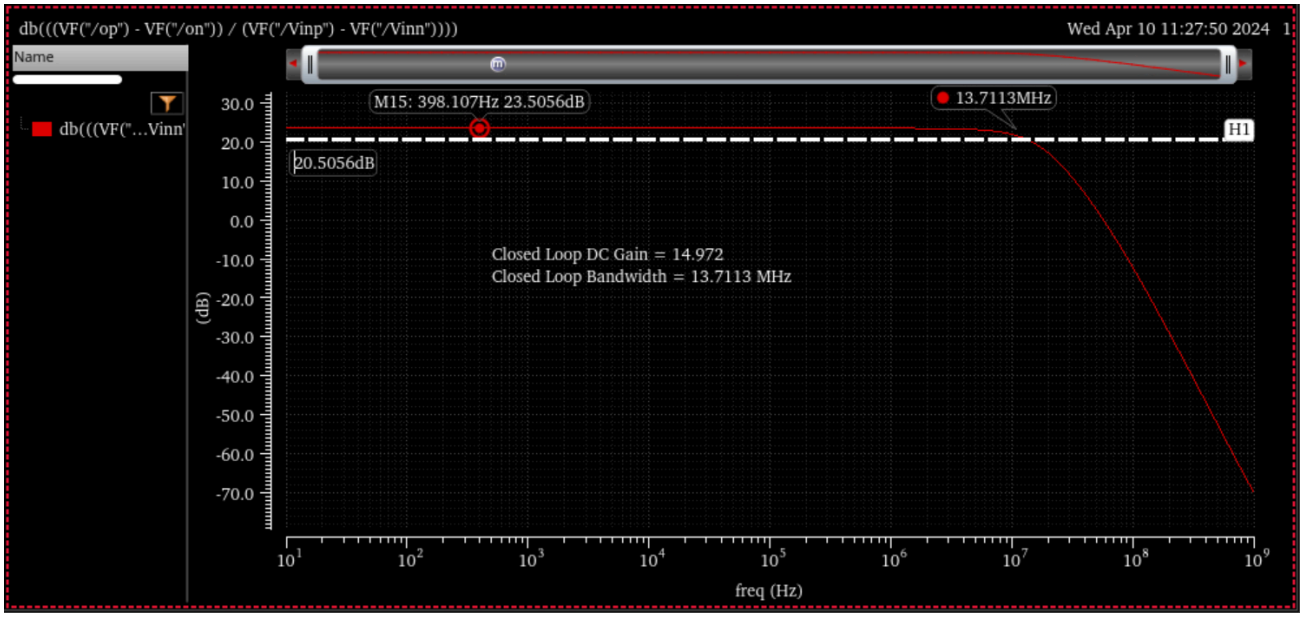


Fig 4 : Closed Loop DC gain and 3-dB bandwidth

The observed closed loop DC gain is 23.5056 dB which corresponds to 14.97 (specification : 15). The observed 3-dB bandwidth is 13.7113 MHz which exceeds the specification of 11 MHz.

c. Closed Loop DC transfer curve

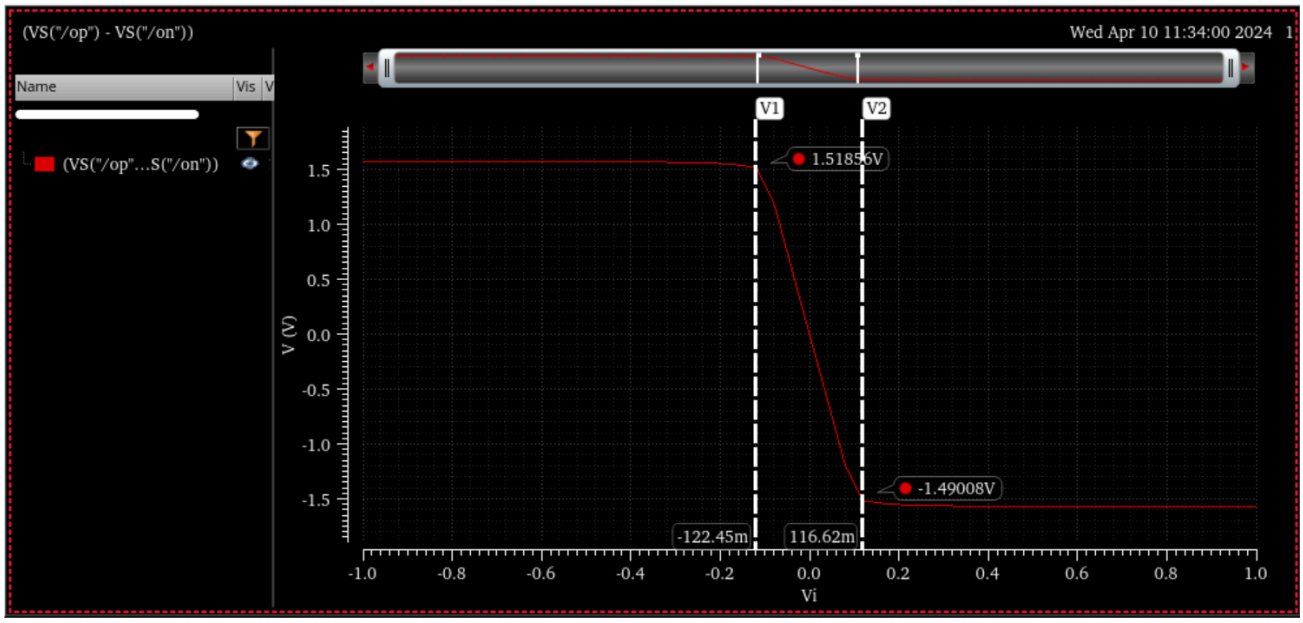


Fig 5 : Closed Loop DC Transfer Curve

The x axis shows the large signal input differential voltage which is varied from -1V to 1V. The common mode is set at 900 mV. In effect, the input voltage varies from 0.4 V to 1.4 V at both the input terminals of the Opamp. The y axis shows the large signal output differential voltage which is observed to go from 1.57 V to -1.57 V as the large signal input differential voltage is increased as shown in the graph above. The opamp is observed to be linear in the input differential voltage range of **-122.45 mV** to **116.62 mV**, i.e. from **838.775 mV to 958.31 mV** the opamp is linear. (Vcm is set to 900 mV)

d. Small signal step response

Fig 6 : Small signal step response

The small signal step response for output stepping from 0 to 0.1 volts is shown in Fig. 6. The rise time used for the step input is 100 ps. Since closed loop gain is 15, input differential input is 6.67 mV.

e. Large Signal step response

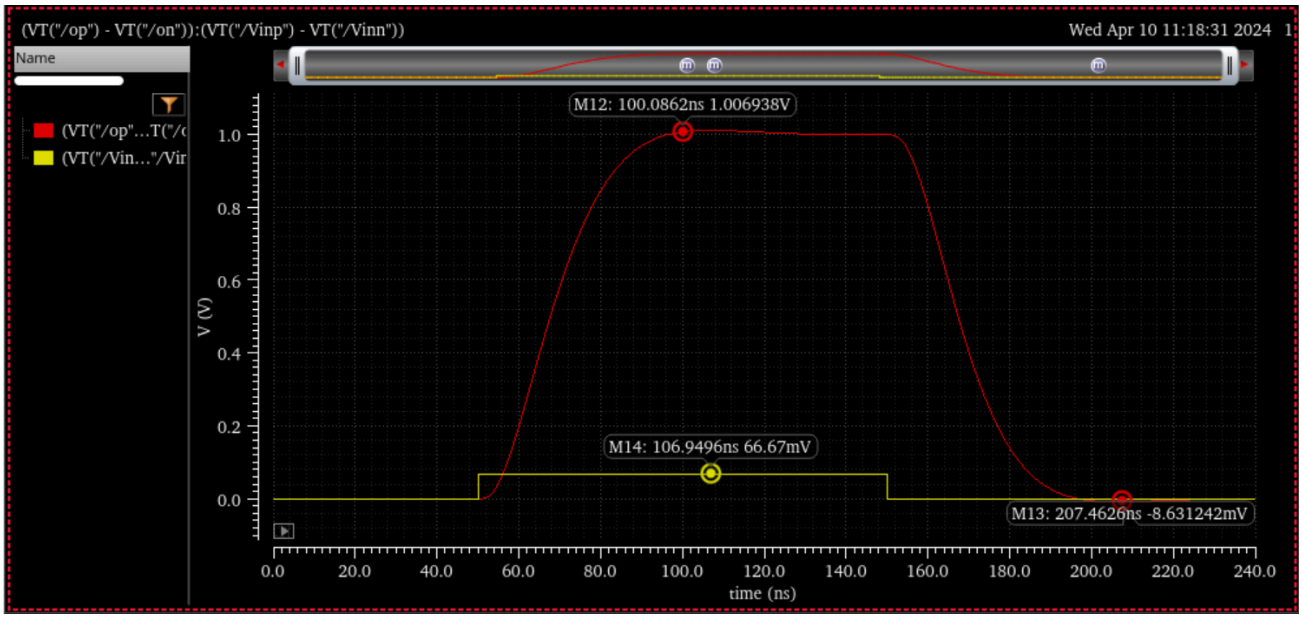


Fig 7 : Large signal step response

The large-signal step-response for input stepping from 0 volts to 1 volts is shown in Fig. 7. The rise time used for the step input is equal to 100 ps. Since closed loop gain is 15, input differential input is 66.67 mV.

f. Output Noise PSD and Input Noise PSD of the closed loop amplifier

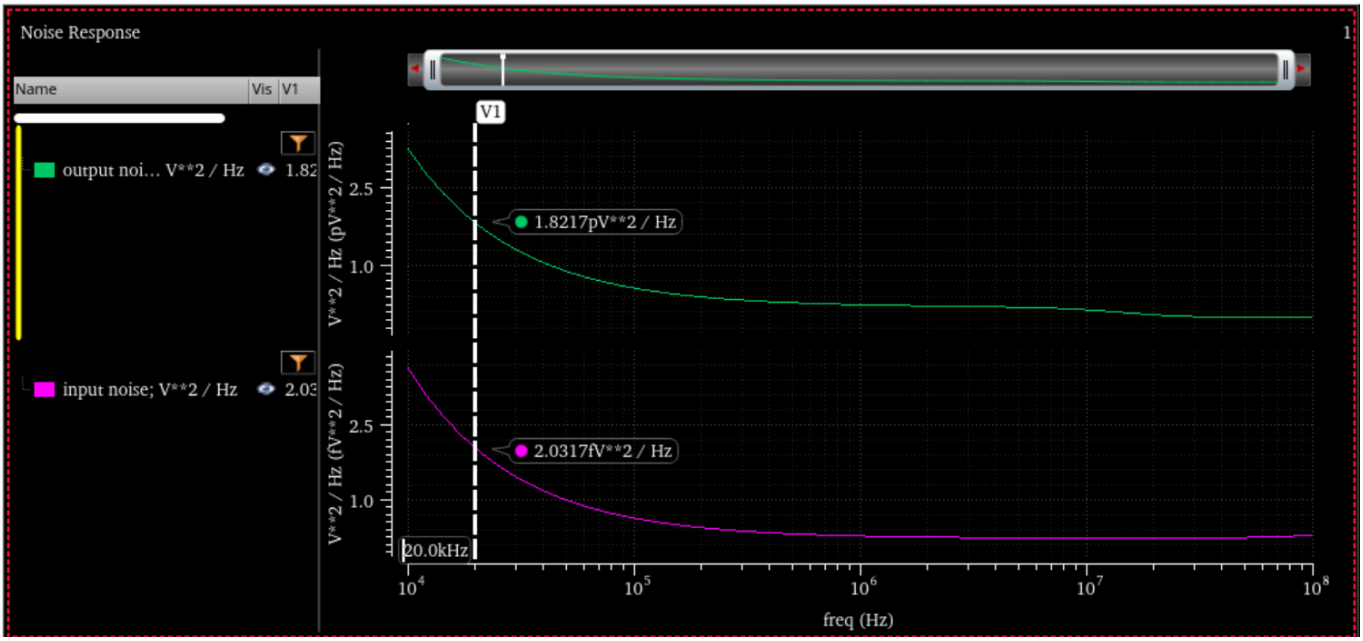


Fig 8 : Output (pV^2/Hz) and Input (fV^2/Hz) Noise PSD of the Closed Loop Amplifier

g. Input Referred Noise of the Opamp

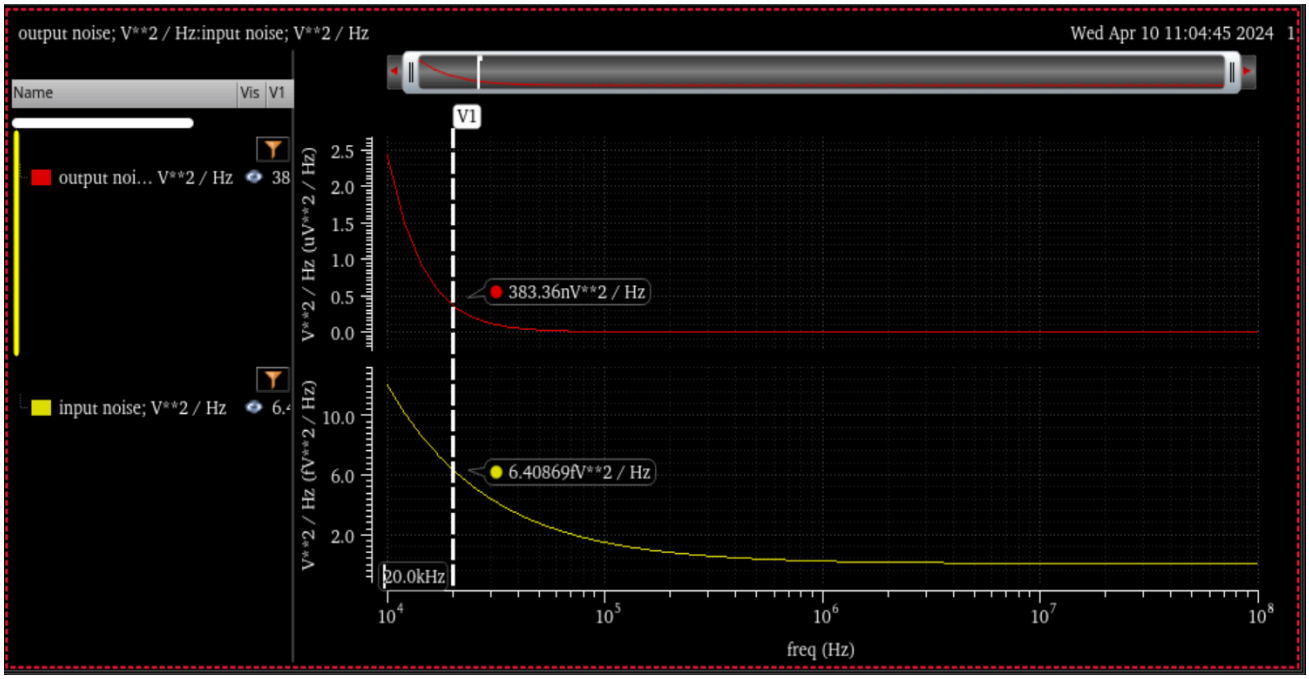


Fig 9 : Output (μV^2/Hz) and Input (fV^2/Hz) Noise PSD of the Opamp

h. Slew Rate

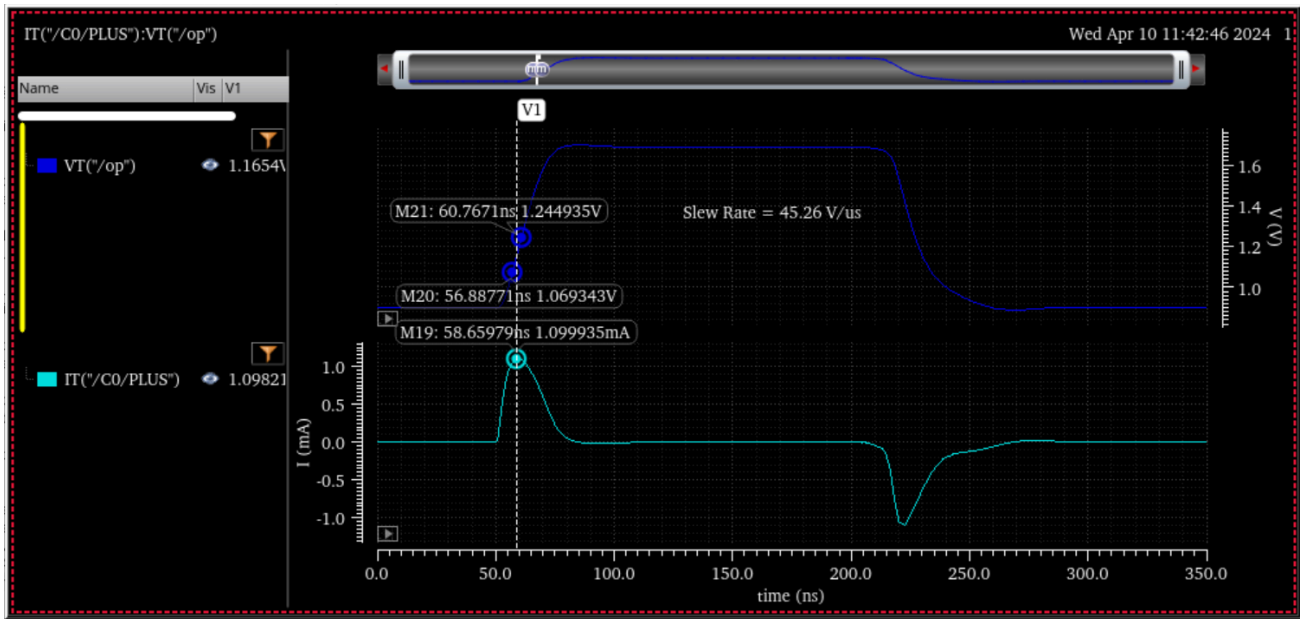


Fig 10 : Calculation of Positive Slew Rate (Vstep = 0.6 V)

The positive slew rate is calculated to be -

$$SR_+ = \frac{1.244935 - 1.069343}{60.7671 - 56.88771} * 10^3 V/\mu s = 45.262 V/\mu s$$

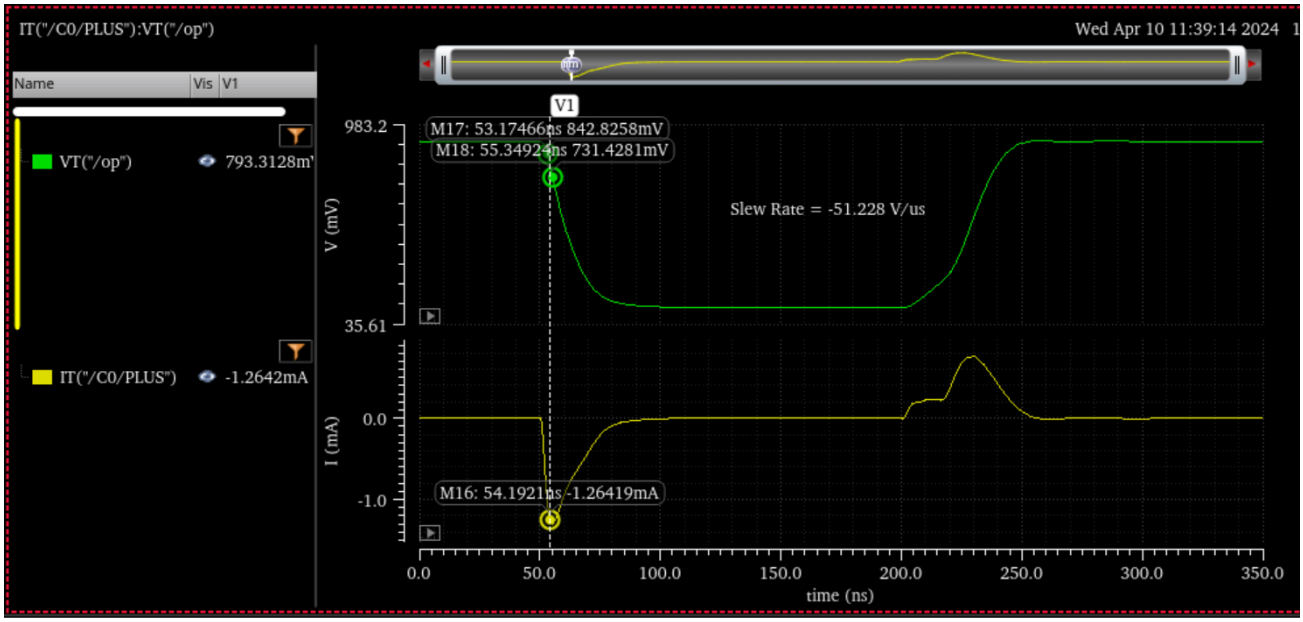


Fig 11 : Calculation of Negative Slew Rate (Vstep = -0.6 V)

The negative slew rate is calculated to be -

$$SR\_ = \frac{842.8258 - 731.4281}{53.17466 - 55.34924} * 10^0 V/\mu s = -51.228 V/\mu s$$

The slew rate was determined by applying a large step and finding the derivative of the voltage (w.r.t to time) when the load current is maximum. The positive and negative slew rates came out to be different as calculated above.

i. HD3 Calculation

Schematic

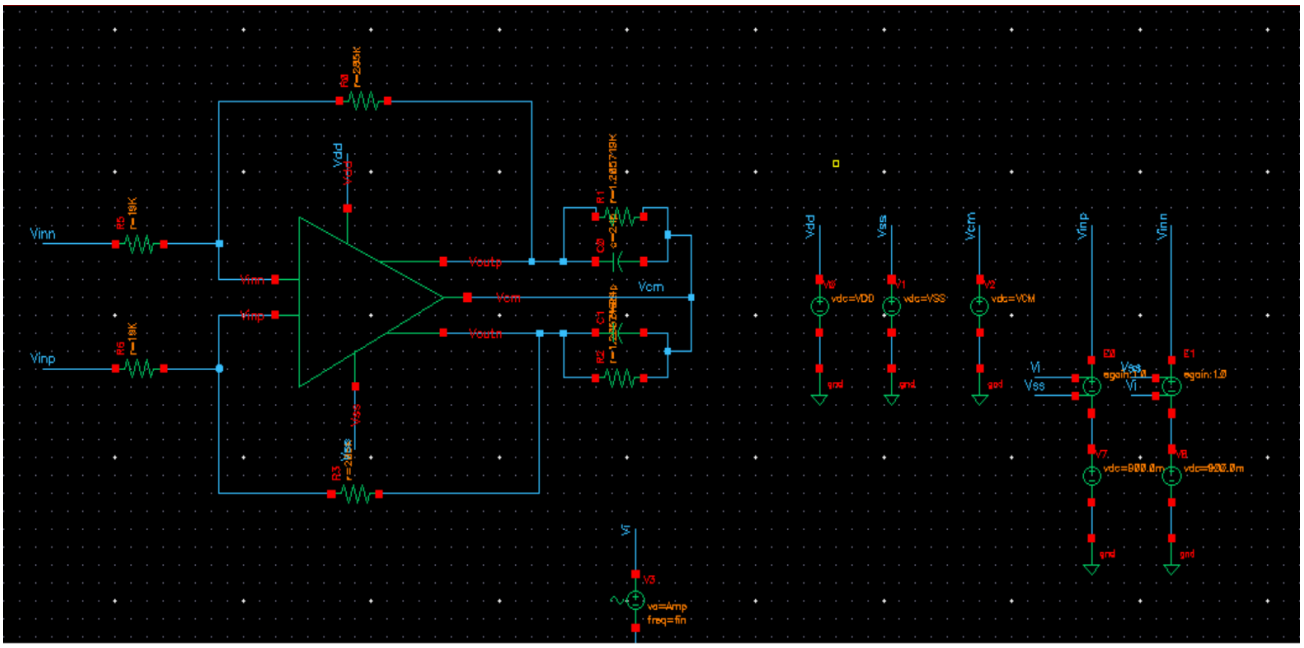


Fig 12 : Schematic for Calculating HD3

Waveforms

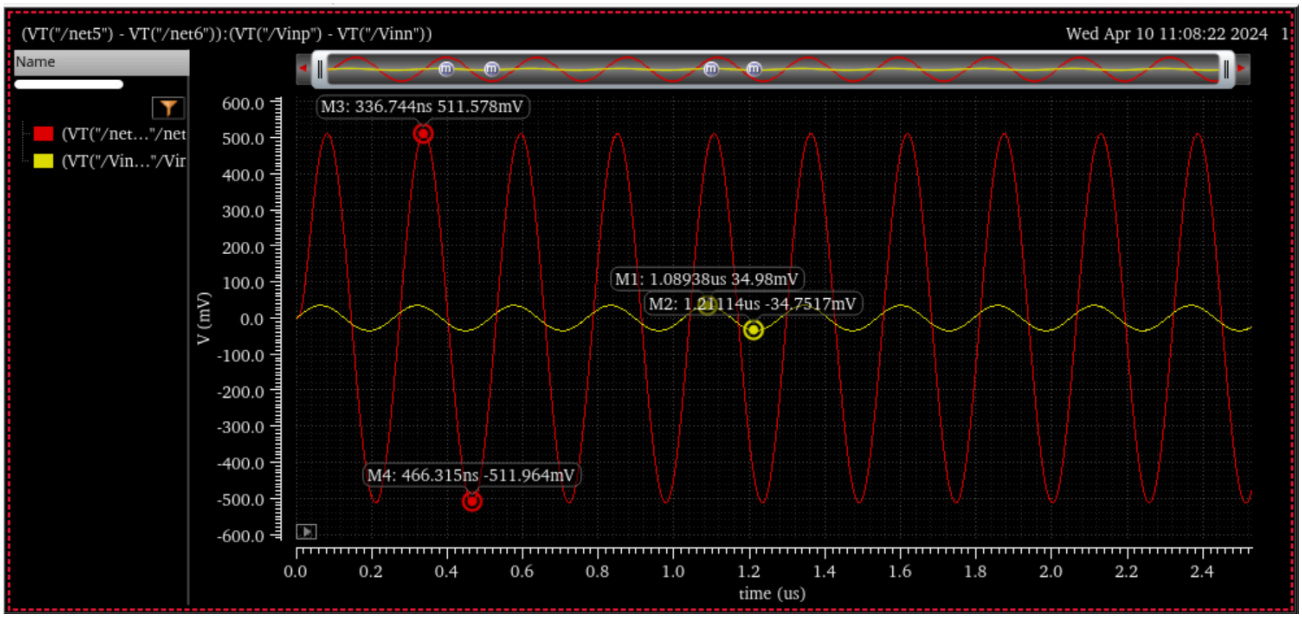


Fig 13: Input voltage applied was such that a 1V peak to peak was observed at the differential output.

Spectrum of the Output waveform

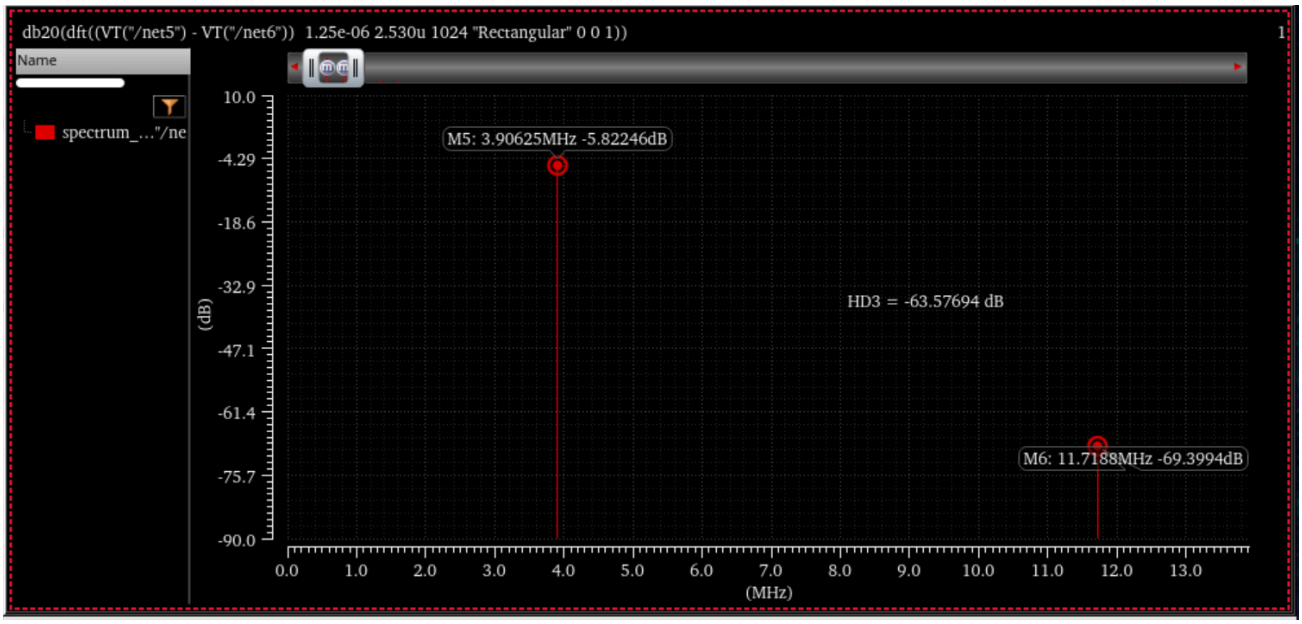


Fig 14: Spectrum of Output (for HD3 analysis)

With a 35mV sinusoidal input having frequency fin = 3.90625 MHz, Fs = 800 MHz, bin = 5, N =1024
1000 transient points have been neglected in the above simulation. Strobe period = Ts/8 is set.

The HD3 is calculated to be -

$$HD_3 = (-69.3994 - (-5.82246))dB = -63.57694dB$$

j. CMFB2 Loop Gain

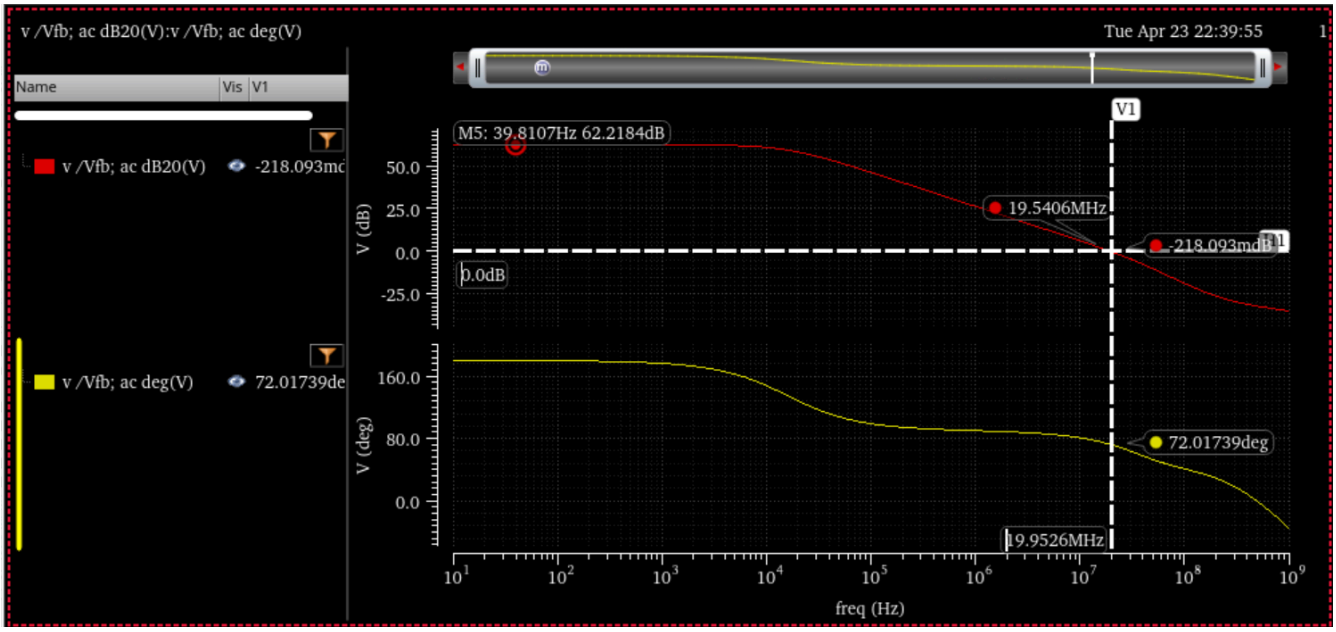


Fig 14 : CMFB2 Loop Gain Magnitude and Phase

The observed unity loop gain frequency is close to 19.9526 MHz and the phase margin at this frequency is equal to 72.01739 degrees. The loop gain magnitude is 62.2184 dB

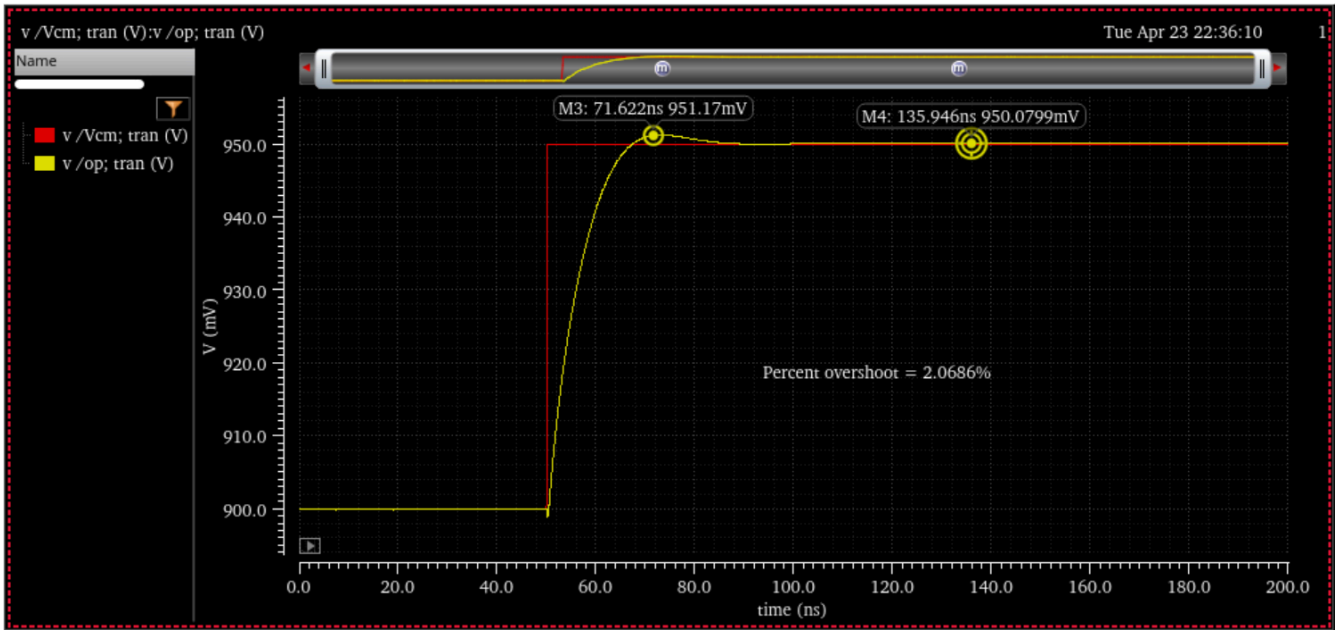


Fig 15 : Common Mode Step Response

The VCM is stepped from 900 mV to 950 mV and the common mode bias voltage at the output op is shown in Fig. 15 above. The output common mode voltage settles to 950.079 mV with an overshoot of 2.068 percent.

Note : All the above simulations can be found on

Path : ee21b019@ams117~/EE5320_Assignment_8