EE5320 : Analog IC Design
Jan - May 2024
Assignment 6

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Table showing OPAMP Parameters

Parameter	Value
Supply Voltage (Vdd)	1.8 V
Vss	0 V
Common Mode Bias (Vcm)	0.9 V
Length of all transistors (L)	0.3 μm
Width of all transistors (W)	1 μm
m00	2 (specified in the Question)
m0	40
m1 = m2 = m5 = m6	57
m3 = m4 = m7 = m8	16
m11	200
m12	65
Bias current (I00)	10 μA
VB56	600 mV
VB78	900 mV
Simulation Temperature	100 ℃
gm1	1.109 mS
gm11	9.103 mS
Cc	1 pF
RL	1205.719 Ω
CL	24 pF
k	15
Closed Loop Bandwidth	11 MHz

Table showing Simulation Results

Parameter	Obtained Value
Closed Loop DC Gain	23.505 dB (= 14.97)
Closed Loop 3-dB Bandwidth	14.0644 MHz
Unity Loop Gain Frequency	9.5216 MHz
Phase Margin	84.2797 degrees
Integrated RMS Output Noise Voltage	1.42158 mV
Opamp Open Loop DC Gain	91.063 dB (= 35739.625)
Positive Slew Rate	29.657 V/μs
Negative Slew Rate	36.498 V/μs
HD3	-43.3845 dB
Supply Voltage	1.8 V
Current Consumption	1.217 mA
Power Consumption	2.1906 mW

Table showing VDSAT results for all the MOSFETs used

Component	Observed VDSAT	Required VDSAT
M0	253.7 mV	250 mV
M1	144.4 mV	150 mV
M2	144.5 mV	150 mV
M3	146.2 mV	150 mV
M4	136.5 mV	150 mV
M5	136 mV	150 mV
M6	136.7 mV	150 mV
M7	135.2 mV	150 mV
M8	146.2 mV	150 mV
M00	255.1 mV	250 mV
M11	255.9 mV	250 mV
M12	232.4 mV	250 mV

VB56 and VB78 are picked such that 50mV swing limit is permitted as described in the Assignment.

Table showing Noise Contribution results

Noise Summary - percentage contribution to noise	
Ri	70.01 %
Rf	4.67 %
First stage of the OPAMP (fn + id noise)	25.27 %
Second stage of the OPAMP	0 %
RL	0 %

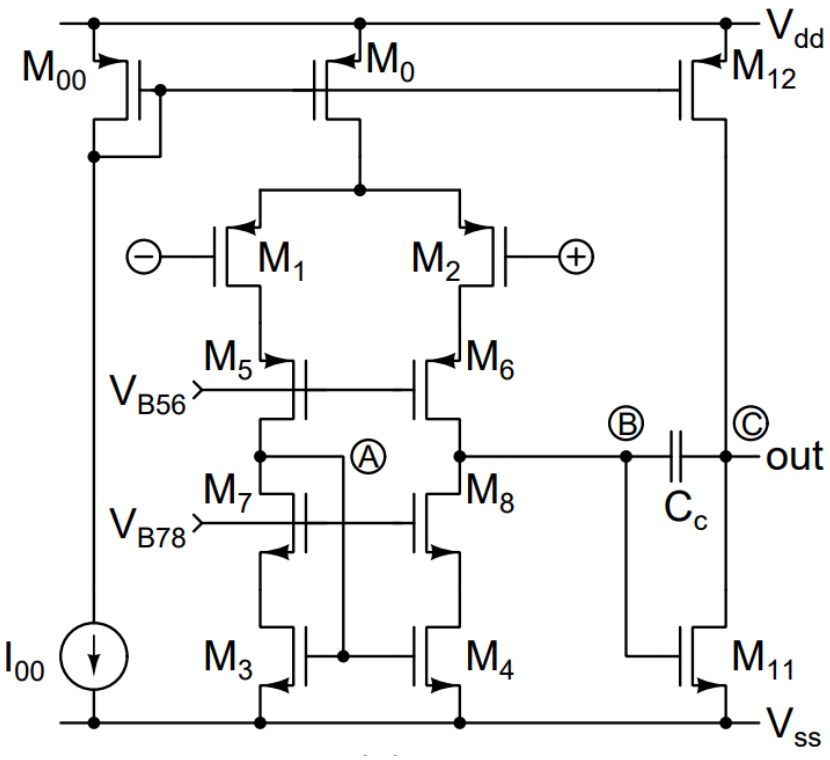
As expected, the noise from the resistors is the maximum, followed by the first stage. The second stage and the load resistor do not contribute to the overall noise. Noise has been integrated from 10 KHz to 100 MHz and results are presented.

Table showing Individual Noise Contribution results

Component Name	Contribution to Noise
Ri	70.01
kRi	4.67
M4	7.27 + 2.76 = 10.03 (Flicker + Thermal)
M3	7.25 + 2.75 = 10.00 (Flicker + Thermal)
M2	2.59 + 0.08 = 2.67 (Thermal + Flicker)
M1	2.41 + 0.08 = 2.49 (Thermal + Flicker)
M7	0.01
M8	0.01
M5	0.01
M6	0.00
M00	0.04
M0	0.05
M11	0.00
M12	0.00
RL	0.00

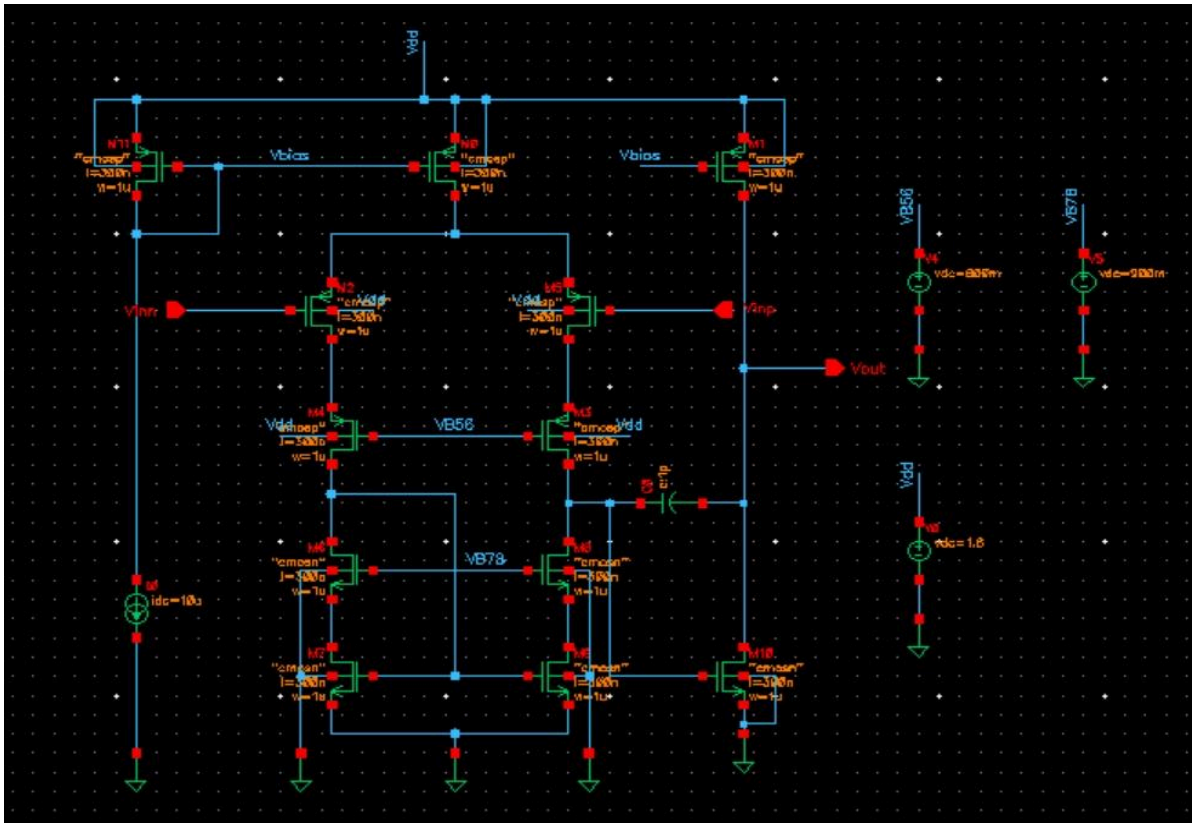
Note : The above are with respect to the MOSFET numbering as in the problem definition.

Circuit Diagram of the Telescopic Opamp



The first stage is a telescopic cascode stage. A pMOS differential pair in the first stage and an nMOS common-source amplifier in the second stage is used in the design.

Schematic



The above schematic has been used for the Opamp and the simulator used is Cadence Virtuoso.

3. **Plots (for the inverting amplifier)** :

a. Loop Gain Magnitude and Phase

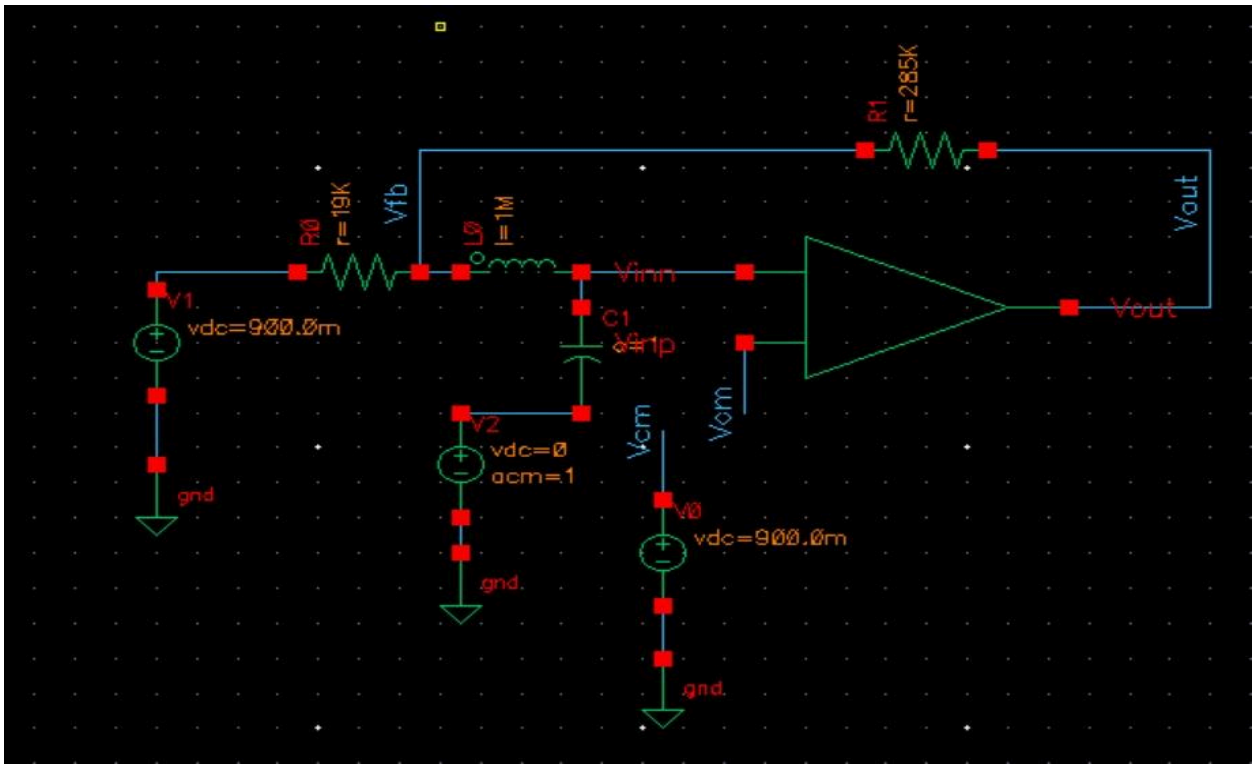


Fig 1 : Loop Gain Test Bench Schematic

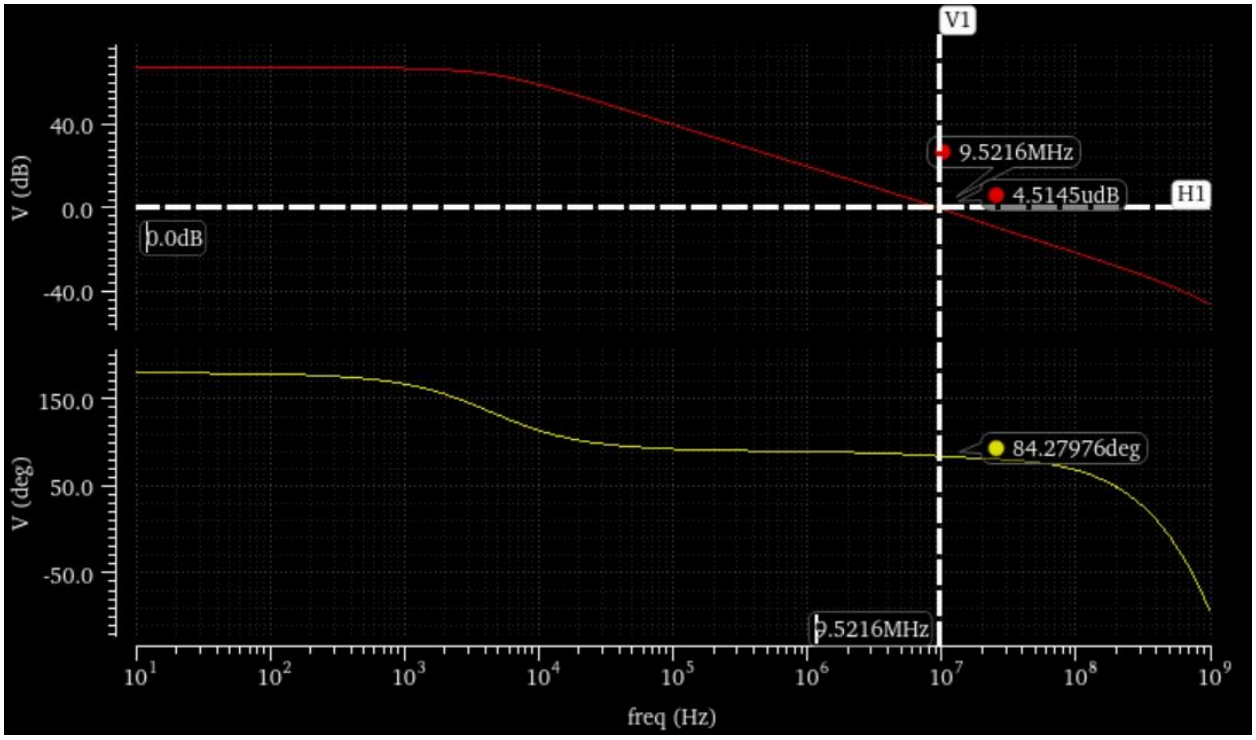


Fig 2 : Loop Gain Magnitude and Phase Plot

The observed unity loop gain frequency is close to 9.5216 MHz and the phase margin at this frequency is equal to 84.2797 degrees. The DC loop gain magnitude is 66.93 dB.

b. Closed Loop DC gain and 3-dB bandwidth

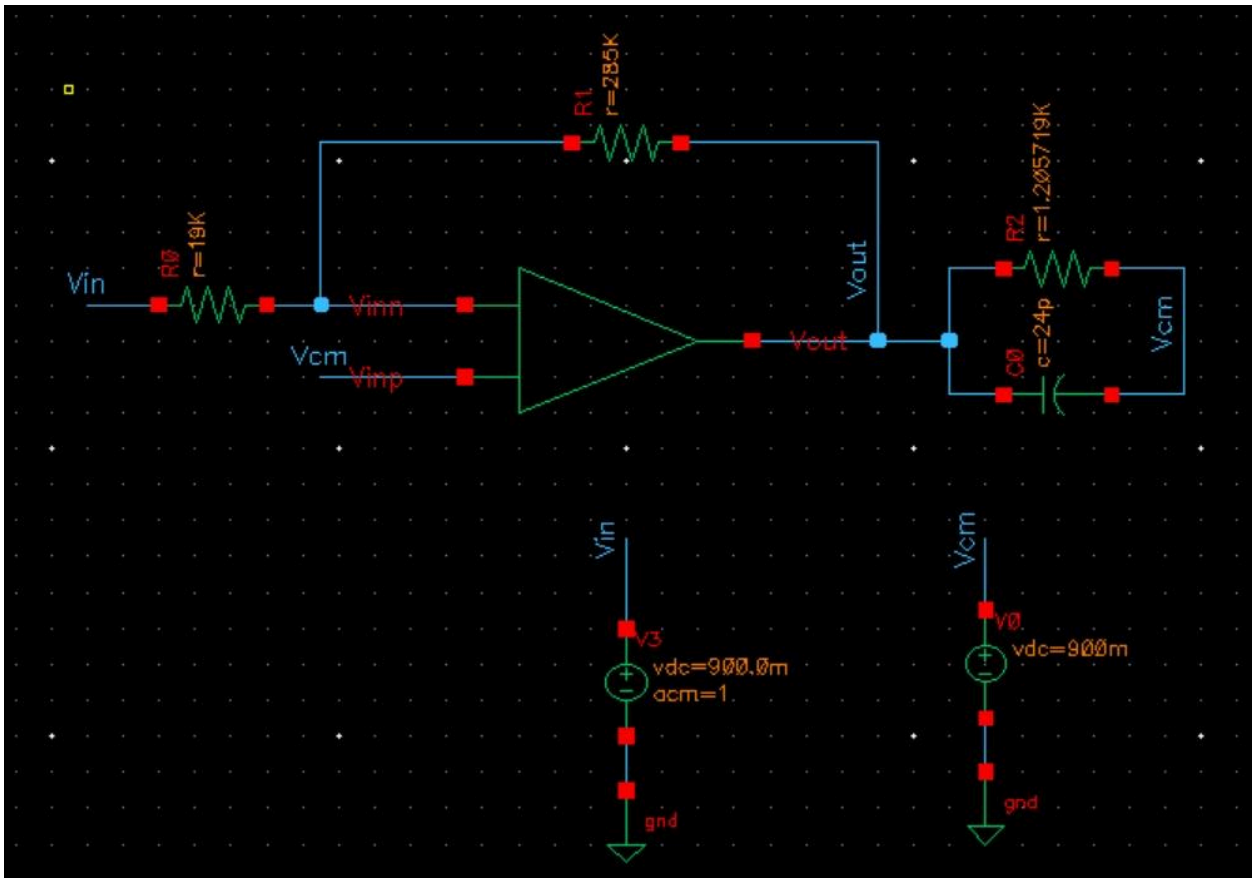


Fig 3 : Closed Loop DC Test Bench Schematic

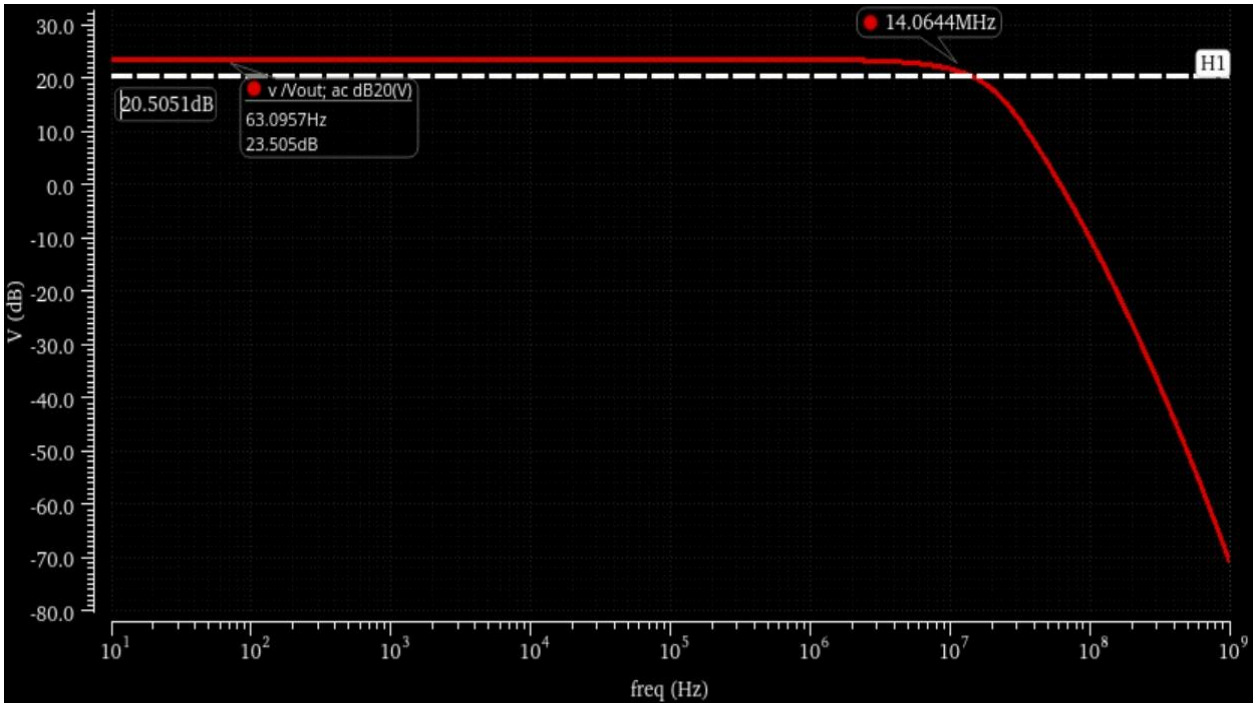


Fig 4 : Closed Loop DC gain and 3-dB bandwidth

The observed closed loop DC gain is 23.505 dB which corresponds to 14.97 (specification : 15).
The observed 3-dB bandwidth is 14.0644 MHz which exceeds the specification of 11 MHz.

c. Closed Loop DC transfer curve

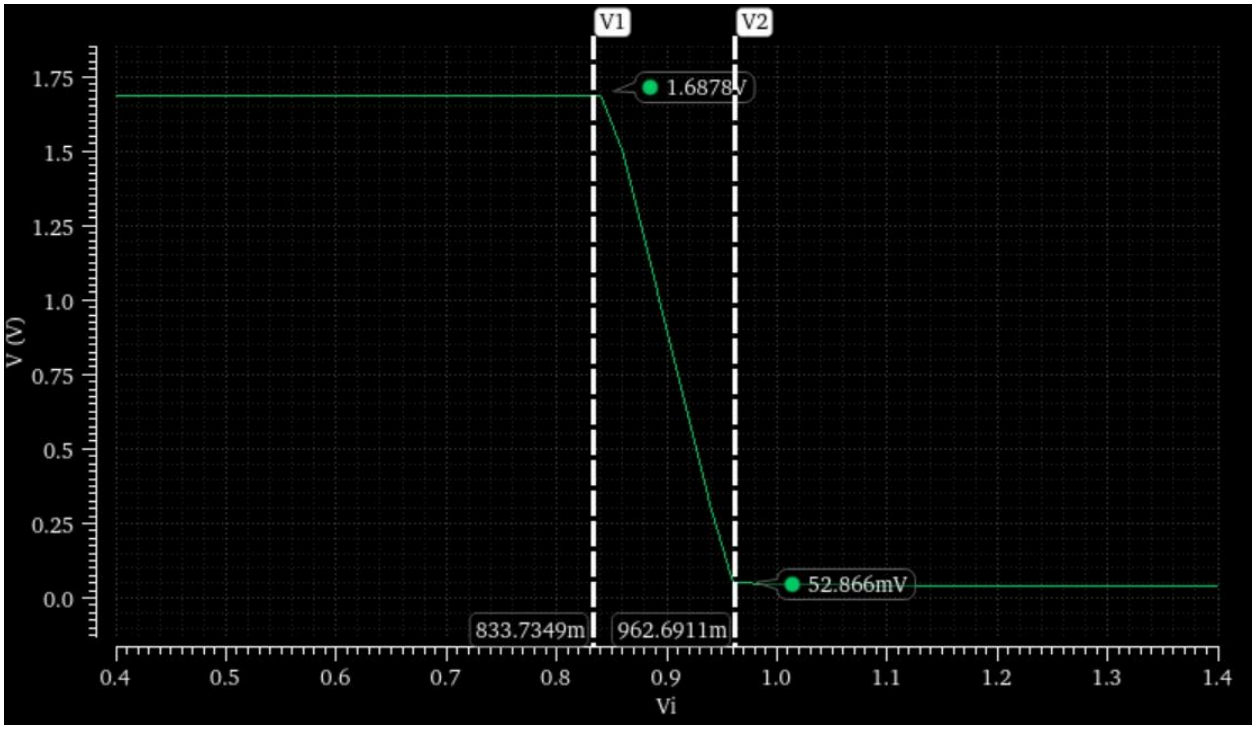


Fig 5 : Closed Loop DC Transfer Curve

The x axis shows the large signal input voltage which is varied from Vcm - 0.5 V (=0.4 V) to Vcm + 0.5 V (=1.4 V). The y axis shows the large signal output voltage which is observed to go from 1.6878 V to 52.866 mV as the large signal input voltage is increased as shown in the graph above. The opamp is observed to be linear in the input voltage range of 833.7349 mV to 962.6911 mV, i.e. from **-66.265 mV to 62.3 mV** the opamp is linear. (Vcm is set to 900 mV)

d. Small signal step response

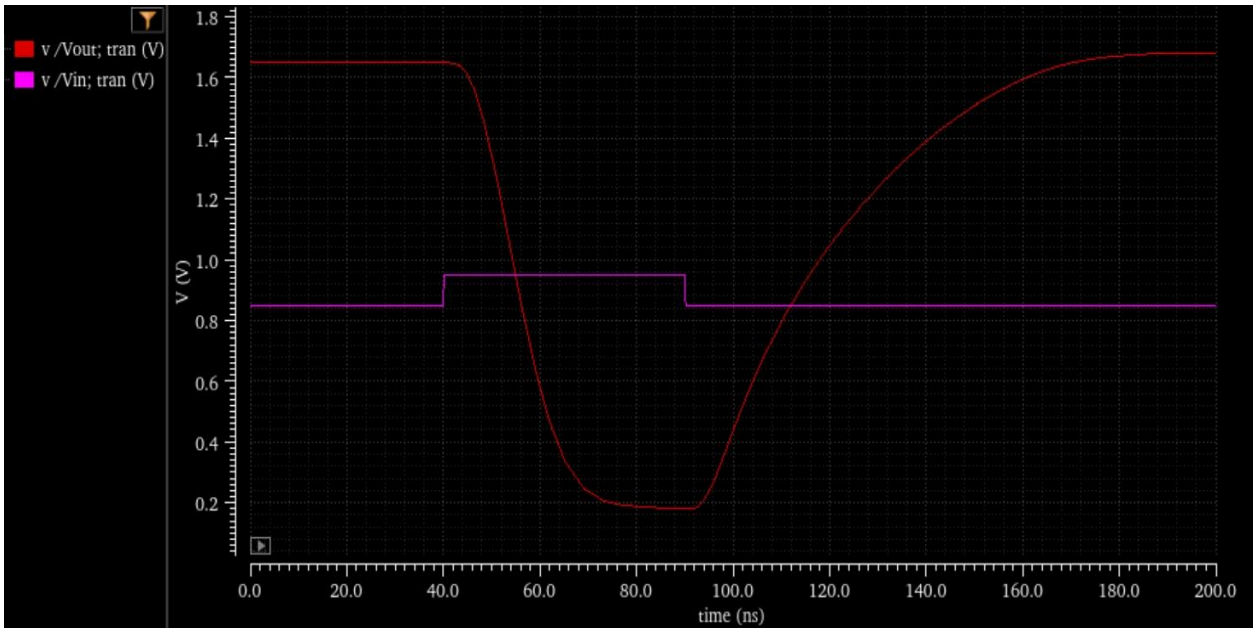


Fig 6 : Small signal step response

The small signal step response for input stepping from (Vcm-0.05) = 0.85 volts to (Vcm+0.05) = 0.95 volts is shown in Fig. 6. The rise time used for the step input is 100 ps.

e. Large Signal step response

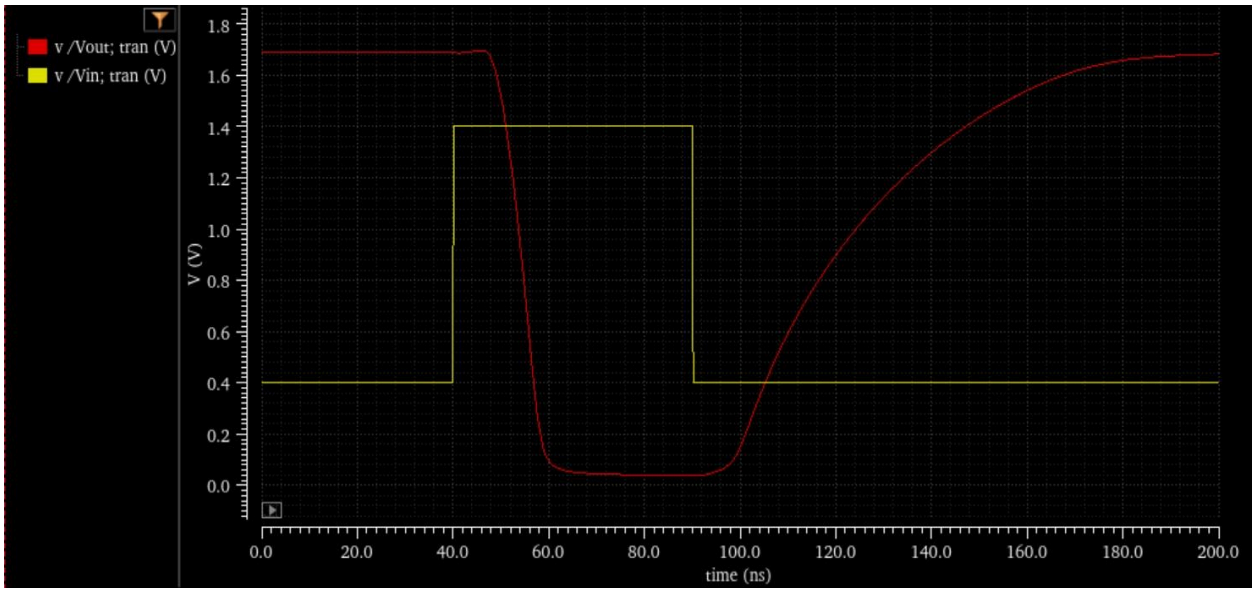


Fig 7 : Large signal step response

The large-signal step-response for input stepping from (Vcm-0.5) = 0.4 volts to (Vcm+0.5) = 1.4 volts is shown in Fig. 7. The rise time used for the step input is equal to 100 ps.

f. Output Noise PSD and Input Noise PSD of the closed loop amplifier

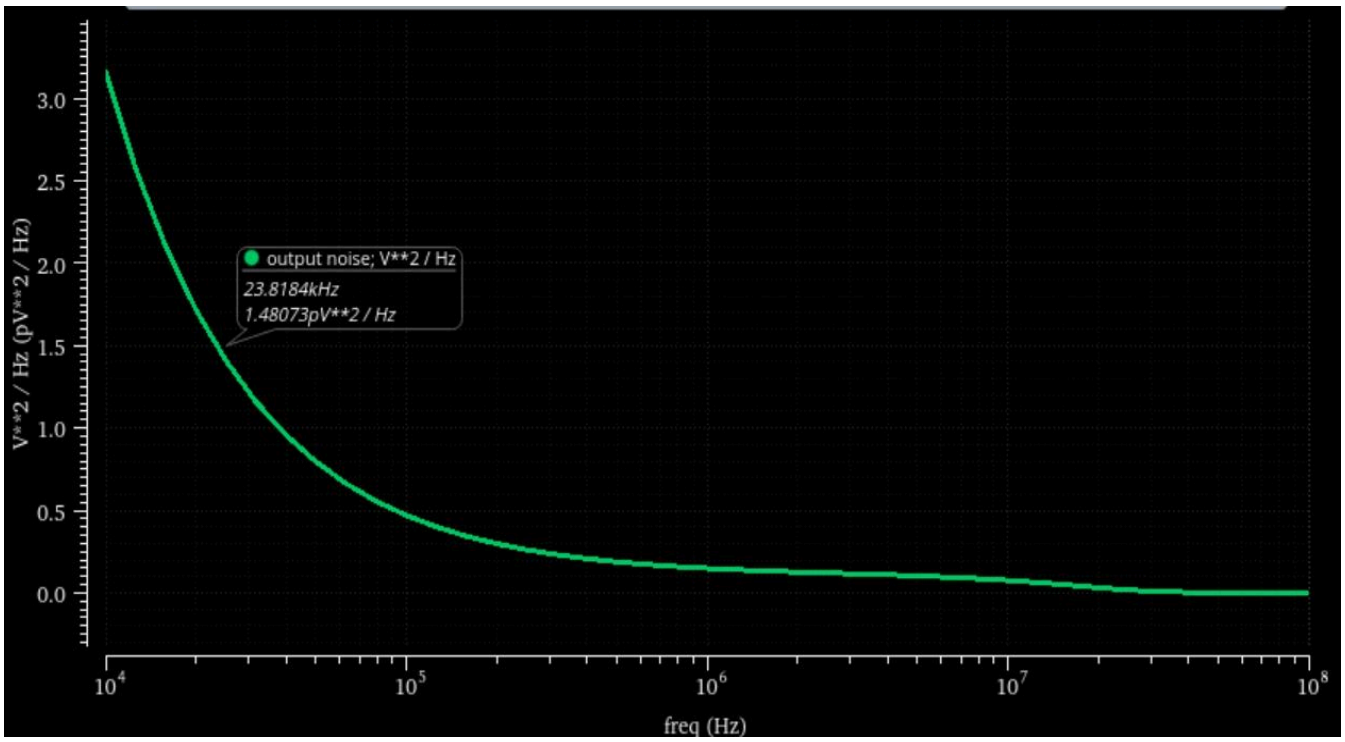


Fig 8 : Output Noise PSD of the closed loop amplifier (pV^2/Hz)

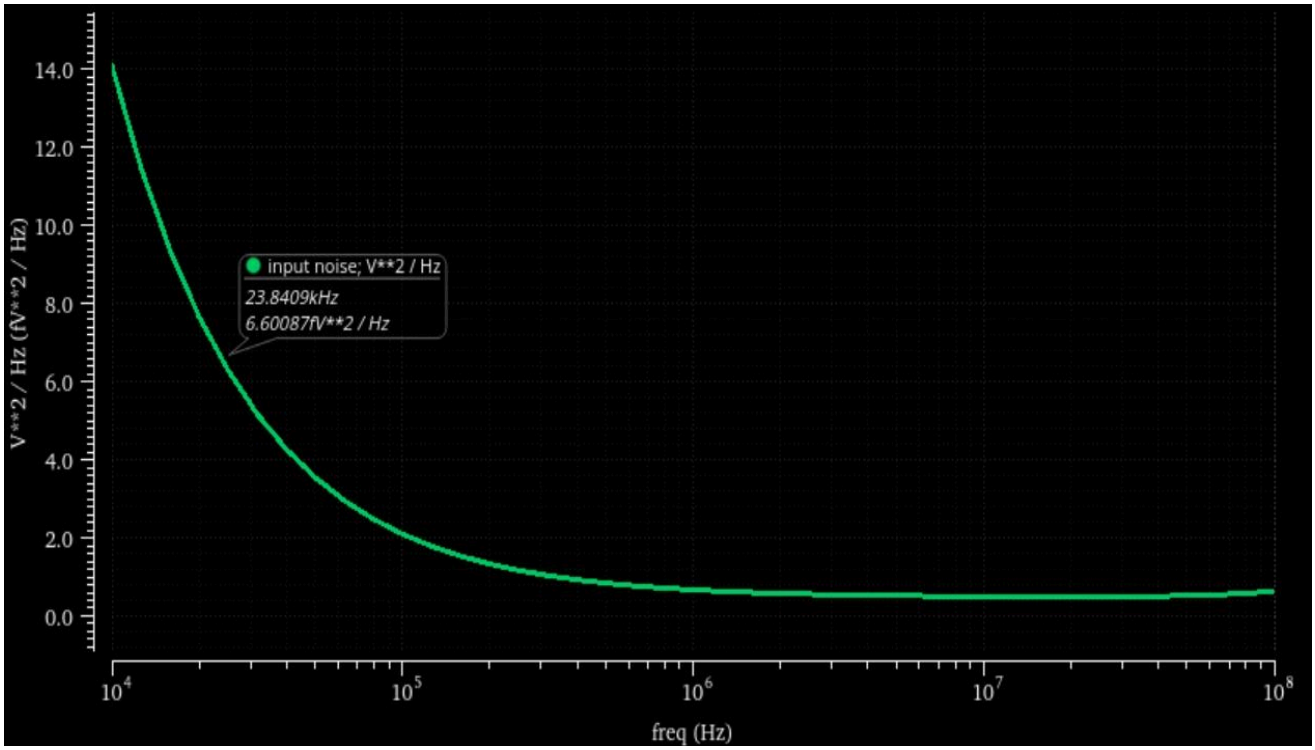


Fig 9 : Input Noise PSD of the closed loop amplifier (fV^2/Hz)

g. Input Referred Noise of the Opamp

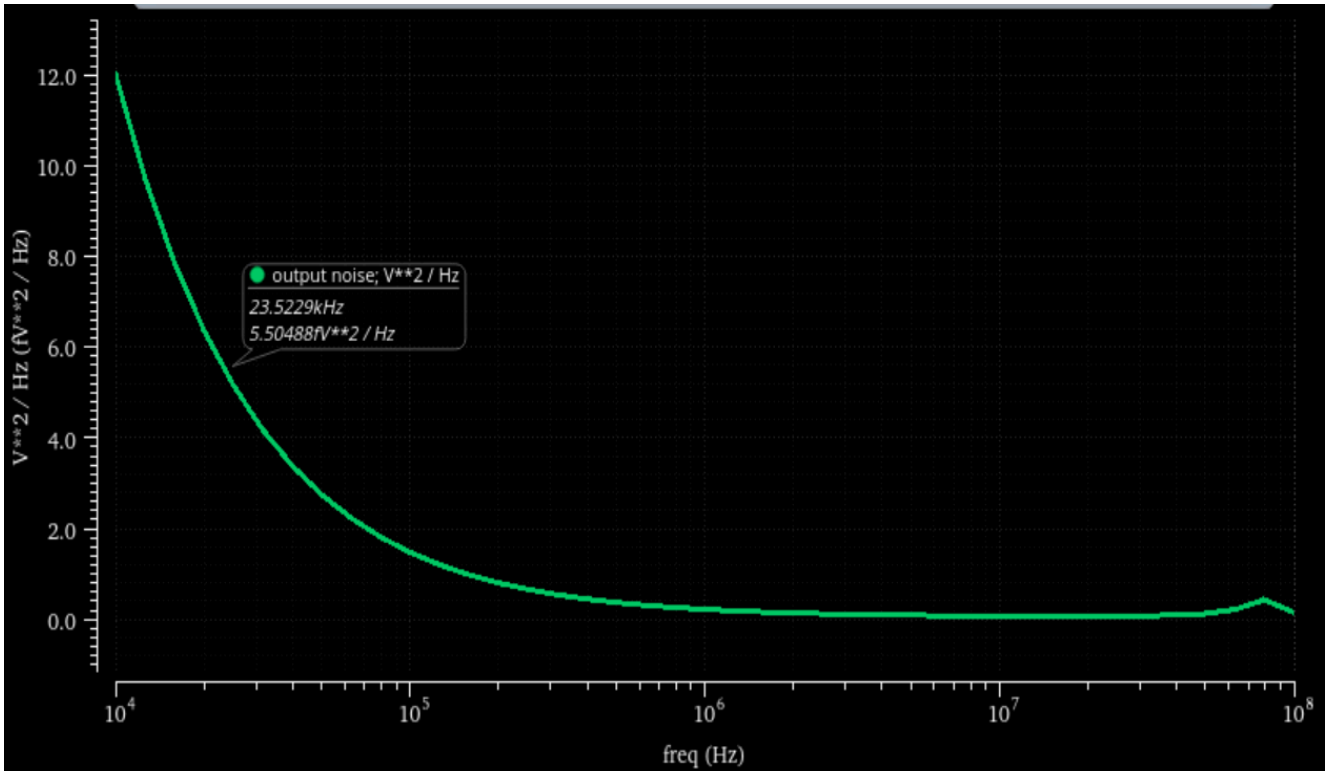


Fig 10 : Output Noise PSD of the opamp (fV^2/Hz)

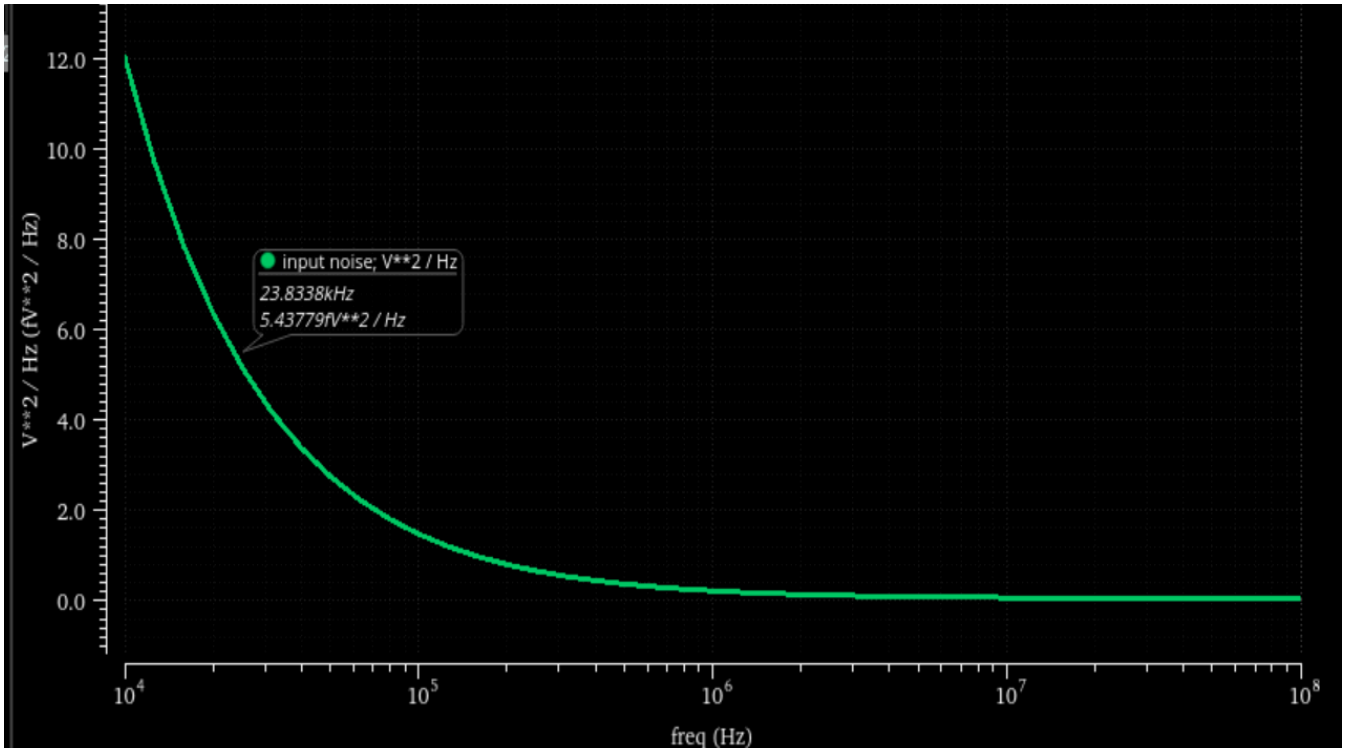


Fig 11 : Input Noise PSD of the opamp (fV^2/Hz)

h. Slew Rate

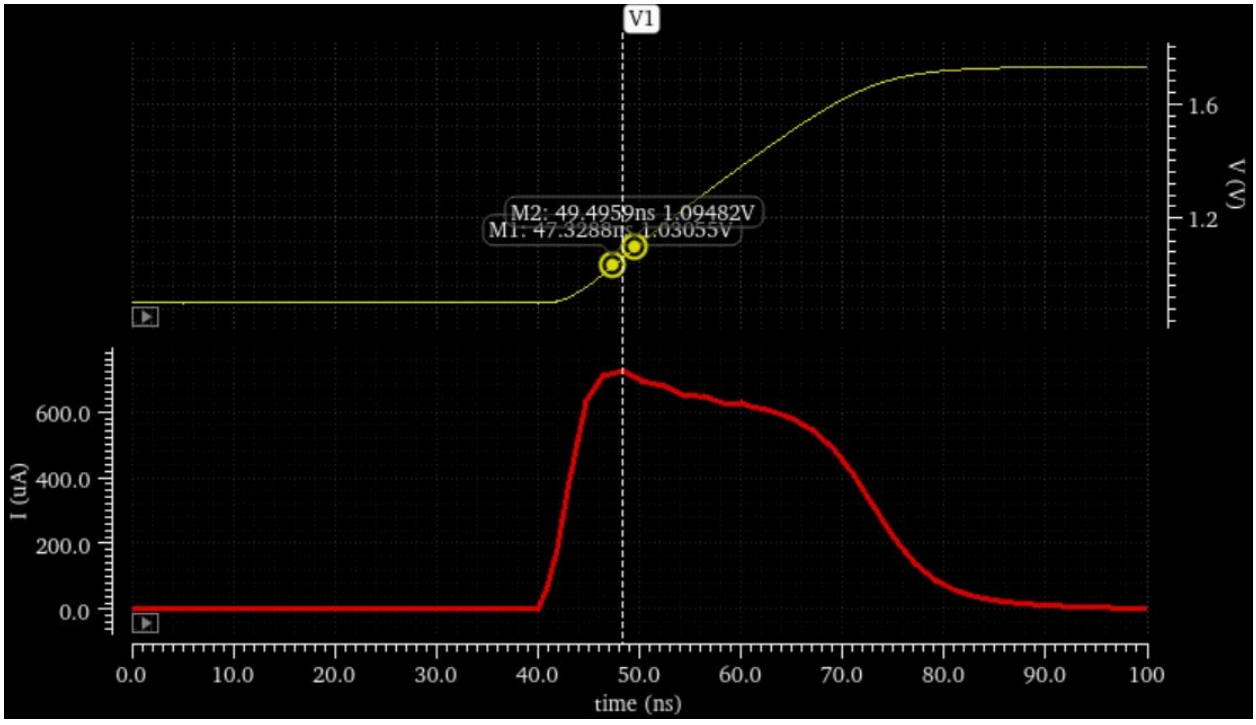


Fig 12 : Calculation of Positive Slew Rate (Vstep = 0.6 V)

The positive slew rate is calculated to be -

$$SR_+ = \frac{1.09482 - 1.03055}{49.4959 - 47.3288} * 10^3 V/\mu s = 29.657 V/\mu s$$

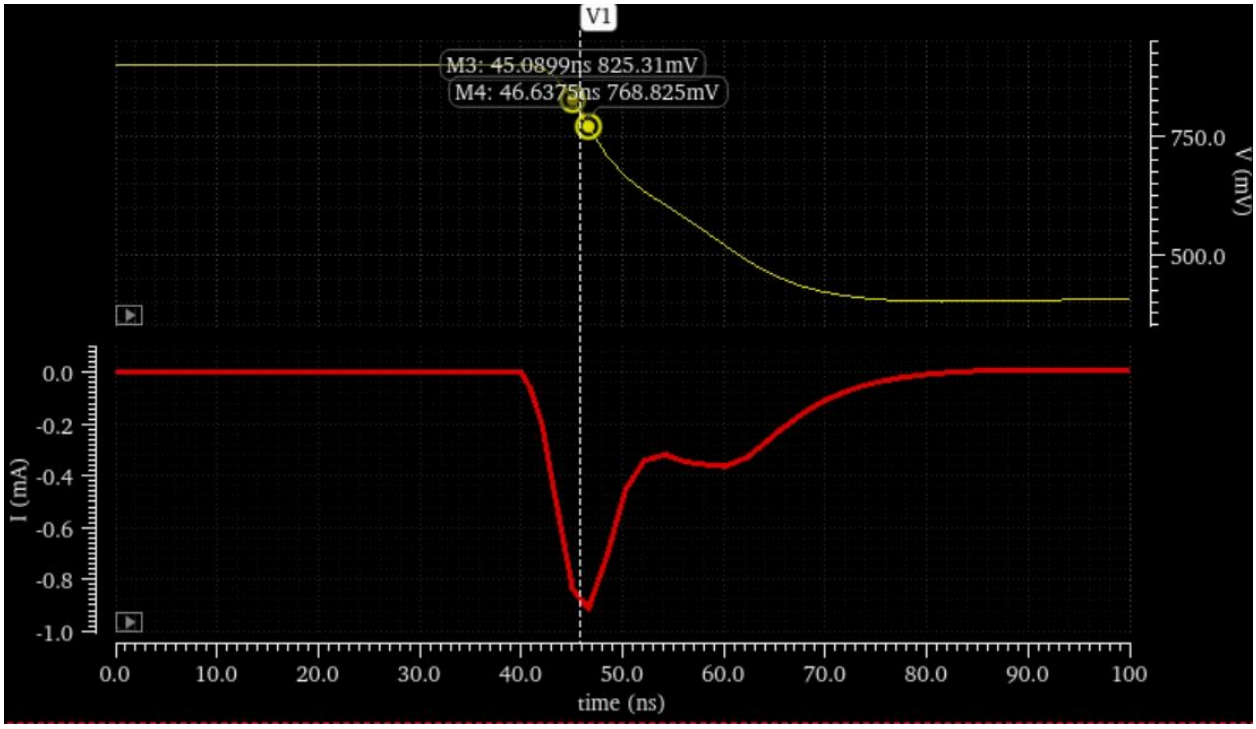


Fig 12 : Calculation of Negative Slew Rate (Vstep = -0.5 V)

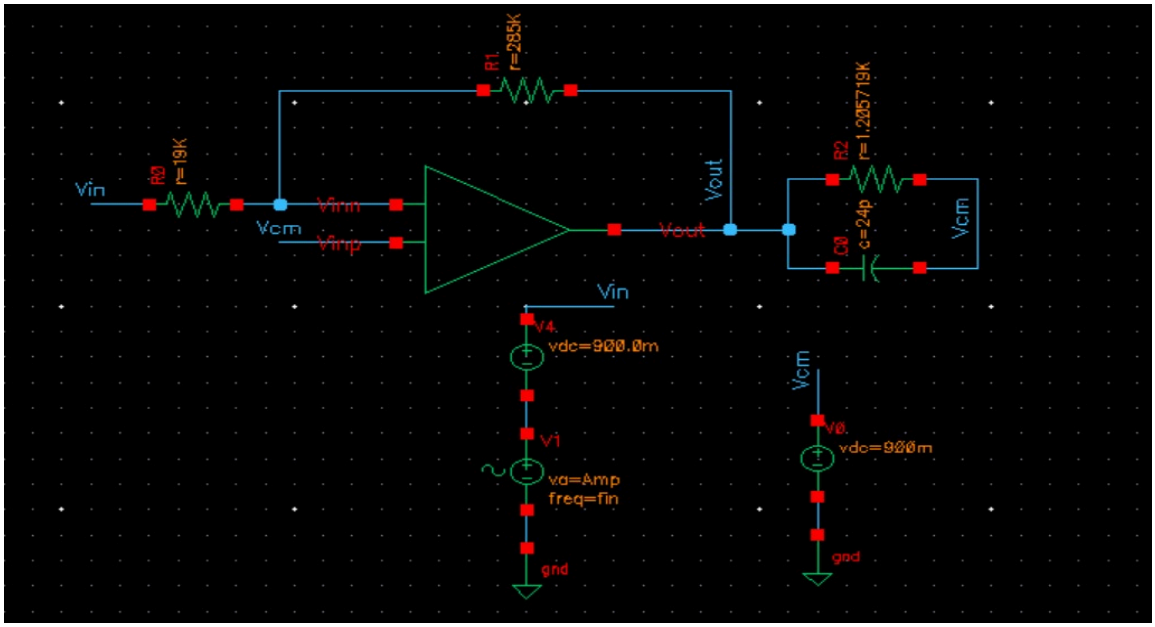
The negative slew rate is calculated to be -

$$SR\_ = \frac{825.31 - 768.825}{45.0899 - 46.6375} * 10^0 V/\mu s = -36.498 V/\mu s$$

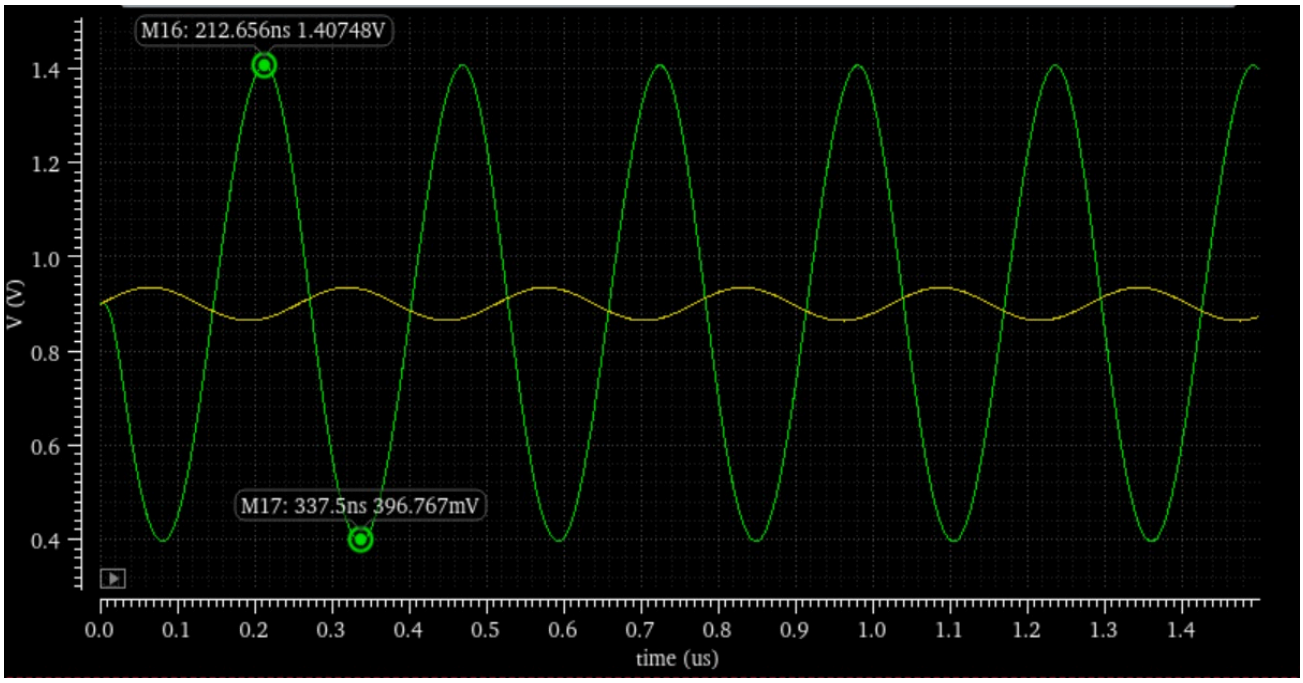
The opamp was placed in unity feedback and the slew rate was determined by applying a large step and finding the derivative of the voltage (w.r.t to time) when the load current is maximum. The positive and negative slew rates came out to be different as calculated above.

i. HD3 Calculation

Schematic

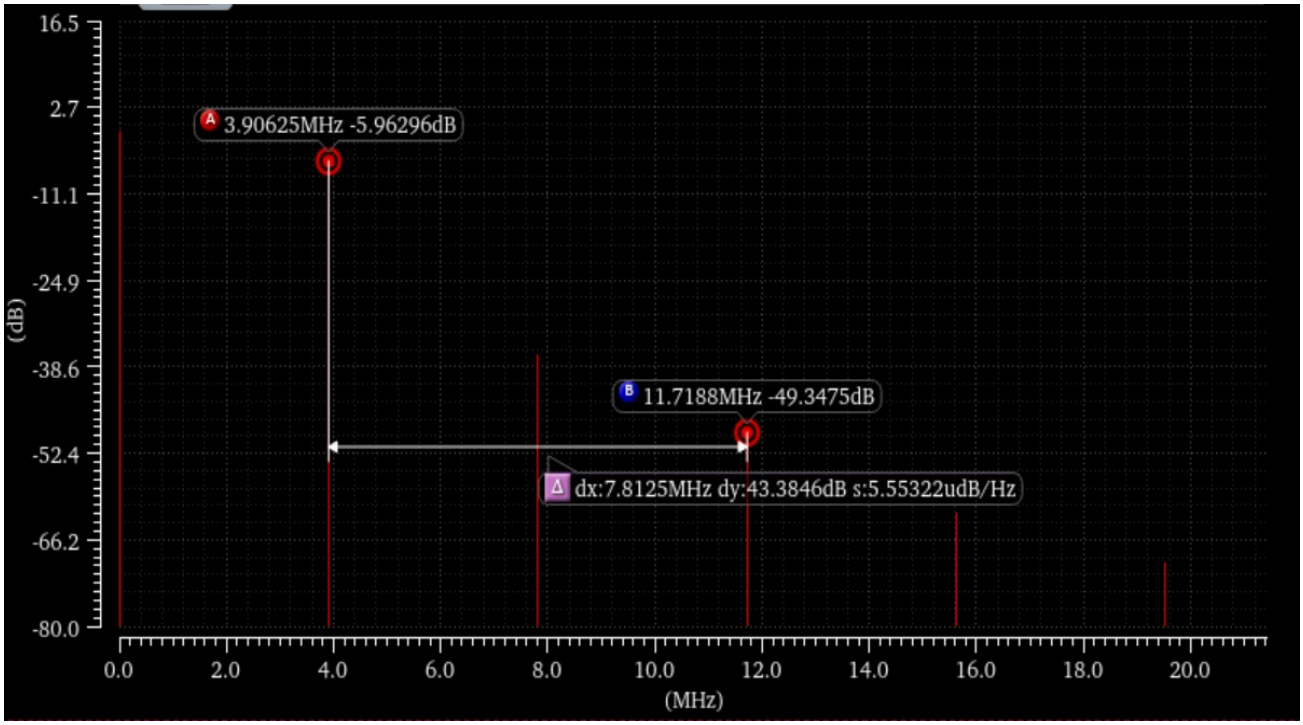


Waveforms



Input voltage applied was such that a 1V peak to peak was observed at the output.

Spectrum of the Output waveform



With a 35mV sinusoidal input having frequency fin = 3.90625 MHz, Fs = 800 MHz, bin = 5, N =1024
100 transient points have been neglected in the above simulation. Strobe period = Ts/8 is set.

The HD3 is calculated to be -

$$HD_3 = (-49.3475 - (-5.96296))dB = -43.38454dB$$

Note : All the above simulations can be found on

Path : ee21b019@ams117~/EE5320_Assignment_6