Assignment 5 (EE6347): Fall 2024

Use the FeFET model provided to answer the following questions.

1. Show the Id-Vg hysteresis of an FeFET: Apply a 5V, 1µs triangular pulse at gate, with V_D = 0.1V, $V_S = V_B = 0V$

2. Demonstrate program and erase operation on a single FeFET cell:

   Programming: Apply a 5V, 500ns pulse to program the FeFET.
   Threshold voltage check after programming: Sweep the gate voltage from -0.5V to 1.5V over 200ns to measure the threshold voltage, keeping $V_D = 0.1V$ and all other terminals grounded ($V_S = V_B = 0V$).
   Erasing: Apply a -5V, 500ns pulse to erase the FeFET.
   Perform the same gate voltage sweep after erasing to measure the threshold voltage under the same conditions.
3. Investigate the effect of varying pulse width on FeFET programming:
   Apply programming pulses at the gate with different widths (500ns, 1µs, 2µs, 4µs) while keeping the pulse amplitude constant at 5V.
   Measure the corresponding threshold voltage after each pulse, similar to Q2
   Discuss the relationship between pulse width and threshold voltage shift.

4. Create a 2x2 FeFET array and set the biasing scheme so that only the bottom-right cell transitions from a higher threshold voltage to a lower threshold voltage, while all other cells remain in the erased state. Note: Initially, all cells are in the high threshold voltage state.

(Note: Width / Length = 1um/1um, $V_{fb} = 0V$, $t_{IL} = 2nm$, $t_{fe} = 10nm$, number of domain (ndom) = 1000)