Assignment 4 (EE6347): Fall 2024

Please create a single document file (word/pdf) for all the plots, diagrams, screenshots. Upload these two documents in a single compressed file.

1. Design a 1Transistor-1RRAM bit cell. Use the 180 nm model file and the RRAM model provided. Perform quasi-DC set-reset operations. Plot the hysteresis (Id vs. Vdd).

Note: Exclude the compliance condition from the RRAM model. Control the compliance current using the transistor in series with the RRAM cell. RRAM parameters: Eam= 0.85, gamma0=20. (keep the other parameters same). Transistor: use 180nm model file, W/L = 18um/0.18um.