Assignment 3 (EE6347): Fall 2024

Upload the completed model as a separate text file. Please create a separate document (word/pdf) for all the plots, diagrams, screenshots. Upload these two documents in a single compressed file.

You are given an incomplete Verilog-A code to implement the Stanford model for a RRAM device.

(a) Your first job is to complete the model. Do so by defining the in/out and other electrical nodes; choosing appropriate values for the parameters (some parameter values are not given); and solving appropriate equations to calculate the current, gap, and the temperature. Upload the completed code as a separate text file.

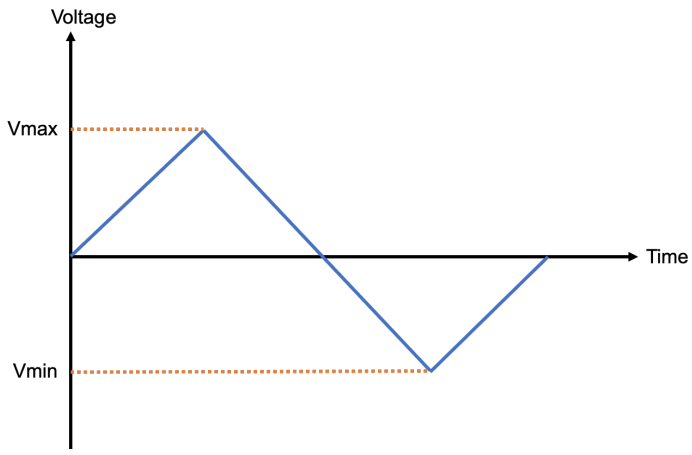
5 marks

(b) Now demonstrate bipolar resistive switching using the model you have created.

i. First, create a schematic for running transient simulations on your device. You should also measure the applied voltage (V) and the resulting current (I) in the device. Show the schematic you have created in a separate document file.

1 mark

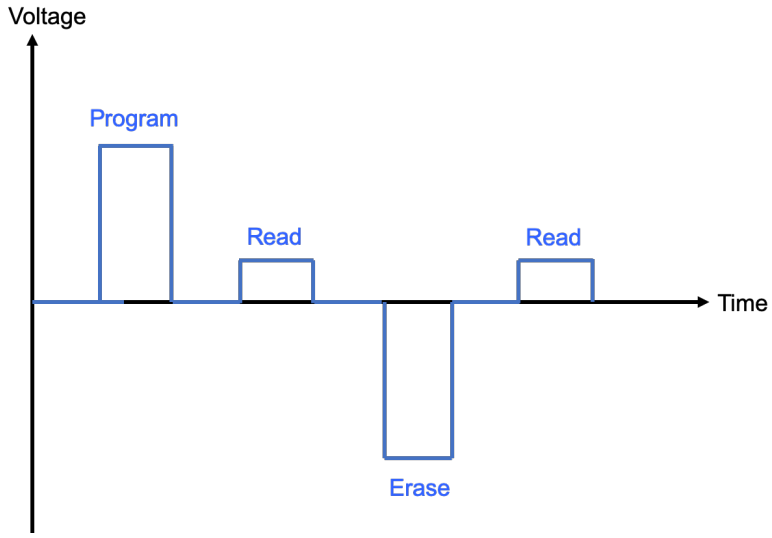
ii. Now, demonstrate SET and RESET operation using a voltage ramp as shown below. Make sure that Vmax >= V_{SET} and |Vmin| >= |V_{RESET}|. Note that you can control V_{SET} and V_{RESET} by changing the device parameters. Plot the simulated I-V characteristics of the device in a semi-log plot. Use a ramp rate of 2V/min.



3 marks

iii. Next, perform program/erase operation on the memory cell using voltage pulses. Use a write-and-verify scheme as shown below. Use a pulse width of 100 µs and duty cycle of 50%. Use V_{read} = 0.1V. Use appropriate V_{SET} and V_{RESET} amplitudes. Calculate the SET and RESET energy.

4 marks



(c) Fit the model you have created using the experimental SET and RESET data provided in two separate csv files. You have to adjust the model parameters to match the model with the experiment. Plot the simulated I-V along with the experimental data in a semi-log plot.

4 marks