EE6320 RF Integrated Circuits
Project: Mixer Design

Mixer Performance Summary Table

	Design Metric	Performance	Specification
Conversion Gain	Minimum Peak Gain in the specified band [$f_{RF} = f_{LO}$]	21.1655 dB	>15 *dB*
	Maximum Peak Gain in the specified band [$f_{RF} = f_{LO}$]	21.214 dB	>15 *dB*
	Peak Gain flatness in specified band [Max-Min Gain]	0.05 dB	-
	3*dB* RF Bandwidth [From the plot of $f_{RF} = f_{LO}$]	3.19 GHz	-
	Minimum Band-Edge Gain in the specified band [$f_{RF} = f_{LO} + 10MHz$]	21.1625 dB	>15 *dB*
	Maximum Band-Edge Gain in the specified band [$f_{RF} = f_{LO} + 10MHz$]	21.211 dB	>15 *dB*
Noise Figure	Maximum SSB Noise Figure for $f_{LO} = 5.17GHz$	7.16369 dB	≤ 10 dB
	Maximum SSB Noise Figure for $f_{LO} = 5.245GHz$	7.20897 dB	≤ 10 dB
	Maximum SSB Noise Figure for $f_{LO} = 5.32GHz$	7.25434 dB	≤ 10 dB
Linearity - IIP_2	Input power used for extrapolation	-50 dBm	-
	Power of Fundamental Tone at output (at chosen input power)	-30 dBm	-
	Power of IM_2 Tone at output (at chosen input power)	-110 dBm	-
	Extrapolated IIP_2	+34.43 dBm	≥ +30*dBm*
Linearity - IIP_3	Input power used for extrapolation	-50 dBm	-
	Power of Fundamental Tone at output (at chosen input power)	-30 dBm	-
	Power of IM_3 Tone at output (at chosen input power)	-120 dBm	-
	Extrapolated IIP_3	-4.71 dBm	≥ −5*dBm*
Power	Mixer DC power consumption [Excluding Bias]	0.203 mW	Minimize
	Bias circuit power consumption	1.44 mW	Minimize
Other	Sum of all resistances [excluding bias]	2.2 kΩ	-
	Sum of biasing resistances	20 kΩ	-
	Sum of all capacitances [Including AC coupling]	4 µF	-
	Sum of all inductances	Nil	
	Load chosen (each R_load)	1.1 kΩ	-
	Differential Mixer Input Capacitance (C_gs Caps)	108 fF	-
	Simulator Used	Cadence Virtuoso	-

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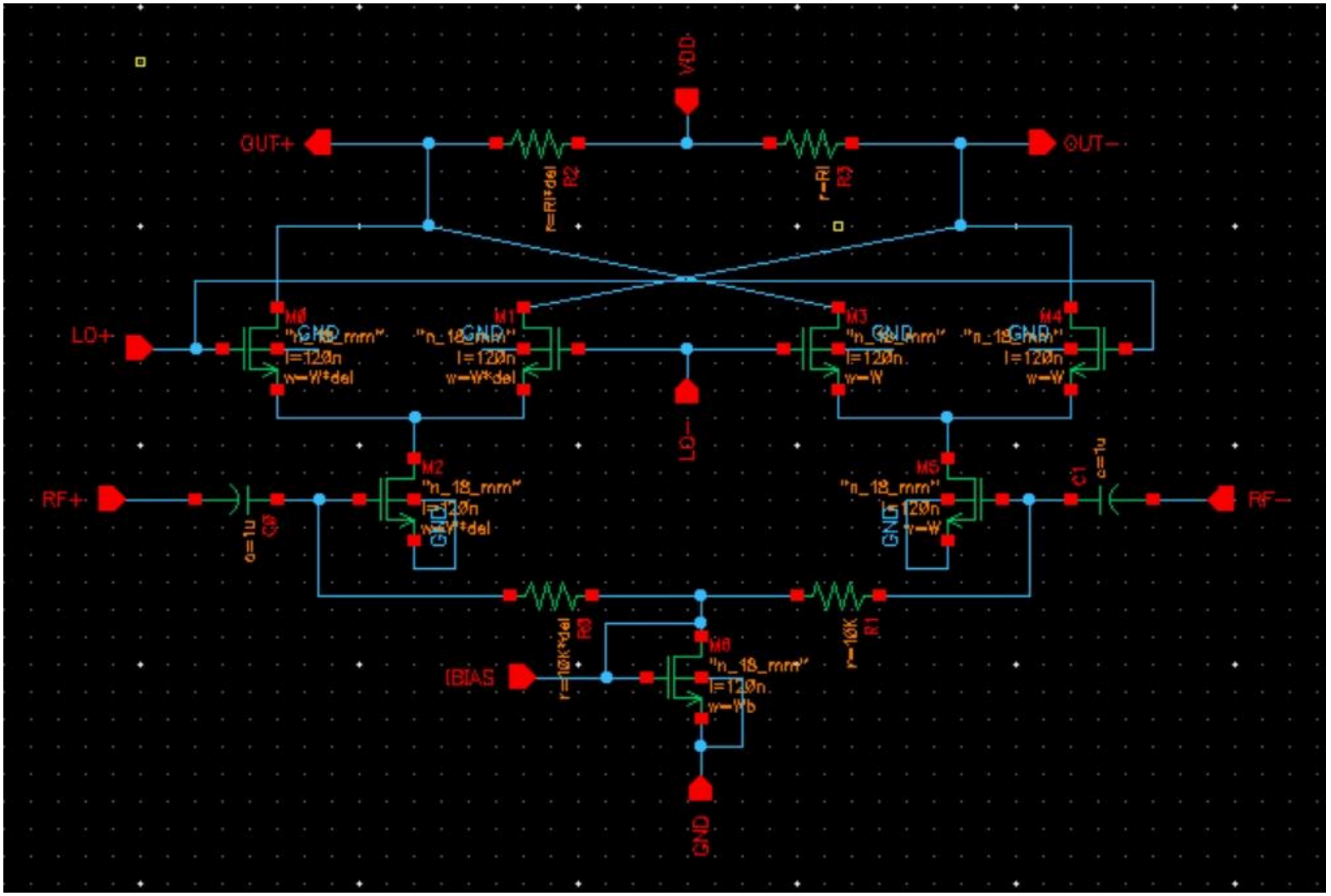
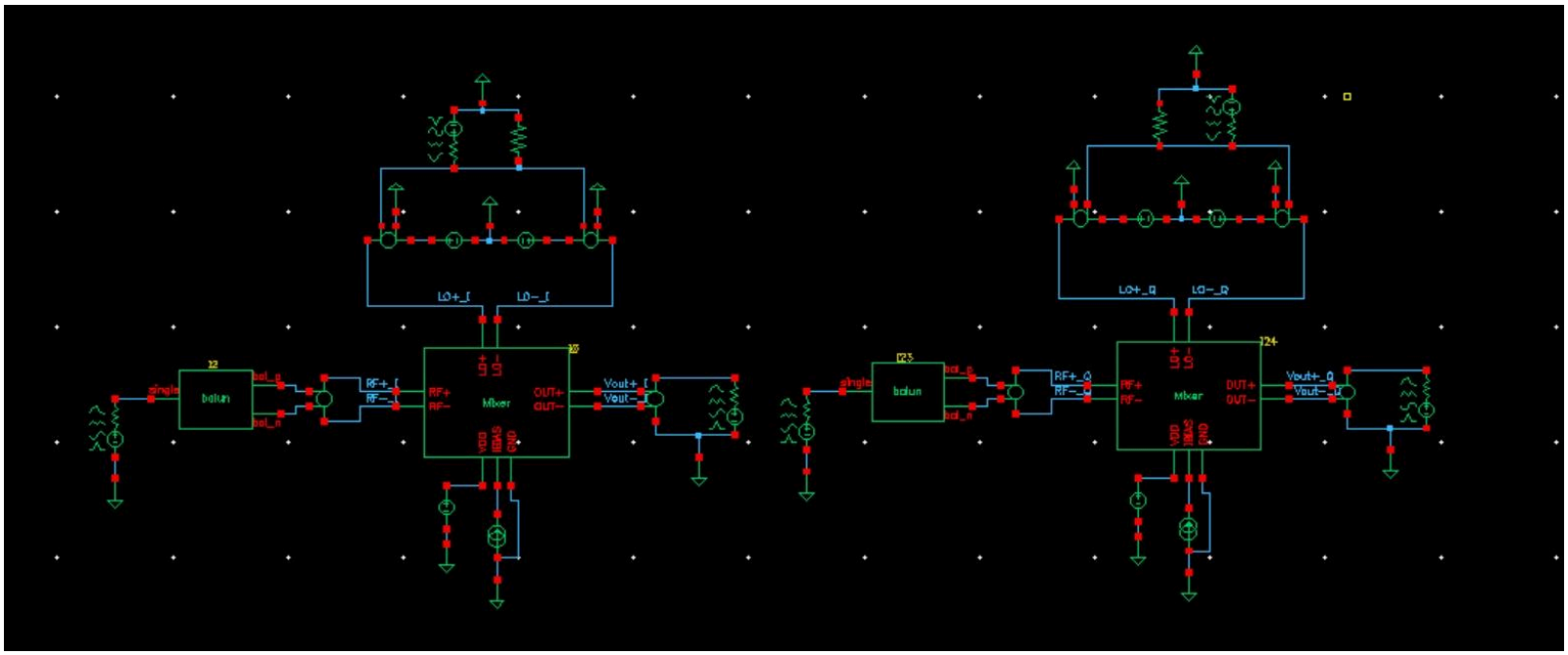
LNA + Mixer Performance Summary Table

	Design Metric	LNA	Mixer	Cascade	
				Expected	Simulated
Conversion Gain	$f_{IN} = f_{LO}$, $f_{LO} = 5.17GHz$	20.8 dB	21.214 dB	42.014 dB	47.42 dB
	$f_{IN} = f_{LO} + 10MHz$, $f_{LO} = 5.17GHz$	21.2 dB	21.211 dB	42.411 dB	47.365 dB
	$f_{IN} = f_{LO}$, $f_{LO} = 5.245GHz$	21.3 dB	21.1896 dB	42.4896 dB	47 dB
	$f_{IN} = f_{LO} + 10MHz$, $f_{LO} = 5.245GHz$	20.7 dB	21.1868 dB	41.8868 dB	46.95 dB
	$f_{IN} = f_{LO}$, $f_{LO} = 5.32GHz$	21.0 dB	21.1655 dB	42.1655 dB	46.61 dB
	$f_{IN} = f_{LO} + 10MHz$, $f_{LO} = 5.32GHz$	19.9 dB	21.1625 dB	41.0625 dB	46.565 dB
Noise Figure	$f_{IN} = f_{LO} + 10MHz$, $f_{LO} = 5.17GHz$	1.53 dB	7.16369 dB	2.34 dB	1.3507 dB
	$f_{IN} = f_{LO} + 10MHz$, $f_{LO} = 5.245GHz$	1.51 dB	7.20897 dB	2.296 dB	1.33508 dB
	$f_{IN} = f_{LO} + 10MHz$, $f_{LO} = 5.32GHz$	1.49 dB	7.25434 dB	2.287 dB	1.32117 dB
Linearity IIP3	Input power used for extrapolation	-30 dBm	-50 dBm	-	-40 dBm
	Power of Fundamental Tone at output (at chosen input power)	-18.7 dBm	-30 dBm	-	-18 dB
	Power of IM_3 Tone at output (at chosen input power)	-72.44 dBm	-120 dBm	-	-71 dBm
	Extrapolated IIP_3	-3.14 dBm	-4.71 dBm	-	-33.9036 dBm
Power	Total power consumption [Excluding Bias]	1.1 mW	0.203 mW	1.303 mW	1.5 mW
	Bias circuit power consumption	2.4 mW	1.44 mW	3.84 mW	3.84 mW

Mixer Schematic



Mixer Testbench



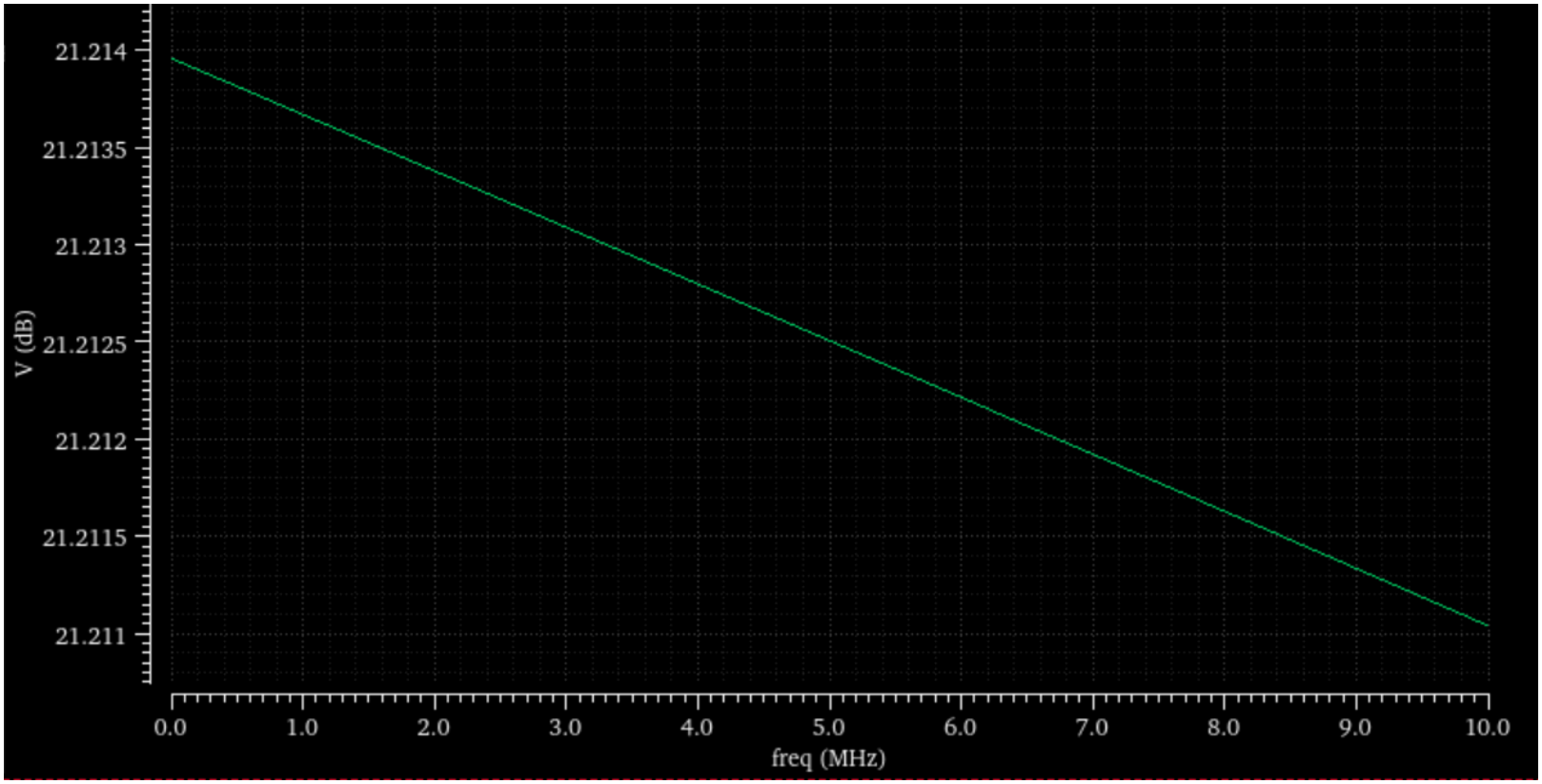
Design Variable Values

Design Variable	Value
Resistance (load, each side)	1.1 kΩ
Length of all MOS	120 nm
Width of Switch MOS (all 4)	48 µm
Width of Transconductance MOS (both MOS)	48 µm
Bias Current	600 µA
V_LO Amplitude	1.2 V

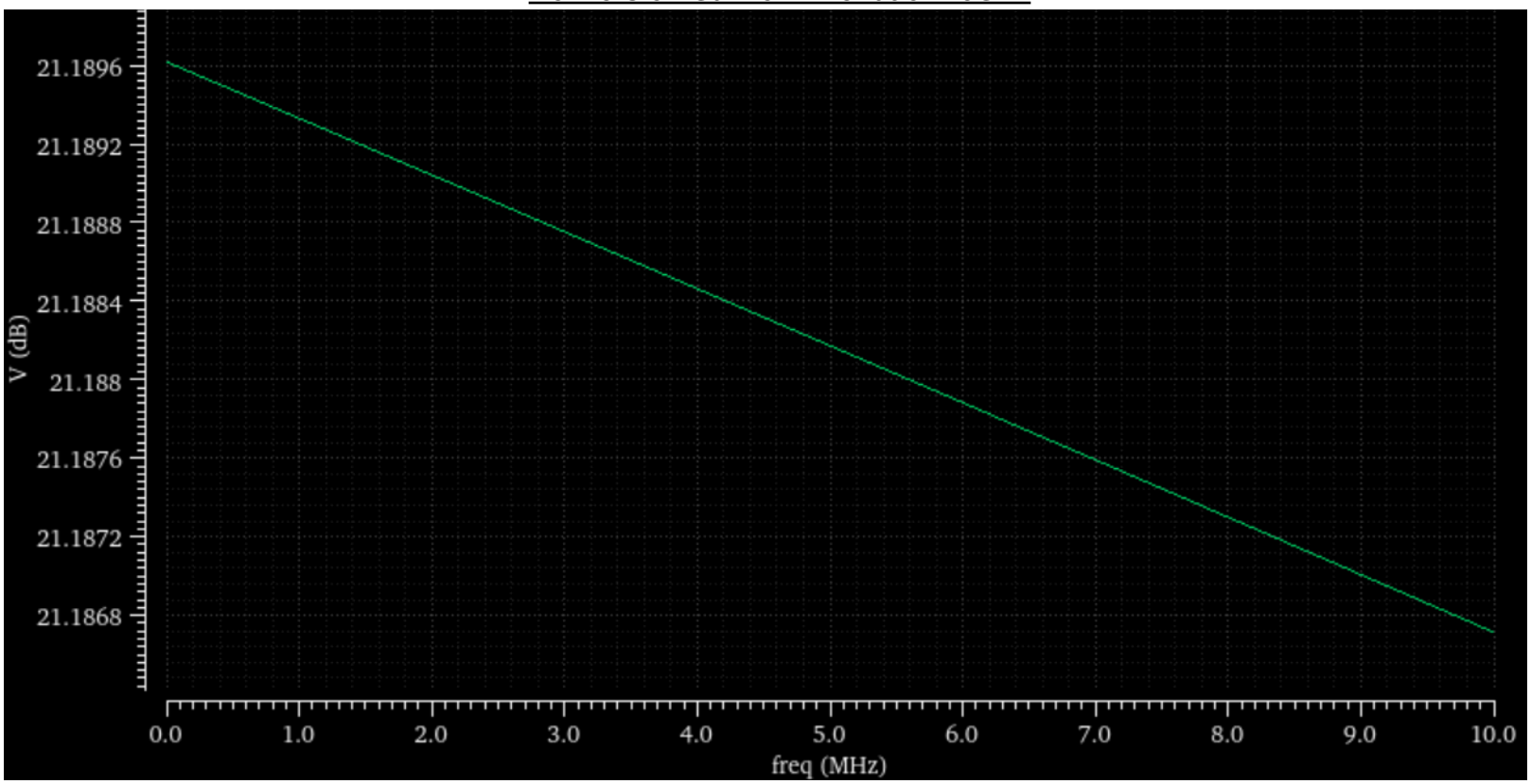
Fixed Constant Parameters

- **Transconductance MOS C_gs: 108 fF**
- **Current Mirror MOS: W = 96 µm , L = 120 nm**
- **Coupling capacitances: 1 µF (each)**
- **Bias Resistances: 10 kΩ (each)**

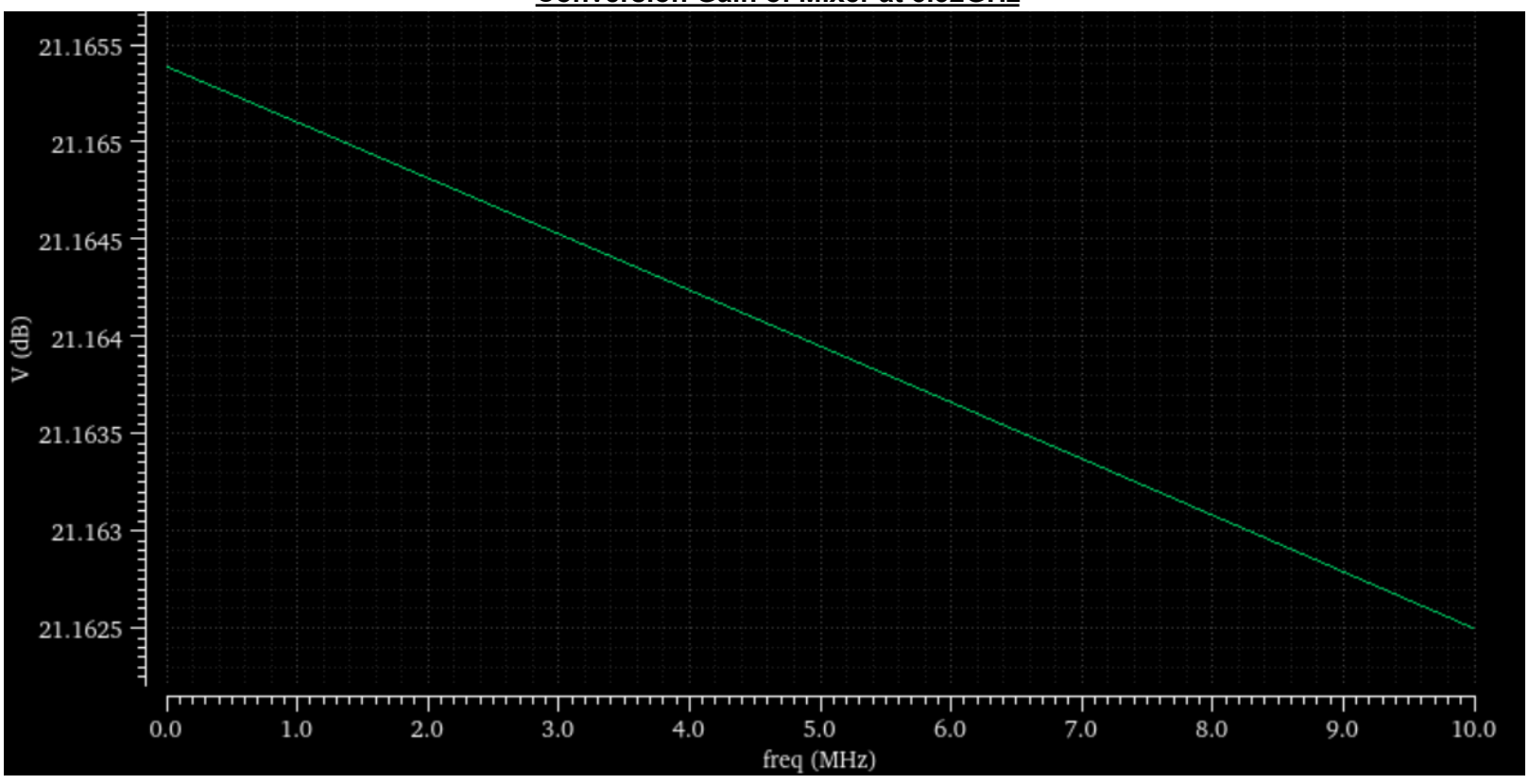
Conversion Gain of Mixer at 5.17GHz



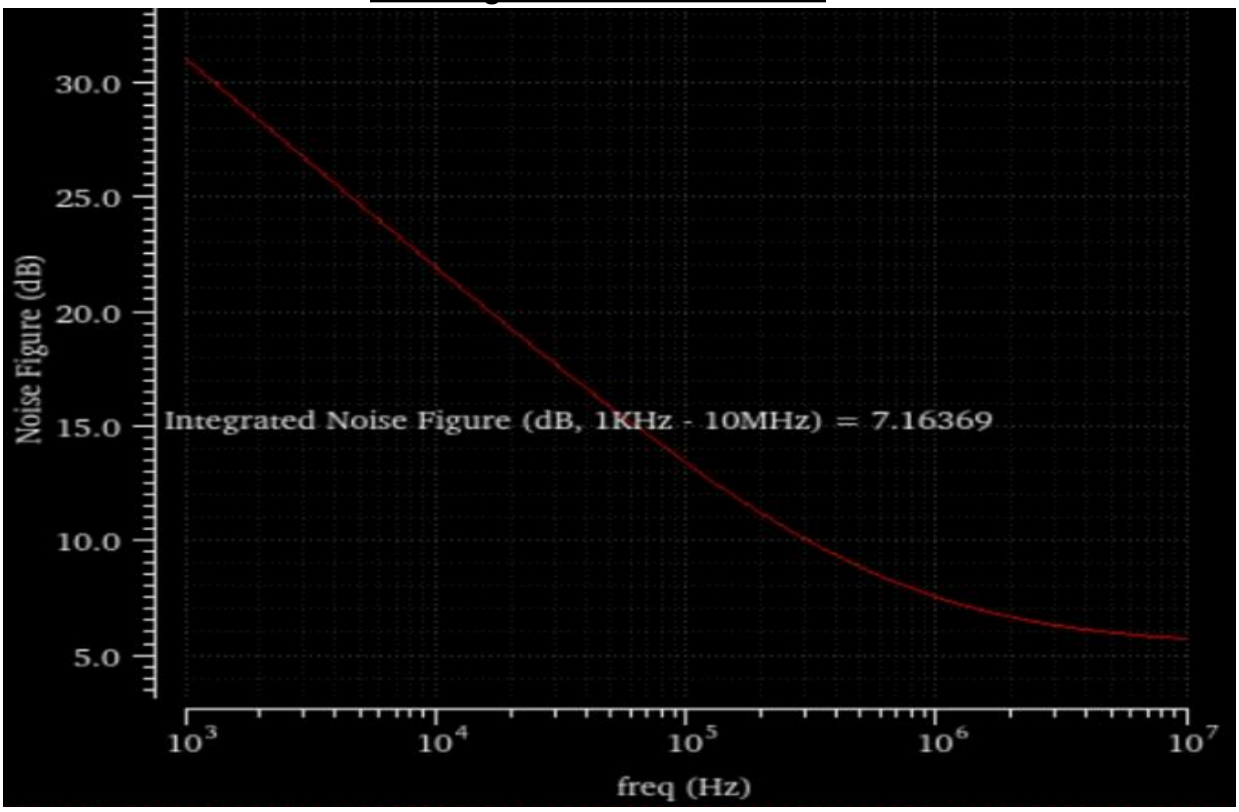
Conversion Gain of Mixer at 5.245GHz



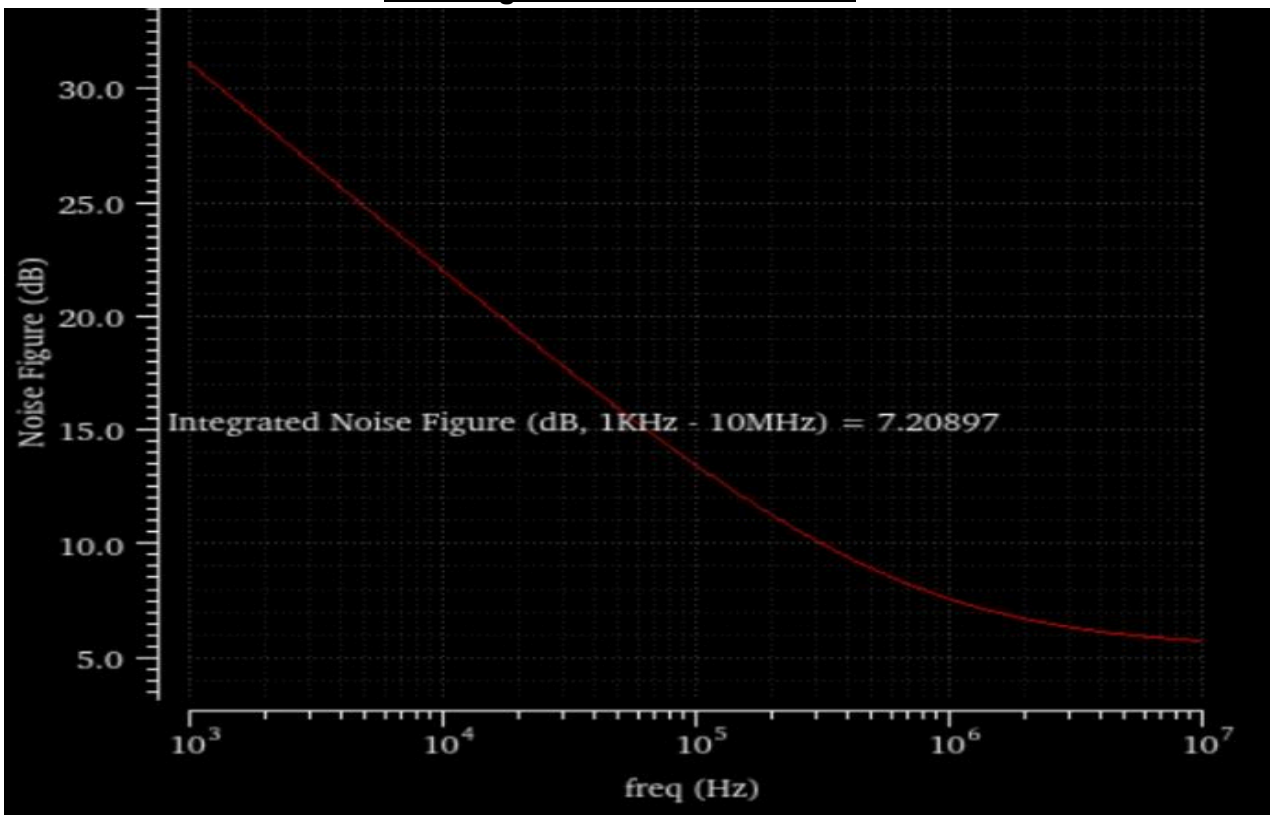
Conversion Gain of Mixer at 5.32GHz



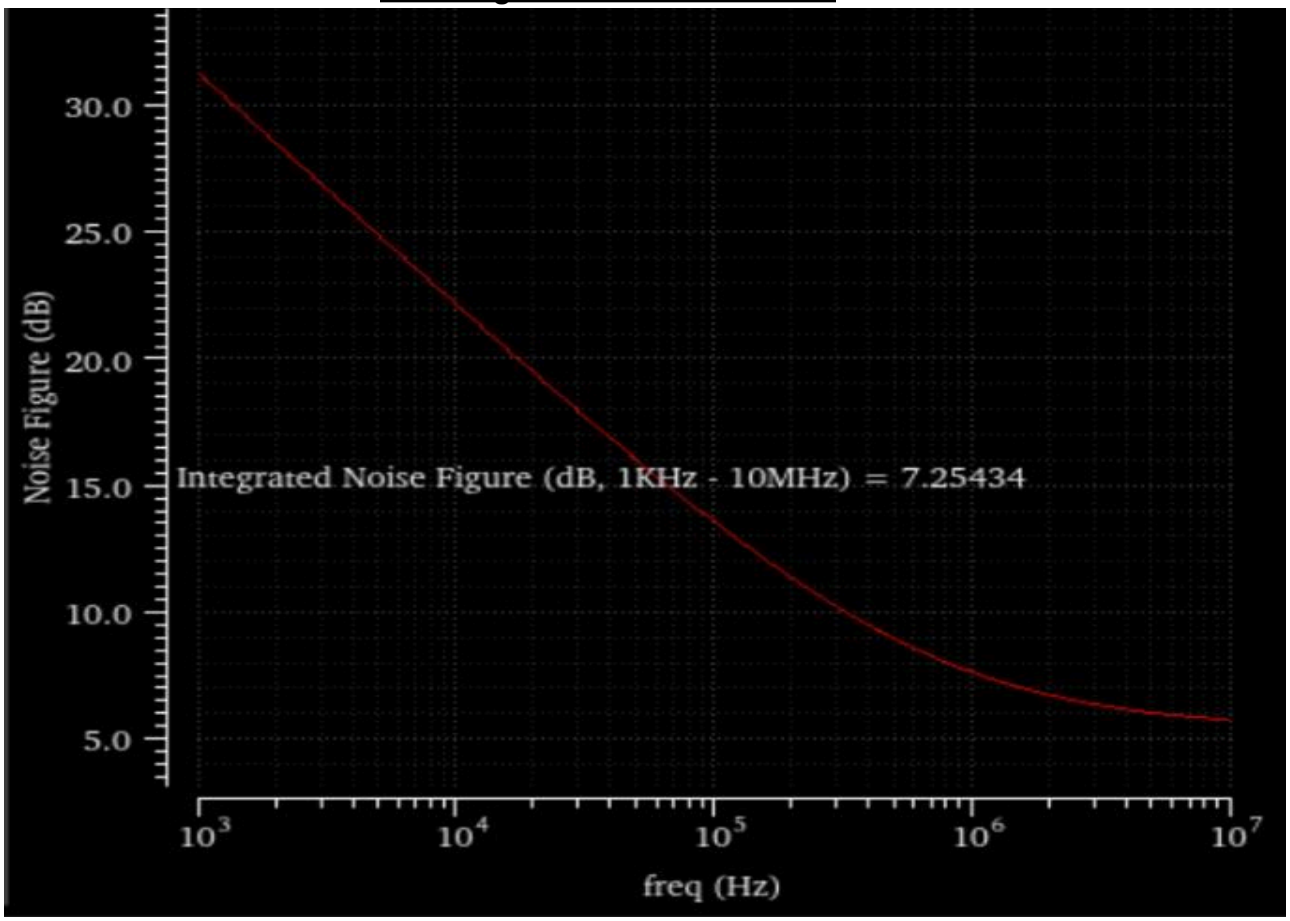
Noise Figure of Mixer at 5.17GHz



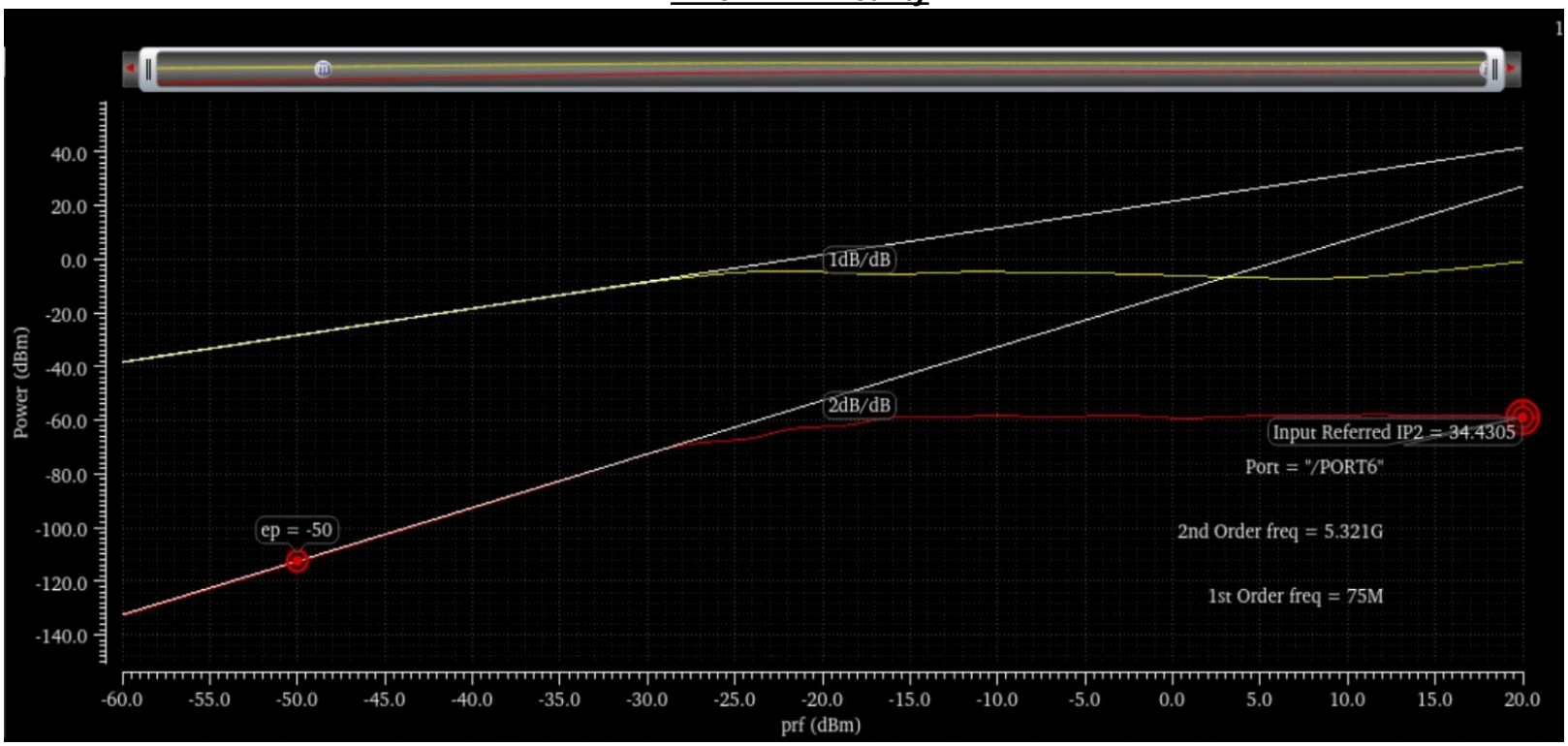
Noise Figure of Mixer at 5.245GHz



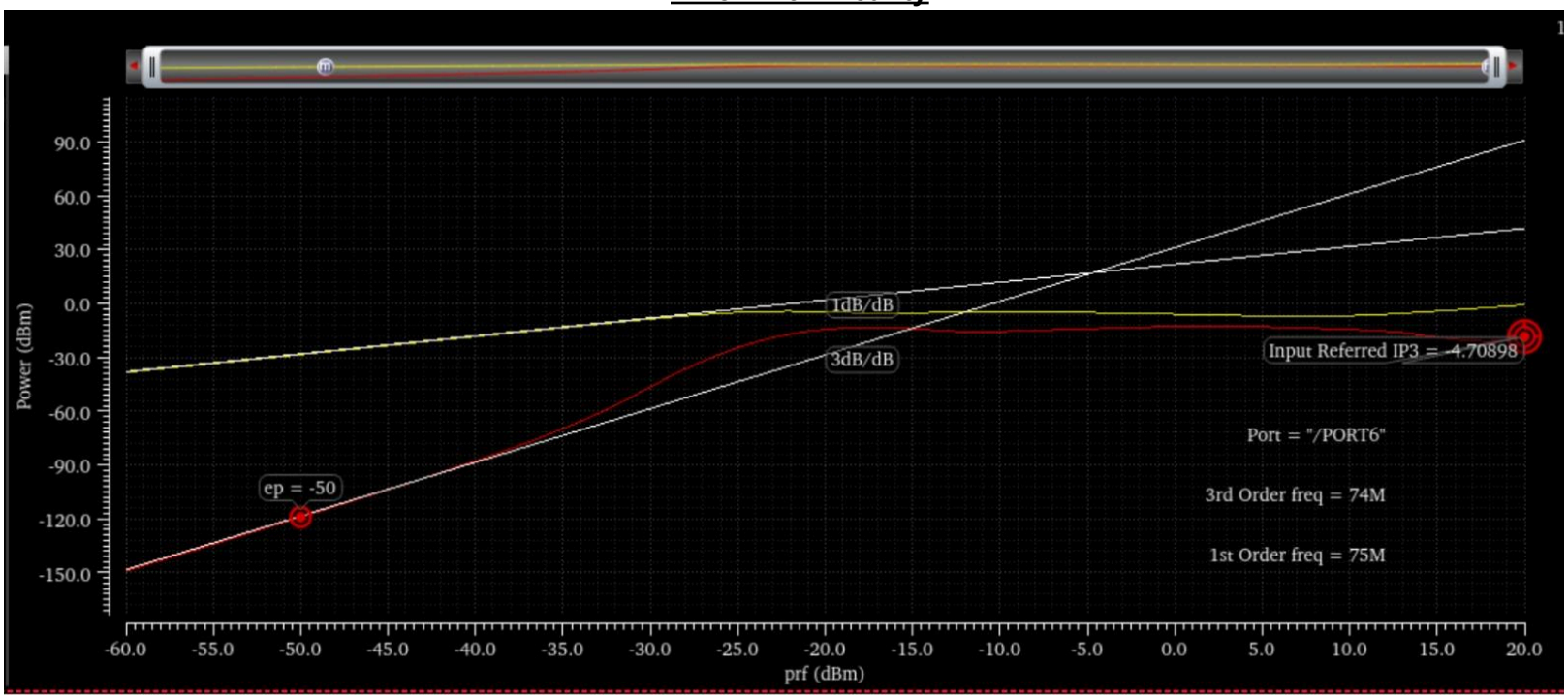
Noise Figure of Mixer at 5.32GHz



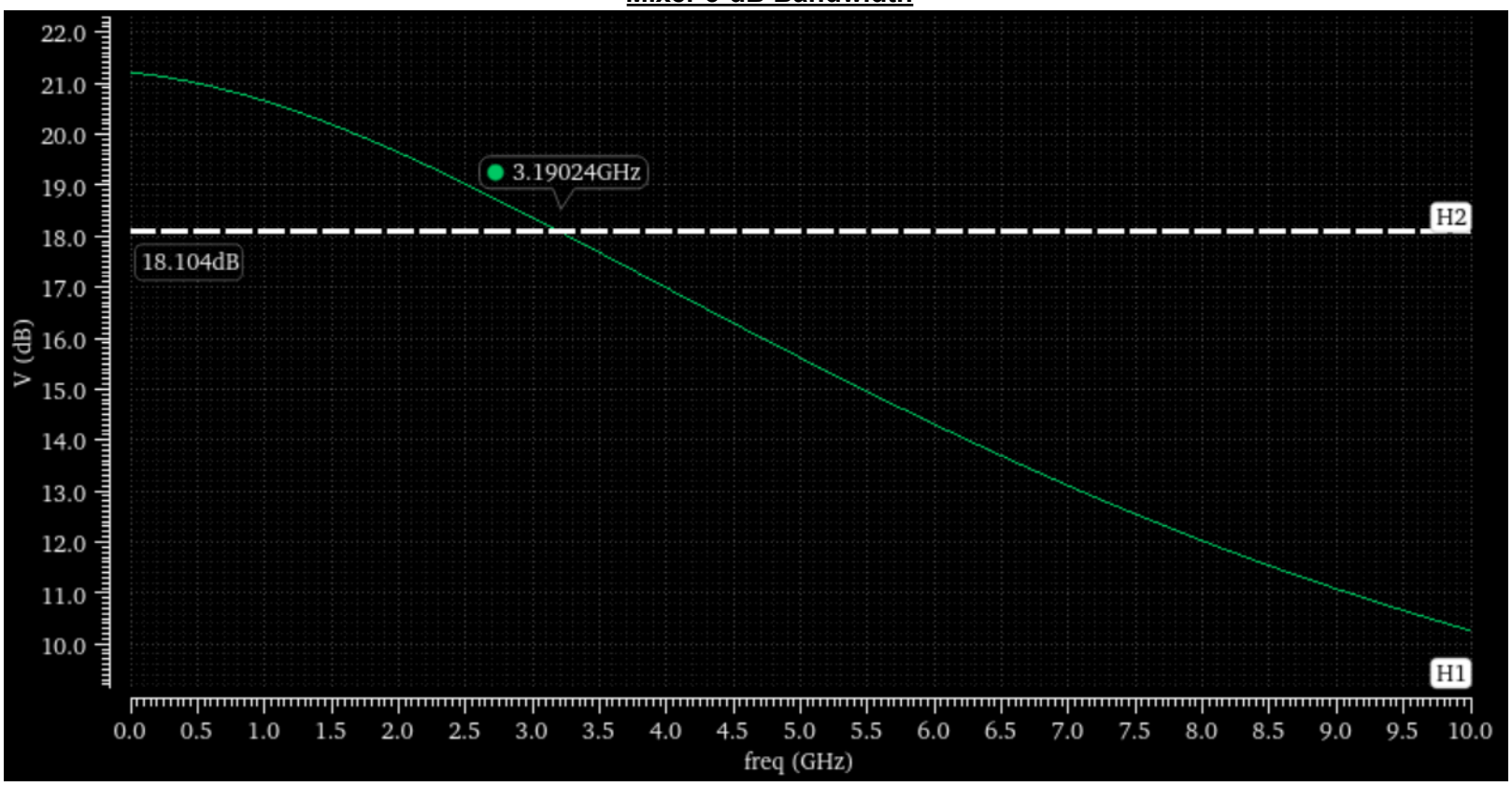
Mixer IIP2 Linearity



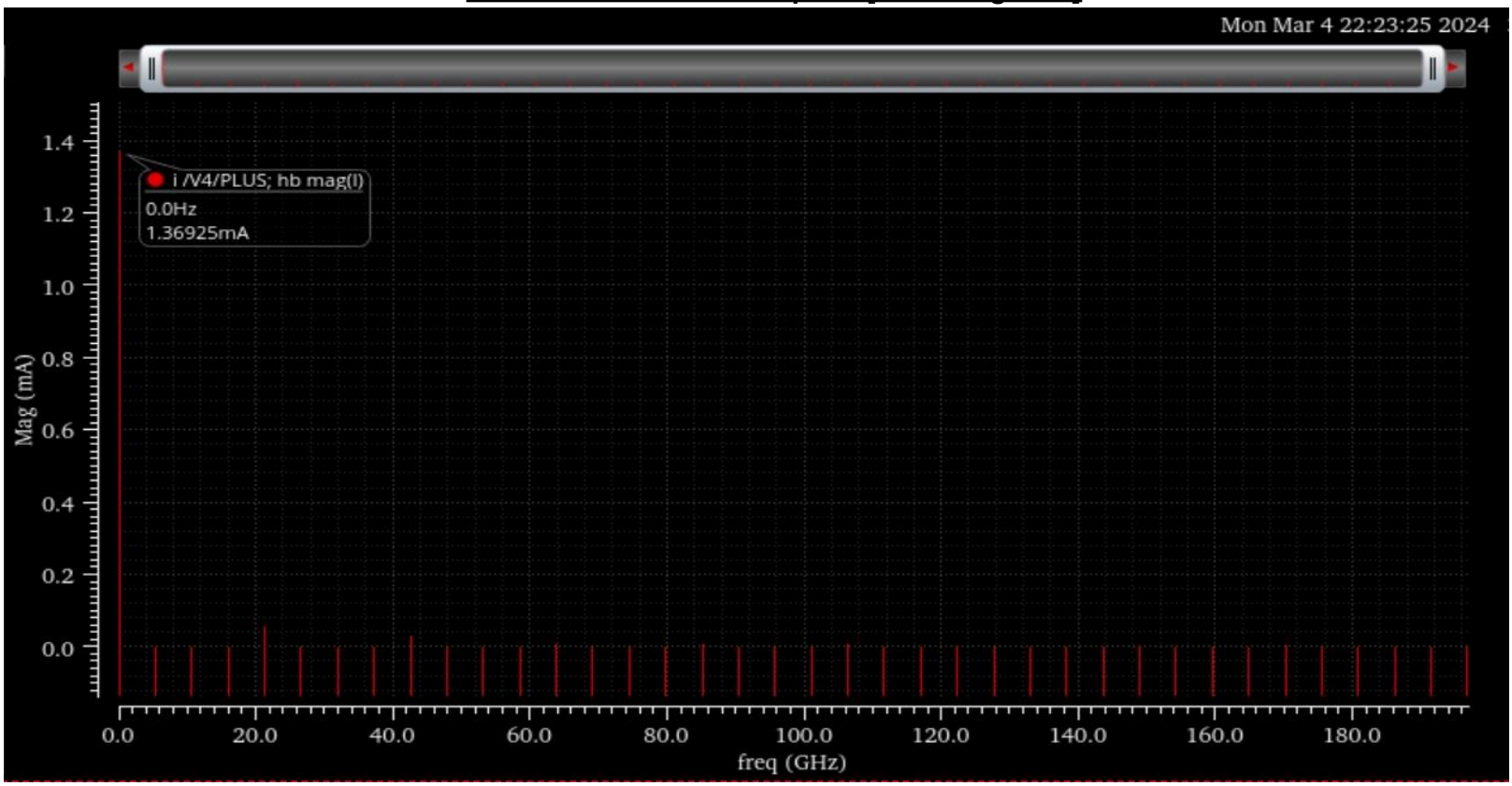
Mixer IIP3 Linearity



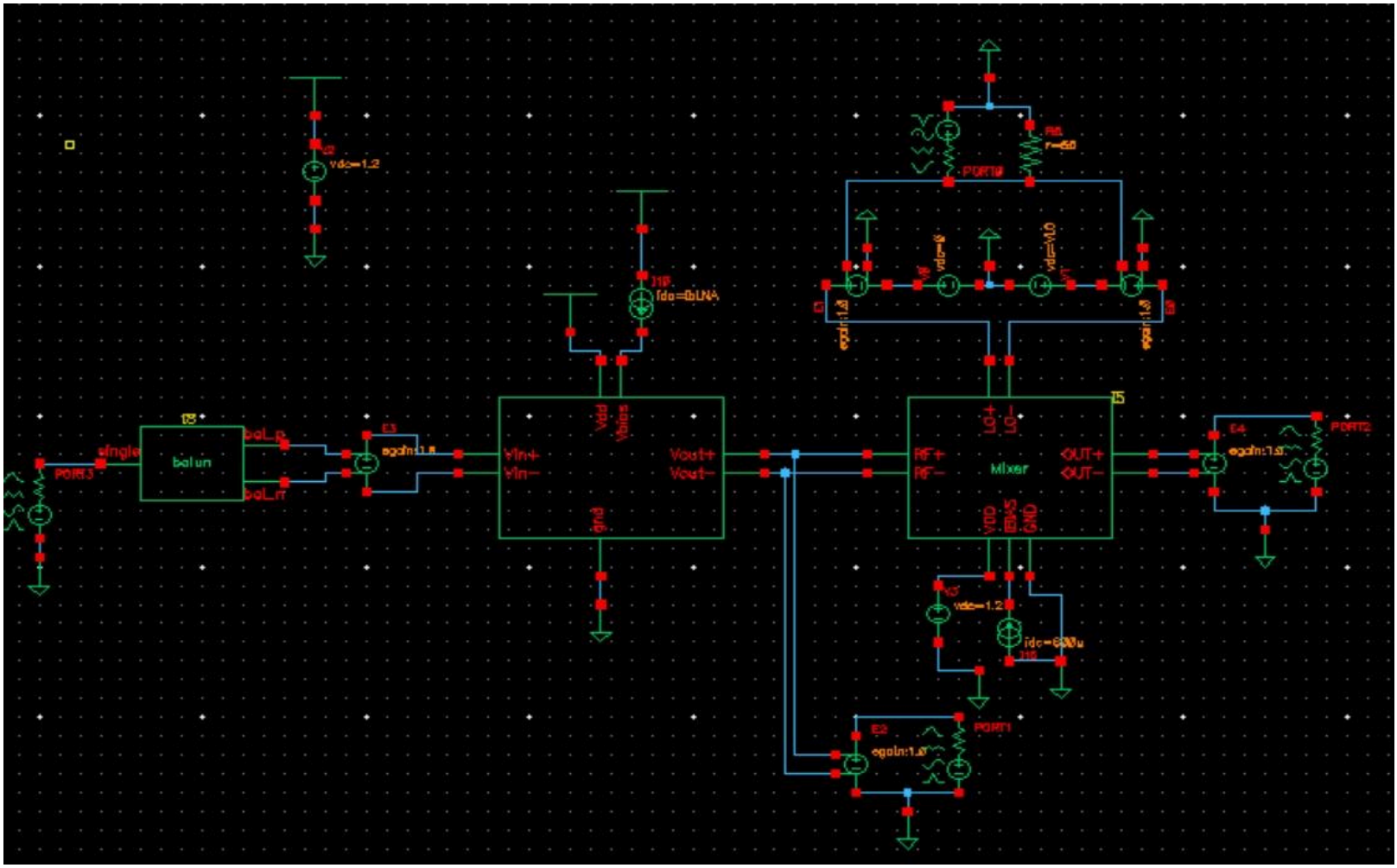
Mixer 3-dB Bandwidth



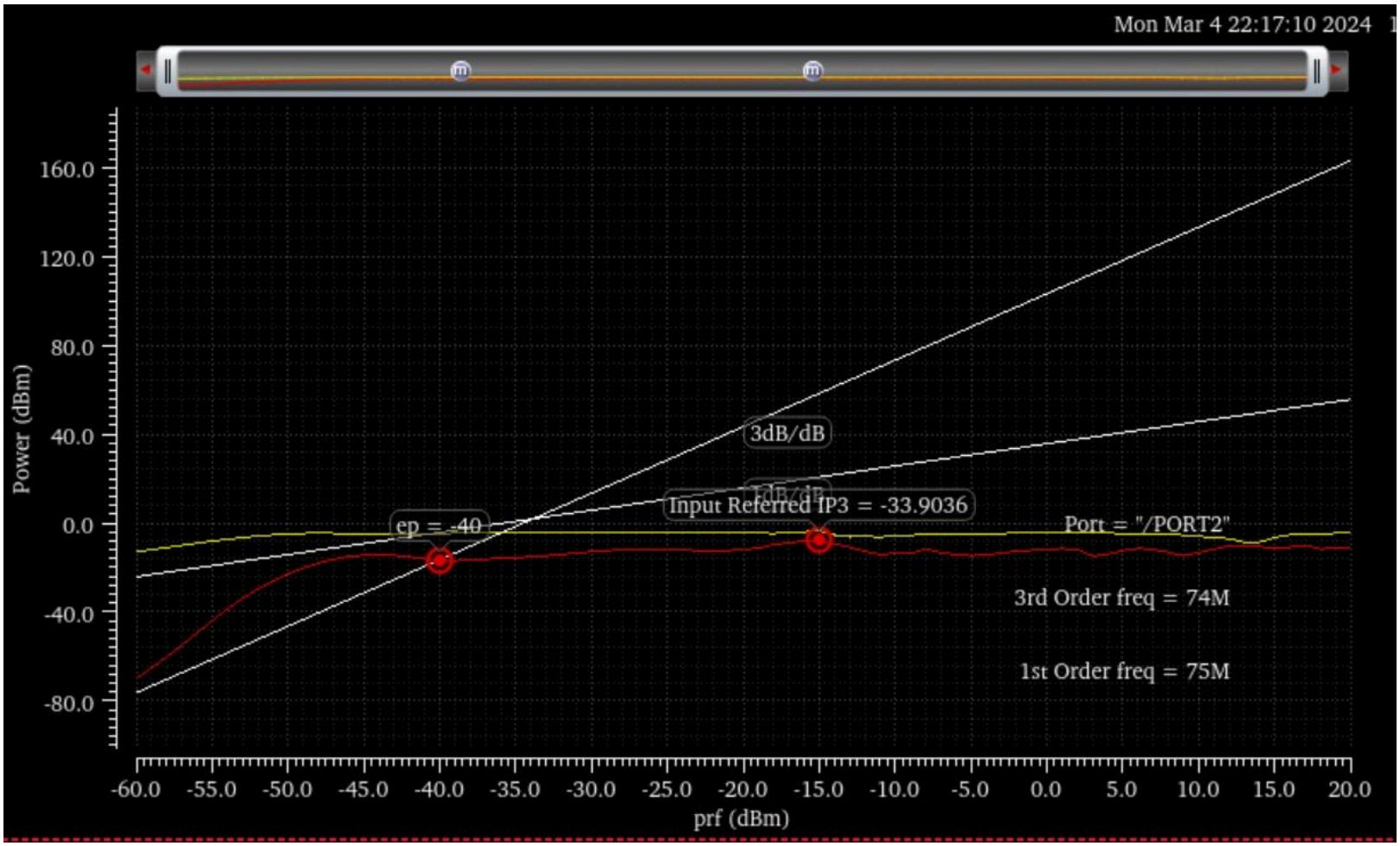
Mixer DC Power Consumption [Excluding Bias]



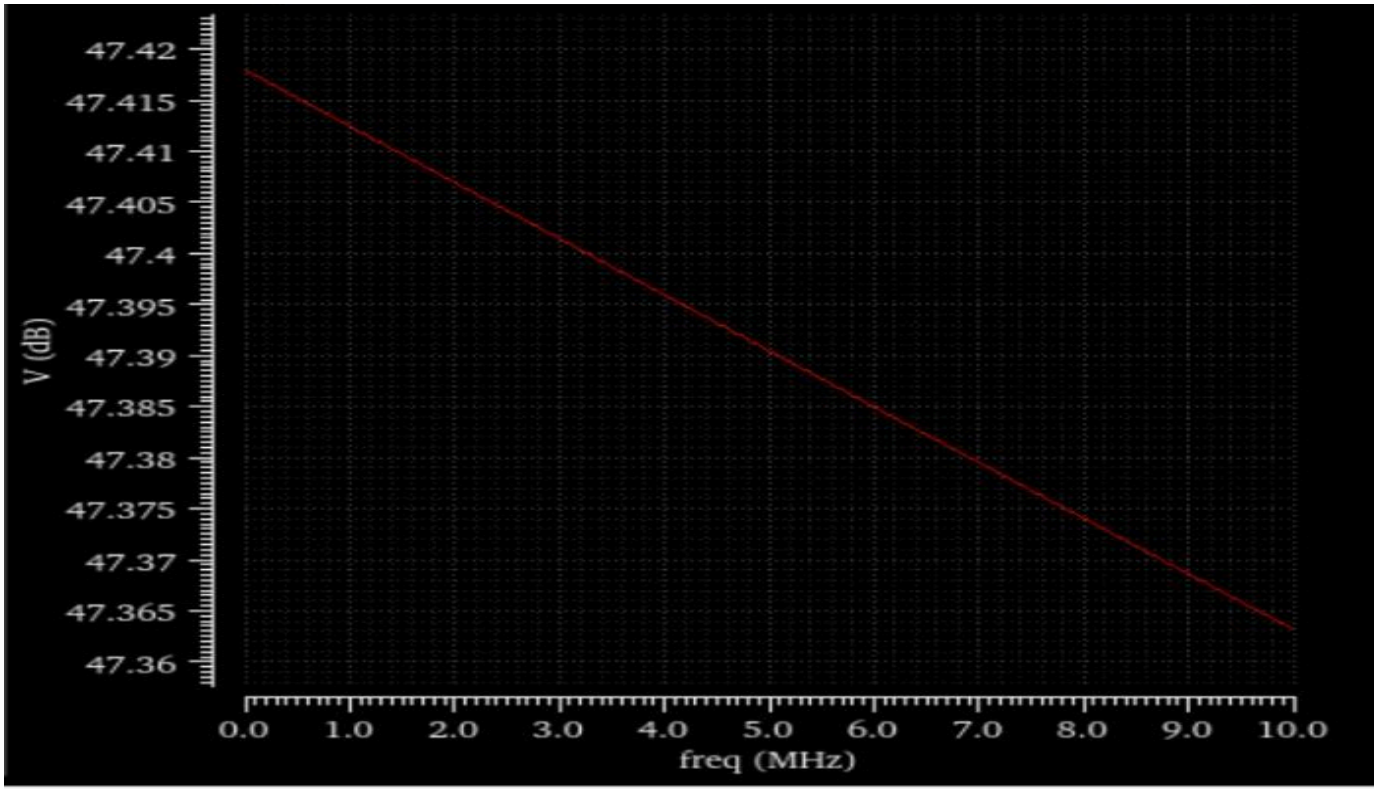
LNA + Mixer Testbench



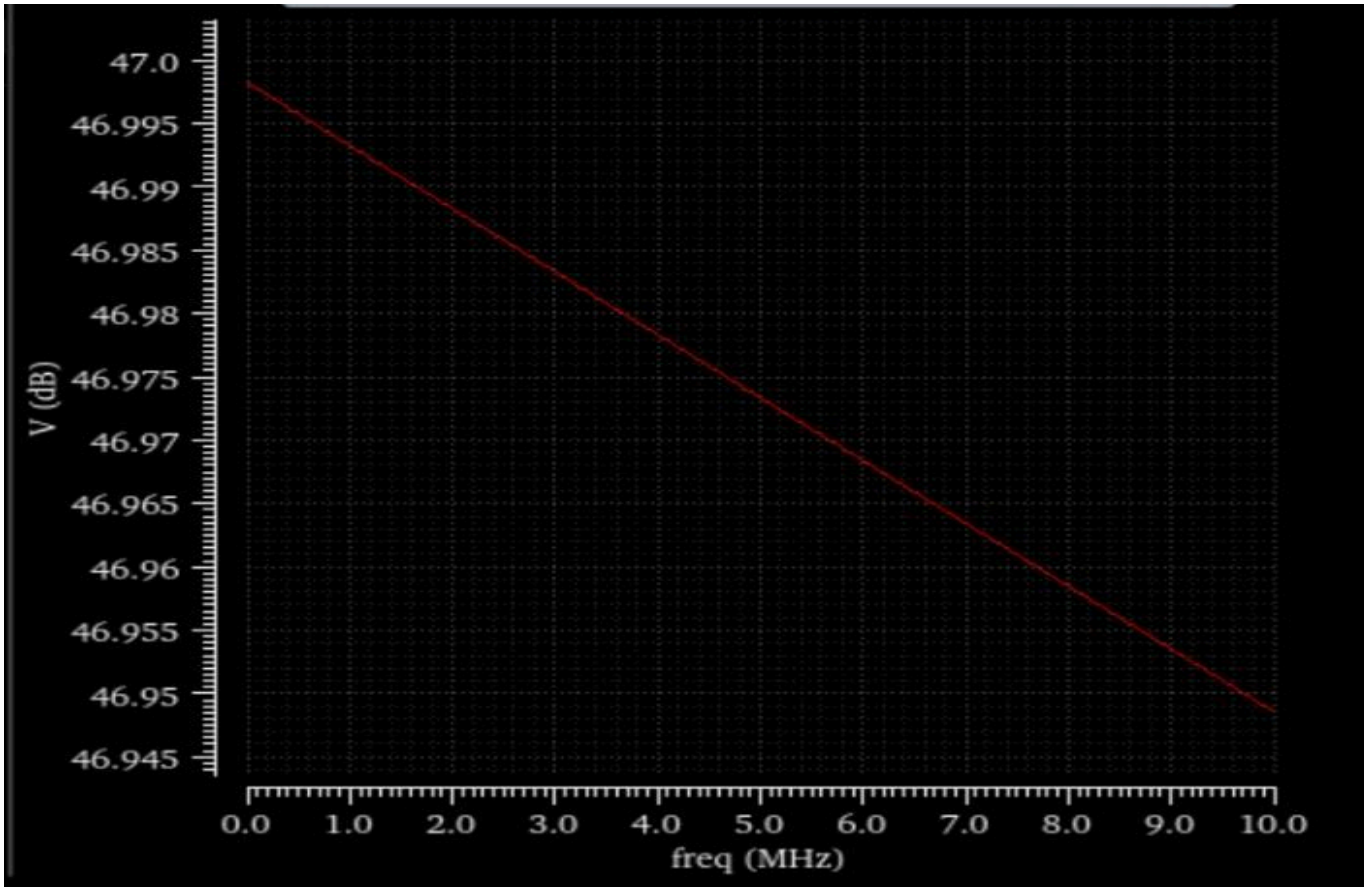
LNA + Mixer IIP3 Linearity



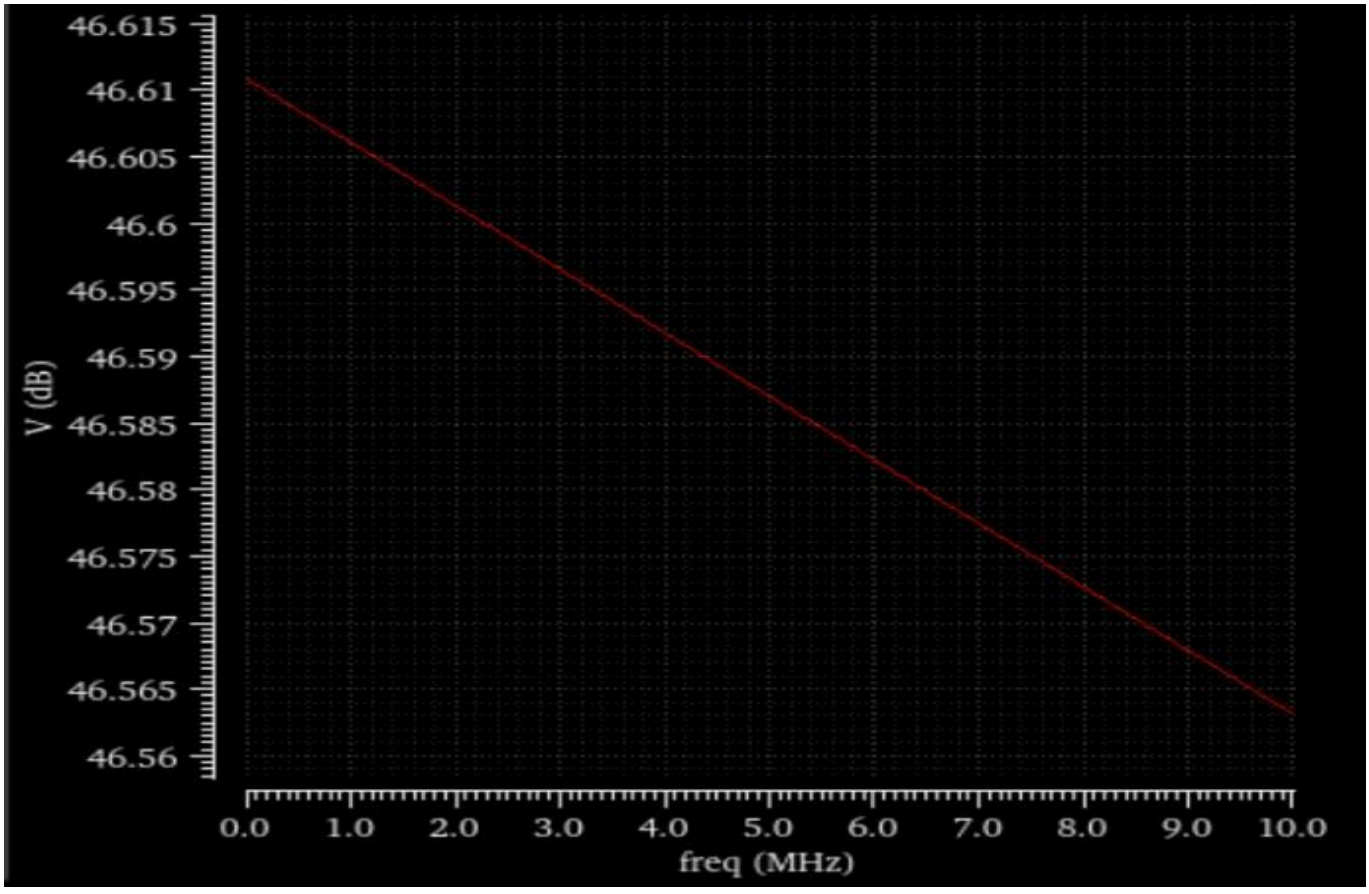
LNA + Mixer Conversion Gain at 5.17GHz



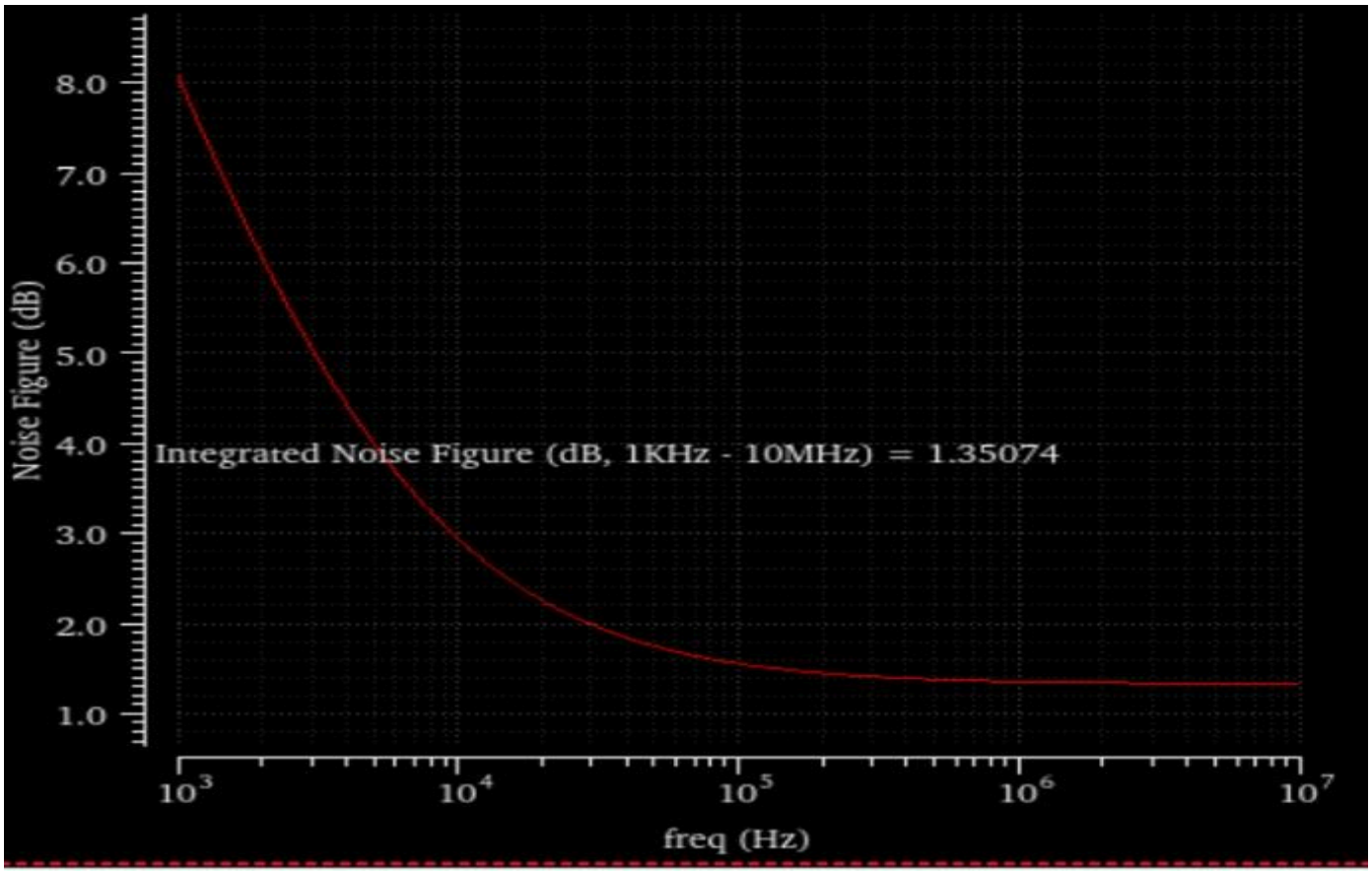
LNA + Mixer Conversion Gain at 5.245GHz



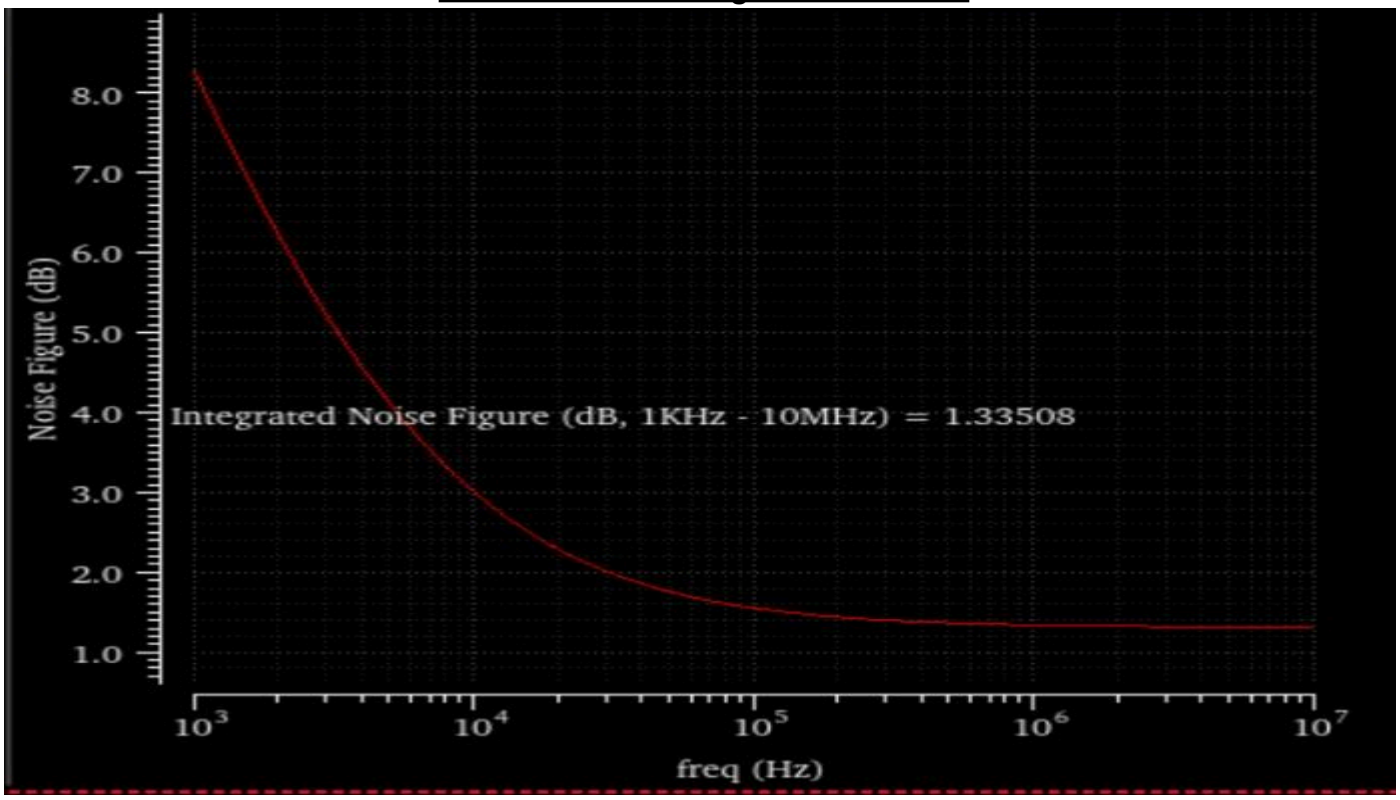
LNA + Mixer Conversion Gain at 5.32GHz



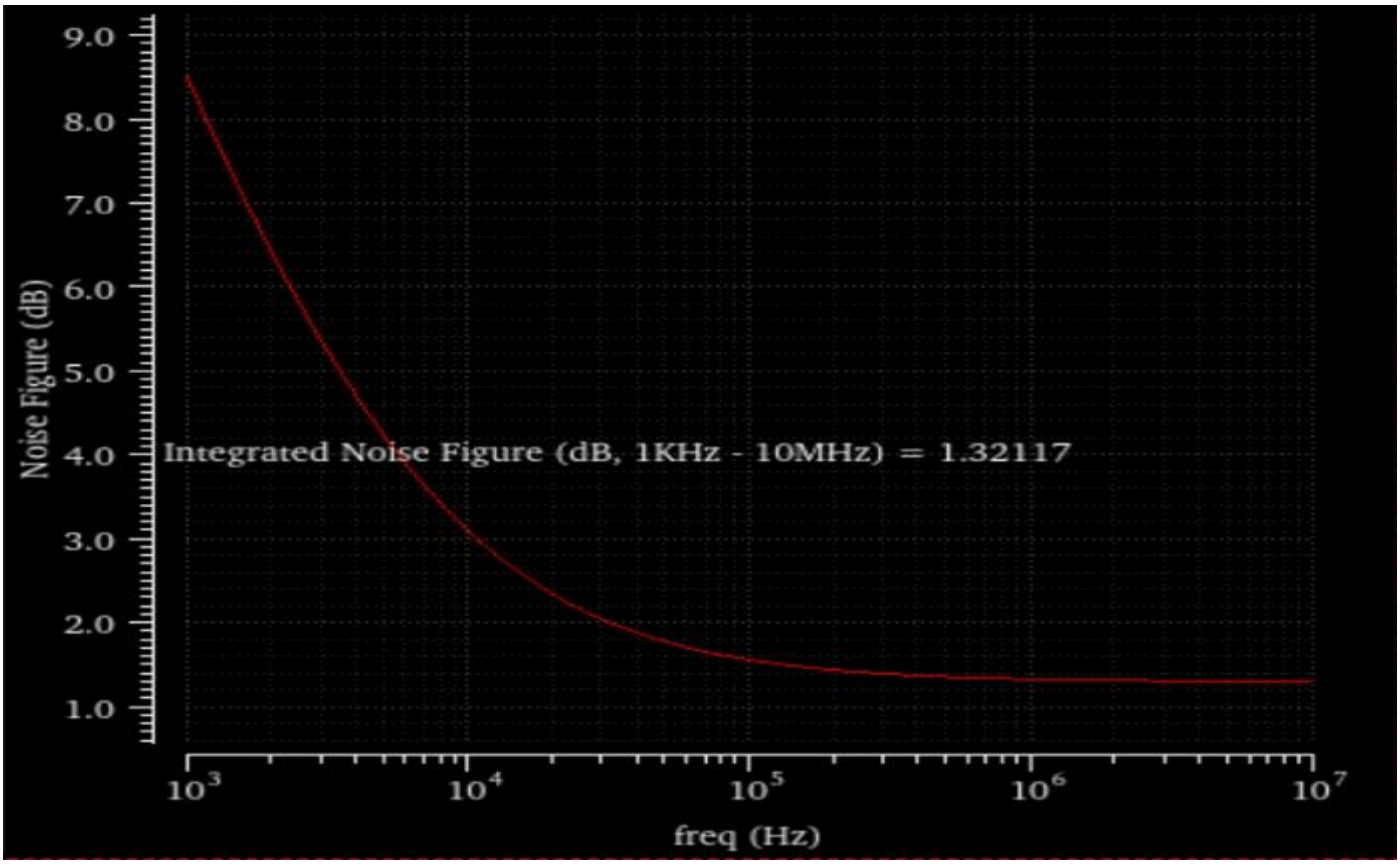
LNA + Mixer Noise Figure at 5.17GHz



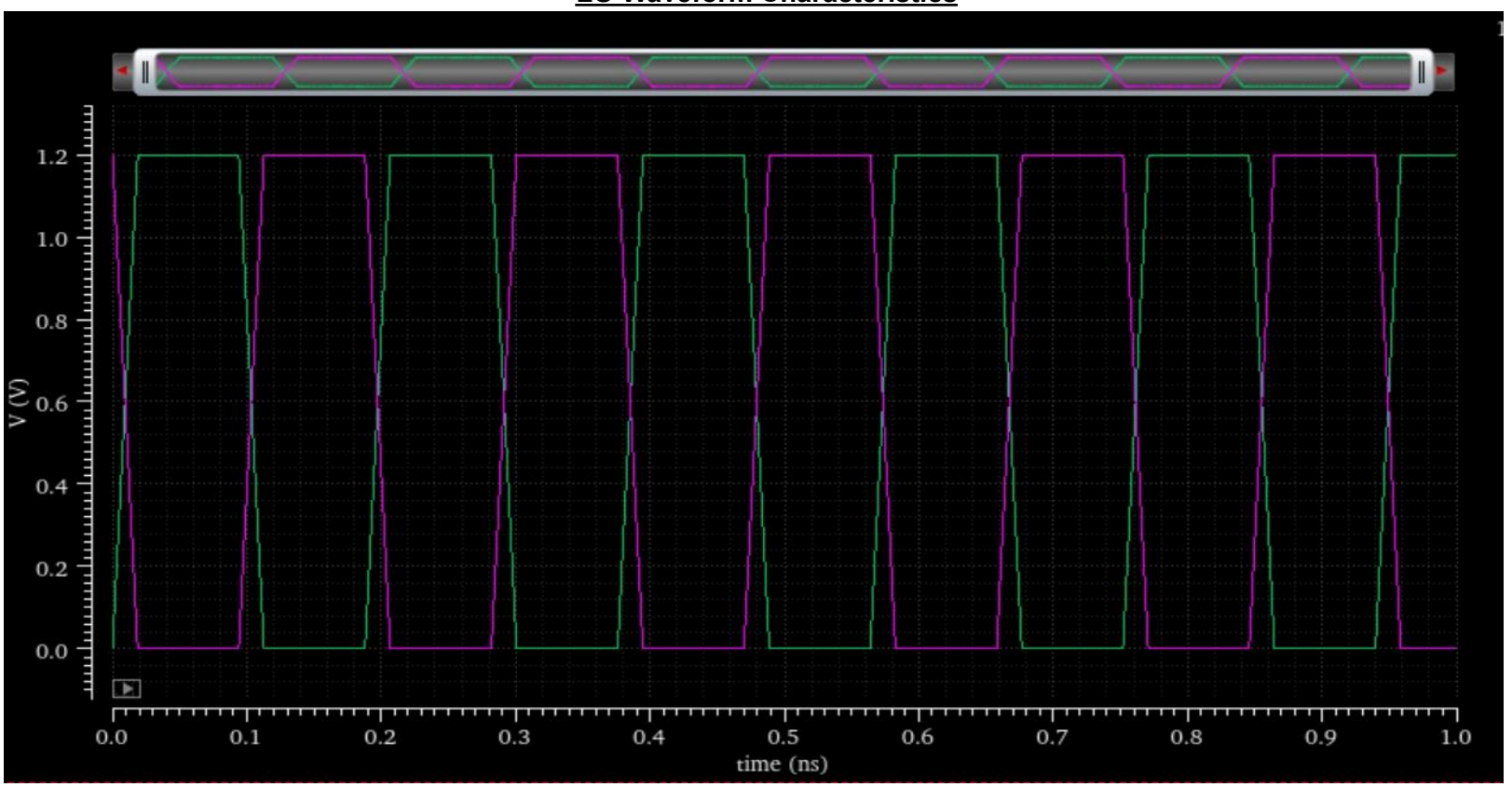
LNA + Mixer Noise Figure at 5.245GHz



LNA + Mixer Noise Figure at 5.32GHz



LO Waveform Characteristics



Characteristics taken are *(for generalized manner, as flo varies for various analysis)*:

- **Frequency: flo Hz**
- **Time period: 1/flo s**
- **Delay time: 0 (for I Lo signal), 0.25/flo (for Q Lo signal)**
- **Pulse Width: 0.40/flo**
- **Rise/Fall Time: 0.10/flo**

Path to the Project Files

Path : ee21b019@ams117~/EE6320_Mixer_Design/Mixer

Design Procedure

1. Hand calculations were performed to get the specific conversion gain using the formula derived in the RFIC video lectures.
2. gm, Rl, and Ibias were picked in such a way that the conversion gain spec. is met, making sure that all the transistors stay in saturation and swing limits are maximised.
3. The length of the transistor was chosen to be the minimum possible length permitted (120 nm).
4. W was picked according to the specification on gm and characteristic mu.Cox value
5. Simulation was performed using the hand calculated values.
6. The conversion gain obtained was slightly lower (around 12 dB), so Ibias was increased.
7. Noise Figure simulated later met the Noise Figure specification
8. The IIP2 and IIP3 specifications were also met.
9. Next, the LNA and Mixer were cascaded.
10. All the simulations were performed on the cascaded combination.
11. The LNA and mixer were slightly tuned to minimize power dissipated.
12. Everything obtained in the cascade was as desired.

Calculations done for the Project

EE6320: RF Integrated Circuit
Mixer Design
Hand Calculations

1) $V_{LO} = V_{dd} = 1.2V$

2) $\mu C_{ox} = 552 \times 10^{-6} \frac{A}{V^2}$ [From mos characterization]

$\frac{2}{\pi} g_m R_d = 10$. (Conversion gain of 20dB)

Set $R_d = 1K\Omega$,

$g_m = 15.7mS$.

$L = L_{min} = 120\ nm$

From previous LNA design, it is known that $I_b = 3mA$ gives a g_m of 15 mS.

$\Rightarrow I_b = 3mA$ meets the spec. with $W = 48\mu m$.

$\therefore W = 48\mu m$, $L = 120\ nm$, $I_b = 3mA$, $R_d = 1K\Omega$

For bias current source,

$W_b = 96\mu m$ as in LNA design.

Noise Figure for Mixer + LNA

From Friis equation,

$$F = F_1 + \frac{F_2 - 1}{g_1} \quad \text{and} \quad NF = 20\log_{10}(F)$$

Eg. For $f_{LO} = 5.17$ GHz, we get

$NF = 2.34\ dB$