EE6320 RF Integrated Circuits
Project: VCO Design

VCO Performance Summary Table

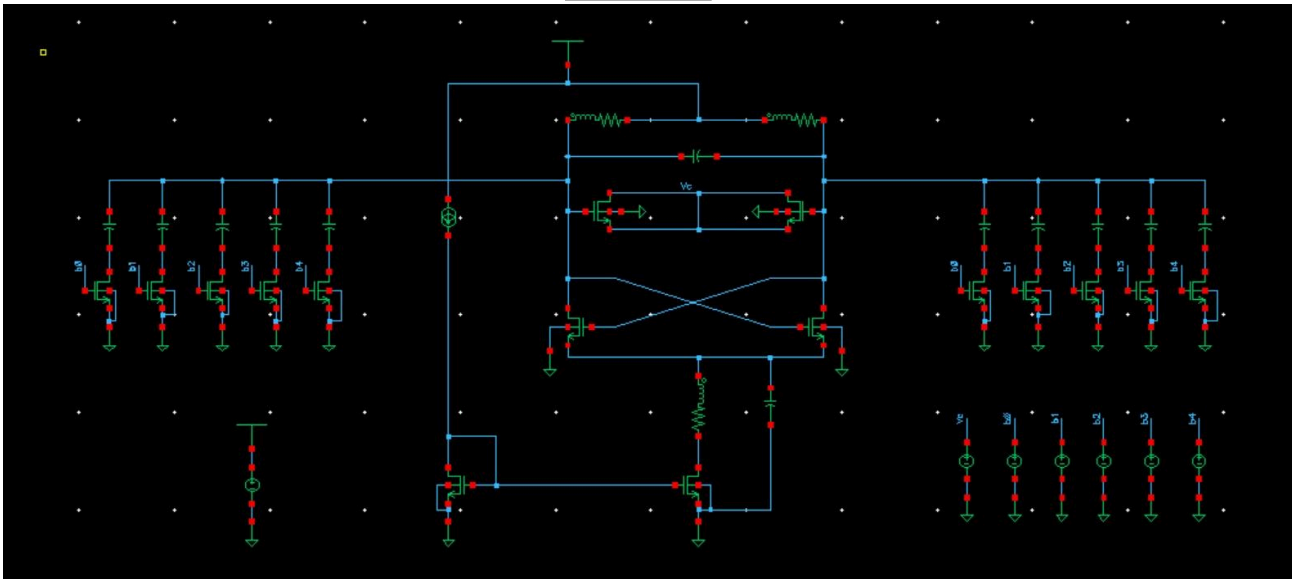
Design Parameter	Design Metric	Performance	Specification
Output Amplitude (Vpp/2)	freq = 5.17 GHz	0.9072 V	≥ 0.8V
	freq = 5.245 GHz	0.9288 V	≥ 0.8V
	freq = 5.32 GHz	0.9340 V	≥ 0.8V
Phase Noise (1 MHz Offset)	freq = 5.17 GHz	-131.46 dBc/Hz	≤ -118 dBc/Hz
	freq = 5.245 GHz	-130.98 dBc/Hz	≤ -118 dBc/Hz
	freq = 5.32 GHz	-128.88 dBc/Hz	≤ -118 dBc/Hz
Phase Noise (20 MHz Offset)	freq = 5.17 GHz	-159.20 dBc/Hz	≤ -150 dBc/Hz
	freq = 5.245 GHz	-159.30 dBc/Hz	≤ -150 dBc/Hz
	freq = 5.32 GHz	-158.12 dBc/Hz	≤ -150 dBc/Hz
Tuning Range	Total Tuning Range	510.93 MHz	≥ 150 MHz
	Number of bits in coarse tuning	5	-
	Voltage range in fine tuning	400 mV	-
	Average KVCO	142.6 MHz/V	150 MHz/V
	% variation in KVCO	31.55 %	minimal
Power Consumption (5.245 GHz)	VCO average power consumption (excluding bias)	6.6156 mW	minimal
	Bias circuit	9 mW	minimal
Other	Sum of all capacitances (in capacitor bank)	930 fF	-
	Net inductance used	800 pH	-
	Simulator used	Cadence Virtuoso	-

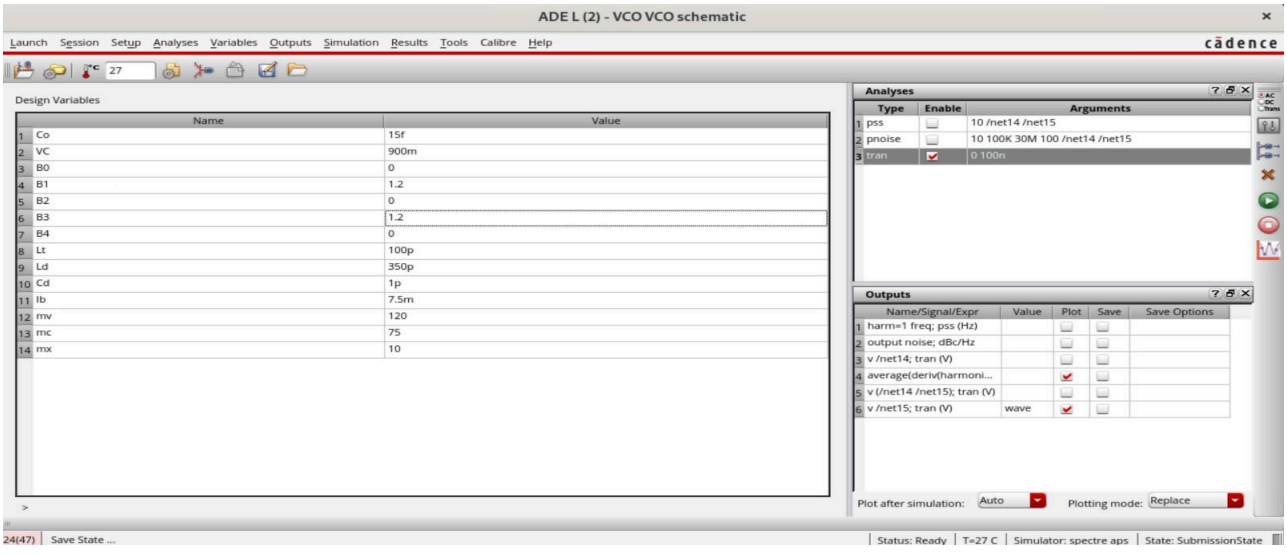
Name: ANIRUDH B S
Roll No: EE21B019

Component Values Table

Component	Value
Current Mirror MOS	W = 1 μm, L = 360 nm
Tail MOS	W = 1 μm, L = 360 nm
Tail Capacitance	10 μF
Tail Tank	L = 100 pH, C = 10 μF
Cross Coupled MOS(s)	W = 1 μm, L = 200 nm
Capacitor Bank	Co = 15 fF (5 binary weighted capacitors)
Varactor MOS	W = 1 μm, L = 200 nm
Drain Tank	L = 350 pH, C = 1 pF
(V bias, I bias)	Vbias = 1.2 V, Ibias = 7.5 mA

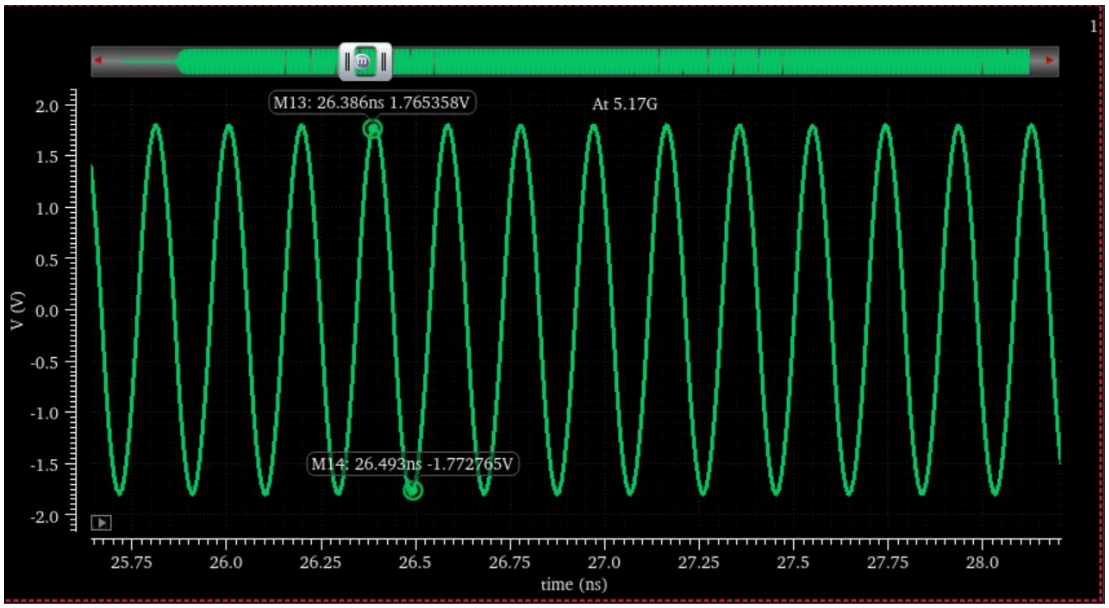
Schematic



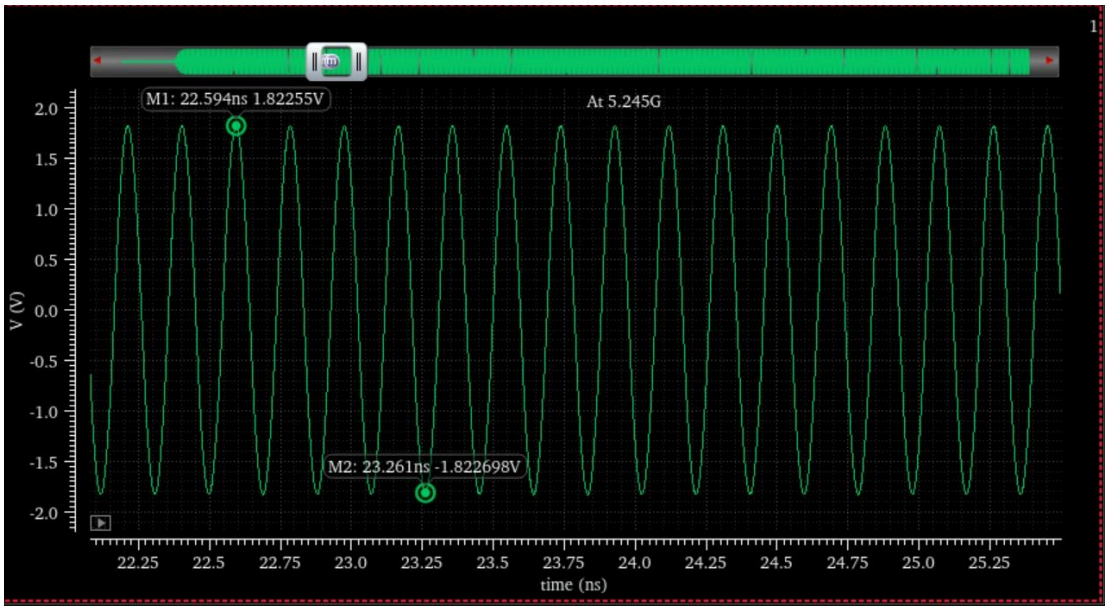


Output Amplitude Plots
(differential settled waveforms)

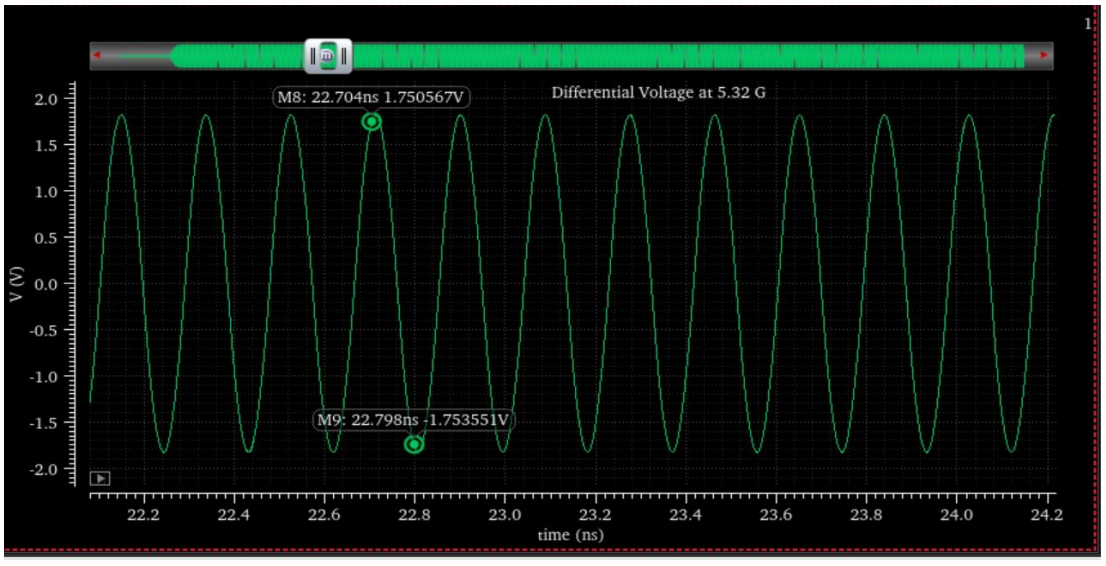
At 5.17 GHz



At 5.245 GHz

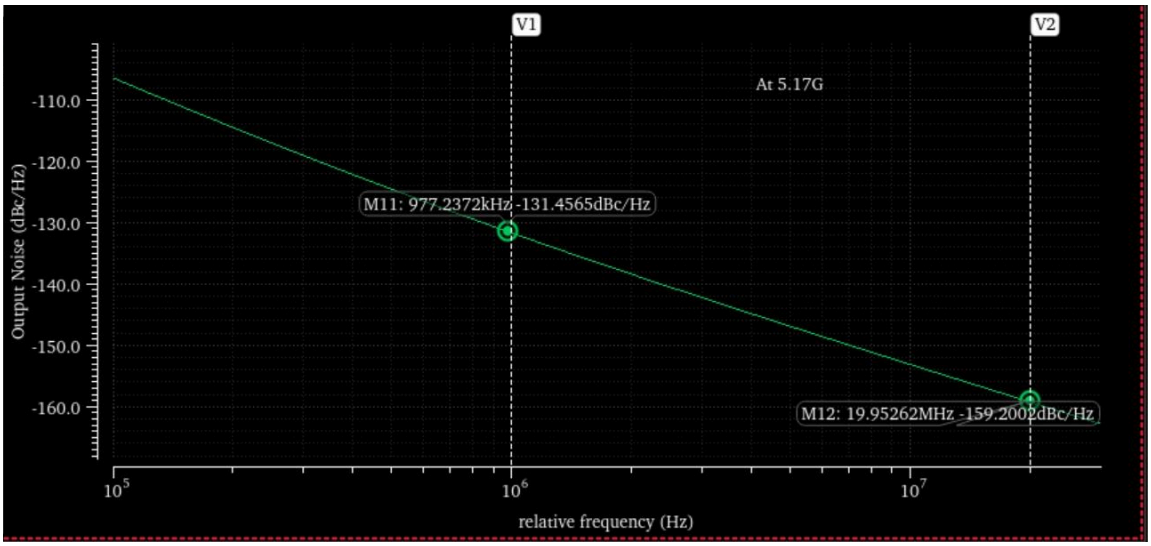


At 5.32 GHz

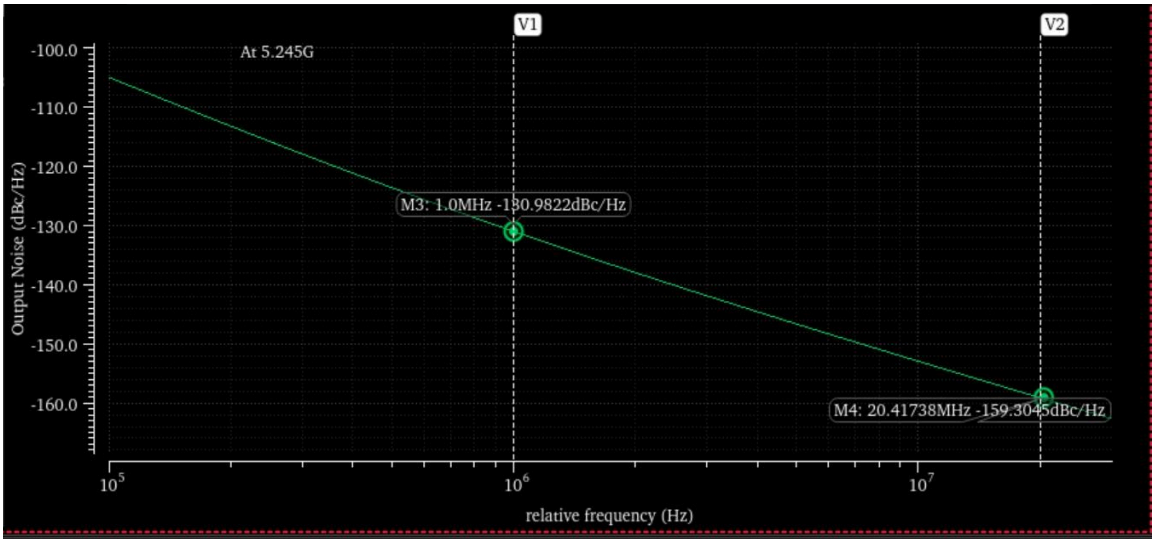


Phase Noise Plots
(at 1 MHz and 20 MHz)

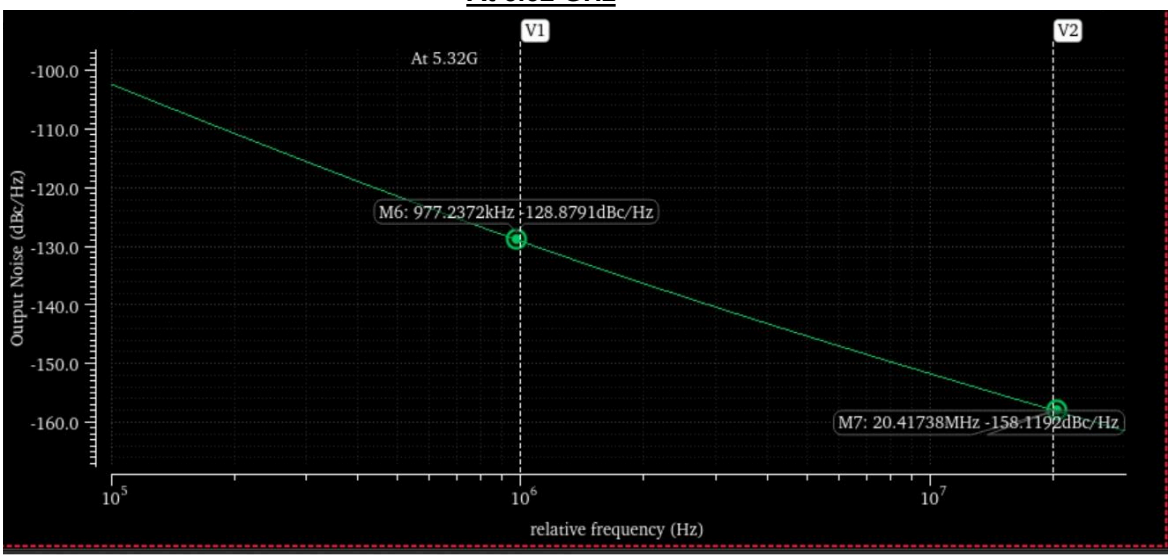
At 5.17 GHz



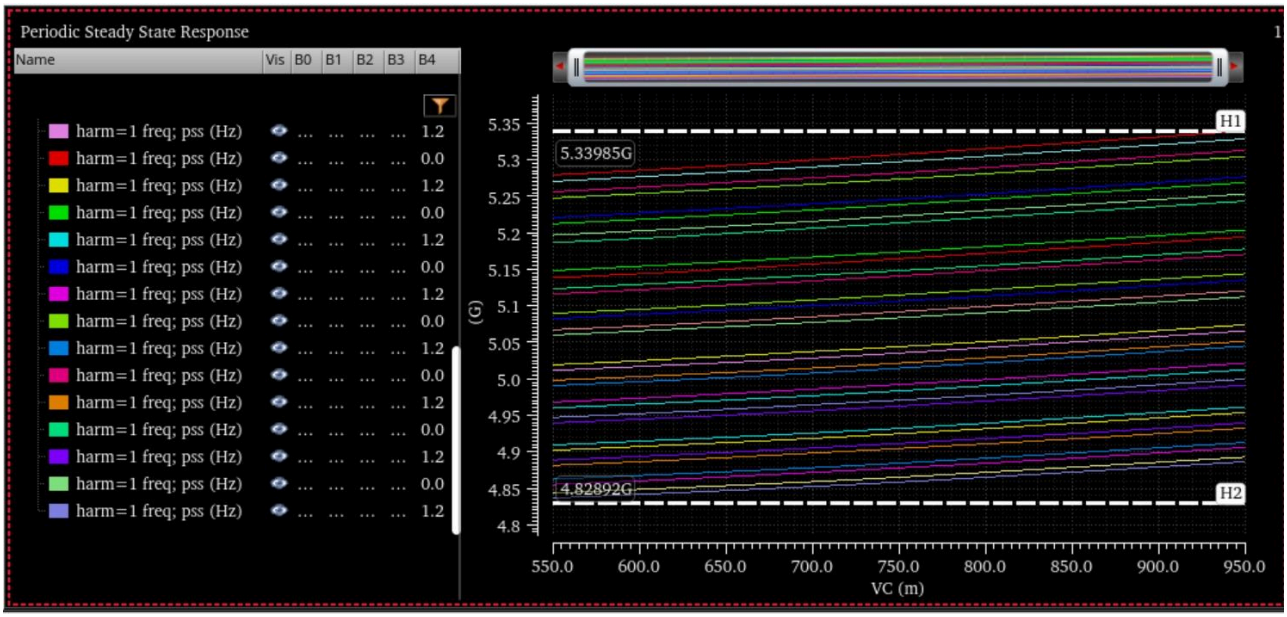
At 5.245 GHz



At 5.32 GHz



Frequency Tuning Range Plot



KVCO Plot

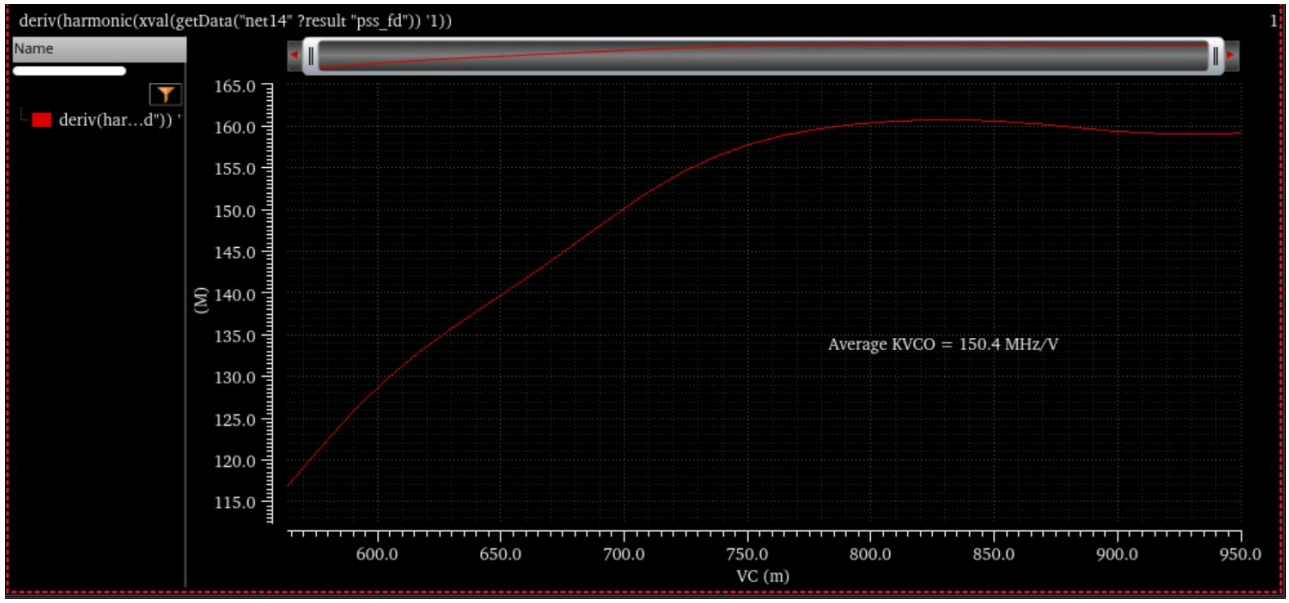


Fig 1 : Average KVCO = 150.4 MHz/V for B0 = B1 = B2 = B3 = B4 = 0

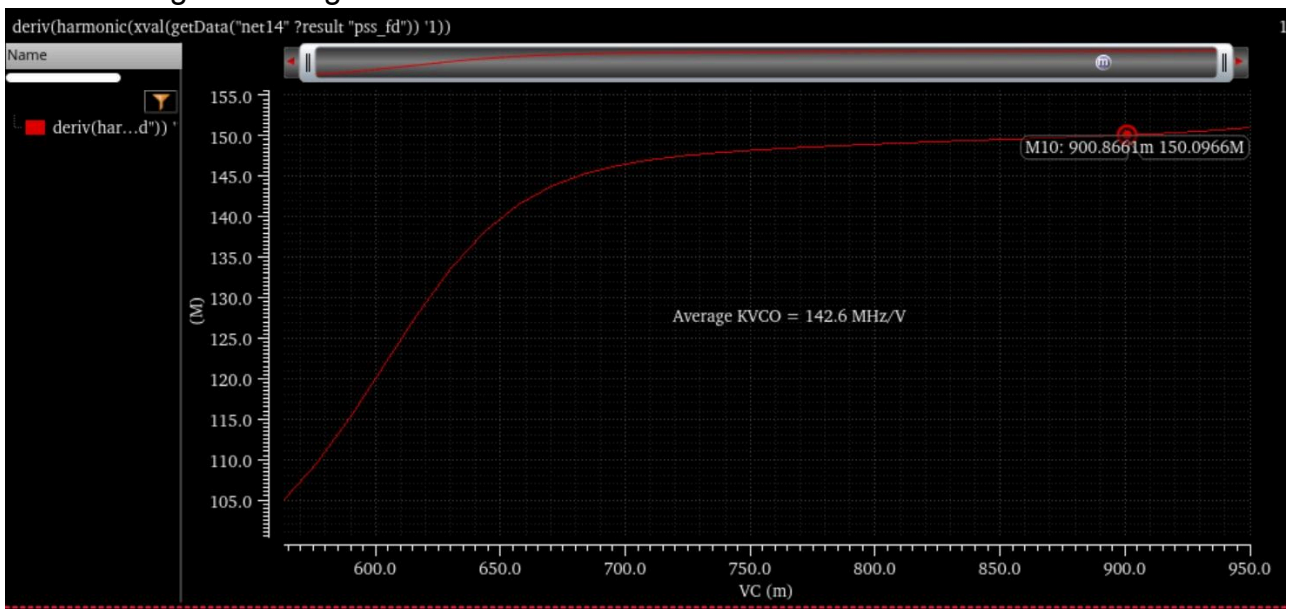


Fig 2 : Average KVCO = 142.6 MHz/V for B0 = B1 = B2 = 1.2, B3 = B4 = 0
(For 5.245GHz at Vc = 900 mV)

Overlap in Coarse Tuning Plots

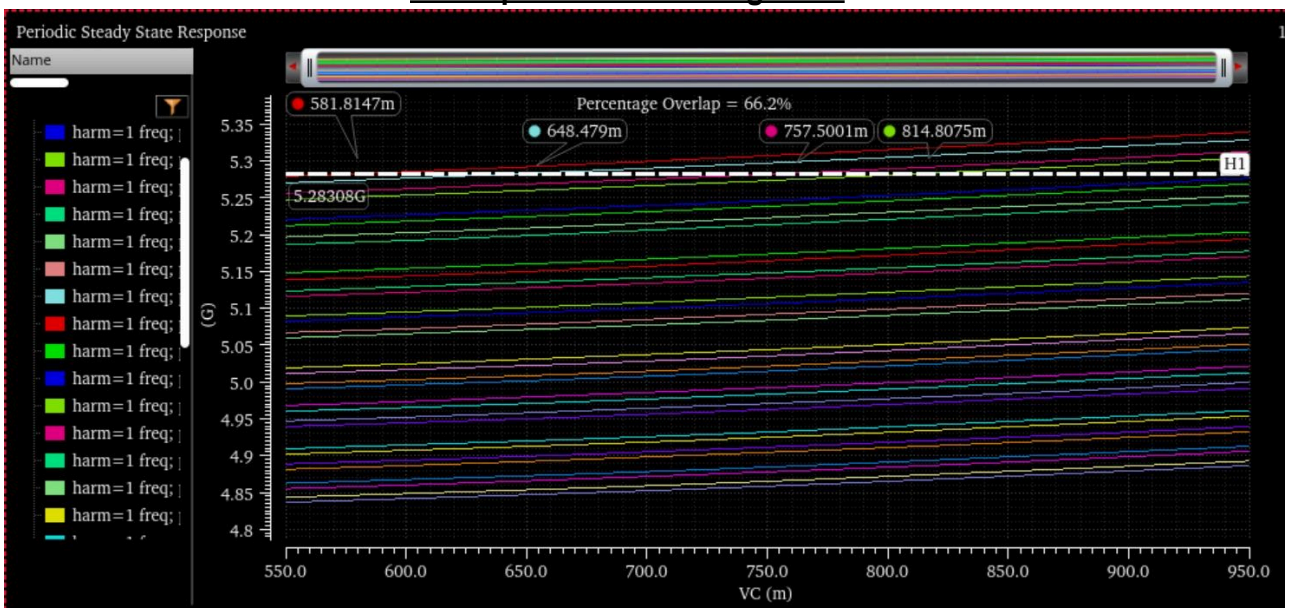


Fig 1 : Overlap between adjacent curves is 66.2%

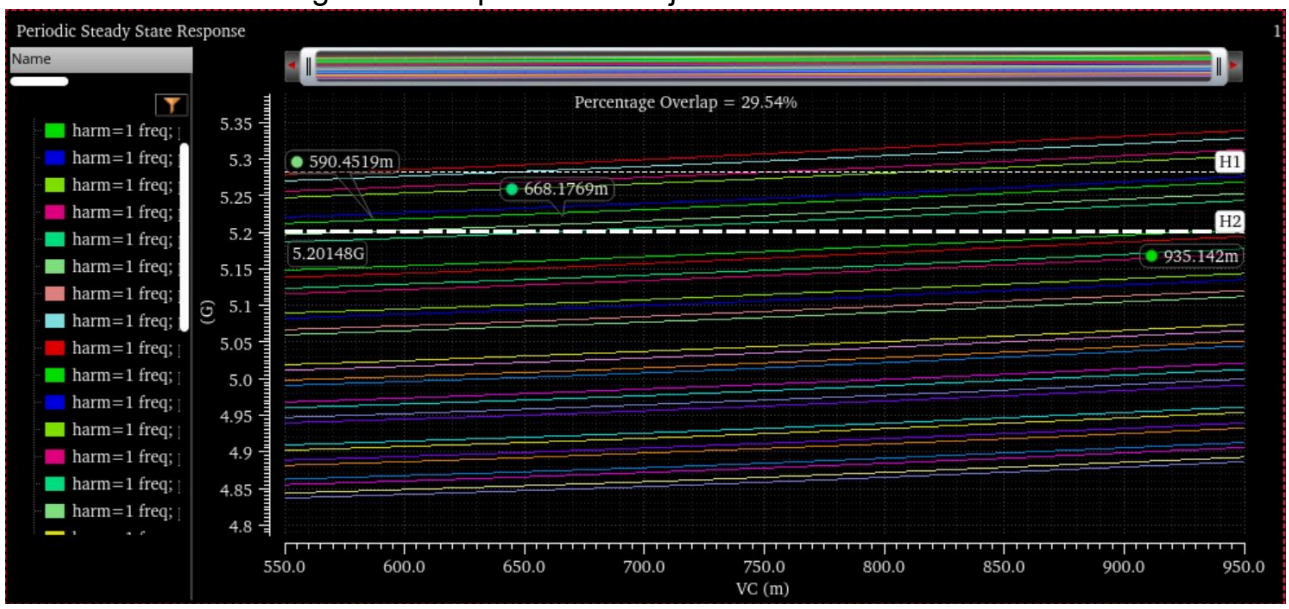


Fig 2 : Overlap between adjacent curves is 29.54%

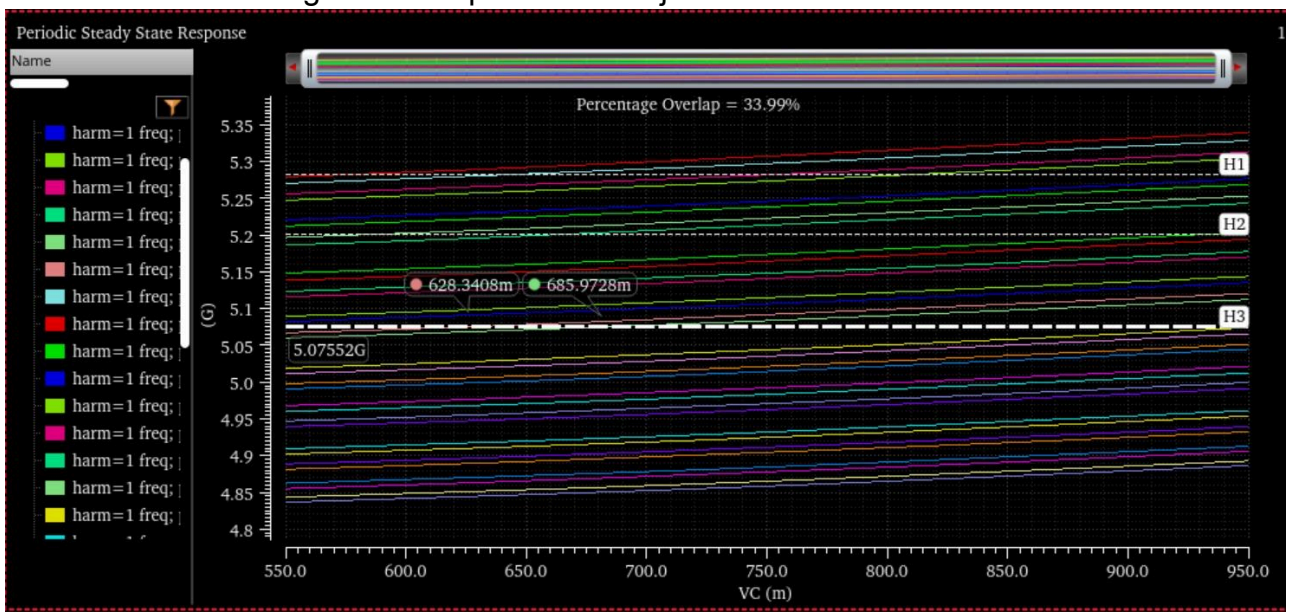
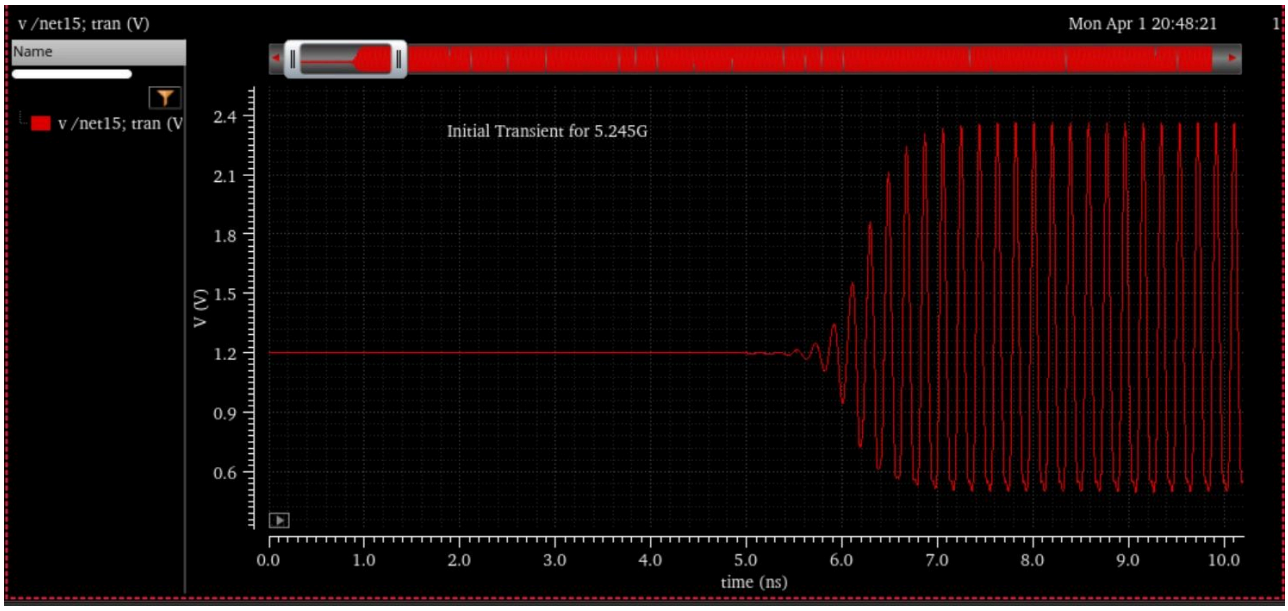
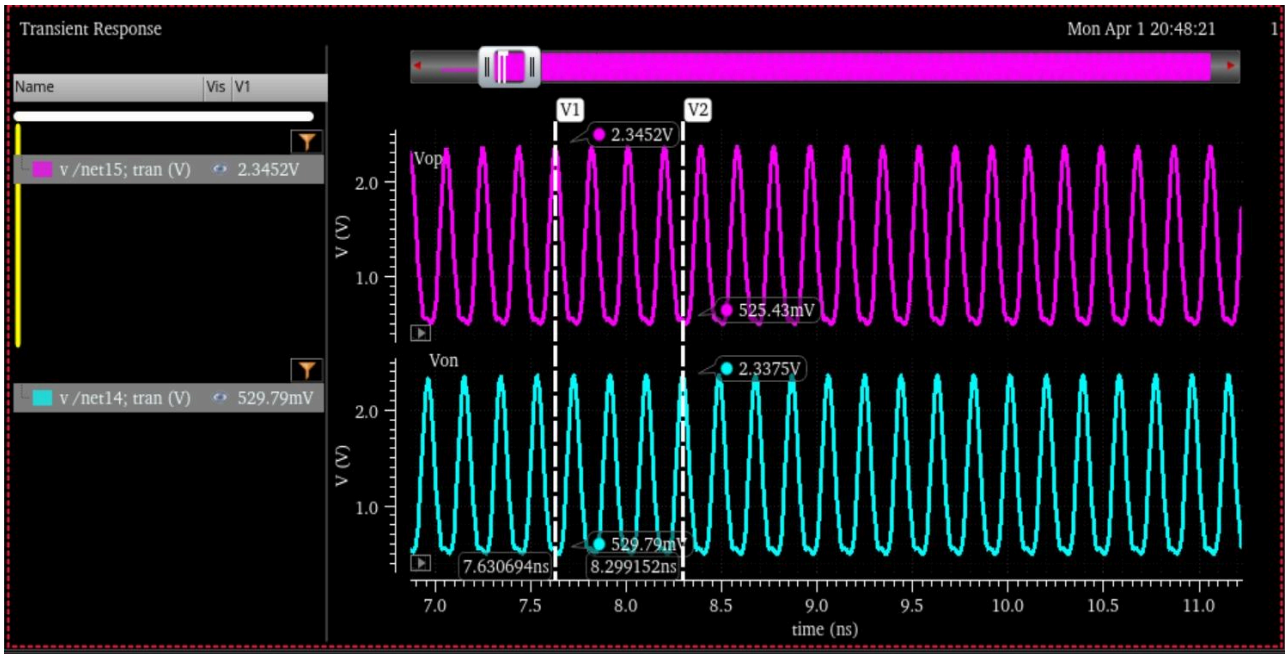


Fig 3 : Overlap between adjacent curves is 33.99%

Initial Transient Response Plot
(for Vop at 5.245 GHz)



Single Ended Output Plot (Vop & Von)
(at 5.245 GHz)



Design Procedure

1. Hand Calculations were performed to find the initial starting point of design
2. Using the hand calculations, the simulation was performed. Specifications were not met.
3. The varactor multiplier and the cross coupled MOS multiplier was adjusted to get required KVCO. Using Ld and Cd the required frequency tuning range was attained.
4. Lt was picked to reject higher order harmonics.
5. The architecture chosen involved capacitor banks for coarse tuning and MOS based varactor for fine tuning. This was chosen so as to have more flexibility over the voltage ranges needed to be attained.
6. The overlap specification of 33% was almost attained on an average.

Path : ee21b019@ams117~/VCO

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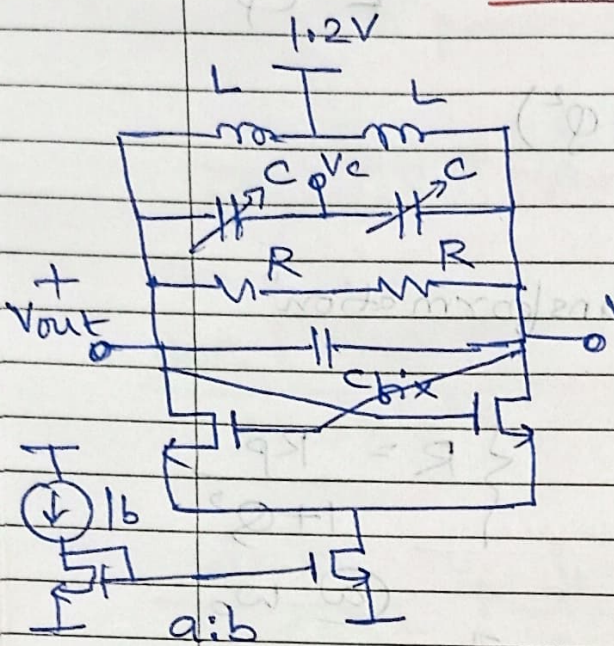
VCO Design
Hand Calculations



Specifications

f_0: 5.17 GHz to 5.32 GHz

$V_{DD} = 1.2V$

VCO single ended output $\geq 0.8V$

From Fourier series,

$$\frac{2}{\pi} I_t R \geq 0.80$$

We will keep $\frac{2}{\pi} I_t R = 1$

So that $I_t R \geq \frac{\pi}{2}$

Single side Analysis

$$\frac{1}{\sqrt{L C_{max}}} = 2\pi \times 5.17 \times 10^9$$

$$\Rightarrow \boxed{C_{max} = 3.79069 \text{ pF} \quad @ L = 250 \text{ pH}.}$$

$$\frac{1}{\sqrt{L C_{min}}} = 2\pi \times 5.32 \times 10^9$$

$$\Rightarrow \boxed{C_{min} = 3.58 \text{ pF} \quad @ L = 250 \text{ pH}.}$$

$$C_{max} = C_{min} + \sum C_i$$

$$\Rightarrow \sum C_i = (1+2+4+8+16) C_0$$

$$= 31 C_0$$

$$31C_0 = 0.21069 \text{ pF}$$

$$\Rightarrow \boxed{C_0 = 6.796 \text{ fF}}$$

$$R = 20 \times (5.245 \times 2\pi \times 10^9) \times 0.25 \times 10^{-9}$$

$$= 164.776\ \Omega$$

$$\Rightarrow \boxed{I_t \geq 9.532 \text{ mA}.}$$