EE6320 RF Integrated Circuits

Project: LNA Design

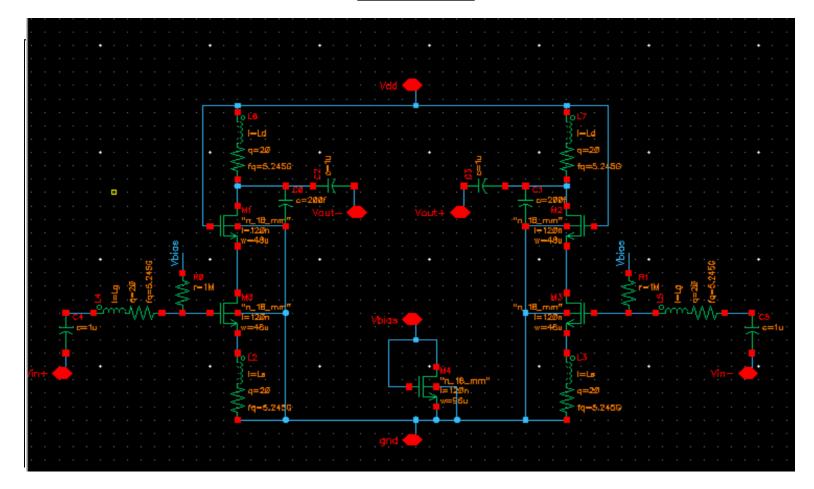
Performance Summary Table

Design metric	Measurement	Simulation Result	Requirement
	Best case S11 in the specified band	-38.94 dB	
	Worst case S11 in the specified band	-14.66 dB	< -10dB
	Band over which S11 ≤ −10dB	5.05GHz to 5.72GHz	5.17GHz to 5.32GHz
Input matching	Band over which S11 ≤ −15dB	5.12GHz to 5.31GHz	-
	Minimum Gain in the specified band	20.80 dB	≥ 20dB
	Maximum Gain in the specified band	21.29 dB	≥ 20dB
	Gain flatness in specified band [Max-Min Gain]	0.49 dB	≤ 2dB
	3dB Bandwidth	0.64 GHz	-
Voltage Gain	Load Capacitance [Differential]	100f F	100f F
	Maximum Noise Figure in the specified band	1.53 dB	≤ 3dB
	Minimum Noise Figure in the specified band	1.49 dB	-
Noise Figure	Band over which NF ≤ 3dB	2.55GHz to 7.88GHz	-
	IIP3 Tones used	5.246GHz, 5.247GHz	-
	Input power used for extrapolation	-30 dBm	-
	Power of Fundamental Tone at output (at	-18.74 dBm	
	chosen input power)		-
	Power of IM3 Tone at output (at chosen input		
	power)	-72.44 dBm	-
Linearity	Extrapolated IIP3	-3.15 dBm	≥ -10dBm
	LNA DC power consumption [Excluding Bias]	1.1 mW	Minimize
Power	Bias circuit power consumption (power supplied	2.4 mW	
	by i_bias)		Minimize
	Sum of all on-chip inductances	8.39 nH	-
	Sum of all off-chip inductances (2 Lg's)	17.7 nH	-
	Sum of all resistances [Including bias]	2 ΜΩ	-
	Sum of all capacitances [Including AC coupling,	4 μF	
•	excluding load]		
Other	Simulator Used	Cadence Spectre	-

Name: ANIRUDH B S

Roll No: EE21B019

LNA Schematic



Component Values (one side values)

Design Component	Hand Calculated Value	Hand Simulated Value
Lg (source inductance)	106.21 nH	8.85 nH
Ls (source inductance)	758 pH	195 pH
Ld (drain inductance)	0.92 nH	4 nH
Rd* (drain resistance)	1 kΩ	2.5 kΩ
R_ls* (res. series with Ls)	1.25 Ω	0.32 Ω
Rg* (res. series with Lg)	175 Ω	14.58 Ω

Fixed Constant Parameters

- LNA MOS parameters: W = 48 μ m , L = 0.12 μ m
- Current Mirror MOS parameters: W = 96 μ m, L = 0.12 μ m
- I_bias (current): 2 mA
- C_coupling: 1 μF

^{* -} intrinsic resistance to respective inductors (doesn't come in net resistance on/off the chip)

Final Component Values

Design Variables			
_ Name	Value		
1 frf	5.245G		
2 prf	-40		
3 Lg	8.85n		
4 Ls	195p		
5 lb	2m		
6 m	1		
7 Ld	4n		
g Rp	2.5K		



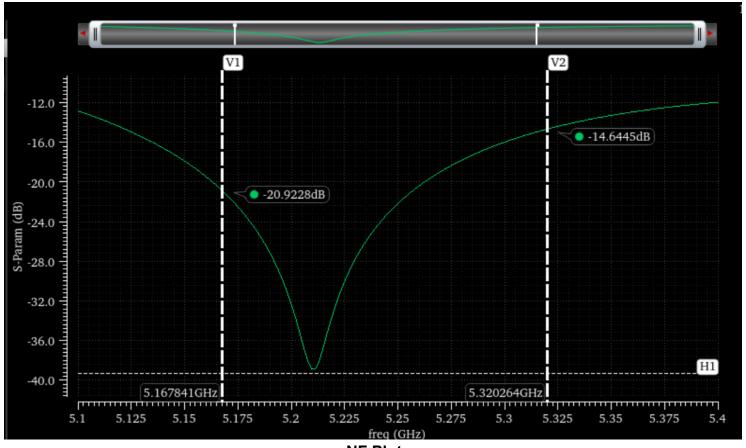
Max Gain through hand calculation: 40 dB

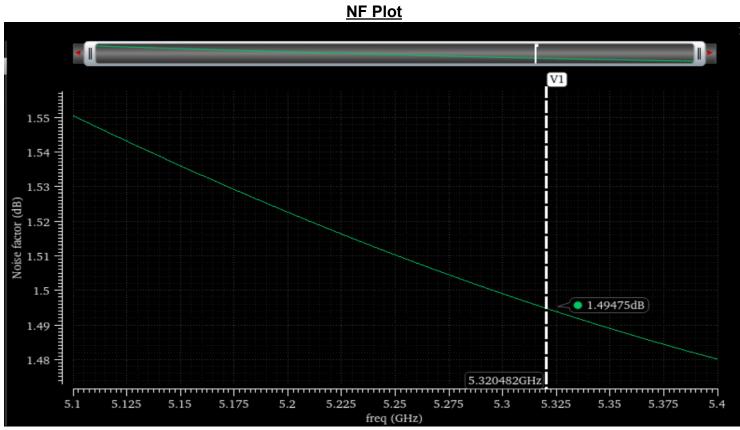
Max Gain from the simulation: 21.3 dB

-3dB Gain comes out to be: 18.3 dB

From the figure, 3dB bandwidth comes out to be: 0.64 GHz

S11 Plot

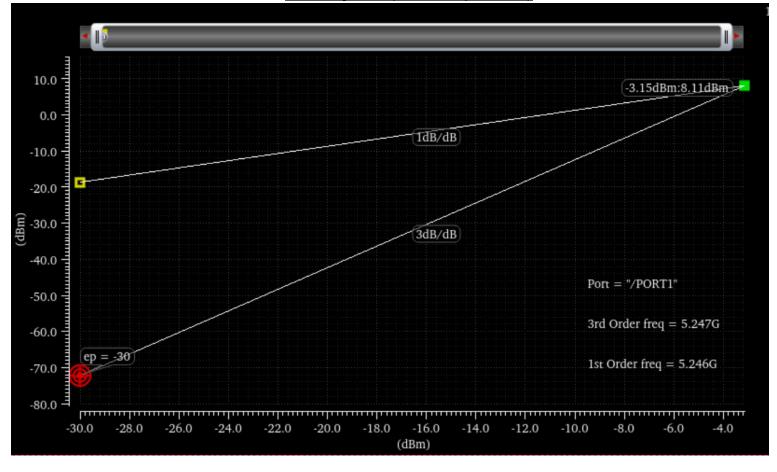




From hand calculations, NF comes out to be: 0.463 dB

From the plot, NF comes out to be: 1.494 dB

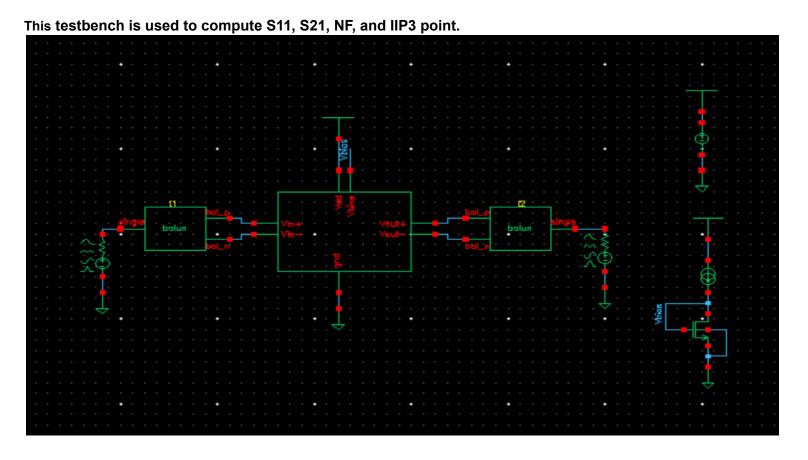
Linearity Plot (IIP3 Computation)



Tones used: 5.246 GHz, 5.247 GHz

IIP3 point comes out to be: -3.15 dBm for an input of -30 dBm

LNA Testbench



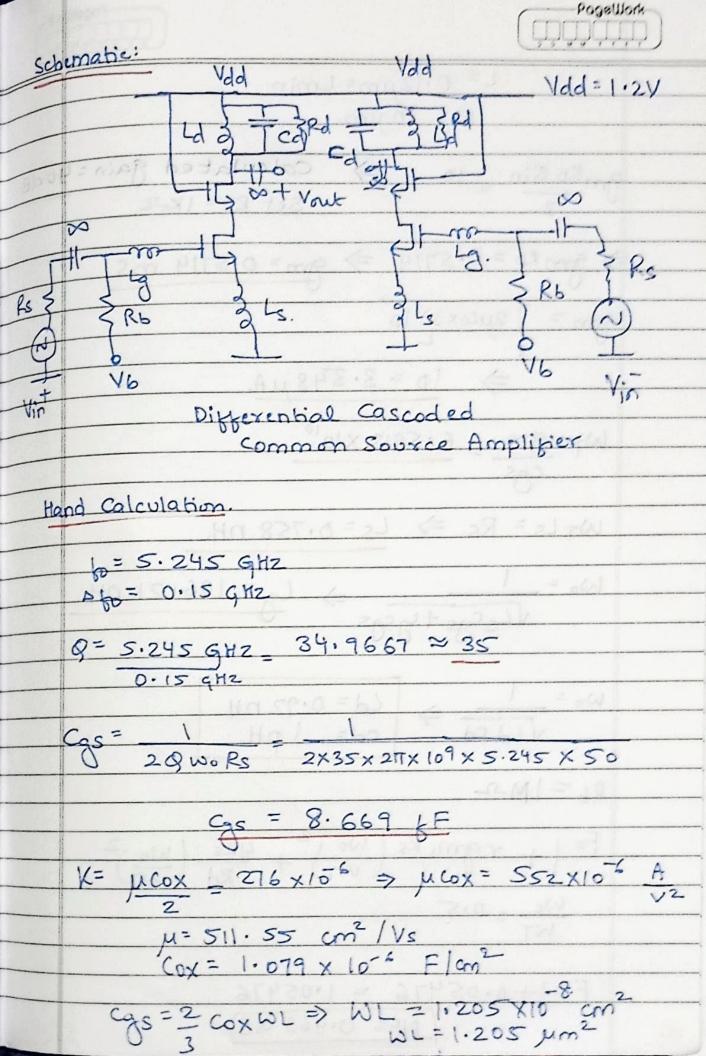
Comments

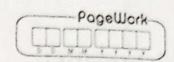
- 1. Improper matching leads to high S11. As soon as the input impedance was set to 50 Ω , there was a sharp drop in the S11. The S11 dip frequency was adjusted by tweaking the values of Lg and Ls. Thus, in my view, Zin is a very critical parameter determining S11.
- 2. Small perturbations in Lg led to large changes in resonant frequency. This appears obvious because the value of Lg is much more than the values of Ls.
- 3. To obtain the required gain, the Rd value needed to be included. Instead of including Rd in the LNA schematic, the Rd is included as the port resistance used in the LNA testbench. This, in principle, is exactly the same as putting Rd in parallel with Ld and Cd.
- 4. The power dissipated was minimized. Power dissipated by the LNA (excluding bias) came to be 1.1 mW, while the bias circuit dissipated 2.4 mW of power.
- 5. Almost no changes needed to be performed in the NF and IIP3. However, the choice of extrapolation point is very critical in IIP3 estimation.

Design Procedure

- 1. Hand Calculations
 - a. Hand calculations were made based on the given specifications using ideal inductor assumptions as discussed in the RFIC video lectures.
 - b. Values obtained using hand calculation were simulated using Cadance Spectre.
- 2. Real inductors with Q = 20 were used in place of ideal inductors.
- 3. Tank inductance and resistance were set based on the Q of the network (Q = 35) from hand calculations.
- 4. Firstly, the plot for Zin was made. The Zin was very much different from 50 Ω due to the effect of parasitics. The parasitics were extracted from the DC operating point and relevant corrections were made in the inductor and capacitor values.
- 5. The S11 was plotted next. Since Zin was adjusted to be around 50 Ω in step 4, the S11 was very low around the center frequency (about -40 dB). Thus, the specification was met here.
- 6. The gain (S21) was plotted. The gain was around 21 dB which met the specification, so no changes needed to be performed here.
- 7. NF was plotted next, the NF came out to be around 1.5 dB which met the specification.
- 8. IIP3 was then plotted for an input power of -30 dBm which gave an IIP3 of -3.15 dBm which met the specifications.
- 9. Biasing resistor was set at 1 M Ω to set the bias point.
- 10. AC Coupling capacitors of 1 μ F were used in all the input and output ports.

Hand Calculations done for the Project





L= 0.12 µm= Lmin W= 10 µm.

gmRD gin 10 => Calculated gain = 40 d8 Set Ro= 1K-2

=> gm RD = 0.5714 => gm = 0.5714 ms

gm = 2 2 4 cox 10

=> 10 = 3.348 MA.

WT= 2m = 6.2913 X1010

WTLS = RS => LS = 0.758 NH.

Wo = 1 = 106.21 nH.

Wo = 1 √Ld cd > Cd = 1 pH

Rh= IM-s

F= | + rgm, Rs | Wo 12 + 4Rs (Wo)2
Rd (WT)

No 20.5

F= 1+0.05476 = 1.05476

NF= 0.463 dB