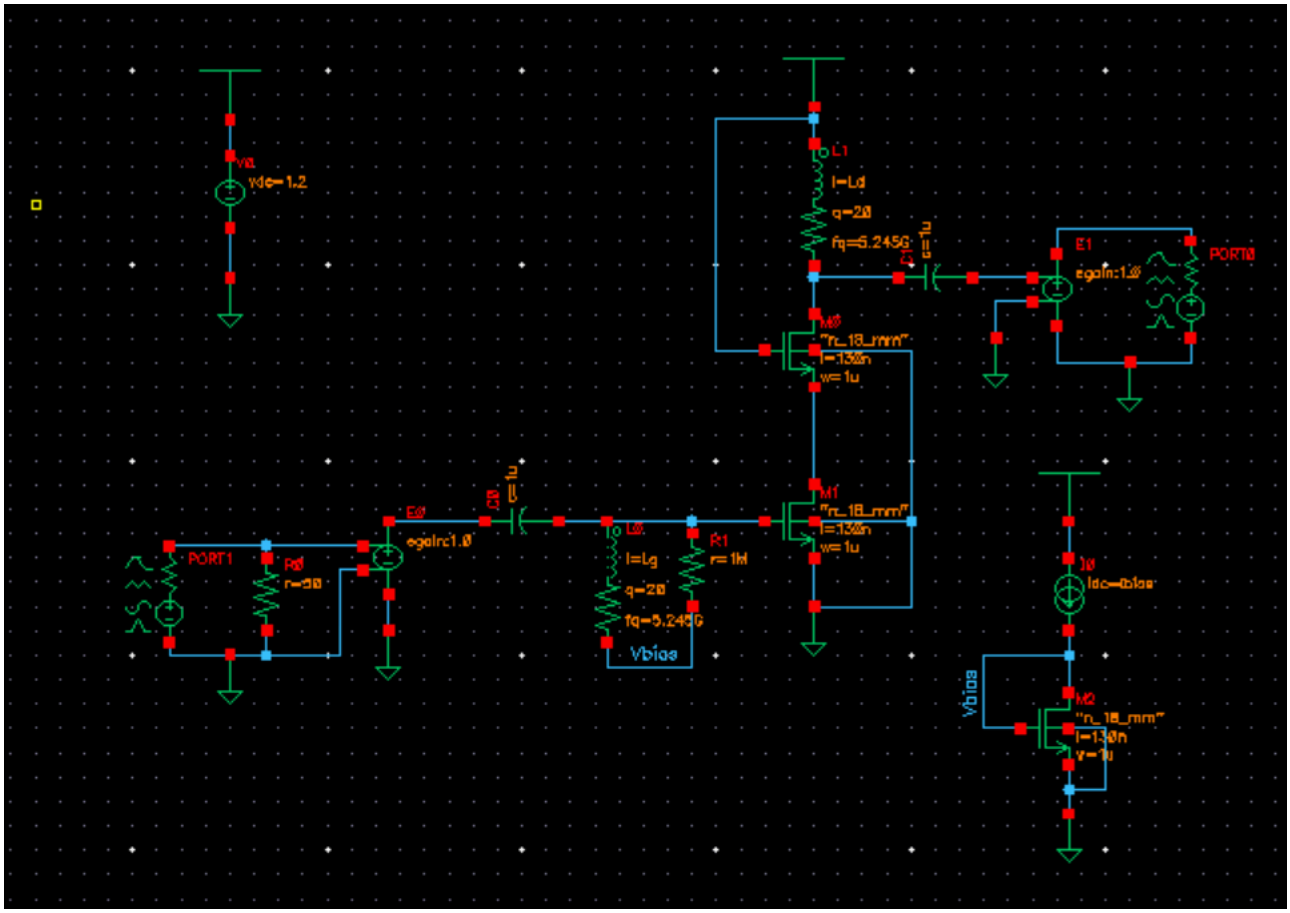
EE6320 RF Integrated Circuits
Project: PA Design

PA Performance Summary Table

Design Parameter	Design Metric	Performance	Specification
Output P1dB	f_o = 5.17 GHz	+10.4068 dBm	$\geqslant$ +10 dBm
	f_o = 5.245 GHz	+11.3505 dBm	$\geqslant$ +10 dBm
	f_o = 5.32 GHz	+12.4042 dBm	$\geqslant$ +10 dBm
AM-PM Deviation (at P1dB)	f_o = 5.17 GHz	1.2821 degrees	$\leqslant$ 5 degrees
	f_o = 5.245 GHz	0.7929 degrees	$\leqslant$ 5 degrees
	f_o = 5.32 GHz	0.0168 degrees	$\leqslant$ 5 degrees
Voltage Gain (from Gate to Drain)	f_o = 5.17 GHz	10.64679 V/V	$\geqslant$ 2
	f_o = 5.245 GHz	10.9020 V/V	$\geqslant$ 2
	f_o = 5.32 GHz	11.16355 V/V	$\geqslant$ 2
Power (at 5.245 GHz)	PA Average Consumption (excluding bias)	5.5707 mW	Minimize
	Bias Circuit Consumption	52 μA	Minimize
Other	Sum of all Capacitances (including ac coupling)	2 μF	-
	Inductance Used	7 nH	-
	Device Width	1 μm	-
	Simulator Used	Cadence Virtuoso	-

Name: ANIRUDH B S
Roll No: EE21B019

PA Schematic



Component Values Table

MOS Amplifier = (W = 1 μm, L = 300 nm)	**Drain Tank = (L = 5 nH)**
Current Mirror MOS = (W = 1 μm, L = 300 nm)	**Bias Current = 52 μA**
R_bias = 1 MΩ, C_coupling = 1 μF	**V_DD = 1.2 V, R_load = 50 Ω**

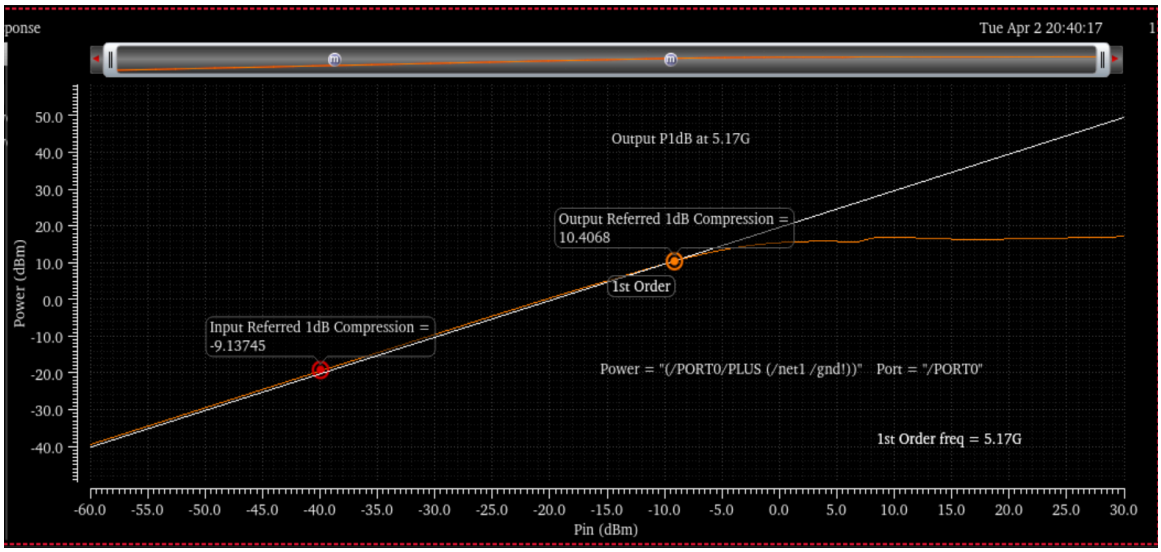
Design Procedure

1. Hand Calculations were performed to find the initial starting point of design
2. Using the hand calculations, the simulation was performed. Specifications were not met.
3. The P1dB compression point was lower compared to the specification. The bias current was increased to meet this specification.
4. Several iterations were performed to meet the specification
5. All the specifications are met.

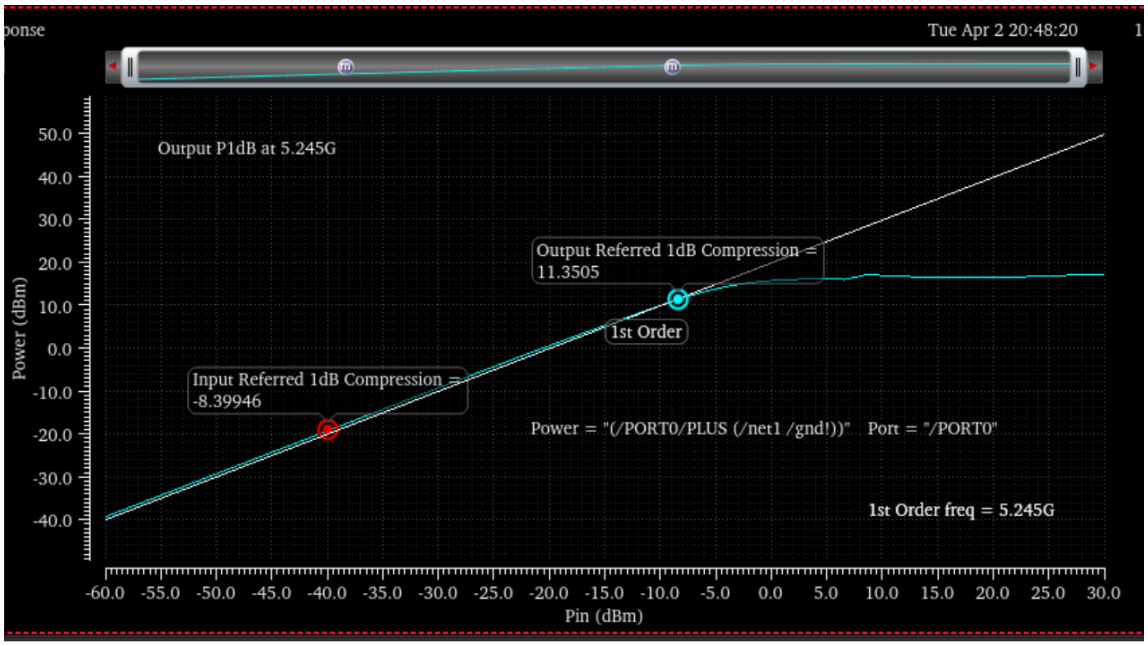
Path : ee21b019@ams117~/PA/PA

Output 1dB Compression Point Plots

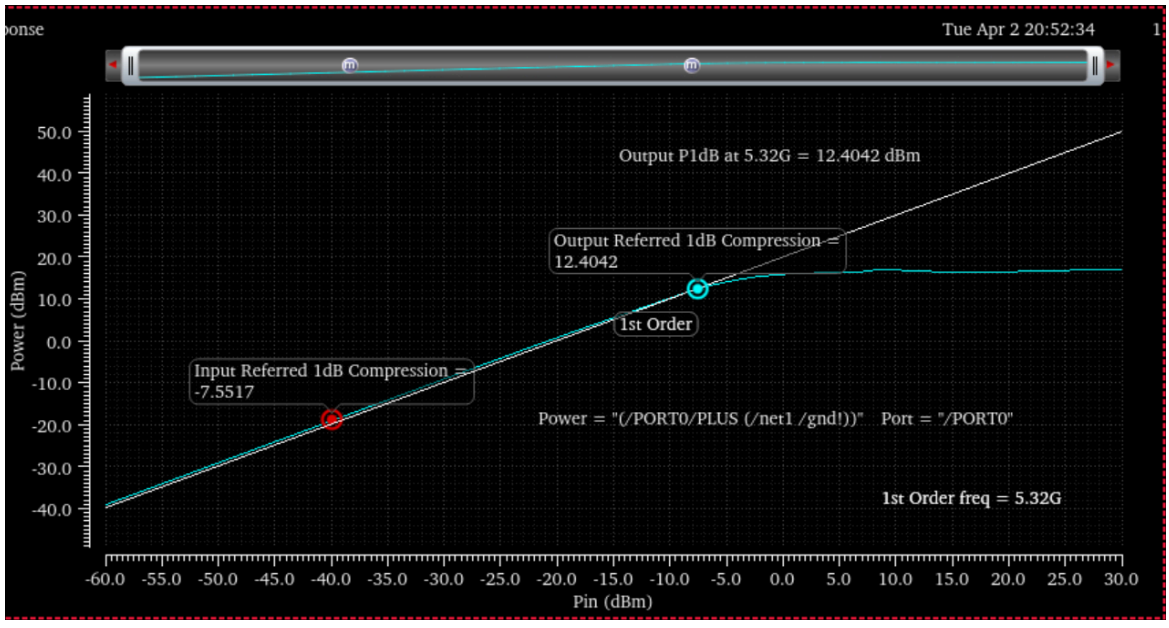
At 5.17 GHz



At 5.245 GHz

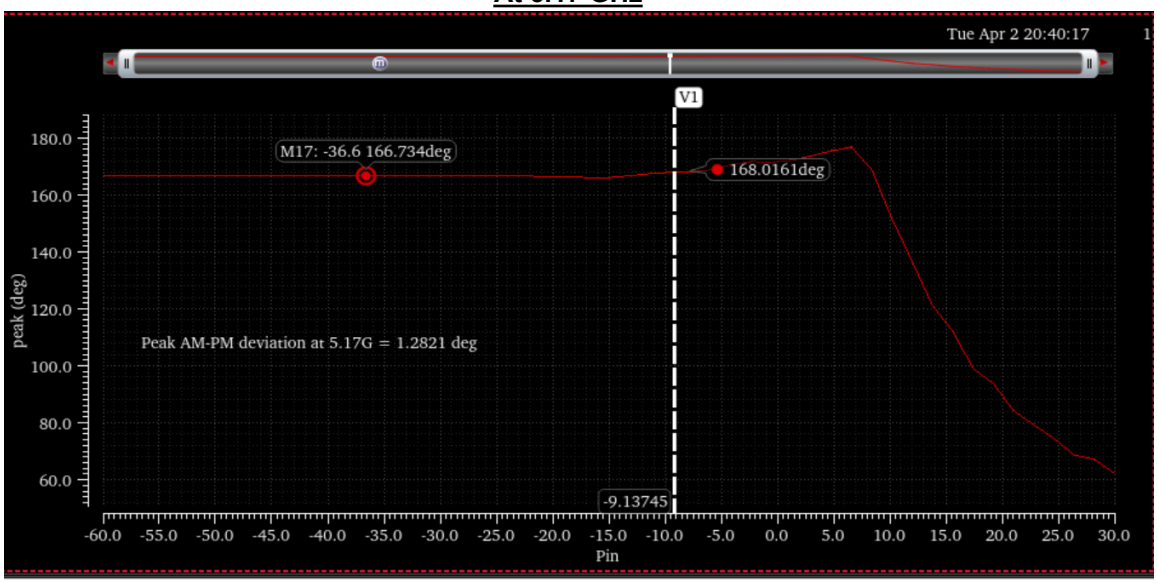


At 5.32 GHz

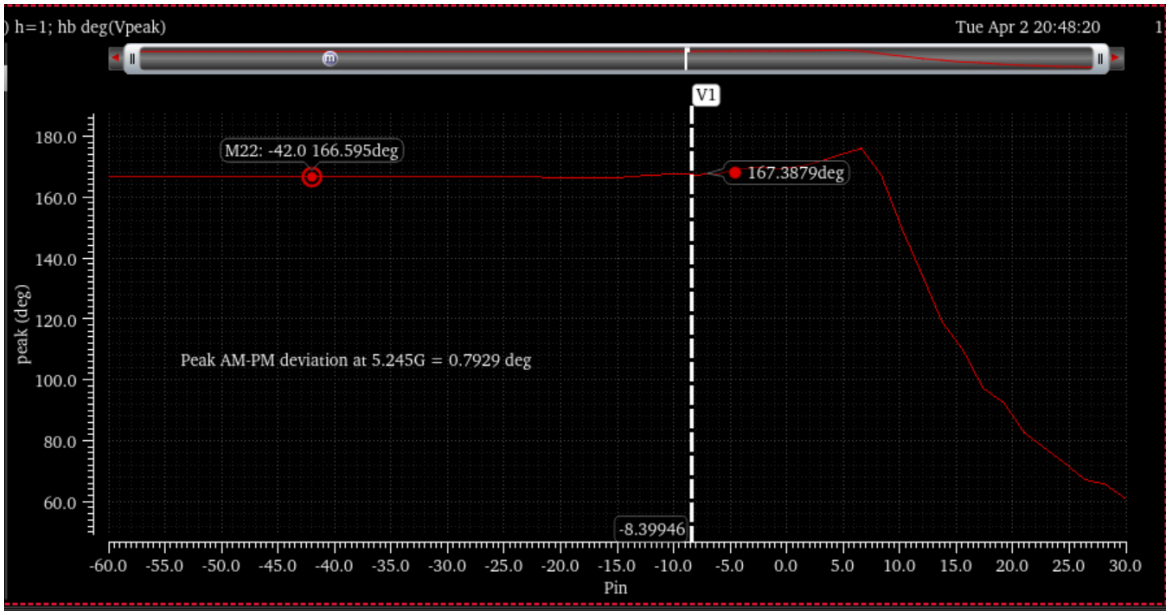


AM-PM Deviation Plots

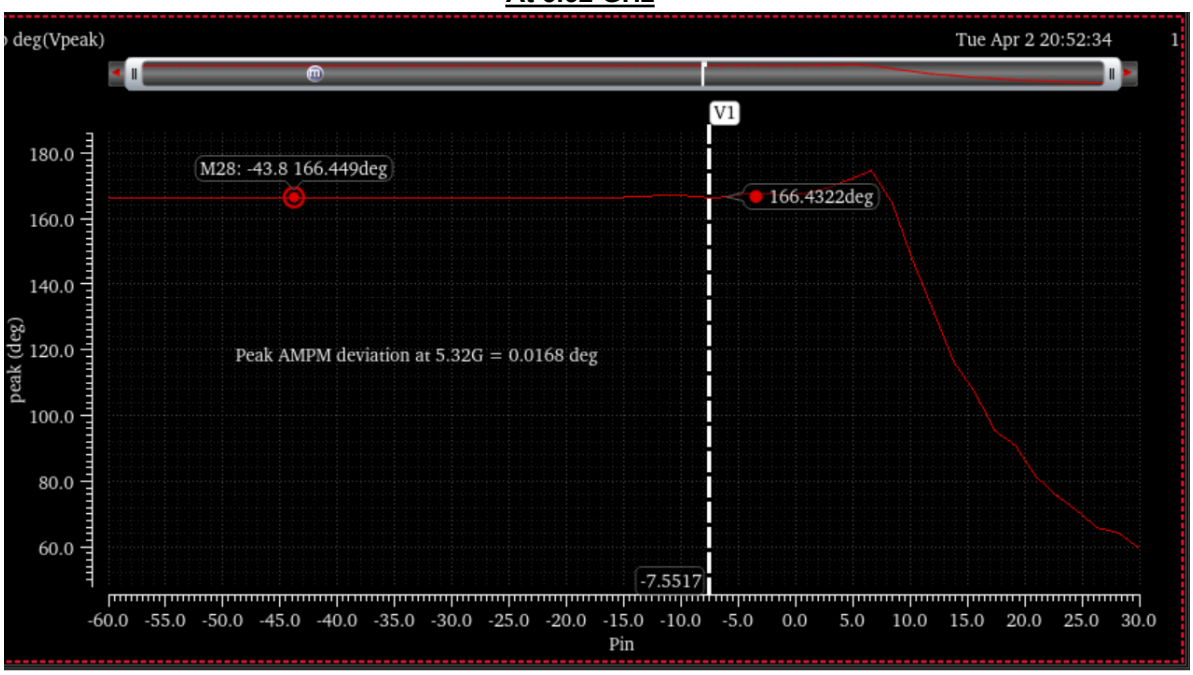
At 5.17 GHz



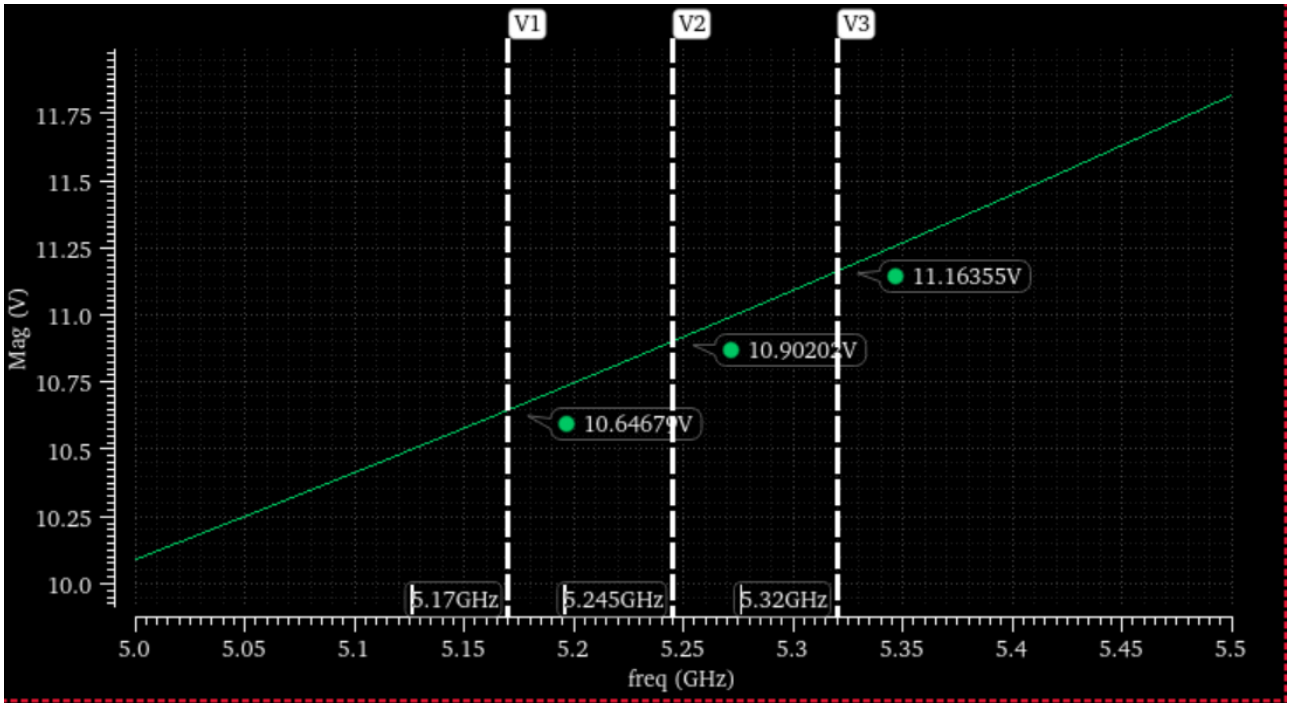
At 5.245 GHz



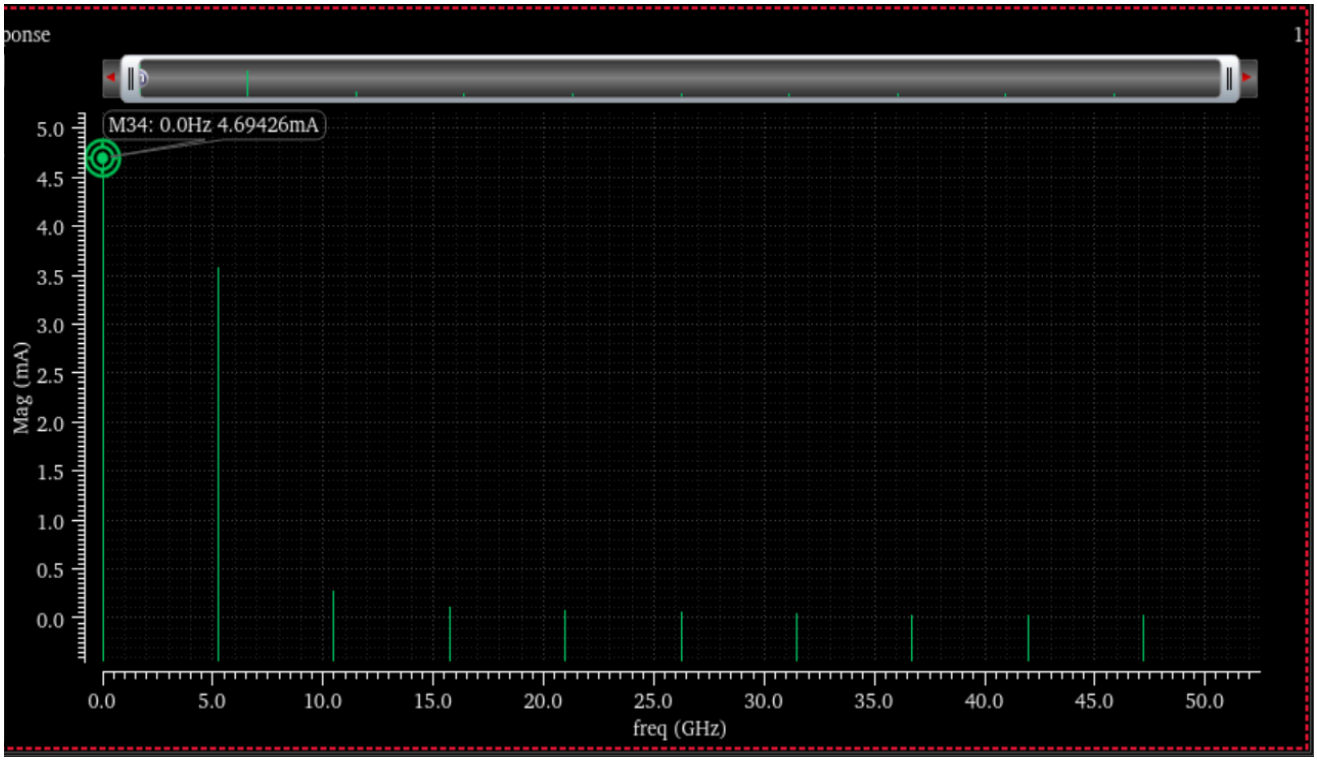
At 5.32 GHz



PA Voltage Gain Plot
(from Gate to Drain)

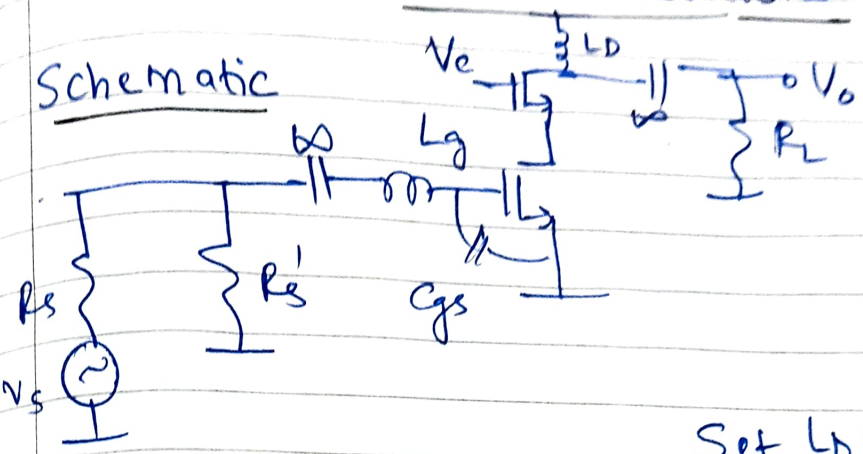


Current through VDD Plot
(at 5.245 GHz)



EE6320: RF Integrated Circuits
PA Design
Hand Calculations

Schematic



Set $L_D = 1nH$.

$$\left|\frac{V_o}{V_s}\right| = \frac{g_m R_L}{2} \geq 2 \qquad f_0 = \frac{1}{2\pi\sqrt{L_g C_{gs}}}$$

$$\Rightarrow g_m R_L \geq 4 \qquad \Rightarrow L_g = 4.185nH$$

Check $\frac{V_{DD}^2}{2R_L} = 14.4mW \geq 10mW$

$\Rightarrow$ No impedance transformation needed.

P: $\frac{(V_{DD} - V_{DSAT})^2}{100} = 10mW$

$\Rightarrow V_{DSAT} = 200mV$

I: $I_{bias} = \frac{1.2 - 0.2}{50} = 20mA$

Set $L = L_{min} = 130nm$

$$\sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} = V_{DSAT} \qquad \mu_n C_{ox} = 552 \times 10^{-6} \frac{A}{V^2}$$

$$\Rightarrow \frac{W}{L} = 1811.59$$

$$\Rightarrow W = 235.5\mu m.$$

$$C_{gs} = \frac{2}{3} C_{ox} W L = \frac{2}{3} \times 1.079 \times 10^{-6} \times 0.13 \times 10^{-8} \times 235.5$$

$$= 0.22pF$$