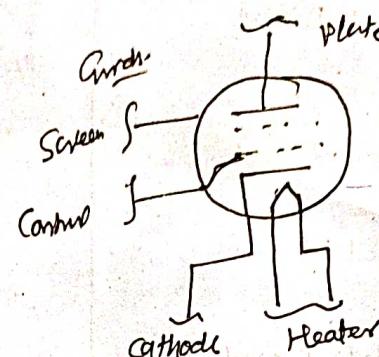


Bipolar Junction Transistor (BJT)

Unit #2

It was invented in 1951 by Dr. William Shockley and Dr. John Bardeen at Bell Laboratory in USA.

- (*) It was replacement of bulky vacuum tubes with few advantages-
- NO heating filament is required
 - Smaller size and light weight
 - Very low operating voltage
 - Great circuit efficiency
 - Long life with no ageing effect
 - They are essentially shock proof
 - Used for amplification of weak signal and switching applications.



(**) BJT stands for Bipolar Junction Transistor.

Conduction of current through Both majority & minority carriers

There are Two Junctions
 $J_1 \rightarrow$ Between Emitter & Base
 $J_2 \rightarrow$ Between Collector & Base

TRANSFER RESISTOR

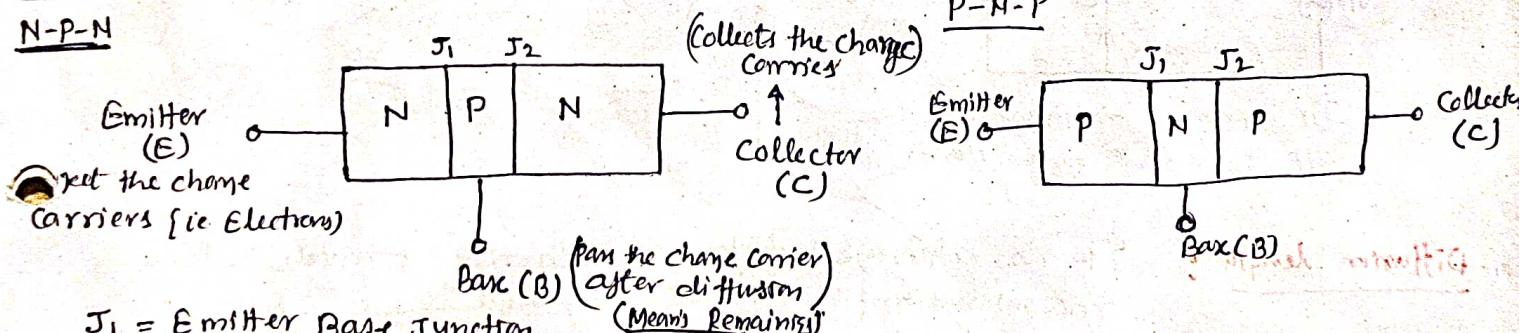
Transfer of ~~Weak~~ Weak Signals from Low Resistance to High Resistance

(***) BJT is a Three Terminal device i.e. Emitter, Base, Collector.

(****) BJT is a current controlled device i.e. if Voltage, current or power all are controlled by input current.

② Physical Structure

N-P-N



$J_1 =$ Emitter Base Junction

$J_2 =$ Collector Base Junction

For width ~~ratio~~ $C > E > B$

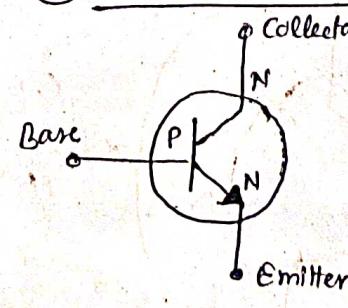
$E > C > B$

Doping

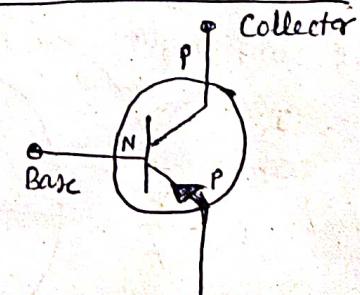
→ Adding Impurity

to create same no. of majority and minority carriers.

③ Symbolic Representation of Transistor



N-P-N Transistor



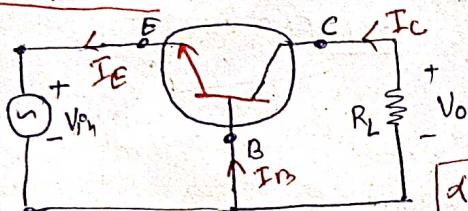
P-N-P Transistor

NOTE * NPN Transistor is mostly used than PNP because in NPN, current conduction mainly depends upon "Electrons" and in PNP on "Holes" but the mobility of electrons is higher than holes. { mobility = $\frac{\text{drift velocity}}{\text{Applied Electric field}}$ }

BIASING OF TRANSISTOR

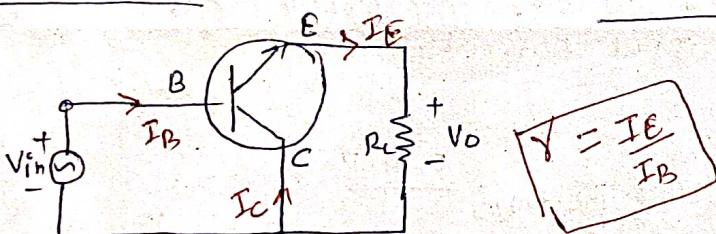
	J ₁ Emitter-Base Junction	J ₂ Collector-Base Junction	Region
①	Forward-Biased	Reverse-Biased	Active (Amplification of weak signal)
②	Forward-Biased	Forward-Biased	Saturation (ON-switch)
③	Reversed-Biased	Reversed-Biased	Cut-off (OFF-switch)
④	Reversed-Biased	Forward-Biased	Inverted Region (Attenuator)

CB Configuration



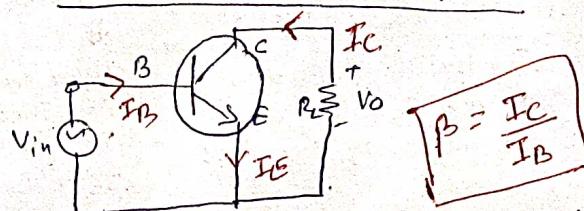
Input terminal = Emitter
O/P Terminal = Collector

Common Collector



IIP Terminal \Rightarrow Base
OIP Terminal \Rightarrow Emitter.

Common Emitter Configuration



IIP Terminal = Emitter-Base
OIP Terminal = Collector

Diffusion length: It is a average distance a carrier travels before recombination.

Lifetime:- Average time for which carrier survives or travels.

CE Configuration

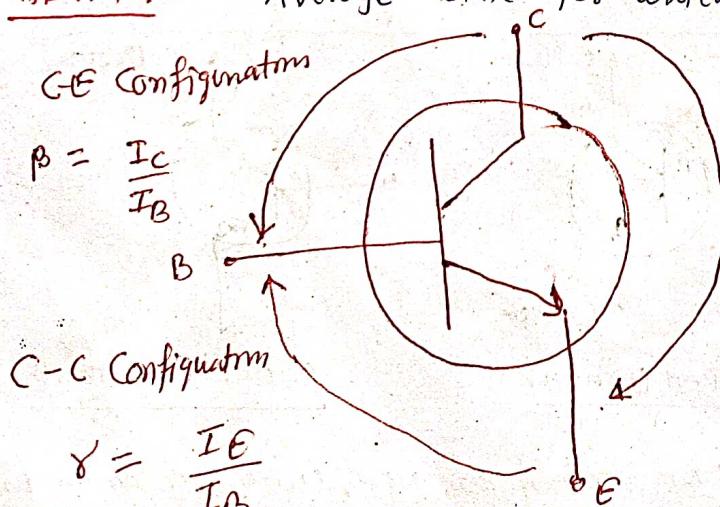
$$\beta = \frac{I_C}{I_B}$$

C-C Configuration

$$\gamma = \frac{I_E}{I_B}$$

CB Configuration

$$\alpha = \frac{I_C}{I_E}$$



NPN Transistor

Emitter < majority carrier \rightarrow Electrons
minority carrier \rightarrow Holes

Base < majority carrier \rightarrow Holes
minority carrier \rightarrow Electrons

Collector < majority " \rightarrow Electrons
minority " \rightarrow Holes

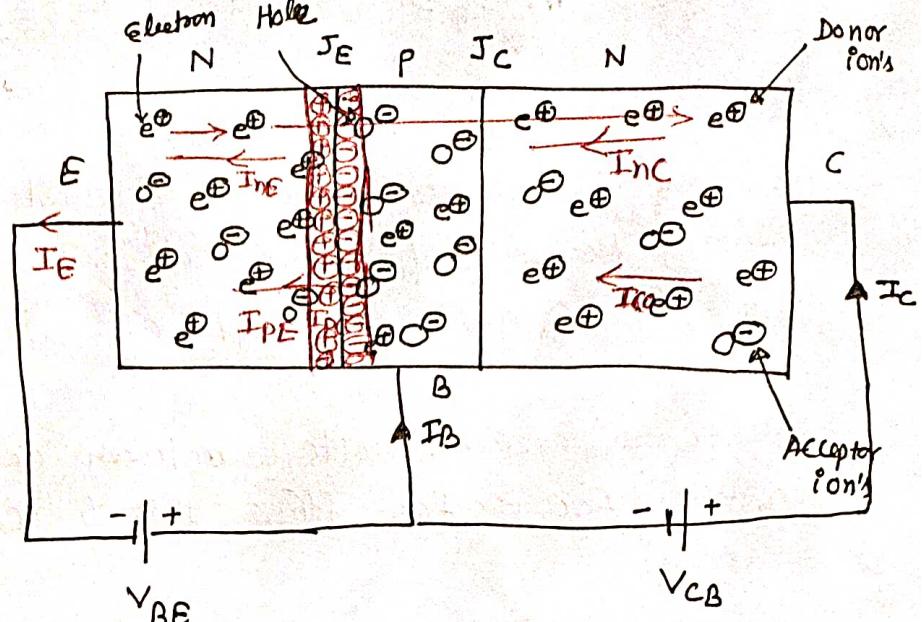
Velocity wise $\Rightarrow V_E > V_B > V_C$

width wise $\Rightarrow W_C > W_E > W_B$

Doping wise $\Rightarrow D_E > D_C > D_B$

$J_E \rightarrow$ Emitter Base Junction or Emitter Junction

$J_C \rightarrow$ Collector-Base Junction or Collector Junction.



(*) For Active region (or Amplification of weak signal), Emitter junction \rightarrow forward biased
Collector junction \rightarrow Reverse biased.

(**) When J_E junction is forward biased, electrons travel from Emitter to base and holes travel from base to Emitter, which results I_{NE} (Electron current through Emitter junction) and I_{PE} (Hole current through Emitter junction) starts to flow from base to Emitter respectively.

Then Net Emitter Current (I_E) = $I_{NE} + I_{PE}$
But $I_{PE} \ll I_{NE}$ so $I_E \approx I_{NE}$

(***) When electrons enter Pn base region, a few of them are recombined with holes and create a depletion region at J_E junction and remaining electrons enter in collector region, so that I_{NC} (Electron current through Collector junction), starts to flow.

(****) The collector region is +ve with respect to base, and this voltage attracts more and more electrons, when V_{CB} is increased, means I_{NC} is also increased.

Transistor factor (α) or Amplification factor = $\frac{e^s \text{ current through } J_C}{e^s \text{ current through } J_E}$

$$\alpha = \frac{I_{NC}}{I_{NE}}$$

$$\text{But } I_{NE} \approx I_E \text{ so } \alpha = \frac{I_{NC}}{I_E} \text{ or } I_{NC} = \alpha I_E$$

(*****) The created depletion region at J_E , opposes the movement of electron and holes across the J_E , therefore base region supplied with compensating holes from base biasing to make it neutral. and due to this compensating holes, base current is also starts to flow. ie

$$I_B + I_{NC} = I_{NE} + I_{PE} \text{ But } I_{PE} \ll I_{NE}$$

$$I_B + I_{AC} = I_{nE} \quad \text{or} \quad I_B = I_{nE} - I_{AC}$$

* If the holes supply to base region increased then base become more +ve and it attracts large no. of electrons from emitter and vice-versa. Therefore, the flow of charge carriers is controlled by Holes supply to base or base current, called Current Controlled device.

(*) Due to the reverse voltage between collector and base, reverse saturation current I_{CO} or I_{CB0} flows through collector junction due to minority carriers.

Apply the KCL at collector region.

$$I_C = I_{nC} + I_{CB0} = \underbrace{I_{nC}}_{\downarrow \text{Majority carrier}} + \underbrace{I_{CO}}_{\downarrow \text{Minority carrier}}$$

But $I_{nC} = \alpha I_E$ then

$$I_C = \alpha I_E + I_{CB0} \quad \text{--- (1)}$$

$$\text{But } I_E = I_C + I_B$$

$$\text{Then } I_C = \alpha(I_C + I_B) + I_{CB0} = \alpha I_C + \alpha I_B + I_{CB0}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CB0}$$

most
Common Base

$$\text{or } I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \frac{I_{CB0}}{(1-\alpha)}$$

Where-

$I_{CB0} \rightarrow$ leakage current between collector to base region when Emitter is open.

$$\text{But } \beta = \frac{\alpha}{1-\alpha}, \text{ and } 1+\beta = 1 + \frac{\alpha}{1-\alpha} = \frac{1}{1-\alpha}$$

$$\text{Then } I_C = \cancel{\beta I_B} + (1+\beta) I_{CB0} \Rightarrow \underline{\text{Common Emitter}}$$

A Transistor having $\alpha = 0.975$ and reverse saturation current $I_{CB0} = 10 \mu\text{A}$, operated in Common Emitter mode. If the base current is $250 \mu\text{A}$, calculate I_E & I_C .

$$\alpha = 0.975$$

$$I_{CB0} = 10 \mu\text{A} = 10 \times 10^{-6} \text{ A}$$

$$I_B = 250 \mu\text{A} = 250 \times 10^{-6} \text{ A}$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.975}{1-0.975}$$

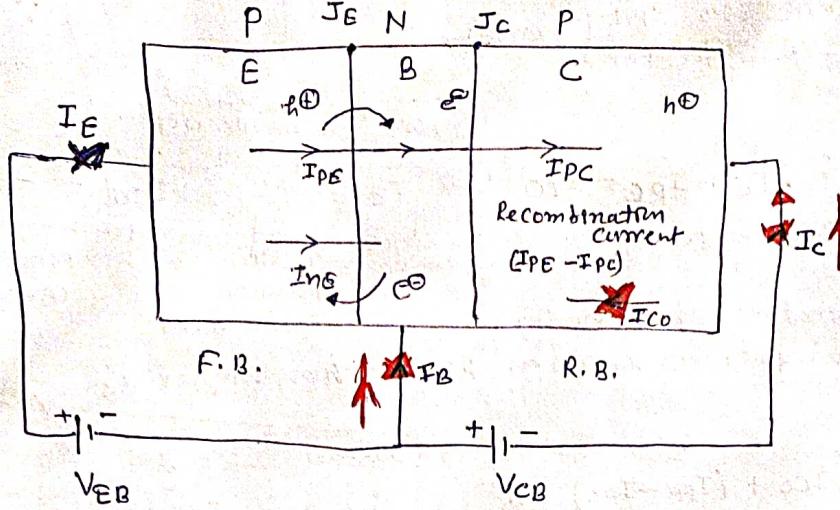
$$\begin{aligned} I_C &= \cancel{\left(\frac{\alpha}{1-\alpha}\right) I_B} + \cancel{\frac{I_{CB0}}{(1-\alpha)}} = \left[\frac{0.975}{1-0.975} \right] * 250 \times 10^{-6} \\ I_C &= \beta I_B + (1+\beta) I_{CB0} \\ \text{--- (1)} \quad I_C &= 10.15 \text{ mA} \end{aligned}$$

and (2)

$$I_E = I_C + I_B = 10.15 \text{ mA} + 250 \mu\text{A}$$

$$= [0.15 \times 10^3 + 250 \times 10^{-6}] = \underline{\underline{10.4 \text{ mA}}}$$

Working of PNP transistor in Active Region :



Physical Structures
Assume of PNP Transistor

$V_E > V_B > V_C \Rightarrow$ Velocity

$W_E > W_B > W_C \Rightarrow$ Width

$D_E > D_B > D_C \Rightarrow$ Doping

$I_{PE} \rightarrow$ Hole current through Emitter Junction

$I_{NE} \rightarrow$ Electron current through Emitter Junction

(*) For Active mode operation of PNP transistor $V_E > V_B > V_C$ & Emitter-Base Junction forward biased and Collector-Base junction is reversed biased.

(**) Due to F.B. of JE junction, holes travel from emitter to base, which result I_{PE} current and electrons from base to emitter, which results I_{NE} current.
Then Net Emitter current $(I_E) = I_{PE} + I_{NE}$

But Emitter is heavily doped, so $I_{PE} \gg I_{NE}$ so $I_E \approx I_{PE}$

Emitter Injection efficiency (η) = $\frac{I_{PE}}{I_E} = \frac{\text{Current through JE due to carrier of Emitter}}{\text{Total current through JE}}$

(*) When holes enter in base region, a few of them are recombined with e^- of base and remaining holes reach to collector region in the form of ~~current~~ Current I_{PC}

(**) Due to reverse bias of JC, collector region has -ve voltage w.r.t. base and this voltage attracts holes current I_{PC} flow into collector region.

Transportation factor (β^* or α_T) = $\frac{I_{PC}}{I_{PE}} = \frac{\text{Holes current through JC}}{\text{Holes current through JE}}$

that measures how efficiently carriers are transported through base.

(***) Due to the recombination holes and e^- are lost. If the base region loses its e^- in recombination, it becomes +ve that may oppose movement of holes from emitter to collector. Therefore the base region supplied with compensating e^- from base biasing supply to keep it neutral. No compensating e^- produces current ($I_{PE} - I_{PC}$), called recombination current and almost equal to recombination current or base current.

(****) If e^- supply to base increased, then base becomes -ve and it attracts large no. of holes from emitter and vice-versa. So flow of electron e^- controlled by e^- supply to base or base current, called as "current controlled device".

(*) Due to the Reverse Voltage 'V_{CB}', a reverse saturation current (I_{CO}) also flows through collector junction.

$$I_{CO} \rightarrow +ve \text{ for NPN }] \text{ Transistor}$$

$$I_{CO} \rightarrow -ve \text{ for PNP }$$

KCL at Collector Junction:

~~Minority carrier current~~

~~Majority carrier current~~

Collector Current is combination of majority and minority carrier currents so known as "Bipolar Junction Device".

KCL at Base Junction

$$I_B \neq I_{nE} + I_{CO} + (I_{pE} - I_{pC}) = 0$$

$$\text{or } I_B = - \left[\underbrace{(I_{pE} - I_{pC})}_{\text{Recombination current}} + I_{CO} + I_{nE} \right]$$

(**) Base current depends mainly upon recombination current ($I_{pE} - I_{pC}$)

$$I_B \approx - (I_{pE} - I_{pC})$$

Current Gain (α),

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$\text{or } \alpha_{dc} = \frac{I_C}{I_E}$$

Current equation for Transistor -

$$\text{or } I_E = -(I_B + I_C) \quad \text{--- (2)}$$

$$\text{From (1) & (2) } I_C = \alpha(I_B + I_C) + I_{CO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CO} \text{ or } I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CO}$$

Early Effect :

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

if $I_E = 0$, $I_{pC} = 0$ then $I_C = I_{CO}$ $\Delta I_C = I_C$, $\Delta I_E = I_E$

$I_E \neq 0$, $I_C = -I_{pC} + I_{CO}$, $\Delta I_E = I_E$

$$I_E = (1+\beta) I_B + (1+\beta) I_{CO}$$

$$\text{But } \beta = \frac{\alpha}{1-\alpha} \text{ then } I_E = \left(1 + \frac{\alpha}{1-\alpha}\right) I_B + \left(1 + \frac{\alpha}{1-\alpha}\right) I_{CO}$$

$$I_E = \left(\frac{1}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CO}$$

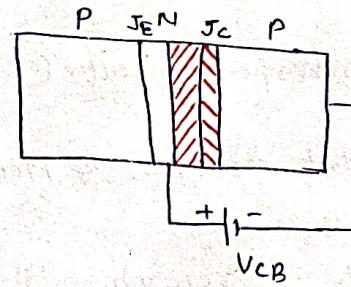
$$\alpha = \beta * \gamma$$

$$I_E + I_C + I_B = 0$$

When Base is common, the $\alpha = \frac{I_{pC}}{I_E} = \frac{I_{pC}}{I_E} \times \frac{I_{pE}}{I_{pE}}$

$$\alpha = \frac{I_{pC}}{I_{pE}} \times \frac{I_{pE}}{I_E} = \beta * \gamma$$

where α & β are current gains for common Base & Emitter



(*) When BJT is in active region mode, collector - junction (J_C) operated in Reverse bias by application of voltage V_{CB}.

(*) When V_{CB} is increased then width of depletion region on J_C junction is also increased but depletion region is more penetrates into Base because it is lightly doped.

(*) Due to this, effective width of Base region is also decreased, known as early effect.

It have main three consequences :-

- ① α Increases: If $V_{CB} \uparrow \rightarrow$ Effective Base width $\downarrow \rightarrow$ No. of holes & e^- recombination in base $\downarrow \rightarrow$ Carrier Transportation becomes more efficient

NOTE: α \uparrow by small amount but very considerably,

$$\uparrow \alpha \leftarrow \uparrow \beta^* \leftarrow$$

Current through Emitter Junction \uparrow So :

$I_E \approx I_{PE}$ which is hole diffusion current \propto Concentration gradient

$$\therefore I_{PE} \propto \frac{dP}{dx} \rightarrow \text{Effective Base width}$$

If $V_{CB} \uparrow \rightarrow$ effective base width $(\Delta x) \downarrow \rightarrow \frac{dP}{dx} \uparrow \rightarrow I_{PE} \uparrow \rightarrow I_E \uparrow$

(3) Punch-through or Reach-through can take place :

- ④ If V_{CB} becomes sufficiently large, depletion region fully occupies the base this is called punch through or reach through.
- ⑤ When punch through occurs effective base width becomes zero & collector gets electrically shorted to emitter.
- ⑥ Strong -ve voltage applied at collector to attracts large no. of holes from emitter which results in a heavy current, it can cause damage to the device.

NOTE:- BJT is damaged due to \Rightarrow punch through or breakdown or thermal runaway takes place.

Relationship between α , β , γ

① $\alpha \& \beta$ We know that $I_E = I_C + I_B$ — ①
dividing both sides by I_C in eqn ①

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

But $\alpha = \frac{I_C}{I_E}$, $\beta = \frac{I_C}{I_B}$
or $\frac{1}{\alpha} = \frac{I_E}{I_C}$ or $\frac{1}{\beta} = \frac{I_B}{I_C}$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta} = \frac{\beta + 1}{\beta}$$

then $\frac{1}{\alpha} / \frac{1}{\beta} / \frac{1}{\gamma} / \frac{1 - \alpha}{\alpha} = \text{W}$ or $\alpha = \frac{\beta}{1 + \beta}$

or $\frac{1}{\alpha} - 1 = \frac{1}{\beta}$

$$\frac{1 - \alpha}{\alpha} = \frac{1}{\beta} \Rightarrow \beta = \frac{\alpha}{1 - \alpha}$$

② $\beta \& \gamma$

Dividing both sides by I_B in eqn ①

$$\frac{I_E}{I_B} = \frac{I_C}{I_B} + \frac{I_B}{I_B}$$

$$\frac{I_E}{I_B} = 1 + \frac{I_C}{I_B}$$

But $\gamma = \frac{I_E}{I_B} \Rightarrow \gamma = 1 + \beta$

or $\beta = \gamma - 1$

$$\beta = \frac{I_C}{I_B}$$

③ $\gamma \& \alpha$

$$I_E = I_C + I_B$$

$$\text{or } I_B = I_E - I_C$$

But $\gamma = \frac{I_E}{I_B} = \frac{I_E}{I_E - I_C} \Rightarrow = \frac{I_E/I_E}{(I_E - I_C)/I_E}$

$$= \frac{1}{\frac{I_E}{I_E} - \frac{I_C}{I_E}} = \frac{1}{1 - \alpha}$$

$$\gamma = \frac{1}{1 - \alpha}$$

④ α, β , and γ

We know that $\beta = \frac{\alpha}{1 - \alpha}$

or $\frac{\beta}{\alpha} = \frac{1}{1 - \alpha}$

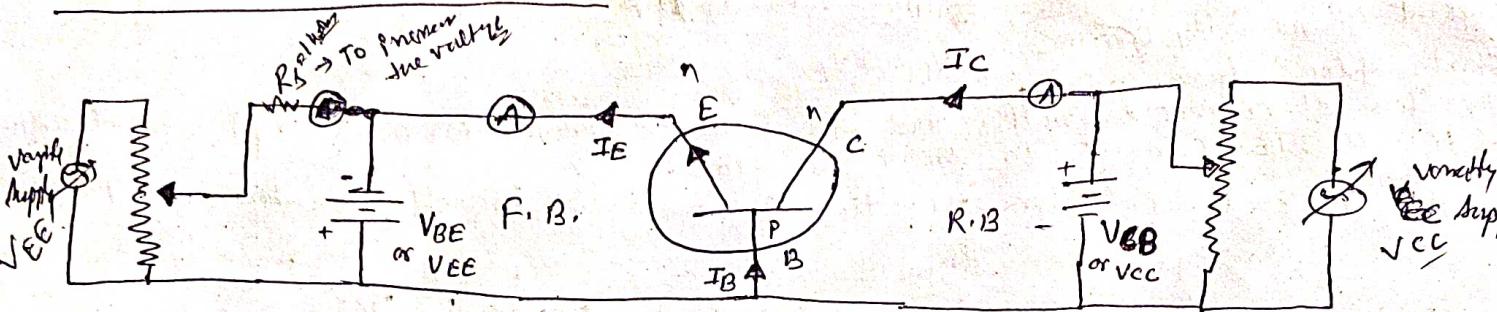
But $\gamma = \frac{1}{1 - \alpha}$

$$\frac{\beta}{\alpha} = \gamma$$

or $\beta = \alpha \cdot \gamma$

But $\alpha = \frac{I_C}{I_E}$
 $\beta = \frac{I_C}{I_B}$
 $\gamma = \frac{I_E}{I_B}$

Common-Base configuration :



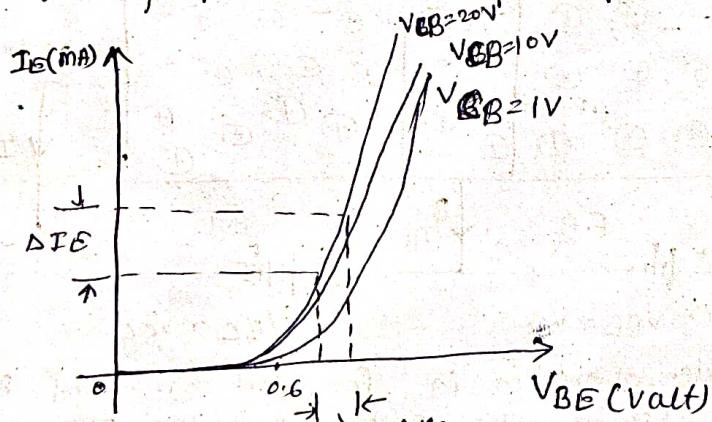
- (*) The Base-Terminal is common between input (Emitter) and output (Collector) terminals of N-P-N transistor.

Input Characteristics : A plot between Input current & Input voltage.

- Step-I : Fixed the value of V_{CB} at any point By changing the DC bias Variable Supply.
- Step-II : Note down the multiple values of input current (I_E) with respect to input voltage (V_{BE}).
- Step-III : Plot the graph between input voltage and input current.

$$I_C = \alpha I_E + I_{CBO}$$

If $I_{CBO} = 0$
 $I_C = I_E$
or $I_E = \frac{I_C}{\alpha}$



Dynamical
input resistance =

$$\frac{\Delta V_{BE}}{\Delta I_E} \quad |_{V_{CB} = \text{Constant}}$$

{ 20 to 100 Ω }

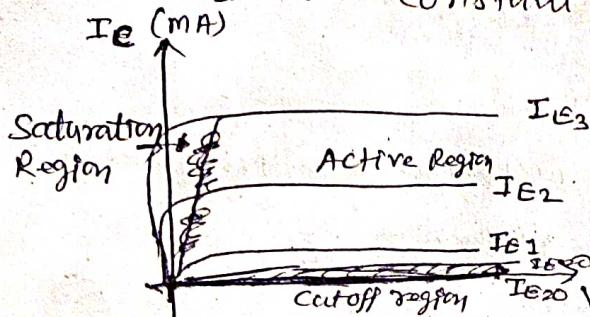
Because
Graph is Non-linear

when we increase the
 V_{CB} the Input current I_E
is sharply increased.

If $K_B \uparrow$ the effective effect is
less power with \uparrow
Then $I_C \uparrow$ with $I_E \uparrow$

Output characteristics for common-base configuration:

It is the variation of collector current (I_C) with collector-base voltage (V_{CB}) at constant value of emitter current (I_E)



$$I_{E3} > I_{E2} > I_{E1} \text{ then } I_{C3} > I_{C2} > I_{C1}$$

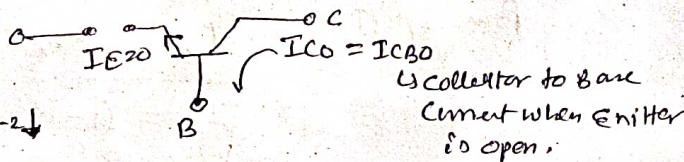
When $I_E \uparrow \rightarrow$ Emitter $\uparrow \rightarrow I_C \uparrow$
When $V_{CB} \uparrow \rightarrow$ Collector $\downarrow \rightarrow$ Transistor \downarrow

Active Region :- Base-Emitter \rightarrow Forward Biased
Collector-Base \rightarrow Reverse Biased

At lower end $\Rightarrow [I_E = 0]$, $I_C = I_{CO}$ (reverse saturation current) but $I_{CO} \downarrow$ at room temp
 \checkmark $I_C = 0$

Means when $I_E \uparrow$ then $I_C \uparrow$

i.e. $I_E \approx I_C \Leftrightarrow \because I_B \text{ is very small}$



Cut-off Region : Between Base to Emitter & Collector to Base \Rightarrow Both are R.B.

i.e. $I_C = 0$ Transistor works as OFF switch
when $I_E = 0$ due to leakage current

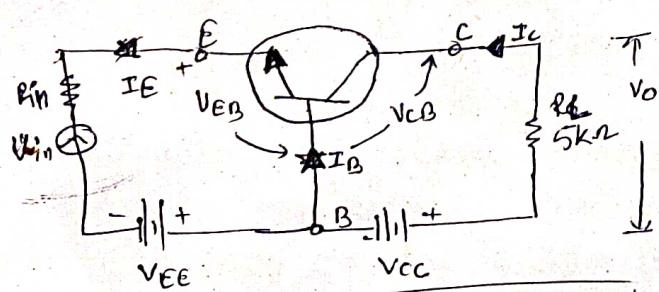
Saturation Region :- Base to Emitter & Collector to Base \Rightarrow Both are Forward Biased
i.e. the Region in the left of $V_{CB} = V_{CE(20)}$.

i.e. when $V_{CB} < 0 \Rightarrow$ then $I_C \uparrow$

when $V_{CB} \geq 0 \Rightarrow$ then $I_C \downarrow$ or (Sharply)

$$\text{Output resistance} = \frac{\Delta V_{CB}}{\Delta I_C} \quad |_{I_E = \text{constant}}$$

Transistor as Amplifying Action



$$\begin{aligned} \text{Input Power} &= 0.5 \times 10^{-3} \times 20 \times 10^{-3} = 1 \times 10^{-6} \text{ watt} \\ \text{O/P Power} &= 0.5 \times 10^{-3} \times 2.5 = 1.25 \times 10^{-3} \text{ watt} \\ [\text{O/P Power}] &> [\text{Input Power}] \end{aligned}$$

For Q.P. $\left\{ \begin{array}{l} \text{input voltage} = 20 \text{ mV} \\ \text{input resist} = 40 \text{ k}\Omega \end{array} \right. \quad \left\{ 20 \text{ mV} \text{ to } 10 \text{ V} \right\}$

$$I_E = \frac{20 \times 10^{-3}}{40} = 0.5 \text{ mA}$$

For Q.P. $V_o = I_C \times R_L$

But $I_E = I_C + I_B$ But $I_B = 0$ \uparrow

$$I_E = I_C = 0.5 \text{ mA} \quad \text{for Active Region & Amplification}$$

$$V_o = 5 \times 10^3 \times 0.5 \times 10^3 = 2.5 \text{ V}$$

$$(Q.P.) = \frac{V_o}{V_{in}} = \frac{2.5}{20 \times 10^{-3}} = 125 \quad \text{i.e. It transfer the signal from low resistance high resistance.}$$

Common Emitter configuration: ④ Emitter Terminal is common between input and output terminals of BJT.

④ Input terminals \Rightarrow Base-Emitter \Rightarrow Forward Biased] for Active mode
 Output terminals \Rightarrow Collector-Emitter \Rightarrow Reverse Biased

⑤ According to KCL eqn.

$$I_E = I_B + I_C \quad \text{--- (1)}$$

$$\text{But } I_C = \alpha I_E + I_{CBO} \quad \text{--- (2)}$$

or Common-Emitter $I_B \rightarrow$ Input current
 $I_C \rightarrow$ Output current

To $I_C = f(I_B)$ means put the value of I_E in eqn (2)

$$I_C = \alpha(I_B + I_C) + I_{CBO} = \alpha I_B + \alpha I_C + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO} \quad \text{--- (4)}$$

$$\boxed{I_C = \beta I_B + (1+\beta) I_{CBO}} \quad \text{where } \beta = \frac{\alpha}{1-\alpha} \quad \text{or } \beta + \beta\alpha = \alpha$$

Assume if $\frac{\alpha}{1-\alpha} = \beta$, $\boxed{\frac{I_{CBO}}{1-\alpha} = I_{CEO} \quad \text{when } I_B=0}$

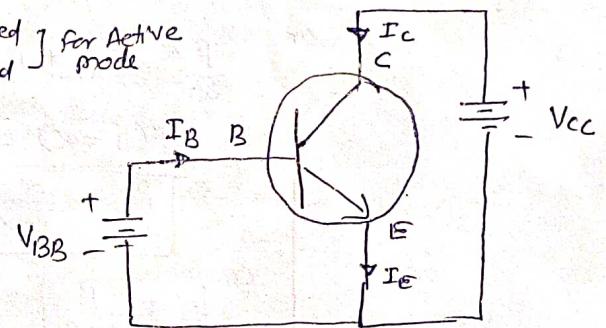
$$\boxed{I_C = \beta I_B + I_{CEO}}$$

Current from Collector-Emitter
 when base is open

$$1+\beta = \frac{\alpha}{1-\alpha} + 1$$

$$= \frac{1+\alpha}{1-\alpha}$$

$$1+\beta = \frac{1}{1-\alpha}$$



The $I_{CEO} \gg I_{CBO}$ because value of α is 0.98 - then and $I_B = 0$

$$I_{CEO} = \frac{I_{CBO}}{1-0.98} = \frac{I_{CBO}}{0.02} = 50 I_{CBO}$$

the value of β will lie in between 20 to 300.

The value of I_{CEO} (collector to emitter leakage current when bases open) $\ll I_C$

$$I_C = \beta I_B$$

$$\text{or } \beta_{dc} = \beta = \frac{I_C}{I_B}$$

Current amplification factor for CE Configuration

$\beta \rightarrow$ Measures the current amplification ability of a transistor.

Relationship between α and β :

The current equation for transistor is $I_E = I_B + I_C$ for small change

$$\Delta I_E = \Delta I_B + \Delta I_C$$

or

$$\frac{\Delta I_E}{\Delta I_C} = \frac{\Delta I_B}{\Delta I_C} + 1$$

But

$$\alpha = \frac{\Delta I_E}{\Delta I_E} = \frac{I_E}{I_C} \quad \text{and} \quad \beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{V}_{CB} = \text{constant} \quad \text{V}_{CE} = \text{constant}$$

then

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 = \frac{1+\beta}{\beta}$$

or

$$\cancel{\frac{\Delta I_E}{\Delta I_C}} = (1+\beta)\alpha = \alpha + \alpha\beta \Rightarrow \cancel{\alpha} \quad \text{or} \quad \beta = \alpha(1+\beta)$$

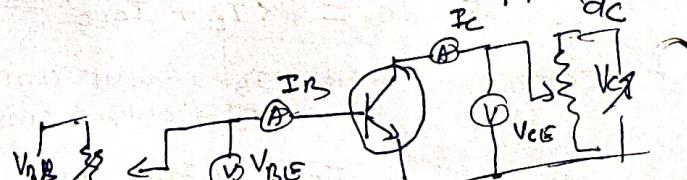
$$\beta(1-\alpha) = \alpha$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

for DC current gain = $\frac{\alpha_{dc}}{1-\alpha_{dc}}$

or

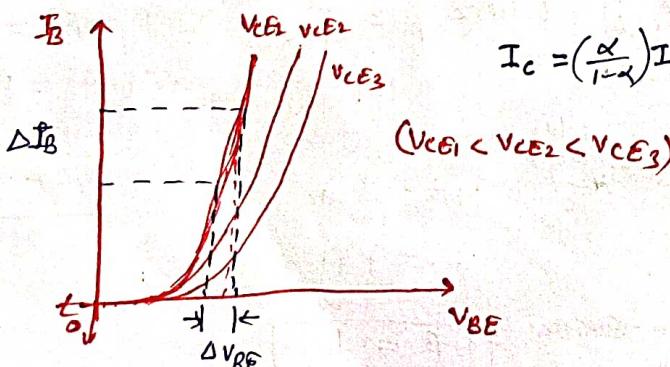
$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$



Input & output characteristics of common Emitter Configuration

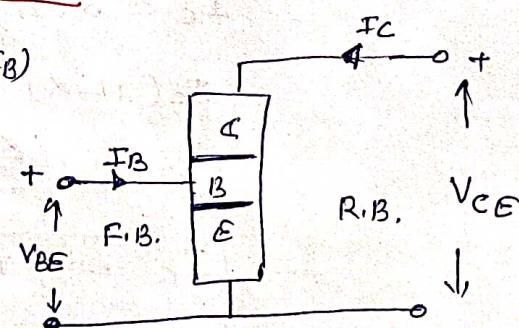
Input characteristics \Rightarrow It is a graph between Input current (I_B) and input voltage (V_{BE}) with a constant output voltage (V_{CE}).

$I_B \propto$ no. of recombination provide the base region.



$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \frac{I_{CBO}}{(1-\alpha)}$$

$(V_{CE1} < V_{CE2} < V_{CE3})$



$$\text{Dynamic resistance } (r_o) = \frac{\Delta V_{BE}}{\Delta I_B}$$

When V_{BE} is less than cut-in voltage then carrier injection from emitter to base will be negligible as a result no recombination occurs inside base and I_B remains negligible or zero.

When V_{BE} exceeds cut-in voltage then more carriers are projected from base from emitter and large no. of recombination takes place means I_B starts flowing. i.e. $[I_B \propto V_{BE}]$ ie diode F.B. characteristics.

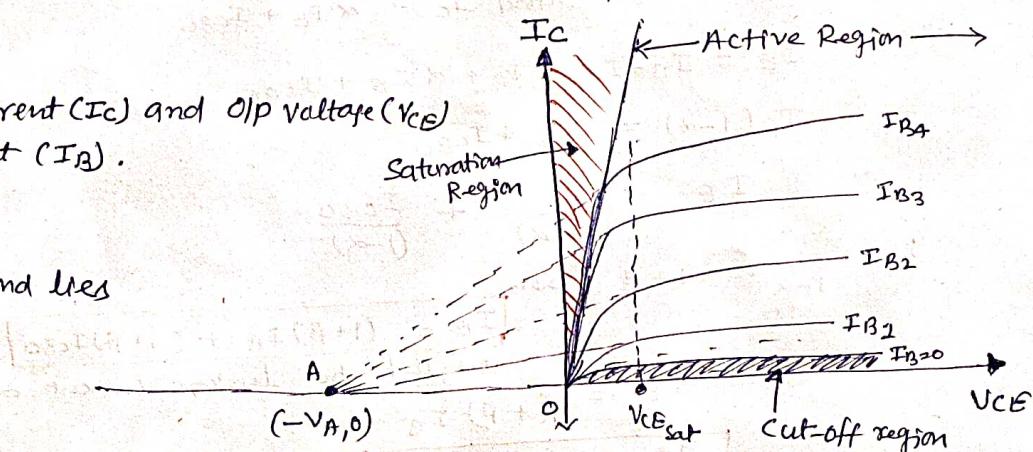
② I_B also depends upon V_{CE} because of early effect.

If $V_{CE} \uparrow \rightarrow V_{CB} \uparrow \rightarrow$ Effective Base width $\downarrow \rightarrow$ No. of Recombination $\downarrow \rightarrow I_B \downarrow$
 $(V_{CB} = V_{CE} - V_{BE})$

Output characteristics :

A graph between O/p Current (I_C) and O/p Voltage (V_{CE}) at constant Base current (I_B).

$V_A \Rightarrow$ Early Voltage and lies
 50V to 100V



Cut-off Region : A Region of characteristics where I_C is approx. zero. It lies on $I_B=0$ curve and to the right of $V_{CE} = V_{CEsat}$.
 i.e. $I_C = \beta I_B + (1+\beta) I_{CO}$
 But $I_B=0$ then $I_C = (1+\beta) I_{CO} = \frac{I_{CO}}{(1-\alpha)} = I_{CEO}$

Saturation Region : Region of characteristics where I_C increases with V_{CE} . It lies above $I_B=0$ curve and to the left of $V_{CE} = V_{CEsat}$.
 $V_{CE} \leq V_{CEsat} \Rightarrow$ BJT is in saturation region.

Active Region : A Region of characteristics where I_C is approx. constant but not exactly constant w.r.t. V_{CE} . It lies above $I_B=0$ curve and right of $V_{CE} = V_{CEsat}$.

In Active region $I_C = \beta I_B + (1+\beta) I_{CO}$ so $I_C \uparrow$ with $\beta \uparrow$ w.r.t. V_{CE} .

If $V_{CE} \uparrow \rightarrow V_{CB} \uparrow \rightarrow$ Effective Base width $\downarrow \rightarrow \alpha \uparrow \rightarrow \beta \uparrow \rightarrow I_C \uparrow$

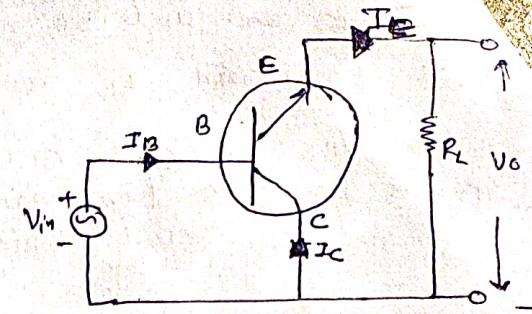
For calculation of I_C if V_{CE} is varied from V_{CE1} to V_{CE2} .

$$I_{C2} = I_{C1} \left[1 + \frac{\Delta V_{CE}}{V_A} \right]$$

$$\text{O/p dynamic resistance. } (r_o) = \frac{\Delta V_{CE}}{\Delta I_C} \quad |_{I_B = \text{constant}}$$

Common Collector Configuration:

- In this configuration collector is common in between input and output terminals of BJT.
- Also known as Emitter follower and used for impedance matching because it have high I_{IP} impedance & low output impedance.



The O/p Emitter current as a function of Base current

$$\text{to } I_E = f(I_B) \quad (1)$$

But $I_E = I_C + I_B$ and $I_C = \alpha I_E + I_{CBO}$
then

$$I_E = I_B + I_C = I_B + \alpha I_E + I_{CBO}$$

$$\text{or } I_E(1-\alpha) = I_B + I_{CBO}$$

$$\text{or } I_E = \frac{I_B}{(1-\alpha)} + \frac{I_{CBO}}{(1-\alpha)}$$

$$\text{But } \frac{1}{1-\alpha} = 1+\beta \text{ then}$$

$$I_E = (1+\beta) I_B + (1+\beta) I_{CBO}$$

$$I_E = (1+\beta) I_B \quad \text{Neglect the leakage current others -}$$

$$\frac{I_E}{I_B} = \gamma = \text{current amplification factor} = (1+\beta)$$

Relation between Current gain γ and α :

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad \text{and} \quad \gamma = \frac{\Delta I_E}{\Delta I_B}, \quad \beta = \frac{\Delta I_C}{\Delta I_B}$$

$$\text{But } I_E = I_C + I_B \quad \text{for small change -}$$

$$\Delta I_E = \Delta I_C + \Delta I_B \Rightarrow \Delta I_B = \Delta I_E - \Delta I_C$$

$$\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} * = \frac{\Delta I_E / \Delta I_E}{\Delta I_E - \Delta I_C / \Delta I_E} = \frac{1}{1 - \frac{\Delta I_C}{\Delta I_E}}$$

$$\gamma = \frac{1}{1-\alpha}$$

$$\text{But } \beta = \frac{\alpha}{1-\alpha} \quad \text{or} \quad \frac{\beta}{\alpha} = \frac{1}{1-\alpha} = \gamma \Rightarrow \beta = \alpha \gamma$$

$$\text{or } \beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{\alpha + 1 - \alpha}{1-\alpha}$$

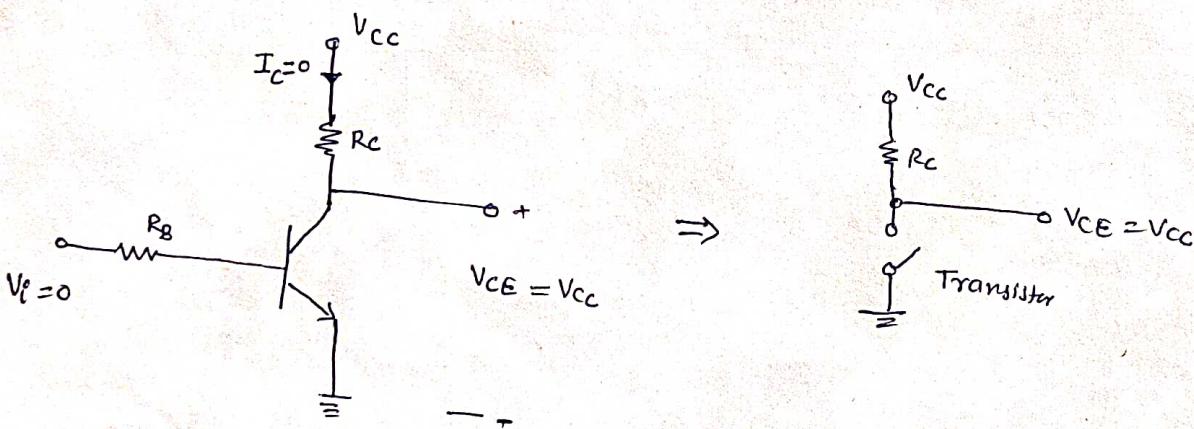
$$\beta + 1 = \frac{1}{1-\alpha}$$

$$\gamma = \beta + 1$$

Comparison Between Three configuration

<u>Parameter</u>	CB	CE	CC
① I _{IP} dynamic resistance	20Ω (Very low)	$1k\Omega$ (Low)	Very High ($750k\Omega$)
② O _{IP} dynamic resistance	$1M\Omega$ (Very High)	$10k\Omega$ (High)	100Ω (50Ω)
③ Current Gain	< 0.98	High (100)	High (100)
④ Leakage current	Very small. $5\mu A \rightarrow Ge$ $1\mu A \rightarrow Si$	Very Large $500\mu A \rightarrow Ge$ $20\mu A \rightarrow Si$	Very large $500\mu A \rightarrow Ge$ Very High $20\mu A \rightarrow Si$
⑤ Voltage Gain	Small (150)	High (500)	Less than Unity

Transistor Switch : (*) Transistor can be used as amplifier and as a switch. For a switching applications, it is biased to operate in the saturation or Cut-off region.



In cut-off region, both the junctions of the transistor are reverse biased and very small reverse current flows through the transistor. The input voltage is zero then $I_B = 0$ and so $I_C = 0$ = transistor is off = open-circuit.

Then according to KCL

$$\Rightarrow V_{cc} = I_C R_C + V_{CE} = V_{CE}$$

When $I_C = 0$ then resistance offered by transistor = ∞ ~~and~~ In this saturation region, transistor acts as a closed switch.

② $B = 100$, $I_E = 10 \text{ mA}$, then find out I_C & I_B .

Ans $\beta = \frac{\alpha}{1-\alpha} \Rightarrow \beta = \alpha(1+\beta)$
 $\Rightarrow \alpha = \frac{\beta}{(1+\beta)} = \frac{100}{101} = 0.99$

Then $\alpha = \frac{I_C}{I_E}$ then $I_C = \alpha I_E = 0.99 \times 10 \times 10^{-3} = 9.8 \text{ mA}$

Ans $I_E = I_C + I_B \Rightarrow I_B = I_E - I_C = 10 \text{ mA} - 9.8 \text{ mA} = 0.2 \text{ mA}$

① In CB configuration, $\alpha = 0.9 = \frac{I_C}{I_E} \Rightarrow I_C = \alpha I_E = 0.9 \times 1 \text{ mA} = 0.9 \text{ mA}$

If $I_E = 1 \text{ mA}$, $I_B = ? \Rightarrow I_E = I_C + I_B \Rightarrow I_B = I_E - I_C = 1 \text{ mA} - 0.9 \text{ mA}$

$$I_B = 0.1 \text{ mA}$$

⑥ In CE Configuration $= \beta = 150 = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{150} = \frac{5 \times 10^{-3}}{150} = \frac{1}{30} \text{ mA}$

Then $I_E = I_C + I_B = 5 \text{ mA} + \frac{1}{30} \text{ mA} = \frac{151}{30} \text{ mA}$

$$I_E = 5.033 \text{ mA}$$

⑦ If $\alpha \rightarrow 0.981$ to 0.987 }
then % change in β . } $\beta = \frac{\alpha}{1-\alpha}$

When $\alpha = 0.981 \Rightarrow \beta = \frac{0.981}{1-0.981} = \frac{0.981}{0.019}$

$$\beta_1 = 51.63$$

When $\alpha = 0.987$

Then $\beta_2 = \frac{0.987}{1-0.987} = \frac{0.987}{0.013} = 75.92$

Change in $\beta_{\text{diff.}} \Rightarrow 75.92 - 51.63 = 24.29$

Then % Change = $\frac{\beta_{\text{diff.}}}{\beta_1} = \frac{24.29}{51.63} \times 100 = 47\%$

⑯ A BJT has base current (I_B) of $200 \mu\text{A}$ and $I_E = 20 \text{ mA}$ then find out I_C and β .

Ans $I_B = 200 \mu\text{A}$] $I_E = I_C + I_B \Rightarrow I_C = I_E - I_B = [(20 \times 10^{-3}) - (200 \times 10^{-6})]$
 $I_E = 20 \text{ mA}$

$$I_C = 20 \times 10^{-3} - 0.2 \times 10^{-3} = 19.8 \text{ mA}$$

Then $\beta = \frac{I_C}{I_B} = \frac{19.8 \times 10^{-3}}{200 \times 10^{-6}} = \frac{19.8 \times 10^3}{200} = 9.9 \times 10^0$

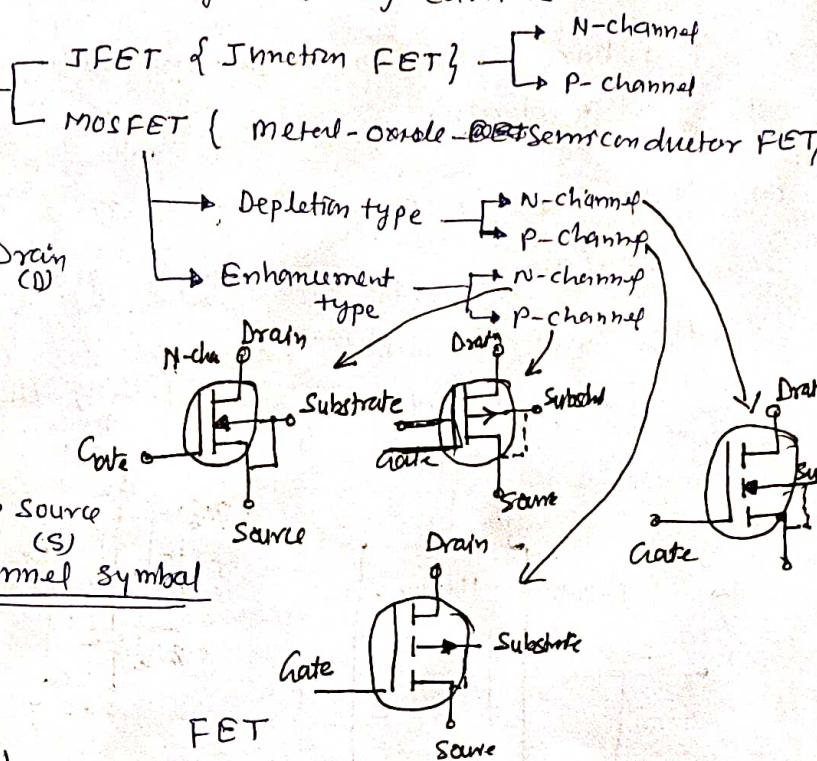
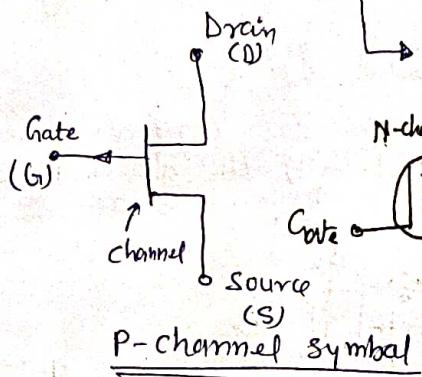
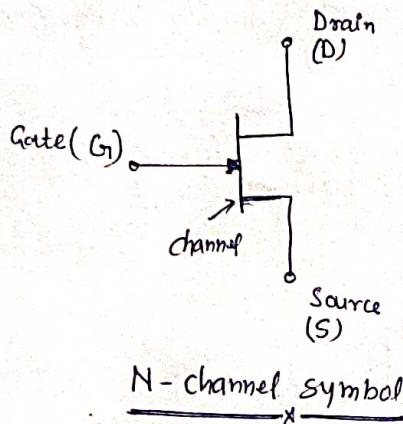
$$\beta = 99$$

⑭ Find the value of I_D at $V_{GS} = -2 \text{ V}$ if $I_{DSS} = 9 \text{ mA}$, $V_p = -4 \text{ V}$.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 = 9 \times 10^3 \left[1 - \frac{(-2)}{(-4)}\right]^2 = 2.25 \text{ mA}$$

FET (Field-effect Transistor)

- (*) FET is a three terminal & Unipolar device means current conduction takes place due to the flow of majority carriers.
- (*) There are two types of FET —
- ② It is voltage controlled device.



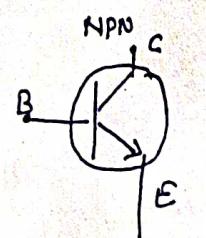
Difference Between BJT and FET

BJT

- ① BJT is a Bipolar Junction Device because its operation depends on the flow of majority as well as minority carriers.
- ② Its input impedance is less because its input section is forward biased.
- ③ It is a current controlled device.
- ④ Thermal stability is less.
- ⑤ Noise is more because of presence of junctions.
- ⑥ Voltage gain is more.
- ⑦ Size is comparatively more and efficiency is less.
- ⑧ Cost is less.
- ⑨ BJT Amplifiers have high gain Bandwidth product.
- ⑩ Due to minority carriers storage effects it has low switching speed and cut-off frequency.

- ① FET is a Unipolar device because its operation depends on the flow of majority carriers only.
- ② Its input impedance is high because its input section is reverse biased.
- ③ It is a voltage controlled device.
- ④ Thermal stability is high.
- ⑤ Noise is less because of absence of voltage junctions.
- ⑥ Gain is less.
- ⑦ Smaller in size, have longer life and better efficiency.
- ⑧ Cost is more.
- ⑨ FET Amplifiers have low gain bandwidth product due to junction capacitive effects.
- ⑩ FET does not suffer from minority carrier storage effects, so it has higher switching speed and cut-off frequency.

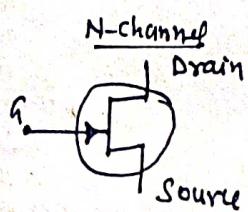
BJT



Base \longleftrightarrow Gate
Collector \longleftrightarrow Drain
Emitter \longleftrightarrow Source
 $I_C \longleftrightarrow I_D$

$$(I_C = \beta I_B) \longleftrightarrow I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

JFET



Prof. Shockley's equations

$I_D \rightarrow$ Drain current =

$I_{DSS} \rightarrow$ maximum drain current , $V_{GS} = 0, I_G = 0$

$V_{GS} \rightarrow$ Gate to source Voltage

$V_P \rightarrow$ Pinch-off voltage = $V_{GS} \neq 0$ or gate is closed

If $V_{GS} = 0$, $I_D = I_{DSS}$ \Rightarrow mean's knob is completely open & no water come out.

If $V_{GS} = V_P$, $I_D = 0$, means knob is completely tight & NO water come out.

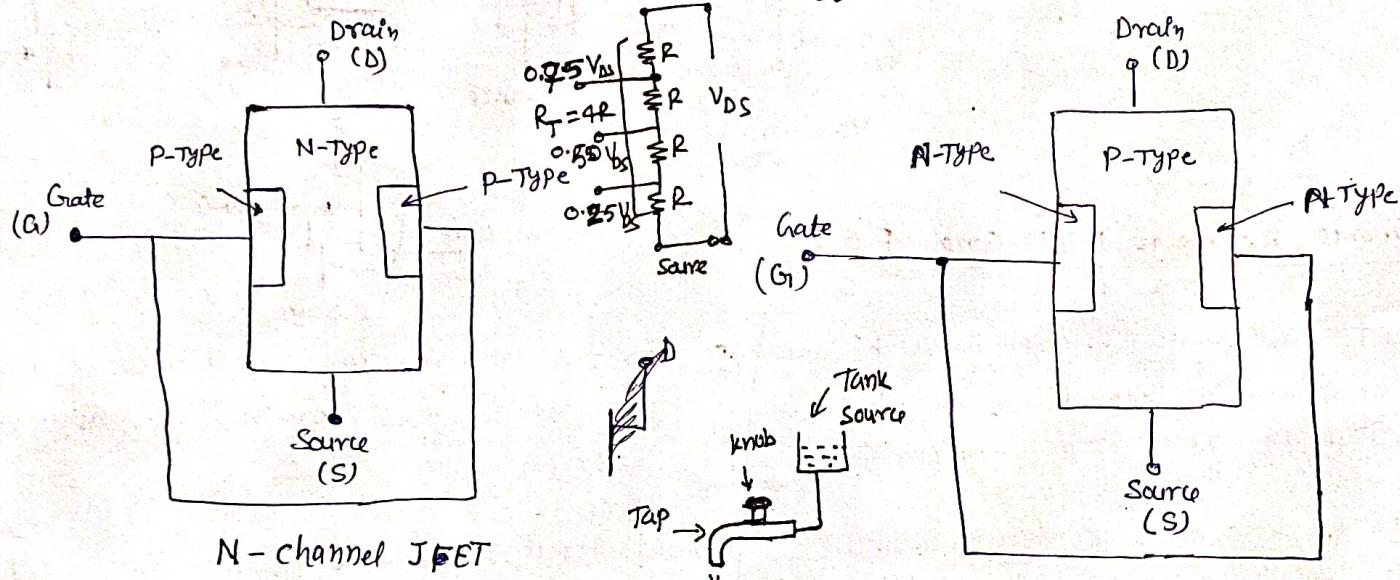
\Rightarrow The output current (I_D) is controlled by Gate to source Voltage
Therefore, known as ~~voltage~~ voltage controlled device.



(Out water from Tap is Controlled)
by knob or gate current

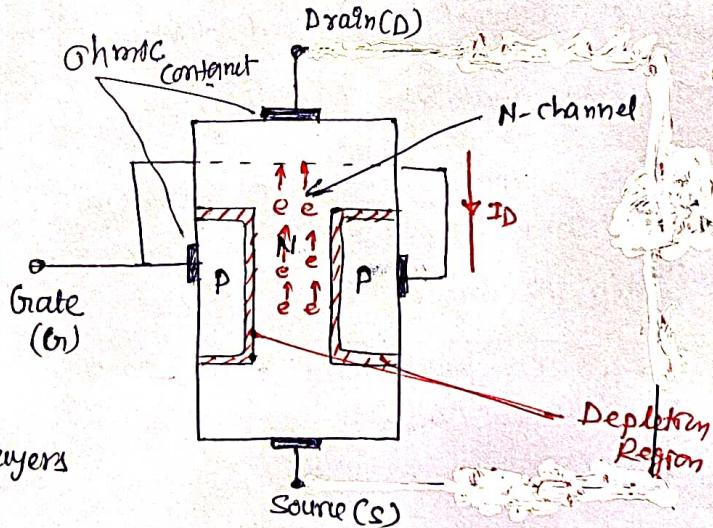
JFET { Junction FET } : There are two types of (N-channel & P-channel) of JFET.

- (*) In N-channel JFET, N-type semiconductor bar with two P-type heavily doped regions diffused on opposite sides of its middle part.
- (*) This bar acts as a resistor between its two terminals called as source and drain.
- (*) These heavily doped P-regions are called gates and usually are connected together to form a single gate.
- (*) The gate terminal is used to control the current flow from source to drain by controlling the drain to source voltage (V_{GS})



Working of N-channel JFET :

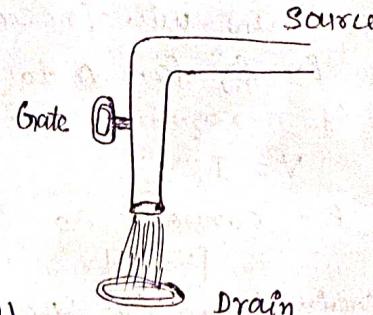
- (*) Major role of ~~is~~ is N-type material in FET is forms the channel between embedded layers of P-type material.
- (*) The top of the N-type channel is connected to Drain (D) and bottom is connected to Source (S). The Gate terminal is connected to the two layers of P-type material.
- (*) When NO potential voltage is applied between Drain and Source then JFET has two p-n junction under no-bias conditions. The result is a depletion region at each junction.



Examples

- ④ Source of water \Rightarrow Applied voltage from drain pressure to source

which establishes a flow of water (electron) from the source.



- ④ The 'barbe' through an applied signal (potential)

Controls the flow of water (charge) to the circuit

Case-I When V_{GS} (gate to source voltage) = 0V and $V_{DS} > 0V$

Drain and source are opposite terminals of the n-channel JFET. Due (+ve) (C-ve)

to the +ve charge at drain majority of bar (electrons) are attracted towards drain and current flow is always opposite to the flow of charge carriers, so I_D (drain current) is starts to flow in opposite direction

- ④ When V_{DS} is increased, +ve charge at drain terminal is also increased and thus I_D increased. i.e

$$I_D \propto I_{DS} \left(1 - \frac{V_{DS}}{V_p} \right)^2$$

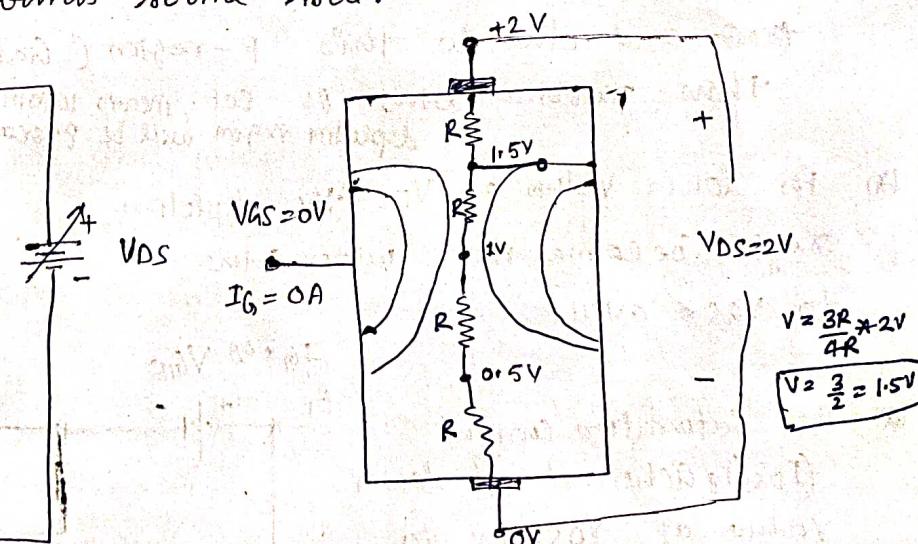
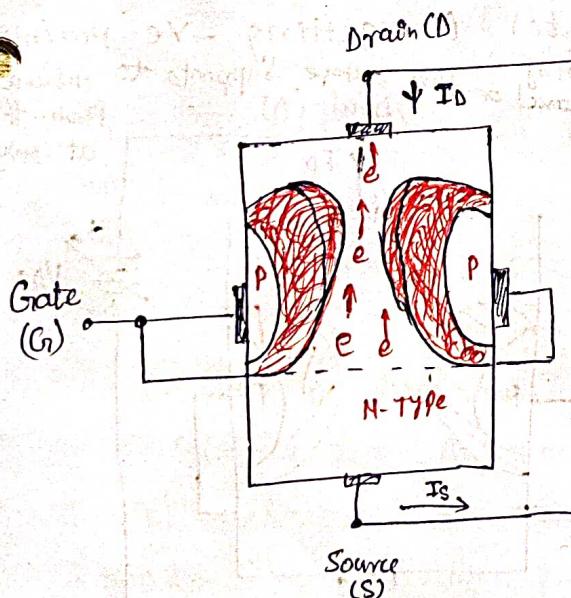
But V_{DS} , I_D increased, $I_D \propto I_{DS}$

$$I_D \propto V_{DS} \text{ when } V_{GS} = 0V \text{ and } I_D = I_S$$

$$I_G = 0A$$

- ④ Since bar is N-type thus +ve charge at drain terminal more reverse biased the bar at drain side. The gate terminal is ~~p-type~~ p-type and bar is N-type, then due to recombination the depletion width increases, according to reversed biased values, i.e decreases from drain to source.

- ④ Due to above reason the depletion width of bar is higher at drain side then reducing towards source side.



When applied reverse voltage is high then
width of depletion region is also high.

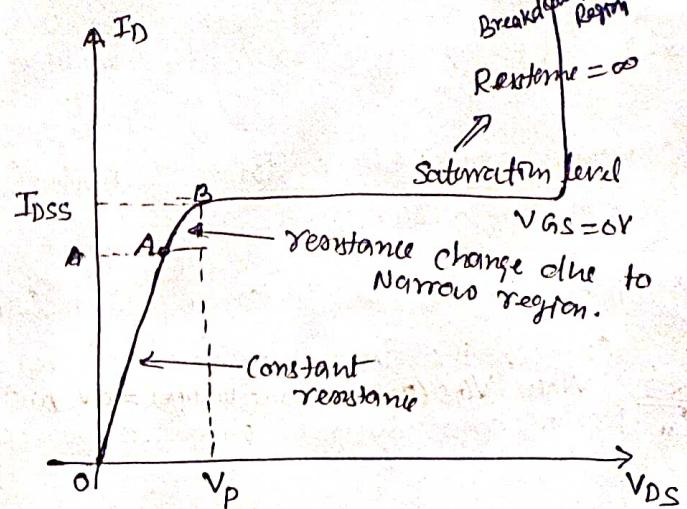
When V_{DS} is increased from 0V to few Volts then current (I_D) will increases linearly as shown in fig from A to B. i.e. resistance of n-region is constant.

$$\text{i.e. } V = IR$$

But $R = \text{constant}$ so

$$V = I$$

As V_{DS} again increased then due to higher charge at drain terminal it become narrow, then n-region resistance increase start to increase, as shown in AB path, then $V \neq I$



The more horizontal curve, the higher the resistance, means the resistance is approaching to ' ∞ ', so current flow or I_D become constant.

The V_{DS} is increased to a level where it appears that the two depletion regions would touch to each other, this condition is known as pinch-off region and voltage level of V_{DS} is known as pinch-off voltage (V_p) i.e. $V_{DS} = V_p$

When $V_{DS} > V_p$ then drain current (I_D) is saturated at point known as I_{DSS} i.e. maximum drain current for a JFET. i.e.

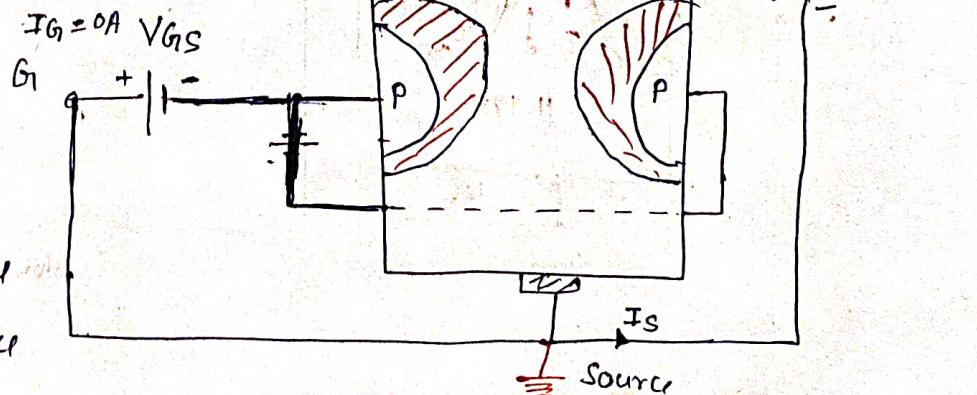
Note $I_D = I_{DSS}$, when $V_{DS} > V_p$ and $V_{GS} = 0V$.

If V_{DS} is continuously increased after pinch-off then ~~JFET~~ JFET is damaged and I_D sharply increased.

Case-II When $V_{GS} < 0$ Volt, $V_{DS} > 0$ Volt

It indicates that V_{GS} is -ve voltage from source gate to drain and due to this P-region (gate) is getting -ve potential thus reverse bias is set, means width of depletion region will be preserved or this voltage supports to Achieve Drain (D)

For lower values of V_{DS} the depletion region become more wider due to $V_{GS} < 0$ Volt.



The saturation current (I_{DSS}) is achieved at lower value of V_{DS} , due to $V_{GS} < 0$ Volt or negative value of gate to source i.e. V_{GS} .

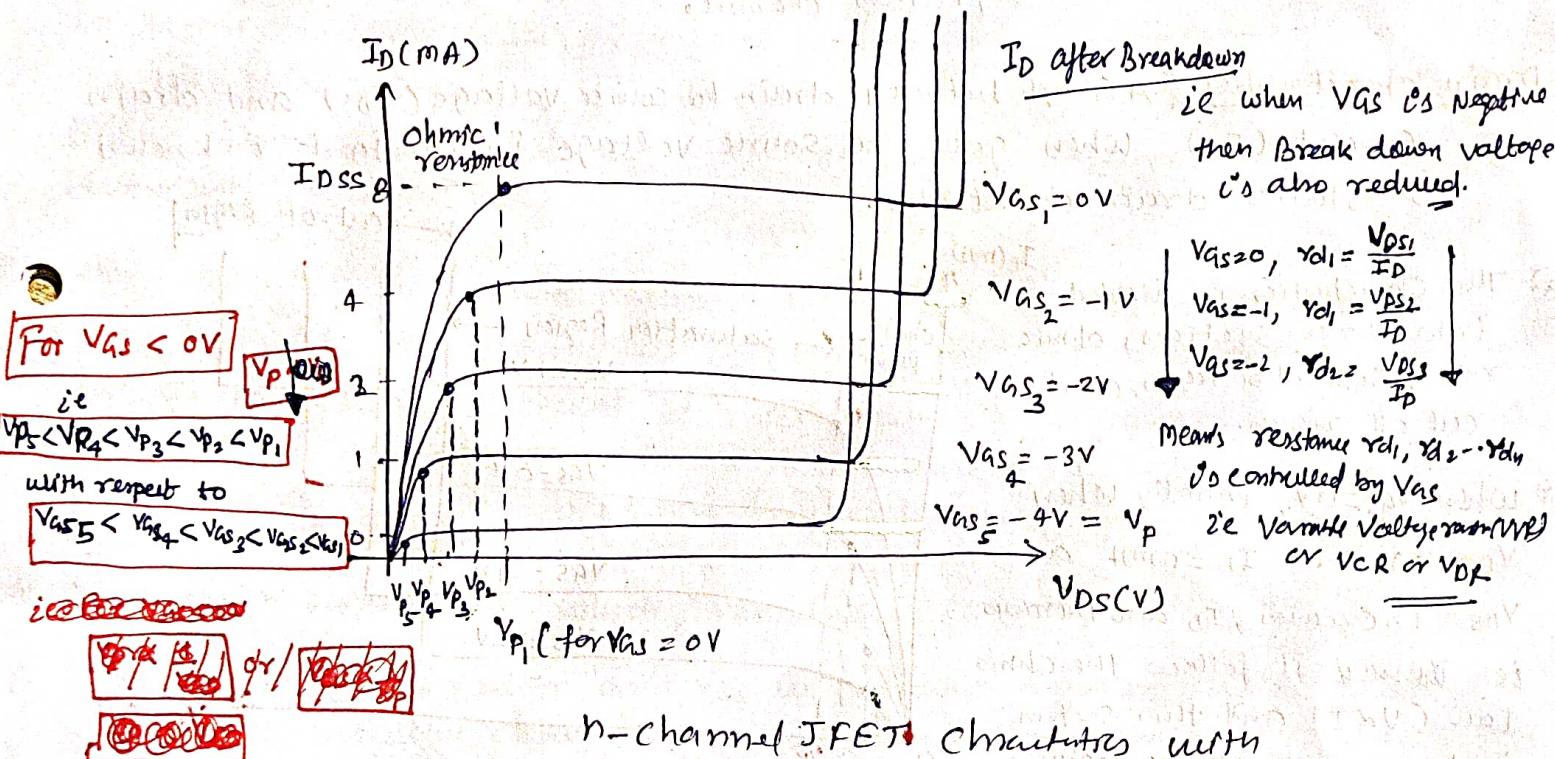
(3)

~~Saturation level of I_D has been reduced.~~

The level of ~~V_{DS}~~ ~~breakdown~~ then $I_D = 0 \text{ mA}$ and devices is called 'turn off'.

(*) The saturation level of I_D current has been reduced.

(*) The level of V_{GS} that results in $I_D = 0 \text{ mA}$ is defined by $V_{GS} = -V_p$, with V_p being a negative voltage for n-channel device and a positive voltage for p-channel JFETs.



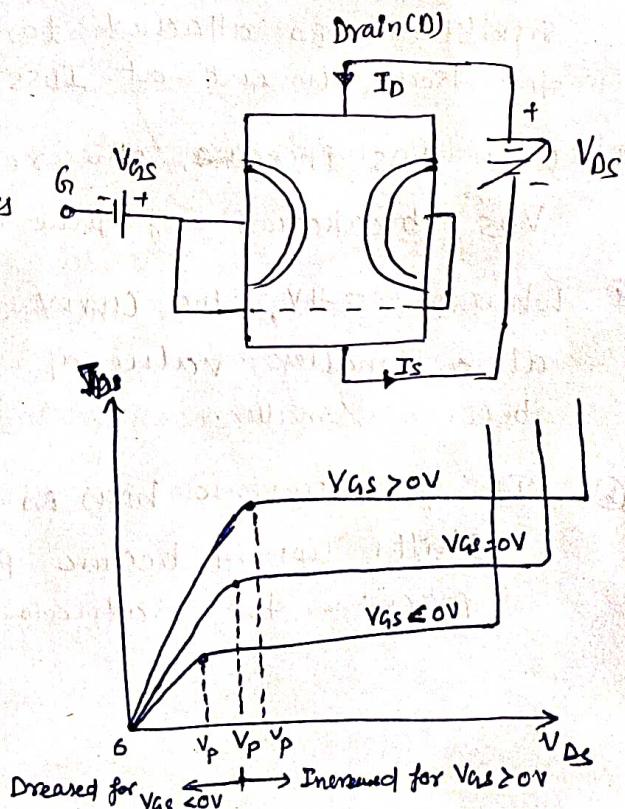
n-channel JFET Characteristics with

$$I_{DSS} = 8 \text{ mA}$$

Case-II: when $V_{GS} > 0 \text{ Volt}$ $V_p = -4 \text{ V}$

(*) It indicates V_{GS} is +ve and when this voltage is applied between gate and source then p-region becomes gets positive supply.

(*) Due to this positive supply the width of depletion region is reduced and V_p is achieved at higher value of V_{DS} and I_D is also increased.

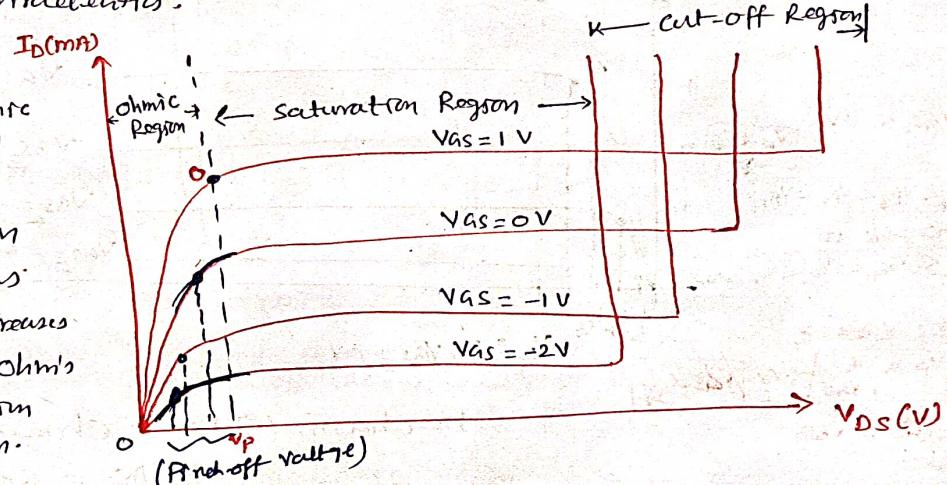


In General, there are four terms; - source, drain, gate and channel.

- ① Source:- A terminal through which the majority carriers enter the bar.
- ② Drain:- A terminal through which the majority carriers leaves the bar.
- ③ Gate:- On the both sides of N-type and P-type, heavily doped P-regions are formed. These regions are called as gates.
- ④ Channel:- Region between source and drain sandwiched b/w 2-gates are called as channel. The majority carriers move from source to drain through this channel.

Drain Characteristics A Graph between drain to source voltage (V_{DS}) and drain current (I_D), when gate to source voltage is constant is known as static drain characteristics.

- ⑤ This characteristics is divided into three sections, ohmic region, saturation region, and cut-off region.
- ⑥ When $V_{GS} = 0V$, initially when $V_{DS} = 0V$ then $I_D = 0mA$ as V_{DS} increases, I_D also increases i.e. It follows the Ohm's Law ($V \propto I$) and this section is known as ohmic region.
- ⑦ Due to the reverse biasing, the width of depletion region increases and as V_{DS} increases pinch-off occurs and current becomes saturated and ~~saturated~~ significant is attached to drain current when $V_{GS} = 0V$ that ~~saturated~~ ^{saturated} the drain current at I_{DSS} (Drain Source current when gate is shorted to source)
- ⑧ When V_{DS} increases, the reverse bias is also increases and thus at high V_{DS} , breakdown of gate junction occurs.
- ⑨ When $V_{GS} = -1V$, the curve shifts downward, because pinch-off occurs at a smaller value of V_{DS} and maximum saturation current is also become smaller.
- ⑩ If gate reverse bias is decreased, means $V_{GS} = 1V$, the curve shifts upward because pinch-off occurs at larger value of V_{DS} , and maximum the saturation current (I_{DSat}) is also increased.



JFET Parameters

- ① Dynamic drain resistance: It is the ratio of small change in the drain voltage to corresponding small change in the drain current at a constant gate voltage.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad | \quad V_{GS} = \text{constant}$$

$$r_d = 400 \text{ k}\Omega$$

Reciprocal of r_d is called drain conductance (g_d) and its unit is ohm^{-1} .

$$g_d = \frac{\Delta I_D}{\Delta V_{DS}} \quad | \quad V_{GS} = \text{constant}$$

- ② Mutual conductance or transconductance

It is the ratio of small change in the drain current to the corresponding small change in the gate voltage at constant drain voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad | \quad V_{DS} = \text{constant}$$

Dimension

It is measured in Siemens (S). Its range from $150 \mu\text{S}$ to $250 \mu\text{S}$.

- ③ Current Amplification factor: It is the ratio of small change in the drain voltage to the corresponding small change in the gate voltage at constant drain current.

$$\mu = - \frac{\Delta V_{DS}}{\Delta V_{GS}} \quad | \quad I_D = \text{constant}$$

NOTE:- Negative sign shows that when $V_{GS} \uparrow$ then $V_{DS} \downarrow$ for maintaining I_D constant.

$$\mu = 100$$

- ④ I_{DSS} : It signifies the drain saturation curve when $V_{GS} = 0\text{V}$ and its value is 7.4 mA .

- ⑤ Power dissipation (P_D): It is the product of I_D and V_{DS} .

$$P_D = I_D * V_{DS}$$

Relationship between u , γ_d and g_m :

I_D depends upon V_{DS} and V_{GS} , means

$$I_D = f(V_{DS}, V_{GS})$$

If Drain Voltage (V_{DS}) changes a small amount from V_{DS} to $(V_{DS} + \Delta V_{DS})$ and Gate Voltage (V_{GS}) is changed by small amount from V_{GS} to $(V_{GS} + \Delta V_{GS})$ then correspondingly small change in drain current (I_D)

i.e.

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}} \cdot \Delta V_{GS}$$

$$\begin{aligned} u &= f(x, y) \\ du &= \frac{\partial f}{\partial x} \cdot dx + \frac{\partial f}{\partial y} \cdot dy \end{aligned}$$

Dividing both sides of eqn by ΔV_{GS} then

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} \cdot \left(\frac{\Delta V_{DS}}{\Delta V_{GS}} \right) + \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}} \cdot \frac{\Delta V_{GS}}{\Delta V_{GS}}$$

Total derivative

But I_D is constant, i.e. $\frac{\Delta I_D}{\Delta V_{GS}} = 0$, then

$$\left(\frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} \cdot \left(\frac{\Delta V_{DS}}{\Delta V_{GS}} \right) + \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}} = 0$$

$$\text{or } \left(\frac{\Delta I_D}{\Delta V_{DS}} \right)_{V_{GS}} \cdot \left(\frac{\Delta V_{DS}}{\Delta V_{GS}} \right) + \left(\frac{\Delta I_D}{\Delta V_{GS}} \right)_{V_{DS}} = 0$$

But

$$\left(\frac{\Delta I_D}{\Delta V_{GS}} \right)_{V_{DS}} = g_m, \quad \left(\frac{\Delta V_{DS}}{\Delta I_D} \right)_{V_{GS}} = \gamma_d, \quad -\left(\frac{\Delta V_{DS}}{\Delta V_{GS}} \right) = u \quad \text{then}$$

$$\left(\frac{1}{\gamma_d} \right) \cdot (-u) + g_m = 0$$

$$-\frac{u}{\gamma_d} + g_m = 0 \Rightarrow u = \gamma_d * g_m$$

Transfer characteristics of JFET: For this V_{DS} is maintained constant at a suitable value greater than the pinch-off voltage (V_p). The V_{GS} is decreased from zero till I_D is reduced to zero.

② The relationship b/w I_D and V_{GS} is defined by Shockley's equation-

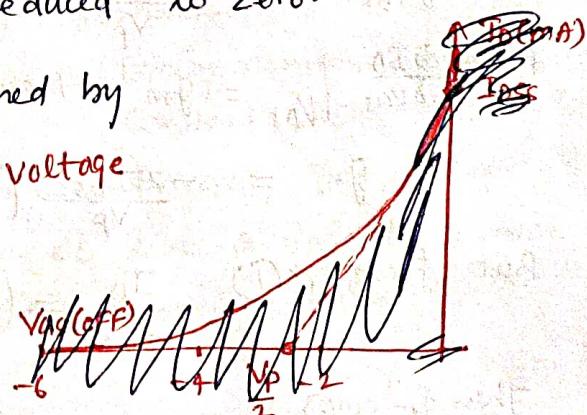
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2 \quad \text{--- (1)}$$

Drain Current or
Drain to Source Current (I_{DS})

Saturation
Drain Current
when $V_{GS} = 0$

Pinch-off
Voltage

Gate to Source Voltage



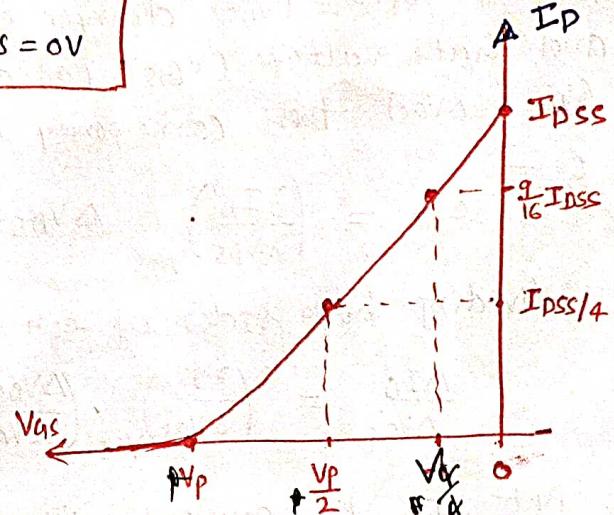
Since $I_{DSS} = \text{constant}$, and $V_p = \text{constant}$ then I_D gives the variation with V_{GS} .

Case-I When $V_{GS} = 0V$ then $I_D = I_{DSS} \left(1 - \frac{0}{V_p}\right)^2$
or $I_D = I_{DSS} \boxed{| V_{GS} = 0V}$

Case-II When $V_{GS} = V_p$ then

$$I_D = I_{DSS} \left(1 - \frac{V_p}{V_p}\right)^2$$

or
i.e. $I_D = I_{DSS} (1-1)^2 = 0$
 $I_D = 0A \boxed{| V_{GS} = V_p}$



Case-III When $V_{GS} = \frac{V_p}{4}$, ~~when $V_{GS} = -1V$, $\frac{V_p}{4}$ is not valid~~

$$I_D = I_{DSS} \left(1 - \frac{V_p}{4}\right)^2 = \frac{9}{16} I_{DSS} \boxed{| V_{GS} = -1V \text{ or } \frac{V_p}{4}}$$

Case-IV When $V_{GS} = \frac{V_p}{2}$ then

$$I_D = I_{DSS} \left(1 - \frac{V_p/2}{V_p}\right)^2$$

$$I_D = \frac{I_{DSS}}{4} \boxed{| V_{GS} = \frac{V_p}{2}}$$

Calculate the expression for g_m .

Differentiate the eqn ① with respect to V_{GS} then

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$\frac{\partial I_D}{\partial V_{GS}} = I_{DSS} \left[2 \left(1 - \frac{V_{GS}}{V_p}\right) \cdot \left(0 - \frac{1}{V_p}\right) \right]$$

$$\text{or } \frac{\partial I_D}{\partial V_{GS}} = -\frac{2 I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p}\right)$$

$$\text{But } \frac{\partial I_D}{\partial V_{GS}} \Big|_{V_{GS}=0} = g_m \text{ then}$$

$$g_m = -\frac{2 I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p}\right) \quad \text{--- (2)}$$

$$\text{But from eqn ① } \frac{I_D}{I_{DSS}} = \left(1 - \frac{V_{GS}}{V_p}\right)^2 \text{ or } \left(1 - \frac{V_{GS}}{V_p}\right)^2 = \sqrt{\frac{I_D}{I_{DSS}}}$$

Then from eqn ②

$$g_m = -\frac{2 I_{DSS}}{V_p} \times \sqrt{\frac{I_D}{I_{DSS}}} = -\frac{2 \sqrt{I_{DSS}} \times \sqrt{I_{DSS}} \times \sqrt{I_D}}{V_p \times \sqrt{I_{DSS}}} \quad \text{--- (3)}$$

$$g_m = -\frac{2 \sqrt{I_D \times I_{DSS}}}{V_p}$$

Assume $g_m = g_{m0}$, when $V_{GS} = 0V$ then for eqn ②

$$g_{m0} = -\frac{2I_{DSS}}{V_P} \left(1 - \frac{0}{V_P}\right) = -\frac{2I_{DSS}}{V_P}$$

then

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_P}\right)$$

Application of JFET :

- ① FET is used as buffer in measuring instruments, receivers because it has high input impedance and low OIP impedance.
- ② FETs are used in RF amplifiers in FM tuners and communication equipments for the low noise level.
- ③ Since Input capacitance is low, so used in cascade amplifiers in memory and test equipments.
- ④ Since it is voltage controlled device, so used as voltage variable resistor in operational Amplifier and tone controls.
- ⑤ FETs are used in mixer circuits in FM and TV receivers and communication equipments because inter modulation distortion is low.
- ⑥ Used in oscillator circuits because frequency drift is low.
- ⑦ As Coupling capacitor is small, so used in low frequency amplifiers in hearing aids and inductive transducer.
- ⑧ It is used in digital circuits in Computers, LSD and memory circuits because of its small size.

JFET As Voltage-variable Resistor : FET is operated in constant-current portion of its output characteristics for linear application. The region before pinch-off, where V_{DS} is small and drain to source resistance (r_d) can be controlled by V_{GS} , thus region is used as VVR or VDR.

The variation of r_d with V_{GS} expressed by expression—

$$r_d = \frac{r_o}{1 - k V_{GS}}$$

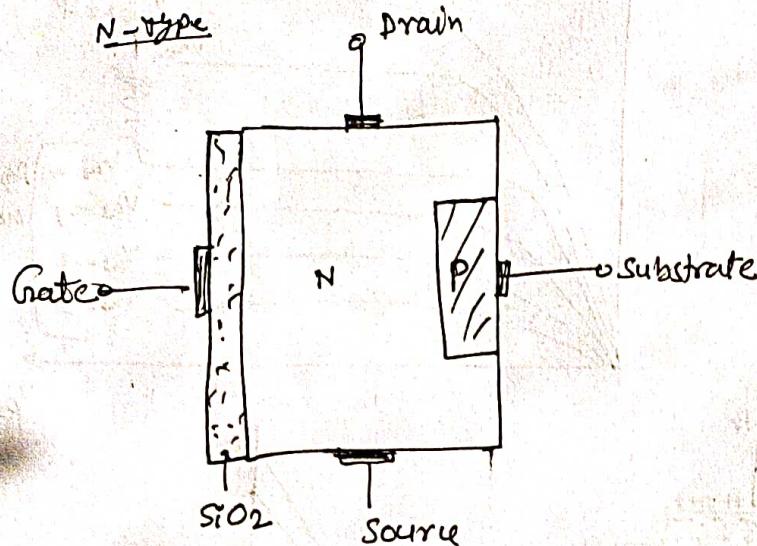
where $r_o \rightarrow$ Drain resistance when $V_{GS}=0V$
 $k \rightarrow$ Constant, depends upon FET type

As r_d varies with respect to V_{GS} ie both are inversely proportional. i.e. when $V_{GS} \uparrow$ then $r_d \downarrow$ and vice-versa. i.e like a Variable passive resistor. and used in automatic gain control Circuits of a multistage amplifier.

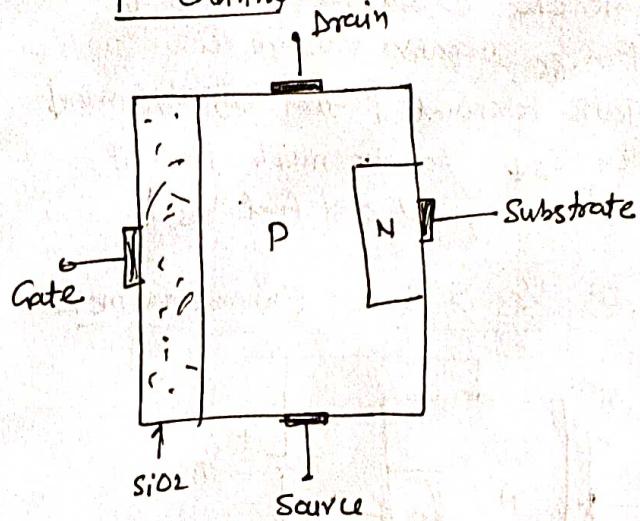
MOSFET

Metal Oxide Semiconductor Field Effect Transistor

N-type



P-Channel



- It consists of single P-type region ~~is called~~ Substrate (SS) and one channel between Source and drain.

- (a) The Gate terminal connected to the channel through SiO_2 layer which is just an insulator, so that its input impedance is very high.

- (b) MOSFET are two types
 - Depletion mosfet — Depletion mode + Enhancement mode
 - Enhancement-mosfet — Enhancement mode only.

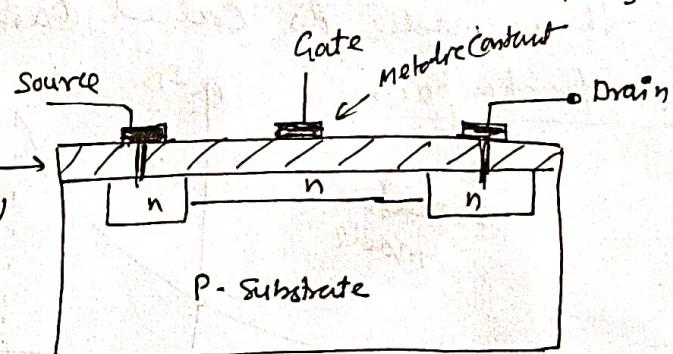
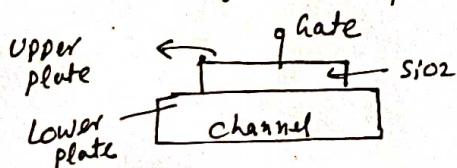
- (c) In depletion mode $V_{GS} = 0$ or < 0 volt but in enhancement mode $V_{GS} > 0$ V

Depletion type N-channel mosfet

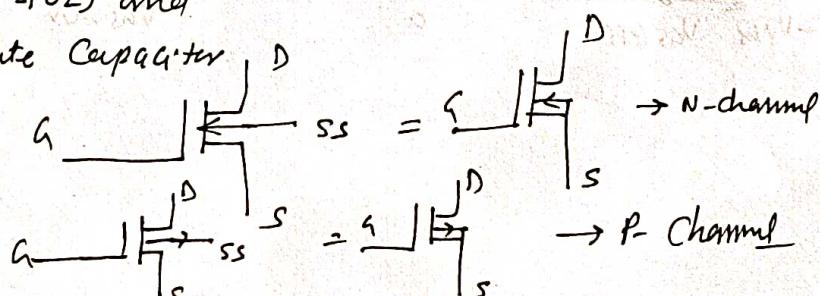
- There is no direct connection between gate and channel, but it is connected through SiO_2 i.e. insulating material so it is also known as Insulating gate FET (IGFET)

- The slab of P-type material is formed from Si base and called substrate.

- The gate (G), insulating layer (SiO_2) and channel forms a parallel plate capacitor.

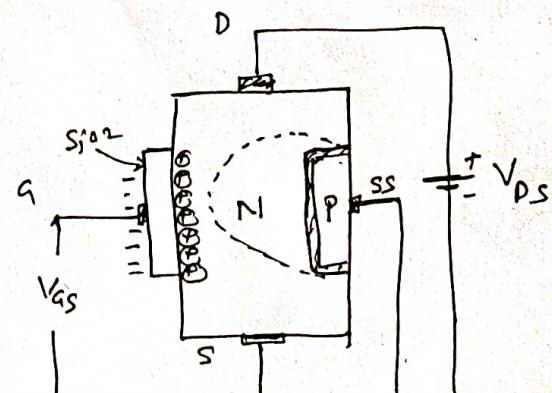
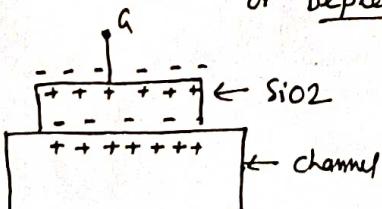


Case-II $V_{GS} > 0$, Work as JFET



Case-II $V_{GS} < 0$ V (i.e. V_{GS} = Negative Voltage)

or Depletion mode, and $V_{DS} > 0$ V
(i.e. Drain = +ve
Gate = -ve)



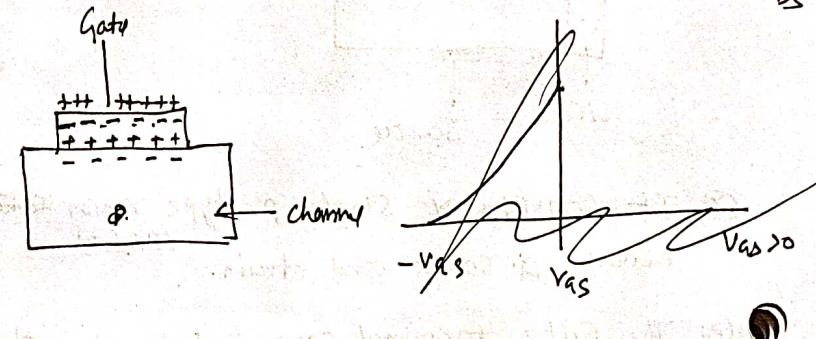
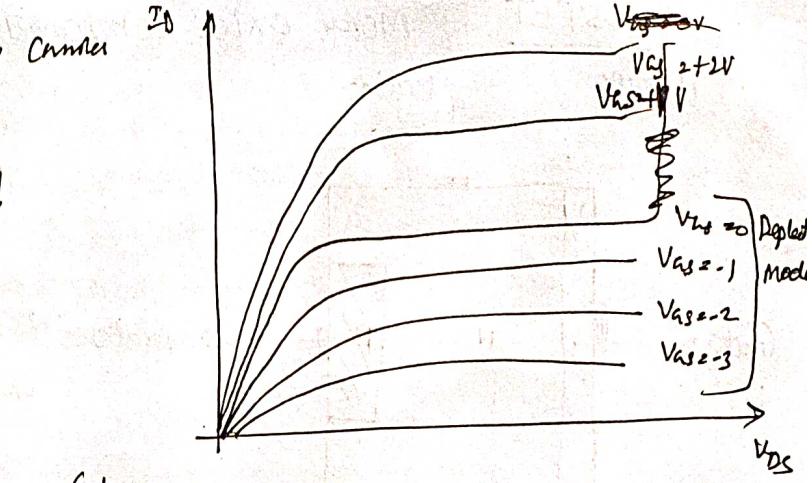
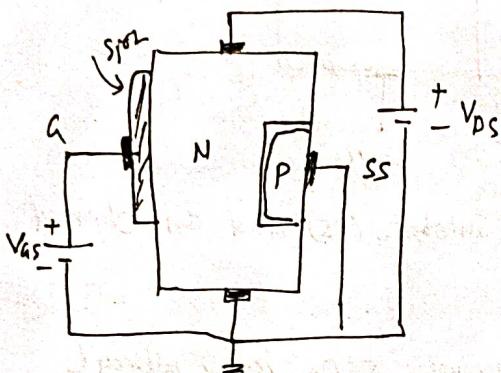
- Due to this +ve charge is generated on N-channel through SiO_2 and electrons on N-region diffused with

- +ve charge and decreased and same time width of depletion region grown and SiO_2 is

means greater decrement in majority carriers
lessen the Conductivity. or $I_D \downarrow$

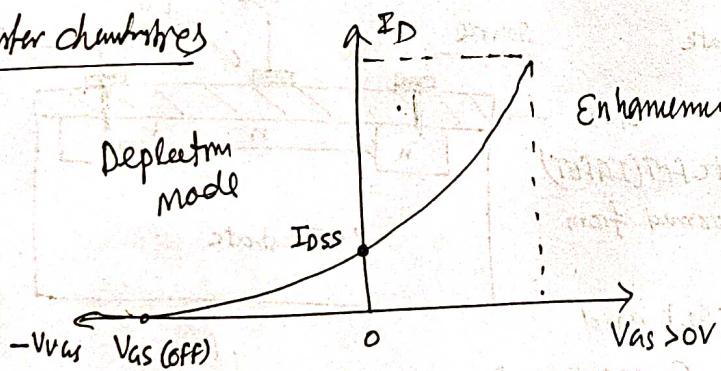
- ② If ~~V_{GS}~~ Negative voltage at
gate terminal \uparrow than majority carriers
Then $I_D \downarrow$, so too much pinch off
Voltage required and final $V_{DS} \uparrow$

Con-II $V_{GS} > 0V$ or Enhancement mode



- ① When positive Voltage V_{GS} is applied at the gate then because of parallel plate capacitor action, $-V_c$ charges are induced in channel.
- ② Due to this no. of majority carriers increases and hence I_D increases.
- ③ In this region $I_D \uparrow$ above I_{DSS} or ~~channel~~ Enhanced above I_{DSS} thus mode is called ~~over~~ enhanced mode.

Transfer characteristics



Enhancement mode.