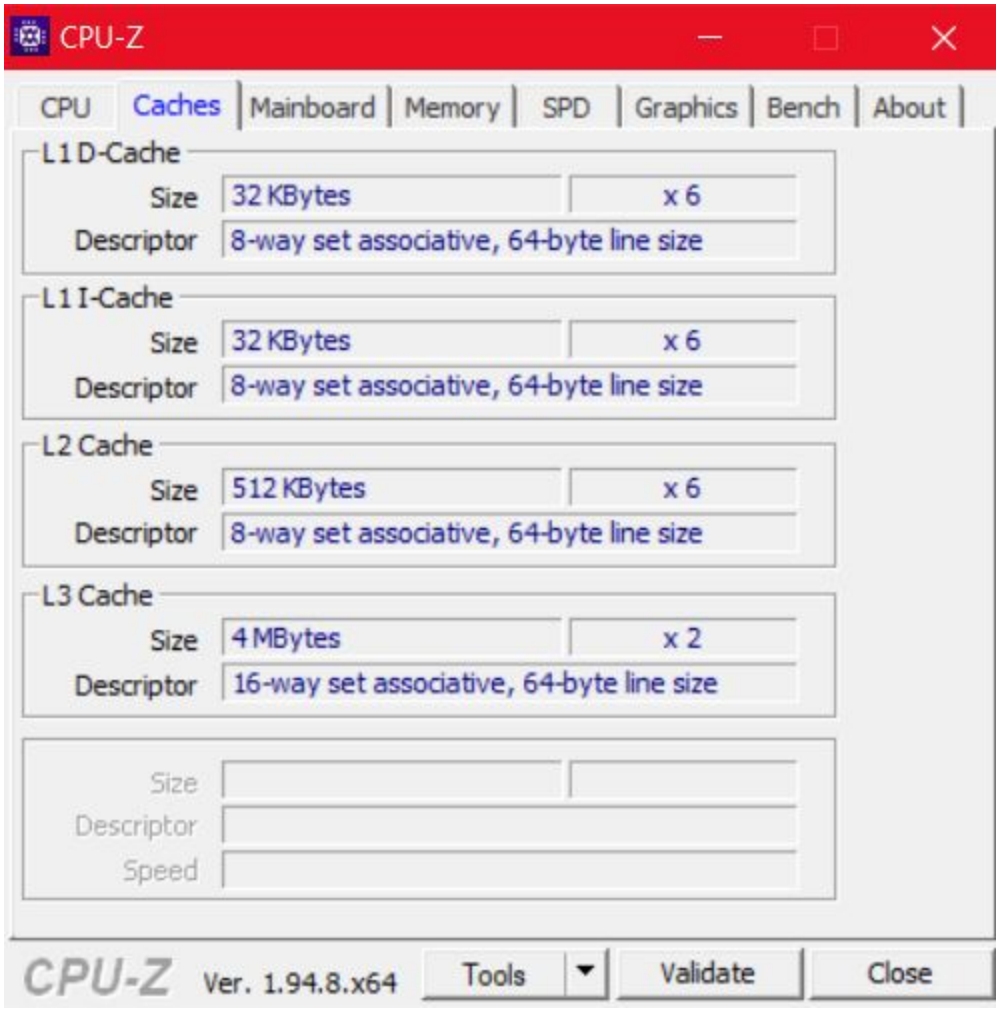
Answer the following questions in a text file named individualAssign1.txt:

1. How many levels of caches does your CPU have (L1, L2, L3, etc.)? Is there a separate L1 cache for data and instructions?
   - My CPU has L1D, L1I, L2, and L3 caches.
2. How big is each level of cache?
   -


3. What is the block size (sometimes it is called line size)?
   - 64 byte line size.
4. Are the caches direct-mapped or set associative? If set associative, how many ways?
   - The caches are set associative, 8 ways.
5. With L1 data cache, how many tag bits, index bits, and offset bits?
   - 32 KB total size = 32 * 8 * 1000 = 256,000 bits
   - # of offset bits = log2(64) = 6 bits
   - # of blocks = 32,000/64 = 500 blocks
   - 500/8 = 62 sets
   - # of index bits = log2(62) = 7 bits
   - # of tag bits = 20 - 7 - 6 = 13 bits