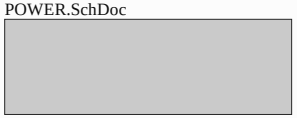
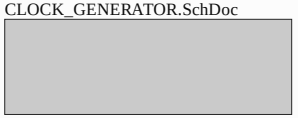
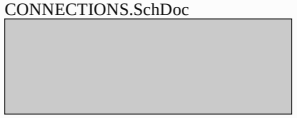
U_POWER
POWER.SchDoc



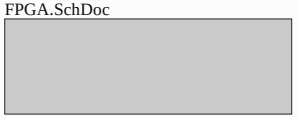
U_CLOCK_GENERATOR
CLOCK_GENERATOR.SchDoc



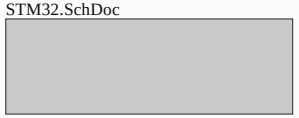
U_CONNECTIONS
CONNECTIONS.SchDoc



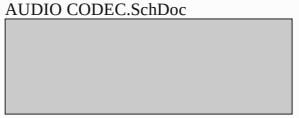
U_FPGA
FPGA.SchDoc



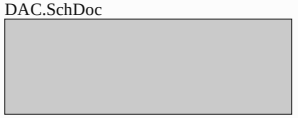
U_STM32
STM32.SchDoc



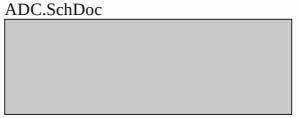
U_AUDIO CODEC
AUDIO CODEC.SchDoc



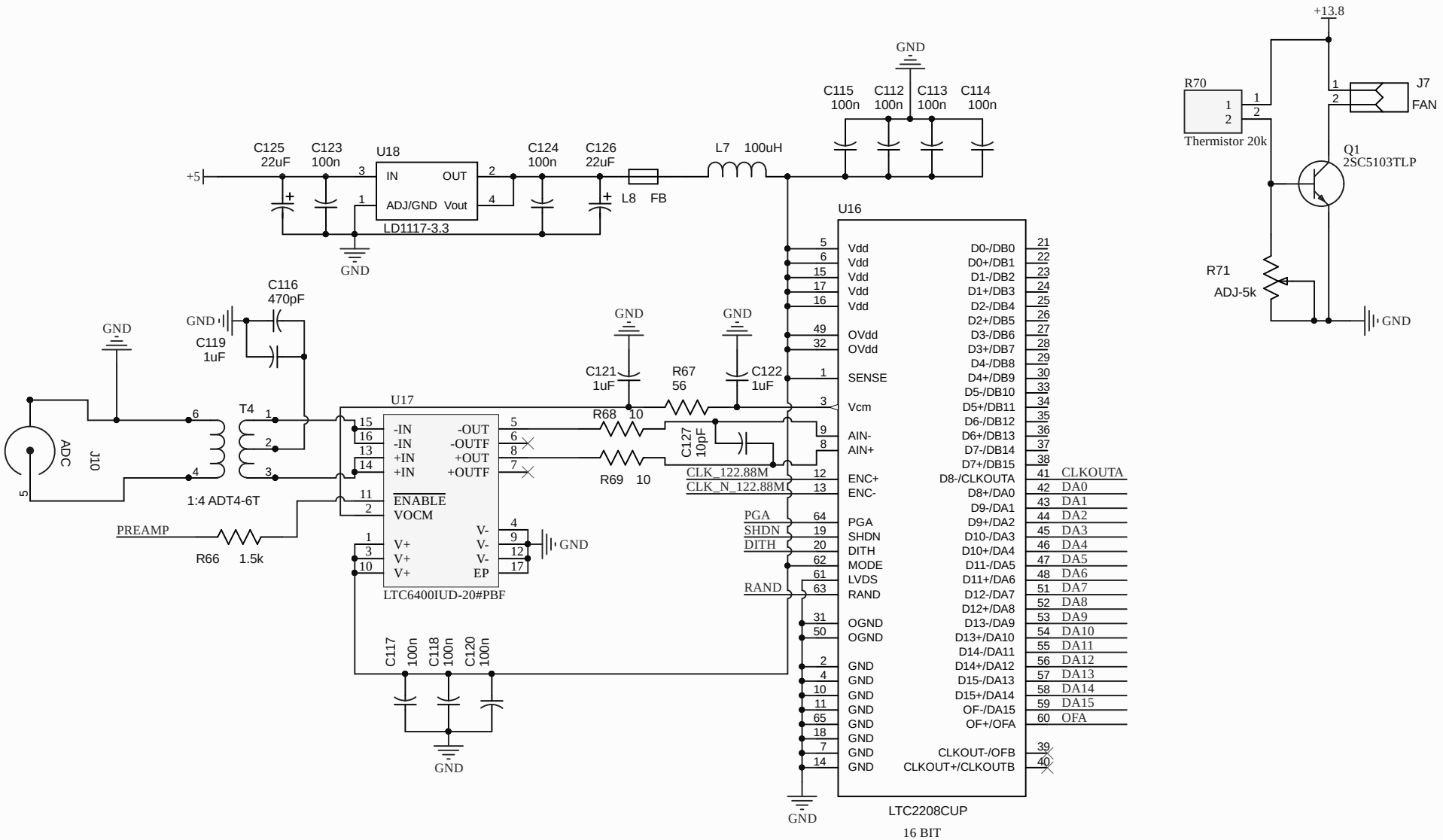
U_DAC
DAC.SchDoc



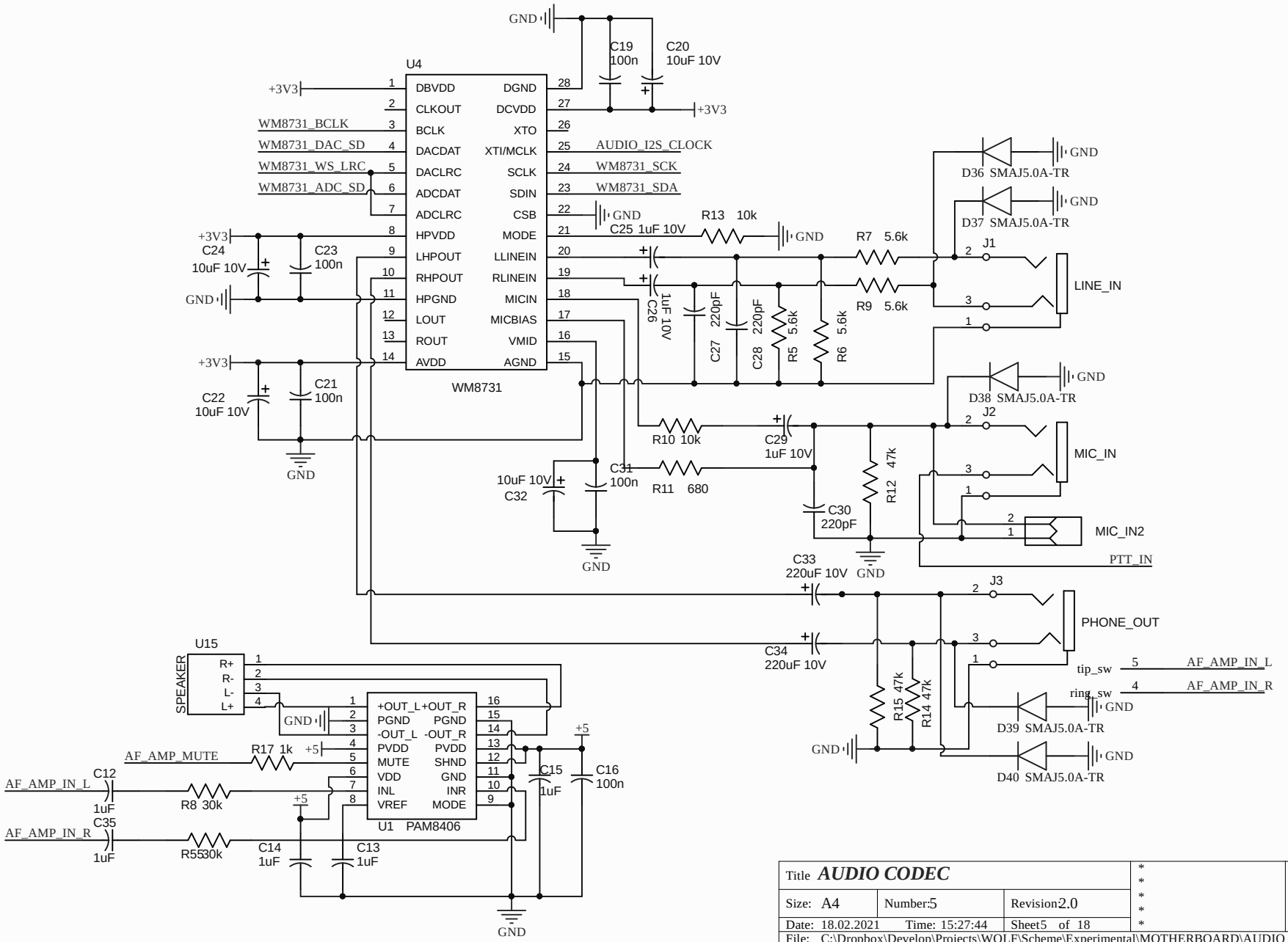
U_ADC
ADC.SchDoc



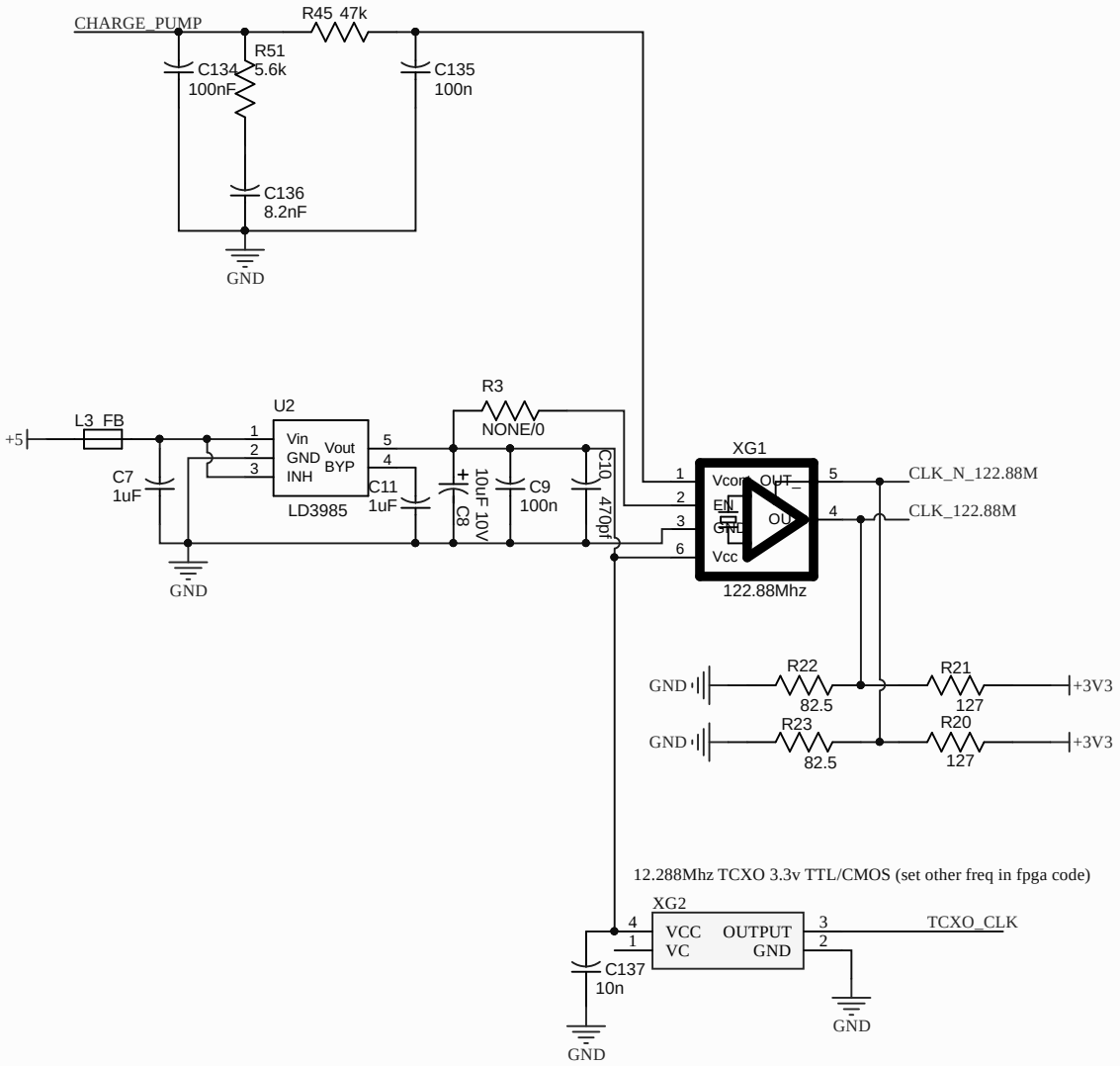
Title ***MOTHERBOARD***			* * * * *
Size: A4	Number:2	Revision:2.0	
Date: 18.02.2021	Time: 15:27:43	Sheet2 of 18	
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\Experimental\MOTHERBOARD\MOTHERBOARD.SCHDOC			



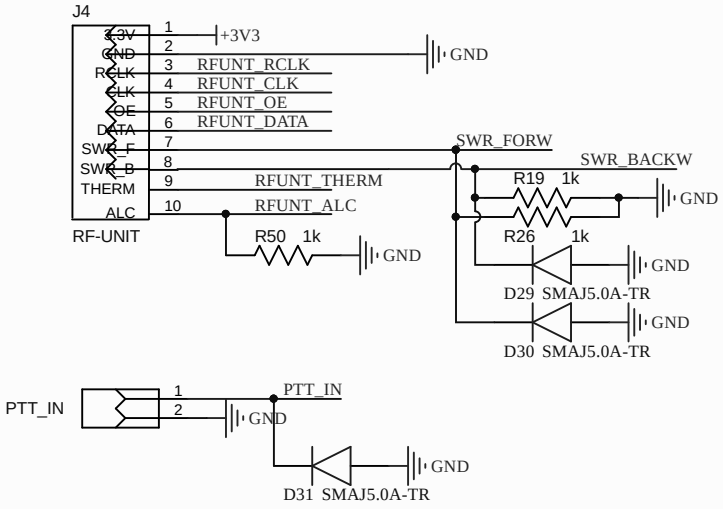
Title *ADC*			
Size: A4	Number:3	Revision:2.0	
Date: 18.02.2021	Time: 15:27:43	Sheet3 of 18	
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\Experimental\MOTHERBOARD\ADC.SchDoc			

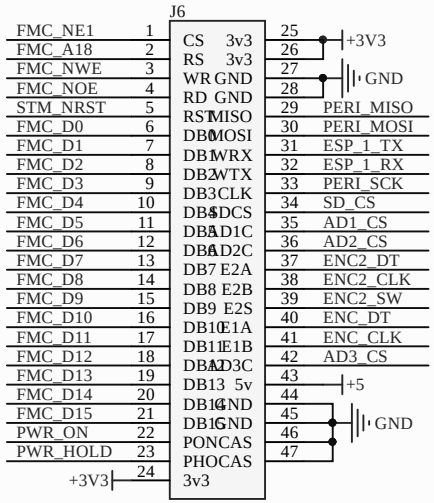


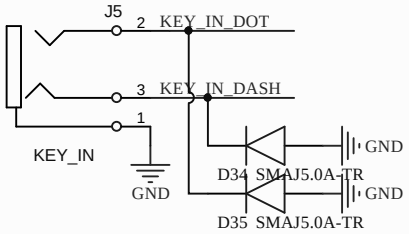
Title	***AUDIO CODEC***		
Size: A4	Number:5	Revision:2.0	
Date: 18.02.2021	Time: 15:27:44	Sheet5 of 18	
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\Experimental\MOTHERBOARD\AUDIO CODEC.SchDoc			

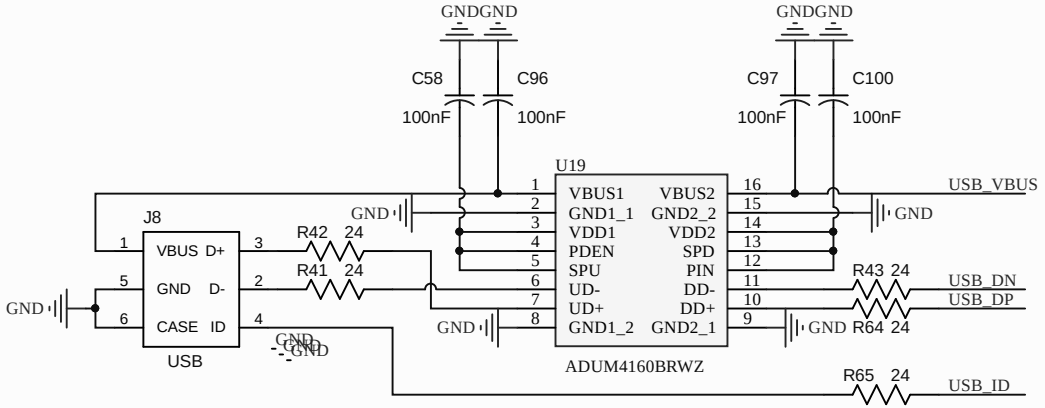


Title	***CLOCK_GENERATOR***		
Size: A4	Number: 6	Revision: 2.0	
Date: 18.02.2021	Time: 15:27:44	Sheet 6 of 18	
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\Experimental\MOTHERBOARD\CLOCK_GENERATOR.SchDoc			

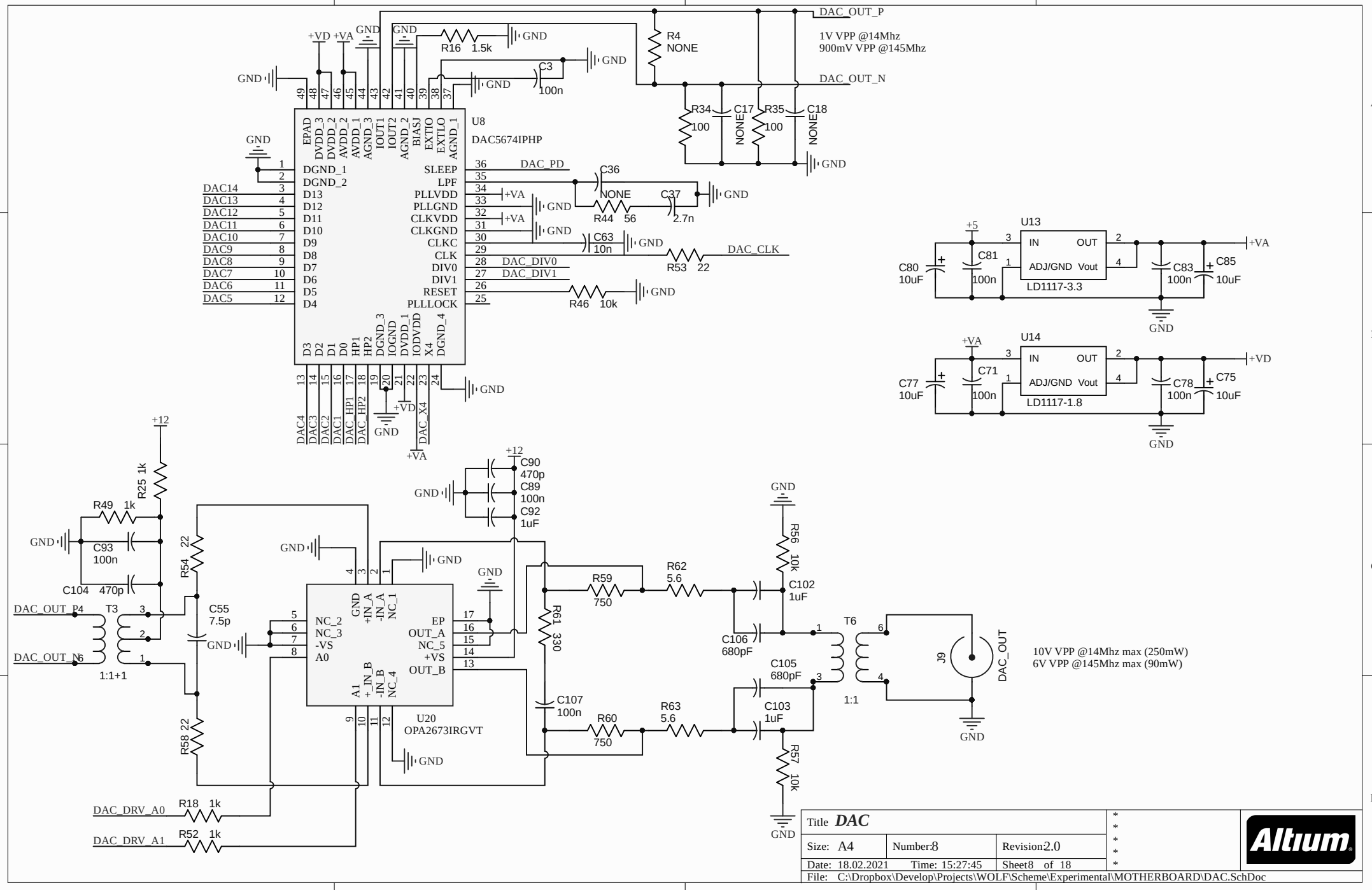


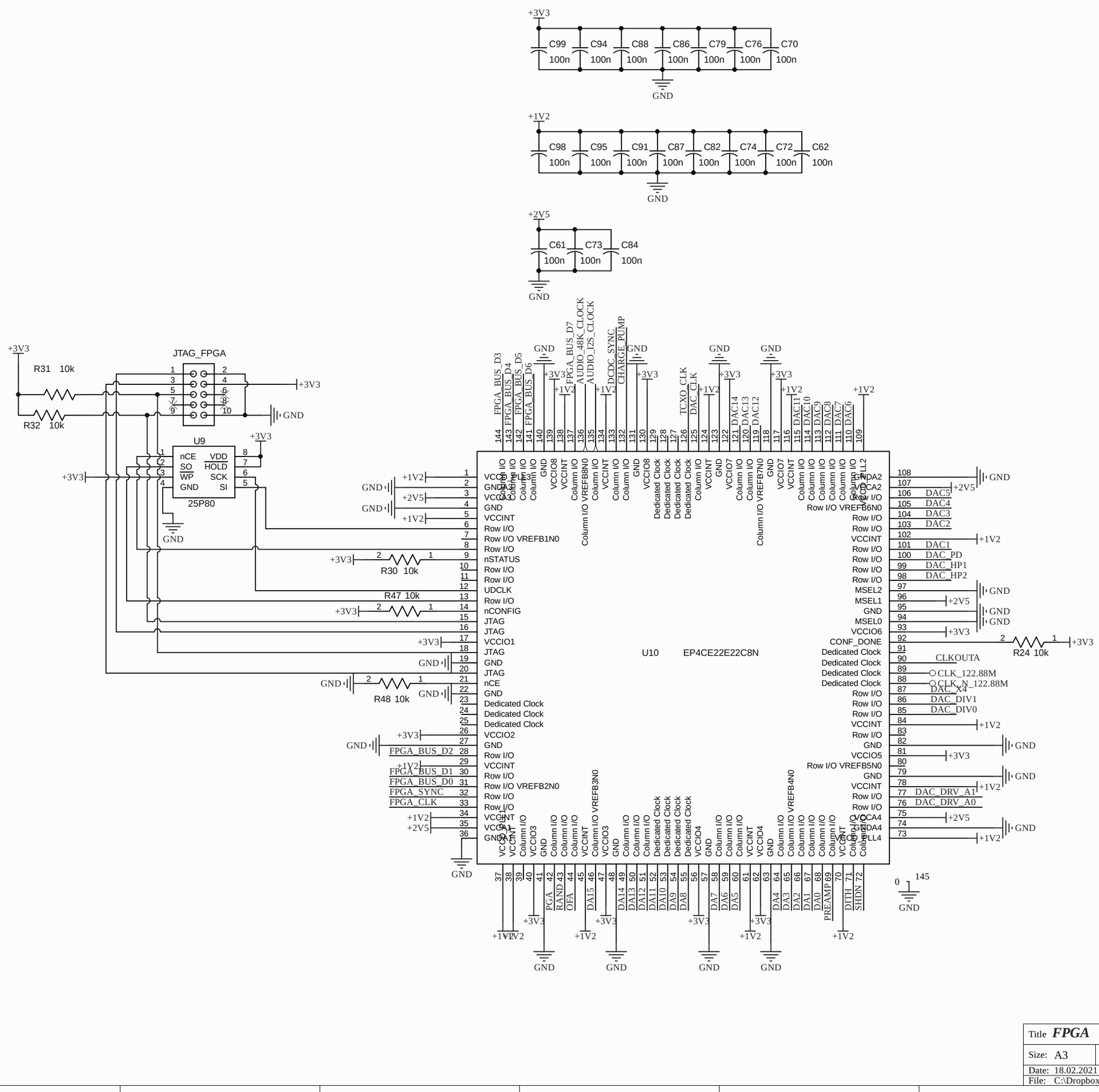






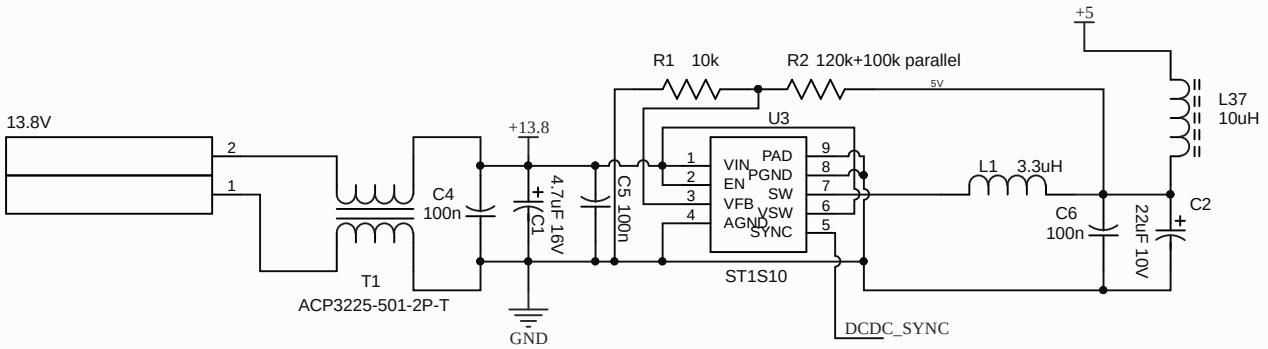
Title	***CONNECTIONS***		
Size: A4	Number:7	Revision:2.0	
Date: 18.02.2021	Time: 15:27:44	Sheet7 of 18	
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\Experimental\MOTHERBOARD\CONNECTIONS.SchDoc			

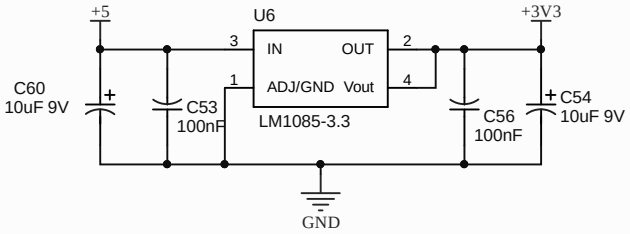

DAC_OUT_P
1V VPP @14Mhz
900mV VPP @145Mhz
DAC_OUT_N
R4
NONE
R16 1.5k
C3
100n
R34 100
C17 NONE
R35 100
C18 NONE
U8
DAC5674IPHP
EPAD DVDD_3 DVDD_2 AVDD_2 AVDD_1 AGND_3 IOUT1 IOUT2 AGND_2 BIASJ EXTIO EXTLO AGND_1
DGND_1 DGND_2 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4
SLEEP LPF PLLVDD PLLGND CLKVDD CLKGND CLKC CLK DIV0 DIV1 RESET PLLLOCK
D3 D2 D1 D0 HP1 HP2 DGND_3 IOGND DVDD_1 IODVDD X4 DGND_4
DAC14 DAC13 DAC12 DAC11 DAC10 DAC9 DAC8 DAC7 DAC6 DAC5
DAC4 DAC3 DAC2 DAC1 DAC_HP1 DAC_HP2 DAC_X4
DAC_PD
C36 NONE
C37 2.7n
R44 56
C63 10n
DAC_CLK
R53 22
DAC_DIV0
DAC_DIV1
R46 10k
U13
LD1117-3.3
C80 10uF
C81 100n
C83 100n
C85 10uF
U14
LD1117-1.8
C77 10uF
C71 100n
C78 100n
C75 10uF
R25 1k
R49 1k
C93 100n
C104 470p
R54 22
C55 7.5p
T3
1:1+1
DAC_OUT_P4
DAC_OUT_N6
C90 470p
C89 100n
C92 1uF
U20
OPA2673IRGVT
R58 22
R18 1k
R52 1k
DAC_DRV_A0
DAC_DRV_A1
R59 750
R62 5.6
R56 10k
C102 1uF
R61 330
C106 680pF
C107 100n
R60 750
R63 5.6
C105 680pF
C103 1uF
R57 10k
T6
1:1
J9
DAC_OUT
10V VPP @14Mhz max (250mW)
6V VPP @145Mhz max (90mW)
Title DAC
Size: A4
Number:8
Revision2.0
Date: 18.02.2021
Time: 15:27:45
Sheet8 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\Experimental\MOTHERBOARD\DAC.SchDoc
Altium

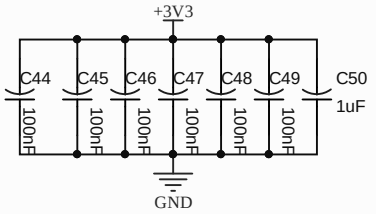


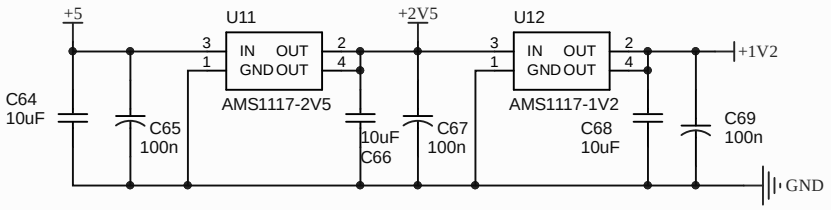
Title	*FPGA*		
Size: A3	Number: 9	Revision: 2.0	
Date: 18.02.2021	Time: 15:27:45	Sheet 9 of 18	
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\Experimental\MOTHERBOARD\FPGA.SchDoc			

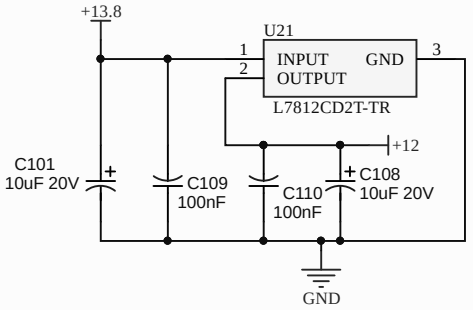
Altium





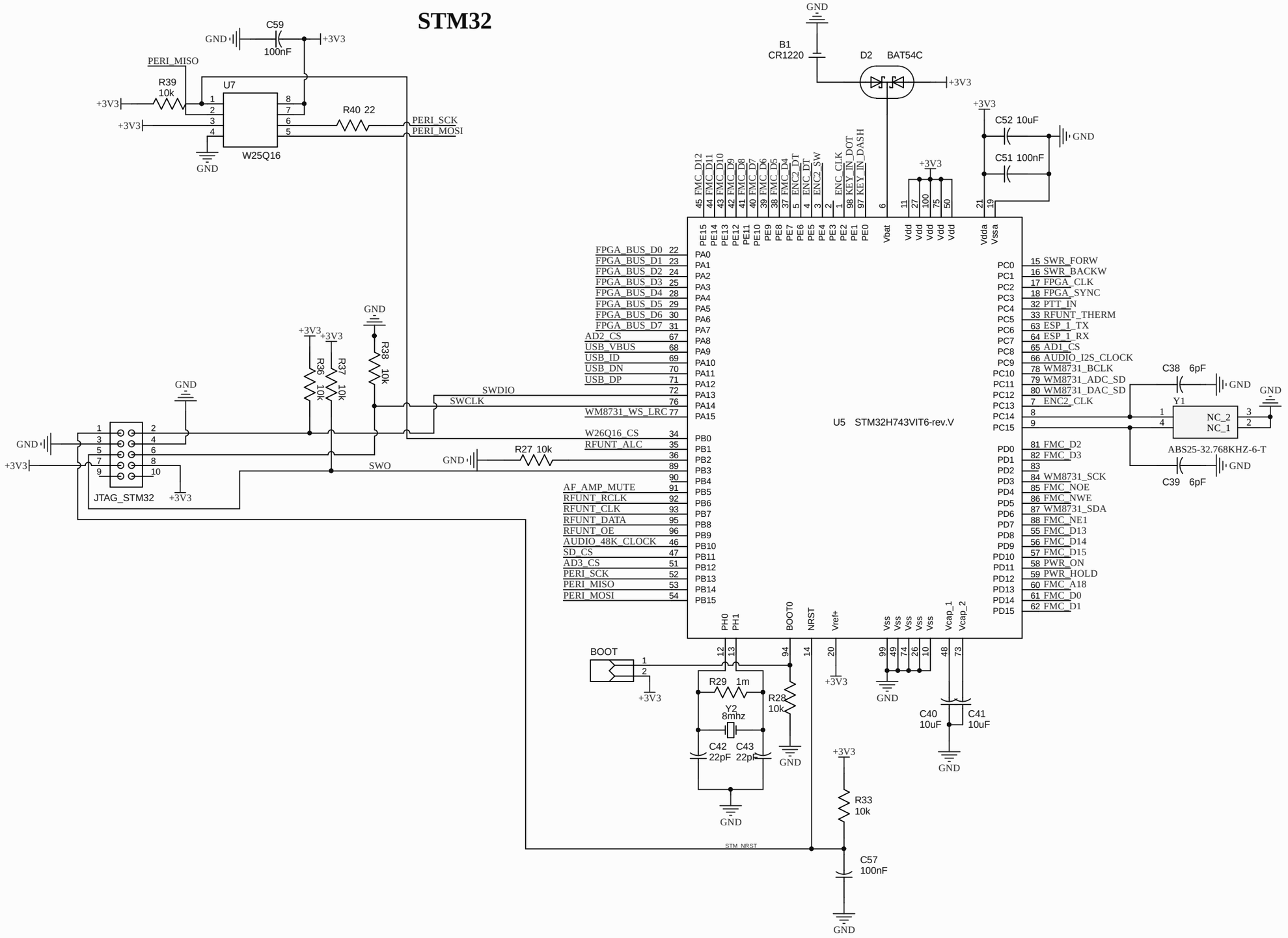






Title **POWER**			
Size: A4	Number:10	Revision:2.0	
Date: 18.02.2021	Time: 15:27:45	Sheet10 of 18	
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\Experimental\MOTHERBOARD\POWER.SchDoc			

STM32



Title	***STM32***		
Size: A3	Number:11	Revision2.0	
Date: 18.02.2021	Time: 15:27:46	Sheet11 of 18	
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\Experimental\MOTHERBOARD\STM32.SchDoc			