SPI, Intel 8080, and Motorola 6800 communication protocol between MCU and OLED driver.

Application Note AN007

Introduction

This application note describes three different communication protocols between MCU and an OLED driver.

SPI

SPI stands for Serial Peripheral Interface. It's a serial bus standard established by Motorola. Devices communicate using a master/slave relationship, in which the master initiates the data frame. SPI is a synchronous serial interface in which data in an 8-bit byte can be shifted one bit at a time (Refer to Figure 1).

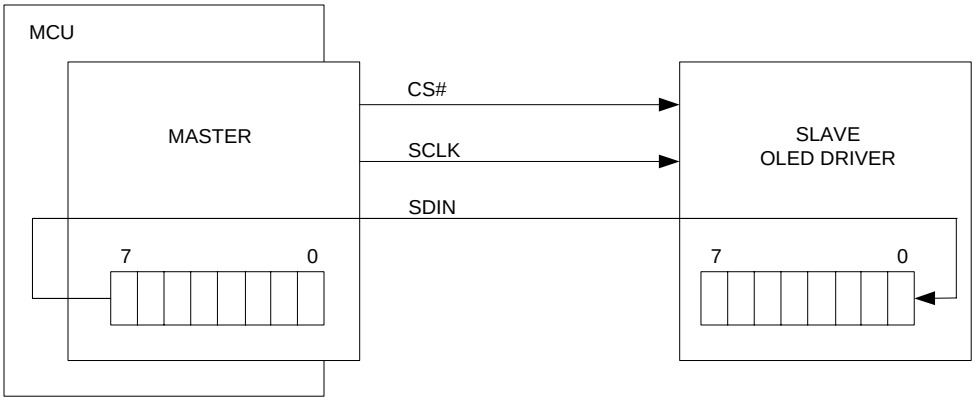

Figure 1: Two SPI Modules Connected in a Master-Slave Configuration

In the master SPI, the bits are sent out of the SDIN pin. The CS# pin must be low to select a slave device. SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, …., D0. D/C is sampled on every eight clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock (Refer to Figure 2).

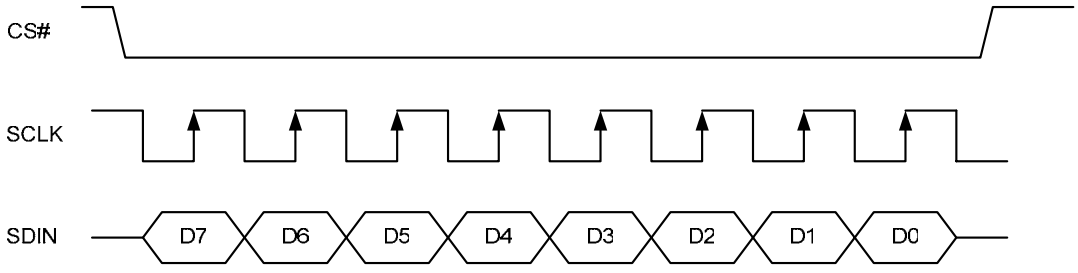

Figure 2 – Display data write procedure in SPI mode

6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), WR#, RD#, and CS#. An input high on R/W# (WR#) indicates a read operation from RAM or the status register. R/W# (WR#) input low indicates a write operation to display data RAM or Internal Command Registers depending on the status of D/C# input. The E (RD#) input serves as data latch signal (clock) when high provided that CS# is low.

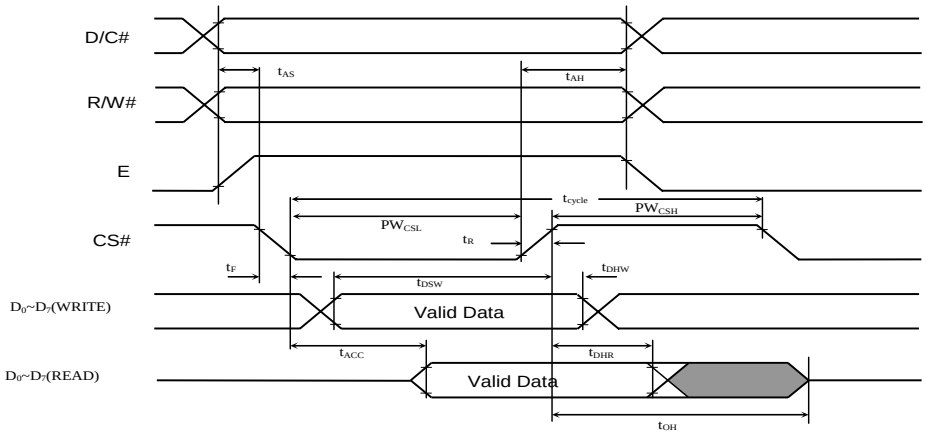

Figure 3: 6800-series MPU Timing Diagram

8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), E (RD#), R/W# (WR#), D/C#, CS#. The E (RD#) input serves as data read latch signal (clock) when it is low, and provided that CS# is low. Data read latch signal is disabled when E (RD#) is high. Display data or status register read is controlled by D/C#. R/W# (WR#) input serves as data write latch signal (clock) when it is low and provided that CS# is low. Display data or command register write is controlled by D/C#.

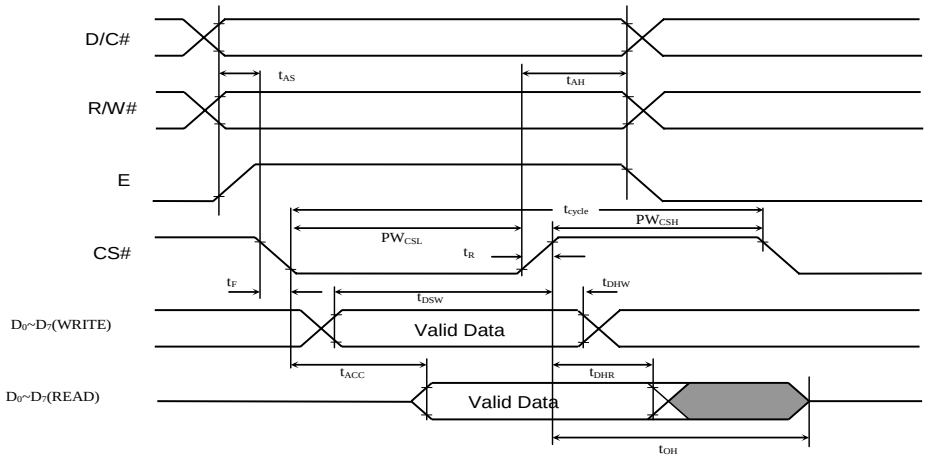

Figure 4: 8080-series MPU Timing Diagram

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