Characterizing Optimizations to Memory Access Patterns using Architecture-Independent Program Features

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ABSTRACT

High-performance computing developers are faced with the challenge of optimizing the performance of OpenCL workloads on diverse architectures. The Architecture-Independent Workload Characterization (AIWC) tool is a plugin for the Oclgrind OpenCL simulator that gathers metrics of OpenCL programs that can be used to understand and predict program performance on an arbitrary given hardware architecture. However, AIWC metrics are not always easily interpreted and do not reflect some important memory access patterns affecting efficiency across architectures. We propose a new metric of parallel spatial locality – the closeness of memory accesses simultaneously issued by OpenCL workitems (threads). We implement the parallel spatial locality metric in the AIWC framework, and analyse gathered results on matrix multiply and the Extended OpenDwarfs OpenCL benchmarks. The differences in the observed parallel spatial locality metric across implementations of matrix multiply reflect the optimizations performed. The new metric can be used to distinguish between the OpenDwarfs benchmarks based on the memory access patterns affecting their performance on various architectures. The improvements suggested to AIWC will help HPC developers better understand memory access patterns of complex codes and guide optimization of codes for arbitrary hardware targets.

KEYWORDS

Architecture Independent Analysis, Heterogenous Computing, Workload Characterization, Memory Access Patterns

1 INTRODUCTION

High-performance computing (HPC) systems are increasingly heterogeneous. A single node on a modern supercomputer may combine traditional CPUs with one or more accelerators such as GPUs, Field Programmable Gate Arrays (FPGAs), or many integrated core devices (MICs). High bandwidth interconnects support tight integration between multiple devices of different types on a single compute node.

The OpenCL programming language is designed to support modern HPC software engineers in writing code that executes on multiple hardware targets. This gives HPC software developers greater flexibility by allowing codes aimed at a range of hardware targets to be written in a single programming language environment.

Application codes differ in resource requirements, control structure and available parallelism. Similarly, compute devices differ in number and capabilities of execution units, processing model, and available resources. These heterogeneous computing environments present opportunities for software engineers and HPC integrators to design highly optimized systems with multiple kernels executing on hardware targets best suited for the diverse computational tasks performed by each kernel [18]. However, this opportunity also presents a challenge in optimizing code to run on diverse architectures. The work reported here aims to help HPC developers understand and optimize memory access patterns to improve performance on heterogeneous systems.

In the evolution of computer architectures over the last few decades, the exponential growth in computational capability has not been matched by proportional increases in memory speeds[4]. Memory accesses pose larger bottlenecks to performance as application demand for main memory scales with the arithmetic capability of computer systems. To mitigate this latency, modern CPU designs have employed a wide

range of cache technologies to reduce main memory accesses using the principle of *spatial locality*: the observation that data that a program accesses close together in time tend to also be close together in memory. On the other hand, GPUs rely on hardware multithreading to hide memory latency, and their architectures favour ALU capability over sophisticated logic to manage a cache hierarchy and out-of-order execution. As a result, the performance of kernels on CPUs and GPUs alike is strongly dependent on memory access patterns intrinsic to the code.

Our aim in this paper is to develop a framework to guide HPC software engineers in hardware-dependent code optimization – specifically by guiding the improvement of memory access patterns. We provide examples of manufacturer-recommended code optimizations to improve memory access patterns on the target architecture, and examine these using the architecture-independent workload characterization (AIWC) [8] plugin for Oclgrind [16]. Our work highlights the benefits and challenges arising from an architecture-independent analysis of memory-based program characteristics. We propose two new metrics for AIWC to better characterize these memory-based optimizations. We measure the presented codes using the new metrics and demonstrate the metrics' effectiveness in capturing the essence of the optimizations performed.

The structure of this paper is as follows. In section 2 we use the example of matrix multiplication on a GPU to showcase the specific vendor-recommended optimizations our work aims to measure. In section 3 we discuss how AIWC and its precursors profiled memory access patterns in an architecture-independent fashion and also consider relevant architecture-dependent approaches to memory access profiling. In section 4 we consider non-parallel memory metrics collected by AIWC and evaluate the suitability of these metrics for capturing the impact of performance optimizations to various OpenCL codes. In section 5 we propose a new parallel spatial locality metric, implement it in the AIWC framework, and evaluate it over the matrix multiplication example from section 2. In section 6 we present the collected metric for selected benchmarks from the Extended OpenDwarfs benchmark suite to validate our methodology in this paper. In section 7 we summarize our findings and present guidelines for interpreting the new parallel spatial metric for OpenCL codes. Finally, in section 8 we discuss further avenues to extend our work and conclude.

2 MOTIVATING EXAMPLE

We aim to capture the essence of vendor-recommended optimizations for target architectures in our metrics. We demonstrate the optimization strategies using an OpenCL kernel which multiplies square matrices of order N. We start with a simple unoptimized kernel, and then improve the memory

access patterns of this kernel by incrementally performing the optimizations recommended in the CUDA Optimization Handbook [14] for NVIDIA GPUs. These incrementally optimized OpenCL codes are then analysed using AIWC to determine the accuracy in profiling favourable memory access patterns of the current framework and the proposed extensions to AIWC.

Simple Unoptimized Matrix Multiplication

The unoptimized matrix multiplication kernel presented in Appendix A is used as a baseline to validate the performance improvements measured from each following optimization. Each thread of the kernel updates the ($globalRow$, $globalCol$) element of matrix C by computing the dot product of the corresponding row of A and column of B. With square matrices of order 2048, we observe an effective performance of 131 GFLOP/s on an NVIDIA Tesla P100 GPU.

Using Shared Memory to Coalesce Global Memory Access to Matrix A

We first notice that the number of global memory accesses to matrices A and B increases as $O(N^3)$ with respect to matrix size N. Global memory is typically located off-chip and accesses induce large delays. NVIDIA GPUs coalesce global memory loads and stores issued within thread-groups into as few DRAM transactions as possible. Multiple global memory loads and stores are coalesced into a single transaction when certain device-specific conditions are met. On most NVIDIA GPUs, data accesses are coalesced when multiple requests are made for memory locations from the same cache line in global memory [15]. Appendix B contains the `coalescedA` kernel, which coalesces accesses to matrix A by storing *tiles*, or square blocks, of A's values into shared memory (OpenCL `__local` memory). We see an improvement to 600 GFLOP/s in effective performance for order 2048 matrix multiplication.

Using Shared Memory to store Tiles of Matrix B

The code is further optimized by improving the locality of reads from Matrix B. While in the previous kernel each thread reads only a single element of matrix A from global memory, each thread reads a full column of matrix B. The repeated reads of elements of matrix B can be shared between threads in a work group by reading tiles from matrix B into shared memory. Appendix C contains the `coalescedAB` kernel which performs this optimization. Performance is further improved to 614 GLOP/s after this optimisation.

Optimizing Handling of Shared Memory

NVIDIA shared memory is divided into multiple banks – stored in independent memory modules – to allow parallel memory access. Bank conflicts occur when shared memory in the same bank is accessed concurrently. The code

in `coalescedAB` kernel is further optimized by implicitly transposing tiles of Matrix *A* while loading from global memory. This improves memory bank utilization during reads to shared memory. The `coalescedABT` kernel demonstrates this optimization by modifying lines 20,21 of `coalescedAB` to:

```
20      ASub[localCol][localRow] = A[tiledRow];
21      BSub[localRow][localCol] = B[tiledCol];
```

We achieve 1061 GFLOP/s after applying all the recommended GPU memory optimisations to the simple matrix multiply kernel.

All the examples above are an incomplete listing of optimization strategies developers can apply to code targeted at NVIDIA GPUs. In section 4, we will compare the collected AIWC metrics with the expected effect of each optimization to examine how effectively our methodology uncovers underlying bottlenecks and guides optimization efforts.

3 RELATED WORK

Hoste and Eeckout [5] show that while conventional architecture-dependent characteristics are useful in locating performance bottlenecks, they can hide the underlying, inherent program behaviour causing performance bottlenecks. A conceptual understanding of the performance characteristics of complex codes is necessary for the programmer to effectively optimize these codes. Architecture-dependent characteristics typically include instructions per cycle (IPC), cache and branch prediction miss rates, page faults and DRAM bus data transfer rates. These are typically collected using hardware performance counters available on most target architectures. These performance counters do not serve to guide optimization beyond highlighting potential bottlenecks [3, 5]. Further, in many cases, architecture-dependent characteristics cannot be directly correlated to specific code patterns. For example, the causes of high cache miss rates in the execution of a program are complex and depend on microarchitecture specific features such as cache size, prefetch behaviour and cache placement policies. A HPC developer tasked with optimizing code for a given hardware target would benefit from architecture-independent metrics of the code that can be used to measure the effect of code modifications. These metrics would help to guide the developer in both finding and fixing performance bottlenecks.

To address the limitations of conventional microarchitecture-dependent characteristics, Hoste and Eeckout [5] developed the Microarchitecture-Independent Workload Characterization tool (MICA). They observed that performance counter-based approaches to profiling codes often failed to find underlying program features that map to improved or worsened usage of performance-critical hardware features of the target architecture. The MICA framework is a holistic characterization tool, and thus collects features including instruction mix, instruction-level parallelism, register traffic, data stream strides and branch predictability.

Of these metrics, data stream strides are of particular interest in memory access pattern profiling. MICA's stride length metric measures the distance between consecutive memory accesses in a single-threaded application. For CPU architectures running single-threaded applications, this metric correlates to the spatial locality of memory accesses – a measure of how closely bunched are memory access in nearby times. This is directly correlated to cache reuse rates, critical to code performance on CPUs [6].

The MICA approach was tailored for single-threaded applications as the metrics collected rely heavily on Pin instrumentation [13]. As such, MICA is unsuited to analysing HPC workloads with heavy use of parallelism. The Workload ISA-Independent Characterization for Applications (WI-ICA) [17] extends MICA to present a framework to analyse single-threaded programs independent of the instruction set architecture (ISA).

Kim and Shrivastava [11] present CuMAPz, a CUDA memory access profiling tool to guide NVIDIA GPU optimizations. CuMAPz focuses on the problem of improving CUDA application performance using NVIDIA memory-based optimizations. CuMAPz analyses CUDA codes structurally and simulates code execution on the memory hierarchy of specific NVIDIA GPU models.

During simulation of the target code, CuMAPz records all memory accesses in various buffers to simulate the global and shared memories on NVIDIA GPUs. Using this detailed simulation data, CuMAPz can estimate the performance-critical (i) shared memory data reuse profit, (ii) profit from coalesced access (iii) memory channel skew cost and (iv) bank conflict cost characteristics of the target code.

The simulation environment used by CuMAPz and the attached analysis framework is highly specific to CUDA enabled GPUs. Replicating the CuMAPz framework for all target architectures is challenging. However, CuMAPz is an interesting simulator from the standpoint of this paper's work since it adheres to the core parts of NVIDIA GPUs' memory models in its analysis, while allowing the user to specify their GPU model specific hardware information.

Our approach is an architecture-independent analysis of memory access patterns to provide metrics correlating to similar performance critical memory access optimizations as CuMAPz. We aim to further the state of the art by providing a framework to guide developers in optimizing OpenCL codes for any given target architecture. To the best of our knowledge, none of the previous works presents a set of performance metrics that accurately characterize memory

access patterns of parallel applications independent of the target architecture.

The Architecture-Independent Workload Characterization (AIWC) tool [8] collects a set of instruction set architecture (ISA)-independent features based on those identified by Shao and Brooks [17]. AIWC runs as a plugin to the Oclgrind [16] framework, which simulates OpenCL kernel execution on an ideal device according to the OpenCL execution and memory models. AIWC collects metrics of kernel memory access, including simple counts such as the (i) total memory footprint, the total number of unique addresses accessed; and (ii) 90% memory footprint, the number of unique addresses covering 90% of memory accesses. While these metrics are architecture-independent, they are correlated to program performance on typical architectures. For example, a small ratio of 90% memory footprint to total memory footprint indicates that a program accesses a small subset of memory addresses frequently, which is highly beneficial for performance in a cached memory hierarchy.

AIWC also records the global memory address entropy (GMAE), a positive real number corresponding to the randomness of the memory access distribution of a program. To measure locality of memory accesses, AIWC collects the local memory address entropy (LMAE) of memory addresses accessed after dropping n least significant bits of all memory addresses accessed by the program. To calculate this, AIWC collects a frequency distribution of all non-register memory accesses by all threads in the target kernel. Using the collected frequency distribution, AIWC calculates 10 separate local memory address entropy (LMAE) values according to increasing number of least significant bits (LSB) skipped using the explicit formula for the n-bits skipped LMAE:

$$LMAE_{n-bits} = \sum_{a \in A_n} p_a \log_2(p_a^{-1}) \qquad (1)$$

- A_n is the set of all addresses accessed after skipping n LSBs of each address.
- $p_a := \frac{\#access_a}{\#access_{total}}$ is the probability (calculated as relative frequency) at which each memory address is accessed.

LMAE measures the locality of memory accesses performed over the full execution of a program. A steeper drop in entropy with increasing number of bits may correlate to more localized memory accesses over the program's execution.

4 NON-PARALLEL MEMORY METRICS

We first consider AIWC memory metrics that do not take into account the interaction between work items executing in parallel. We compare these metrics for the incrementally

optimized versions of the matrix multiplication example presented in section 2.

In addition to the memory metrics reported in [8], we added a new metric of relative local memory usage. This measures the proportion of all memory accesses from the symbolic execution of the kernel that occurred to memory allocated as `__local`. On NVIDIA GPUs, this memory address space is mapped to fast on-chip shared memory. Relative local memory usage is an example of a metric that is useful to measure performance-critical access patterns on some architectures such as GPUs, and not others, such as CPUs. CPUs do not typically have a notion of user-controlled on-chip memory shared between hardware threads such as NVIDIA GPUs' shared memory. This is a natural consequence of programming for a heterogeneous system. Specific code patterns may translate to performance improvements only on certain hardware.

In the original AIWC tool [10], global and local memory address entropy (MAE) were calculated using physical addresses of memory used by the Oclgrind simulator back-end of AIWC. This caused irregularities in entropy calculations across multiple runs of the same simulation. We improved the calculation of memory address entropy by using *virtual addresses* to calculate MAE values using an abstract ideal address space on which all memory accesses by the kernel occur. This allows AIWC to accurately abstract over the hardware and ISA-specific differences in memory layouts across the diverse hardware targets.

Figure 1 shows execution times for the matrix multiplication kernels presented in section 2 for $N \times N$ matrices of different sizes. We recorded kernel execution time exclusive of data transfer on an NVIDIA Tesla P100 using NVIDIA OpenCL 1.2 CUDA 10.1.236 (driver 418.87), and took the average of 100 runs. Across varying problem sizes, the vendor recommended optimizations to the matrix multiplication code lead to increased performance.

Table 1 summarizes AIWC memory metrics collected for each of the matrix multiply kernels in section 2. Note that only two LMAE values are shown for brevity. We now analyse the effectiveness of AIWC metrics in profiling the NVIDIA recommended memory optimizations applied to the matrix multiplication kernel.

Relative local memory usage: As reliance on NVIDIA GPUs' shared memory increases in each kernel from `simple` to `coalescedAB`, we find that the proportion of OpenCL local memory usage increases as expected.

Global and local MAE: Entropy measurements decrease from `simple` to `coalescedAB`, as the optimizations reduce the number of reads from matrices A and B in global memory, replacing these with reads from smaller tiles in local memory. We observe an almost completely uniform distribution of memory accesses in `simple`, where the program makes N
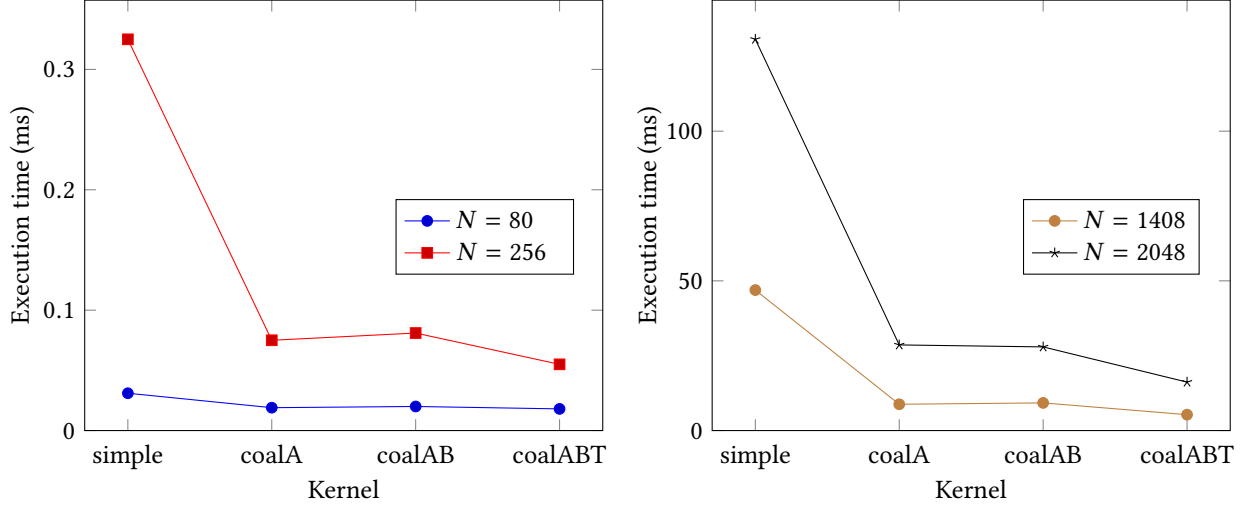
Figure 1: Execution time of matrix multiplication kernels (NVIDIA Tesla P100)

	simple	coalescedA	coalescedAB	coalescedABT
Total memory footprint	196608	196608	196608	196608
90% Memory Footprint	118196	56176	489	489
Global MAE	17.02	13.18	9.78	9.78
LMAE #bits=3	16.02	12.18	8.78	8.78
LMAE #bits=10	9.02	5.18	1.78	1.78
Relative Local Memory Usage	0	0.50	0.94	0.94

Table 1: Selection of AIWC[8] metrics for 256×256 matrix multiplication

loads to each element of A and B with N the dimension of the matrices. The distribution of memory accesses becomes increasingly non-uniform as we perform fewer accesses to matrices A and B and more accesses to smaller local memory buffers, resulting in decreases in local and global memory entropy values from simple to coalescedAB.

Memory Footprint: Similar to trends in global and local MAE, we find that the ratio of 90% memory footprint to total memory footprint decreases from 60.12% for simple to 0.25% (coalescedAB). Increased utilization of local memory in the optimized kernels means that the local memory buffers make up a greater proportion of total memory accesses in the program. As the local memory buffers are small and reused within a workgroup, the memory footprint of the local memory buffers is also smaller.

AIWC's metrics strongly reward optimizations that tend to localize memory accesses. Local memory buffers are typically smaller than global memory arrays when programming

for GPUs due to hardware limitations on sizes of shared memory [15]. However, the metrics currently measured by AIWC do not have a direct causal relation to code patterns that optimize memory accesses on GPUs. The proposed relative local memory usage metric is the first to correspond to a recommended optimization strategy of using fast on-chip shared memory. Further, we find that all current AIWC metrics do not measure any sizeable difference between coalescedAB and coalescedABT codes. We address this by proposing another new metric for locality of memory accesses in the following section.

5 A PARALLEL SPATIAL LOCALITY METRIC

Aggregate metrics of the kind presented by AIWC necessarily present a simplified view of program behaviour, omitting many details. Different ways of aggregating program measurements lead to different features of program execution being emphasized in the final metrics. For example, the calculation of memory address entropy described in section 3

relies only on the frequency distribution of memory accesses to all addresses accessed by the kernel, and discards temporal information. The order of sequential memory accesses performed by each thread, as well the relationship between work items in an OpenCL work group, are both vital in accurately characterizing parallel codes.

We propose a new architecture-independent metric, *parallel spatial locality*, to measure memory access patterns in parallel programs. The proposed metric is inspired by CuMAPz' direct approaches to measuring optimization specific characteristics of CUDA codes.

During simulation, AIWC collects a list of all memory accesses by each thread of execution. In the OpenCL programming model, threads within a work groups execute the same code and share access to *local memory*. We can group together memory accesses of threads in a work group at each logical time step in the symbolic execution of the code. On a GPU, memory accesses executed at the same time by different threads in a work group are likely to interact, determining the extent of memory access coalescing and bank conflicts.

There are three steps involved in generating an AIWC metric: *recording*, *calculating* and *summarizing* data collected from the symbolic execution of the kernel under inspection.

Record: we first record memory accesses performed by each thread in an OpenCL work group as described above to achieve a global ordering of all memory accesses performed by the group. This ordering is collected in the form of logical timestamps $(t_0..t_{last})$ at which memory accesses occur.

Calculate: for each timestamp $t = t_0..t_{last}$, calculate the n-bits-dropped entropy of memory addresses accessed by all threads in a work group within the timestamp t. Here n can range between 0 and 10 as was the case for *LMAE*.

Summarize: average the collected entropy values across all the timestamps to calculate the parallel spatial locality metrics for one thread group. We then average the n-bits-dropped entropy summaries across thread groups to obtain the n-bits-dropped parallel spatial locality metrics for the kernel's execution. The theoretical maximum for an n-bits dropped parallel spatial locality value is $\log_2(group\_size)$. We divide the calculated average entropy values by $\log_2(group\_size)$ to normalize the parallel spatial locality metric. This allows us to derive trends on the normalized metrics allowing comparison across separate OpenCL codes with different work distribution structures.

The proposed metric is a parallel computing analogue for MICA's data stride metric that measures the distance between consecutive data accesses in a single-threaded environment. In parallel programs, to accurately measure spatial locality of accesses, we must consider memory accesses performed by multiple threads in a close temporal scope. The proposed metric calculates the locality of accesses in

each time step of the program's execution and steeper reductions in n-bits-dropped parallel spatial locality scores will be observed in programs that often access nearby memory addresses within the same timestamp. Such programs will perform better on GPUs, as they will make better use of both global memory access coalescing and shared memory bank structures. To a lesser extent, the proposed metric reflects performance-critical memory access patterns on CPUs, as pulling a single cache line from global memory into last-level cache may improve memory access times for all CPU cores.

Figure 2 shows the proposed parallel spatial locality metric as measured by AIWC for each of the matrix multiplication kernels from section 2. We observe that the `coalescedABT` kernel has the steepest reductions in entropy as the number of bits skipped is increased, which correlates to better locality of parallel memory accesses. It is expected for this kernel to exhibit better parallel spatial locality than `simple`, as `coalescedABT` makes use of local memory, where accesses tend to be localized simply due to the small size of shared on-chip memory typically available on GPUs. Further we find that the proposed metric successfully distinguishes between the `coalescedAB` and `coalescedABT` kernels. It accurately depicts a steeper reduction for the more optimized `coalescedABT` kernel, where a larger proportion of parallel memory accesses make better use of the memory bank structure of GPU shared memory than all previous kernels. This is a significant improvement over the state-of-the-art AIWC metrics in characterizing how codes localize simultaneous memory accesses to better use the hardware provided.

6 EVALUATION: EXTENDED OPENDWARFS BENCHMARK SUITE

The Extended OpenDwarfs benchmark suite [9, 12] is a set of diverse OpenCL workloads. Each benchmark is assigned to one of the 13 Berkeley Dwarfs, common computational and communication patterns which aim to capture the landscape of parallel computing workloads [2]. To show that the proposed parallel spatial locality metric is useful for understanding performance properties of a wide range of application codes, we present the results of running the AIWC tool on selected benchmarks from the suite [1]. The workloads presented are not optimized for any specific architecture – hence optimizations using OpenCL local memory (which translates to CUDA shared memory) are not performed.

Many of these benchmarks can be run with up to four problem sizes based on the sizes of caches found in modern CPU memory hierarchies [9]. For these results we used a problem size setting of *medium*, except for the GEM benchmark, which is run at a setting of *tiny*. For benchmarks such as BFS that have multiple kernel invocations per run, we present the AIWC parallel spatial locality metrics for the invocation with the highest number of LLVM-SPIR instructions
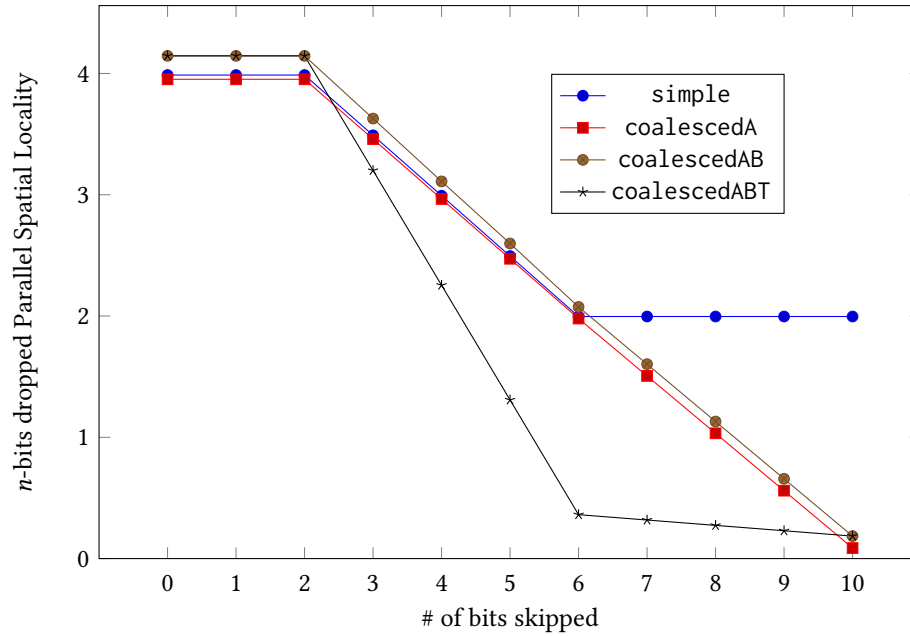
Figure 2: Parallel spatial locality metric obtained from AIWC for matrix multiply kernels for 256 × 256 matrix multiplication

executed. Note that the presented benchmarks use 32-bit numeric types (OpenCL `int` and `float`), so dropping up to 2 bits of the memory addresses accessed will not change the parallel spatial locality, since any addresses accessed are at least 4 bytes apart.

N-body methods: GEM

The GEM benchmark computes the electrostatic potential of a biomolecule by calculating the sum of charges contributed by all atoms in the biomolecule at each specific surface vertex. This is an embarrassingly parallel problem. Each OpenCL work-item operates on a single surface vertex, finding the electrostatic potential generated by looping through every atom in the biomolecule in global order. The computation pattern is highly regular and memory accesses are perfectly synchronized. Atom data is accessed consecutively, with all work-items simultaneously accessing each atom's data. The parallel spatial locality metric reflects this pattern of efficient memory utilization (single loads from global memory servicing all OpenCL work-items). The recorded parallel spatial locality approaches the theoretical limit of 0 (0.0124 at 10 bits dropped). This indicates that almost all memory accesses made by the kernel are perfectly synchronized between OpenCL threads. Performance results [9, 12] show that GEM performs significantly better on GPUs than on CPUs, as memory unit stalls are at low levels for both CPUs and GPUs due to the highly efficient memory utilization of this benchmark. As memory operations do not present a

bottleneck, this benchmark is able to take advantage of the superior floating-point compute capability of GPUs [12].

Dense Linear Algebra: Lower-upper decomposition (LUD)

LUD in OpenDwarfs is a program to decompose an input $N \times N$ matrix as the product of one lower and one upper diagonal matrix. Memory access patterns in a dense linear algebra workload such as LUD are typically highly regular and deterministic for each OpenCL work item, based on the matrix dimension and offset parameters. The OpenDwarfs implementation of LUD [1] splits the LUD computation into three kernels: LUD perimeter and LUD diagonal kernels spawn work-items in a single work dimension; while LUD internal is decomposed in both dimensions of the input.

The LUD kernels partially benefit from memory access coalescing on GPUs, for the lines of code where all the work-items access contiguous memory along a row of the input matrix. However, when threads simultaneously access a column of the input matrix, multiple memory requests are made as addresses accessed are too distant to be coalesced into a single memory transaction on GPUs. This is reflected in the drop in parallel spatial locality for the LUD kernels to approximately half the value at 0 bits skipped. Taking LUD internal as an example, the 0-bits skipped parallel spatial locality metric is 0.5115, while the 10-bits skipped parallel spatial locality metric is 0.2561. The swift decline of the
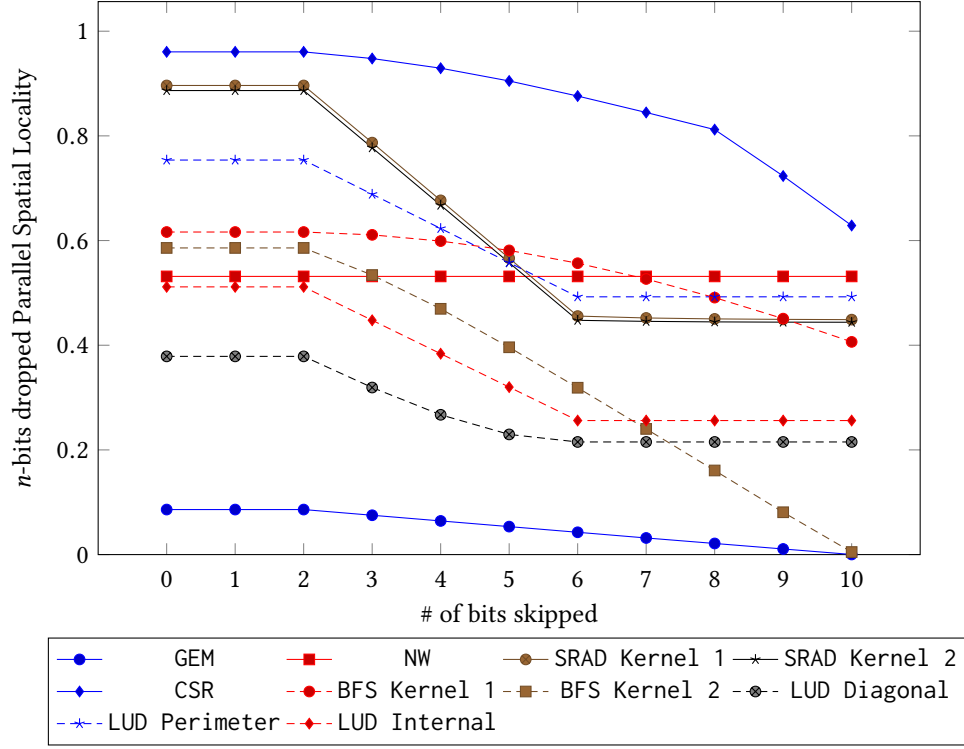
Figure 3: Normalised parallel spatial locality metric for selected OpenDwarfs benchmark kernels

metric to 0.2561 from 2 to 6-bits skipped parallel locality indicates that approximately half the parallel memory accesses in `LUD internal` are highly localized. This occurs when work-items simultaneously access contiguous memory along a matrix row. Similar to the presented matrix multiply codes, LUD can be optimized for GPUs by effective utilization of shared memory [1].

Dynamic Programming: Needleman-Wunsch (NW)

Needleman-Wunsch is a dynamic programming algorithm used to perform protein sequence alignment by identifying the similarity between two strings of amino acids. The computation of each element in the similarity matrix depends on its west, north and north-west neighbours. This dependency enforces a wavefront computation pattern, travelling along the main diagonal of the matrix. Each iteration of the kernels computes over an antidiagonal of the matrix, starting at its top left corner, and finishing at its bottom right corner.

In particular, the wavefront pattern of computations causes each work-item to request distant memory addresses in a parallel fashion. Thus, parallel memory requests into the input matrix prohibit locality. We note the lack of any dropoff in parallel spatial locality as the number of bits dropped increases. This rightly indicates that memory addresses accessed at each logical timestamp are very distant. On GPUs,

this translates to poor utilization of both memory access coalescing and caching [12]. This trend in the parallel spatial locality metric suggests that a possible improvement for GPU performance would be to load blocks of the input matrix into on-chip local memory to reduce the number of global memory requests – this is typically performed in GPU optimized implementations of the Needleman-Wunsch algorithm [1].

Structured Grids: Speckle Reducing Anisotropic Diffusion (SRAD)

SRAD removes locally correlated noise from images by following a repeated grid update computation pattern on image pixel grids. Conditional statements in the code cause thread divergence, potentially within a work-group, to handle boundary conditions. These boundaries constitute a small portion of the executed work-items, especially on larger datasets and so the effective thread divergence is minimal. Memory access patterns in SRAD are statically determined and relatively localized. Similar to the LUD and `simple` kernels, both SRAD kernels observe a rapid drop-off in parallel spatial locality (figure 3) as the number of bits skipped is increased, with the metric stabilizing at approximately half its original value when 0 bits are skipped.

At each point in the kernels' memory access profile, each work-item with global ID (i, j) in an OpenCL work-group

accesses the $(i, j)^{th}$ elements of various matrices. The sequential memory access pattern is non-linear since different matrices are accessed consecutively by the kernel, prohibiting ideal caching [12]. However, memory requests made simultaneously by a work-group always fall within a rectangular block of one of the matrices. This allows memory access coalescing on GPUs for OpenCL work-items accessing contiguous matrix data, greatly reducing the number of memory requests made on each line of the kernel code on GPUs. However, work-items accessing data along a column of the matrix do not observe memory access coalescing. Thus we observe that while cache hit rates are typically low on this benchmark, particularly on GPUs [12], GPUs can hide the latency of global memory accesses through memory access coalescing to some extent.

Graph Traversal: BFS

Graph traversal algorithms require pointer chasing operations to traverse nodes of a graph and perform calculations. The Breadth-First Search implemented in OpenDwarfs calls two OpenCL kernels to traverse nodes immediately connected to the list of nodes at each depth starting from the root node. BFS is characterized by an imbalanced workload per kernel launch depending on the degree of the nodes being operated on, with only a proportion of launched nodes performing meaningful work. As such, the AIWC features collected for each kernel invocation vary significantly. The parallel spatial locality metric collects the entropy of memory accesses at each time step, and workload imbalances across work-items are dealt with by averaging entropy scores across all the time steps in the execution of an OpenCL work-group.

Of the two BFS kernels, it is `BFS kernel 1` that performs the graph traversal necessary to generate a list of neighbours at each node. The memory access patterns in `BFS kernel 1` are irregular. Work-items fetch discontinuous memory locations attributed to any particular node in the graph, depending on the connectivity of the node they operate on. The program structure involves multiple levels of pointer-chasing and thus the precise memory addresses accessed are data-dependent. This leads to poor parallel spatial locality. Thus, we see a slow dropoff in parallel spatial locality for `BFS kernel 1`.

Sparse Linear Algebra: CSR

Compressed Sparse Row Matrix-Vector Multiplication (CSR) computes the product of a sparse matrix and a dense vector. The matrix is stored in a compressed row storage sparse matrix format, which is very efficient for storage when the number of zero elements is far greater than the number of non-zero elements. Three inputs are provided to the CSR

kernel. The non-zero elements of a matrix are stored in row-major order in Ax, along with separate arrays Aj, Ap indicating the position of each non-zero element in the matrix.

In the OpenDwarfs implementation, each row of the input sparse matrix is assigned to a separate OpenCL work item. The locations of matrix data read by each work-item are dependent on the number and position of non-zero values in the sparse-matrix, which are decided by the values in Aj and Ap. Similar to BFS, this means memory access patterns are runtime-dependent due to indirect addressing. This pattern of indirect addressing is typical of applications in the Spare Linear Algebra Dwarf, which severely hinders locality of memory accesses performed. The collected parallel spatial locality metric reflects this trend. Figure 3 shows the gradual decline in parallel spatial locality as the number of bits dropped is increased.

7 GUIDELINES: USING THE PARALLEL SPATIAL LOCALITY METRIC

The recorded parallel spatial locality in GEM starts at a low value of 0.08604 and approaches the theoretical lower limit of 0 (2.18e-4 at 10 bits dropped). This indicates that almost all memory accesses made by the kernel are perfectly synchronized between OpenCL threads. From a memory performance standpoint, this is the best possible scenario as single memory accesses service all the active synchronised threads on the GPU.

Codes with a mix of favourable and unfavourable access patterns (typically involving two-dimensional matrices such as LUD and SRAD) will have a steep dropoff in PSL to about half of the starting PSL metric as n increases, and the curve flattens out at that point.

In the extreme case, when parallel memory accesses are entirely disparate as for Needleman-Wuntsch, we observe a flat parallel spatial locality graph. The worst possible memory access pattern: all threads in a workgroup accessing results in a flat PSL metric of 1. The PSL metric for Needleman-Wuntsch is a flat line at 0.53. This indicates that parallel memory accesses are entirely disparate. However, the workload imbalance across threads in each OpenCL work group eases pressure on the memory unit when not all threads are active.

Codes with irregular or data-driven memory access patterns like CSR and BFS in the OpenDwarfs Suite have a slow dropoff in the PSL metric at low n values. This is reflective of the mostly disparate parallel memory access pattern in these codes. The increasing steepness of the dropoff at higher n in codes with data-driven memory accesses is reflective of the size of buffers being operated upon as the data structures used during computation cause localisation of memory accesses.

8 CONCLUSIONS AND FUTURE WORK

To the best of our knowledge, this work is the first to propose the use of architecture-independent metrics of parallel memory access to characterise hardware-specific optimization. We implemented and evaluated a new feature, relative local memory usage, to help characterize memory-based GPU code optimizations. We also implemented a new parallel spatial locality metric to capture the idea of closeness of memory accesses made by parallel OpenCL workloads. We ran the enhanced AIWC tool on matrix multiply kernels and selected OpenDwarfs benchmarks, presenting results and analysis to validate our methodology.

Our proposed parallel spatial locality metric may also correlate to some memory-based optimization strategies for CPUs. Future work would apply the approach followed by this paper to optimizations for CPU and FPGA architectures to critically evaluate the viability of AIWC in analyzing memory access patterns in codes targeted to these architectures.

REFERENCES

[1] Extended OpenDwarfs. https://github.com/ANU-HPC/OpenDwarfs/commit/dee488cac9833f029dfada35ff6ae4077b68c4b5, Jan 2020.

[2] Krste Asanovic, Ras Bodik, Bryan Christopher Catanzaro, Joseph James Gebis, Parry Husbands, Kurt Keutzer, David A Patterson, William Lester Plishker, John Shalf, Samuel Webb Williams, et al. The landscape of parallel computing research: A view from berkeley. Technical report, Technical Report UCB/EECS-2006-183, EECS Department, University of California, Berkeley, 2006.

[3] Karthik Ganesan, Lizy John, Valentina Salapura, and James Sexton. A performance counter based workload characterization on Blue Gene/P. In *International Conference on Parallel Processing (ICPP)*, pages 330–337. IEEE, 2008.

[4] John L. Hennessy and David A. Patterson. *Computer Architecture - A Quantitative Approach, 5th Edition.* Morgan Kaufmann, 2012.

[5] Kenneth Hoste and Lieven Eeckhout. Microarchitecture-independent Workload Characterization. *IEEE Micro*, 27(3), 2007.

[6] Intel Corporation. Intel® 64 and IA-32 Architectures Optimization Reference Manual. 2016.

[7] Beau Johnston, Gregory Falzon, and Josh Milthorpe. Opencl performance prediction using architecture-independent features. In *2018 International Conference on High Performance Computing & Simulation, HPCS 2018, Orleans, France, July 16-20, 2018*, pages 561–569. IEEE, 2018.

[8] Beau Johnston and Josh Milthorpe. AIWC: OpenCL-based architecture-independent workload characterization. *IEEE/ACM Workshop on the LLVM Compiler Infrastructure in HPC (LLVM-HPC)*, Nov 2018.

[9] Beau Johnston and Josh Milthorpe. Dwarfs on accelerators: Enhancing OpenCL benchmarking for heterogeneous computing architectures. In *Proceedings of the 47th International Conference on Parallel Processing Companion*, ICPP '18, pages 4:1–4:10, New York, NY, USA, 2018. ACM.

[10] Beau Johnston, James Price, Moritz Pflanzer, Petros Kalos, Tom Deakin, Nido Media, and Daniel Saier. BeauJoh/Oclgrind: Adding AIWC – An Architecture Independent Workload Characterisation Plugin. https://doi.org/10.5281/zenodo.1134175, December 2017.

[11] Yooseong Kim and Aviral Shrivastava. CuMAPz: a tool to analyze memory access patterns in CUDA. In Leon Stok, Nikil D. Dutt, and Soha Hassoun, editors, *Proceedings of the 48th Design Automation Conference, DAC 2011, San Diego, California, USA, June 5-10, 2011*, pages 128–133. ACM, 2011.

[12] Konstantinos Krommydas, Wu-chun Feng, Christos D Antonopoulos, and Nikolaos Bellas. OpenDwarfs: Characterization of dwarf-based benchmarks on fixed and reconfigurable architectures. *Journal of Signal Processing Systems*, 85(3):373–392, 2016.

[13] Chi-Keung Luk, Robert Cohn, Robert Muth, Harish Patil, Artur Klauser, Geoff Lowney, Steven Wallace, Vijay Janapa Reddi, and Kim Hazelwood. Pin: building customized program analysis tools with dynamic instrumentation. In *ACM SIGPLAN notices*, volume 40, pages 190–200. ACM, 2005.

[14] NVIDIA Corporation. CUDA C++ Best Practices Guide. 2019.

[15] NVIDIA Corporation. CUDA C++ Programming Guide. 2019.

[16] James Price and Simon McIntosh-Smith. Oclgrind: An extensible OpenCL device simulator. In *Proceedings of the 3rd International Workshop on OpenCL*, page 12. ACM, 2015.

[17] Yakun Sophia Shao and David Brooks. ISA-independent workload characterization and its implications for specialized architectures. In *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pages 245–255. IEEE, 2013.

[18] Kyle Spafford, Jeremy Meredith, and Jeffrey Vetter. Maestro: data orchestration and tuning for OpenCL devices. *Euro-Par 2010-Parallel Processing*, pages 275–286, 2010.

A SIMPLE KERNEL

```
1    __kernel void simpleMultiply(__global float *A,
2        __global float *B,
3        __global float *C,
4        int N)
5    {
6      const int globalRow = get_global_id(0); //
           Row ID of C (0..N-1)
7      const int globalCol = get_global_id(1); //
           Col ID of C (0..N-1)
8      // Compute a single element of C (loop over
           K)
9      float acc = 0.0f;
10     for (int k = 0; k < N; ++k) {
11       acc += B[k * N + globalCol] * A[globalRow
             * N + k];
12   `   }
13     // Store the result
14     C[globalRow * N + globalCol] = acc;
15   }
```

B COALESCEDA KERNEL

```
1    __kernel void coalescedAMultiply(
2        const __global float* A,
3        const __global float* B,
4        __global float* C,
5        const int N)
6    {
7      __local float aTile[TILE_DIM][TILE_DIM];
8
9      const int localRow = get_local_id(0);
10     const int localCol = get_local_id(1);
11
12     const int globalRow = get_global_id(0);
13     const int globalCol = get_global_id(1);
14
15     __private float sum = 0.0f;
16
17     const int numTiles = N / TILE_DIM;
18     __private const int tiledRow = globalRow*N+
           localCol;
19     for (int i = 0; i < numTiles; i++) {
20       aTile[localRow][localCol] =
             A[tiledRow+i*TILE_DIM];
21       barrier(CLK_LOCAL_MEM_FENCE);
22       for (int k = 0; k < TILE_DIM; k++) {
23         sum += aTile[localRow][k] *
               B[(i*TILE_DIM+k)*N+globalCol];
24       }
25       barrier(CLK_LOCAL_MEM_FENCE);
26     }
27     C[globalRow*N+globalCol] = sum;
28   }
```

C COALESCEDAB KERNEL

```
1    __kernel void coalescedABMultiply(
2        const __global float* A,
3        const __global float* B,
4        __global float* C,
5        const int N) {
6      __local float ASub[TILE_DIM][TILE_DIM];
7      __local float BSub[TILE_DIM][TILE_DIM];
8
9      const int localRow = get_local_id(0);
10     const int localCol = get_local_id(1);
11     const int globalRow = get_global_id(0);
12     const int globalCol = get_global_id(1);
13
14     float acc = 0.0f;
15     const int numTiles = N/TILE_DIM;
16
17     for (int i = 0; i < numTiles; i++) {
18       const int tiledRow =
             globalRow*N+i*TILE_DIM + localCol;
19       const int tiledCol = globalCol +
             (TILE_DIM*i + localRow)*N;
20       ASub[localRow][localCol] = A[tiledRow];
21       BSub[localRow][localCol] = B[tiledCol];
22
23       barrier(CLK_LOCAL_MEM_FENCE);
24
25       for (int k=0; k<TILE_DIM; k++) {
26         acc += ASub[localRow][k] *
               BSub[k][localCol];
27       }
28
29       barrier(CLK_LOCAL_MEM_FENCE);
30     }
31     C[globalRow*N + globalCol] = acc;
32   }
```