

# Characterising Optimisations to Memory Access Patterns using Architecture Independent Program Features

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## ABSTRACT

This paper addresses the challenge of profiling a code base to help programmers effectively optimise their codes for high performance. Current methods of analysing program behaviour have largely relied on performance counters on various architectures to provide architecture dependent metrics of code behaviour. However, if workload characteristics are tied to architectural features specific to a particular system, these analysis frameworks may not generalise to alternative or future systems. Considering the trend towards heterogeneous computing, we work towards a framework to guide developers in optimising codes for any given hardware target using the architecture independent workload characterisation (AIWC) tool – specifically in profiling memory access patterns of code. Metrics must be easily interpreted and conceptually linked to patterns in hardware-specific memory access optimisations. To this end we propose, implement and analyse the addition of two new metrics to AIWC and present a new approach to profile spatial locality intrinsic to parallel codes. The improvements suggested to AIWC will help HPC developers better understand memory access patterns of complex codes, a crucial step in guiding optimisation of codes for arbitrary hardware targets.

## KEYWORDS

Architecture Independent Analysis, Heterogenous Computing, Workload Characterisation, Memory Access Patterns

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## 1 INTRODUCTION

High-performance computing (HPC) systems are increasingly incorporating a multitude of heterogeneous compute elements. Single nodes on supercomputers now comprise of traditional CPUs and multiple accelerators such as GPUs, Field Programmable Gate Arrays (FPGAs), and many-integrated-core devices (MICs). The development of high bandwidth interconnects between compute devices supports tight integration between multiple devices of different types on the same compute node.

The OpenCL programming language is designed to support modern HPC software engineers in writing code that executes on multiple hardware targets. The language provides support for individual *kernels*, portions of parallelisable codes that make up a HPC code base, to be executed independently on diverse hardware targets such as traditional CPUs, GPUs and FPGAs [11]. This gives HPC software developers greater flexibility by allowing codes aimed at a range of hardware targets to be written in a single programming language environment.

Application codes differ in resource requirements, control structure and available parallelism. Similarly, compute devices differ in number and capabilities of execution units, processing model, and available resources. These heterogeneous computing environments present opportunities for software engineers and HPC integrators to design highly optimised systems with multiple kernels executing on hardware targets best suited for the diverse computational tasks performed by these kernels [15]. However this opportunity raises the twin challenges of deciding on the right hardware target for complex kernels; and optimising codes to run on these diverse architectures. Our work is directed at helping developers tackle the latter of these two problems.

Modern computer architectures have suffered from the exponential growth in computational speeds being unmet

by proportional increases in memory speeds[6]. Memory accesses pose larger bottlenecks to performance as applications' demand for main memory scales with the arithmetic capability of computer systems. To mitigate this latency, modern CPU designs have employed a wide range of cache technologies to reduce main memory accesses using the principle of *spatial locality*: the idea that programs repeatedly access memory addresses in close locality. On the other hand, GPUs rely on hardware multithreading to hide memory latency, and their architectures favour ALU capability over sophisticated logic to manage a cache hierarchy and out-of-order execution. As a result, the performance of kernels on CPUs and GPUs alike is strongly dependent on memory access patterns intrinsic to the code.

Our aim in this paper is to develop a framework to guide HPC software engineers in hardware dependent code optimisation – specifically by guiding the improvement of codes' memory access patterns. We provide examples of manufacturer recommended code optimisations to improve memory access patterns on the target architecture, and examine these using AIWC [8], a state of the art architecture-independent code analysis tool for parallel workloads. Our work highlights the benefits and challenges arising from an architecture independent analysis of memory based program characteristics. We suggest the addition of two new metrics to AIWC to better characterise these memory-based optimisations. We measure the presented codes using the new metrics and discuss the metrics' effectiveness in capturing the essence of the optimisations performed. With these improvements, we show that AIWC is better suited to be used by HPC software engineers in guiding optimisation of their codes.

The structure of this paper is as follows. In section 2, we use the example of GPU matrix multiplication code to showcase the specific vendor recommended optimisations our work aims to measure. In section 3 we discuss how AIWC and its precursors profiled memory access patterns in an architecture independent fashion, and relevant architecture dependent approaches to memory access profiling. Then in section 4 we provide a methodology to critically examine AIWC, the current state of the art architecture independent workload characterisation tool. In section 5 we measure the accuracy of AIWC in profiling the impact of performance optimisations to various OpenCL codes. In section 6 we suggest new methods to accurately capture code patterns correlating to hardware specific memory optimisations. Finally, in section 8 we discuss further avenues to extend our work and conclude.

## 2 MOTIVATING EXAMPLE

We aim to capture the essence of vendor recommended optimisations for target architectures in our metrics. We demonstrate the optimisation strategies being analysed by presenting a simple unoptimised matrix multiplication kernel for input square matrices of order  $N$ , and then improve the memory access patterns of this kernel by incrementally performing optimisations recommended in the CUDA Optimisation Handbook [3] for NVIDIA GPUs. These incrementally optimised OpenCL codes are then analysed using AIWC to determine the accuracy in profiling favourable memory access patterns of the current framework and the proposed extensions to AIWC.

### Simple unoptimised matrix multiplication

The unoptimised matrix multiplication kernel presented in Appendix A is used as a baseline to validate the performance improvements measured from each following optimisation. Each thread of the kernel computes the  $(globalRow, globalCol)$  element of matrix  $C$  by reading the appropriate row and column from matrices  $A$  and  $B$  respectively.

### Using Shared Memory to Coalesce Global Memory Access to Matrix A

We first notice that the number of global memory accesses to matrices  $A$  and  $B$  increases at an order  $O(N^3)$  with respect to matrix size  $N$ . Global memory is typically located off-chip and accesses induce large delays. NVIDIA GPUs coalesce global memory loads and stores issued within thread-groups into as few DRAM transactions as possible. Multiple global memory loads and stores are coalesced into a single transaction when certain device specific conditions are met. On most NVIDIA GPUs, data accesses are coalesced when multiple requests are made for memory locations from the same cache-line in global memory [4]. Appendix B contains the `coalescedAMultiply` kernel, which coalesces accesses to matrix  $A$  by storing *tiles*, or square blocks, of  $A$ 's values into shared memory.

### Using Shared Memory to store Tiles of Matrix B

The code is further optimised by improving how the previous `coalescedAMultiply` kernel handles accesses to Matrix  $B$ . While each thread in `coalescedAMultiply` accesses only a single element of matrix  $A$  from global memory, each thread accesses a full column of matrix  $B$ . The repeated reads to elements of matrix  $B$  across multiple threads can be alleviated by reading tiles from matrix  $B$  into shared memory. Appendix C contains the `coalescedAB` kernel which performs this optimisation.

### Optimising handling of shared memory

NVIDIA shared memory is divided into multiple banks – stored in independent memory modules – to allow parallel accesses to shared memory. Bank conflicts occur when shared memory in the same bank is accessed concurrently. The code in `coalescedAB` kernel is further optimised by implicitly transposing tiles of Matrix *A* while loading from global memory. This improves memory bank utilisation during reads to shared memory tiles are performed during the necessary computation. The `coalescedABT` kernel demonstrates this optimisation by modifying lines 20,21 of `coalescedAB` to:

```
20   ASub[localCol][localRow] = A[tiledRow];
21   BSub[localRow][localCol] = B[tiledCol];
```

### Alignment of Memory Allocation

Memory access alignment is important to best utilise all parts of GPU memory architecture. Global memory buffer alignment can allow threads to access blocks of global memory aligned to the nearest cache line. This enables coalescing of memory accesses. If buffers are misaligned, parallel memory requests may cross over cache lines, and may double the number of slow global memory accesses needed as demonstrated in figures 1 and 2.

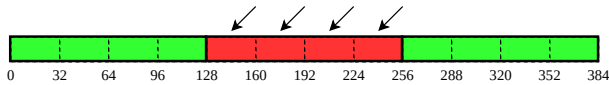


Figure 1: All threads access memory aligned to nearest cache line in parallel [3]

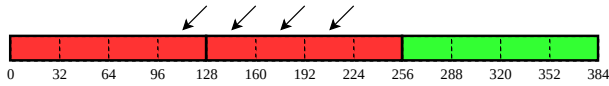


Figure 2: Unaligned sequential memory addresses fit in two cache lines [3]

A similar principle applies when using shared memory. Bank conflicts may be reduced by aligning allocations of shared memory buffers. The `alignedABT` kernel improves the alignment of shared memory tiles in `coalescedABT`. An arbitrary large alignment value of 4096 is chosen as it is larger than the size of modern hardware's cache lines and attributed to the local array declarations in the existing code as shown below.

```
1   __local float aTile[TILE_DIM][TILE_DIM]
   __attribute__((aligned(4096)));
2   __local float bTile[TILE_DIM][TILE_DIM]
   __attribute__((aligned(4096)));
```

All the examples above are an incomplete listing of optimisation strategies developers can perform to code targeted at NVIDIA GPUs. We analyse the correlations between the collected AIWC metrics for each of these kernels and our conceptual understanding of GPU memory optimisations. This allows us to examine how effectively our methodology uncovers underlying bottlenecks and guides optimisation efforts.

### 3 RELATED WORK

Hoste and Eeckhout [7] show that while conventional architecture dependent characteristics are useful in locating performance bottlenecks, they can hide the underlying, inherent program behaviour causing performance bottlenecks. A conceptual understanding of the performance characteristics of complex codes is necessary for the programmer to effectively optimise these codes. Architecture dependent characteristics typically include instructions per cycle (IPC), cache and branch prediction miss rates, page faults and DRAM bus data transfer rates. These are typically collected using hardware performance counters available on most target architectures. These performance counters do not serve to guide optimisation beyond highlighting potential bottlenecks [5, 7]. Further, in many cases, architecture dependent characteristics usually cannot be directly correlated to specific code patterns. For example, the causes of high cache miss rates in the execution of a program are too complex and widely variant on microarchitecture specific features such as cache size, prefetch behaviour and cache placement policies. In summary, we argue that a HPC developer tasked with optimising code for a given hardware target would benefit from architecture-independent metrics of the code that can be conceptually correlated to hardware specific optimisation patterns. Such architecture-independent metrics will effectively guide the HPC developer's workflow in both finding and fixing bottlenecks in code performance.

The Architecture Independent Workload Characterisation (AIWC) tool [8] relies on a set of instruction set architecture (ISA)-independent features determined by Shao and Brooks [14]. AIWC measures memory based metrics to characterise the target code's memory behaviours. AIWC firstly collects aggregate simple counts such as the (i) total memory footprint, the total number of unique addresses accessed; and (ii) 90% memory footprint, the number of unique addresses covering 90% of memory accesses. A small ratio of 90% memory footprint to total memory footprint correlates to programs

accessing the same small subset of memory addresses repeatedly – which can be linked to increased performance in a cached memory hierarchy.

AIWC also records the global memory address entropy (GMAE), a positive real number corresponding to the randomness of the memory access distribution of a program. To measure locality of memory accesses, AIWC collects the local memory address entropy (LMAE) of memory addresses accessed after dropping  $n$  least significant bits of all memory addresses accessed by the program. To calculate this, AIWC collects a frequency distribution of all non-register memory accesses by all threads in the target kernel. Using the collected frequency distribution, AIWC calculates 10 separate local memory address entropy (LMAE) values according to increasing number of least significant bits (LSB) skipped using the explicit formula for the  $n$ -bits skipped LMAE:

$$LMAE_{n-bits} = \sum_{a \in A_n} p_a \log_2(p_a^{-1}) \quad (1)$$

- $A_n$  is the set of all addresses accessed after skipping  $n$  LSBs of each address.
- $p_a := \frac{\#access_a}{\#access_{total}}$  is the probability (calculated as relative frequency) at which each memory address is accessed.

LMAE measures the locality of memory accesses performed over the full execution of a program. A steeper drop in entropy with increasing number of bits may correlate to more localised memory accesses over the program's execution.

Limitations of the memory footprint and local memory address entropy values as memory access pattern metrics are further discussed by this work.

### Advancements in Memory Access Pattern Characterisation

We provide a brief summary of past work in architecture independent program characterisation and Memory Access Pattern analysis:

- The Microarchitecture Independent Workload Characterisation Tool (MICA) [7] was the first microarchitecture independent workload characterisation tool for single threaded programs.
- The Workload ISA-Independent Characterization for Applications (WIICA) [14] extends MICA to present a framework to analyse single threaded programs independent of the ISA.
- CuMAPz: CuMAPz [12] is a CUDA memory access profiling tool and the first to present metrics for CUDA codes which can be generalised to any given NVIDIA GPU.

### MICA

The MICA framework was developed by Hoste and Eeckout [7] in response to their findings on the limitations of conventional microarchitecture dependent characteristics. Hoste and Eeckout discovered that performance counter based approaches to profiling codes often struggled in finding underlying program features that map to improved or worsened usage of performance critical hardware features of the target architecture. The MICA framework is a holistic characterisation tool, and thus collects features including instruction mix, instruction-level parallelism, register traffic, data stream strides and branch predictability.

Of these metrics, data stream strides are of particular interest in memory access pattern profiling. MICA's stride length metric measures the distance between consecutive memory accesses in a single threaded application. For CPU architectures running single threaded applications, this metric correlates to the spatial locality of memory accesses – a measure of how closely bunched are memory access in nearby times. This is directly correlated to cache reuse rates, critical to code performance on CPUs [2].

The MICA approach was tailored for single-threaded applications as the metrics collected rely heavily on Pin instrumentation [13]. As such, MICA is unsuited to analysing conventional supercomputing workloads with heavy use of parallelism.

### CuMAPz

Kim and Shrivastava [12] present CuMAPz, a CUDA memory access pattern analysis tool to guide NVIDIA GPU optimisations. CuMAPz focuses on the problem of improving CUDA application performance using NVIDIA memory-based optimisations. CuMAPz analyses CUDA codes structurally and simulates code execution on the memory hierarchy of specific NVIDIA GPU models.

During the simulated run of the target code, CuMAPz records all memory accesses in various buffers to simulate the global and shared memories on NVIDIA GPUs. Using this detailed simulation data, CuMAPz can estimate the performance critical (i) shared memory data reuse profit, (ii) profit from coalesced access (iii) memory channel skew cost and (iv) bank conflict cost characteristics of the target code.

The simulation environment described in CuMAPz and the attached analysis framework is highly specific to CUDA enabled GPUs. Replicating the CuMAPz framework for all target architectures is challenging. However, CuMAPz is an interesting simulator from the standpoint of this paper's work since it adheres to the core parts of NVIDIA GPUs' memory models in its analysis, while allowing the user to specify their GPU model specific hardware information.

Our approach is an architecture independent analysis of memory access patterns that provides metrics correlating to similar performance critical memory access optimisations as CuMAPz. We aim to further the state of the art by providing a framework to guide developers in optimising OpenCL codes for any given target architecture. To the best of our knowledge, none of the previous works present a set of performance metrics that accurately characterise memory access patterns of parallel applications independent of the target architecture.

#### 4 METHODOLOGY

To provide memory access pattern metrics that represent vendor recommended optimisations on GPUs, we improved AIWC by adding a new metric: relative local memory usage. This measures the proportion of all memory accesses from the symbolic execution of the kernel that occurred to memory allocated as `__local`. On GPUs, this memory address space is mapped to fast on-chip shared memory.

Relative local memory usage is an example of a metric that is useful to measure performance critical access patterns on some architectures such as GPUs, and not others, such as CPUs. CPUs do not typically have a notion of user controlled on-chip memory shared between hardware threads such as NVIDIA GPUs' shared memory. This is a natural consequence of programming for a heterogeneous system. Specific code patterns may translate to performance improvements only on certain hardware.

In the original AIWC tool [10], global and local memory address entropy (MAE) were calculated using physical addresses of memory used by the Oclgrind simulator back-end of AIWC. This caused irregularities in entropy calculations across multiple runs of the same simulation. We improved the calculation of memory address entropy by using *virtual addresses* to calculate MAE values using an abstract ideal address space on which all memory accesses by the kernel occur. This allows AIWC to accurately abstract over the hardware and ISA-specific differences in memory layouts across the diverse hardware targets.

#### 5 RESULTS

Figure 3 shows that across varying problem sizes, the vendor recommended optimisations to the matrix multiplication code lead to increased performance. Note that a matrix size of 80 is small – overheads attached to optimisation techniques may be causing the observed decrease in performance as some optimisations are performed.

Table 1 summarises AIWC memory metrics collected for each of the matrix multiply kernels in section 2. Note that only two LMAE values are shown for brevity. We now analyse the effectiveness of AIWC metrics in profiling the NVIDIA recommended memory optimisations applied to the matrix multiplication kernel.

*Relative local memory usage:* As reliance on NVIDIA GPUs' shared memory increases in each kernel from `simpleMultiply` to `coalescedAB`, we find that the ratio of OpenCL local memory usage increases as expected.

*Global and local MAE:* Entropy measurements decrease from `simpleMultiply` to `coalescedAB`. This is explained by the optimisations performed incrementally reducing accesses to matrix *A* and *B*, and instead performing the bulk of computations on smaller tiles in on-chip shared memory. We observe an almost completely uniform distribution of memory accesses in `simpleMultiply`, where the program makes *N* loads to each element of *A* and *B* with *N* the dimension of the matrices. The frequency distribution of memory addresses accessed become increasingly non-uniform as we perform less accesses to matrices *A* and *B* and offset this by increasing the frequency of accesses to smaller, more localised shared memory buffers. The non-uniformity of relative frequency with which each memory cell is accessed by the program translates directly to decreases in local and global memory entropy values as reliance on small shared memory buffers increases from `simpleMultiply` to `coalescedAB`.

*Memory Footprint:* Similar to trends in global and local MAE, we find that the ratio of 90% memory footprint to total memory footprint decreases from 60.12% for `simpleMultiply` to 0.25% (`coalescedAB`). Increased utilisation of shared memory in the optimised kernels means that the shared memory buffers make up a greater proportion of total memory accesses in the program. As the shared memory buffers are small and reused within a workgroup, the memory footprint of the shared memory buffers is also smaller.

AIWC's metrics strongly reward optimisations that tend to localise memory accesses. Shared memory buffers are typically smaller than global memory arrays when programming for GPUs due to hardware limitations on sizes of shared memory buffers [4]. However, the metrics currently measured by AIWC do not have a direct causal relation to code patterns that optimise memory accesses on GPUs. The proposed relative local memory usage metric is the first to correspond to a recommended optimisation strategy of using fast on-chip shared memory. Further, we find that all current AIWC metrics do not measure any sizeable difference between `coalescedAB`, `coalescedABT` and `alignedABT` codes. We address the root cause of this – a lack of temporal information about memory accesses, in the next section.

#### 6 DISCUSSION

AIWC metrics are inherently lossy. Given the set of metrics calculated for an unknown kernel, we can not reconstruct the kernel based on these metrics. Specifically to memory access pattern analysis, the calculation of memory address entropy of a kernel relies only on the frequency distribution

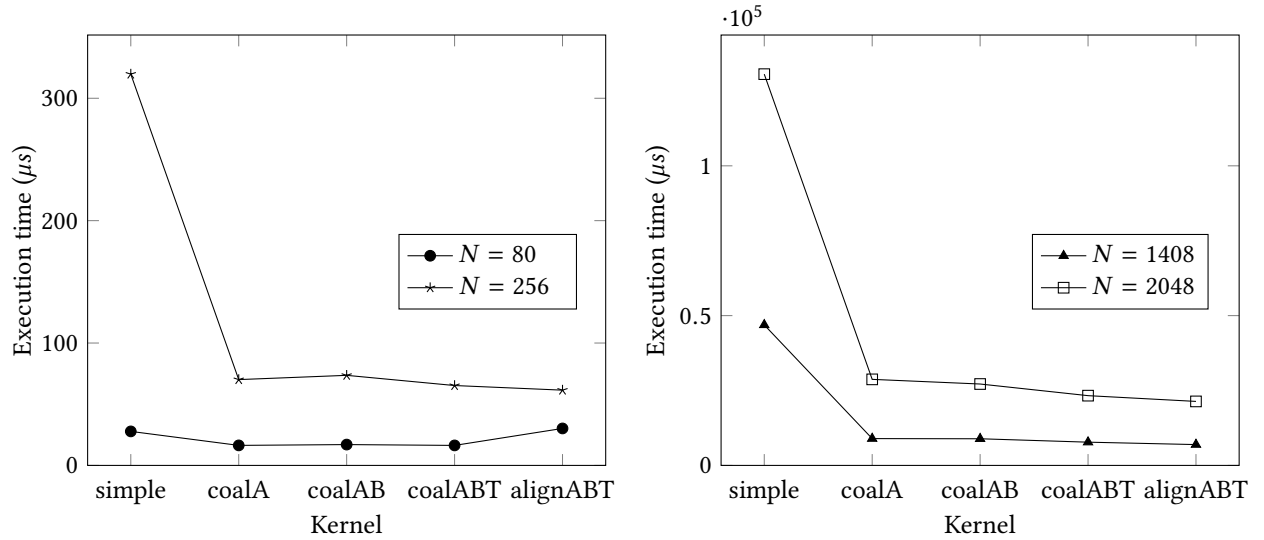


Figure 3: NVIDIA Tesla P100 Runtime performance of section 2 codes averaged over 100 runs

	simple	coalescedA	coalescedAB	coalescedABT	alignedABT
Total memory footprint	196608	196608	196608	196608	196608
90% Memory Footprint	118196	56176	489	489	489
Global MAE	17.02	13.18	9.78	9.78	9.78
LMAE #bits=3	16.02	12.18	8.78	8.78	8.78
LMAE #bits=10	9.02	5.18	1.78	1.78	1.78
Relative Local Memory Usage	0	49.9083	94.28	94.28	94.28

Table 1: Selection of AIWC[8] metrics for  $256 \times 256$  matrix multiplication

of memory accesses to all addresses accessed by the kernel. We observe that calculation of memory address entropy does not make use of temporal information. The order of sequential memory accesses performed by each thread, as well as addresses requested in parallel by multiple threads in an OpenCL thread group, are both vital in accurately characterising parallel codes.

We propose a new architecture independent metric to measure memory access patterns of parallel programs. The proposed metric is inspired by CuMAPz’ direct approaches to measuring optimisation specific characteristics of CUDA codes.

AIWC currently collects a list of all memory accessed by each thread of execution. In the OpenCL programming model, threads within thread groups execute the same code and are allowed to cooperate on *local memory* addresses. We can group together threads by their work groups to align histories of memory accesses of threads in a group to analyse memory accesses performed by thread groups at each logical time step in the symbolic execution of the code. We argue

that analysing the accesses occurring at the same logical time step is an accurate, conceptually sound method of predicting the extent of memory access coalescing and bank conflicts we are likely to find upon executing the code on a GPU.

The precise definition of the proposed metric is provided in the following section.

### A Parallel Spatial Locality Metric

There are three steps involved in generating an AIWC metric: *recording*, *calculating* and *summarising* data collected from the symbolic execution of the kernel under inspection.

*Record*: we first record memory accesses performed by each thread in an OpenCL thread group as described above to achieve a global ordering of all memory accesses performed in a thread group. This ordering is collected in the form of logical timestamps ( $t_0..t_{last}$ ) at which memory accesses occur.

*Calculate*: for each timestamp  $t = t_0..t_{last}$ , calculate the n-bits dropped entropy of memory addresses accessed by all

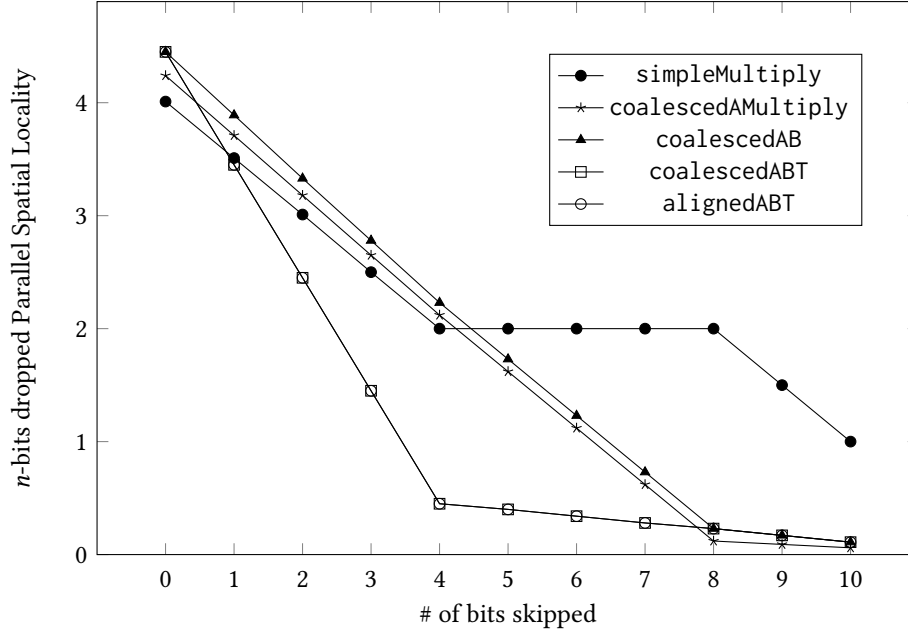


Figure 4: Calculated parallel spatial locality metric for matrix multiply kernels for  $256 \times 256$  matrix multiplication

threads in a work group within the timestamp  $t$ . Here  $n$  can range between 1 and 10 as was the case for *LMAE*.

*Summarise:* average the collected entropy values across all the timestamps to calculate the parallel spatial locality metrics for one thread group. We then average the  $n$ -bits dropped entropy summaries across thread groups to obtain the  $n$ -bits dropped parallel spatial locality metrics for the kernel’s execution.

The proposed metric is a parallel computing analogue for MICA’s data stride metric that measures the distance between consecutive data accesses in a single threaded environment. In parallel programs, to accurately measure spatial locality of accesses, we must consider memory accesses performed by multiple threads in a close temporal scope. The proposed metric calculates the locality of accesses in each time step of the program’s execution and steeper drop-offs in  $n$ -bits dropped parallel spatial locality scores will be observed in programs that access nearby memory addresses within the same timestamp. Such programs will perform better on GPUs, as they will make better use of both global memory access coalescing and shared memory bank structures.

In figure 4 we see theoretical calculations for the proposed parallel spatial locality metric for each of the matrix multiplication kernels from section 2. In particular we observe that the coalescedABT and alignedABT kernels have the steepest drop-offs in entropy as the number of bits skipped is increased, which correlates to better locality of parallel

memory accesses. It is expected for these kernels to exhibit better parallel spatial locality than simpleMultiply, as coalescedABT and alignedABT make use of shared memory, where accesses tend to be localised simply due to the small size of shared on-chip memory typically available on GPUs. Further we find that the proposed metric successfully distinguishes between the coalescedAB and coalescedABT kernels. It accurately depicts a steeper drop-off for the more optimised coalescedABT kernel, where a larger proportion of parallel memory accesses make better use of the memory bank structure of GPU shared memory than all previous kernels. This is a significant improvement over the state-of-the-art AIWC metrics in characterising how codes localise shared memory accesses to better use the hardware provided.

## 7 RESULTS

We present the results of running the AIWC tool on the Extended OpenDwarfs benchmark suite [1, 9].

### N-body methods: GEM

#### Dense Linear Algebra: LUD

Lower-upper decomposition (LUD) in OpenDwarfs is a program to decompose an input square matrix as the product of one lower and one upper diagonal matrix. LUD is a Memory access patterns in a dense linear algebra workload such as LUD are typically highly regular and deterministic for each OpenCL work item, based on the the matrix dimension and offset parameters.



The OpenDwarfs implementation [1] splits the LUD computation into three kernels, ...

### Structured Grids: SRAD

Speckle Reducing Anisotropic Diffusion (SRAD) attempts to remove locally correlated noise from images by following a repeated, structured grid update computation pattern. Conditional statements in the code cause thread divergence, potentially within a work-group, to handle boundary conditions. These boundaries constitute a small portion of the executed work-items, especially on larger data-sets and so the .

### Graph Traversal: BFS

Graph traversal algorithms require pointer chasing operations to traverse nodes of a graph to perform calculations. The Breadth First Search

## 8 CONCLUSIONS AND FUTURE WORK

To the best of our knowledge this work is the first to critically examine architecture independent methods to measure memory access patterns and guide hardware-specific optimisation. We implemented and justified the addition of relative local memory usage to AIWC in our steps to characterise memory-based GPU code optimisations. We have also proposed the methodology to implement a new parallel spatial locality metric to AIWC. Upon implementation, our work would be the first to measure memory access patterns of parallel codes in an architecture-independent, easily interpreted manner.

Our proposed parallel spatial locality metric may also correlate to some memory-based optimisation strategies for CPUs. Future work would apply the approach followed by this paper to CPU and FPGA architectures to evaluate the viability of an architecture independent characterisation of memory access patterns in codes targeted to these architectures.

Future work will provide a concrete implementation of this new parallel spatial locality metric in the AIWC framework. It is then feasible to test these new metrics across a larger set of GPU targeted OpenCL codes. This will allow a critical examination of the effectiveness of both proposed metrics in accurately profiling memory access patterns of these diverse codes.

## REFERENCES

- [1] OpenDwarfs (base version). <https://github.com/vtsynergy/OpenDwarfs/commit/31c099aff5343e93ba9e8c3cd42bee5ec536aa93>, Feb 2017.
- [2] Intel Corporation. Intel® 64 and ia-32 architectures optimization reference manual. 2016.
- [3] NVIDIA Corporation. Cuda c best practices guide. 2019.
- [4] NVIDIA Corporation. Cuda c programming guide. 2019.
- [5] Karthik Ganesan, Lizy John, Valentina Salapura, and James Sexton. A performance counter based workload characterization on Blue Gene/P. In *International Conference on Parallel Processing (ICPP)*, pages 330–337. IEEE, 2008.
- [6] John L. Hennessy and David A. Patterson. *Computer Architecture - A Quantitative Approach, 5th Edition*. Morgan Kaufmann, 2012.
- [7] Kenneth Hoste and Lieven Eeckhout. Microarchitecture-independent workload characterization. *IEEE Micro*, 27(3), 2007.
- [8] Beau Johnston and Josh Milthorpe. AIWC: opengl based architecture independent workload characterisation. *CoRR*, abs/1805.04207, 2018.
- [9] Beau Johnston and Josh Milthorpe. Dwarfs on accelerators: Enhancing opengl benchmarking for heterogeneous computing architectures. In *The 47th International Conference on Parallel Processing, ICPP 2018, Workshop Proceedings, Eugene, OR, USA, August 13-16, 2018*, pages 4:1–4:10. ACM, 2018.
- [10] Beau Johnston, James Price, Moritz Pflanzner, Petros Kalos, Tom Deakin, Nido Media, and Daniel Saier. BeauJoh/Oclgrind: Adding AIWC – An Architecture Independent Workload Characterisation Plugin. <https://doi.org/10.5281/zenodo.1134175>, December 2017.
- [11] Khronos OpenCL Working Group. *The OpenCL Specification, Version 1.1*, 2011.
- [12] Yooseong Kim and Aviral Shrivastava. Cumapz: a tool to analyze memory access patterns in CUDA. In Leon Stok, Nikil D. Dutt, and Soha Hassoun, editors, *Proceedings of the 48th Design Automation Conference, DAC 2011, San Diego, California, USA, June 5-10, 2011*, pages 128–133. ACM, 2011.
- [13] Chi-Keung Luk, Robert Cohn, Robert Muth, Harish Patil, Artur Klauser, Geoff Lowney, Steven Wallace, Vijay Janapa Reddi, and Kim Hazelwood. Pin: building customized program analysis tools with dynamic instrumentation. In *ACM SIGPLAN notices*, volume 40, pages 190–200. ACM, 2005.
- [14] Yakun Sophia Shao and David Brooks. Isa-independent workload characterization and its implications for specialized architectures. In *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pages 245–255. IEEE, 2013.
- [15] Kyle Spafford, Jeremy Meredith, and Jeffrey Vetter. Maestro: data orchestration and tuning for OpenCL devices. *Euro-Par 2010-Parallel Processing*, pages 275–286, 2010.

## A SIMPLEMULTIPLY KERNEL

```

1  __kernel void simpleMultiply(__global float *A,
2  __global float *B,
3  __global float *C,
4  int N)
5  {
6  const int globalRow = get_global_id(0); //
7  const int globalCol = get_global_id(1); //
8  // Compute a single element of C (loop over
9  float acc = 0.0f;
10 for (int k = 0; k < N; ++k) {
11     acc += B[k * N + globalCol] * A[globalRow
12         * N + k];
13 }
14 // Store the result
    C[globalRow * N + globalCol] = acc;

```



---

15       }

## B COALESCEDMULTIPLY KERNEL

---

```

1  __kernel void coalescedAMultiply(
2      const __global float* A,
3      const __global float* B,
4      __global float* C,
5      const int N)
6  {
7      __local float aTile[TILE_DIM][TILE_DIM];
8
9      const int localRow = get_local_id(0);
10     const int localCol = get_local_id(1);
11
12     const int globalRow = get_global_id(0);
13     const int globalCol = get_global_id(1);
14
15     __private float sum = 0.0f;
16
17     const int numTiles = N / TILE_DIM;
18     __private const int tiledRow = globalRow*N+
19         localCol;
20     for (int i = 0; i < numTiles; i++) {
21         aTile[localRow][localCol] =
22             A[tiledRow+i*TILE_DIM];
23         barrier(CLK_LOCAL_MEM_FENCE);
24         for (int k = 0; k < TILE_DIM; k++) {
25             sum += aTile[localRow][k] *
26                 B[(i*TILE_DIM+k)*N+globalCol];
27         }
28         barrier(CLK_LOCAL_MEM_FENCE);
29     }
30     C[globalRow*N+globalCol] = sum;
31 }

```

---

## C COALESCEDEDAB KERNEL

---

```

1  __kernel void coalescedAB(
2      const __global float* A,
3      const __global float* B,
4      __global float* C,
5      const int N) {
6      __local float ASub[TILE_DIM][TILE_DIM];
7      __local float BSub[TILE_DIM][TILE_DIM];
8
9      const int localRow = get_local_id(0);
10     const int localCol = get_local_id(1);
11     const int globalRow = get_global_id(0);
12     const int globalCol = get_global_id(1);
13
14     float acc = 0.0f;
15     const int numTiles = N/TILE_DIM;
16

```

```

17     for (int i = 0; i < numTiles; i++) {
18         const int tiledRow =
19             globalRow*N+i*TILE_DIM + localCol;
20         const int tiledCol = globalCol +
21             (TILE_DIM*i + localRow)*N;
22         ASub[localRow][localCol] = A[tiledRow];
23         BSub[localRow][localCol] = B[tiledCol];
24
25         barrier(CLK_LOCAL_MEM_FENCE);
26
27         for (int k=0; k<TILE_DIM; k++) {
28             acc += ASub[localRow][k] *
29                 BSub[k][localCol];
30         }
31         barrier(CLK_LOCAL_MEM_FENCE);
32     }
33     C[globalRow*N + globalCol] = acc;
34 }

```

---