Smart Fusion Evaluation Kit

Actel Fusion2 based FPGA Evaluation Kit

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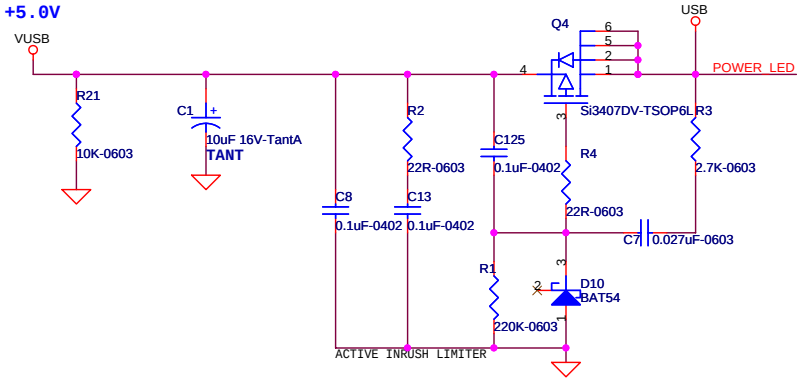
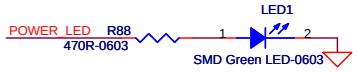
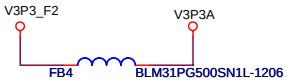
Rev B Schematics: DVP-100-000290-001
Rev B Layout: DVP-101-000290-001
Rev B Gerber and Assy Files: DVP-102-000290-001
Rev B BOM: DVP-103-000290-001

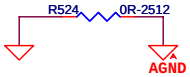
Originated By Deepali Gupta	*Copyright©2009 System Level Solutions, Inc. All rights reserved.*
Designed By Bhavesh Desai	**Schematic** sch_00_Top Cover Page
Verified By Deepali Gupta, Bhavesh Desai	**Title** Smart Fusion Evaluation Kit
Customer Actel Corporation	**Size** A; **Document Number** Actel P/N: DVP-100-000290-001 SCH-SMFSNEVK-0940-B1B; **Rev** B
Customer P/N DVP-100-000290-001	**Date:** Tuesday, December 29, 2009 **Sheet** 1 **of** 15

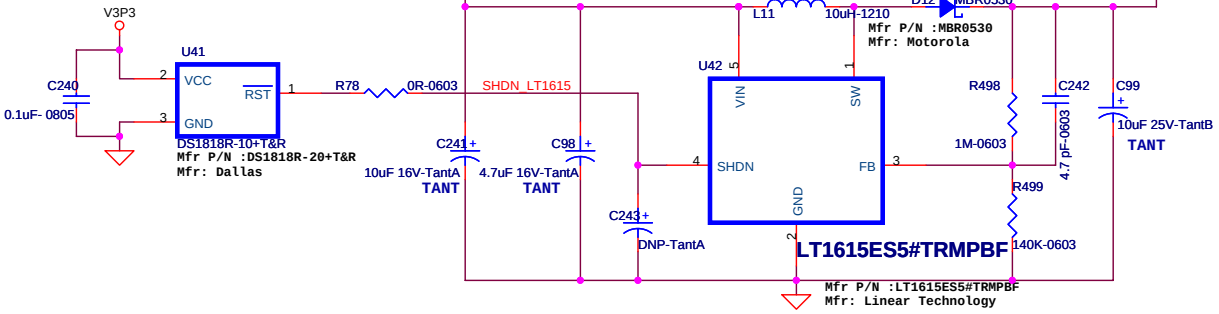
USB ACTIVE IN RUSH LIMITER



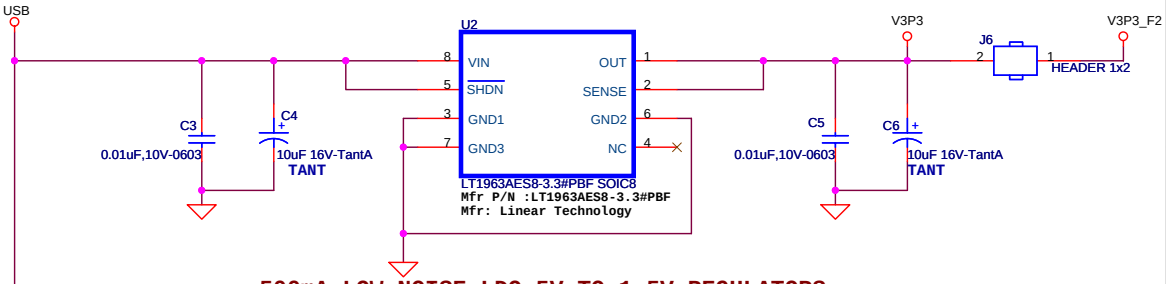




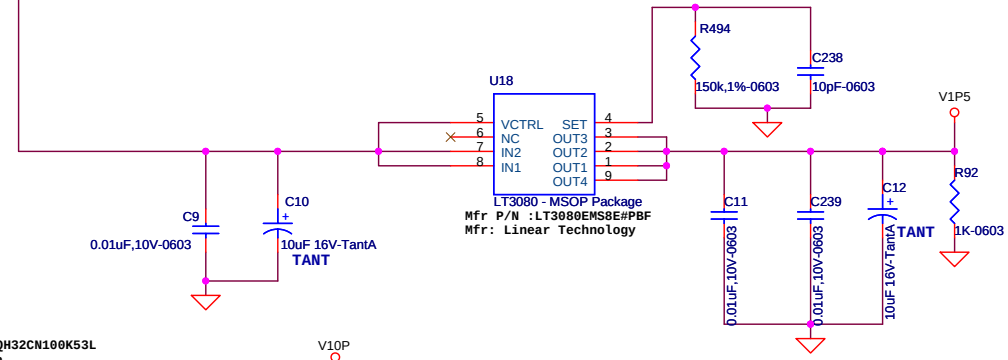


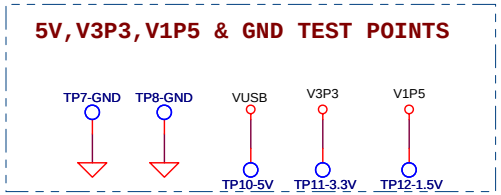


1.5A LOW NOISE 5V TO 3.3V REGULATORS



500mA LOW NOISE LDO 5V TO 1.5V REGULATORS





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Schematic	sch_00_Top	Power Supply	
Title	Smart Fusion Evaluation Kit		
Size: Custom	Document Number: SCH-SMFSNEVK-0940-B1B		Rev: B
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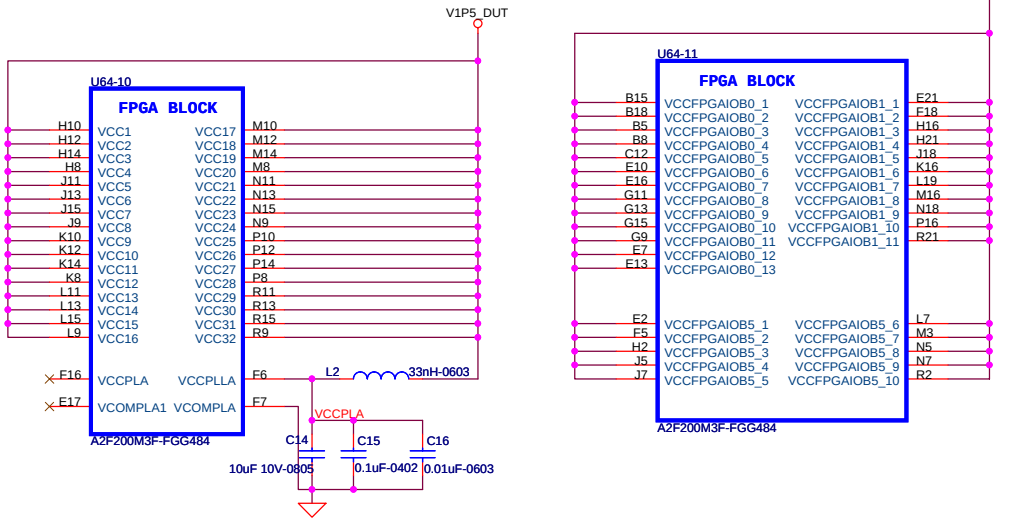
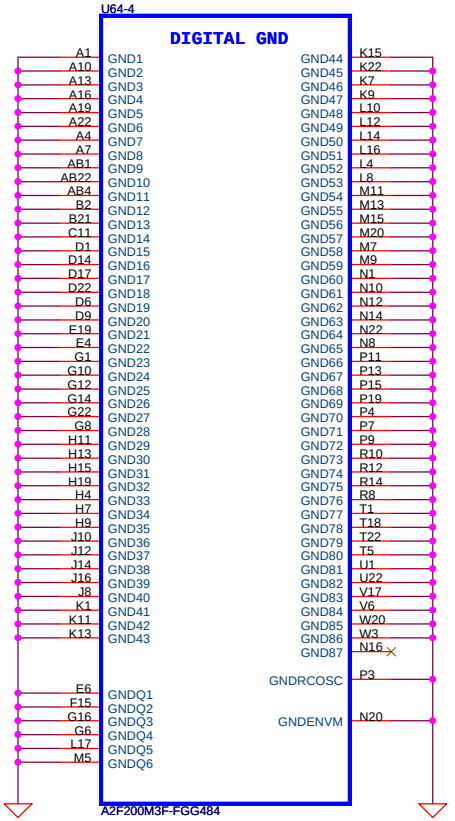
DIGITAL PWR & GND

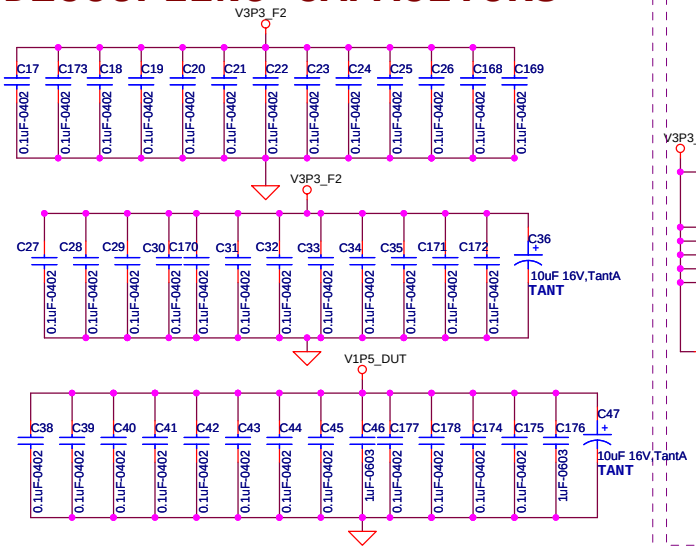
FPGA BLOCK POWER SUPPLY



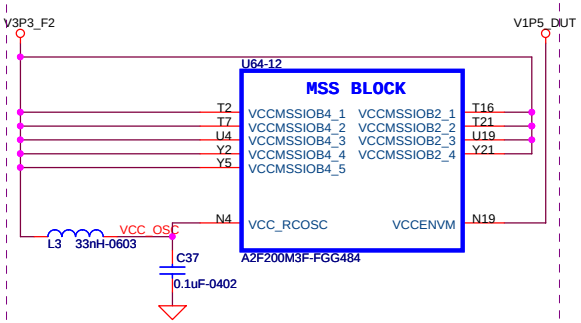
DIGITAL GROUND



DECOUPLING CAPACITORS



MSS BLOCK POWER SUPPLY



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Schematic	sch_00_Top	Digital Power & GND
Title	Smart Fusion Evaluation Kit	
Size B	Document Number SCH-SMFSNEVK-0940-B1B	Rev B
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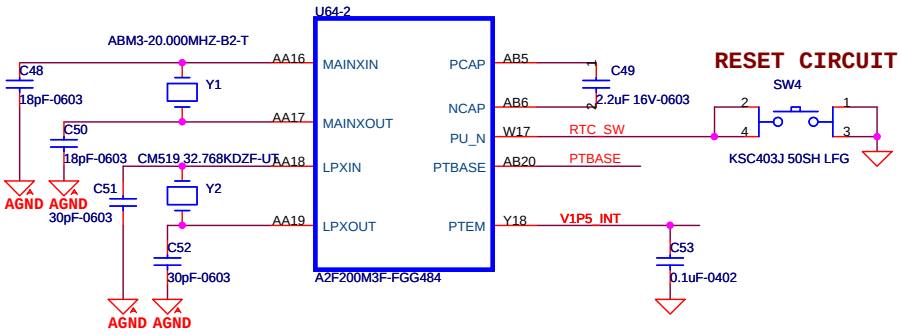
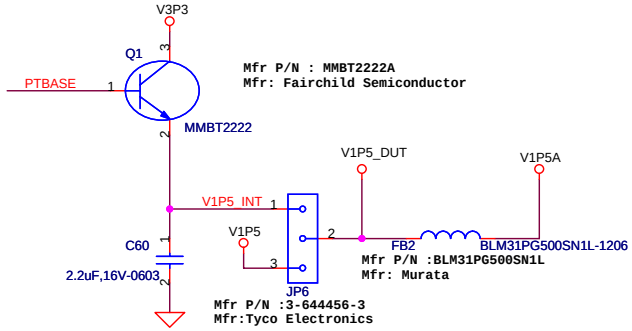
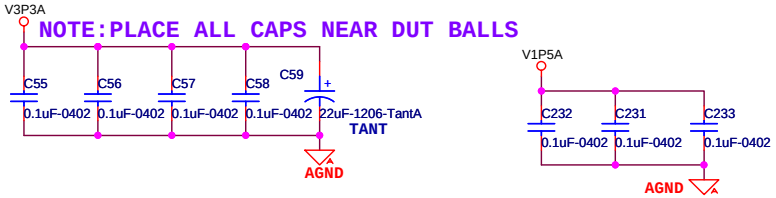
ANALOG SIGNAL PWR & GND

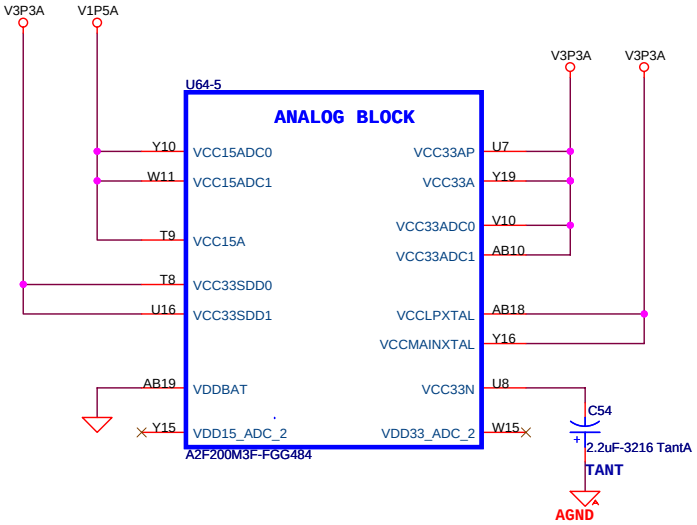
ANALOG BLOCK



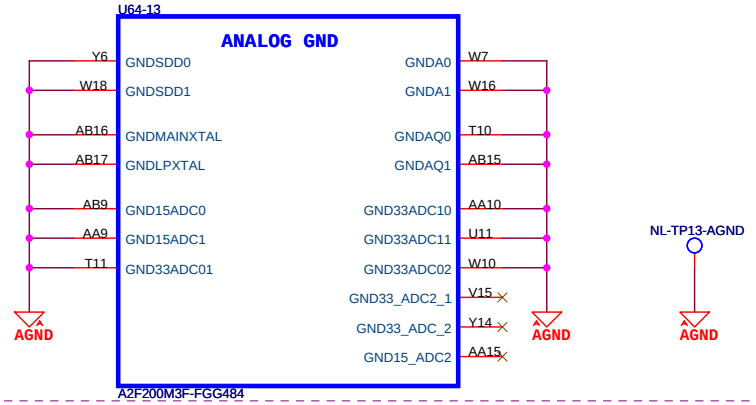




ANALOG POWER SUPPLY



ANALOG GROUND



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Schematic	sch_00_Top	Analog Power	
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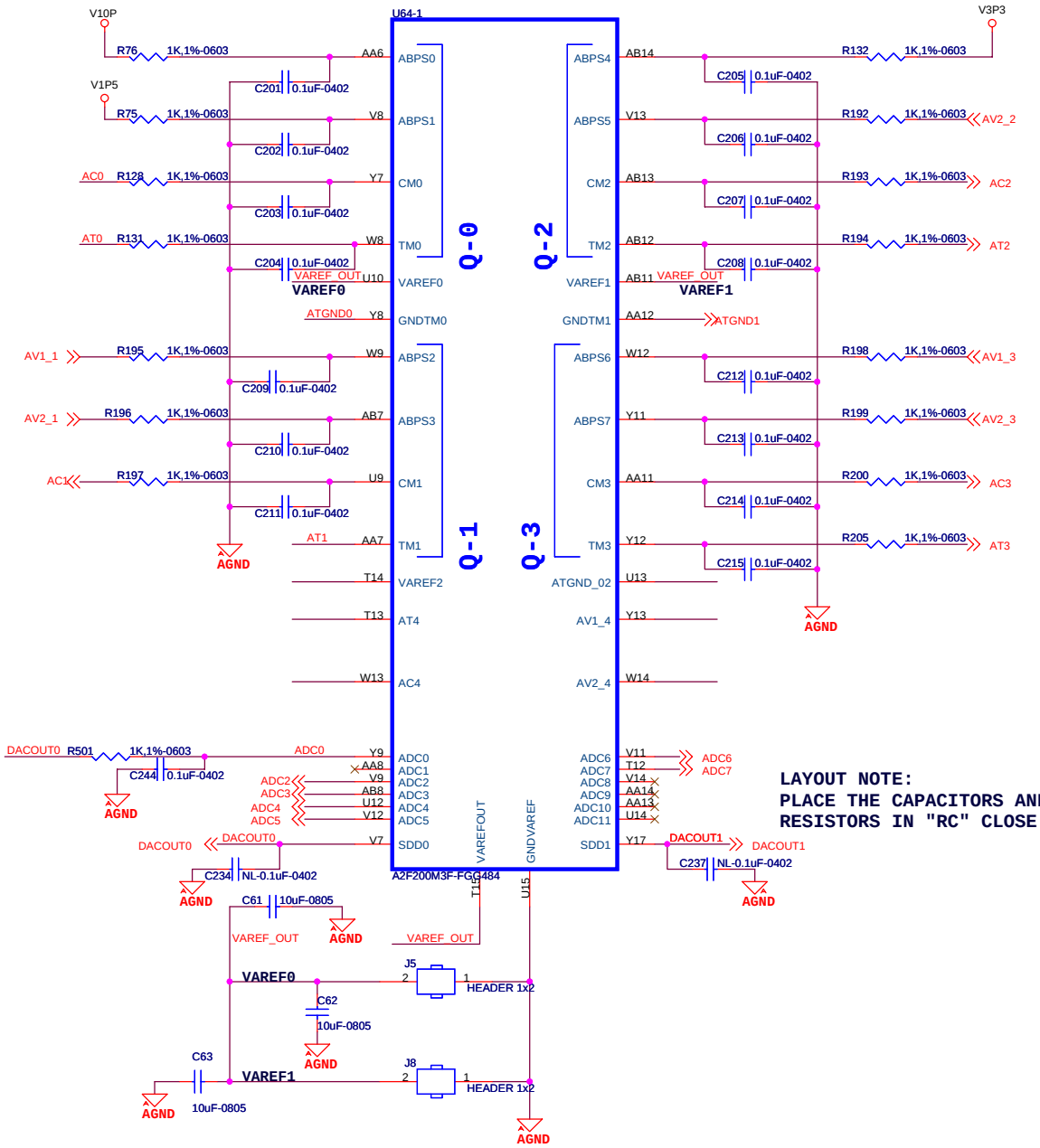
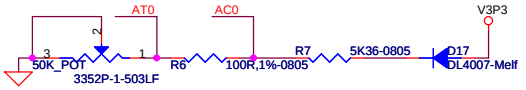
Size: Custom	Document Number: SCH-SMFSNEVK-0940-B1B		Rev: B
Date: Monday, January 04, 2010	Sheet 4 of 15		

ANALOG SIGNAL



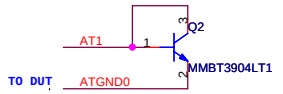
LAYOUT NOTE:
PLACE THE CAPACITORS AND
RESISTORS IN "RC" CLOSE TO FPGA PIN

CURRENT MONITORING



Mfr P/N : 3352P-1-503LF
Mfr: Bourns Inc.

TEMP DIODE



Mfr P/N :MMBT3904LT1
Mfr:Infineon Technologies

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Schematic	sch_00_Top	Analog Signal	
Title	Smart Fusion Evaluation Kit		
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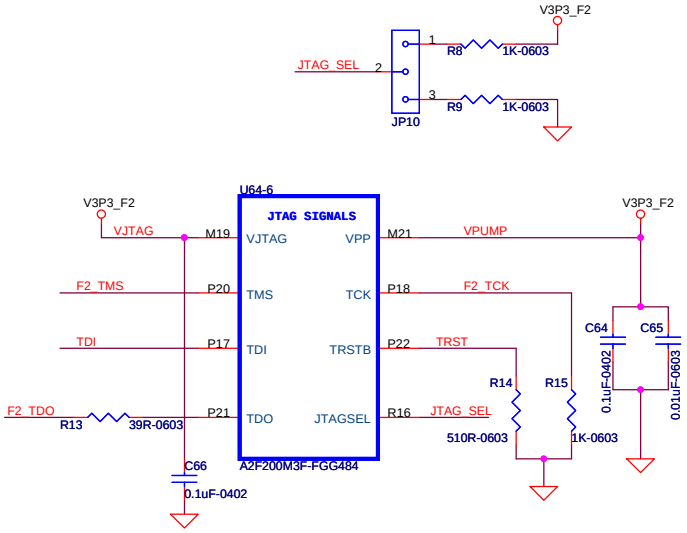
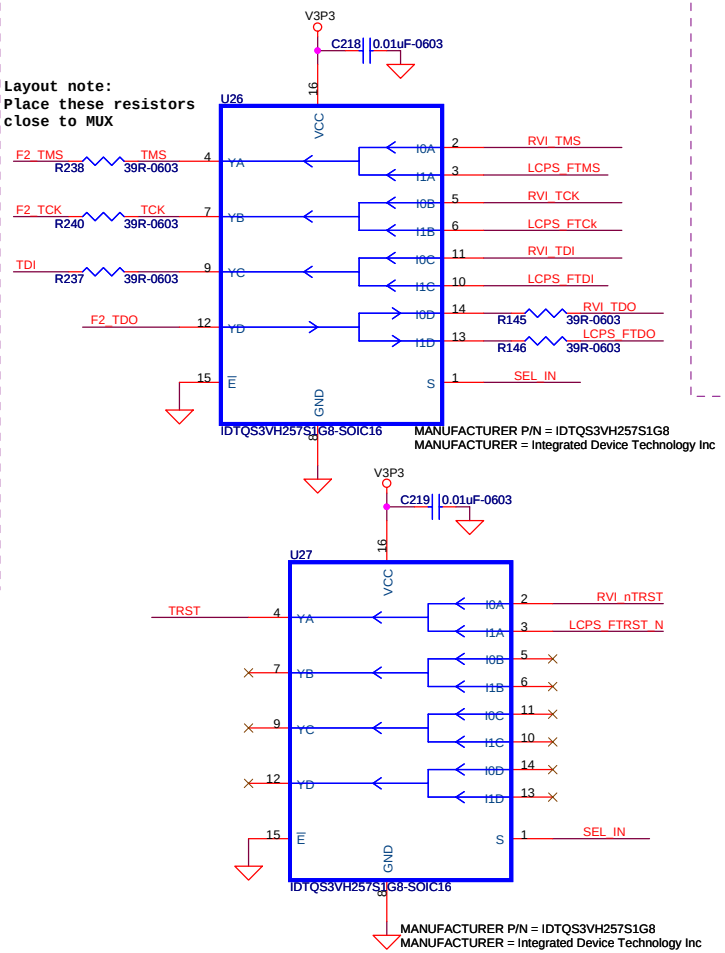
JTAG CHAIN PROGRAMMING

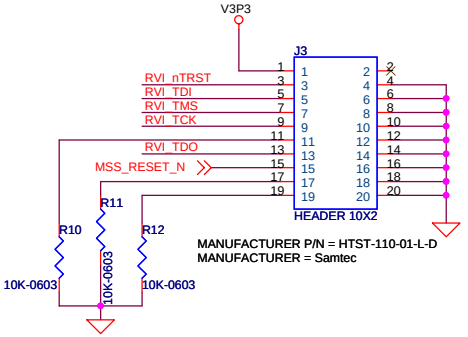
F2 JTAG



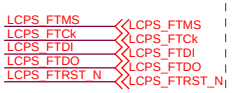
2:1 MUX/DEMUX



RVI HEADER

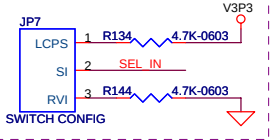


LCPS JTAG Signals



INPUT SELECTING OPTION

JTAG Config for MUX	Shunt b/w JP7 pins	
LCPS	1	2
RVI	2	3



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Schematic	sch_00_Top	JTAG CHAIN PROGRAMMING	
Title	Smart Fusion Evaluation Kit		
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NO Connects

U64-20

K17	E11	W2_P	M6
J17	E12	W1_N	N6
F21	E23	W4_P	P2
F20	E24	W3_N	P1
G18	E33	W6_P	N2
G17	E34	W5_N	N3
E18	E35	W8_P	M1
F17	E36	W7_N	M2
		W10_P	L3
		W9_N	M4
D7	N1	W12_P	L1
E8	N2	W11_N	L2
C4	N3	W14_P	K4
C5	N4	W13_N	L5
B3	N5		
B4	N6		
D8	N9	W15	L6
C7	N10	W16	K6
C8	N11	SPARE1	T19
B7	N12	SPARE2	T20
A17	N35	SPARE3	R20
A18	N36		

A2F200M3F-FGG484

U64-8

SRAM INTERFACE

A8	EMC_AB[0]/IO04NDB0V0	EMC_DB[0]/GEA2/IO59NDB5V0	K2
A9	EMC_AB[1]/IO04PDB0V0	EMC_DB[1]/GEB2/IO59PDB5V0	K3
B10	EMC_AB[2]/IO05NDB0V0	EMC_DB[2]/IO60NPB5V0	K5
B11	EMC_AB[3]/IO05PDB0V0	EMC_DB[3]/GEC2/IO60PPB5V0	J4
E11	EMC_AB[4]/IO06NDB0V0	EMC_DB[4]/GEA0/IO61NDB5V0	J3
E12	EMC_AB[5]/IO06PDB0V0	EMC_DB[5]/GEA1/IO61PDB5V0	J2
B12	EMC_AB[6]/IO07NDB0V0	EMC_DB[6]/GEB0/IO62NDB5V0	J1
A12	EMC_AB[7]/IO07PDB0V0	EMC_DB[7]/GEB1/IO62PDB5V0	H1
C13	EMC_AB[8]/IO08NDB0V0	EMC_DB[8]/GEC0/IO63NDB5V0	H3
D13	EMC_AB[9]/IO08PDB0V0	EMC_DB[9]/GEC1/IO63PDB5V0	G3
D11	EMC_AB[10]/IO09NDB0V0	EMC_DB[10]/IO69NPB5V0	F4
D12	EMC_AB[11]/IO09PDB0V0	EMC_DB[11]/IO69PPB5V0	G5
A14	EMC_AB[12]/IO10NDB0V0	EMC_DB[12]/IO70NDB5V0	D2
A15	EMC_AB[13]/IO10PDB0V0	EMC_DB[13]/GAC2/IO70PDB5V0	D3
B13	EMC_AB[14]/IO11NDB0V0	EMC_DB[14]/GAB2/IO71NDB5V0	C1
B14	EMC_AB[15]/IO11PDB0V0	EMC_DB[15]/GAA2/IO71PDB5V0	B1
C14	EMC_AB[16]/IO12NDB0V0		
C15	EMC_AB[17]/IO12PDB0V0	EMC_OEN0_N/IO03NDB0V0	D10
B16	EMC_AB[18]/IO13NDB0V0	EMC_OEN1_N/IO03PDB0V0	C10
B17	EMC_AB[19]/IO13PDB0V0	EMC_BYTEN[0]/GAC0/IO02NDB0V0	B9
F13	EMC_AB[20]/IO14NDB0V0	EMC_BYTEN[1]/GAC1/IO02PDB0V0	C9
F14	EMC_AB[21]/IO14PDB0V0	EMC_CS0_N/GAB0/IO01NDB0V0	A5
C17	EMC_AB[22]/IO15NDB0V0	EMC_CS1_N/GAB1/IO01PDB0V0	A6
C18	EMC_AB[23]/IO15PDB0V0	EMC_RW_N/GAA1/IO00PDB0V0	B6
C16	EMC_AB[24]/IO16NDB0V0	EMC_CLK/GAA0/IO00NDB0V0	C6
D16	EMC_AB[25]/IO16PDB0V0		

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U64-19

CAN SIGNALS

L21	GDB0/IO30NDB1V0	GDC2/IO32PDB1V0	L22
M22	IO32NDB1V0	GDB2/IO33PDB1V0	M18

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U64-7

NC PINS

A11	NC1	NC22	F12
A2	NC2	NC23	F8
A20	NC3	NC24	F9
A21	NC4	NC25	G7
A3	NC5	NC26	M17
AA20	NC6	NC27	N17
AA21	NC7	NC28	N21
AB21	NC8	NC29	P5
C2	NC9	NC30	P6
C20	NC10	NC31	R17
C3	NC11	NC32	R18
D19	NC12	NC33	R19
D20	NC13	NC34	R22
D4	NC14	NC35	R4
D5	NC15	NC36	R5
E15	NC16	NC37	R6
E20	NC17	NC38	R7
E5	NC18	NC39	U6
E9	NC19	NC40	V16
F10	NC20	NC41	W6
F11	NC21		

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U64-18

UART HANDSHAKING

PORT1

L18	GDA2/IO33NDB1V0	UART_1_TXD/GPIO_28	V20
L20	GDB1/IO30PDB1V0	UART_1_RXD/GPIO_29	W22

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U65-22

G2	GFB0/IO65NPB5V0
K20	GDC1/IO29PDB1V0
K21	GDC0/IO29NDB1V0
D18	GBA1/IO19PPB0V0
H18	GCC2/IO25PDB1V0
K18	GDA1/IO31PDB1V0

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Schematic	sch_00_Top	Memory	
Title	Smart Fusion Evaluation Kit		
Size: Custom	Document Number: SCH-SMFSNEVK-0940-B1B		Rev: B
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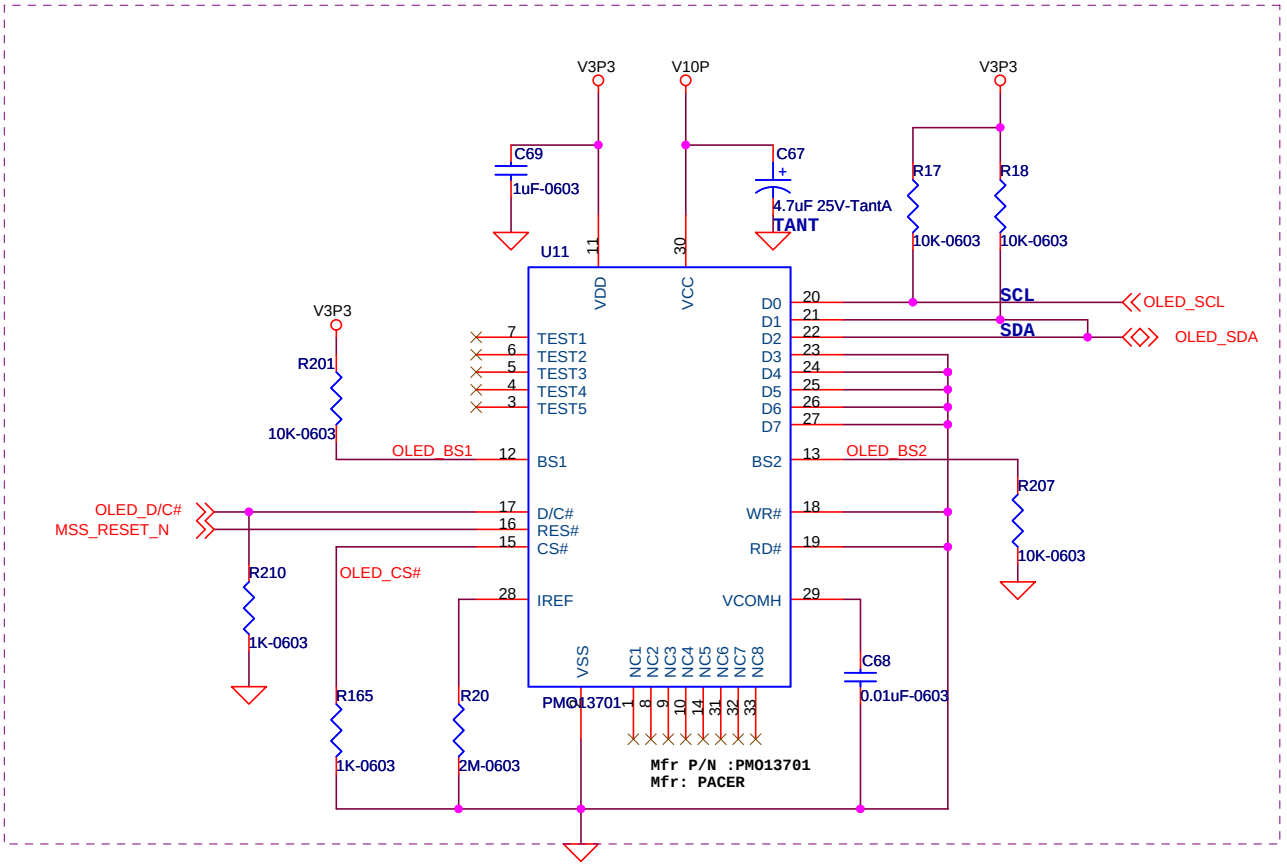
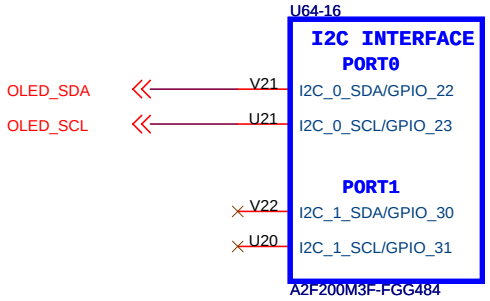
OLED DISPLAY



MSS BLOCK PAGE 1

Fusion2 MSS I2C Interface



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Schematic	sch_00_Top	OLED Display
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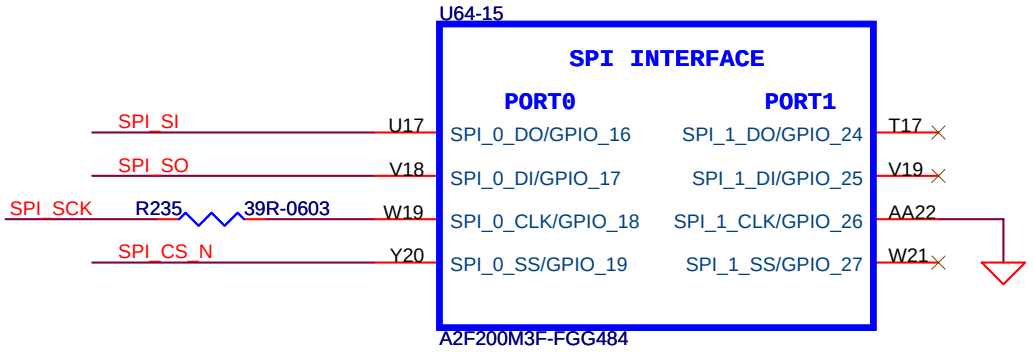
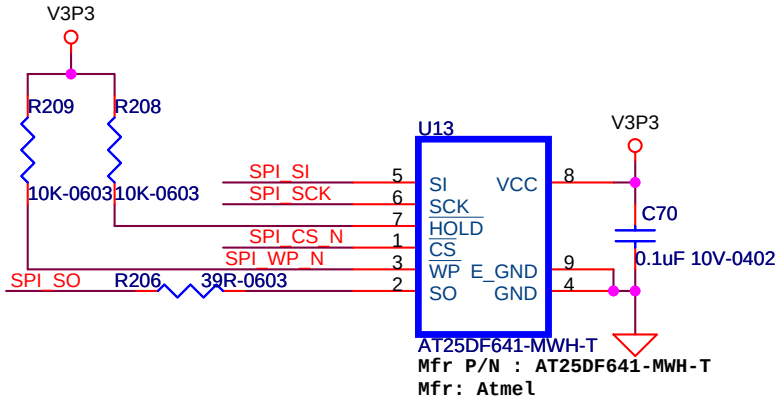
MSS BLOCK PAGE 2

Fusion2 MSS SPI Interface



SPI FLASH 8 MByte



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Schematic	sch_00_Top	MSS Block2	
Title	Smart Fusion Evaluation Kit		
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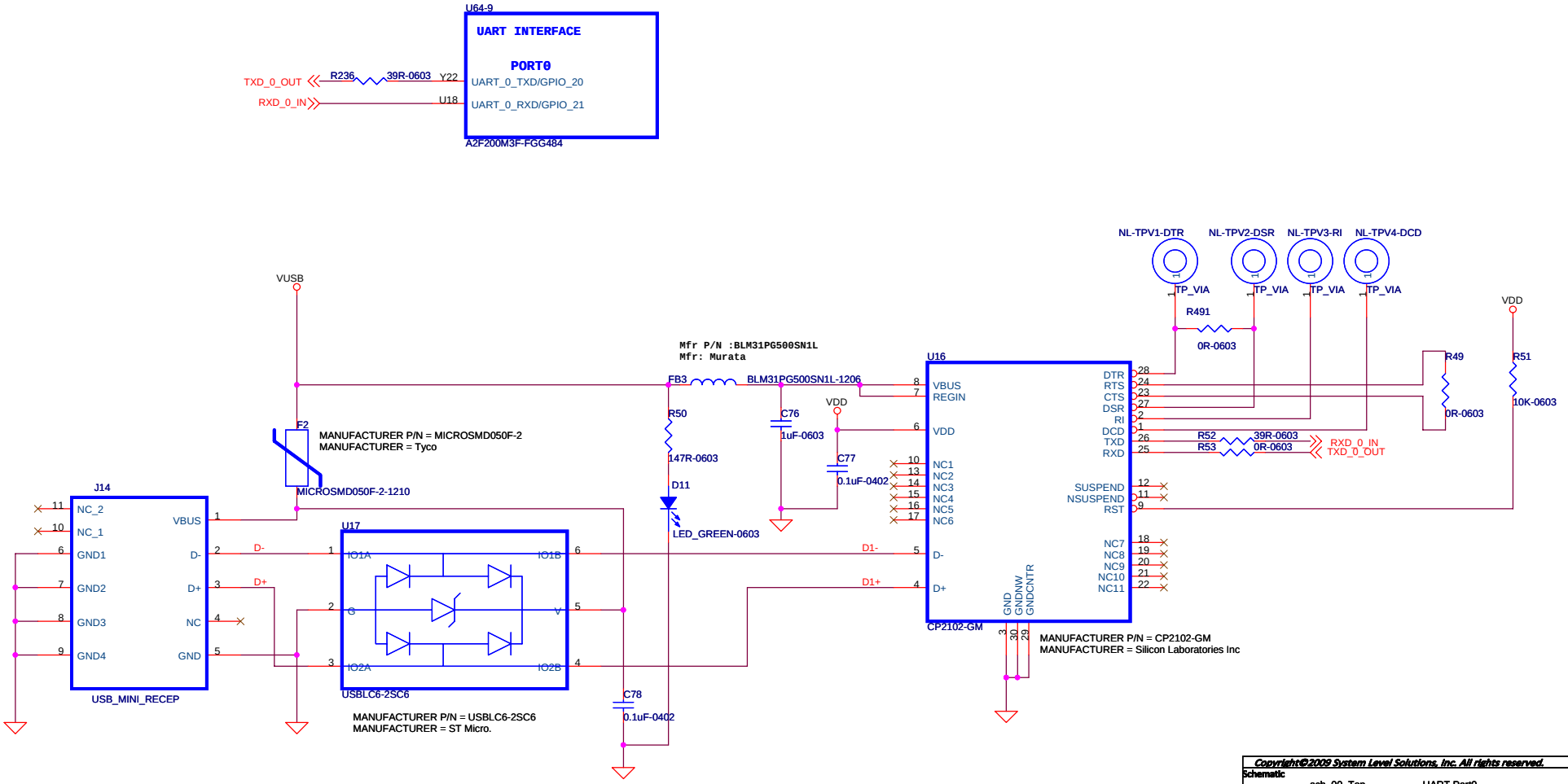
UART PORT 0



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Schematic	sch_00_Top	UART Port0	
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Size B	Document Number SCH-SMFSNEVK-0940-B1B		Rev B
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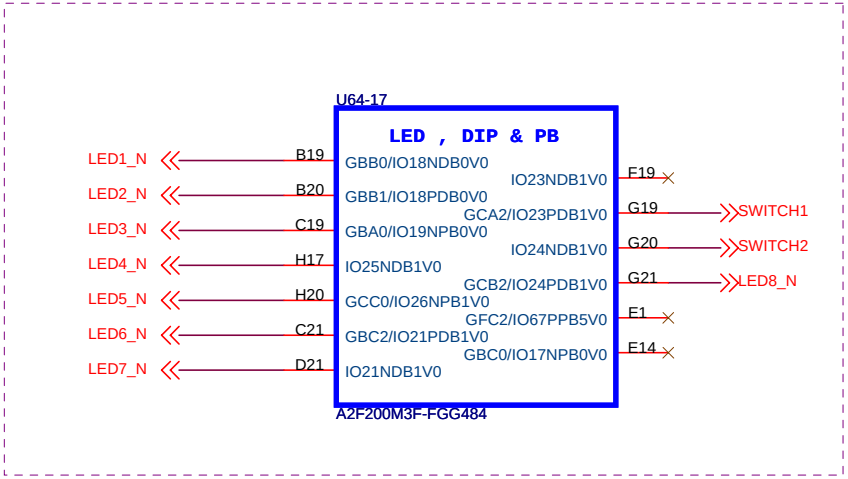
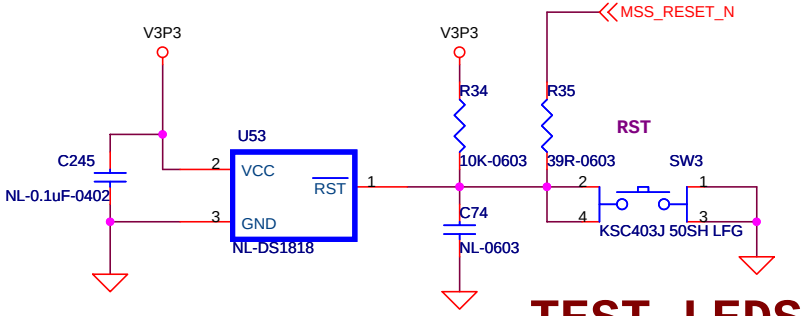
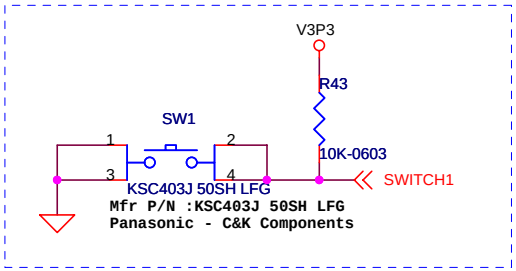
USER DEBUG LOGIC

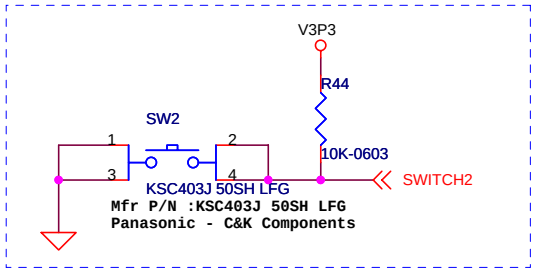
PUSH BUTTON SYSTEM RESET FOR DUT



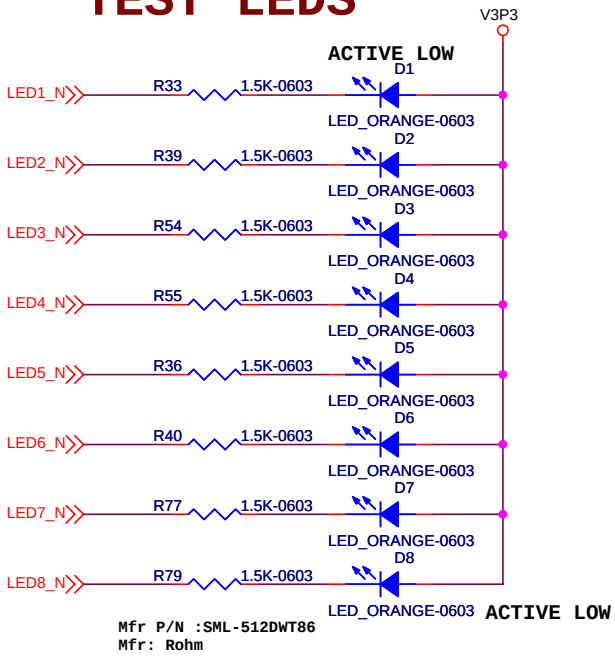


TEST & NAVIGATION SWITCHES





TEST LEDS



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Schematic	sch_00_Top	Debug Logic	
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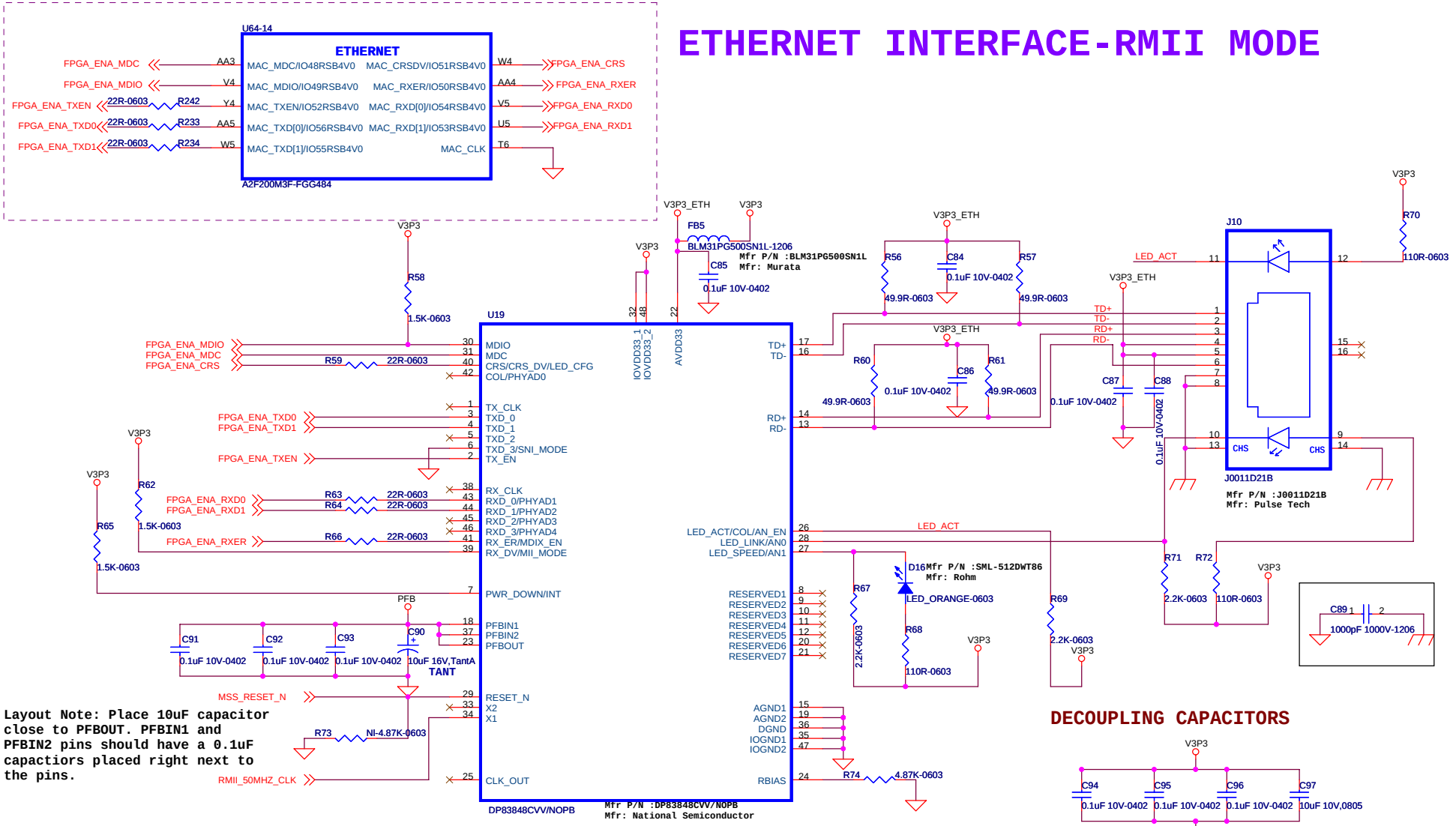
ETHERNET INTERFACE-RMII MODE



Layout Note: Place 10uF capacitor close to PFBOUT. PFBIN1 and PFBIN2 pins should have a 0.1uF capactiors placed right next to the pins.

DECOUPLING CAPACITORS

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Schematic	sch_00_Top	Ethernet Interface	
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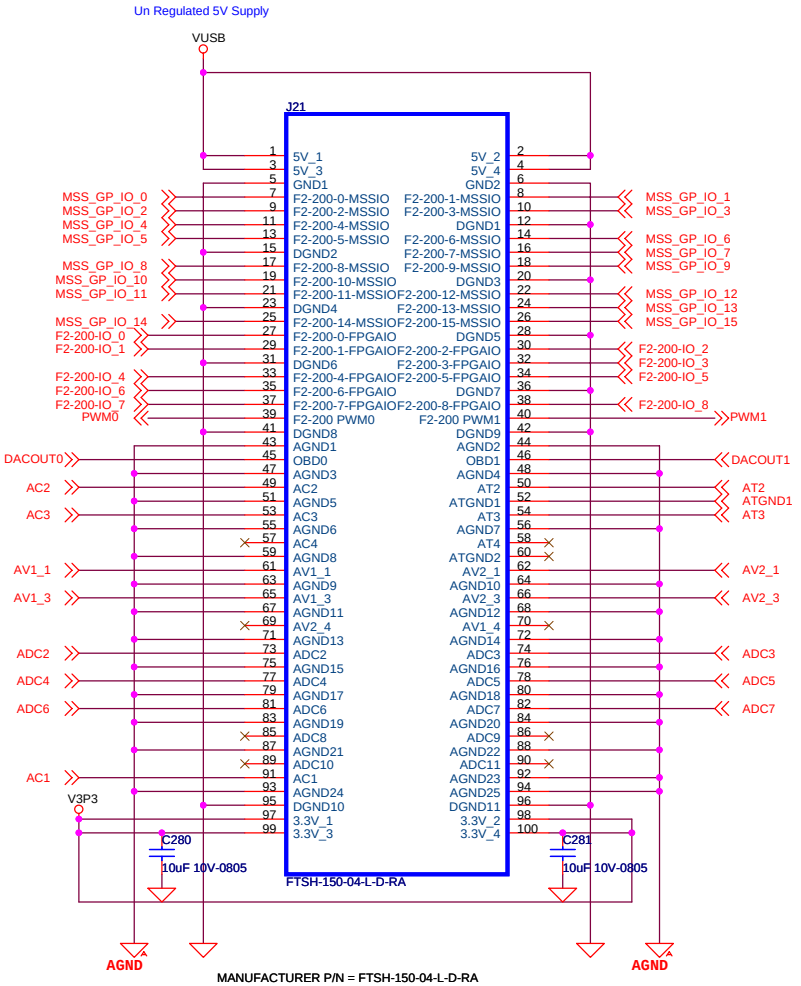
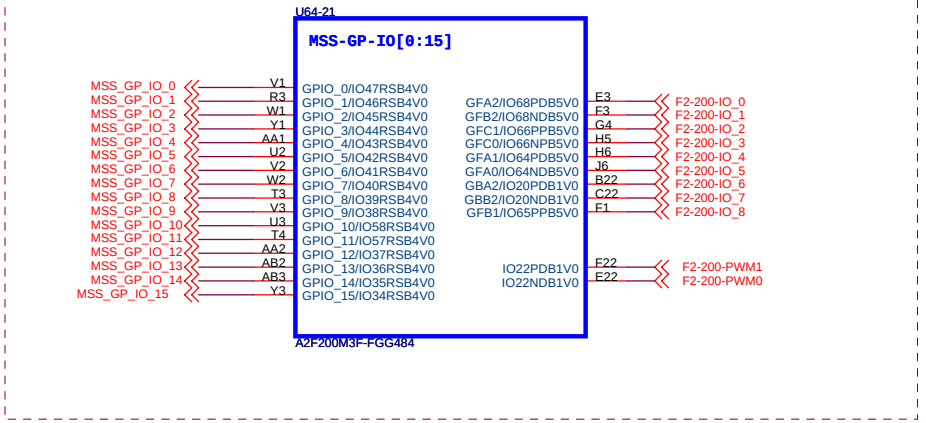
MIXED SIGNAL CONN & DIRECTC

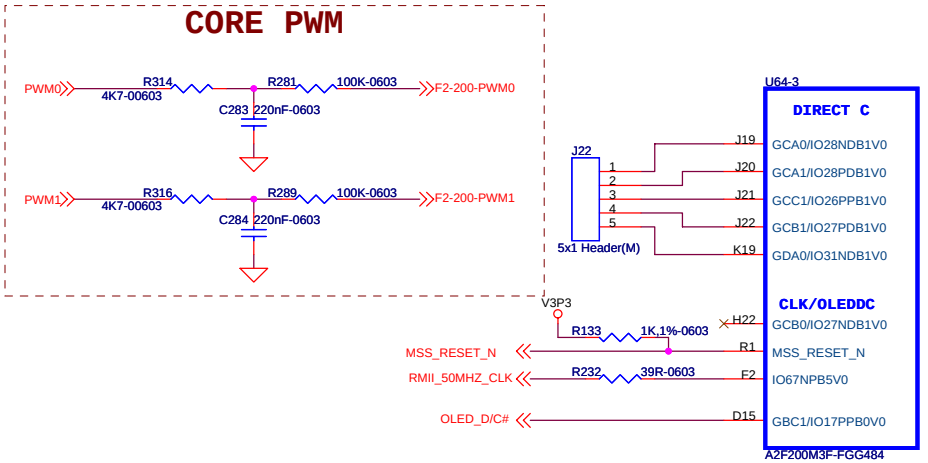
MIXED SIGNAL CONNECTOR



MANUFACTURER P/N = FTSH-150-04-L-D-RA
MANUFACTURER = Samtec

Mating Connector : CLP-150-02-F-DH
Manufacturer: Samtec





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Schematic	sch_00_Top	Mix Signal Connector	
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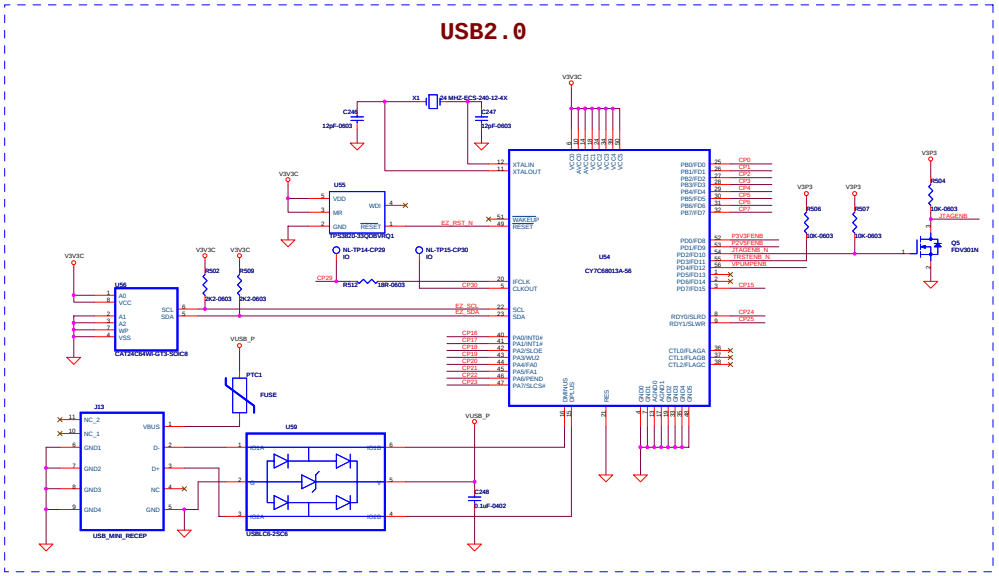
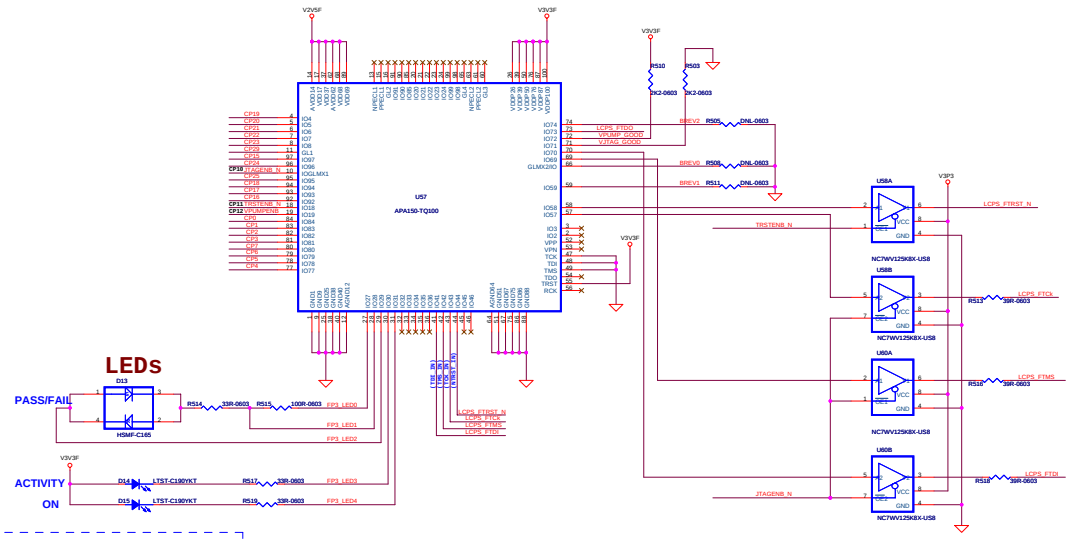
LCPS Programming Section

USB2.0

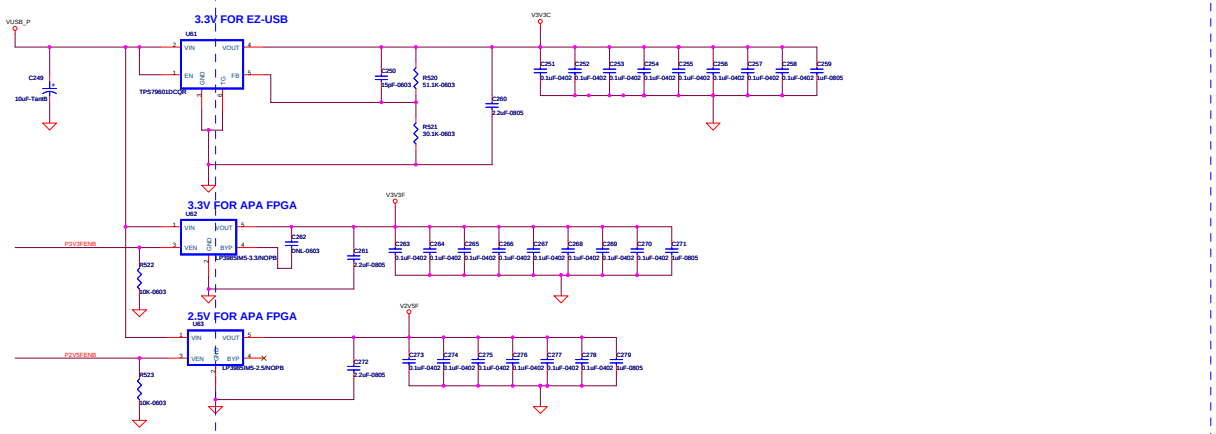


APA150-TQ100

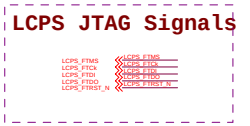


LEDs

POWER REGULATORS



LCPS JTAG Signals



Schematic	sch_00_Top	LCPS Interface	
Title	Smart Fusion Evaluation Kit		
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FM1

Board FAB

Board FAB

Board fiducials

M1

Fiducial

M2

Fiducial

M3

Fiducial

M4

Fiducial

M15

Rubber Foot

M16

Rubber Foot

M17

Rubber Foot

M18

Rubber Foot

M23

Rubber Foot

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Schematic	sch_00_Top	Manufacturing Points
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