

Power Matters.



SmartFusion2 Design Seminar

Hosted by Microsemi & Avnet-Memec

September 2013



Agenda

- Introductions
 - Microsemi Products / Applications Overview
- SmartFusion2 Overview
- SmartFusion2 Design Flow : Fabric FPGA
 - FPGA Fabric Architecture
 - Lab 1 – FPGA design with Libero SoC
- SmartFusion2 Design Flow : Microcontroller Subsystem
 - Microcontroller Subsystem Architecture
 - Lab 2 – ARM Cortex-M3 Lab with SoftConsole
 - Lab 3 – USB Implementation
- Igloo 2 introduction

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Microsemi Products/Applications Overview

About Microsemi Corporation (Nasdaq: MSCC)

- Global provider of semiconductor solutions for applications focused on delivering power, reliability, security and performance.
- High-value, high barrier-entry markets:
 - Communications
 - Defense & Security
 - Aerospace
 - Industrial
- FY 2012 Revenue: \$1 billion



Corporate headquarters in Aliso Viejo, CA

Successful Product Technology Portfolio

corp

FY2011:



FY2010:



FY2009:



FY2008:



FY2007:



FY2006:



FY2011

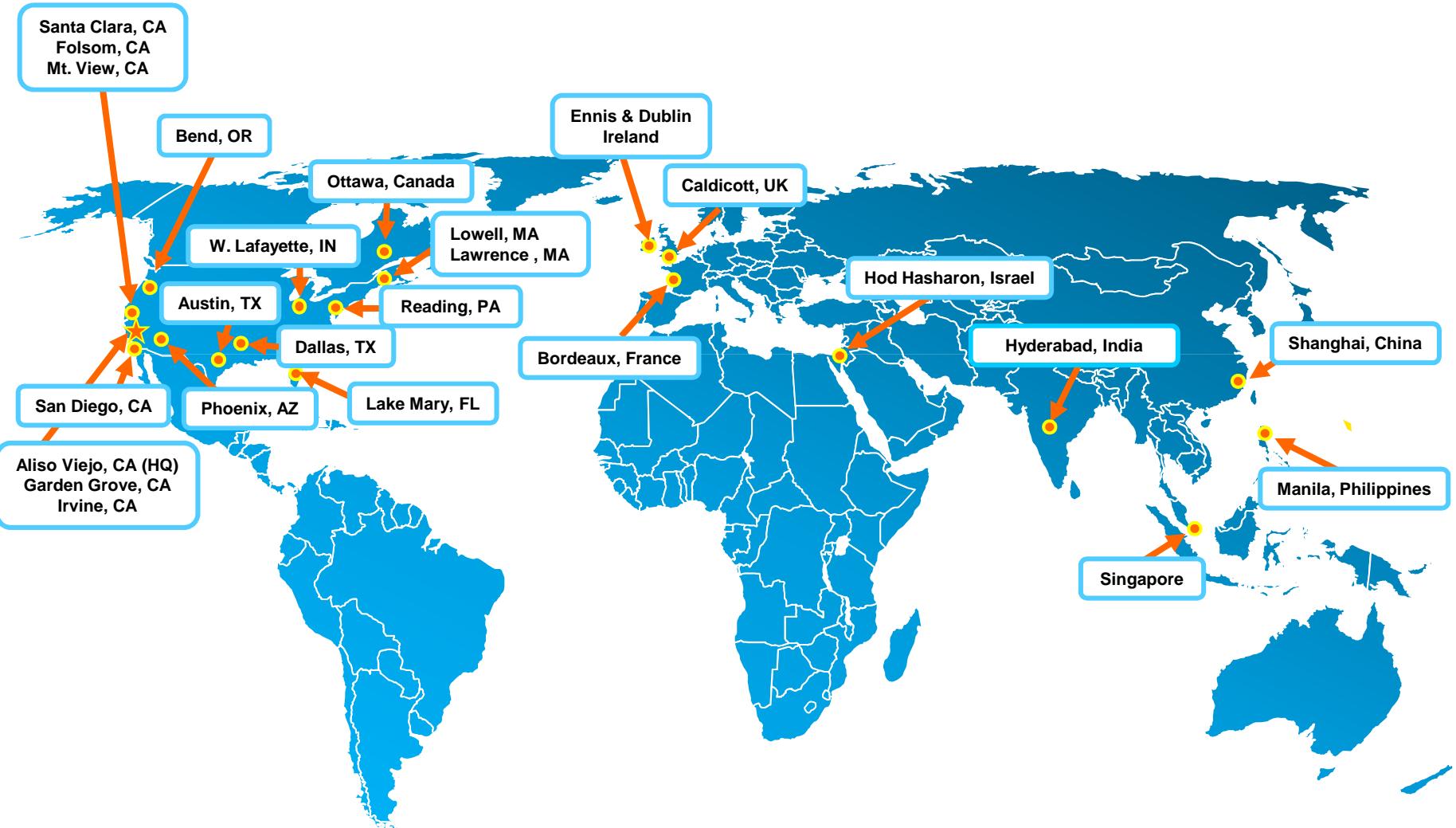


FY2012



Timing, Synchronization
and Synthesis Business

Key Design Centers Worldwide



A Model of Managed Growth

***Consistently Driving
SAM Expansion***

2001 SAM: \$500M

- Small Signal Transistors
- Medium Signal Transistors
- Inverters
- LDOs

2001

2006 SAM: \$850M

- GaAs Diodes
- RF Power Amplifiers
- Power Switching
- Small Signal Transistors

2006

2012 SAM: \$5.2B

- Network Timing & Sync
- Power-over-Ethernet
- Voice Line Circuits
- WLAN Power Amplifiers
- FPGAs/SoCs
- Anti-tamper
- Board Level Systems
- DC/DC
 - ICs
 - Converters
 - Subsystems
- GaAs Diodes
- LED Backlighting
- RadHard
 - MOSFETs
 - Hybrids
 - Transistors

2012

Microsemi Market/Customer Focus

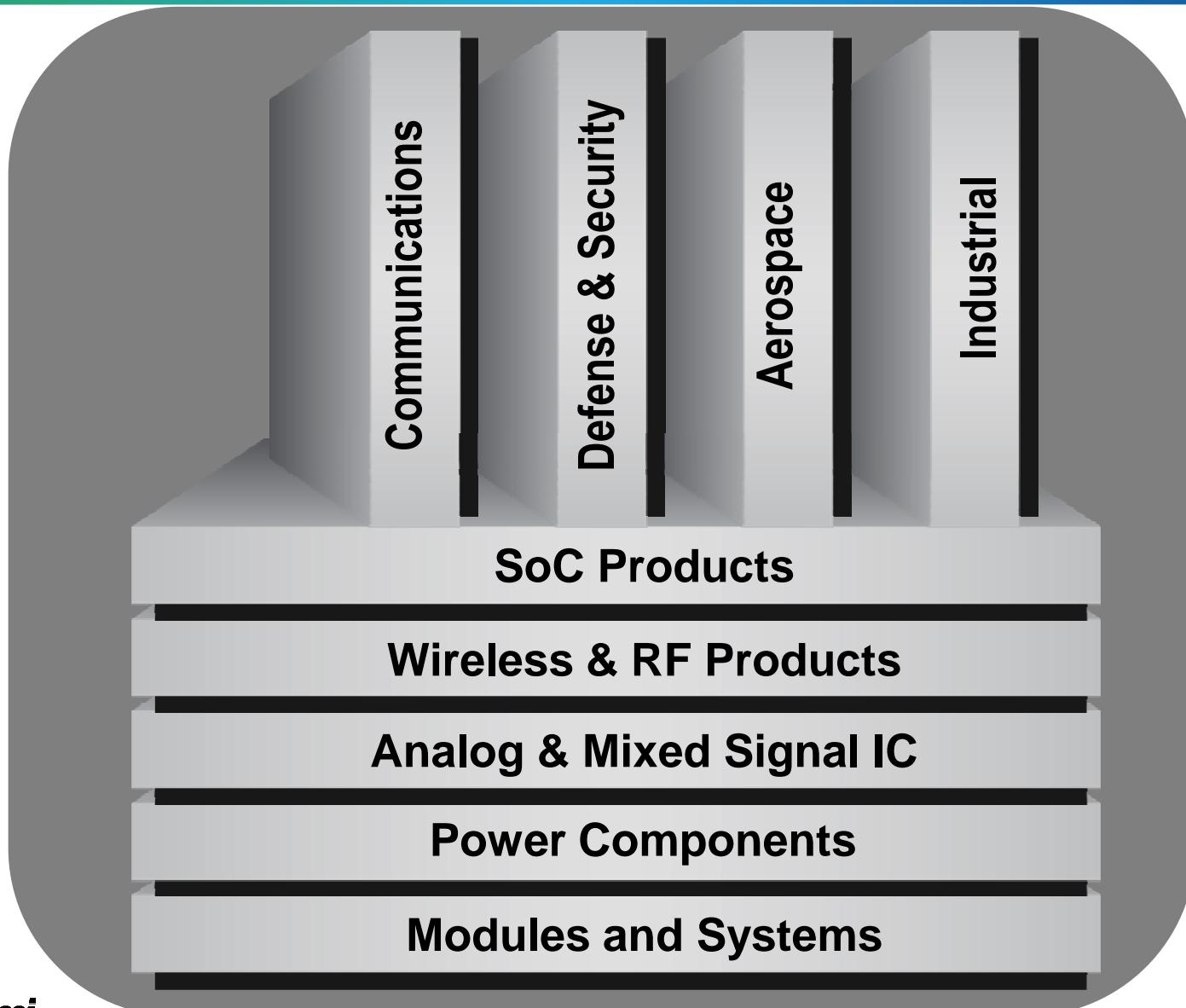
Communications 31% of Revenue	Defense & Security 31% of Revenue	Aerospace 19% of Revenue	Industrial 19% of Revenue
Wireless Backhaul Base Station Routing & Switching Networking Access & CPE Wireless Terminal	Military Communication Military Aircraft Unmanned Vehicle Information Assurance Security Scanners Anti-Tamper	<u>Commercial Air</u> Engine Control Avionics Actuation <u>Space</u> Power Delivery Payload Electronics Launch Systems	Industrial Control Medical Devices Alternative Energy Hybrid Vehicles SEMI Cap Equipment Machine to Machine



Based on FQ1 2013 revenue

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Industry's Broadest Product Portfolio



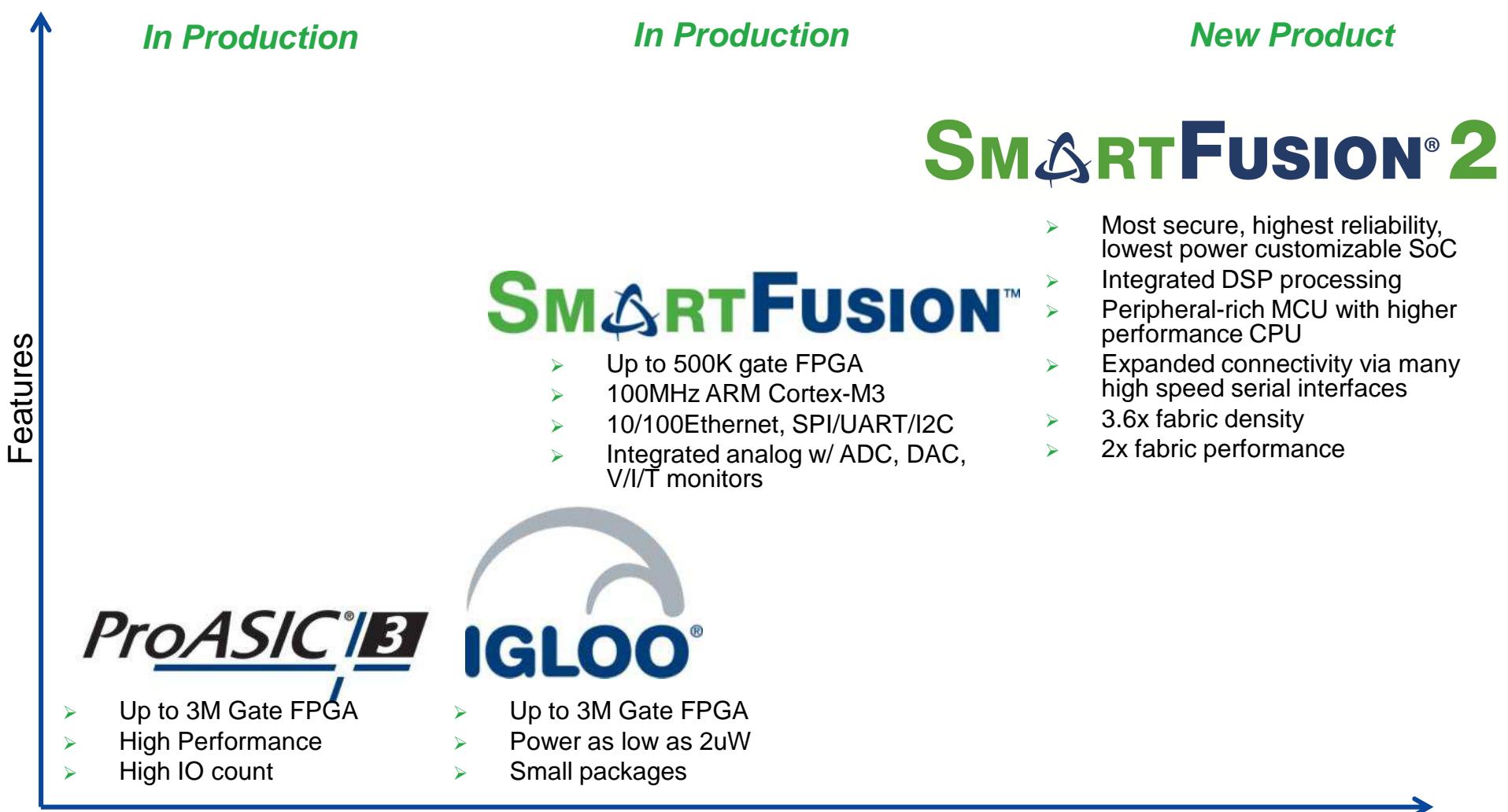
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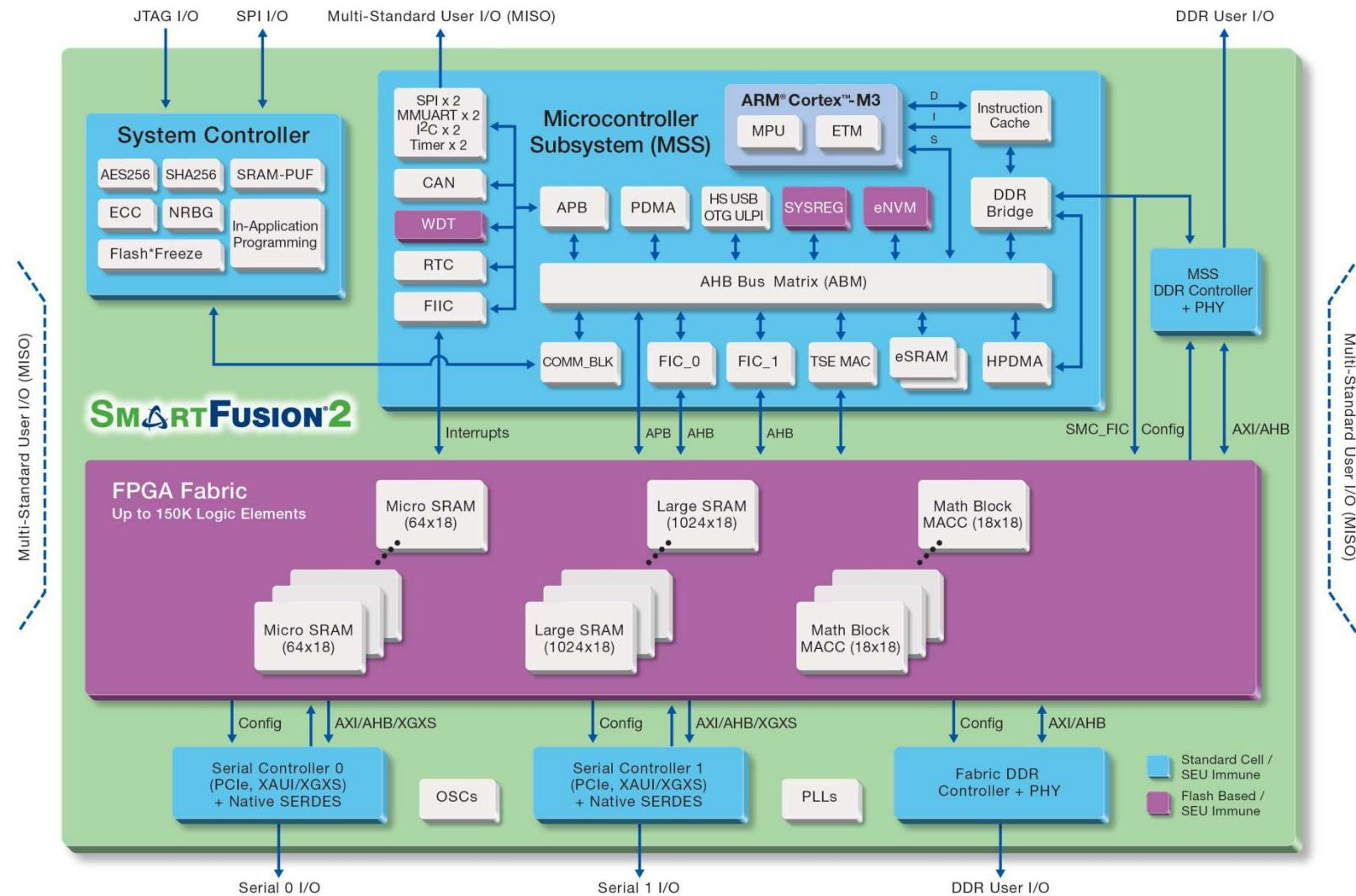
SmartFusion2 Overview

Microsemi SoC Product Roadmap

Increasing system features on differentiated flash technology



SmartFusion2 Architecture



SmartFusion2 Family

	Features	M2S005	M2S010	M2S025	M2S050	M2S090	M2S100	M2S150								
Logic/DSP	Maximum Logic Elements (4LUT + DFF)	6,060	12,084	27,696	56,340	86,316	99,512	146,124								
	Math Blocks (18x18)	11	22	34	72	84	160	240								
	PLLs and CCCs	2		6			8									
Security	AES256, SHA256, RNG	1 each			1 each											
	ECC, PUF	-			1 each											
MSS	Cortex-M3 + Instruction cache	Yes														
	eNVM (K Bytes)	128	256			512										
	eSRAM (K Bytes)	64														
	eSRAM (K Bytes) Non SECDED	80														
	CAN, 10/100/1000 Ethernet, HS USB	1 each														
	Multi-Mode UART, SPI, I2C, Timer	2 each														
Fabric Memory	LSRAM 18K Blocks	10	21	31	69	109	160	236								
	uSRAM1K Blocks	11	22	34	72	112	160	240								
	Total RAM (K bits)	191	400	592	1314	2074	3040	4488								
High Speed	DDR Controllers (Count x Width)	1x18			2x36	1x18	2x36									
	SERDES Lanes	0	4		8	4	8	16								
	PCIe End Points	0	1		2			4								
User I/Os	MSIO (3.3V)	115	123	157	139	306	292	292								
	MSIOD (2.5V)	28	40	40	62	40	106	106								
	DDRIO (2.5V)	66	70	70	176	66	176	176								
	Total User I/O	209	233	267	377	412	574	574								

SmartFusion2 Packaging Options

Type	Package Options									
	VF400		FG484		FG676		FG896		FC1152	
Pitch (mm)	0.8		1.0		1.0		1.0		1.0	
Length x Width (mm)	17x17		23x23		27x27		31x31		35x35	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2S005	169*	-	209*	-						
M2S010(T)	195	4	233	4						
M2S025(T)	195	4	267	4						
M2S050(T)	207	4	267	4			377	8		
M2S090(T)			267	4	412*	4*				
M2S100(T)									574	8
M2S150(T)									574	16
* Preliminary										

Die and Package Rollout

Die	Package	Libero Design Support	ES / PP	Commercial	Industrial
M2S005	FG484	11.0 SP1 (6/14/13)	N/A	Sep-13	Oct-13
M2S010	FG484	Now	Jun-13	Jul-13	Aug-13
M2S025	FG484	Now	N/A	Aug-13	Sep-13
M2S050	FG484	Now	NOW	May-13	Jun-13
M2S090	FG484	Coming Soon	N/A	Mar-14	Apr-14

Die	Package	Libero Design Support	ES / PP	Commercial	Industrial
M2S005	VF400	Coming Soon	N/A	Oct-13	Nov-13
M2S010	VF400	11.0 SP1 (6/14/13)	Aug-13	Sep-13	Nov-13
M2S025	VF400	11.0 SP1 (6/14/13)	N/A	Oct-13	Nov-13
M2S050	VF400	11.0 SP1 (6/14/13)	Jun-13	Sep-13	Nov-13

Die	Package	Libero Design Support	ES / PP	Commercial	Industrial
M2S050	FG896	Now	NOW	May-13	Jun-13
M2S090	FG676	Coming Soon	Jan-14	Mar-14	Apr-14

Die	Package	Libero Design Support	ES / PP	Commercial	Industrial
M2S100	FC1152	11.0 SP1 (6/14/13)	TBD	Mar-14	Apr-14
M2S150	FC1152	11.0 SP1 (6/14/13)	Dec-13	Feb-14	Mar-14

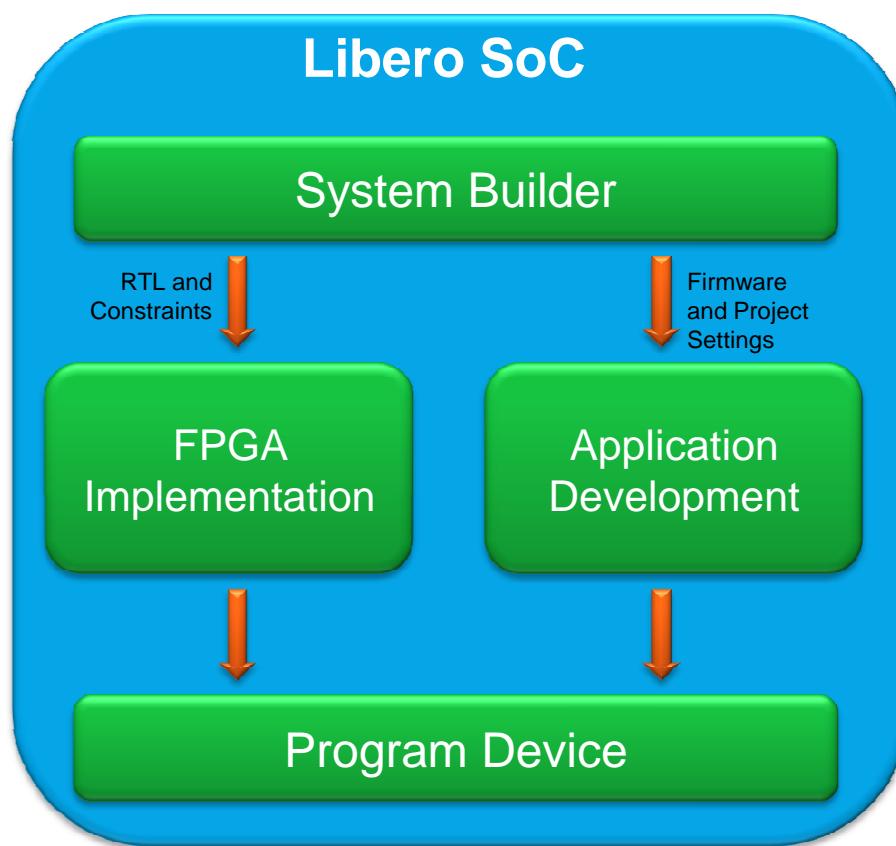
SmartFusion2 Device Variations

- Variety of Features are available for each Die size
 - The smallest device M2S005 does not have the Transceivers option
 - M2S050 examples shown below

Device	Transceivers	Design Security	Advanced Data Security
M2S050	No	Yes	No
M2S050T	Yes	Yes	No
M2S050S	No	Yes	Yes
M2S050TS	Yes	Yes	Yes

SmartFusion2 Design Flow

Libero SoC v11.1

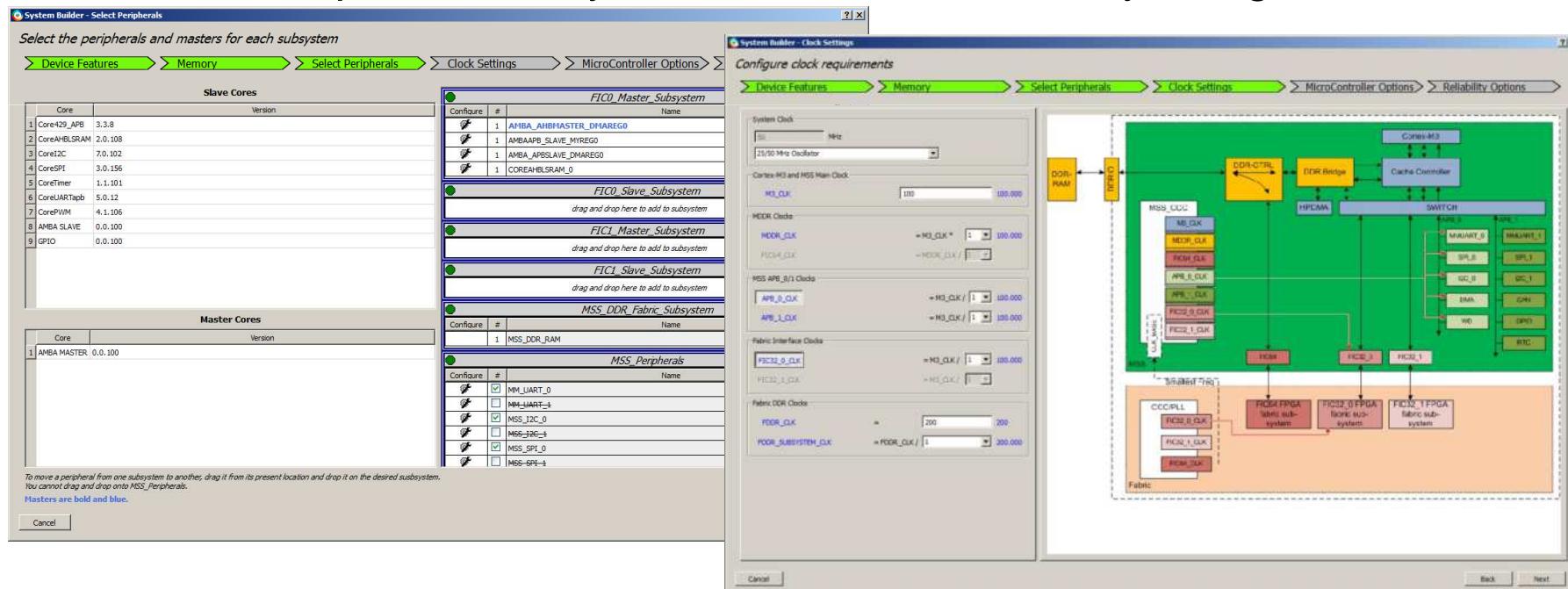


- Libero SoC integrates the traditional FPGA design flow with Microcontroller firmware development

SmartFusion2 System Builder

- **System Builder Wizard**

- Asks the user basic questions on system architecture
 - Adds any additional peripherals in the fabric
 - Walks through configuration options for each selected feature
 - Builds complete base system and API – correct by design



Accelerates architecture design, so engineers can focus on their value add

Libero SoC v11.1 SP1

- **FPGA Design Tools**
 - SmartDesign design entry
 - Rich IP library & user block support facilitates design reuse
 - Synplify Pro® synthesis
 - ModelSim® simulation
 - Power-driven place-and-route
 - SmartPower power analysis
 - SmartTime timing analysis
 - Flexible Programming Options
 - SmartDebug
- **Embedded Design Flow**
 - System Configuration
 - Project Creation
 - Firmware generation
 - Include file setup
 - SoftConsole Eclipse-based IDE
 - GNU GCC
 - GNU GDB debug

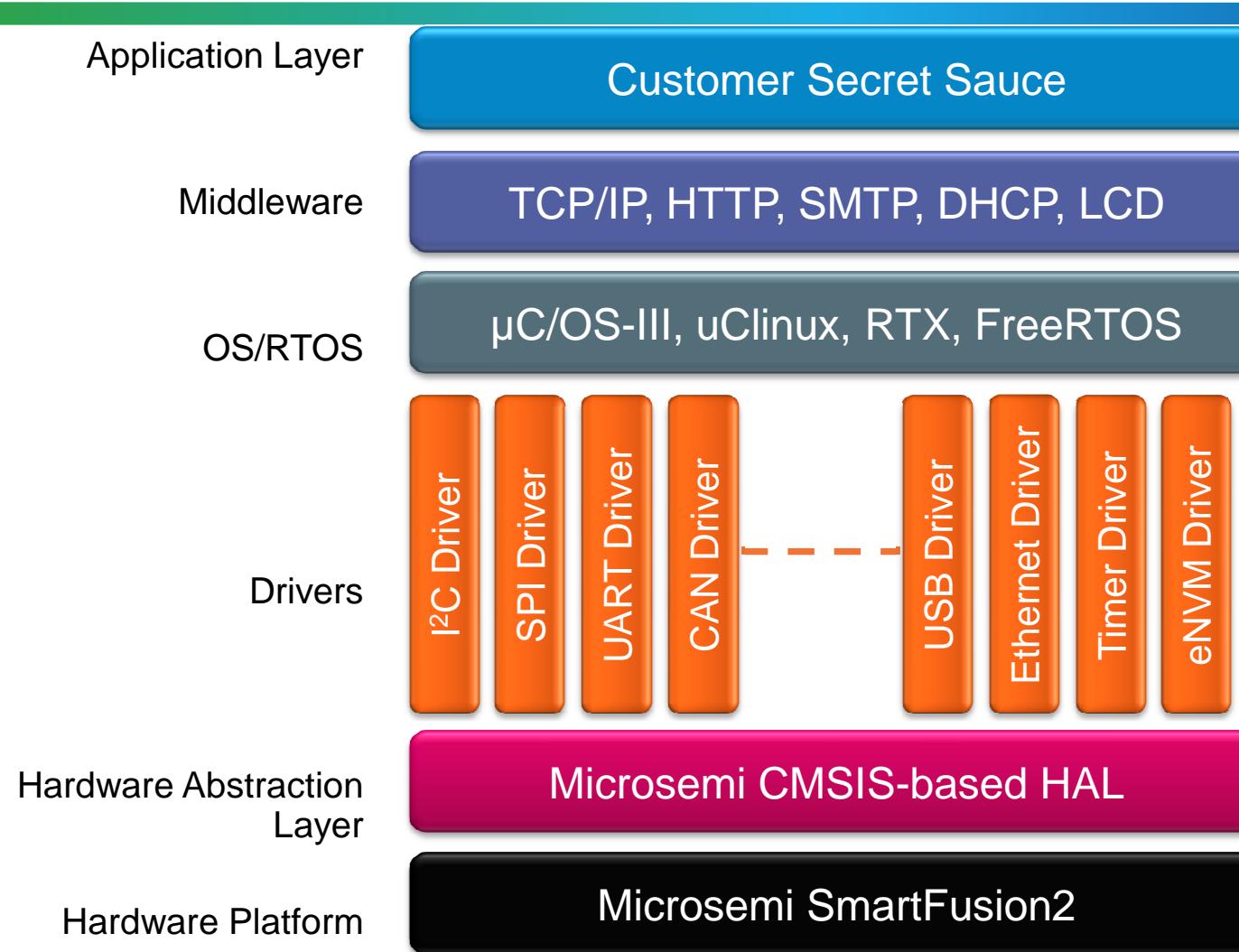


Embedded Design Options

 CMSIS COMPLIANT <small>ARM® Cortex® Microcontroller Software Interface Standard</small>	 Microsemi.	 KEIL™ An ARM® Company	 IAR SYSTEMS
Software IDE	SoftConsole	Keil MDK	IAR Embedded Workbench®
Website	www.microsemi.com/soc	www.keil.com	www.iar.com
Free versions from SoC Products Group	Free with Libero SoC	32 K code limited	32 K code limited
Available from Vendor	N/A	Full version	Full version
Compiler	GNU GCC	RealView C/C++	IAR ARM Compiler
Debugger	GDB debug	Vision Debugger	C-SPY® Debugger
Instruction Set Simulator	No	Vision Simulator	Yes
Debug Hardware	FlashPro4	ULINK2® or ULINK-ME	J-LINK™ or J-LINK Lite

- SmartFusion2 starter kit software options include
 - Free Libero SoC license
 - Free SoftConsole support
 - Optional Embedded Linux design environment

SmartFusion2 Software Stack



SmartFusion stack accelerates application development

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SmartFusion2 Starter Kit

SmartFusion2 Starter Kit



SF2-STARTER-KIT Overview



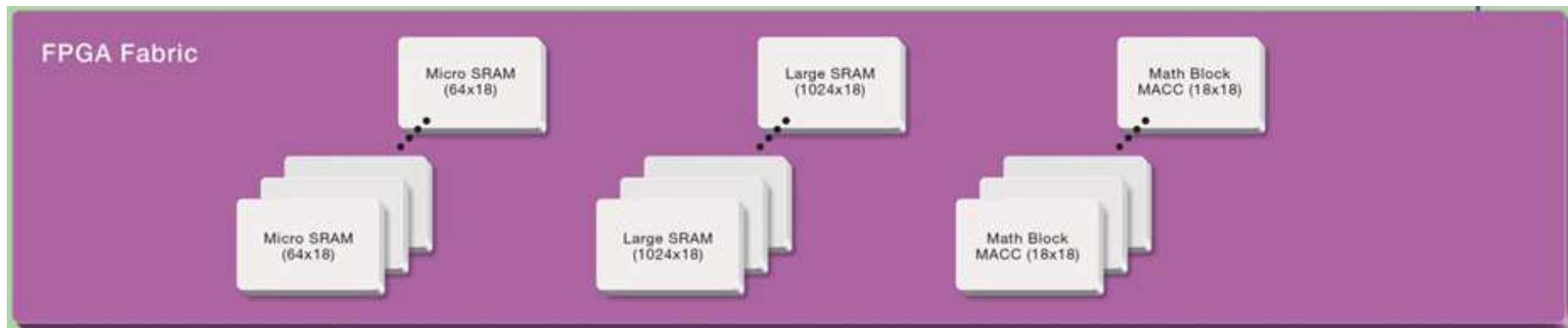
- Cost-effective and flexible platform for entry into designing with SmartFusion2
- USB OTG interface and mini-USB connector
- USB based Wi-Fi module
- JTAG Interface for program and debug using FlashPro4
- 64MB LPDDR, 16MB SPI flash
- Two user-controlled LEDs connected to GPIO on the SOM
- Power good LED indicating presence of the +3.3 V SOM power
- Reset push button, Reset-out LED
- Breadboard area available for GPIO or FPGA I/O connection
- On-module clocks
- Watchdog Timer (WDT)

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FPGA Fabric Architecture

FPGA Fabric

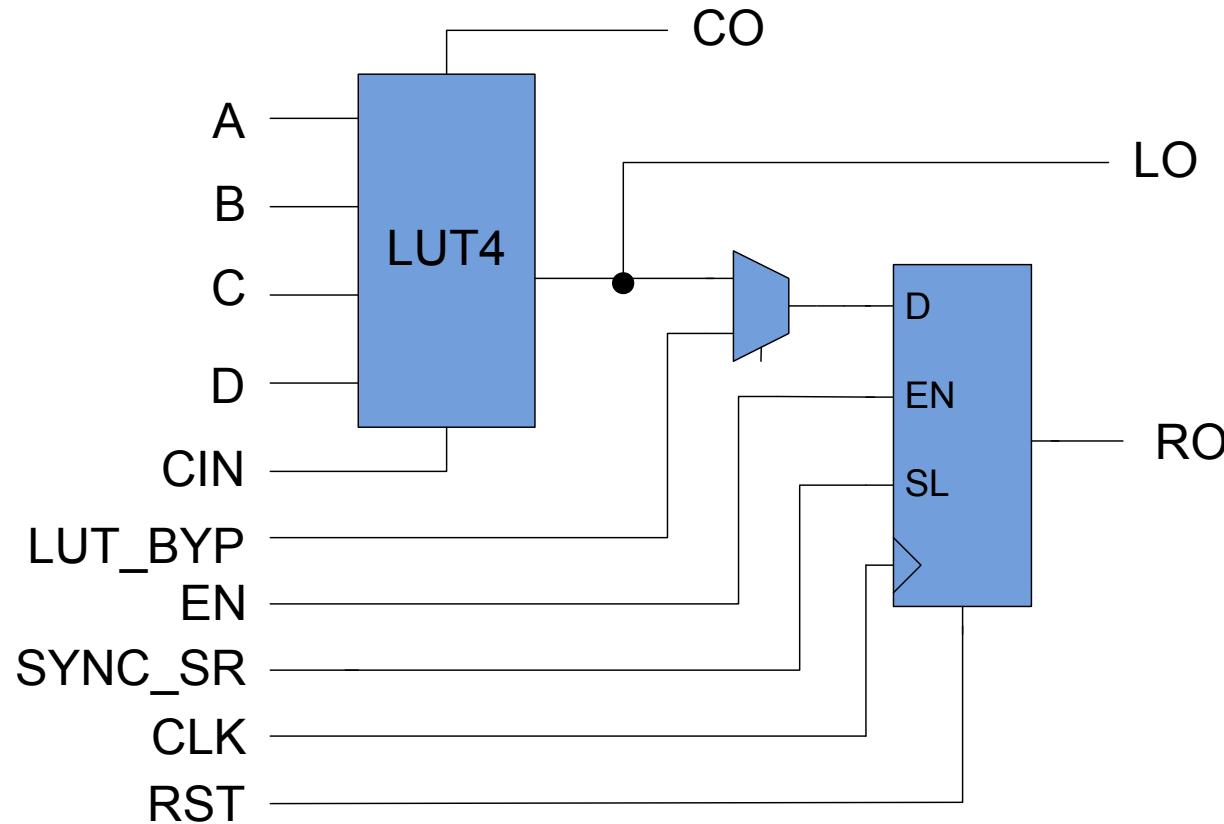


	Features	M2S005	M2S010	M2S025	M2S050	M2S090	M2S100	M2S150
FPGA	Logic Modules (4-Input LUT)	6,060	12,084	27,696	56,340	86,316	99,512	146,124
	LSRAM 18K Blocks	10	21	31	69	109	160	236
	uSRAM1K Blocks	11	22	34	72	112	160	240
	Total RAM (bits)	191K	400K	592K	1,314K	2,074K	3,040K	4,488K
	Math Blocks	11	22	34	72	84	160	240
	PLLs and CCCs	2	2	6	6	6	8	8

High-Performance FPGA (Fabric)

- Efficient 4-Input LUT architecture for lowest power
 - Carry chains for high performance
 - DFF
- Up to 236 Blocks of Dual-Port 18 Kbit SRAM (Large SRAM)
 - 400 MHz Synchronous Performance (x18, x9, x4, x2, x1)
- Up to 240 Blocks of Three-Port 1 Kbit SRAM (Micro SRAM)
 - 2 Read ports and 1 write port
- High Performance DSP Signal Processing
 - Up to 185 Fast Math Blocks with 18x18 Multiplier / 44-Bit Accumulator

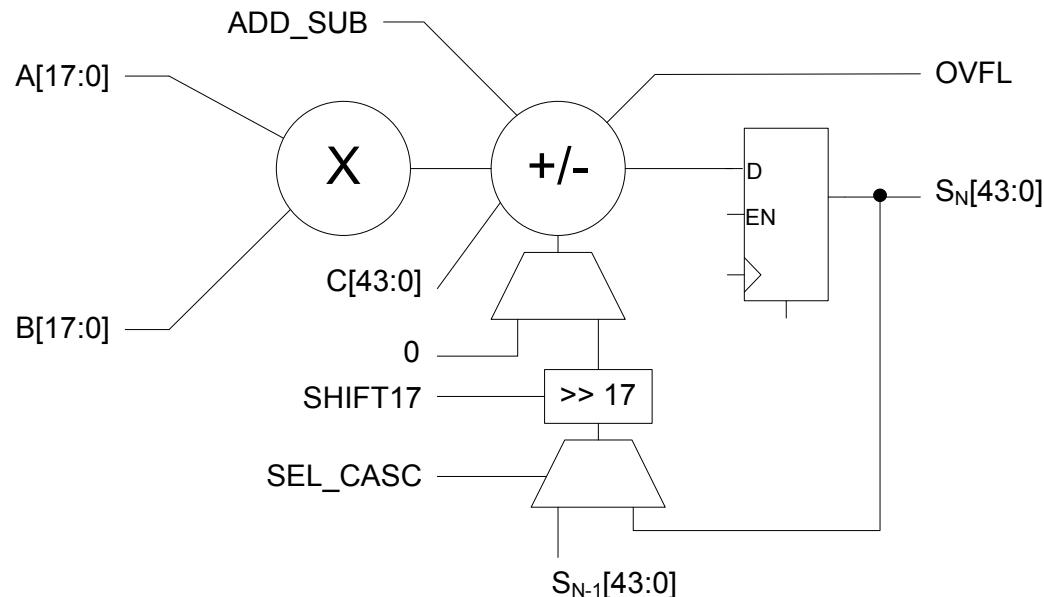
FPGA Logic Module



Simplified Diagram

FPGA Math Block

- 11 to 240 math blocks
- Supports 18×18 signed, 17×17 unsigned
- Internal cascade signals (44-bit CDIN and CDOUT) to support larger accumulators/adders/subtracters without extra logic
- Loopback capability to support adaptive filtering
- Supports dot-product ($A[8:0] \times B[17:9] + A[17:9] \times B[8:0]$) $\times 29$
- Adder support: $(A \times B) + C$ or $(A \times B) + D$ or $(A \times B) + C + D$

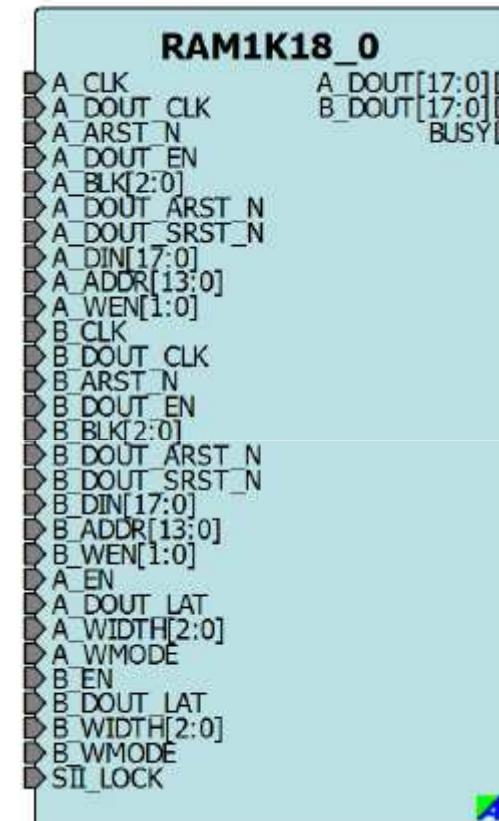


SYNOPSYS®
Synplify Pro®
Symphony Model Compiler

MathWorks®
MATLAB®
Simulink®

FPGA Memory Blocks – Large SRAM

- RAM 18,432 bits
 - Dual Port Configuration
 - Both ports are 18 bits wide or less
 - 1kx18, 2kx9, 4kx4, 8kx2, 16kx1
 - Two Port Configuration
 - One port at least 36 bits wide
 - Other port is either
 - 36,18,9,4,2 or 1 bit wide
 - High performance synchronous operation
 - 400 MHz
 - Ideal for creating larger memories



FPGA Memory Blocks

- uRAM1K bit
 - 18-bit Three Port Memory (2 Reads and 1 Write)
 - Synchronous Writes - always
 - Asynchronous or Synchronous Read Operation
 - 400 MHz
 - Sync Write, Sync Read
 - Configurations
 - 64x18, 128x9, 256x4, 512x2, and 1024x1
 - Implemented as a register file
 - Ideal for small memory, small FIFO, register file, and small DSP look-up tables



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FPGA Fabric Lab

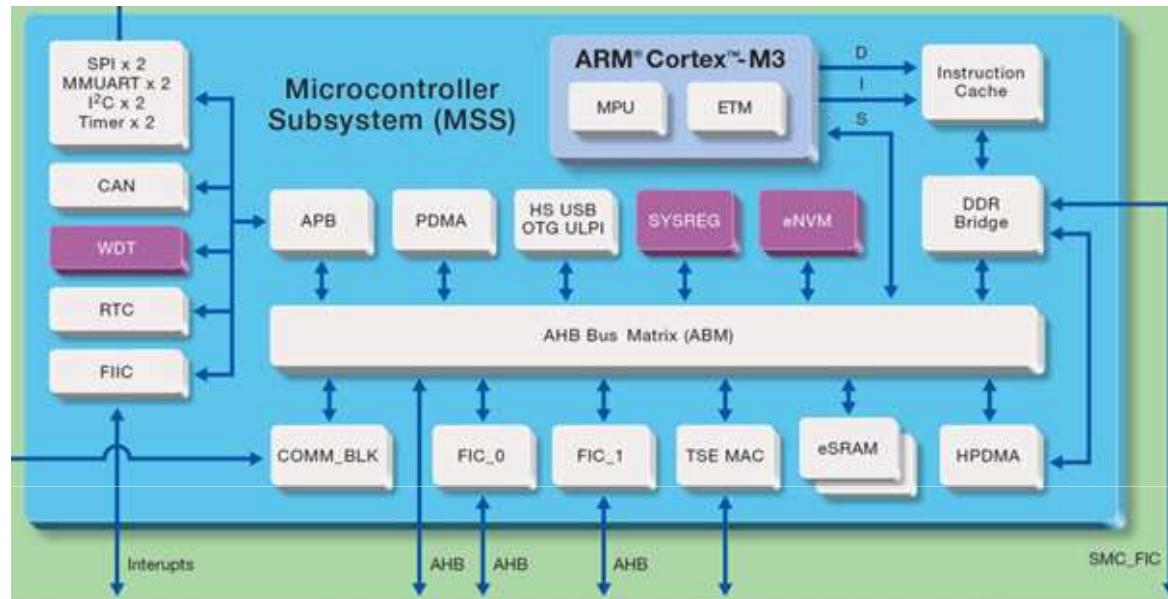
How to implement a basic SmartFusion2 FPGA fabric design using SmartDesign

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Microcontroller Subsystem Architecture

Microcontroller Subsystem

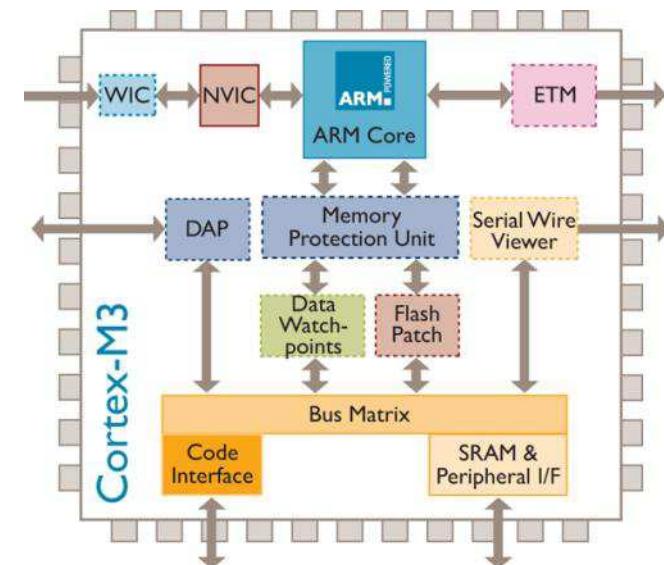
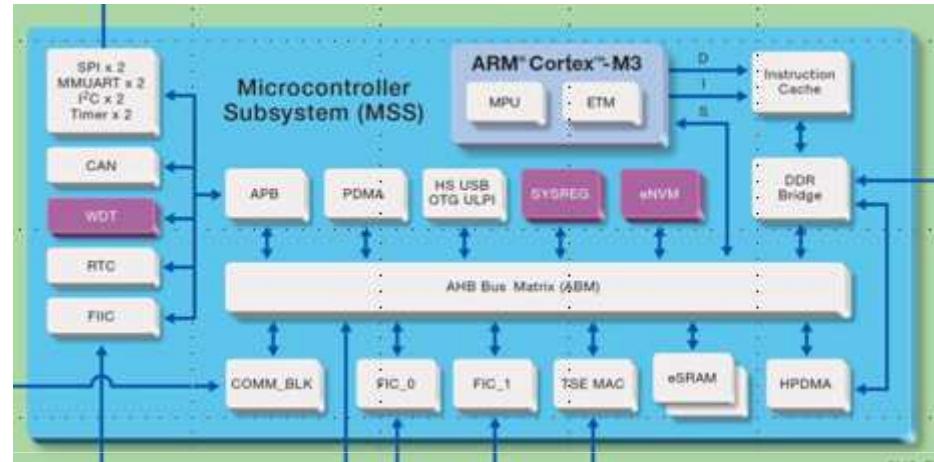


Equivalent to > 70K Luts

	Features	M2S005	M2S010	M2S025	M2S050	M2S080	M2S120
MSS	Cortex-M3 + Instruction cache	YES	YES	YES	YES	YES	YES
	eNVM (Bytes)	128K	256K	256K	256K	512K	512K
	eSRAM (Bytes)	64K	64K	64K	64K	64K	64K
	eSRAM (Bytes non-SECDED)	80K	80K	80K	80K	80K	80K
	CAN / 10/100/1000 MAC /HS USB OTG	1 ea.					
	MMUART/SPI/I2C/Timer	2 ea.					

Micro-Controller Subsystem

- 166 MHz Cortex M3 with Instruction Cache
- 4 Port DDR bridge for data caching
- HS USB OTG
- 10/100/1000 Triple Speed Ethernet
- CAN 2.0a/b with 32 transmit and receive message buffers
- All memories SEU tolerant or SECDED.
- Equivalent to >35K LE's



eNVM

- Page Size
 - 128 bytes
- 64 bit data bus
- SECDED – 1 bit correct 2 bit detect
- Access time for read mode: tbd
- Page-mode for Write/Program/Erase
- Write/Program granularity: Page write, Page program
- Erase granularity: Page erase, Sector erase, Array erase
- Endurance – 10,000+ Page Erase/Program Cycles

eSRAM

- Two Modes

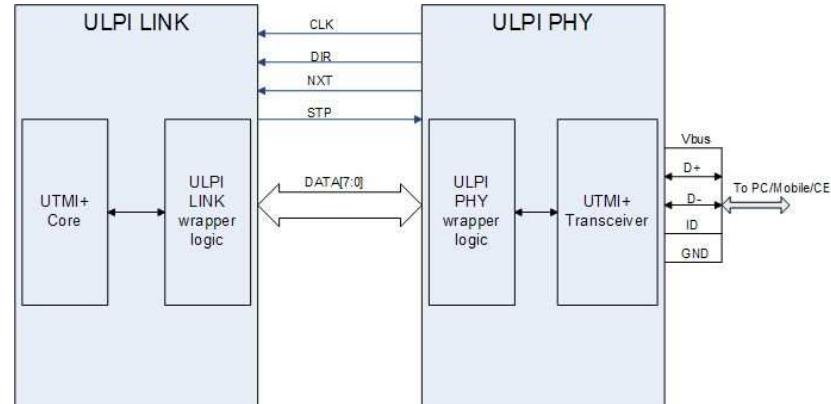
- SECDED enabled
 - 32 Kbyte memory with single error correct double error detect
 - 8 Kbyte memory used for hamming code
- SECDED disabled
 - 32 Kbyte memory with no correction
 - 8 Kbyte memory available for user

Tri Mode Ethernet

- 10,100,1000
 - GMII, MII, TBI Interfaces brought to FPGA Fabric
 - CoreRGMMI
 - Converts GMII to RGMMI
 - CoreRMII
 - Converts MII to RGII
 - CoreTBItoEPSC
 - Converts TBI to SGMII via EPSC lane on SERDES
- Built-in DMA, Performance Monitors
- Local Buffering (SECDED capable)
 - 8K Byte Receive FIFO
 - 4K Byte Transmit FIFO

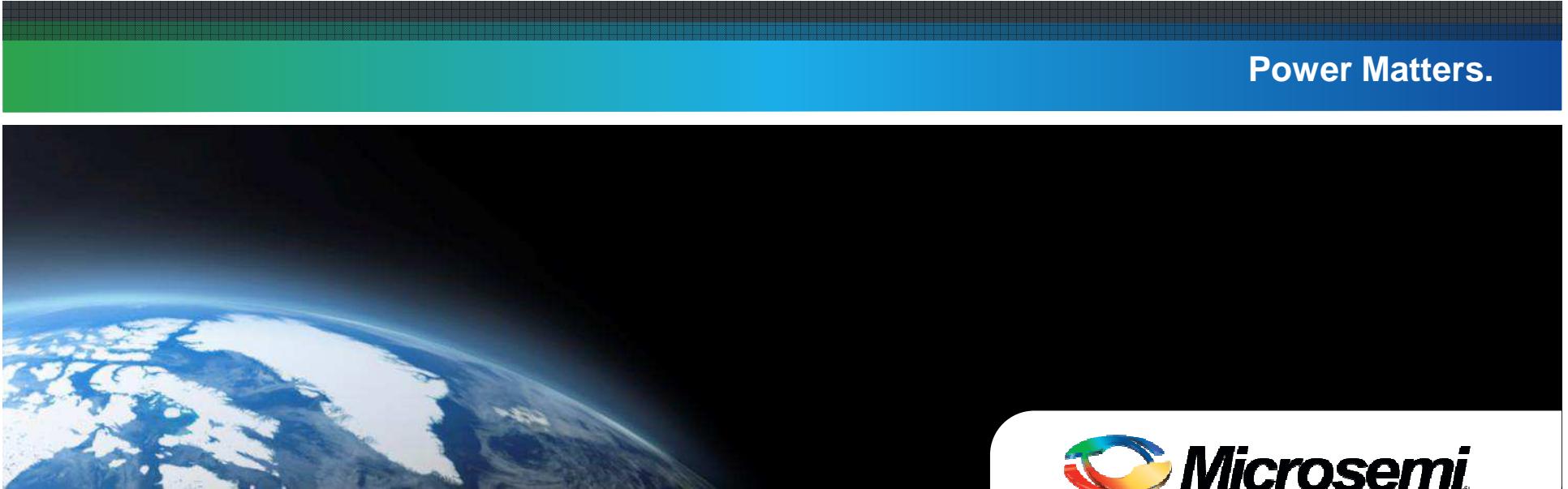
USB

- HS USB OTG
 - Device mode class driver support
 - Mass Storage, HID, & CDC
 - Host Mode class driver support
 - Mass Storage, HID, & CDC
- Local buffers SECDED
- ULPI Interface
 - 12 pin LVCMSOS interface to external PHY



CAN 2.0

- Full CAN 2.0A/B compliant
 - Conforms to ISO 11898-1 - Bosch Compliant
- Receive path
 - 32 receive buffers (SECDED capable)
 - Each buffer has its own message filter
 - Message filter covers ID, IDE, RTR, Data byte1 & Data byte2
 - Useful for DeviceNet protocol
 - Message buffers can be linked together to build a bigger message array
 - Automatic Remote Transmission Request(RTR) response handler with optional generation of RTR interrupt
- Transmit path
 - 32 transmit message holding registers with programmable priority arbitration (SECDED)
 - Message abort command
 - Single shot transmission (No automatic re-transmission upon error or arbitration loss)



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Microcontroller Subsystem Lab

How to implement a basic SmartFusion2 microcontroller subsystem (MSS) configuration that uses the GPIO block and MMUART_0 using the SmartFusion2 MSS configurator

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SmartFusion2 USB Lab

How to configure and use SmartFusion2 USB OTG controller

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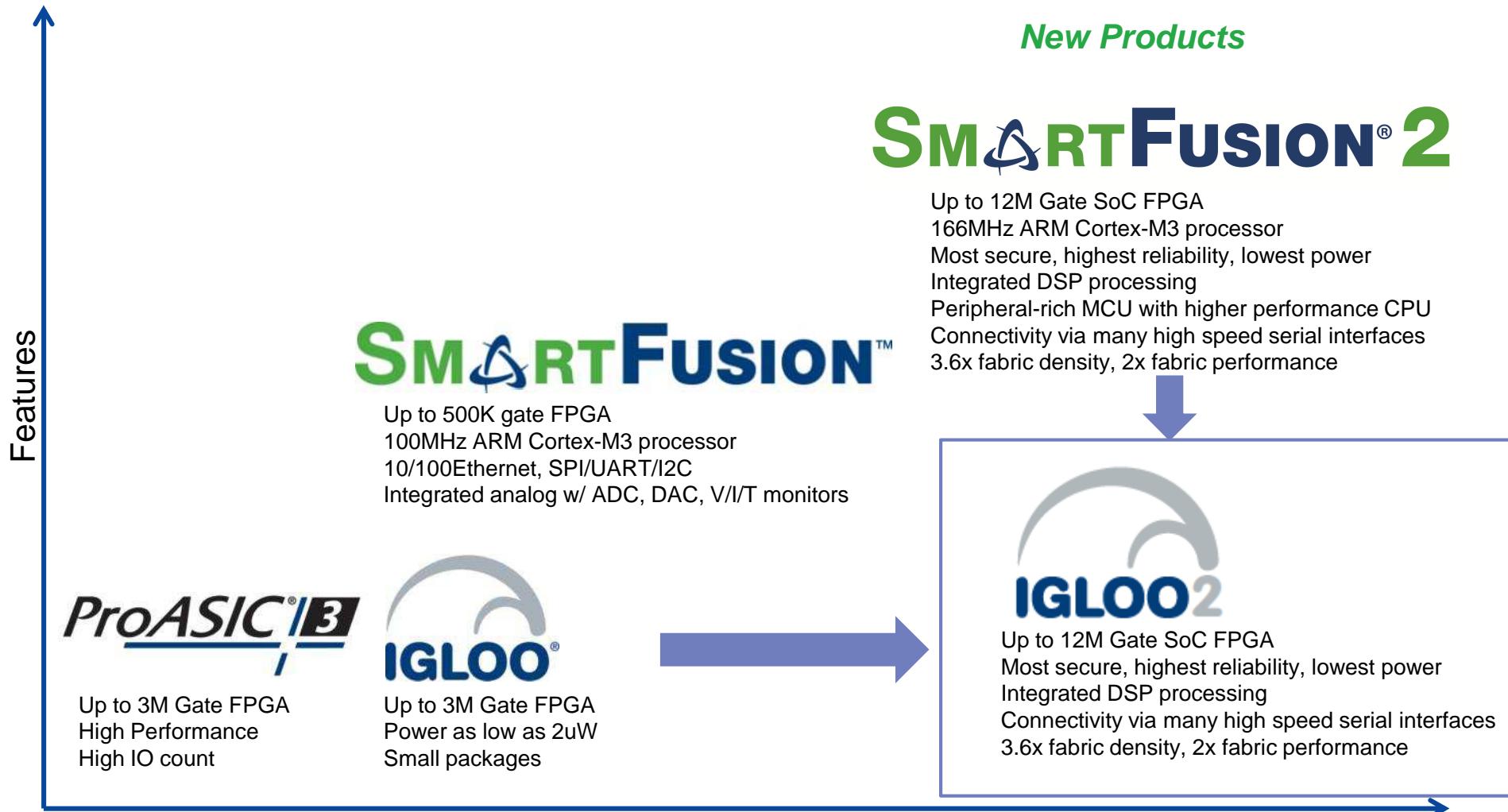
Microsemi IGLOO®2 FPGAs

Highly Integrated FPGA

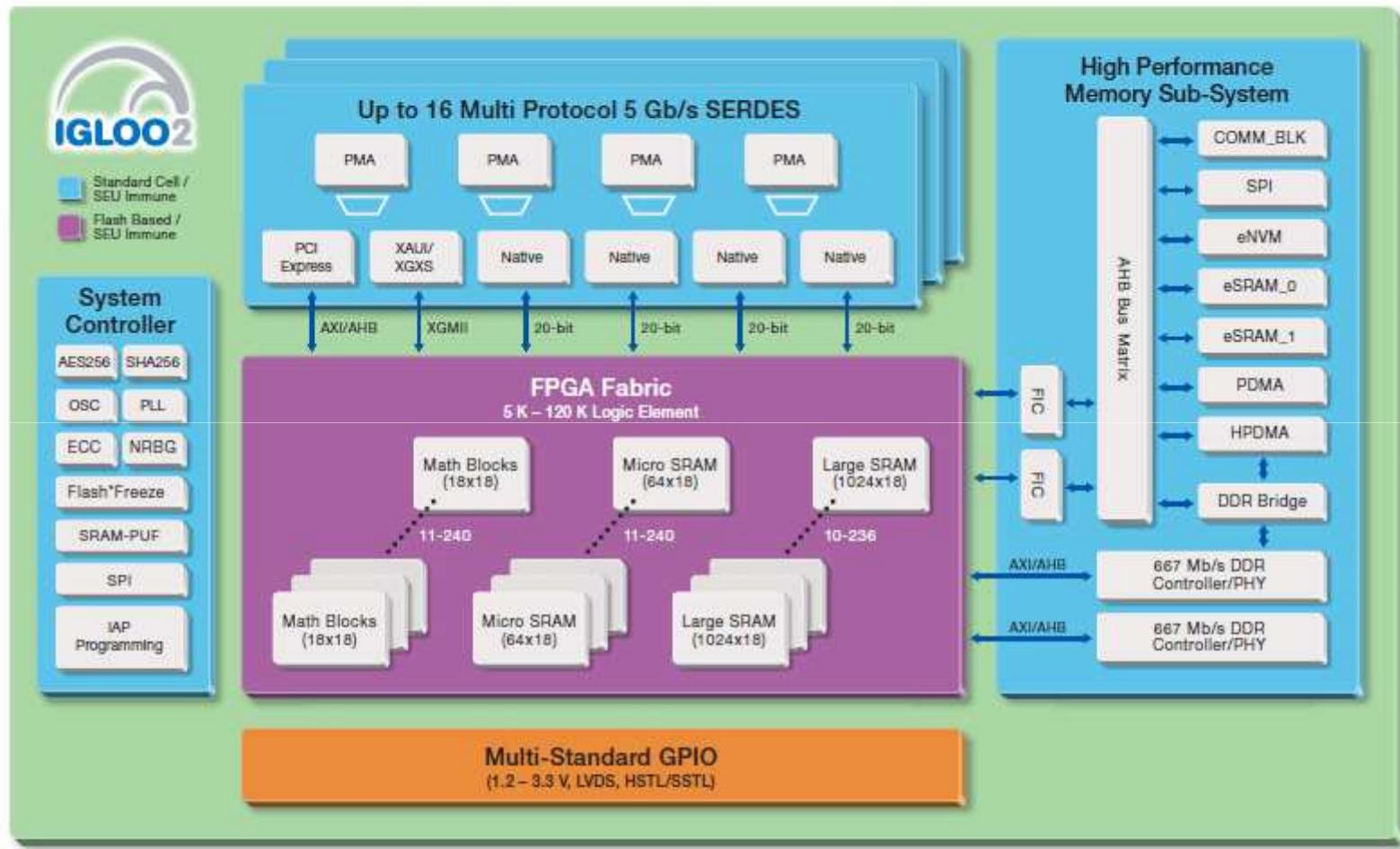


Microsemi SoC Product Roadmap

Increasing system features on differentiated flash technology



Igloo2 Architecture



Igloo2 Family

	Features	M2GL005	M2GL010	M2GL025	M2GL050	M2GL090	M2GL100	M2GL150			
Logic/DSP	Logic Modules (4-Input LUT)	6,060	12,084	27,696	56,340	86,316	99,512	146,124			
	Math Blocks (18x18)	11	22	34	72	84	160	240			
	PLLs and CCCs	2		6			8				
	SPI/HPDMA/PDMA	1 each									
	Security	AES256, SHA256, RNG					AES256, SHA256, RNG, ECC, PUF				
Memory	eNVM (K Bytes)	128	256				512				
	LSRAM 18K Blocks	10	21	31	69	109	160	236			
	uSRAM1K Blocks	11	22	34	72	112	160	240			
	eSRAM (K Bytes)	64									
	Total RAM (K bits)	255	464	656	1378	2138	3104	4552			
High Speed	DDR Controllers	1x18			2x36	1x18	2x36				
	SERDES Lanes	0	4		8	4	8	16			
	PCIe End Points	0	1		2			4			
User I/Os	MSIO (3.3V)	115	123	157	139	306	292	292			
	MSIOD (2.5V)	28	40	40	62	40	106	106			
	DDRIO (2.5V)	66	70	70	176	66	176	176			
	Total User I/O	209	233	267	377	412	574	574			

Device Offering

- Devices without transceivers
 - M2GL150
- Devices with transceivers
 - M2GL150T
- Devices with enhanced security capabilities
 - M2GL150S
- Devices with transceivers and enhanced Security
 - M2GL150TS
- S devices available in -1 Speed Grade / Industrial Temp
- Mil Temp Availability in Q1 2014
 - T, TS devices

Igloo2 Packaging Plan

Type	Package Options									
	VF400		FG484		FG676		FG896		FC1152	
Pitch (mm)	0.8		1.0		1.0		1.0		1.0	
Length x Width (mm)	17x17		23x23		27x27		31x31		35x35	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2GL005	169*	-	209*	-						
M2GL010(T)	195	4	233	4						
M2GL025(T)	195	4	267	4						
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Die and Package Rollout

Die	Package	Libero Design Support	Commercial	Industrial
M2GL005	FG484	11.0 SP1 (6/14/13)	Nov-13	Dec-13
M2GL010	FG484	11.0 SP1 (6/14/13)	Oct-13	Dec-13
M2GL025	FG484	11.0 SP1 (6/14/13)	Oct-13	Dec-13
M2GL050	FG484	11.0 SP1 (6/14/13)	Jun-13	Aug-13
M2GL090	FG484	Coming Soon	Apr-14	May-14

Die	Package	Libero Design Support	Commercial	Industrial
M2GL005	VF400	Coming Soon	Nov-13	Dec-13
M2GL010	VF400	11.0 SP1 (6/14/13)	Oct-13	Dec-13
M2GL025	VF400	11.0 SP1 (6/14/13)	Nov-13	Dec-13
M2GL050	VF400	11.0 SP1 (6/14/13)	Oct-13	Dec-13

Die	Package	Libero Design Support	Commercial	Industrial
M2GL050	FG896	11.0 SP1 (6/14/13)	Jul-13	Aug-13
M2GL090	FG676	Coming Soon	Apr-14	May-14

Die	Package	Libero Design Support	Commercial	Industrial
M2GL100	FC1152	11.0 SP1 (6/14/13)	Apr-14	May-14
M2GL150	FC1152	11.0 SP1 (6/14/13)	Mar-14	Apr-14

Competitive Landscape

Features	Microsemi IGLOO2	Xilinx Artix-7	Altera Cyclone V
Logic Elements (K)	150	131	150
Max I/O	574	300	480
Max 3.3V PCI Compliant I/O	306	300	N/A
Max SERDES Lanes	16	8	9
Max PCI Express Endpoints	4	1	2
Hard DDR3 Controllers	2	0	2
Max DSP Blocks	240	240	312
Max RAM Mbits	5	5	7
High Performance Memory Subsystem	Yes	No	No
Embedded Flash (eNVM)	Yes	No	No
Low Power	Yes	No	No
Instant-On	Yes	No	No
Security	Yes	No	No
Reliability	Yes	No	No
Power Supplies	2	3	3

Competitive Offerings Are Under Serving Key Requirements

More Resources Available on Smaller Device

IGLOO2 Higher Max I/O per LE Density

K LE	IGLOO2	Max I/O	Cyclone V-GT	Max I/O	Artix-7	Max I/O
10	M2GL010T	233	-	-	XC7A20SLT	216
25	M2GL025T	267	-	-	XC7A35SLT	216
50	M2GL050T	377	-	-	XC7A50SLT/75	300
90	M2GL090T	412	5CGTD5	336	XC7A100T	300
150	M2GL150T	574	5CGTD7	480	XC7A100T	300

K LE	IGLOO2	Max 5G SERDES Channels	Cyclone V-GT	Max 5G SERDES Channels	Artix-7 SLT	Max 5G SERDES Channels
10	M2GL010T	4	-	-	-	-
25	M2GL025T	4	-	-	XC7A20/35SLT	4
50	M2GL050T	8	-	-	XC7A50SLT/75	8
100	M2GL0100T	8	5CGTD5	6	XC7A100T	8
150	M2GL150T	16	5CGTD7	9	-	-

***Customers Forced to Buy Larger LE Count Devices
To Meet Application Requirements***

IGLOO2 Best In Class Reliability

✓ SEU Immunity

- SEU immune zero FIT flash FPGA configuration cells
- SEU protected memories: eSRAMs, eNVM



✓ SECDED Support

- Hard 667 Mbps DDR2/3 controllers with error correction



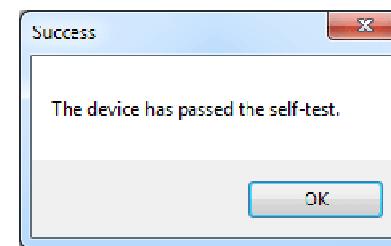
✓ Extended Junction Temperatures

- 125 °C – Mil Temp, 100 °C – Ind Temp, 85 °C – Comm Temp



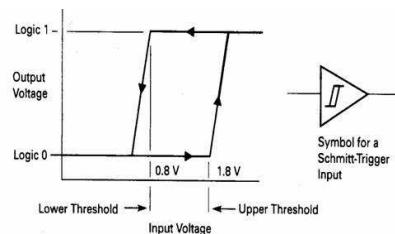
✓ On-Demand Digest

- Built-in self test on eNVM and Fabric



✓ Reliable I/Os

- Built-in hysteresis



IGLOO2 Design Security

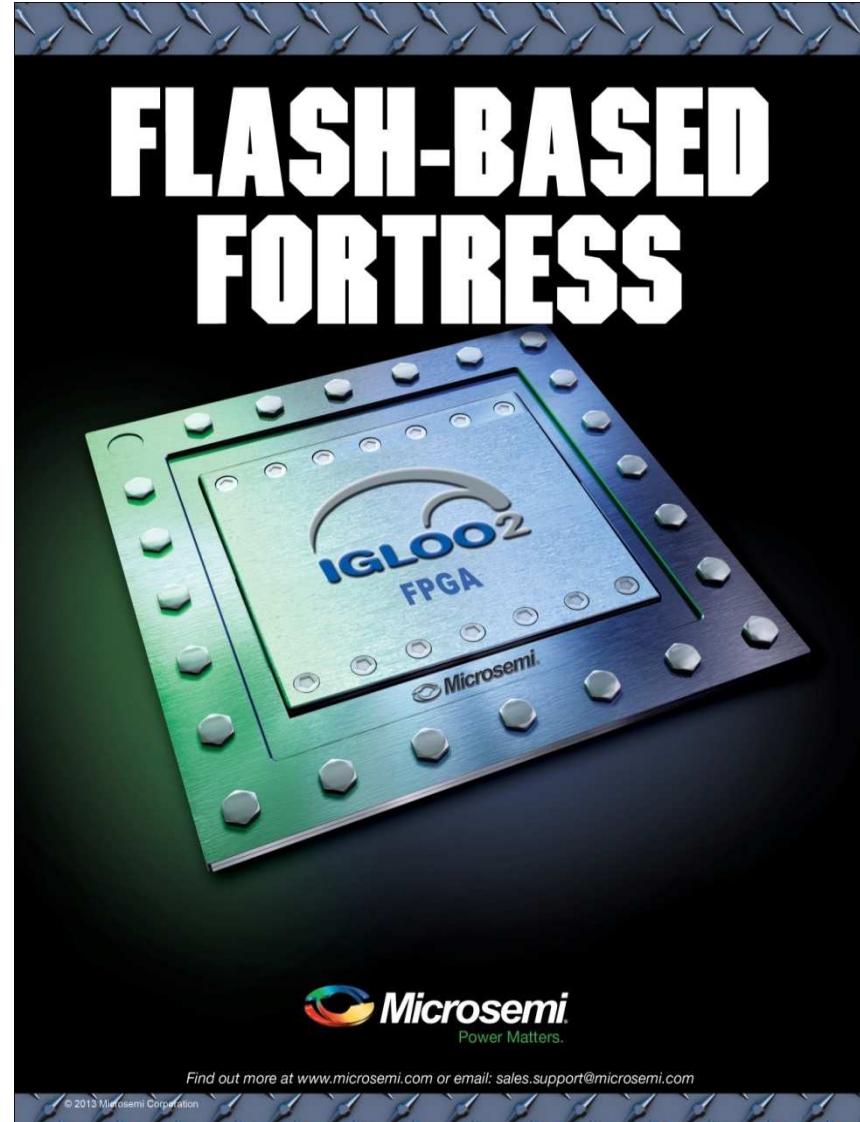
- Microsemi is the solution
 - Its Simple
 - Its Secure
 - Its Included in every device
- IGLOO2 FPGAs are the ONLY secure FPGAs in production which are easy to use.



Just because it says AES doesn't mean its Secure!



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 **Microsemi**
Power Matters.

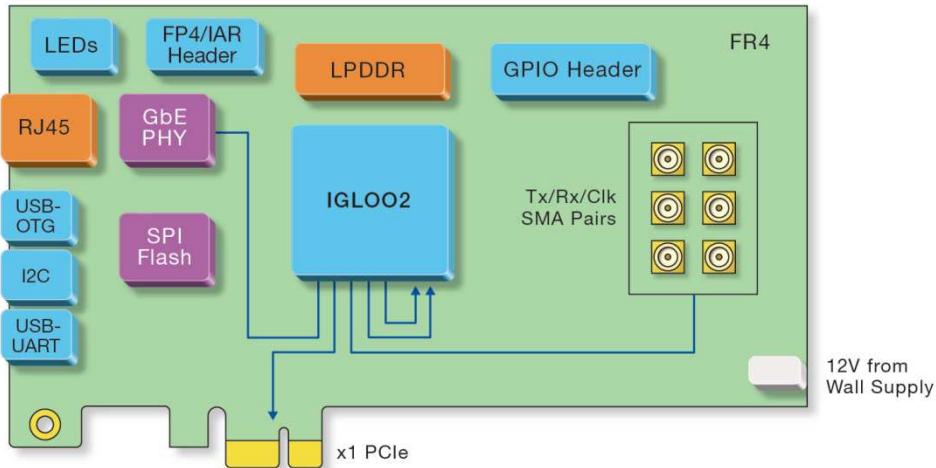
Find out more at www.microsemi.com or email: sales.support@microsemi.com

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Power Matters. 54

IGLOO2 Kit

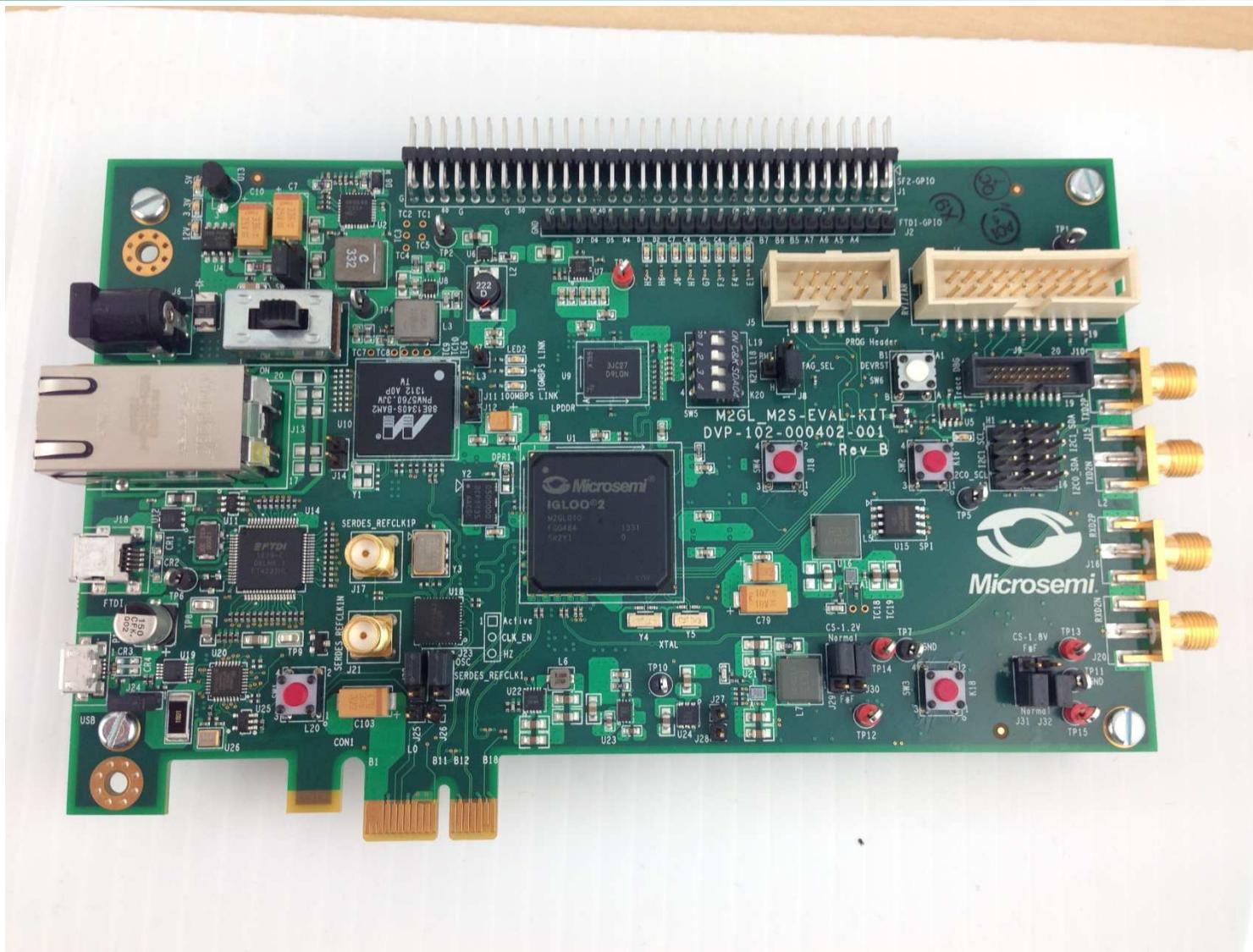
- M2GL Low-Cost Kit
 - Less than \$99 for a limited time. (~\$300 full price)
 - PCIe x1, SGMII, SMAs, and Tx->Rx Loopback SERDES Connections



Production in September

- Minimal Jumpers for Ease of Use
- LPDDR
- SPI Flash
- Connectors (USB, I2C, SPI, etc.)
- Power Sources
 - Wall
 - PCIe
 - USB

M2GL-EVAL-KIT Prototype Pictures



Thank you

