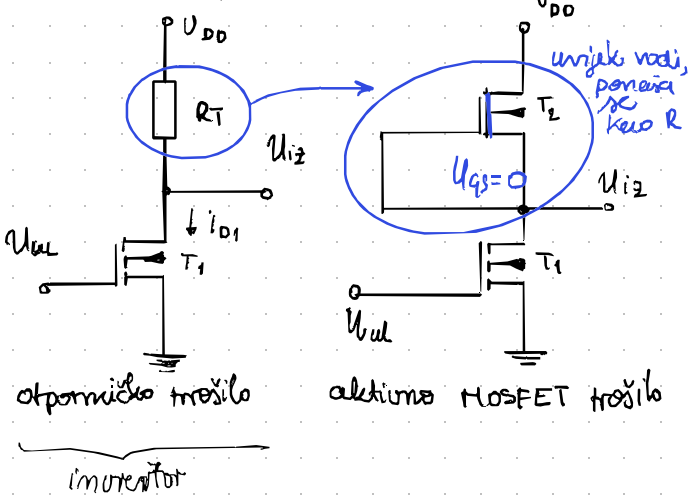
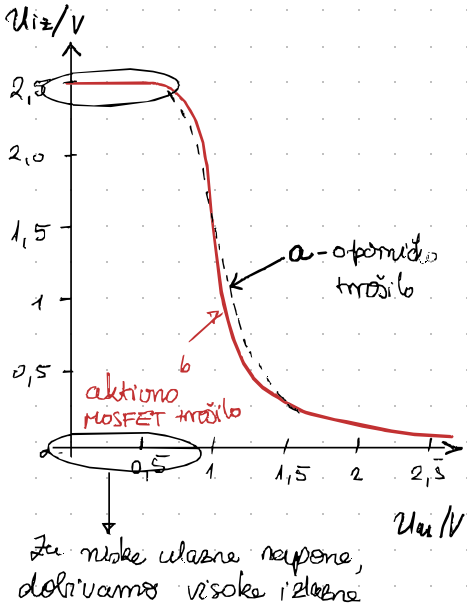
6.4. CMOS inverter

v digitalni sklopovi ~ → 0, 1

MOSFET sklopke – inverteri



unijeli vodi, ponaša se kao R

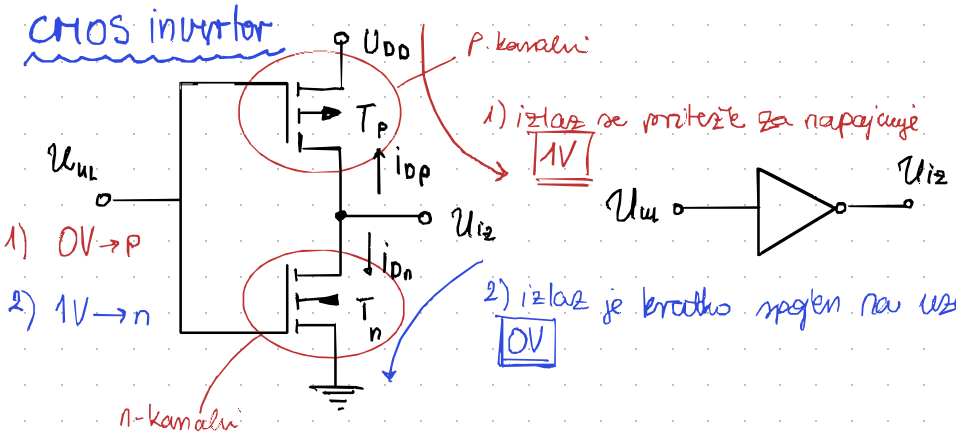


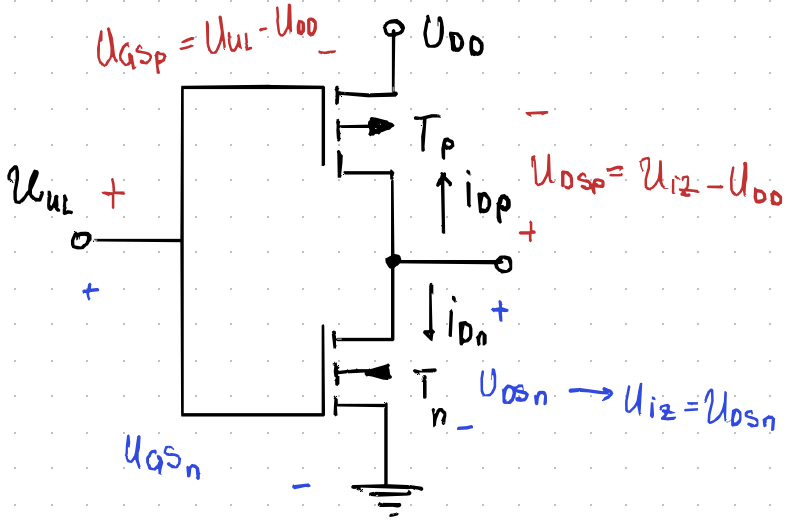
Za niske ulazne napone, dobivamo visoka izlazna

LOŠE:

- na ulazu niska razina napona [1V], na izlazu je [0]
  ↳ moguće samo ako teče struja kroz MOSFET i kroz OTPORNIK!
  → dodatna trošenje snage (pa tako i energije)

CMOS inverter





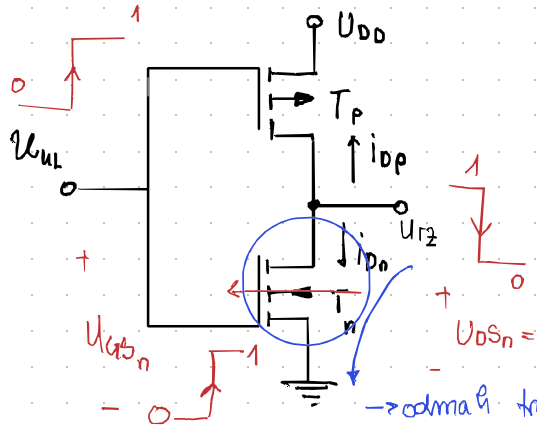
$U_{GSp} = U_{UL} - U_{DD}$

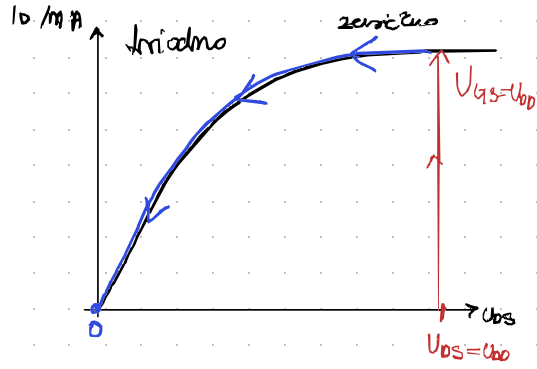
$U_{DSp} = U_{iz} - U_{DD}$

$U_{GSn} = U_{UL}$

$U_{DSn} = U_{iz}$

$i_{Dn} = -i_{DP}$





$U_{DSn} = U_{DD} \longrightarrow U_{DSn} \to 0$

→ odmah tranzistor priteže na 0

Stacionarna stanja - ulazni napon niske razine

trioda područje: $i_{Dp} = K_p (U_{GSp} - U_{GSOp}) U_{DSp}$

$$R_p = \frac{U_{DSp}}{i_{Dp}} = \frac{1}{K_p (U_{GSp} - U_{GSOp})}$$

$\sim k\Omega$

izlazni napon visoke razine (napon logičke 1)

$\longrightarrow U_1 - U_{DD}$

-II- Ulazni napon visoke razine

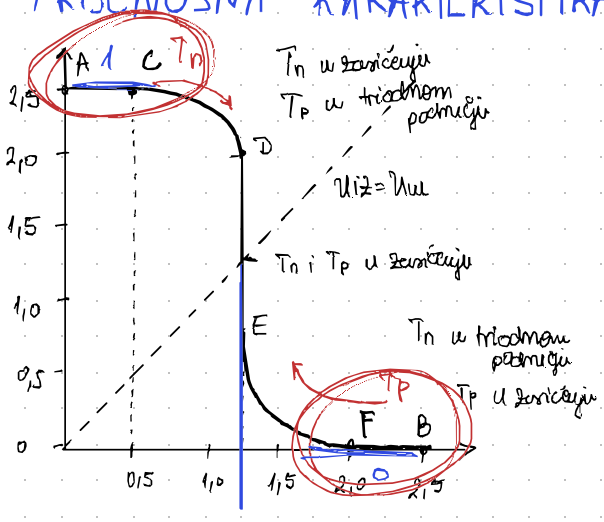
T_p ne vodi, T_n vodi - u početku triodnog područja

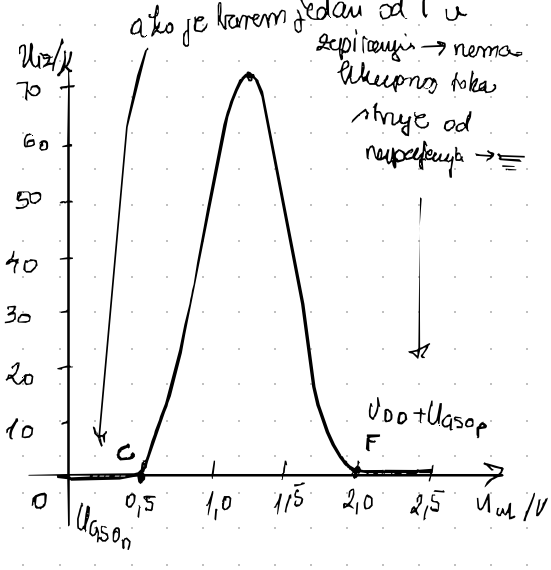
$$i_{Dn} = K_n (U_{GSn} - U_{GSOn}) U_{DSn} \qquad R_n = \frac{U_{DSn}}{i_{Dn}} = \frac{1}{K_n (U_{GSn} - U_{GSOn})}$$

izlazni napon niske razine (napon logičke 0) $U_0 \to 0$

→ ni u jednom trenu ne vode oba tranzistora

PRIJENOSNA KARAKTERISTIKA





U_{P0} - napon praga okidanja

- napon na ulazu → izlaz bio log. 0
- napon na ulazu → izlaz bio log. 1

$$U_{P0} = \frac{U_{DD}}{2}$$

Napon praga okidanja

Prag okidanja → točka u kojoj pravac $u_{iz} = u_{ul}$ siječe prijenosnu karakteristiku

Za napon praga okidanja $U_{PO} = u_{iz} = u_{ul}$ → tranzistori rade u zasićenju

$$i_{Dn} = -i_{Dp} \longrightarrow -K_n \underbrace{(U_{PO} - U_{GSon})}_{u_{GSn}}{}^2 = -K_p \underbrace{(U_{PO} - U_{DD} - U_{GSOp})}_{u_{GSp}}{}^2$$

$$\Rightarrow r = \sqrt{\frac{-K_p}{K_n}} = \pm \frac{U_{PO} - U_{GSon}}{U_{PO} - U_{DD} - U_{GSop}} > 0 !$$

za fizikalno rješenje trebamo minus → $r = \dfrac{U_{PO} - U_{GSon}}{U_{DD} - U_{PO} - U_{GSop}}$

$$\Rightarrow U_{PO} = \frac{r(U_{DD} + U_{GSOp}) + U_{GSon}}{1 + r} \xrightarrow{r} U_{PO} = \frac{U_{DD}}{2}$$

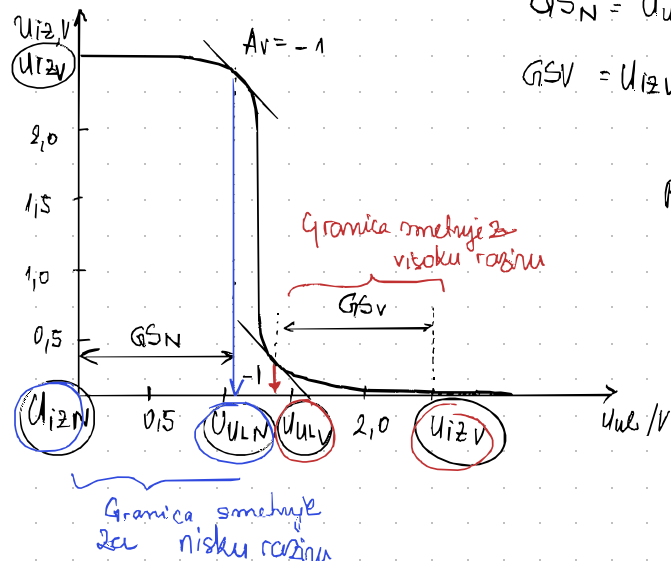
1) $r = 1$

2) $|U_{GSOp}| = |U_{GSOn}| \rightarrow U_{GSop} = -U_{GSon}$

$$\frac{1 \cdot (U_{DD} - U_{GSon}) + U_{GSon}}{2} = \frac{U_{DD}}{2} \quad \checkmark$$

→ određuje maksimalni napon za nisku razinu i minimalni napon za visoku razinu

Granice smetnje



$$GS_N = U_{ULN} - U_{izN} = U_{ULN}$$

$$GS_V = U_{izV} - U_{ULV} = U_{DD} - U_{ULV}$$

primjer:

$U_{DD} = 2{,}5\,V$

$U_{ULN} = 1{,}04\,V \quad U_{ULV} = 1{,}46\,V$

$GS_N = U_{ULN} = 1{,}04$

$GS_V = U_{DD} - U_{ULV} = 2{,}5 - 1{,}46$

$GS_V = 1{,}04$

Granice smetnje

Primjer 6.12.)

$t_{ox} = 6nm$ → za oba $U_{GSon} = -U_{GSop} = 0{,}5V$

$\mu_n = 270 cm^2/Vs$ $U_{DD} = 2{,}5V$

$\mu_p = 90 cm^2/Vs$

Sličnost: $\frac{\mu_n}{\mu_p} \approx 3$

a) duljine kanala oba tranzistora jednake: $L_n = L_p$

izračunati $\frac{W_p}{W_n}$ za T_n i T_p

+ $U_{Po} = \frac{U_{DD}}{2} = 1{,}25V$

$C_{oxn} = C_{oxp}$

U_{GSO} komplementarni → $r = 1$ za $U_{Po} = \frac{U_{DD}}{2}$ ⟹ $K_n = -K_p$

$$\frac{-K_p}{K_n} = \frac{+\mu_p \cdot C_{oxp} \frac{W_p}{L_p}}{\mu_n \cdot C_{oxn} \frac{W_n}{L_n}} = \frac{\mu_p W_p}{\mu_n W_n} = 1 \rightarrow \frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} = 3$$

(μ_n ← e^-, μ_p → šupljine)

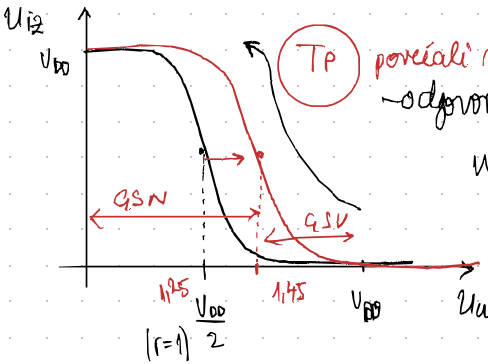
moramo raditi 3 puta veće p kanale NMOSFETE

CMOS DIG SKLOPOVI: pMOS mora biti $W_p \approx 3W_n$

b) Izračunati novu vrijednost napona praga okidanja U_{Po} ako se širina kanala tranzistora T_p u odnosu na širinu iz a) četverostruči

$$r = \sqrt{\frac{-K_p}{K_n}} = \sqrt{\frac{\mu_p W_p}{\mu_n W_n}} = \sqrt{\frac{\mu_p}{\mu_n} \cdot 3 \times 3} = 1{,}73$$

$$U_{Po} = \frac{r(U_{DD} + U_{GSOp}) + U_{GSOn}}{1 + r} = 1{,}45V \qquad U_{DD} = 2{,}5V,\ \frac{U_{DD}}{2} = 1{,}25V$$



T_p povećali smo širinu T_p

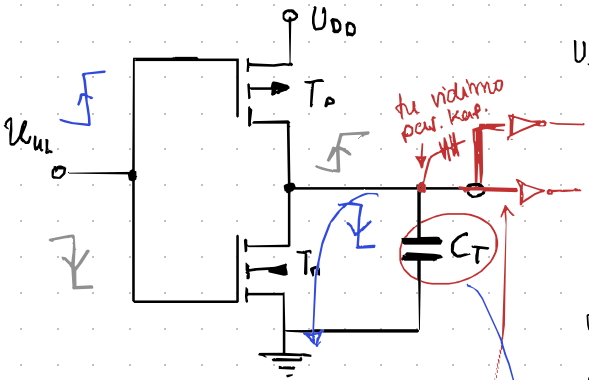
- odgovoran za primjenjivanje izlaza na visoku razinu

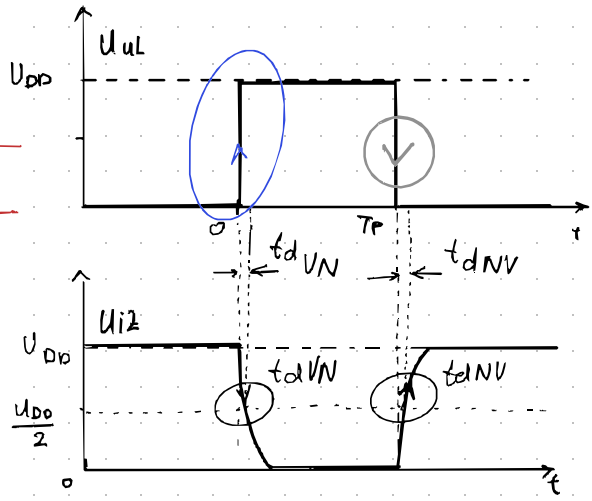
$W_p \uparrow$ $K_p \uparrow$ prijelaz učiti u zasićenje za ISTE napone!

- pomicanje p.k. udesno:

$r = 1 \rightarrow G_{SN} = G_{SV}$

Vremenski odziv

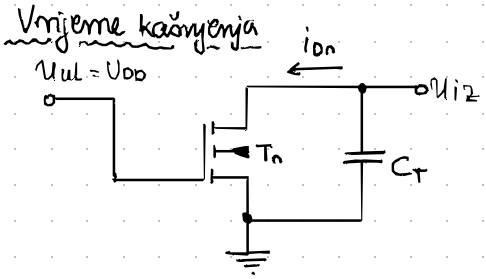


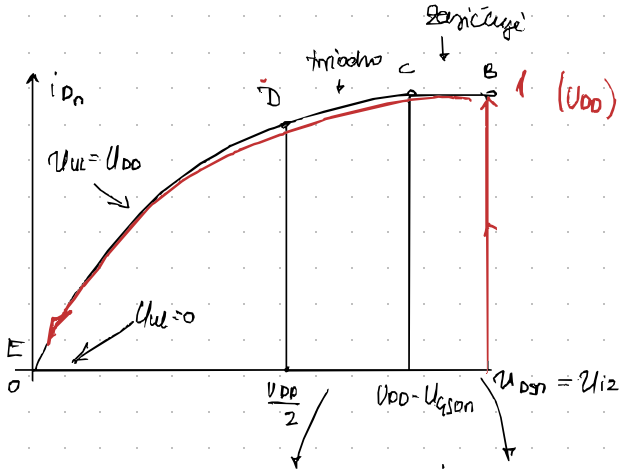


C_T -> izl. kapaciteti MOSFET-a
- parazitični kapaciteti linija
- ulazni kapaciteti sklopova spojenih na izlaz invertera

pražnjenje preko T_n.

Vrijeme kašnjenja





$$I_D = \frac{K}{2}(U_{GS} - U_{GSO})^2$$

$$i_{Dn} \sim C \cdot \frac{du}{dt} \longrightarrow i_{on} \cdot dt = -C\, dU_{iz}$$

$$t_{dVN} = -C_T \int_{U_{DD}}^{\frac{U_{DD}}{2}} \frac{dU_{iz}}{i_{Dn}(U_{iz})}$$

$$i_{on} = K_n (U_{DD} - U_{GSon}) U_{iz} - \frac{K_n}{2} U_{iz}^2$$

→ prepostavimo da je između B i D

$$i_{on} = \frac{K_n}{2}(U_{DD} - U_{GSon})^2$$

$$i_{Dn} = \frac{K_n}{2}(U_{DD} - U_{GSon})^2$$

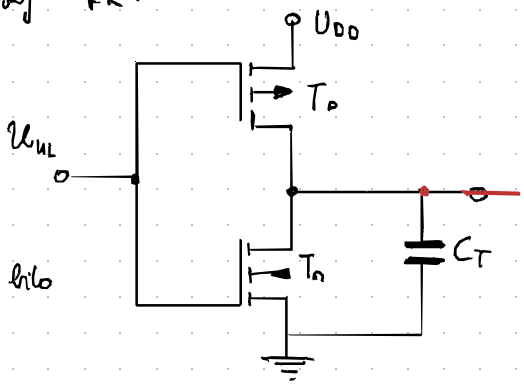
$$\Rightarrow t_{dVN} \approx \frac{C_T\left(U_{DD} - \frac{U_{DD}}{2}\right)}{\frac{K_n}{2}(U_{DD} - U_{GSon})^2} \rightarrow t_{dVN} = \frac{C_T U_{DD}}{K_n (U_{DD} - U_{GSon})^2}$$ n-kanalni

$$\rightarrow t_{dNV} = \frac{C_T U_{DD}}{-K_p (U_{DD} + U_{GSOP})^2}$$ p-kanalni

- cilj nam je da je kašnjenje što manje

→ povećavamo strujne koeficijente bla bla

Primjer 6.13) Za CMOS iz prošlog PR:



t_{dVN}=?

$C_T = 10fF$

$W_n = 2L_n = 0{,}5\mu m$

Kolika je W_p ako $L_n = L_p$ da bi t_{dNV} bilo jednako vremenu kašnjenja t_{dVN}?

t_{dVN} → ako provede n-kanalni

$$t_{dVN} = \frac{C_T U_{DD}}{K_n (U_{DD} - U_{gsoN})^2} \qquad K_n = \mu_n \cdot C_{ox} \frac{W_n}{L_n}$$

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{r,ox}}{t_{ox}} = \frac{8{,}854 \times 10^{-14} \frac{F}{cm} \cdot 3{,}9}{6 \times 10^{-7}\, cm} \qquad [F/cm^2]$$

$$C_{ox} = 576\ nF/cm^2$$

$$\rightarrow K_n = 270 \cdot \frac{cm^2}{Vs} \cdot 576 \cdot 10^{-9} \frac{F}{cm^2} \cdot 2 = 311\,\mu A/V^2$$

$$t_{dVN} = \frac{10 \times 10^{-15} \cdot 2{,}5}{311 \times 10^{-6} \cdot (2{,}5 - 0{,}5)^2} = \boxed{20.1\ ps}$$

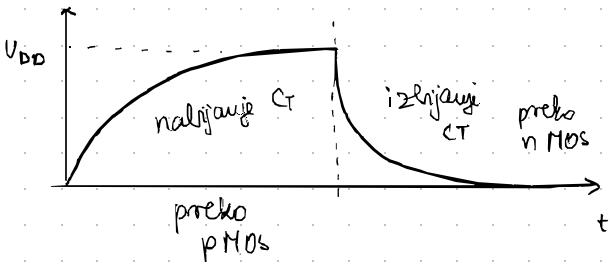
W_p=? $t_{dNV} = t_{dVN}$

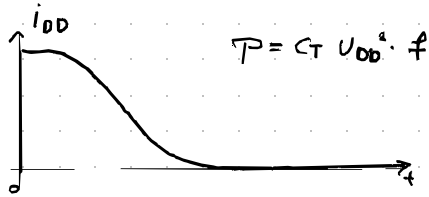
$U_{gsoN} = U_{gsoP} \rightarrow K_n = -K_p$

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} = \frac{270}{90} = 3 \rightarrow W_p = 3 \cdot W_n = 3 \cdot 0{,}5$$

$$W_p = 1{,}5\,\mu m$$

Disipacija snage





$$E_{DD} = \int_0^\infty \underbrace{i_{DD} \cdot U_{DD}}_{P(t)} \underbrace{dt}_{\cdot dt} = U_{DD} \int_0^\infty C_T \frac{du_{iz}}{dt} = C_T U_{DD} \int_0^{U_{DD}} du_{iz} = C_T \cdot U_{DD}^2$$

$$E_C = \int_0^\infty i_{DD} u_{iz}\, dt = \int_0^\infty C_T \frac{du_{iz}}{dt} u_{iz}\, dt = C_T \int_0^{U_{DD}} u_{iz} \cdot du_{iz} \Rightarrow \frac{C_T U_{DD}^2}{2}$$

pola proizvedene en. otpada na kapacitet

→ smanjivanjem ulaznog napona → P ↓ jer pada s kvadratom

$(P = C_T \cdot U_{DD}^2 \cdot f)$

Primjer 6.14)

$U_{DD} = 2{,}5V \quad C_T = 10fF \quad f = 1GHz$

$P = ?$

(1 perioda) $E_{DD} = C_T U_{DD}^2 = 10^{-14} \cdot 2{,}5^2 = \underline{62{,}5fJ}$

$P = C_T \cdot U_{DD}^2 \cdot f = E_{DD} \cdot f = \underline{62{,}5\mu W}$ ×1 cmos inverter

↳ ali to je na jednom čipiću

↳ na 1G milijun čipića to bude puno