SINTFF

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

ENTITY sintff IS PORT (
        clk : IN STD_LOGIC;
        t : IN STD_LOGIC;
        clr : IN STD_LOGIC;
        st : IN STD_LOGIC;
        q : OUT STD_LOGIC;
        qn : OUT STD_LOGIC);
end sintff;

ARCHITECTURE arch OF sintff IS
        BEGIN

                PROCESS (clk)
                        VARIABLE stanje: std_logic := '0';
                BEGIN

                        IF falling_edge (clk) THEN

                            --glavni dio
                                IF clr='1' THEN stanje := '0';
                                ELSIF st='1' THEN stanje := '1';
                                ELSIF t='1' THEN stanje := NOT stanje;
                                END IF;
                            --kraj glavni dio

                        END IF;

                        q <= stanje AFTER 10 ns;
                        qn <= not stanje AFTER 10 ns;

                END PROCESS;

        END arch;
```

ASINTFF

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

ENTITY asintff IS PORT (
        clk : IN STD_LOGIC;
        t : IN STD_LOGIC;
        clr : IN STD_LOGIC;
        st : IN STD_LOGIC;
        q : OUT STD_LOGIC;
        qn : OUT STD_LOGIC);
end asintff;

ARCHITECTURE arch OF asintff IS
```

```
    BEGIN

        PROCESS (clk, st, clr)
            VARIABLE stanje: STD_LOGIC :='0';
        BEGIN

          --GLAVNI DIO
            IF clr='1' THEN stanje:='0';
            ELSIF st='1' THEN stanje:='1';
            ELSIF falling_edge(clk) THEN IF t='1' THEN stanje:=NOT stanje; END IF;
            END IF;
          --KRAJ GLAVNI DIO

        q<=stanje AFTER 10 ns;
        qn<=stanje AFTER 10 ns;


        END PROCESS;

    END arch;
```

SEKVSKLOP

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

ENTITY sekvsklop IS PORT (
    clk : IN STD_LOGIC;
    reset : IN STD_LOGIC;
    p : IN STD_LOGIC;
    q : OUT STD_LOGIC_VECTOR (4 DOWNTO 0));
end sekvsklop;

ARCHITECTURE arch OF sekvsklop IS

    SIGNAL
        i_np_r,
        i_p_r,
        i_iq0_iq1,
        i_iq0_iq1_iq2,
        i_iq0_iq1_iq2_iq3

    : STD_LOGIC;

    SIGNAL i_q: STD_LOGIC_VECTOR (4 DOWNTO 0);

BEGIN
                --(clk,t,clr,st,q,qn)

    comp_1: ENTITY work.sintff PORT MAP (clk, '1', i_np_r, i_p_r, i_q(0), open);
    comp_2: ENTITY work.sintff PORT MAP (clk, i_q(0), reset, '0', i_q(1), open);
    comp_3: ENTITY work.sintff PORT MAP (clk, i_iq0_iq1, reset, '0', i_q(2), open);
```

```
        comp_4: ENTITY work.sintff PORT MAP (clk, i_iq0_iq1_iq2, reset, '0', i_q(3), open);
        comp_5: ENTITY work.sintff PORT MAP (clk, i_iq0_iq1_iq2_iq3, reset, '0', i_q(4), open);

        i_np_r <= NOT p AND reset;
        i_p_r <= p AND reset;
        i_iq0_iq1 <= i_q(0) AND i_q(1);
        i_iq0_iq1_iq2 <= i_iq0_iq1 AND i_q(2);
        i_iq0_iq1_iq2_iq3 <= i_iq0_iq1_iq2 AND i_q(3);

        q(0) <= i_q(0);
        q(1) <= i_q(1);
        q(2) <= i_q(2);
        q(3) <= i_q(3);
        q(4) <= i_q(4);

END arch;
```