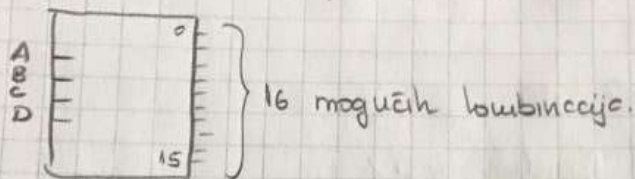


- ① Dekoderom želimo realizirati funkciju.
 n ulaza, 2^n izlaza



sklopom ili biramo!
pozbrajamo sve.

$C_1, C_2, a, C_4, b, c, d$

$$C_2 = a \oplus c \oplus d$$

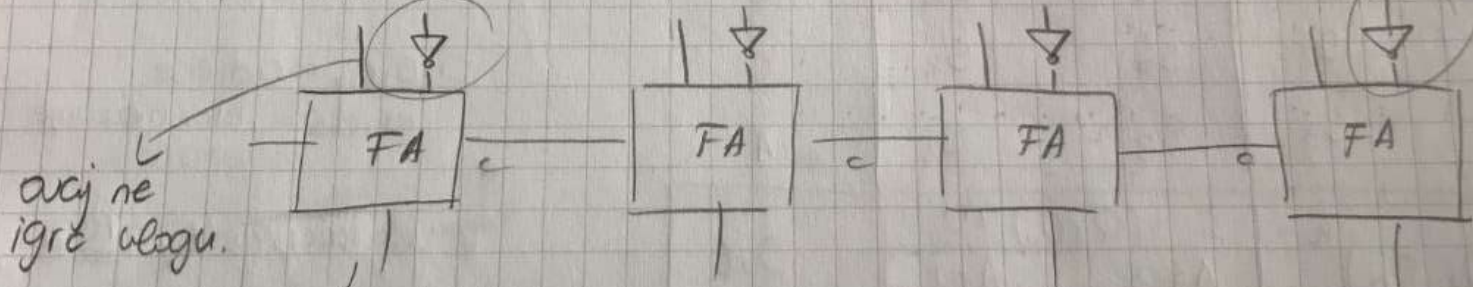
→ to je poredak paritet

mi želimo napravi

→ spojimo koje očemo! tj. komplemente čemo!

TREBAO BIN. DEKODER.
3/8

- ② 4 potpuno zbrajala } oduzimamo.
4 invertora

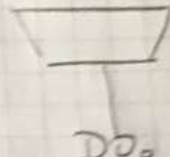
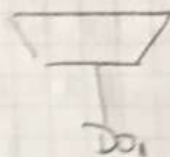
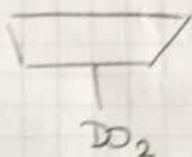
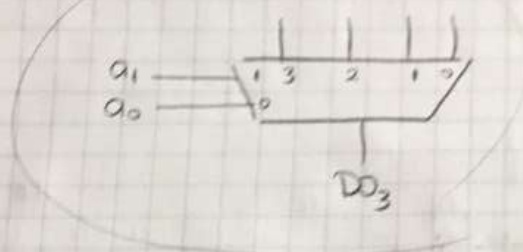


Cod 1, 2, 3, 4,

→ $4 \cdot t_{2c \text{ carry}}$
→ $4 \cdot t_{\text{invertora}}$

$4 \cdot 10$
+
30
= 70

③ 4 MUX-a



	3	2	1	0
00	3	2	1	0
01	0	3	2	1
10	2	1	0	3
11	3	3	2	1

nema posmaka. pojavljuje se isti podatak! $d_0 = DI_3$

krozi u desno za 1 desno $d_1 = DI_0$

krozi u lijevo za 1 lijevo $d_2 = DI_2$

antimehizmu \rightarrow DESNO povećava se 1. bit. $d_3 = DI_3$

⑥ ROM kao generator funkcije

B	C	D	A=0	A=1	A=0	A=1	
a_2	a_1	a_0	d_3	d_2	d_1	d_0	
0	0	0	0	0	1	1	3
0	0	1	0	1	1	0	6
0	1	0	1	0	0	0	8
0	1	1	0	1	0	0	4
1	0	0	0	1	1	1	7
1	0	1	0	1	0	0	4
1	1	0	0	1	1	1	7
1	1	1	1	1	0	1	D

$$f = \overline{A}\overline{B}C\overline{D} + BCD + AD + AB$$

$\rightarrow A$

7

PLA \rightarrow programirajiv - može se programirati - možemo konstat više puta

$$f = \sum m(0, 1, 4, 5, 14, 15)$$

$$g = \sum m(2, 3, 4, 5, 14, 15)$$

$$h = \sum m(0, 1, 2, 3, 14, 15)$$

f

		AB			
		00	01	11	10
CD	00	1	1		
	01	1	1		
	11			1	
	10			1	

g

		AB			
		00	01	11	10
CD	00		1		
	01		1		
	11	1		1	
	10	1		1	

h

		AB			
		00	01	11	10
CD	00	1			
	01	1			
	11	1		1	
	10	1		1	

D se poništio

ukupno 4 implikanta \Rightarrow to su izlazi polja I
ulazi A, B, C
izlazne funkcije = 3

8

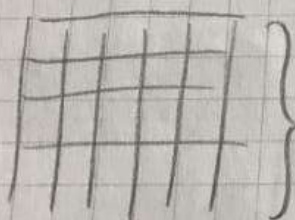
Kapacitet je 2^{12} bita

$D_7 \dots D_0 \Rightarrow$ riječ \Rightarrow 8 bita

LOGIČKA RIJEČ - bitanost

2D organizacija \rightarrow raspoređeno \rightarrow s MUX-om biramo logičku riječ

- adresni dekodera 64 izlaza \rightarrow adresira riječi \Rightarrow FIZIČKE RIJEČI



64 redaka ima

64 kockice

$$2^{12} : 2^6 = x$$

$$2^6 = x$$

$$x = 64$$

- odjednom adresiramo red od 64

a uau ide 8 jedini po jedini

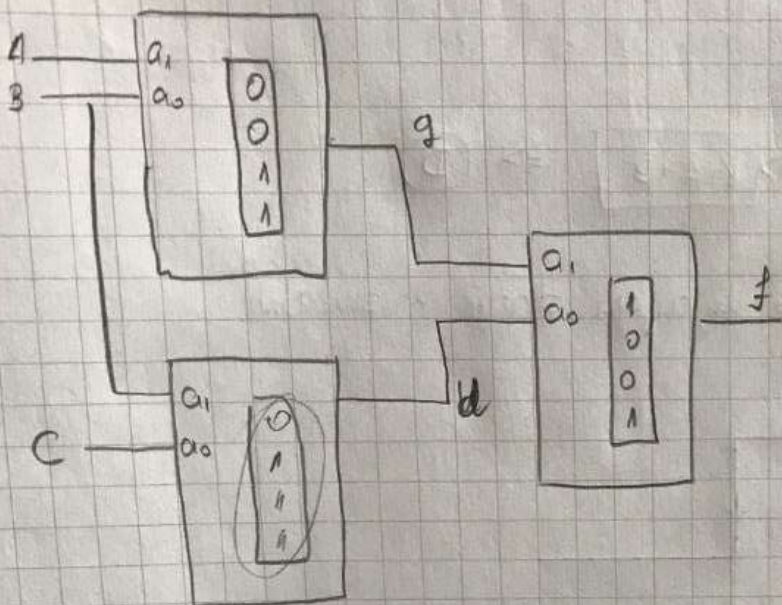
$$\text{u FIZIČKOJ IH JE } 8 \Rightarrow \frac{64}{8} = 8$$

(E)

FPGA

Gledamo samo LuT → Look Up Table.

$$f(A, B, C) = \bar{A}\bar{B}\bar{C} + AB + AC$$



$$g = A$$

$$f = \text{XOR} = \bar{g}\bar{d} + gd = \overline{g \oplus d}$$

$$f = \underbrace{\bar{A}\bar{d}}_{\bar{B}\bar{C}} + \underbrace{Ad}_{(B+C)}$$

$$d = B + C$$

$$\bar{d} = \bar{B}\bar{C}$$

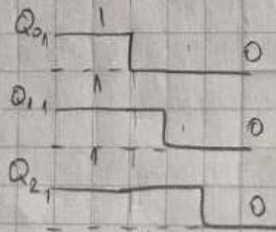
-C

10

A → b-broj → 3 bita

stanje \emptyset
↑
127

kad se dekodira bilo se tranzijentnih pogrešaka
dekodiranje gube
↓
privremeno



→ druge prebacuje kasni!

↓
0 0
1 1
7 6 4 → DVIJE POGREŠKE

11

$$Q_{n+1} = \bar{Q}_n \bar{B} + Q_n AB$$

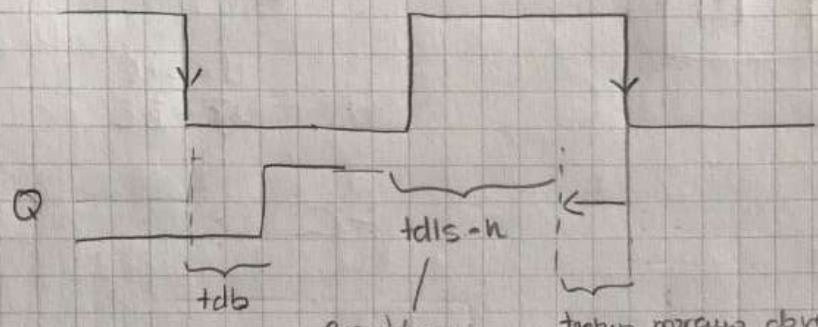
ABQⁿ | Qⁿ⁺¹ | JK

$$Q_{n+1} = \bar{K} Q_n + J \bar{Q}_n$$

$$J = \bar{B} \quad K = AB \Rightarrow K = \bar{A} + \bar{B} \Rightarrow \textcircled{D}$$

12

32 bistabla → isporrems uijeyaju stauje → SINCRONI



Esq sklopovi tsetup moramo obresh odredeni podatak. more bit stabilan. da dvedemo novi CP

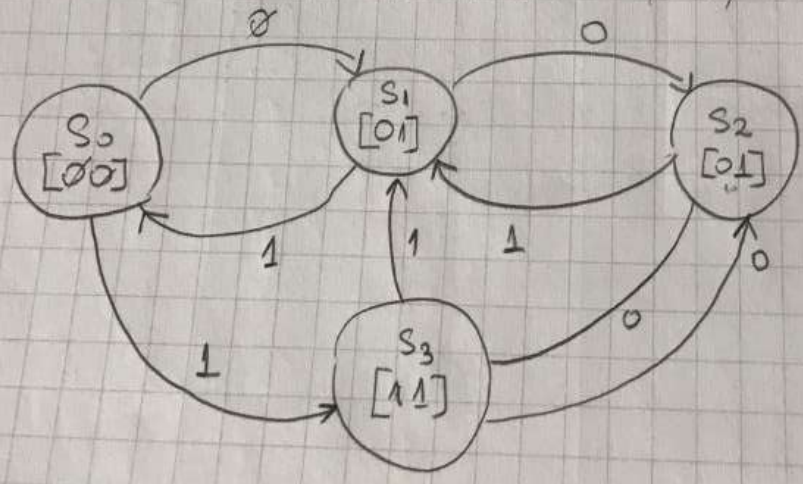
$$\frac{1}{12.5 \text{ MHz}} \rightarrow \text{odluameus tdb, tdis, f}$$

$$\frac{1}{12.5 \cdot 10^6} = tdb + tsetup + n \cdot tdis$$

$$\frac{1}{12.5 \cdot 10^6} - tdb - tsetup = n \cdot tdis$$

13

Automat izveden JK bistabilima, X, binamo kodirauje, K₀ = 2



Q^n	Q^{n+1}	Z	$(Q_1 Q_0)^n$	$(Q_1 Q_0)^{n+1}$
S_0	$X=0$ $S_1=00$	$X=1$ S_3		
S_1	$S_2=01$	S_0		
S_2	S_3	S_1		
S_3	S_2	S_1		

$X(Q_1 Q_0)^n$	$(Q_1 Q_0)^{n+1}$	SET J_0	RSET K_0	$J_1 K_1$
0 00	0 1	1	X	
0 01	1 0	X	1	
0 10	1 1	1	X	
0 11	1 0	X	1	
1 00	1 1	1	X	
1 01	0 0	X	1	
1 10	0 1	1	X	
1 11	0 1	X	0	

J	K	Q^n	Q^{n+1}
0	0	0,1	Q^n
0	1	0,1	0
1	0	0,1	1
1	1	0,1	$\overline{Q^n}$

Q_0	Q_1	Q_2	Q_3
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

14

međi
1024 x 8 bita.

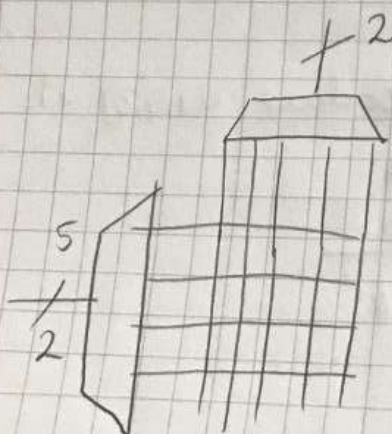
BD org.

ulazi na dekoderni?

→ 3Dm se smanjuje
dehoder

→ postigli smo 2x manje izlaza.

1024 → DESET BITOVA ZA TE RIJEČI



→ ukupno 4 u svakom 2^n

izlaza ukupno $2 \cdot 2^5 = 2^6$

→ ukupno 10, ne svakom 5

15

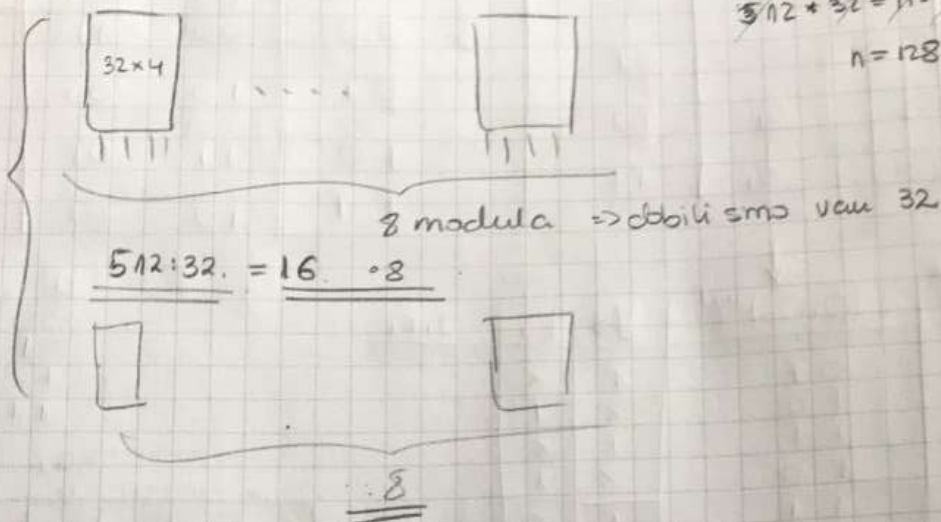
Moramo ostaviti mem 512 x 32

blokovi su 32 x 4

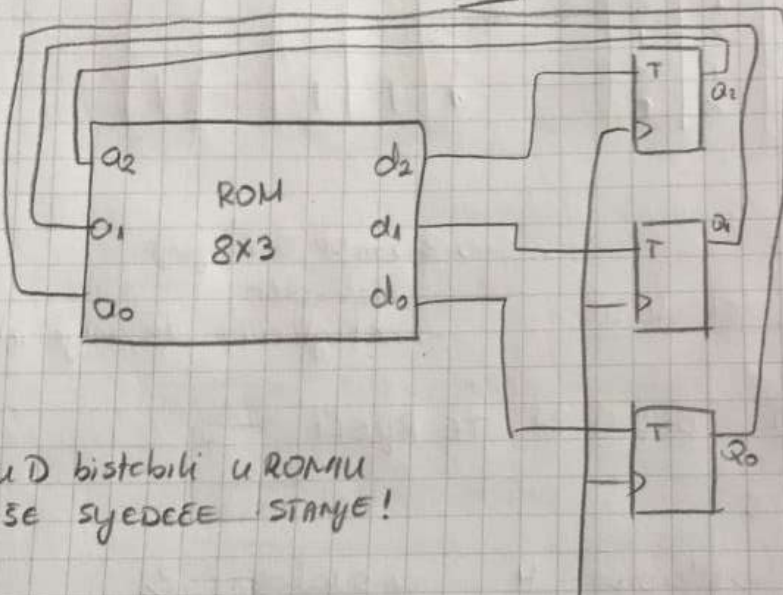
$$512 : 32 = n \cdot 32 \cdot 4$$

$$n = 128$$

16



17



ROM

npr. register s nekim
stanjem sve do uvođenja
neke adrese odredenoj
se stanjem i kao
pročitati sig. ulaz

Dasu D bistabili u ROMU
piše sigurno stanje!

Zadano 0, 1, 5, 3, 4, 1

a_2 a_1 a_0	$(Q_2 Q_1 Q_0)^{CP_{n+1}}$			d_2 d_1 d_0
Q_2 Q_1 Q_0				T_2 T_1 T_0
0 0 0	1	1	1	1 1 1
0 0 1	0	0	0	
0 1 0	1	0	0	
0 1 1	0	1	0	
1 0 0	0	0	1	
1 0 1	0	1	1	1 1 0
1 1 0	0	0	0	1 1 0
1 1 1	1	0	1	0 1 0

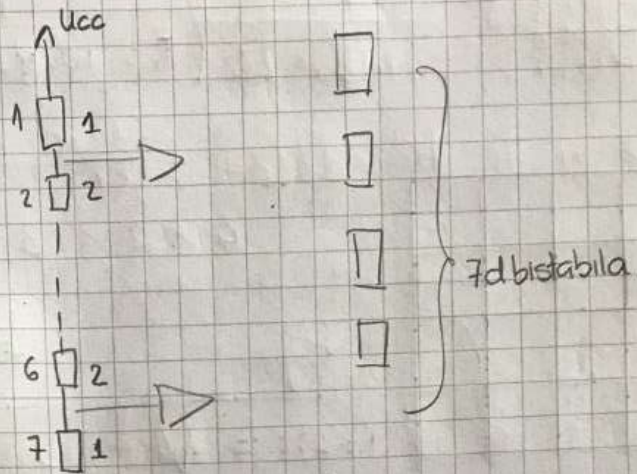
SIGURAN
START ←

19

7 komparatora

$U_{REF} = 7V$

$U_a = 0,9$



$$2^N - 1 \text{ podruge} \Rightarrow 2^7 - 1 \Rightarrow \underline{127}$$

7V referenlna

1V = podruge

$U_a \Rightarrow 0,9V$ $\rightarrow 1$

Temometarski $\rightarrow 1 \rightarrow B$

20

n bitni DA pretvornik

težinski raspoređeni

