

Lab 11

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1 Executive Summary

This lab had three parts: creating the Write Back stage, finishing the complete datapath, and then testing the datapath with code that performs a simple division. For the Write Back stage, a new module did not have to be created, a mux was simply added to the current datapath module. The division test did not require a new module to be created either, machine code for the division simply had to be created and implemented. All three parts of the lab were successful.

2 Test Report

To verify operation of these modules, this lab required two test benches.

1. Datapath Test Bench
2. Division Test Bench

2.1 Datapath Test Bench

The Datapath Test Bench contains:

1. Inputs
 - (a) reset - reset button that sets PC source to 0
2. Outputs
 - (a) read_data1 - data stored in read register 1
 - (b) read_data2 - data stored in read register 2
 - (c) write_data - the output of the Write Back stage

2.2 Division Test Bench

The Division Test Bench contains:

1. Inputs
 - (a) reset - reset button that sets PC source to 0
2. Outputs
 - (a) read_data1 - data stored in read register 1
 - (b) read_data2 - data stored in read register 2
 - (c) write_data - the output of the Write Back stage

Figure 1: Expected Results of the Datapath test.

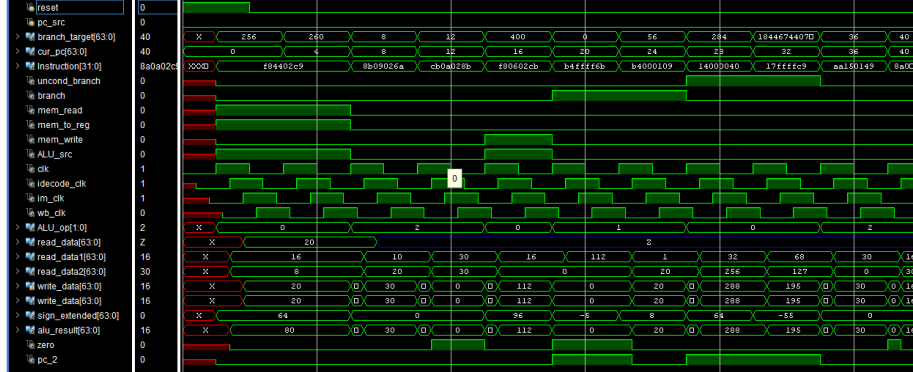
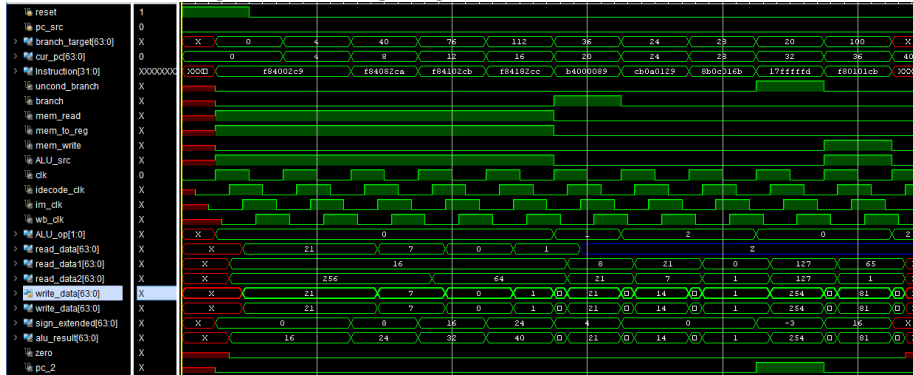


Figure 2: Timing diagram for the Division test.



3 Code Appendix

Listing 1: Verilog code for testing a register.

```

`include "definitions.vh"

module datapath;

    reg reset, pc_src;
    wire [WORD-1:0] branch_target, cur_pc;
    wire [INSTR_LEN-1:0] Instruction;
    wire uncond_branch, branch, mem_read, mem_to_reg, mem_write, ALU_src;
    wire clk, fetch_clk, idecode_clk, im_clk, wb_clk; // clkplus1, clkplus2, clkplus3
    wire [1:0] ALU_op;
    wire [WORD-1:0] read_data, read_data1, read_data2, write_data, sign_extended;

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wire [‘WORD-1:0] alu_result;
wire zero , pc_2;

    //fetch takes 2ns to complete. So clk and clkplus1 are used in fetch
    oscillator r_clk(.clk(clk));
    delay #(.DELAYAMT(2)) ClkPlus2(.a(clk), .a_delayed(idecode_clk));
//write clk
//    delay #(.DELAYAMT(3)) ClkPlus3(.a(clk), .a_delayed(clkplus3));
///
//    delay #(.DELAYAMT(4)) ClkPlus4(.a(clk), .a_delayed(clkplus4));
//    delay #(.DELAYAMT(5)) ClkPlus5(.a(clk), .a_delayed(clkplus5));
delay #(.DELAYAMT(4)) ClkPlus6(.a(clk), .a_delayed(im_clk));
//
delay #(.DELAYAMT(6)) ClkPlus8(.a(clk), .a_delayed(wb_clk));
//

    fetch fetch_mod(.clk(clk),
                    .reset(reset),
                    .branch_target(branch_target),
                    .pc_src(pc_src),
                    .instruction(instruction),
                    .cur_pc(cur_pc));

    iDecode decode_mod(
        .write_data(write_data),
        .instruction(instruction),
        .uncond_branch(uncond_branch),
        .branch(branch),
        .mem_read(mem_read),
        .mem_to_reg(mem_to_reg),
        .mem_write(mem_write),
        .ALU_src(ALU_src),
        .read_clk(idecode_clk),
        .write_clk(wb_clk),
        .ALU_op(ALU_op),
        .read_data1(read_data1),
        .read_data2(read_data2),
        .sign_extended(sign_extended));

    iExecute execute_mod(
        .pc_in(cur_pc),
        .read_data1(read_data1),
        .read_data2(read_data2),
        .sign_extend(sign_extended),
        .opcode(instruction[31:21]),

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        .alu_op(ALU_op),
        .alu_src(ALU_src),
        .alu_result(alu_result),
        .zero(zero),
        .branch_target(branch_target));

    iMemory memory_mod(
        .im_clk(im_clk),
        .alu_result(alu_result),
        .read_data2(read_data2),
        .mem_read(mem_read),
        .mem_write(mem_write),
        .zero(zero),
        .branch(branch),
        .uncondbranch(uncond_branch),
        .read_data(read_data),
        .pc_src(pc_2));

    iWrite_back writeback_m(.read_data(read_data),
        .alu_result(alu_result),
        .MentoReg(mem_to_reg),
        .write_data(write_data));

initial
    begin
        reset = 1;
        pc_src = 0; #10
        reset = 0; #100
        //      write_data = 20; #10;
        //      write_data = 30; #10;
        //      write_data = 0; #10;
        //      write_data = 1234; #50;
        //      write_data = 30; #10;
        //      write_data = 16; #6;

        $finish;
    end

endmodule

```