Lab 13

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1 Executive Summary

The goal of the lab is adding the register buffers between each stage and get a simple pipeline working and then implement the 10 instruction (NOP doesn't count in). In this lab, the iFetch, iDecode, iExecute, Memory and Writeak stages are all connected together. the pipeline buffers are added between each stage based on the buffer table.NOP instruction are added because there is no dataforwarding and hazard detection. The lab was successful.

2 Test Report

To verify operation of the pipeline, this lab requires 1 test bench.

1. Pipeline simulation

2.1 Pipeline Test Bench

The Pipeline Test Bench contains:

1. Inputs
   (a) branch_target - branch address
   (b) pc_src - the control of branch mux
   (c) reset - set the current pc to be 0
2. Outputs
   (a) control signals that stored in buffer

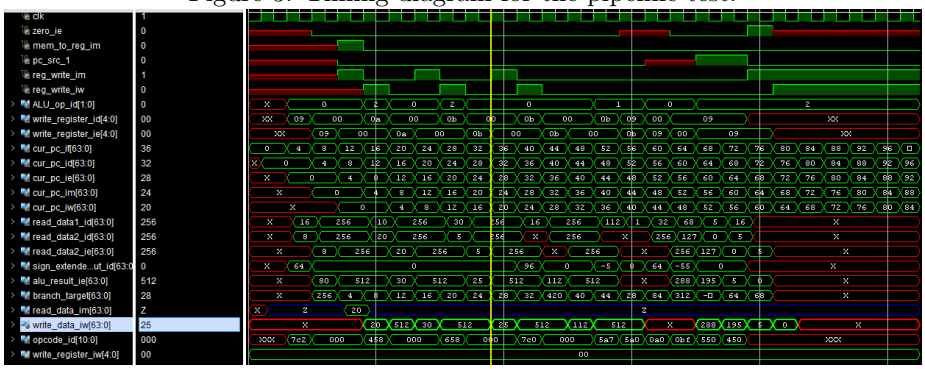
Figure 1: Piepline buffer table.

Fetch				Decode				Execute				Memory				Write Back			
Input	Src	Output	Dst	Input	Src	Output	Dst	Input	Src	Output	Dst	Input	Src	Output	Dst	Input	Src	Output	Dst
pc_src	IM													pc_src	IF				
branch_target	IE									branch_target	IF								
		cur_pc_if	ID	cur_pc_if	IF	cur_pc_id	IE	cur_pc_id	ID	cur_pc_ie	IM	cur_pc_ie	IE	cur_pc_im	IW				
		instruction_if	ID	instruction_if	IF														
				write_data_iw	IW													write_data_iw	ID
				write_register_iw	IW	write_register_id	IW	write_register_id		write_register_ie		write_register_ie		write_register_im		write_register_im	ID	write_data_iw	ID
				reg_write_iw	IW	reg_write_id	IW	reg_write_id		reg_write_ie		reg_write_ie		reg_write_im		reg_write_im	ID	reg_write_iw	ID
						sign_extended_output_id	IE	sign_extended_output_id	ID										
						uncondbranch_id	IM	uncondbranch_id		uncondbranch_ie		uncondbranch_ie	ID						
						branch_id	IM	branch_id		branch_ie		branch_ie	ID						
						mem_read_id	IM	mem_read_id		mem_read_ie		mem_read_ie	ID						
						mem_to_reg_id	IW	mem_to_reg_id	ID	mem_to_reg_ie	IW	mem_to_reg_ie	ID	mem_to_reg_im	IW	mem_to_reg_im	ID		
						alu_op_id	IE	alu_op_id	ID										
						mem_write_id	IM	mem_write_id		mem_write_ie		mem_write_ie	ID						
						alu_src_id	ID	alu_src_id	ID										
						read_data1_id	IE	read_data1_id	ID										
						read_data2_id	IE/IM	read_data2_id	ID	read_data2_ie		read_data2_ie	ID						
						opcode_id	IE	opcode_id	ID										
										alu_result_ie	IM	alu_result_ie	IE						
										zero_ie	IM	zero_ie	IE						
														read_data_im	IW	read_data_im	IM		

Figure 2: Expected Results of the pipeline test.

	Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6	Instruction 7	Instruction 8	Instruction 9	Instruction 10
Instruction	LDUR X9, [X22, #64]	ADD X10, X19, X9	SUB X11, X20, X10	STUR X11, [X22, #96]	CBZ X11, -5	CBZ X9, 8	B 64	B -55	ORR X9, X10, X21	AND X9, X22, X10
Machine Instruction (hex)	F84402C9	8B09026A	CB0A028B	F80602CB	B4FFFF6B	b4000109	14000040	17FFFFC9	AA150149	8A0A02C9
opcode (binary)	11111000010	10001011000	11001011000	11111000000	10110100	10110100	000101	000101	10101010000	10001010000
sign_extended_output (hex)	0000000000000040	0000000000000000	0000000000000000	0000000000000060	FFFFFFFFFFFFFFFB	0000000000000008	0000000000000040	FFFFFFFFFFFFFFC9	0000000000000000	0000000000000000
reg2_loc	0	0	0	1	1	1	0	0	0	0
branch	0	0	0	0	1	1	0	0	0	0
mem_read	1	0	0	0	0	0	0	0	0	0
mem_to_reg	1	0	0	0	0	0	0	0	0	0
alu_op	00	10	10	00	01	01	00	00	10	10
mem_write	0	0	0	1	0	0	0	0	0	0
alu_src	1	0	0	1	0	0	0	0	0	0
reg_write	1	1	1	0	0	0	0	0	1	1
uncondbranch	0	0	0	0	0	0	1	1	0	0
write_data (decimal)	20	30	0	X	X	X	X	X	30	16
read_data1 (decimal)	16	10	30	16	X	X	X	X	30	16
read_data2 (decimal)	X	20	5	0	0	20	X	X	0	30
branch_target	X	4	8	396	-4	52	280	-192	32	36
alu_result	80	30	0	112	0	20	X	X	30	16
zero	0	0	1	0	1	0	0	0	0	0

Figure 3: Timing diagram for the pipeline test.



3 Code Appendix

Listing 1: Verilog code of piepline.

```
`include "definitions.vh"

module pipeline;

    reg reset, pc_src;
    wire [`INSTR_LEN-1:0] instruction_if;
    wire uncond_branch_id, uncond_branch_ie,
         branch_id, branch_ie,
         mem_read_id, mem_read_ie,
         mem_to_reg_id, mem_to_reg_ie,
         mem_write_id, mem_write_ie,
         reg_write_id, reg_write_ie,
         ALU_src_id, clk,
         zero_ie, mem_to_reg_im, pc_src_1,
         reg_write_im, reg_write_iw;
    wire [1:0] ALU_op_id;
    wire [4:0] write_register_id, write_register_ie;
         // Future
         /* write_register_im,
         write_register_iw*/
    wire [`WORD-1:0]
         cur_pc_if, cur_pc_id, cur_pc_ie, cur_pc_im, cur_pc_iw,
         read_data1_id,
         read_data2_id, read_data2_ie,
         sign_extended_output_id,
         alu_result_ie,
         branch_target,
         read_data_im,
         write_data_iw;
    wire [10:0] opcode_id;
    // Temporary Registers for Simulation

    reg [4:0] write_register_iw;

    // Base Clock
    oscillator r_clk(.clk(clk));

    // Fetch Stage
    fetch fetch_mod(
        .clk(clk),
        .reset(reset),
        .branch_target(branch_target),
        .pc_src(pc_src),
        .instruction(instruction_if),
```

```
        .cur_pc(cur_pc_if));

    // Decode Stage
    iDecode decode_mod(
        .cur_pc_in(cur_pc_if),
        .cur_pc_out(cur_pc_id),
        .write_data(write_data_iw),
        .write_register_in(write_register_iw),
        .write_register_out(write_register_id),
        .reg_write_in(reg_write_iw),
        .reg_write_out(reg_write_id),
        .instruction(instruction_if),
        .uncond_branch(uncond_branch_id),
        .branch(branch_id),
        .mem_read(mem_read_id),
        .mem_to_reg(mem_to_reg_id),
        .mem_write(mem_write_id),
        .ALU_src(ALU_src_id),
        .write_clk(clk),
        .ALU_op(ALU_op_id),
        .read_data1(read_data1_id),
        .read_data2(read_data2_id),
        .sign_extended_output(sign_extended_output_id),
        .opcode(opcode_id));

    iExecute execute_mod(
        .clk(clk),
        .pc_in(cur_pc_id),
        .pc_out(cur_pc_ie),
        .write_register_in(write_register_id),
        .write_register_out(write_register_ie),
        .reg_write_in(reg_write_id),
        .reg_write_out(reg_write_ie),
        .uncond_branch_in(uncond_branch_id),
        .uncond_branch_out(uncond_branch_ie),
        .branch_in(branch_id),
        .branch_out(branch_ie),
        .mem_read_in(mem_read_id),
        .mem_read_out(mem_read_ie),
        .mem_to_reg_in(mem_to_reg_id),
        .mem_to_reg_out(mem_to_reg_ie),
        .mem_write_in(mem_write_id),
        .mem_write_out(mem_write_ie),
        .read_data1(read_data1_id),
        .read_data2_in(read_data2_id),
        .read_data2_out(read_data2_ie),
```

```
        .sign_extend(sign_extended_output_id),
        .opcode(opcode_id),
        .alu_op(ALU_op_id),
        .alu_src(ALU_src_id),
        .alu_result(alu_result_ie),
        .zero(zero_ie),
        .branch_target(branch_target));


    iMemory memory_mod(
        .im_clk(clk),
        .pc_in(cur_pc_ie),
        .pc_out(cur_pc_im),
        .alu_result(alu_result_ie),
        .read_data2(read_data2_ie),
        .mem_read(mem_read_ie),
        .mem_write(mem_write_ie),
        .mem_to_reg_in(mem_to_reg_ie),
        .mem_to_reg_out(mem_to_reg_im),
        .reg_write_in(reg_write_ie),
        .reg_write_out(reg_write_im),
        .zero(zero_ie),
        .branch(branch_ie),
        .uncond_branch(uncond_branch_ie),
        .read_data(read_data_im),
        .pc_src(pc_src_1));

    iWrite_back writeback_m(
        .iw_clk(clk),
        .read_data(read_data_im),
        .alu_result(alu_result_ie),
        .MemtoReg(mem_to_reg_im),
        .write_data(write_data_iw),
        .pc_in(cur_pc_im),
        .reg_write_in(reg_write_im),
        .reg_write_out(reg_write_iw),
        .pc_out(cur_pc_iw));

initial
    begin
       reset = 1;
       pc_src = 0;
       write_register_iw = 0;#5
       reset = 0; #100
   $finish;
    end
```

```
endmodule
```