

Lab title

your names

March 6, 2019

1 Executive Summary

The Executive Summary section should be a single concise paragraph that describes the following items. Please note that this should be a paragraph, not an itemized list like I have below. The list is just to tell you what I'm looking for...it is not there for you to fill it in on your lab report. See the Lab 1 Example Report.pdf on Canvas to see a good example of what I'm looking for.

1. The goal of the lab
2. What modules you created and what they do. This should describe how the modules function and how they fit into the overall processor that we are building. For instance, for Lab 1, you will want to describe the operation of the register and the fact that it is used to store the program counter, which is used to keep track of which instruction to execute next.
3. Whether your lab was successful. If not successful, please state what is not currently working.

2 Test Report

To verify operation of this/these module(s), this lab requires N test bench(es). (You can just copy this statement and fill it in with the correct number of test benches)

1. Register Test Bench

Address	Disassembly	Comment	Value	Symbol
23	movl \$0, %eax		0	
24	movl \$0, %eax		0	
25	movl \$0, %eax		0	
26	movl \$0, %eax		0	
27	movl \$0, %eax		0	
28	movl \$0, %eax		0	
29	movl \$0, %eax		0	
30	movl \$0, %eax		0	
31	movl \$0, %eax		0	
32	movl \$0, %eax		0	
33	movl \$0, %eax		0	
34	movl \$0, %eax		0	
35	movl \$0, %eax		0	
36	movl \$0, %eax		0	
37	movl \$0, %eax		0	
38	movl \$0, %eax		0	
39	movl \$0, %eax		0	
40	movl \$0, %eax		0	
41	movl \$0, %eax		0	
42	movl \$0, %eax		0	
43	movl \$0, %eax		0	
44	movl \$0, %eax		0	
45	movl \$0, %eax		0	
46	movl \$0, %eax		0	
47	movl \$0, %eax		0	
48	movl \$0, %eax		0	
49	movl \$0, %eax		0	
50	movl \$0, %eax		0	
51	movl \$0, %eax		0	
52	movl \$0, %eax		0	
53	movl \$0, %eax		0	
54	movl \$0, %eax		0	
55	movl \$0, %eax		0	
56	movl \$0, %eax		0	
57	movl \$0, %eax		0	
58	movl \$0, %eax		0	
59	movl \$0, %eax		0	
60	movl \$0, %eax		0	
61	movl \$0, %eax		0	
62	movl \$0, %eax		0	
63	movl \$0, %eax		0	
64	movl \$0, %eax		0	
65	movl \$0, %eax		0	
66	movl \$0, %eax		0	
67	movl \$0, %eax		0	
68	movl \$0, %eax		0	
69	movl \$0, %eax		0	
70	movl \$0, %eax		0	
71	movl \$0, %eax		0	
72	movl \$0, %eax		0	
73	movl \$0, %eax		0	
74	movl \$0, %eax		0	
75	movl \$0, %eax		0	
76	movl \$0, %eax		0	
77	movl \$0, %eax		0	
78	movl \$0, %eax		0	
79	movl \$0, %eax		0	
80	movl \$0, %eax		0	
81	movl \$0, %eax		0	
82	movl \$0, %eax		0	
83	movl \$0, %eax		0	
84	movl \$0, %eax		0	
85	movl \$0, %eax		0	
86	movl \$0, %eax		0	
87	movl \$0, %eax		0	
88	movl \$0, %eax		0	
89	movl \$0, %eax		0	
90	movl \$0, %eax		0	
91	movl \$0, %eax		0	
92	movl \$0, %eax		0	
93	movl \$0, %eax		0	
94	movl \$0, %eax		0	
95	movl \$0, %eax		0	
96	movl \$0, %eax		0	
97	movl \$0, %eax		0	
98	movl \$0, %eax		0	
99	movl \$0, %eax		0	
100	movl \$0, %eax		0	
101	movl \$0, %eax		0	
102	movl \$0, %eax		0	
103	movl \$0, %eax		0	
104	movl \$0, %eax		0	
105	movl \$0, %eax		0	
106	movl \$0, %eax		0	
107	movl \$0, %eax		0	
108	movl \$0, %eax		0	
109	movl \$0, %eax		0	
110	movl \$0, %eax		0	
111	movl \$0, %eax		0	
112	movl \$0, %			

Name	Value	0 ns	10 ns	20 ns	30 ns	40 ns	50 ns
clk	1						
rst	0						
d[63:0]	5						
q[63:0]	5						

Listing 1: Verilog code for testing a register.

2

```

        'ALU_PASS: begin
            alu_result <= b_in;
        end
    endcase
end
endmodule

```

Listing 2: Verilog code for implementing a register.

```

#include "definitions.vh"

module register(
    input wire clk ,
    input wire reset ,
    input  wire ['WORD-1:0] D,
    output reg  ['WORD-1:0] Q='WORD'b0
);

    always @(posedge( clk ),posedge( reset )) begin
        if ( reset==1'b1)
            Q<='WORD'b0;
        else
            Q <= D;
        end
    end
endmodule

```