EE3230 VLSI Design (2019 Fall) HW #1

Due date: 2019/10/04 (Friday) 10am

No plagiarism is allowed!!

0. Go through the tutorial document on the class webpage.

1. Use a combination of 2-input CMOS logic gates (in gate-level symbols) to generate the schematics for the following functions from inputs of A, B, and C.
Then complete the stick diagrams for each of the following functions according to the schematics you draw.

(a) Y=A'+B'(15%)

(b) Y=A'B'C'(15%)

(c) Y=AC+BC+B' (15%)

2. Draw the fabrication steps of an inverter (cross section).
Explain the "self-aligned poly-silicon gate" as well as "lightly-doped drain (LDD)". (35%)

3. Please simulate and analyze a CMOS inverter according to the following conditions using the model provided by TA (CIC018.l).

* Set the supply voltage to 1.8 V.
* Set the output load of this inverter to 0.15 pF.
* Use the minimum channel length for both NMOS and PMOS.
* Use the minimum channel width for NMOS.

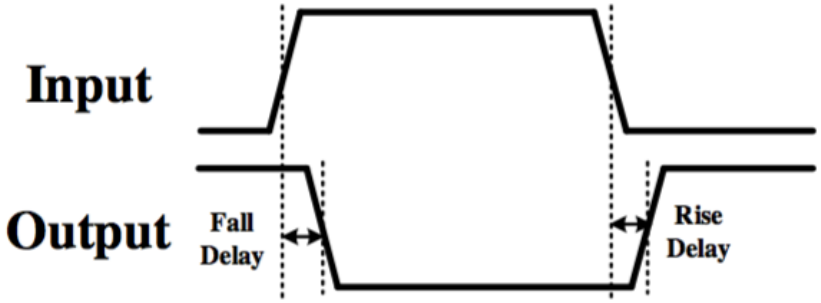
3a) Find and report the optimal width for PMOS for a balanced trigger point of inverter at TT corner and 25°C. The meaning of a balanced trigger point is as the following.
Vin = Vout = 0.5×VDD (That is to say, Vout equals to Vin when Vin is set to half of VDD.)

3b) Perform DC sweep and plot Vout vs. Vin as Vin sweeps from 0 V to VDD with the step of 0.05 V in five different process/temperature corners.

3c) Repeat 3b) with the NMOS width set to 5X of minimum channel width. Then complete the following table. (Report Vout value when Vin is set to half of VDD.)

Process	Temperature	NMOS width 1X	NMOS width 5X
		Vout at Vin=0.5×VDD	Vout at Vin=0.5×VDD
TT	25°C		
FF	–40°C		
SS	125°C		
SF	25°C		
FS	25°C		

4. Follow the previous question, run transient simulations for all 10 conditions and measure the input to output delay of the inverter. Set the rise and fall time of the input waveforms to 1 ns.



Attach the simulated waveforms for TT 25°C (with rise and fall time labeled clearly) for both 1X NMOS and 5X NMOS.

Process	Temperature	NMOS width 1X		NMOS width 5X	
		Fall Delay	Rise Delay	Fall Delay	Rise Delay
TT	25°C				
FF	–40°C				
SS	125°C				
SF	25°C				
FS	25°C				