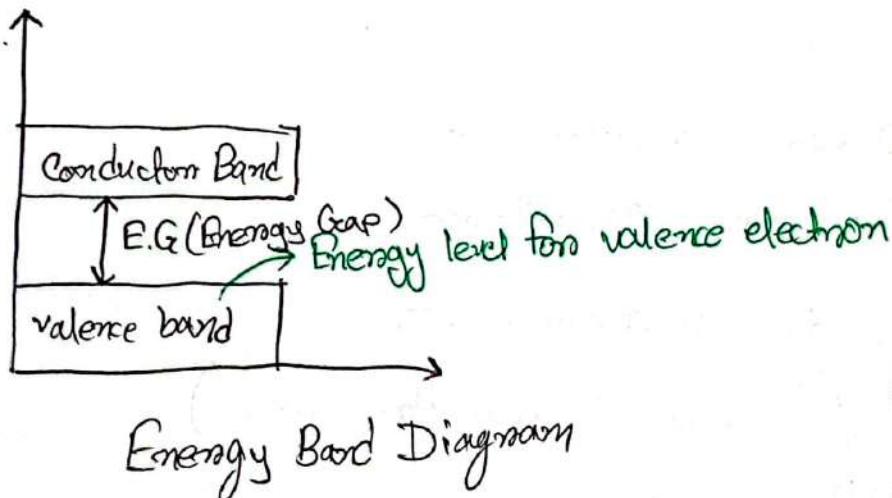
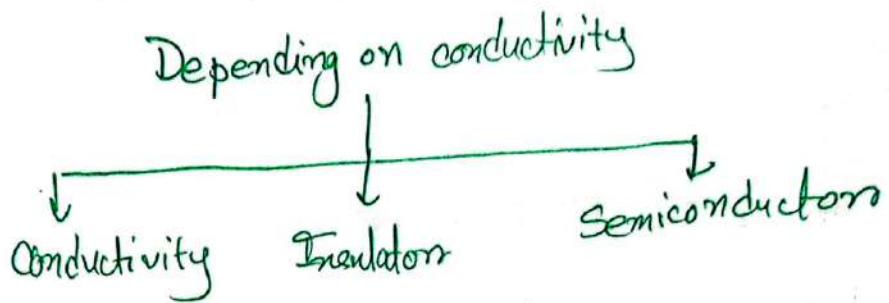


EEE

C-2 (w-1)

Semiconductor



* Conductors has $E.G = 0$
" " = big

* Insulators "

* Semiconductors " " =

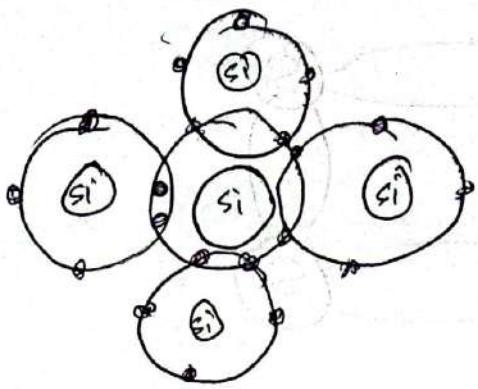
$$\text{Conductivity} = \frac{1}{\text{Resistivity}}$$

* Si is ideal bc
- abundant in nature
- ! (temp sensitive)

* Semiconductors has $4 e^-$ in valence shell

- energy released to complete octet = energy absorbed to complete octet

* Multiple atoms together form lattice



* Adding impurities in intrinsic is called doping
(Slides + HSC knowledge)

n-type:

- created by adding pentavalent element
[Antimony (Sb)
Arsenic (As)
Phosphorus (P)]

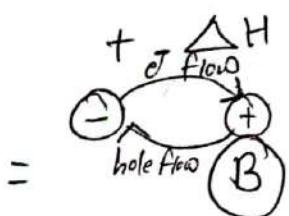
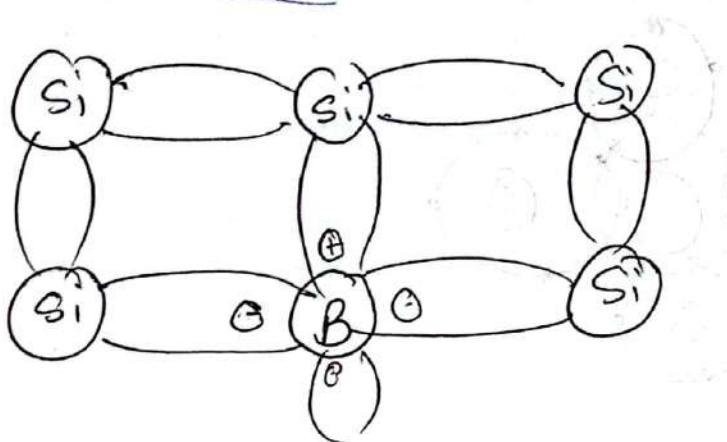
- conductivity depends on the level of doping
- pentavalent atoms = donor atoms
- majority charge carriers = electric electron

p-type:

- created by adding trivalent element
[Boron (B)
Gallium (Ga)
Indium (In)]

- trivalent atoms = acceptor atoms
- majority carriers = hole → [lack of electrons]

Electron vs Hole flow



* valence electron gets kinetic energy

creates
a vacancy because
the electron is
missing

goes to an
unfilled
hole

3/4/24

L-1 (W-1)

EEE - Lab

- Diode
- BJT
- Oscilloscope

Attend	— 10
Lab Rep	— 10
Perf	— 10
Exam - 1	— 35 (setup + viva)
Exam - 2	— 35 (setup + viva)

* Ultimate Goal : Find Graph

+ Lab - 1 : Graph of diode

Ashfaq

* Lab - 2 : Rectifier

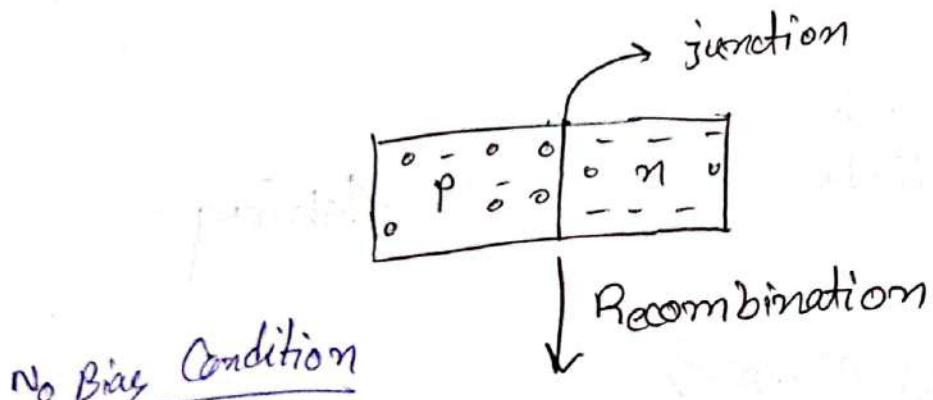
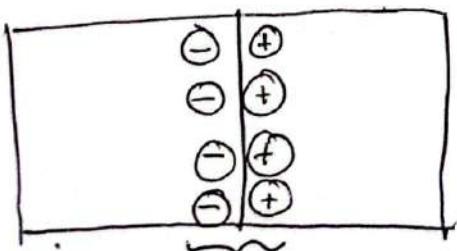
+ Lab - 3 : Clippers and Clamper

+ Lab - 4 : Zener's Diode

C-3 (W-2)Semiconductor Diode:

Joining of n-type and p-type material

Room switches are electrical
Diodes are electronic switches

No Bias Condition

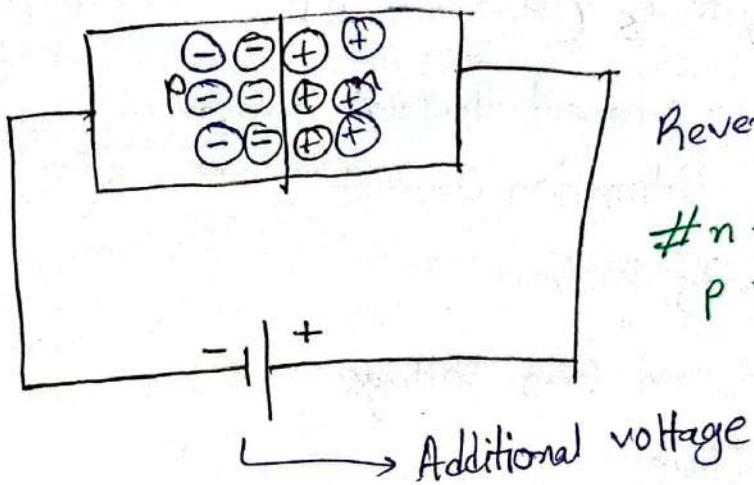
Depletion region \rightarrow depleted charge

\hookrightarrow Barrier potential

\hookrightarrow varies in each material

Bias: External voltage applied to receive ~~extreme~~ exact response

$V_d < 0 V$

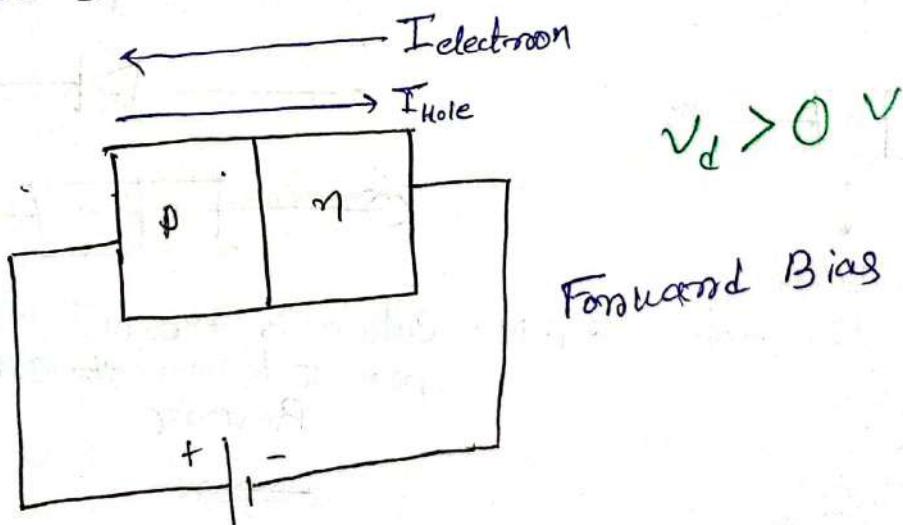


Reverse Bias

n - ^(+ve) terminal
p - ^(-ve) terminal

No majority flow

But some current will flow for minority carriers with constant value called Reverse Saturation Current $\rightarrow I_s$ (usually in nA)



$V_d > 0 V$

Forward Bias

Majority flows
minority will flow as the same Majority

* Read Book

Shockley's Equation

$$I_D = I_s (e^{\frac{V_D}{nV_T}} - 1)$$

↳ Current through diode

I_s = Reverse Saturation Current

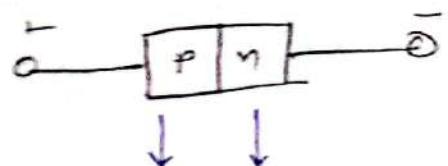
$\underline{I_s} = n$ = Ideality Factor

V_D = Applied Forward Bias Voltage

V_T = Thermal voltage

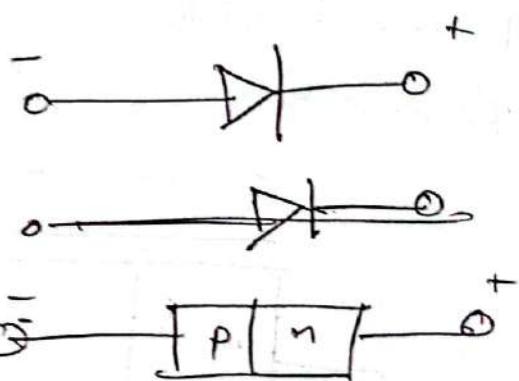
~~Done
chat slide~~

Diode:



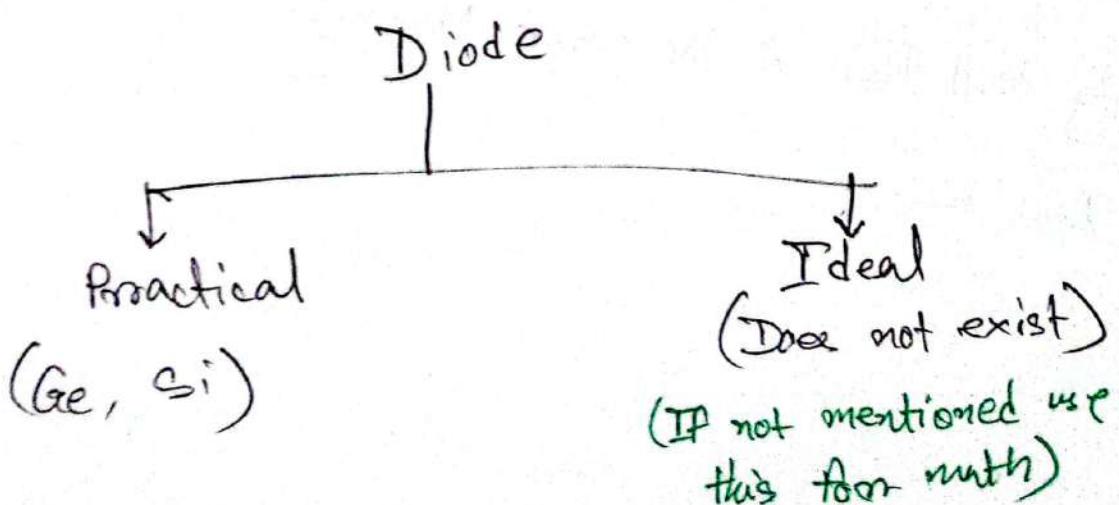
Anode Terminal Cathode Terminal

Forward ~~Potential~~ Bias

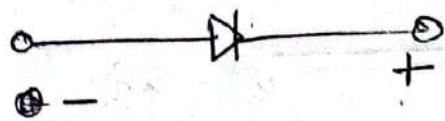


*H.N: Cation is +ve and will flow to -ve pole. That's why ~~cathode~~ cathode is -ve
Reverse Bias

~~Forward~~ Bias



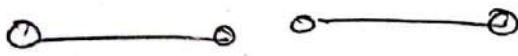
* Ideal Diode



For Reverse Bias of an ideal circuit diode makes open circuit

$$\therefore i = 0$$

$$\therefore v = \text{something}$$

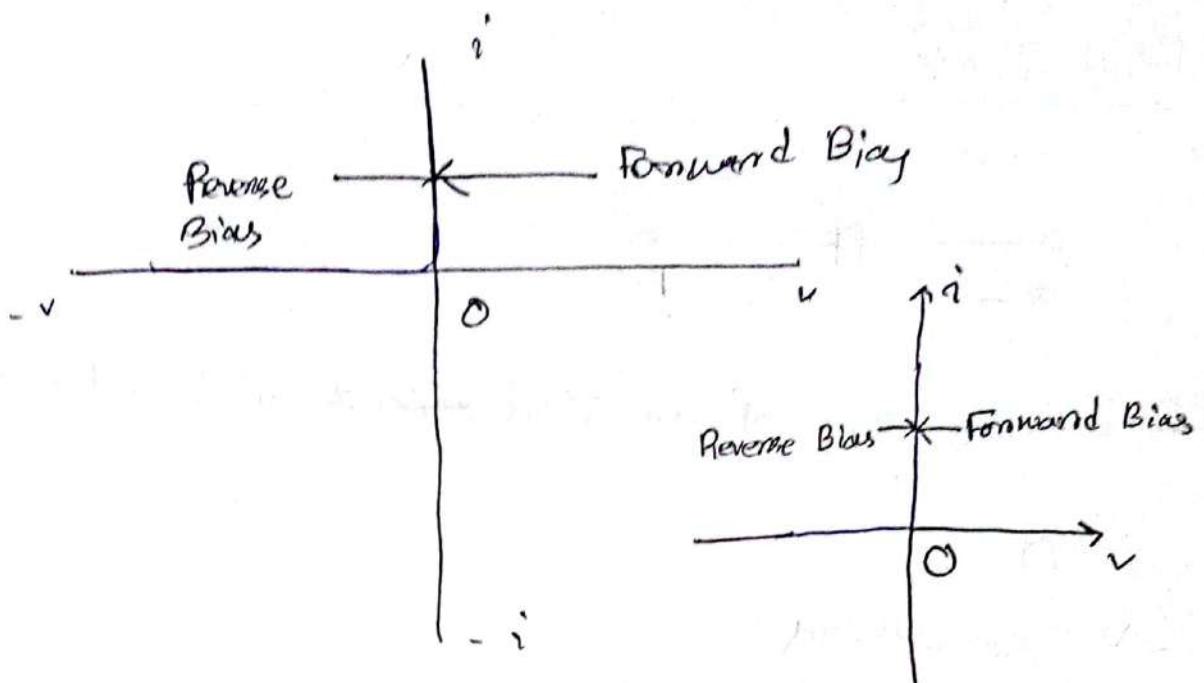


Forward Bias of an ideal diode makes short circuit

$$\therefore i = \text{something}$$

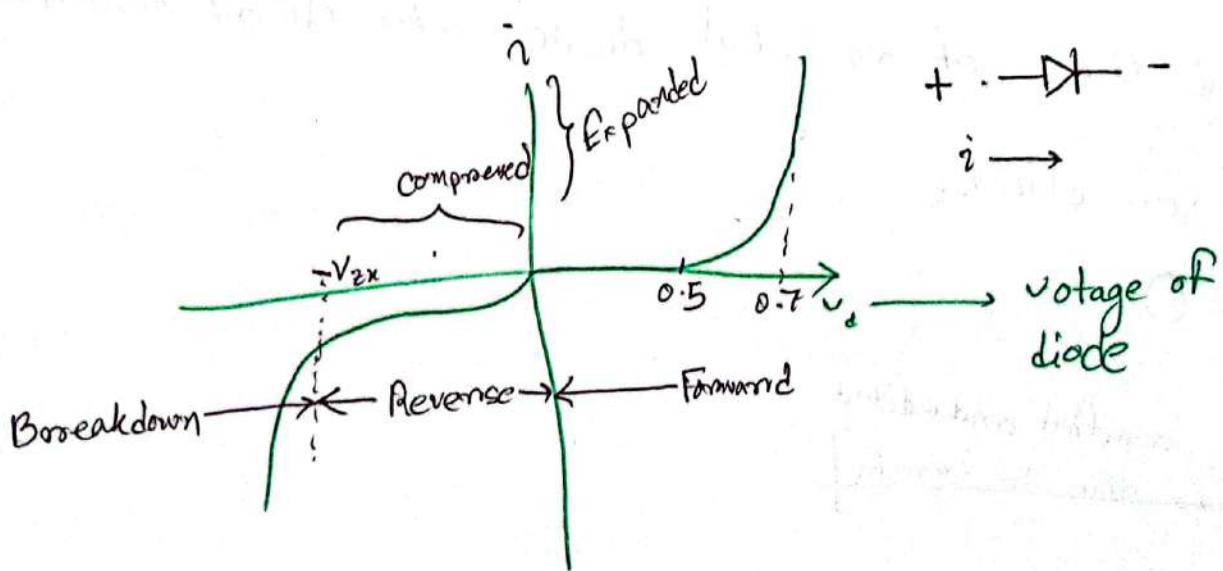
$$\therefore v = 0$$

verified and edited
[use diode to verify]



$I - V$ Graph

* For an ideal diode, no depletion region exists



Forward Bias ($V > 0$)

Reverse " ($V < 0$)

Breakdown ($V < V_{ZK}$)

↳ Zener / Breakdown Voltage

For Forward Bias [V > 0]

$$i = I_s (e^{v/v_T} - 1)$$

* i_s depends on temp and is proportional to cross sectional area of diode

$$v_T = \frac{kT}{q} = 25.8 \text{ mV}$$

$$\left| \begin{array}{l} k = \text{boltzmann constant} \\ = 1.38 \times 10^{-23} \text{ J/K} \\ T = \text{absolute temp in kelvin} \\ q = \text{magni e}^- \text{ charge} = 1.6 \times 10^{-19} \text{ C} \end{array} \right.$$

$$i = I_s e^{v/v_T} - I_s$$

or, $i = I_s e^{v/v_T}$; [when I_s is very small]

or, $v = v_T \ln \left(\frac{i}{I_s} \right)$

$$\therefore v_2 - v_1 = 2.3 v_T \ln \left(\frac{I_2}{I_1} \right)$$

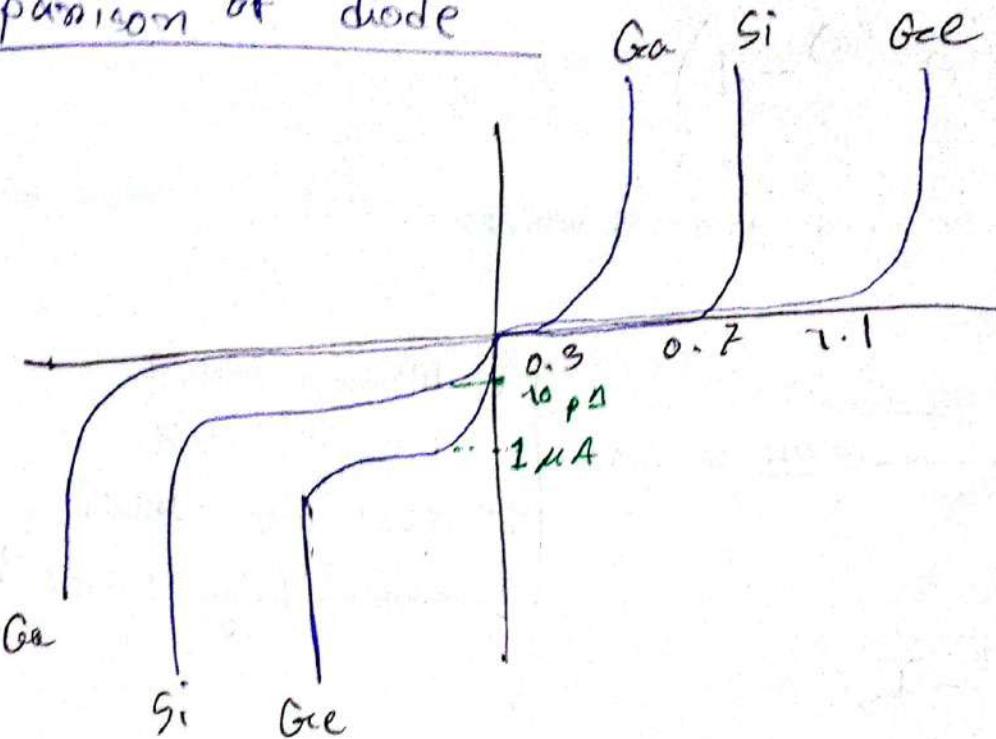
[Check slides
for better understanding]

For Reverse Bias, [V < 0]

$$i = I_s (e^{v/v_T} - 1)$$

$$\therefore i = I_s ; [\because e^{v/v_T} \text{ very small}]$$

* Comparison of diode



Application:

- Blocking current
- Rectifiers
- Voltage regulators
- Clippers
- Clampers
- LED
- Tuner
- Logic Photodiode (Ask later)
- Multipliers.

C-4 (N-2)

Theoretical
Not for ikezane

16/04/24

Breakdown

* More potential = More depletion = More Electric Field
= More speed = More kinetic energy

Temperature Effect:

For Si,

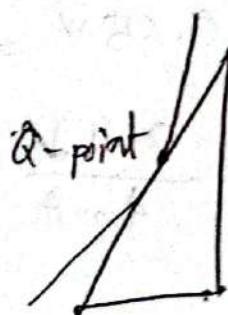
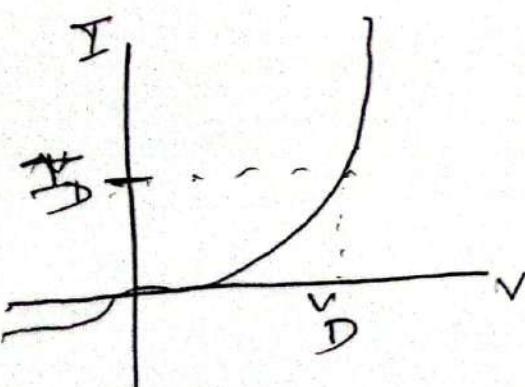
each ~~10~~ 1°C makes 2.5 mV change; [forward]

each 10°C doubles current flow

Diode Resistance

AC Resistance

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$



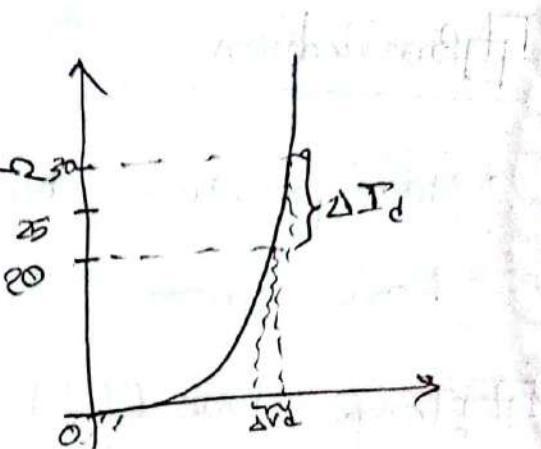
DC Resistance:

$$R_D = \frac{V_D}{I_D}$$

Math on DC

At 2 mA,

$$R_D = \frac{V_D}{I_D} = \frac{0.7 \text{ mV}}{2 \text{ mA}} = 350 \Omega$$



At 25 mA,

$$R_D = \frac{V_D}{I_D} = \frac{0.79}{25 \text{ mA}} = 31.62 \Omega$$

Math on AC

At 2 mA,

$$\Delta I_D = 4 \text{ mA} - 0 \text{ mA} = 4 \text{ mA}; \text{ we graph}$$

$$\Delta V_D = 0.76 \text{ V} - 0.65 \text{ V} = 0.11 \text{ V}$$

$$\therefore r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.11 \text{ V}}{4 \text{ mA}} = 27.5 \Omega$$

At 25 mA,

$$\Delta I_D = 30 \text{ mA} - 20 \text{ mA} = 10 \text{ mA}$$

$$\Delta V_d = 0.8 \text{ V} - 0.78 \text{ V} = 0.02 \text{ V}$$

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.02 \text{ V}}{10 \text{ mA}} = 2 \Omega$$

#NHT Approach

$$\frac{d}{d V_D} I_D = -\frac{d}{d V_D} \left[I_s (e^{V_D/nV_T} - 1) \right]$$

$$\text{or, } \frac{d I_D}{d V_D} = I_s (e^{V_D/nV_T}) / nV_T$$

$$\text{or, } \frac{d I_D}{d V_D} = (I_D + I_s) / nV_T$$

$$\text{but, } \frac{d I_D}{d V_D} \approx \frac{I_D}{nV_T}$$

since the derivative of a function is slope of tangent,

$$\frac{d I_D}{d V_D} = \frac{1}{m_d} = \frac{I_D}{nV_T}$$

$$\therefore m_d = nV_T / I_D$$

Diode Equivalent Circuit:

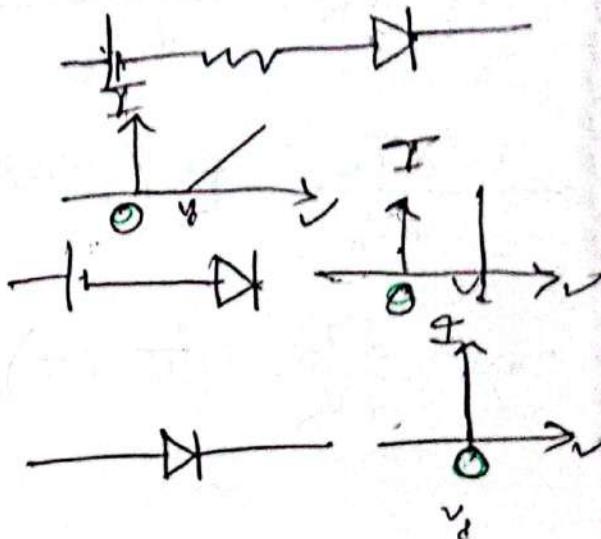
Piecewise - linear

Simplified model $R_{\text{network}} \gg r_{\alpha v}$

Ideal device

$$R_{\text{network}} \gg r_{\alpha v}$$

$$F_{\text{network}} \gg V_u$$



Load Line Analysis:

$$E = V_D + I_D R$$

$$\text{on, } V_D = E - I_D R$$

$$\therefore V_D = E ; [\text{if } I_D = 0]$$

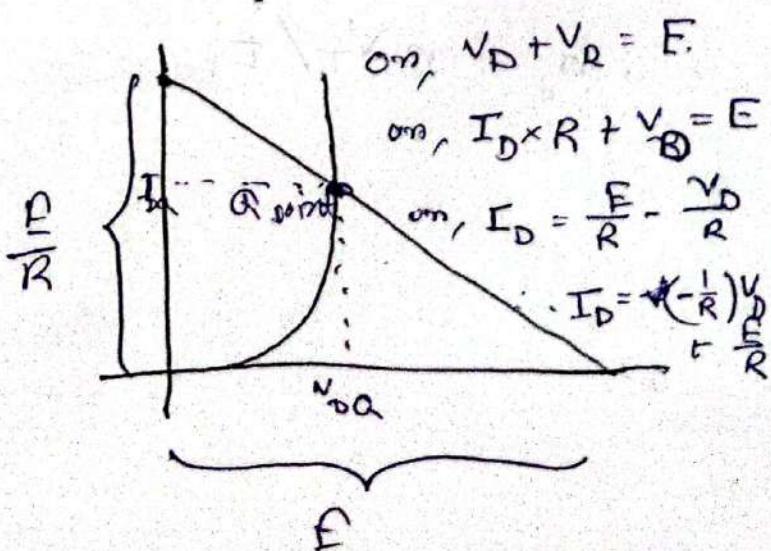
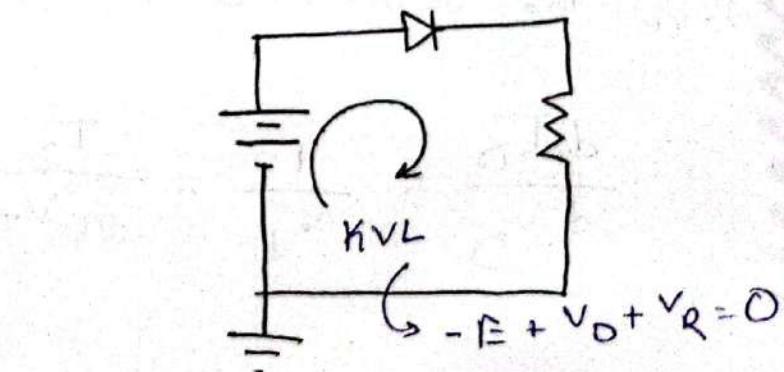
Again,

$$E = V_D + I_D R$$

$$\therefore I_D = \frac{E}{R} ; [\text{if } V_D = 0]$$

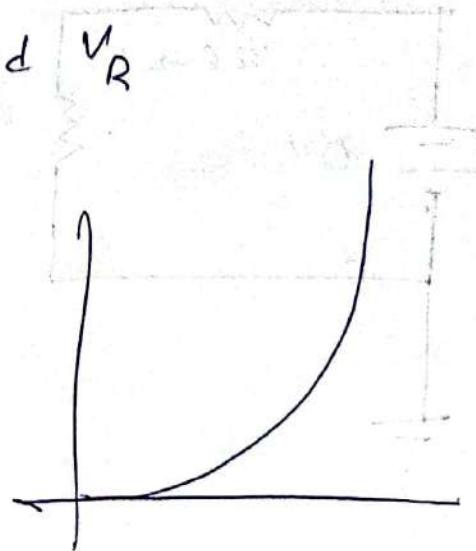
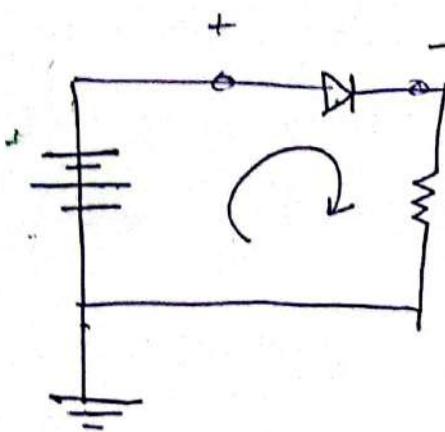
*H.N: Use $V_D = 0, I_D = 0$

to find $\frac{E}{R}$ and $\frac{I_D}{V_D}$



Q1] Math on Load Analysis:

Determine V_{DQ} , I_{DQ} , R_D and V_R



$$I_D = \frac{E}{R} \Big|_{V_D=0V} = \frac{10V}{0.5k\Omega} = 20mA$$

* Use $V_D = 0$ and $I_D = 0$ after KVL

$$V_D = E \Big|_{I_D=0A} = 10V$$

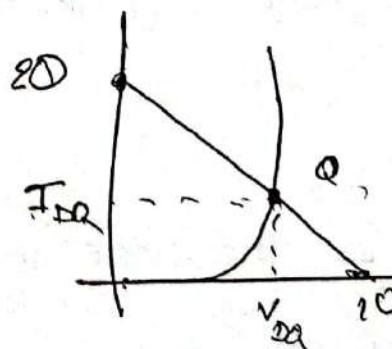
* Use graph to find V_{DQ} and I_{DQ}

$$\therefore V_{DQ} \approx 0.78mV$$

* Plug those in KVL to get V_R

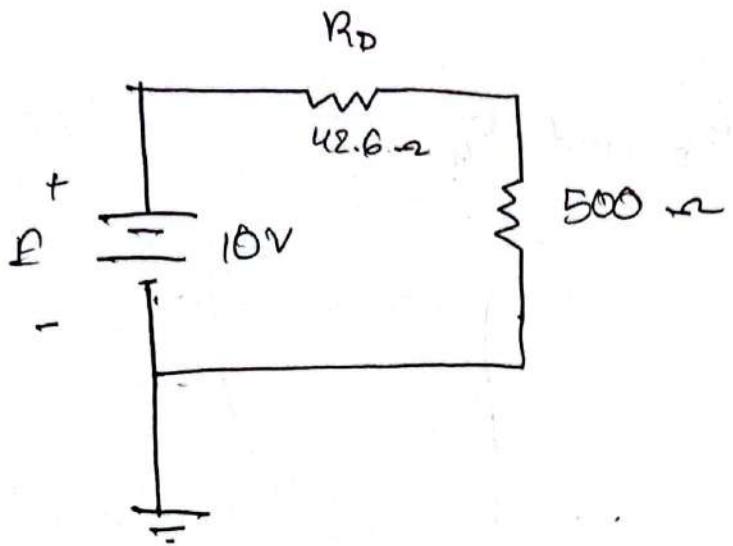
$$\therefore I_{DQ} \approx 18.5mA$$

* Use $V = IR$ to get R_D ; $\frac{V_R}{I_{DQ}}$



$$\therefore V_R = E - V_D = 10V - 0.78V = 9.22V$$

$$\therefore R_D = \frac{V_R}{I_{DQ}} = \frac{9.22V}{18.5mA} = 49.6\Omega$$



Diode in a network:

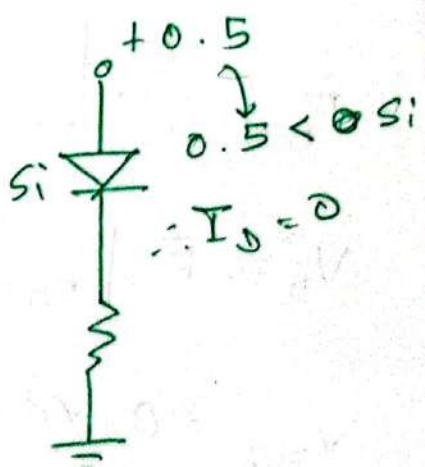
- * Find state (For/Rev)
- * Replace with equivalent voltage source
- * Solve

Watch out if ~~yes~~ the diode will work

"Questions will ~~be~~ tricky not hard lol" ~ Sim

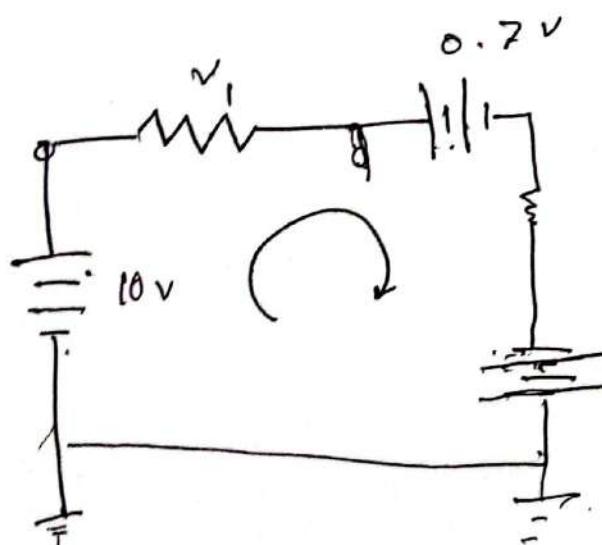
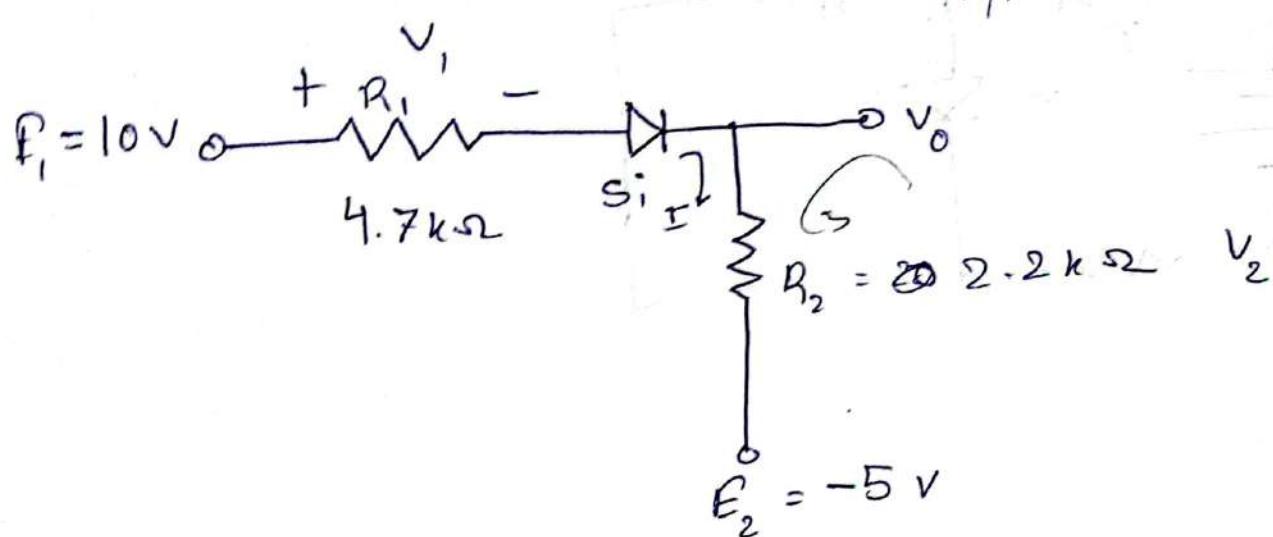
- * If I_D is on the same direction it forward
" " " opposite " " reverse

If || two diff' pot! then smol one will count



#ACTUAL Math

Determine I , V_D , V_1 , V_2 and V_0



// Use KVL

$$-10 + V_1 + 0.7 + V_2 + 5 = 0$$

$$\therefore 4.7I + 2.2I = 4.3$$

$$\therefore I = 2.07 \text{ mA}$$

$$\therefore V_D = 0.7 \text{ V}$$

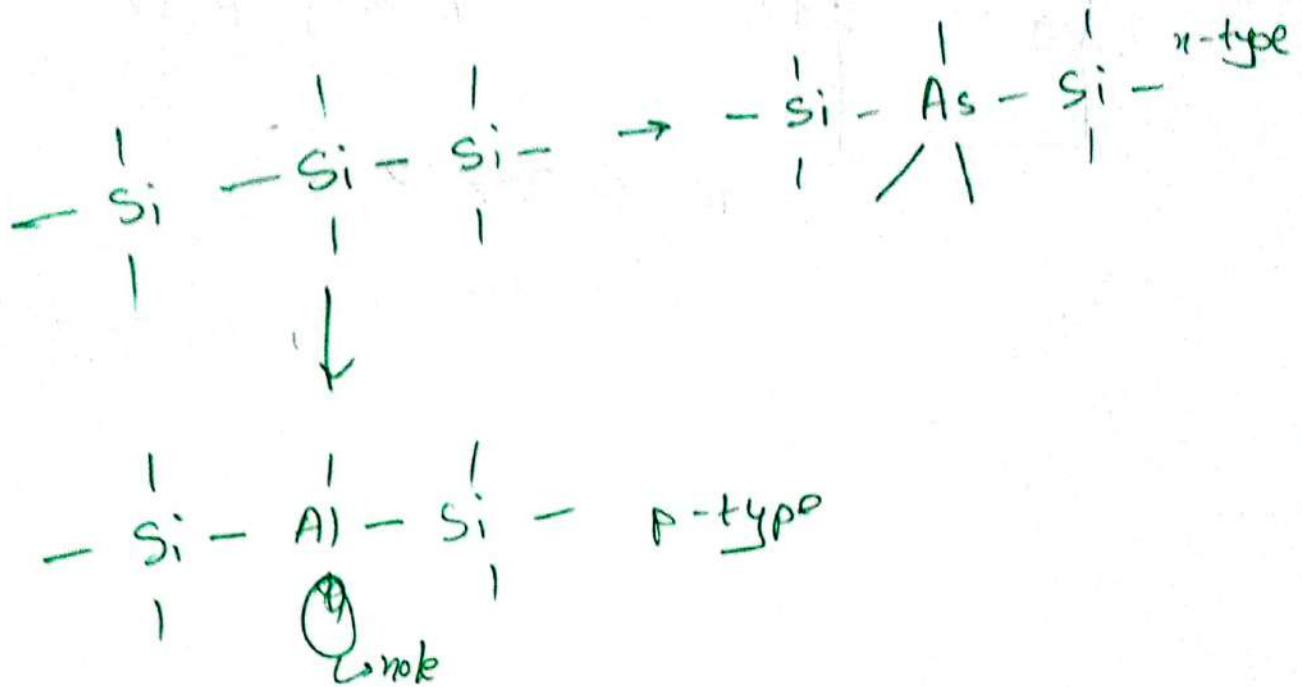
// Use $V = IR$ on R_1

$$V_1 = 2.07 \times 4.7$$

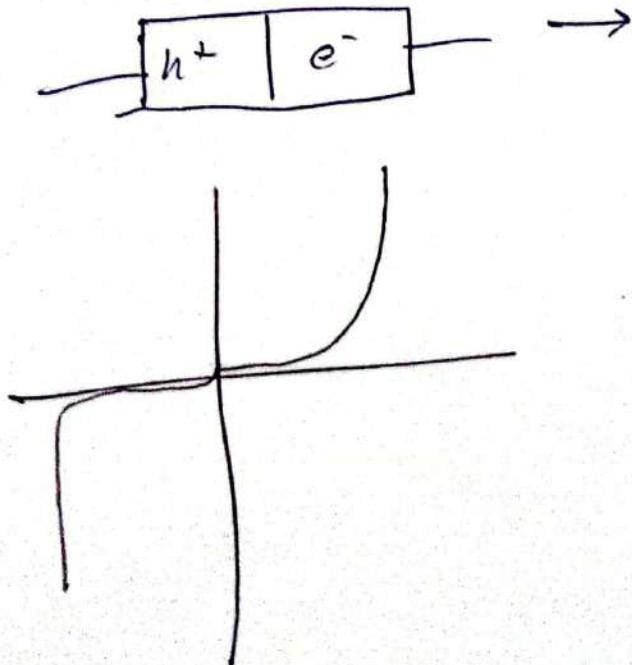
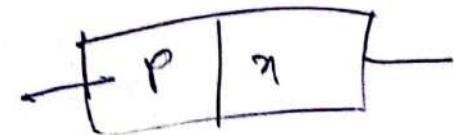
// Use $V = IR$ on R_2

$$V_2 = 2.07 \times 2.2$$

$$= 4.55 \text{V}$$

Exp - 1: I-V characteristics of a diode

Diode :

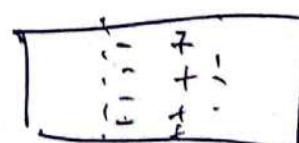


at Forward Bias

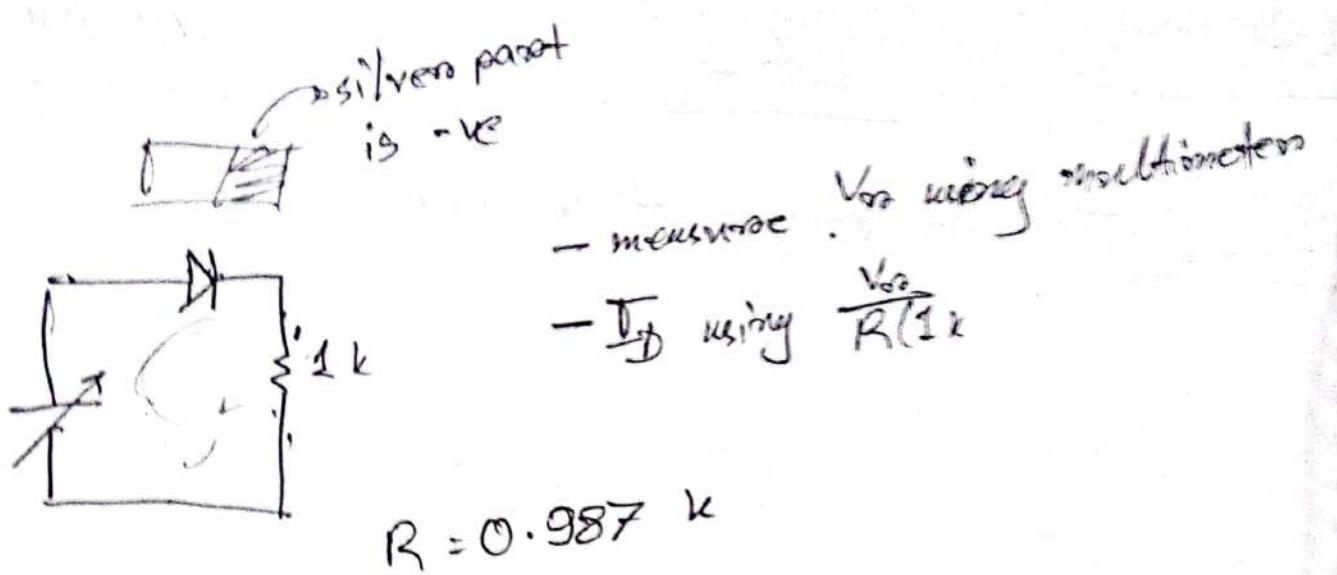
decreases depletion layer

at Reverse Bias

increases depletion layer



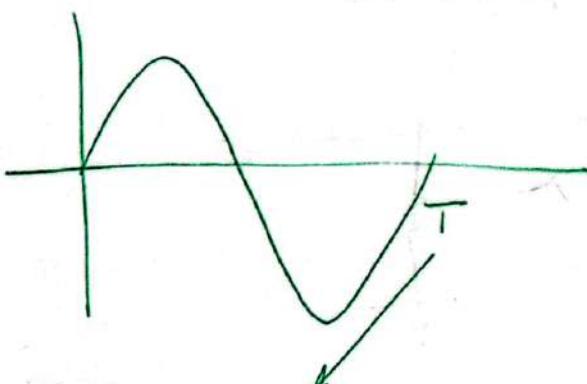
in
potential
variation



RectifiersRectifiers:

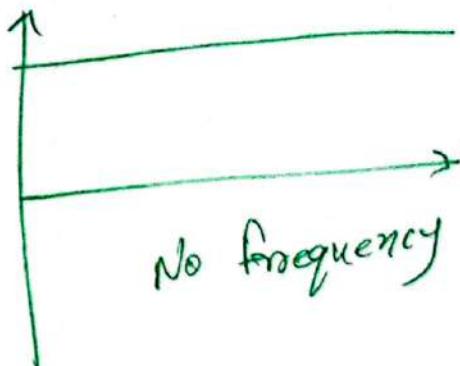
electrical device that converts AC to DC by periodically reversing it.

↓
process is called rectification

AC:

Time period
↓
After which it repeats

* Magnitude different for each time state

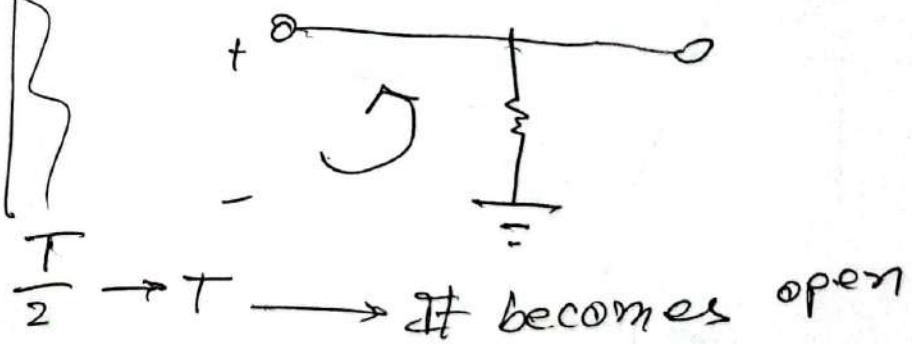
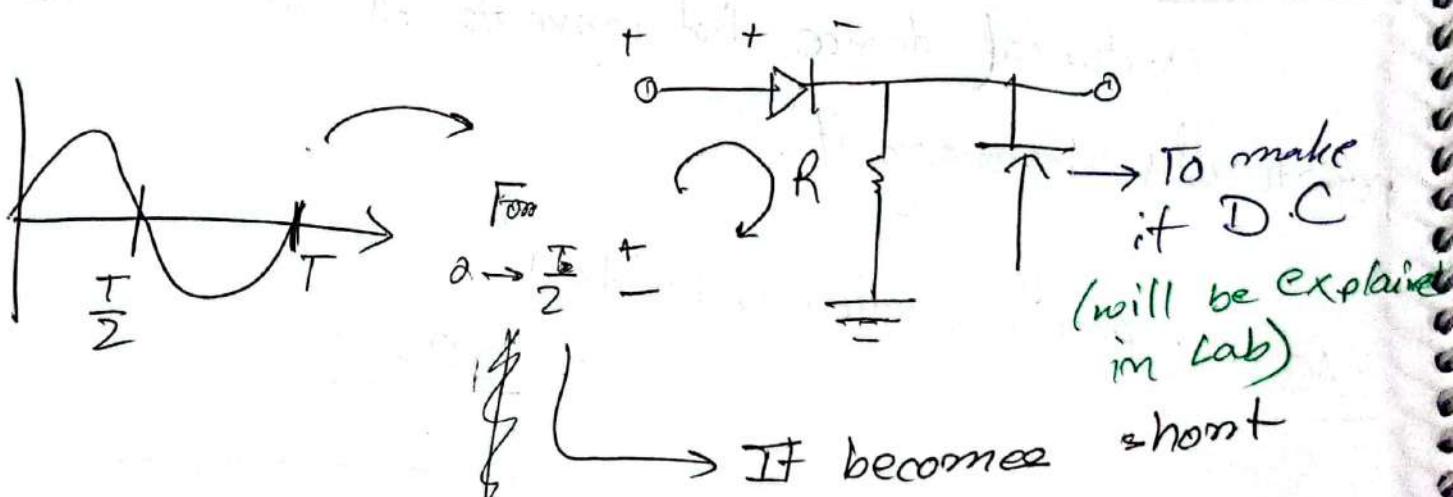
DC:

No frequency

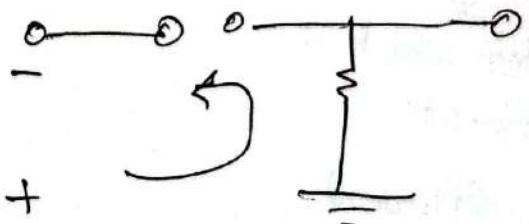
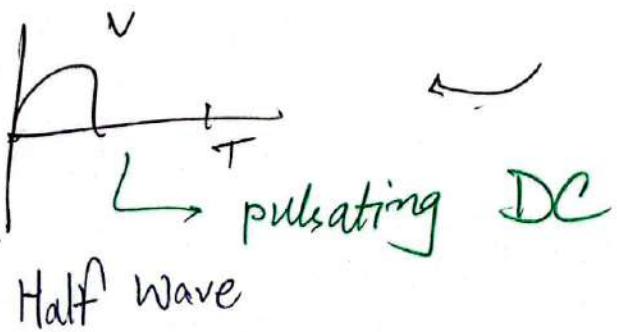
* Magnitude is same for each state

Half Wave Rectifier:

only allows one half cycle of an AC voltage



output



* Check Slides + Book for extra
clarification

* Arrange DC output:

$$V_{dc} = \frac{1}{2\pi} \int_0^{2\pi} v_o d(\text{acet})$$

$$= \frac{1}{2\pi} \int_0^{\pi} V_m \sin \omega t d(\text{acet})$$

$$= \frac{V_m}{2\pi} \left[\cos \omega t \right]_0^\pi$$

$$\therefore V_{dc} = 0.318 V_m$$

* Rectifier mean loss

* Rectification Efficiency:

For dc, $P_{dc} = I_{dc}^2 R_L = \left(\frac{I_m}{\pi} \right)^2 R_L$

For ac, $P_{ac} = I_{max}^2 (r_d + R_L) = \left(\frac{I_m}{2} \right)^2 (r_d + R_L)$

$$\therefore \eta = \frac{P_{dc}}{P_{ac}} = \frac{\left(\frac{I_m}{\pi} \right)^2 R_L}{\left(\frac{I_m}{2} \right)^2 (r_d + R_L)} \times 100 \%$$

$$= \frac{40.6}{\frac{r_d + R_L}{1 + (r_d/R_L)}} \% \rightarrow \text{very small}$$

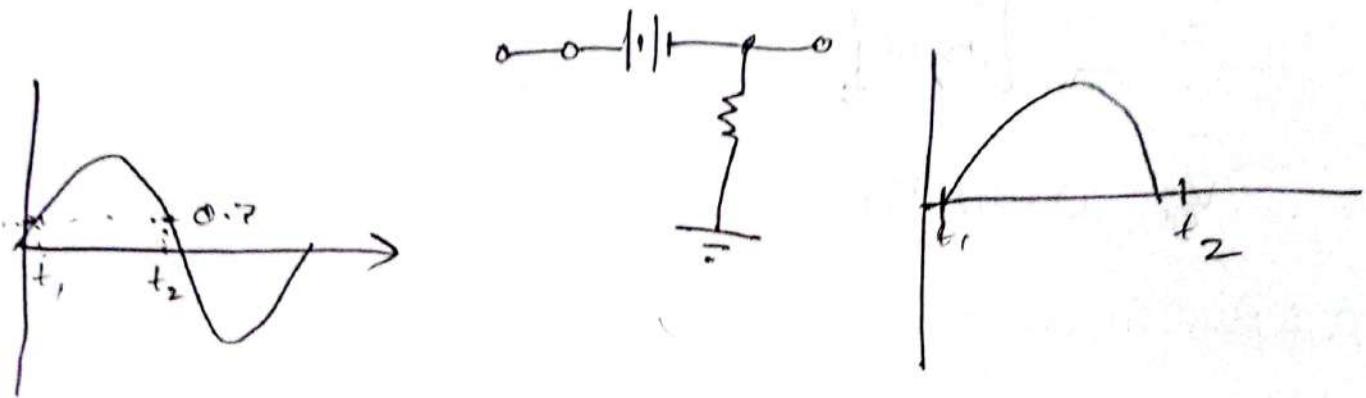
when $r_d \ll R_L$

= 40.6% → max % for an ideal diode.

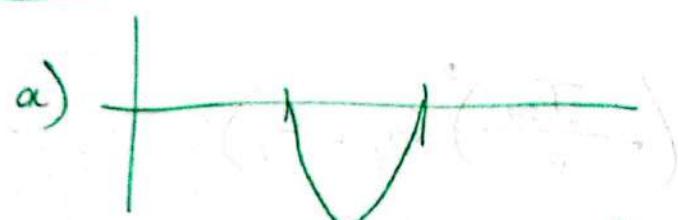
* Effect of V_k on half-wave rectified signal

$$V_o = V_i - V_k$$

$$\text{For, } V_m \gg V_k ; \quad V_{DC} = 0.318(V_m - V_k)$$



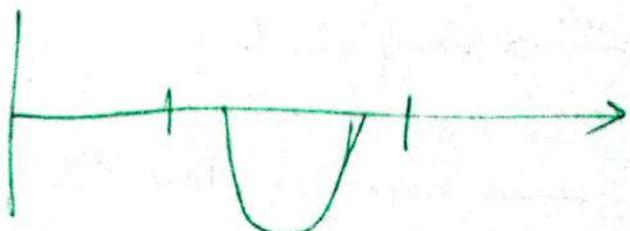
* Slide math



$$\therefore V_{DC} = 0.318 \times (-20) \\ = 0 - 6.36 V$$

\rightarrow put value in graph

$$\text{b) } V_{DC} = 0.318 \times (19.5) = -6.14$$



Peak Reverse Voltage:

The ^{maximum} voltage rating for which the diode breaks down

- * If $I_{through} > PIV$ then the diode will no longer rectify
- * Will be explained during clippers and clamps



C-6 (W-3)

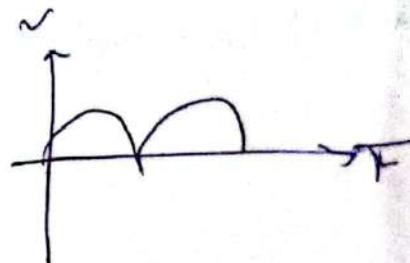
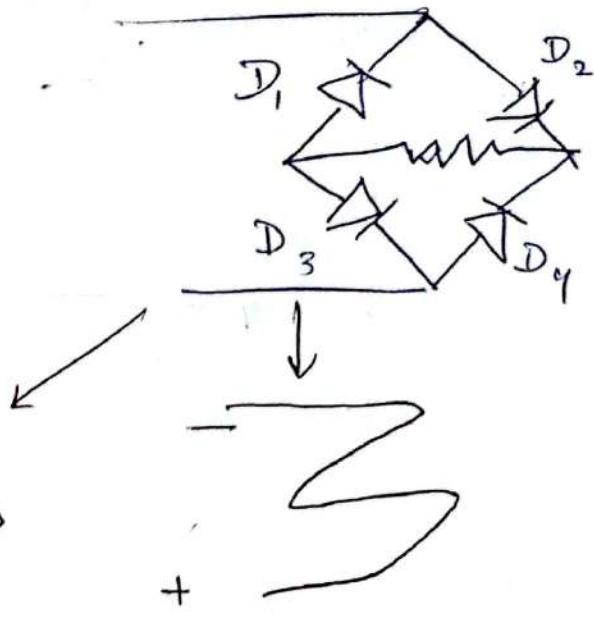
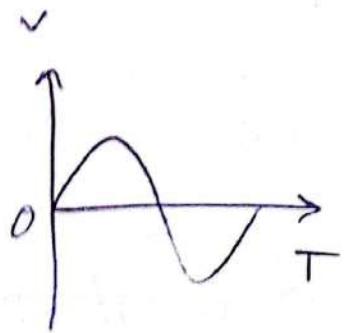
Full Wave Rectification

23/04/24

FWR:

converts both half of AC to same side

$$V_{dc} = 0.636 V_m$$



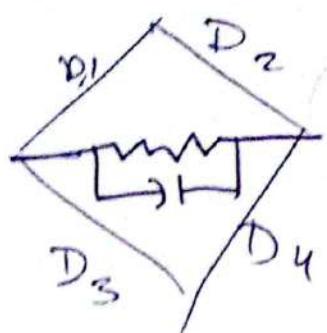
Pulsating DC: $\frac{V_m}{V_o}$ has some characteristics of AC but not all.

$$\text{Pulse width} \rightarrow V_m - V_o = \text{ripple voltage}$$

= peak to peak

$$V_{(p-p)} \frac{V_o}{fRC} \rightarrow \text{to reduce ripple} \rightarrow fRC$$

Filter



$$X_C = \frac{1}{2\pi f C}$$

* Inductors and ~~the~~ Capacitors
are reactive elements
↓
depends on f (Hz)

Use capacitance to send AC to ground
* Capacitance either charges or discharges

V_s be a potential

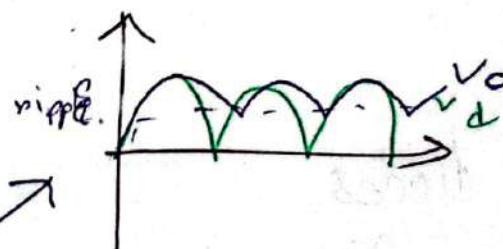
If $V_s > V_c \rightarrow$ charge

$$\tau = RC$$

$V_s < V_c =$ discharge

+ The capacitor absorbs the potential to be charged

[Read Book]



* Basically:

i) Capacitor takes charge

ii) Capacitor takes longer to discharge

iii) Before it fully discharges, it starts charging again ~~for~~ because of V_d

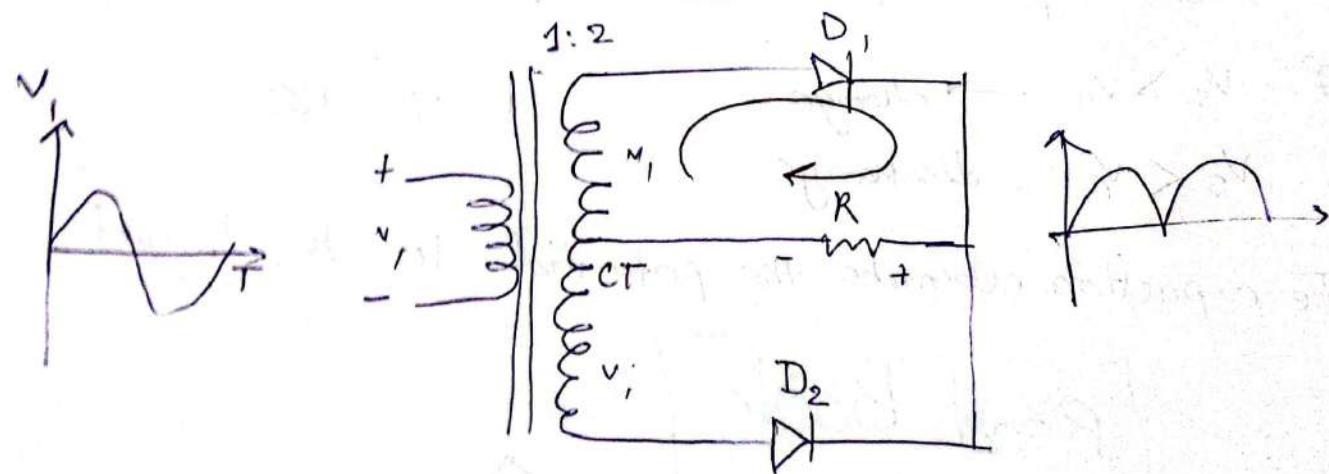
iv) As a result it ~~starts~~ ripple reduces.

+ FWR - Bridge Network

$$V_{dc} = 0.636(V_m - 2V_{an})$$

+ FWR - Tap Centers Tapped Transformers

can be divided into two equal voltages
at power electronic diode \rightarrow powerful in terms of voltage
and current tolerance



+ Less diodes

\therefore More efficiency

Avg DC output:

$$\text{Avg } V_{dc} = V_{dc} = \frac{1}{\pi} \int_0^{\pi} V_m \sin \omega t \, d(\omega t)$$
$$= \frac{V_m}{\pi} \left[-\cos \omega t \right]_0^{\pi}$$
$$= 0.636 V_m$$

Efficiency:

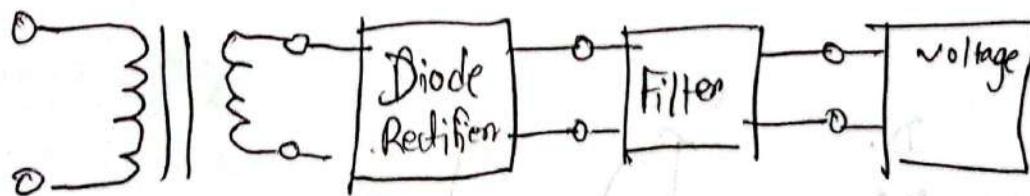
Same to as HWR

$$\therefore \eta = \frac{81.2}{1 + m_d / R_L} \%$$

$$\approx 81.2 \% \quad [\because m_d \ll R_L]$$

(max possible)

\triangleright = Zener diode



L-3 (W-3)

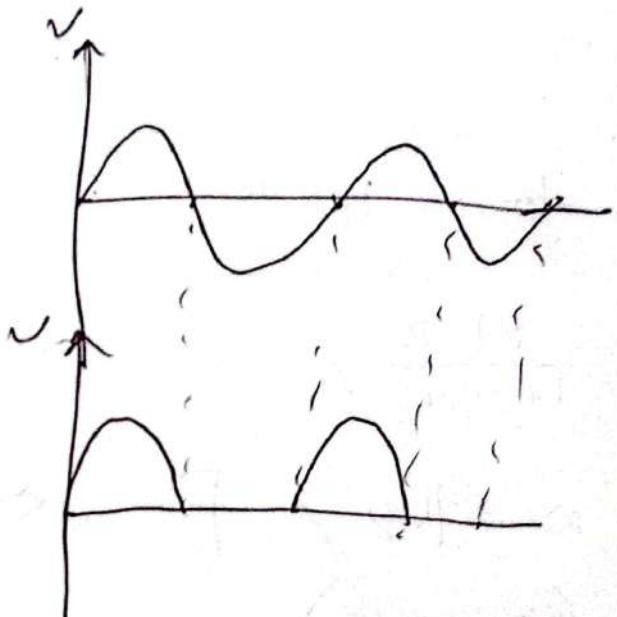
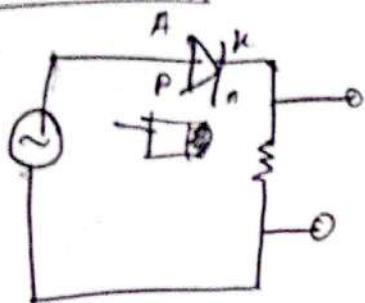
24/04/24

Exp - 3

Exp - 02: Diode rectifiers circuits

Defn: A Rectifier is a circuit that ^{converts} ~~creates~~ an AC signal.
Diode rectifiers is of 2 types: 1. Half-wave
2. full wave

Half Wave:



Full Wave:

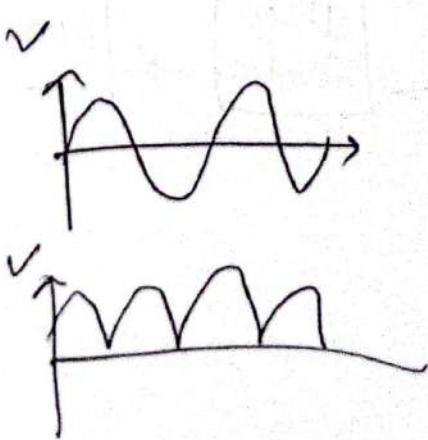
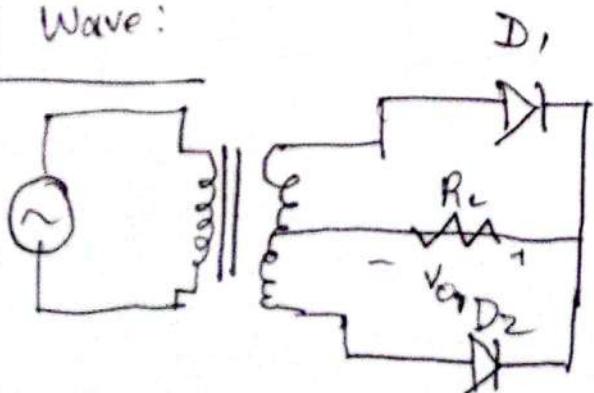
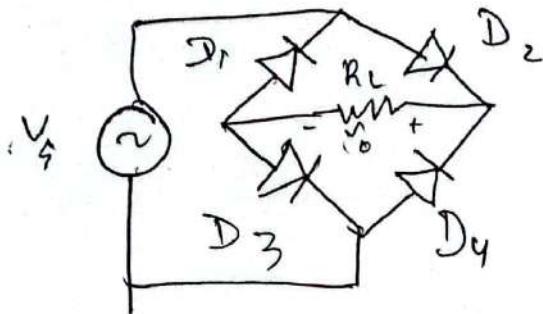


Fig: Center Tapped



~~10 Hz~~ ✓

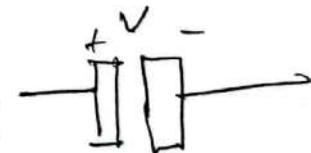
~~1 kHz~~



$$V_o = \frac{V_m}{fRC} - \text{for Half Wave}$$

so, if $f \uparrow \left\{ \begin{array}{l} V_o \downarrow \\ \text{or } C \uparrow \end{array} \right\}$

* Capacitors : ~~Coupling and~~ Charging and Discharging



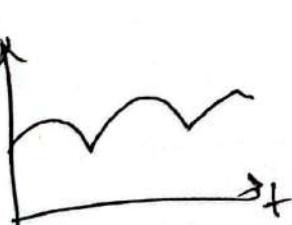
$$v(t) = V_m(1 - e^{-\frac{t}{\tau}})$$

Time constant, $\tau = RC$

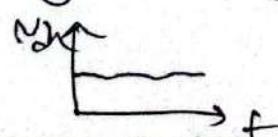
τ is the time required to discharge to around $\frac{36.8}{37}\%.$ of the initial voltage.

* Effect of Inserting a capacitor in parallel with R_L of Rectifier

Circuit :

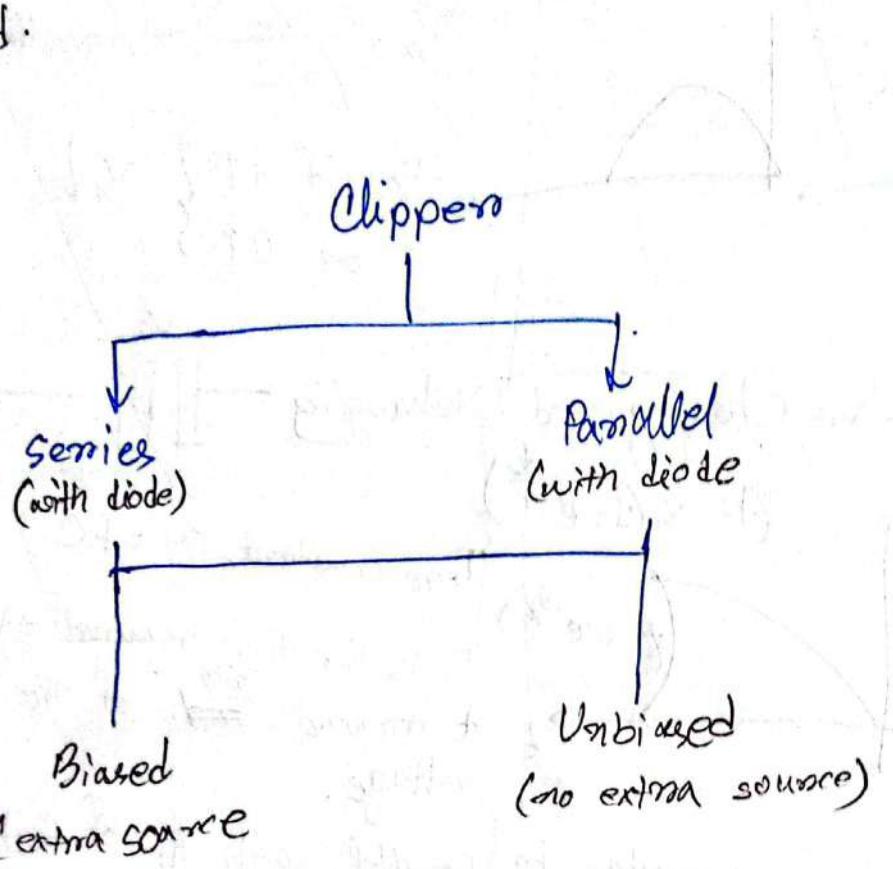


* Now, if you increase $f;$ it means if you decrease discharge time, then you will get a constant line.

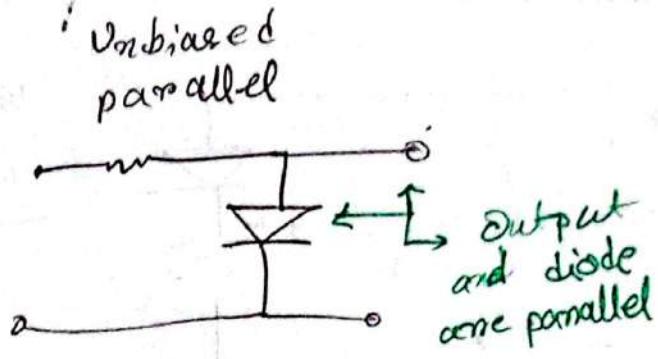
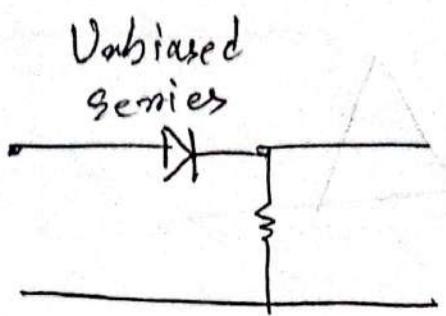


*Clipper:

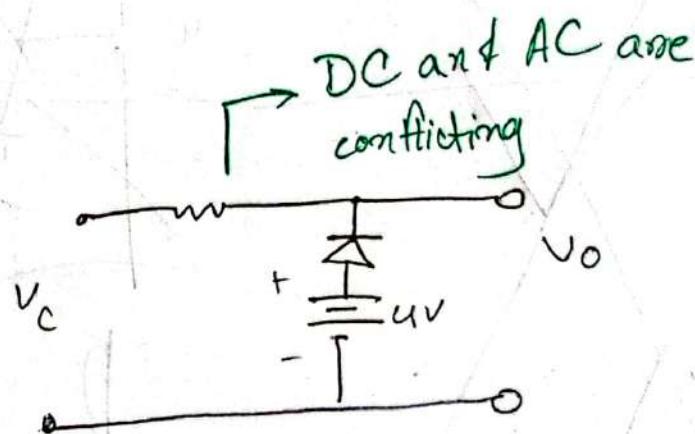
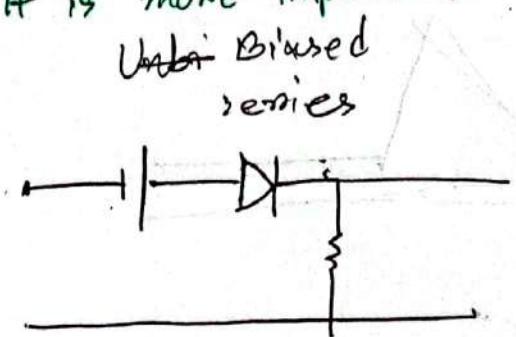
Wave shaping circuit that controls the shape of the output waveform by removing or clipping portions of the applied.



* Half wave Rectifier is a type of series clipper

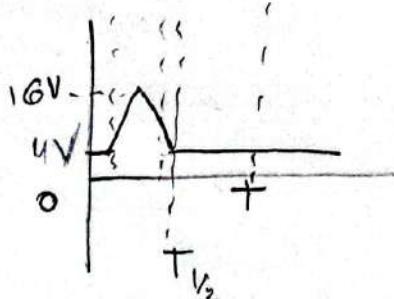
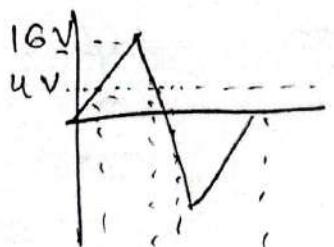


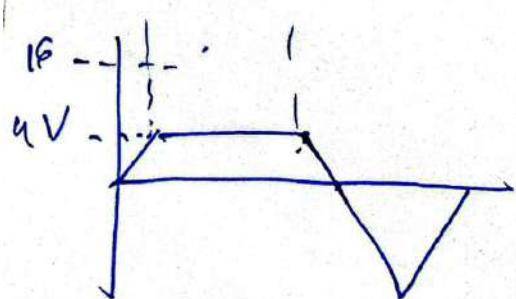
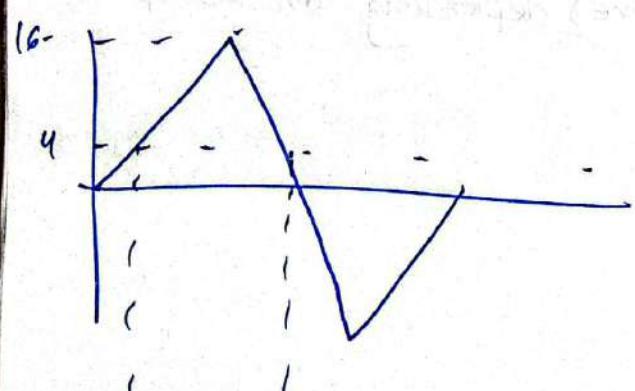
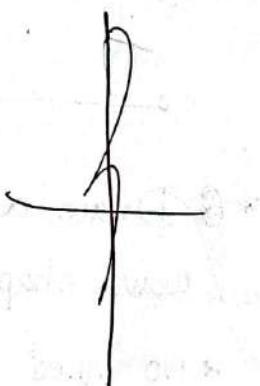
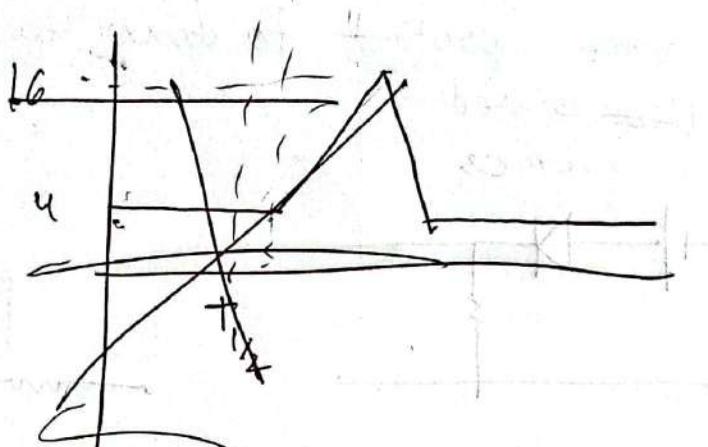
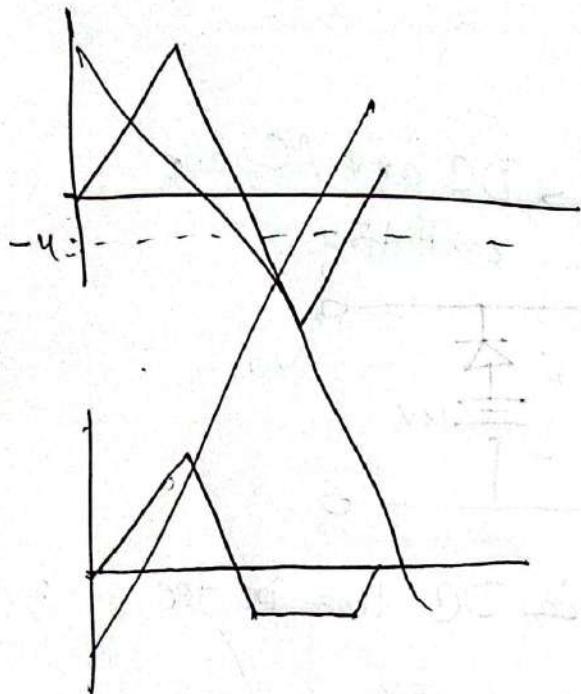
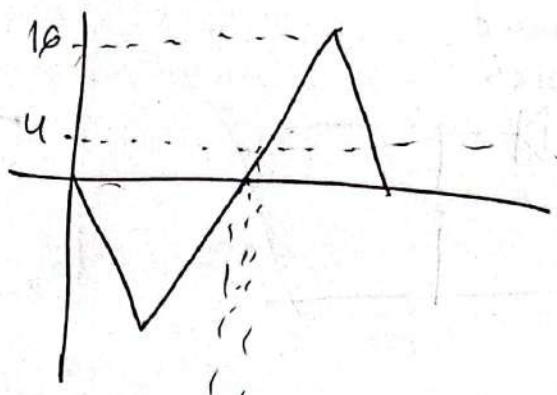
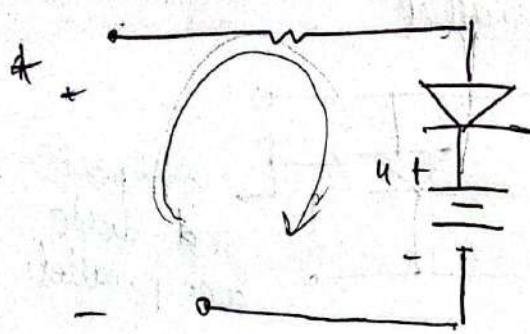
* it is more important to draw wave shape

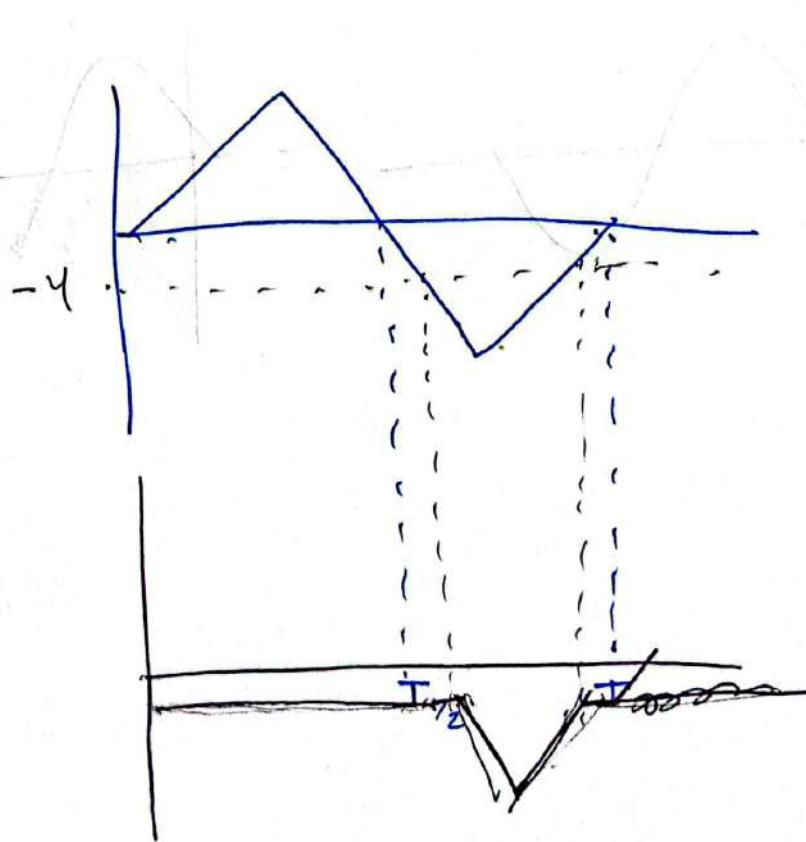
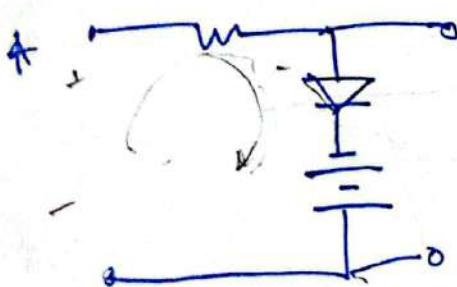
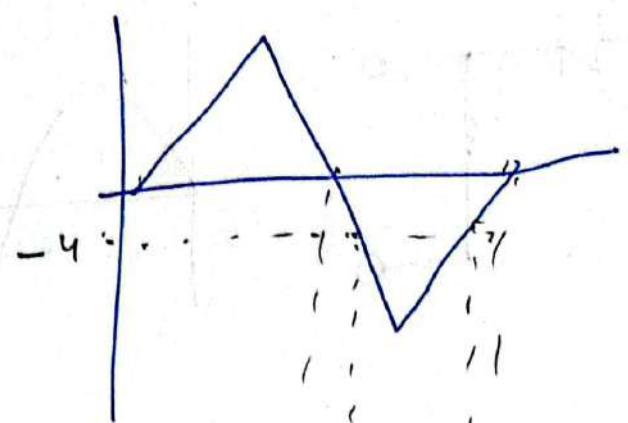
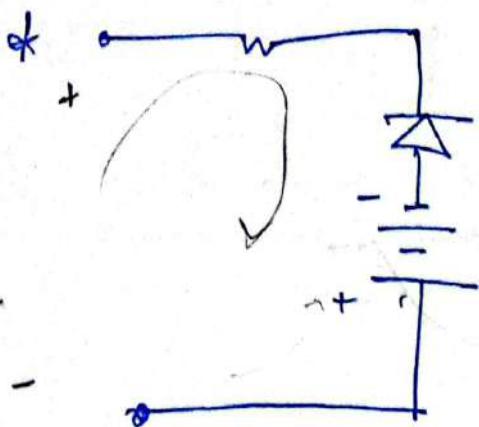


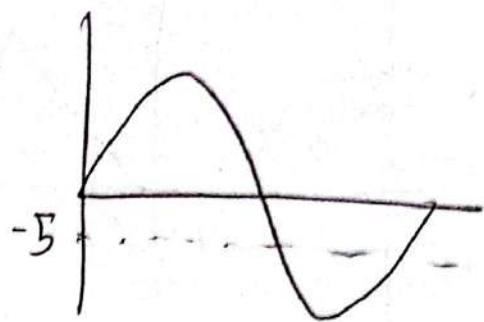
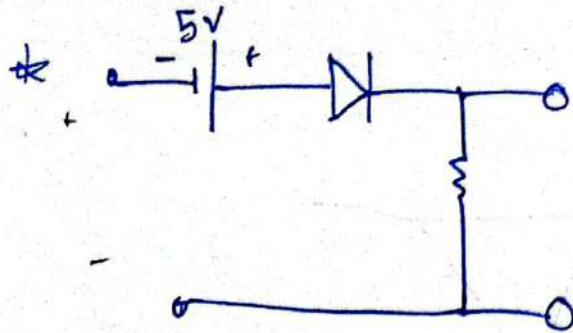
* @ Draw a dc DC line in the wave shape.

* No need to consider negative cycle (or positive) depending on setup





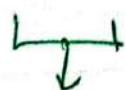




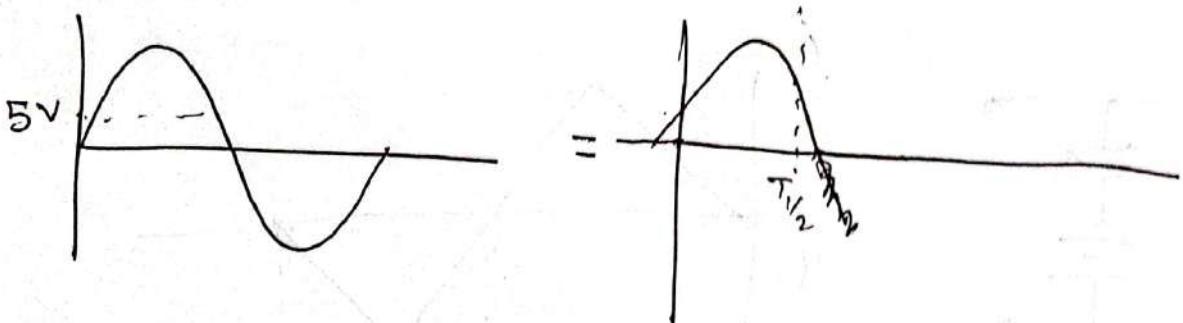
According to KVL

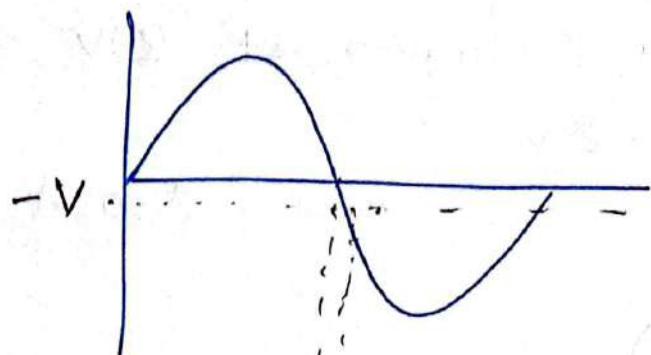
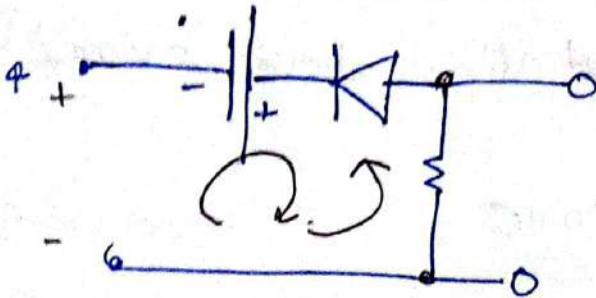
$$-V_i + 5V + V_o = 0$$

$$\text{or}, \quad V_o = V_i + 5V$$



AC and DC
cannot be added
So, graph will be shifted





$$-V_0 + V_{dc} + V_i = 0$$

$$\therefore V_0 = V_i + V_{dc}$$

For positive cycle,
diode is open

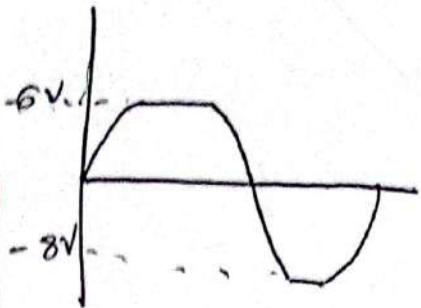
$$\therefore V = 0$$

For negative

$$V_i = -(V_0 + V_{dc})$$

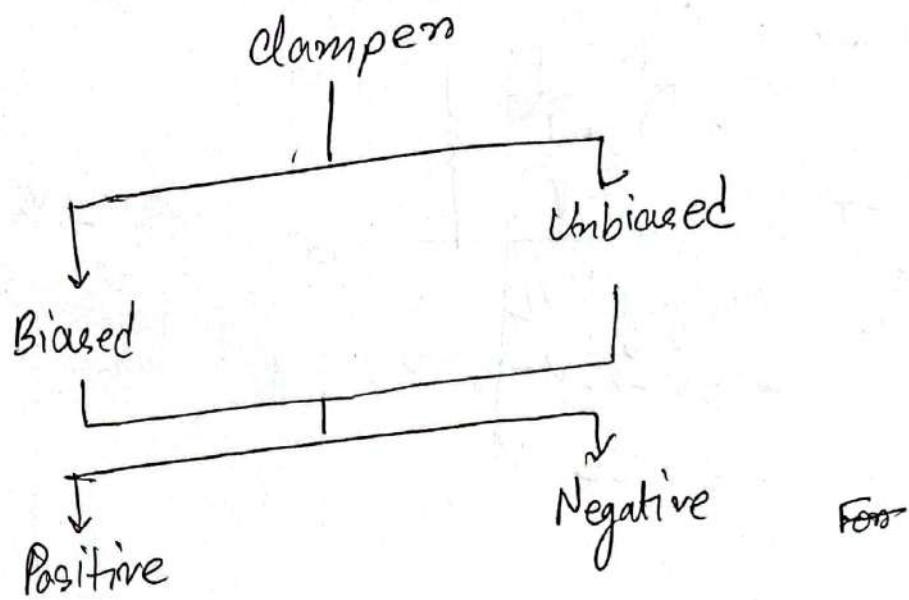
*Design a clipper of 20V that clips above 6V and below -8V

*do at home



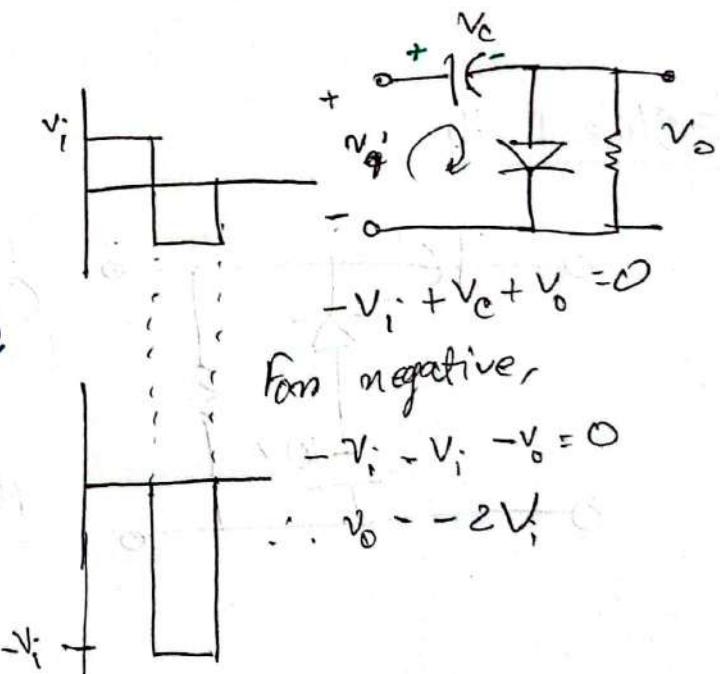
* Has capacitor

* Diode will always be parallel to load / resistance

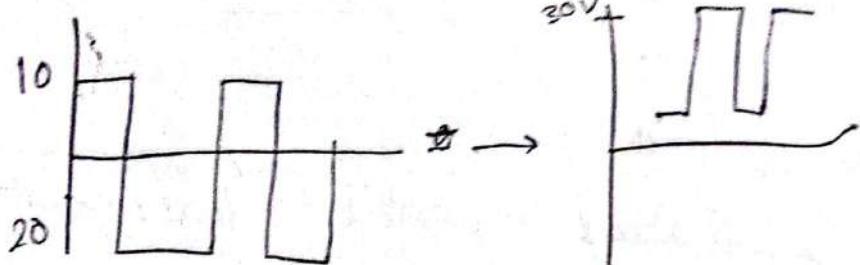


Wave diagram graph:

- i) Assume capacitors has no polarity
- ii) Check which cycle turns diode on
- iii) Use that cycle to find capacitor's V_C
- iv) Polarity obtained ^{in capacitor} will not change
- v) HVL again to find V_o

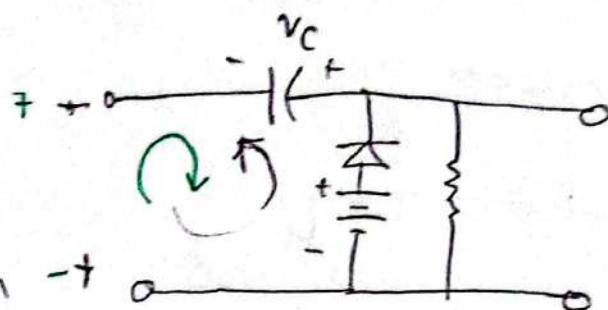


Biased



Here,

~~electrode~~
diode is on during negative
(↑) Cycle

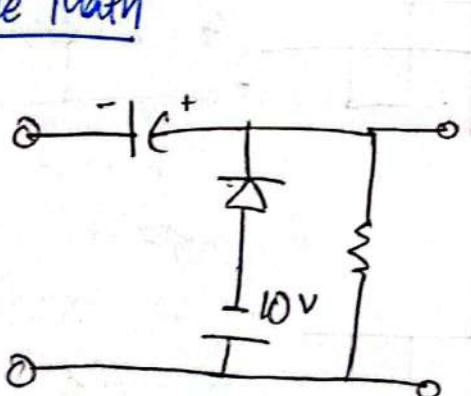


Applying KVL

$$+10V - 25V - V_o = 0$$
$$\therefore V_o = 35V$$

$$-20V + V_c - 5V = 0$$
$$\therefore V_c = -25V$$

Slide Math



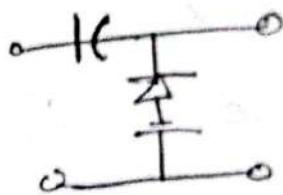
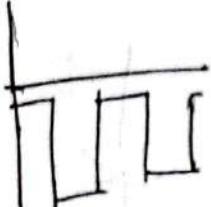
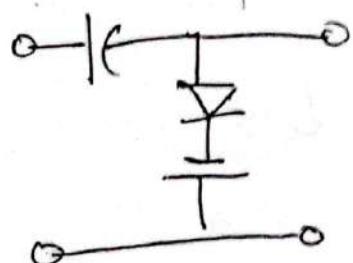
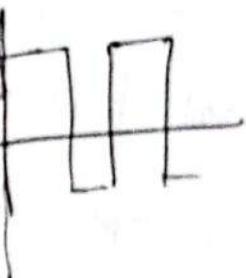
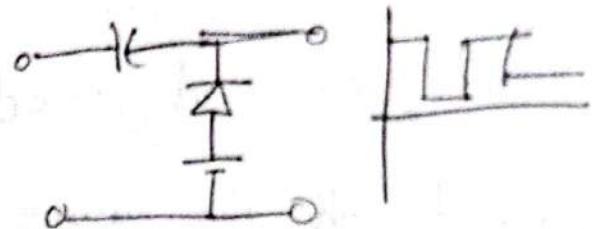
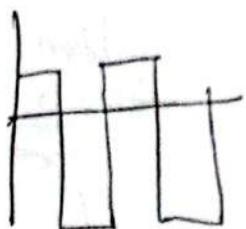
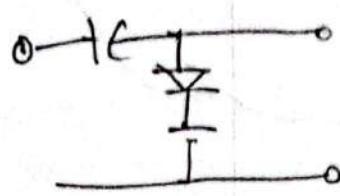
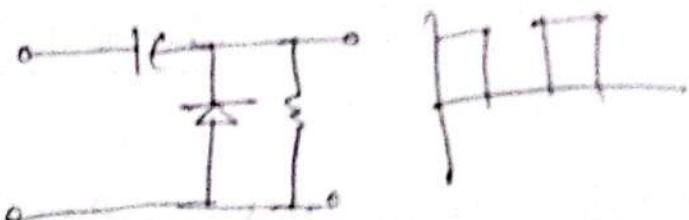
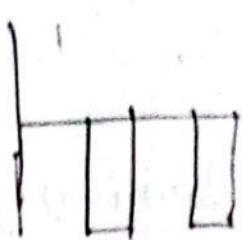
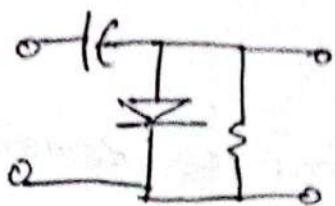
Verification:
Neg. Cycle:
 $\downarrow V_i - V_c - 10V = 0$

$$\therefore V_c = 10V$$

Positive cycle:

$$-V_i - V_c + V_o = 0$$
$$\therefore V_o = V_i + V_c = 30$$

Squaring



Ques. Design a square wave oscillator using an op-amp.

Zener Diode

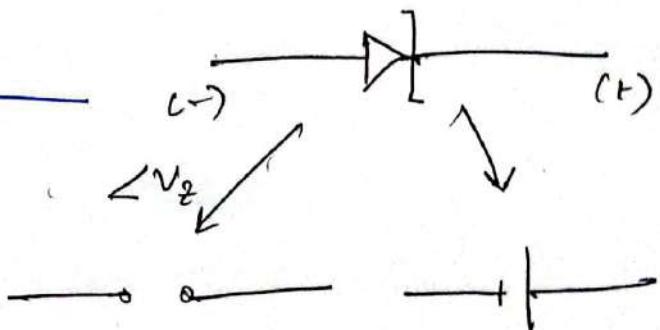
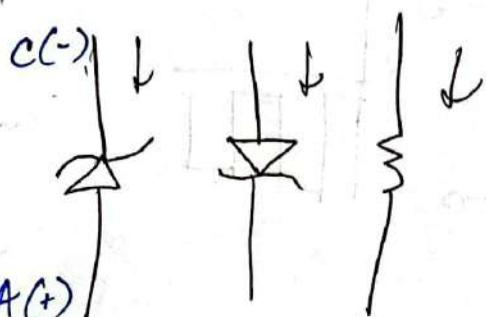
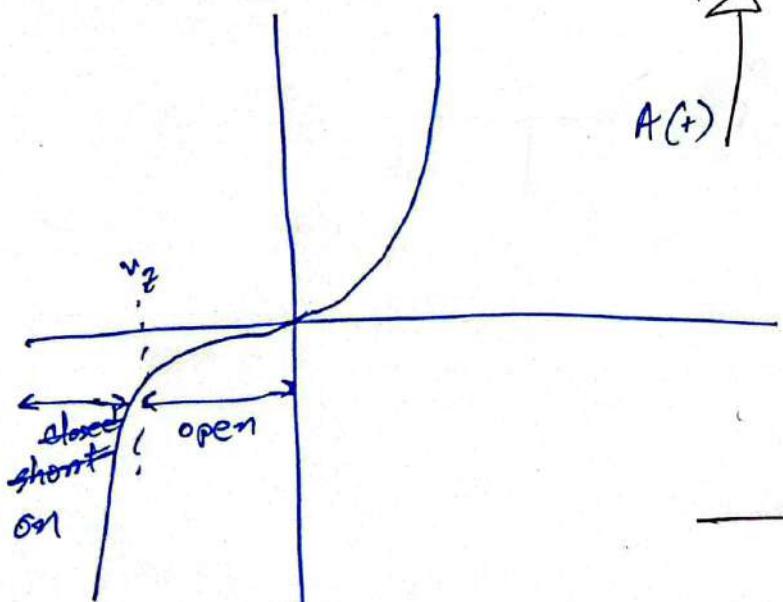
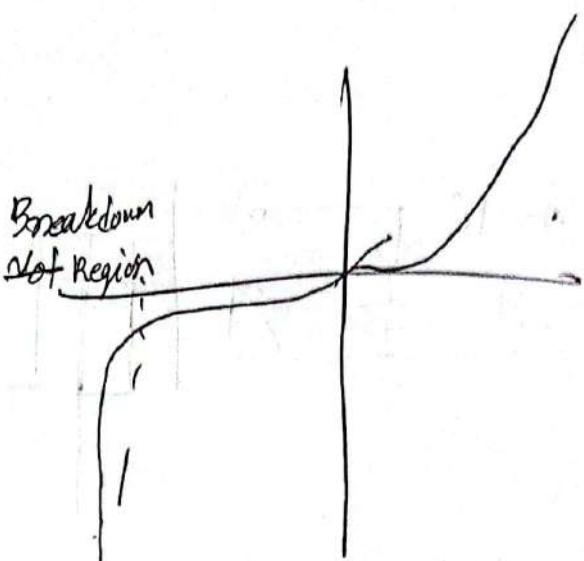
* The region that works in breakdown region is zener diode

* It works in reverse biased

* Replace it with the same voltage.

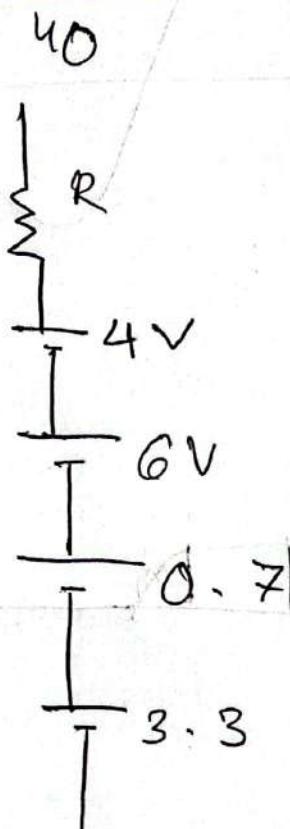
* Can be 1.8 to 200 V

* Temp dep sensitive



* When in forward, it works like silicon diode

#Slide Math

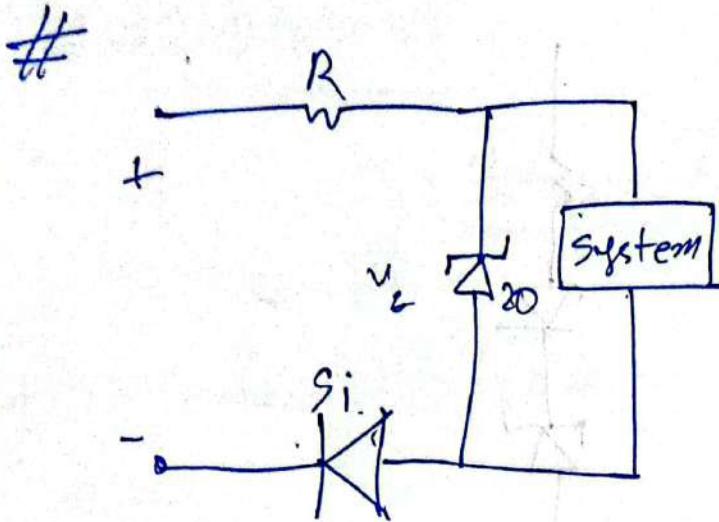


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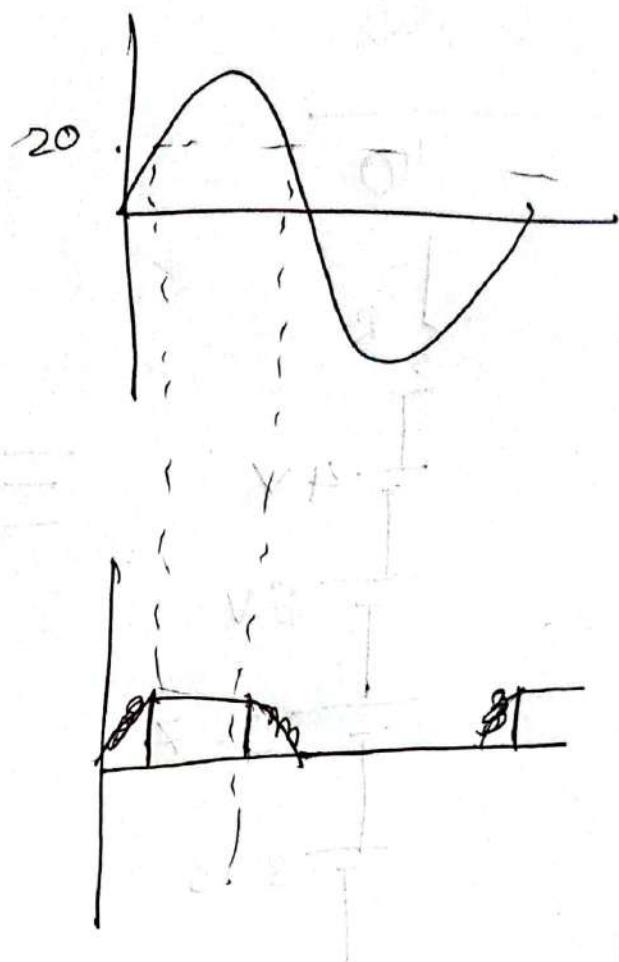


$$\therefore V = 40 - (4 + 6 + 3.3 + 0.7)$$
$$= 26$$

$$\therefore I = \frac{V}{R}$$

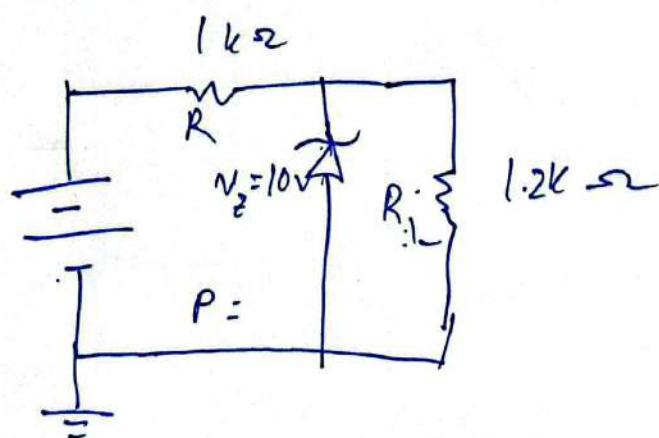


Draw waveform



Determine V_L , V_R , I_2 , P_2

Repeat with $R_L = 3 \text{ k}\Omega$



Using Voltage divider rule's

$$V_{R_L} = \frac{1.2}{1 + 1.2} \times 10 \\ = 8 \dots$$

V_2 will not activate

$$\therefore V_L = 8 \dots$$

$$\therefore V_R = 10 - 8 \dots \\ = 2 \dots$$

$$\therefore I_2 = 0 \\ P_2 = 0$$

When $R_L = 3$,

$$V_L = \frac{3}{3+1} \times 4 \\ = 12$$

$$\therefore V_L = 10V; [Zener is on]$$

$$\therefore V_R = 16 - 10 \\ = 6V$$

$$\therefore V = IR$$



Use other branch



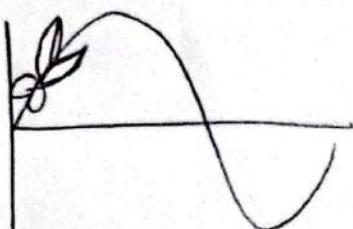
$$\therefore I - I_{R_L} = I_2$$

$$\therefore R_Z = VI$$

#Designers Voltage Problem

[Slide math.. Use Brain]

Message to future self: Good Luck :)

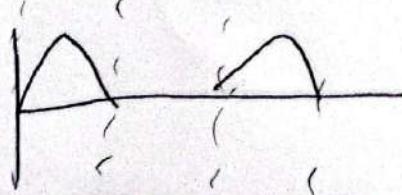
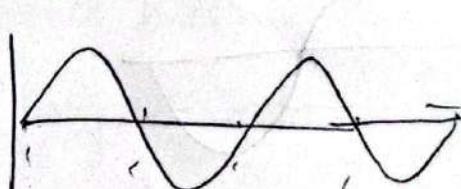
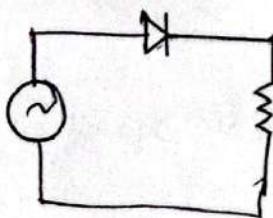
Expt - 3Clippers:

clippers removed signed voltage
above/below a specified level

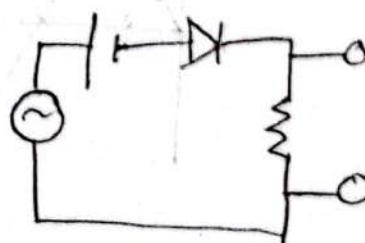
4 types:

- i) Positive Clipper cut  series
- ii) Negative " "  parallel
- iii) Biased " "
- iv) Combinational " "

* Positive Clipper:
(series)

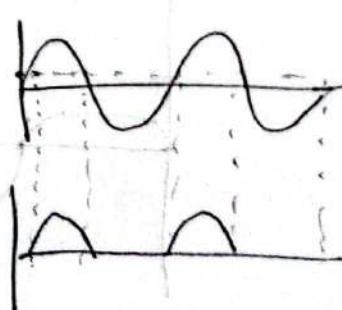


* Biased (series) Clipper:



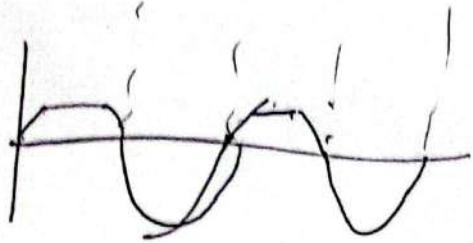
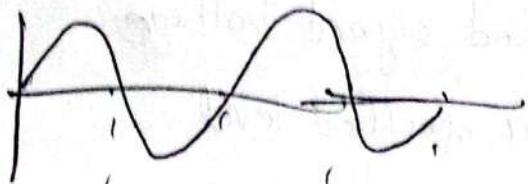
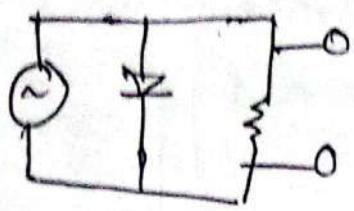
For $(0 \text{ to } \frac{\pi}{2})$ positive half cycle,

when $v_s < (V_b + V_D)$
→ diode off

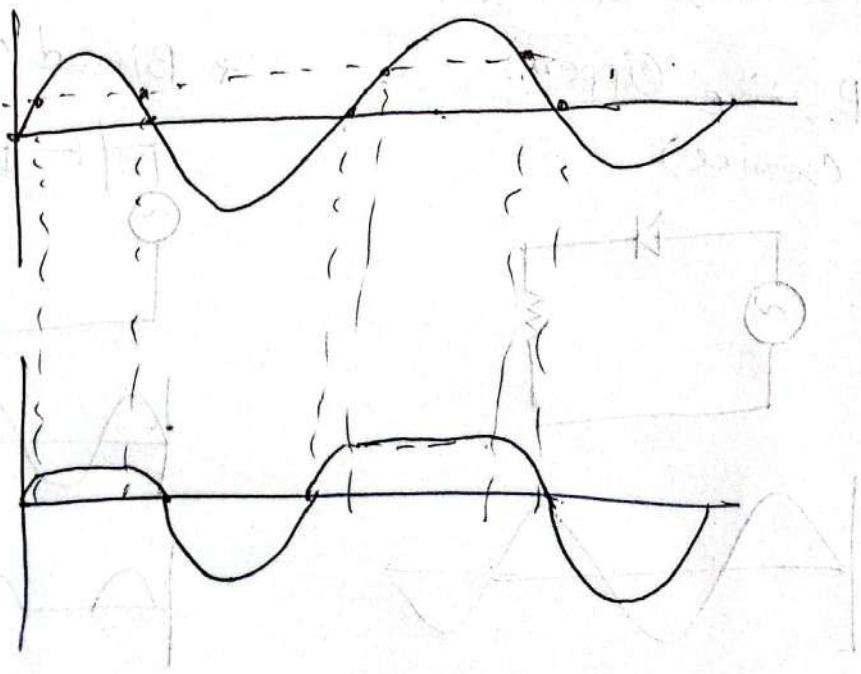
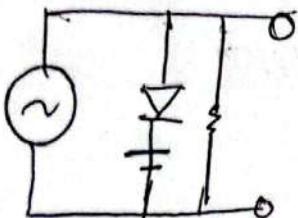


when $v_s \geq (V_b + V_D)$
→ diode on

* Positive Clipper (Parallel):



* Parallel Positive Clipper: (Bridged)



Expt 04 : Zener Diode Applications.

Normal Diode

- i) lightly doped and hence depletion region is thick
- ii) Depletion Electric field generated at depletion region is ^{not that} strong
- iii) Due to low electric field, current can't flow in the reverse connection
- iv) Breakdown is called avalanche region
- v) Can't be operated in reverse bias

vi) Symbol: 

Zener Diode

heavily doped and hence depletion region is thin.

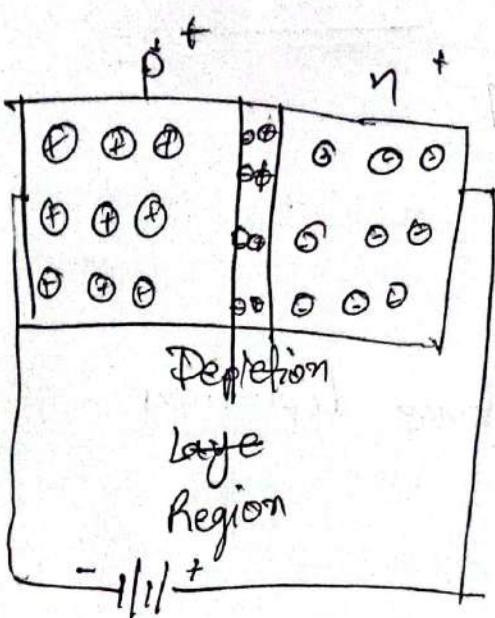
② Electric field potential at the depletion region is ~~strong~~ strong because of heavy concentration of impurity within the depletion layer.

Due to strong electric field, ~~can~~ electrons can flow in the reverse condition.

Breakdown is called Zener breakdown

In reverse bias, it can hold a constant voltage

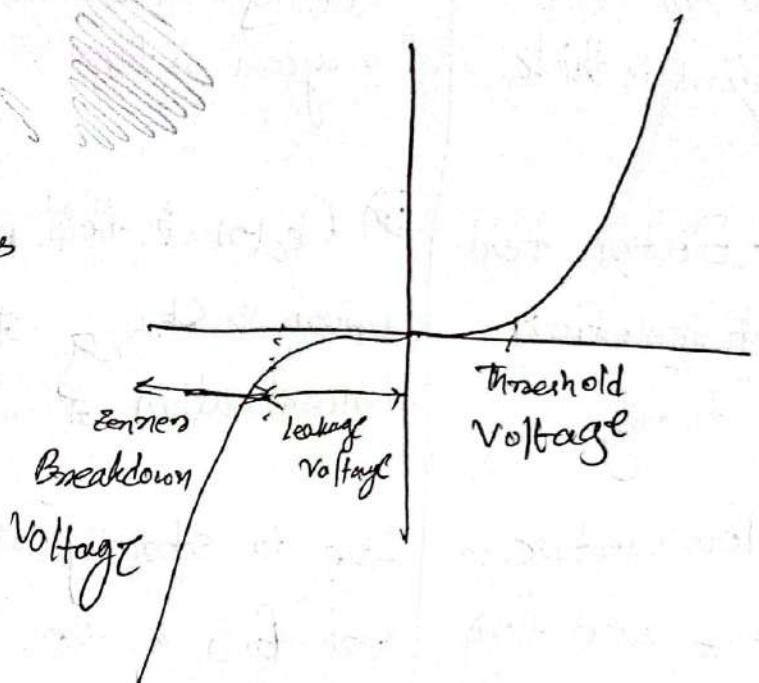
Symbol: 



Electric field of depletion layers:

$> 300 \text{ kV/cm}$

fig: Internal Schematics
of Zener Diode



C-9 (W-7)

20/05/24

Bipolar Junction Transistor

(Transistor of College)

27/05/24

Monday

Clippers

Quiz - 2

Clipper, Clamper
and Zener Diode

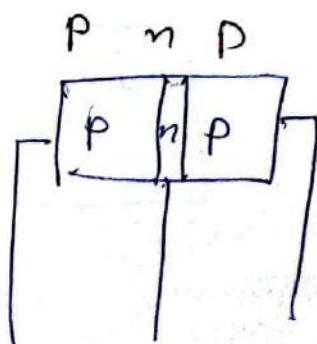
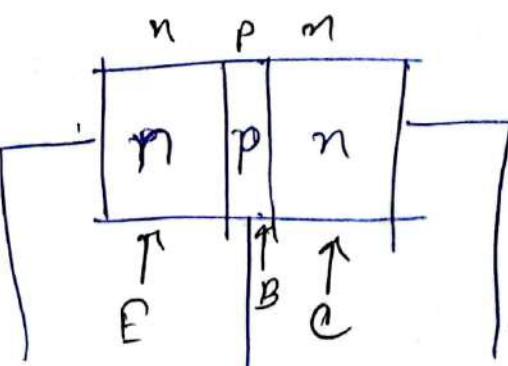
* Construction

* Three layers

- Two n-type + One p-type : $n-p-n$
- Two p-type + One n-type : $p-n-p$

* Three terminals :

- Emitter (E) : Heavy doping
- Base (B) : Light doping
- Collector (C) :
(more than B)



* Two types :

- BE
- BC

* Bipolar

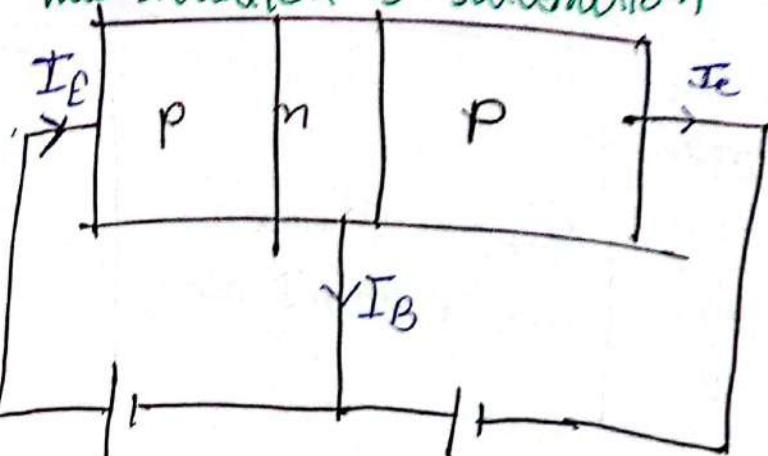
+ Operation

+ when both are forward, it will be neutral.

This situation is saturation

+ In pnp, holes will flow from emitter to collector

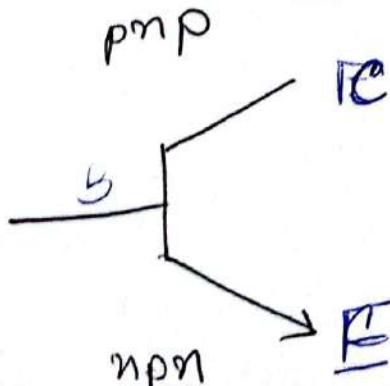
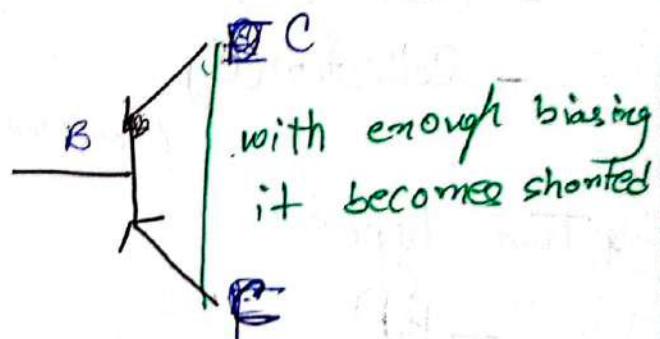
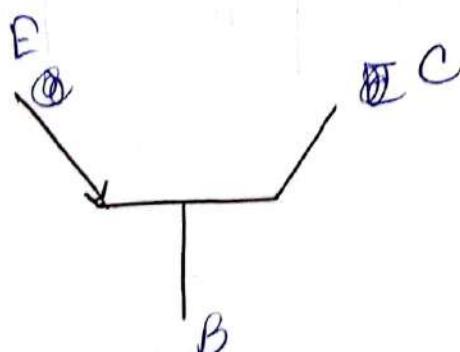
Emitter \rightarrow Base : Majority
Base \rightarrow Collector: Minority



$$\therefore I_E = I_B + I_C$$

+ In npn, opposite happens

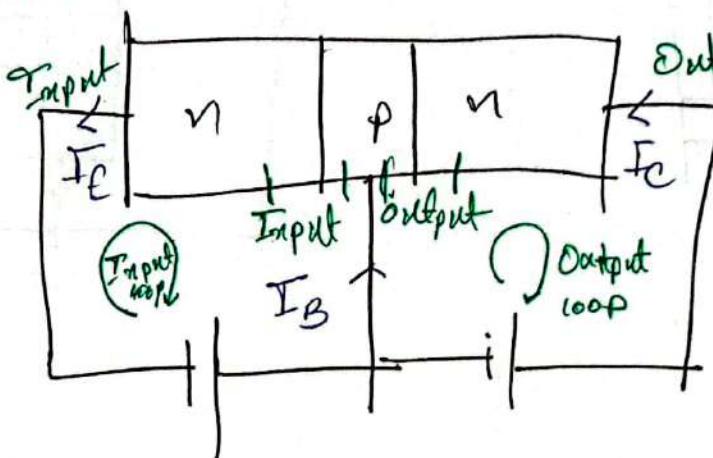
$$I_C = I_{C_{\text{major}}} + I_{C_{\text{minor}}}$$



* Classification:

i) Common Base:

(not important for non EEE people)

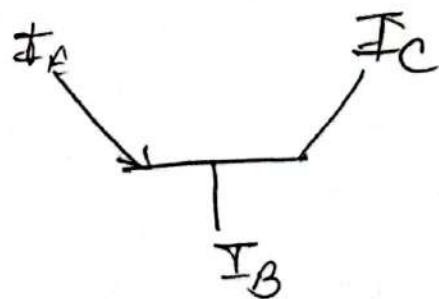


If I_B is always present in KVL, it is common base

Input:

$$\text{Voltage: } V_{BB} = 0.7 \text{ V}$$

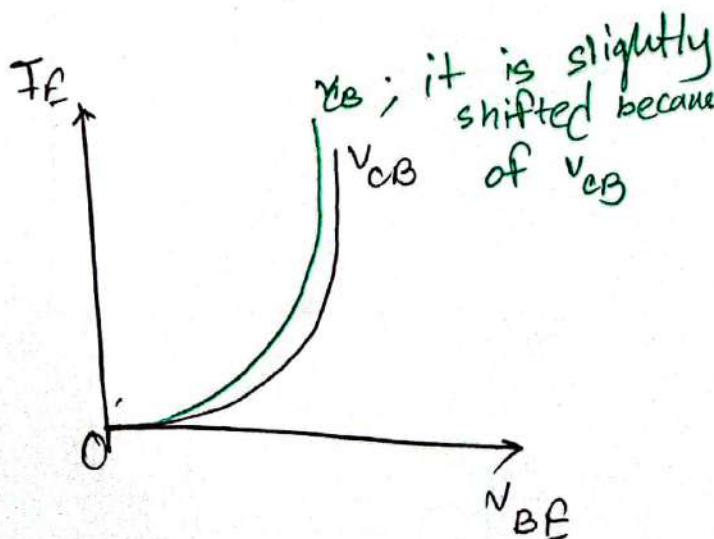
Current: I_E (mA)



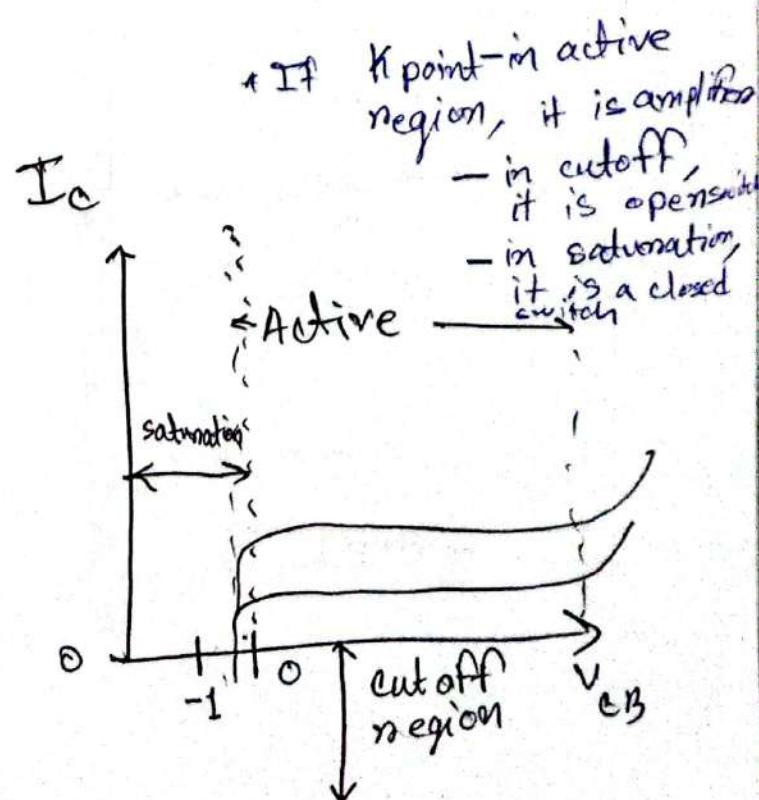
Output

Voltage: V_{CB}

Current: I_C



Input wave



$$\therefore \text{Current Gain} \Rightarrow \alpha_c = \frac{I_C}{I_E}$$

$$\boxed{\text{Gain} = \frac{\text{Output}}{\text{Input}}}$$



VFO or oscillator

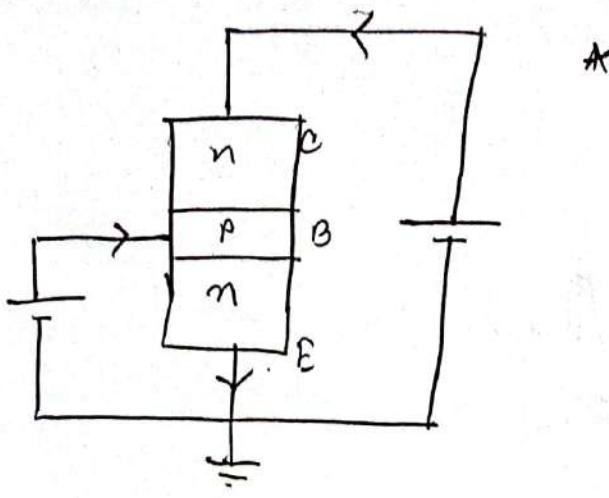
(Modulation)

RF amplifier

Detector



* Common Emitter :

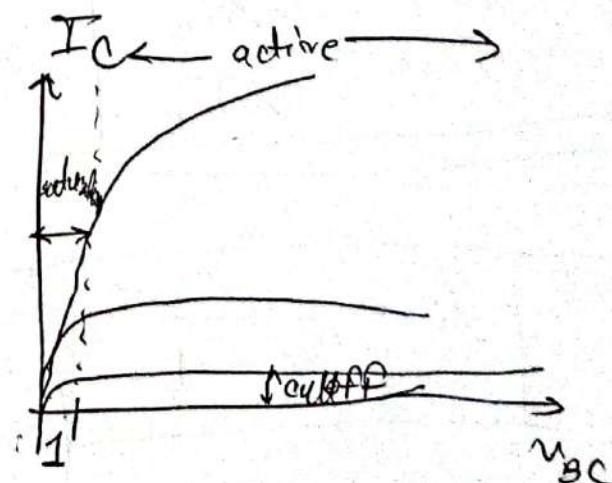
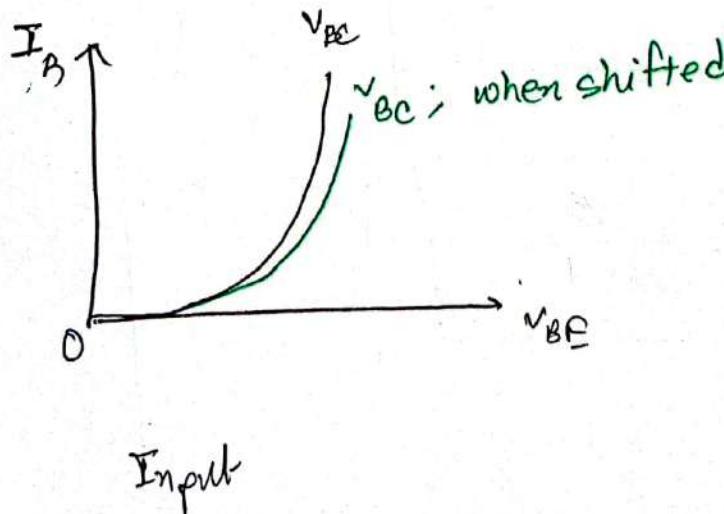


* Input

- Voltage : V_{BE}
- Current : I_B

* Output :

- Voltage : V_{BC}
- Current : I_C



$$\alpha = \frac{I_c}{I_E} ; \quad I_E = I_B + I_C$$

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{C\min}}{1 - \alpha}$$

* If $I_B = 0$, α is close to 0,
it acts as Buffer circuit \rightarrow input = output

.. Current Gain,

$$\beta_{dc} = \frac{I_C}{I_B} \approx 50 \rightarrow 400$$

$$\beta_{ac} = \left. \frac{\Delta I_C}{\Delta I_B} \right|_{V_{CE} = \text{constant}}$$

$$\beta = \frac{\alpha}{\alpha - 1}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

Common Collector

Almost same as common emitter

Good luck
future me

things are
same so just
use slide

C-10 ($\omega - z$)

DC

21/05/24

BJT Biasing

25/6/24

CT - 3

BJT Construction
+ (DC + AC) Biasing

* Characteristic curves are important for lab final

* Biasing: To get an exact response

* Do both cases: one for AC, one for DC

* For DC, all reactive elements should be removed.

* If subscripts are capital, they are for DC

For Input Loop:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \beta = \frac{I_C}{I_B}$$

$$\therefore I_C = \beta I_B$$

For Output Loop:

$$V_{CE} = V_{CC} - R_C \times I_C$$

$$V_{BE} = V_B - V_E \rightarrow 0$$

$$\therefore V_{BE} = V_B$$

$$\therefore V_{CE} = V_C$$

Example (Slide Math) (Fixed Bias)

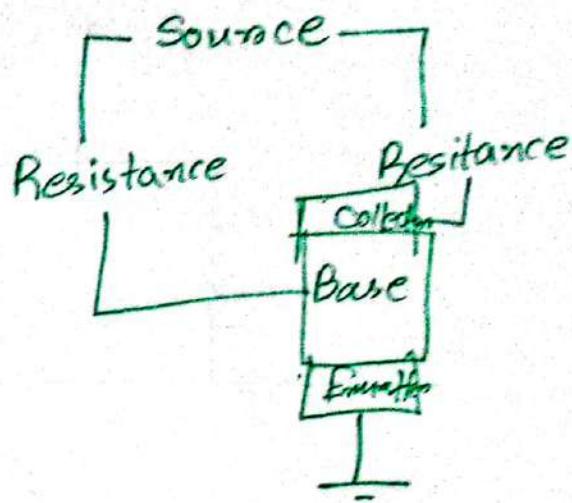
For DC,

$$V_{CC} = +12 \text{ V}$$

$$R_B = 240 \text{ k}\Omega$$

$$R_C = 2.2 \text{ k}\Omega$$

$$\beta = 50$$



a). $I_B = \text{_____}$ Input Loop:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{240}$$

$$= 0.047 \text{ mA (Ans)}$$

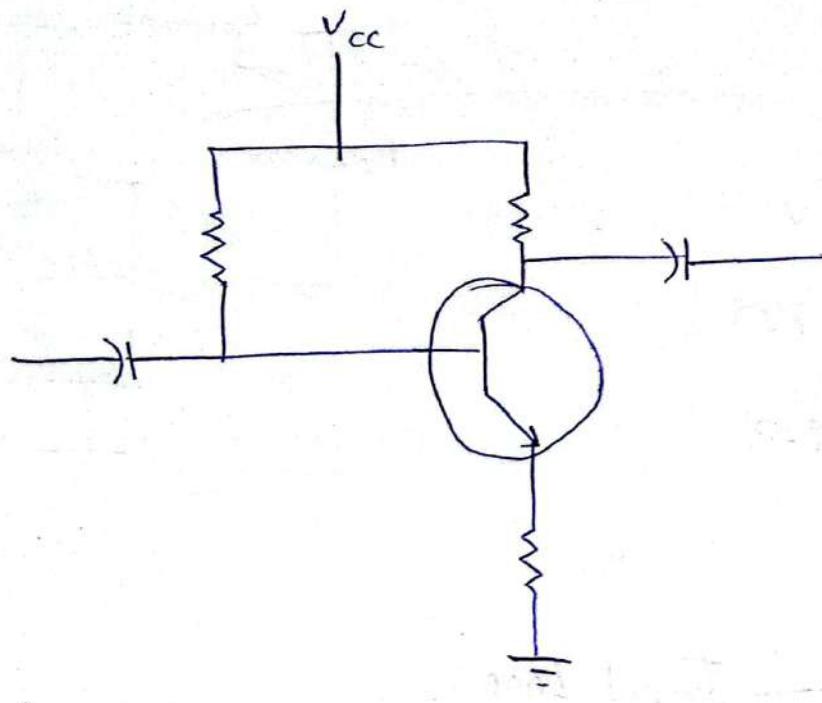
$$I_C = \beta \cdot I_B = 50 \times 0.047$$

$$= 2.35 \text{ mA (Ans.)}$$

b) $V_{CE} = V_{CC} - I_C R_C = 6.83 \text{ V}$

c) $V_{BE} = V_B - V_E = V_B = 0.7 \text{ V}$
 $V_{CE} = V_C - V_E = V_C = 6.83 \text{ V}$
 $\therefore V_{BC} = V_B - V_C = 0.7 - 6.83 \text{ V} = -6.13 \text{ V}$
 $\therefore \text{Base-Emitter is in reverse bias}$

* Emitter Bias:



Input Loop:

$$* I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} = \frac{V_{CC} - V_{BE}}{R_B + F_E R_E}$$

$$* I_C = \beta I_B$$

Output Loop:

$$* V_{CE} = V_{CC} - I_C (R_C + R_E); \quad [\text{when } I_B \rightarrow 0, \quad F_E = I_C]$$

$$* V_E = \beta I_E / R_E$$

$$* V_B = V_{BE} + V_E \quad , \quad V_C = \frac{V_{CE} - V_E}{= V_{CC} - I_C R_C}$$

Example :-

$$I_B = \frac{V_{cc} - V_{BE}}{R_E + R_L}$$

Part me
has headache

Its in slide
so DIY

C-11 (W-8)

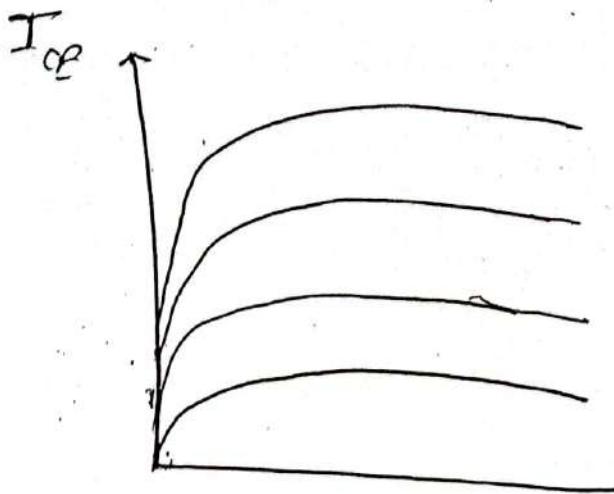
BJT DC BiasingLoad Line Analysis:Fixed Bias

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$V_{CE} = V_{cc} - I_B R_B$$

$$\therefore V_{CE} = V_{cc} \quad | \quad I_C = 0 \text{ mA}$$

$$\therefore I_C = \frac{V_{cc}}{R_B} \quad | \quad V_{CE} = 0 \text{ V}$$



Output Curve

∴ We will work with output loop

Slide Math : DIY

Self/Emitter Bias:

$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta + D)\beta_p}$$

$$\text{and, } V_{CB} = V_{cc} - I_C(R_C + R_E)$$

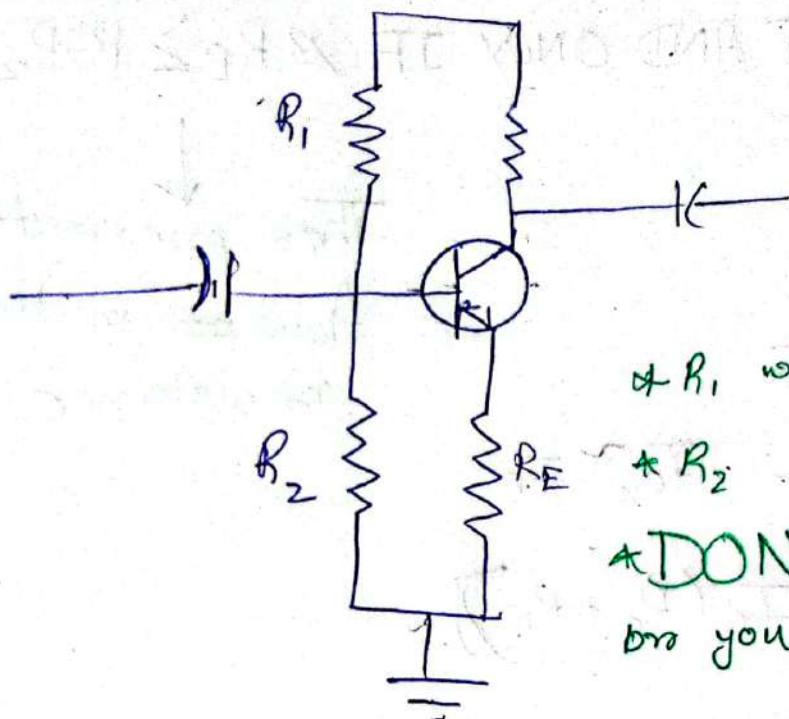
$$\therefore V_{CE} = V_{cc} \quad | \quad I_C = 0$$

$$\therefore I_C = \frac{V_{cc}}{R_C + R_E} \quad | \quad V_{CE} = 0$$

* Question cannot be complicated from here.

Slide Math : DIY

Voltage Divider Bias



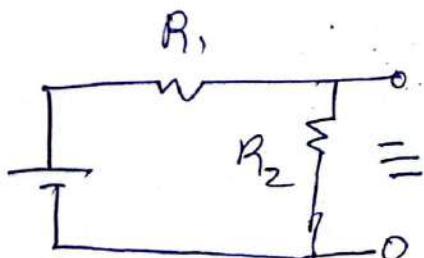
* R_1 will be the one above
" " " " " below

* R_2 " " "

* DONT mess it up
but you can derive it yourself

Exact Analysis:

Circuit =



$$R_{th} = R_1 \parallel R_2$$

$$E_{th} = \frac{R_2}{R_1 + R_2} \times V_{ac}$$

This is why

$$I_B = \frac{E_{th} - V_{BE}}{R_{th} + (\beta + 1)R_E}$$

Applied Approximate Analysis

Can be done IF AND ONLY IF $\beta R_E \geq 10 R_2$

$$\therefore V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$\therefore V_E = V_B - V_{BE}$$

$$\therefore I_E = \frac{V_E}{R_E} \quad I_C \approx I_E$$

$$\therefore V_{O_E} = V_{CE} - I_C (R_C + R_E)$$

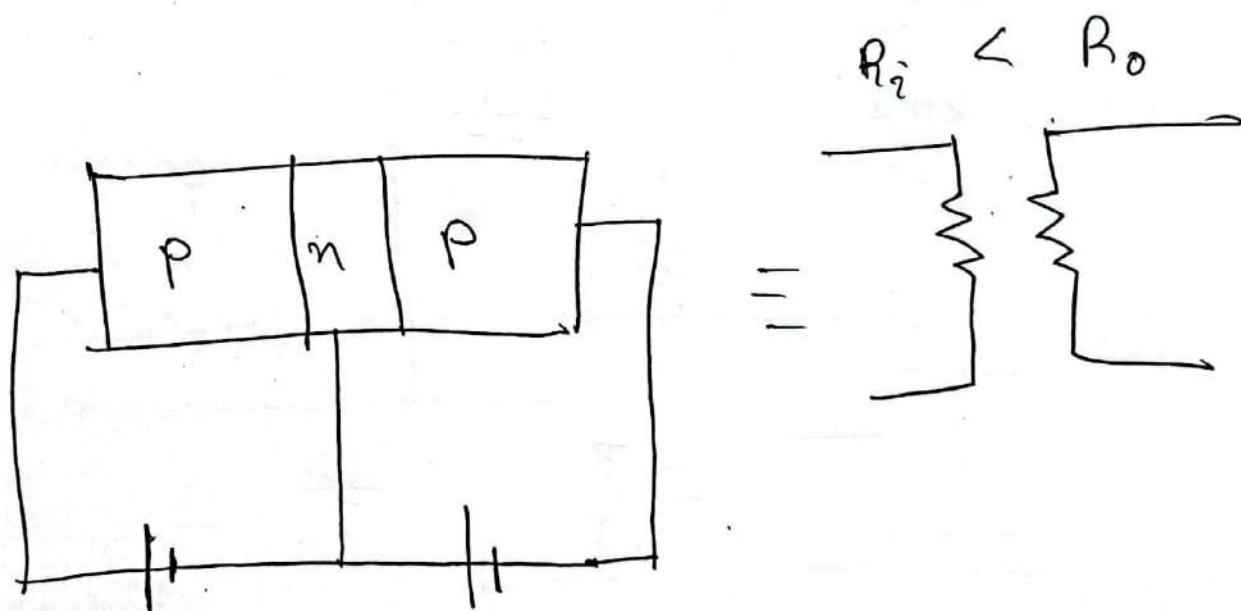
↓
This prevents electricity
flow ~~out~~ in the big
resistance

BJT AC Analysis

* BJT is a current control device

+ We find gain here

* Transistor = Transfer of resistance - on



* Find Z_i , Z_o , A_i , $A_{\text{something}}$

+ r_e model $>$ Hybrid π Model $\xrightarrow{\text{Equivalent}} \xrightarrow{\text{For everything else}} \xrightarrow{\text{For nothing because no one cares,}}$ Hybrid π Model

For transistor

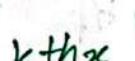
For everything else

For nothing because no one cares,

AC Equivalent Circ.

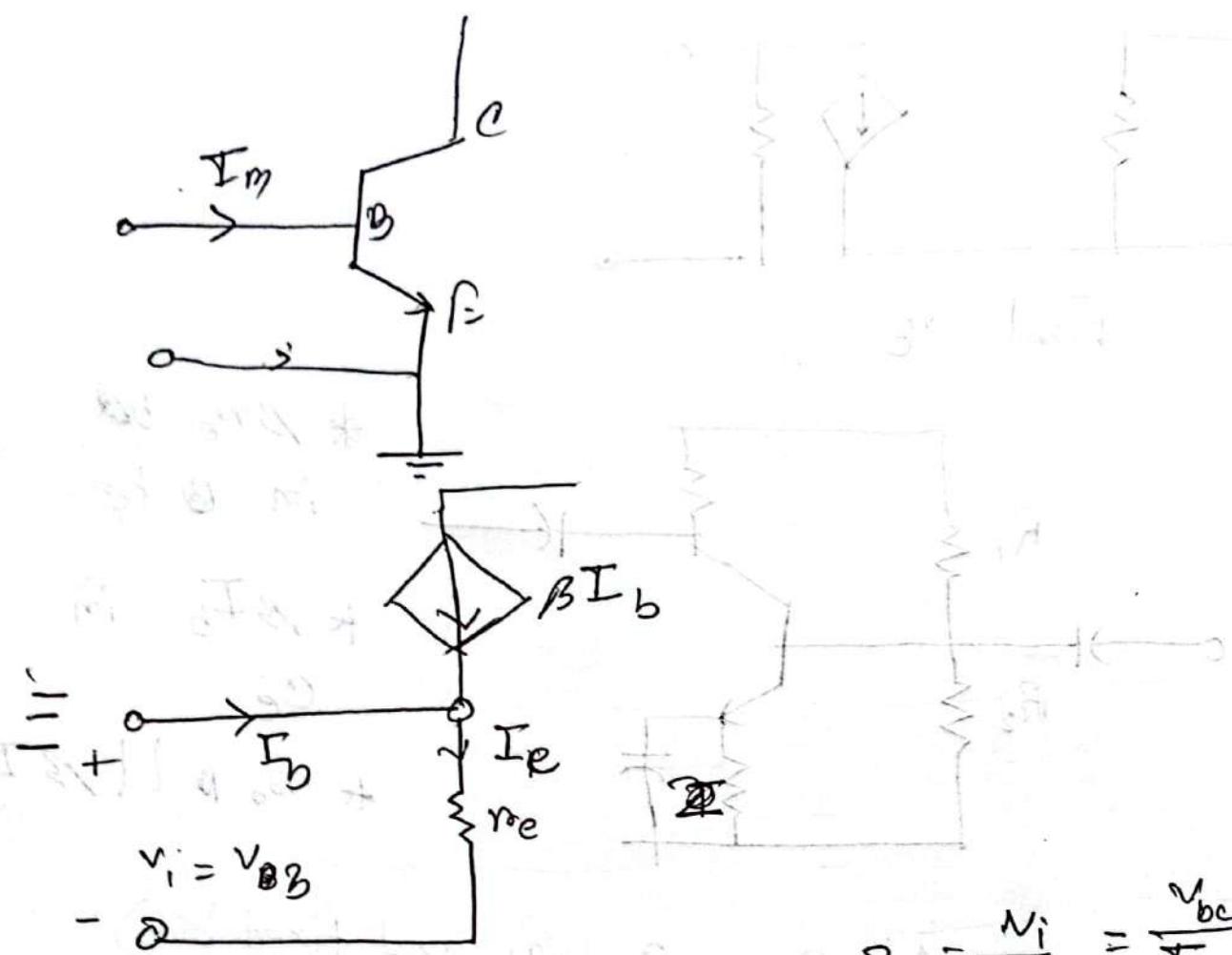
1. Set all dc source to zero
 2. Capacitors are to be shorted
 3. Remove all bypassed element
 4. Redraw in a logical (and convenient form)
*Dear Future Me,
Draw circuit from Slide*

Dear Future Me,
Draw Circuit from Slide

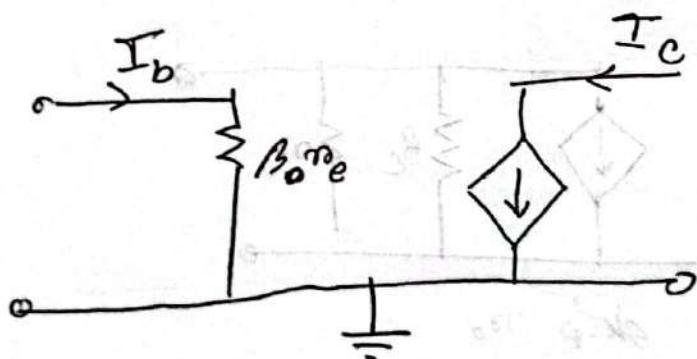


- ## 5. Replace At Transistor Model.

Fig me Transistor model



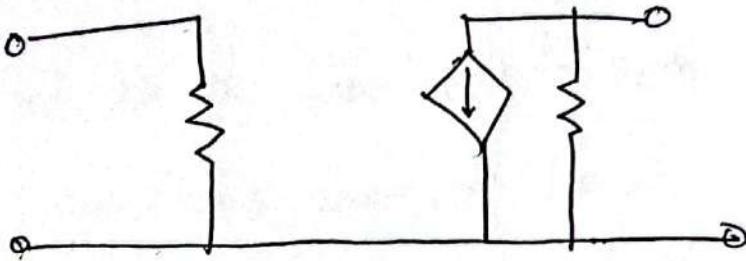
$$Z_i = \frac{N_i}{I_b} = \frac{v_{bc}}{I_b}$$



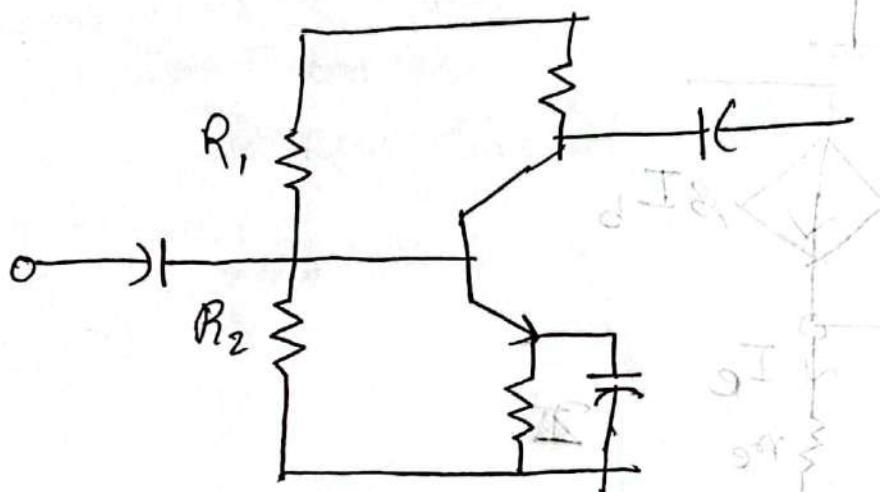
$$v_{be} = I_e r_{be}$$

$$\begin{aligned} Z_i &= (\beta + 1) r_{be} \\ &= \beta r_C \end{aligned}$$

Improved BJT circuit

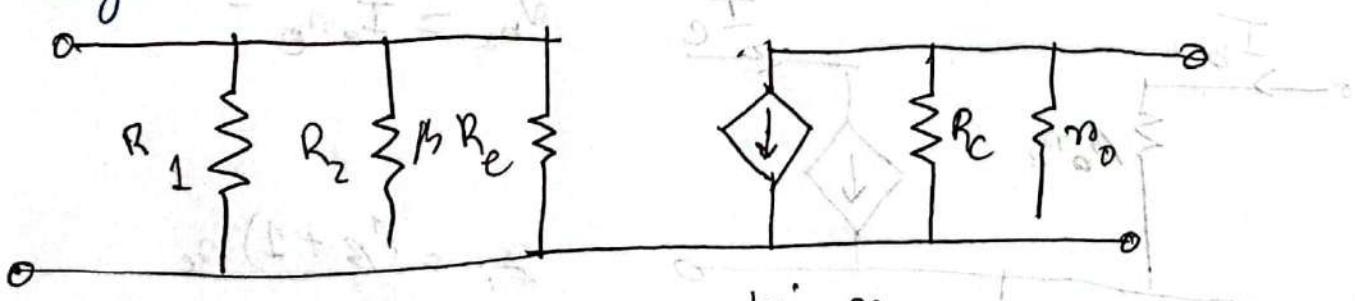


Final r_e



* βr_e b/w
in Q₀ be
* βI_b in
C_e
* $r_o = 1/\beta I_g$

Voltage divider (Do for self-bias and fixed bias)



If $r_o \geq 10^{\text{mV}}$, we can skip r_o

[Check slide for Formulae Derivation]

$$A_o = \frac{V_o}{V_i} = -\frac{R_C || R_E}{R_E}$$

$$r_E = \frac{26 \text{ mV}}{I_E}$$

- 7 (w-o)

05/08/24

Bipolar = Two Both ~~sides~~ holes and e⁻ flow

F - R \rightarrow Active

R - R \rightarrow Cutoff. (switch off)

F - F \rightarrow saturation (switch on)

C-13 (10-10)

24/06/24

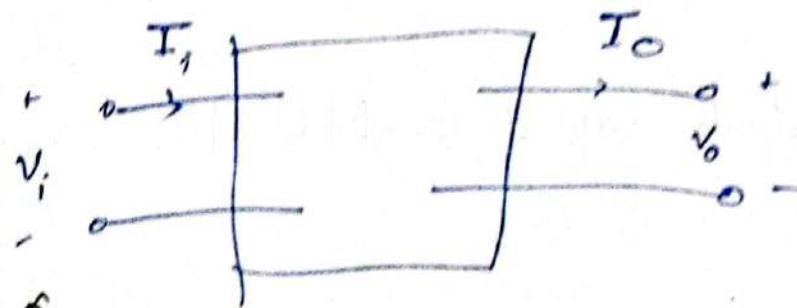
10^{-3}

$\underline{10^3}$

$\underline{\underline{10^{-2}}}$

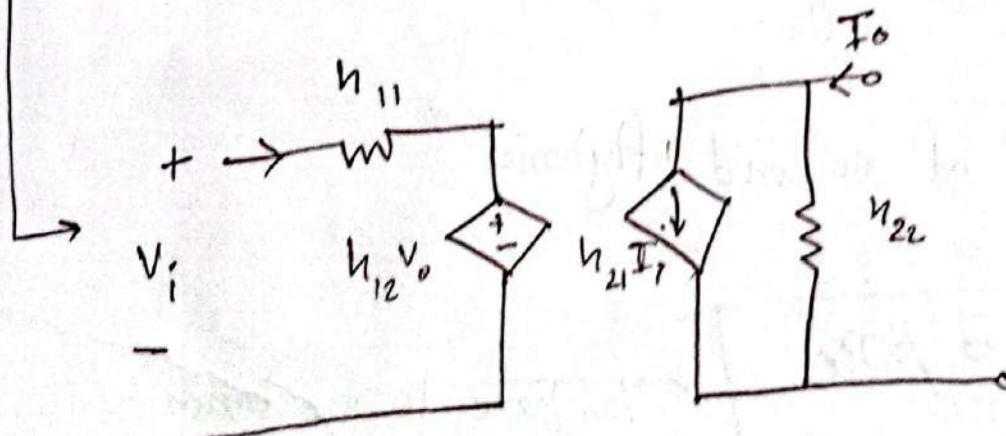
Hybrid Equivalent Model

* Any 2 port System will have 3 poles



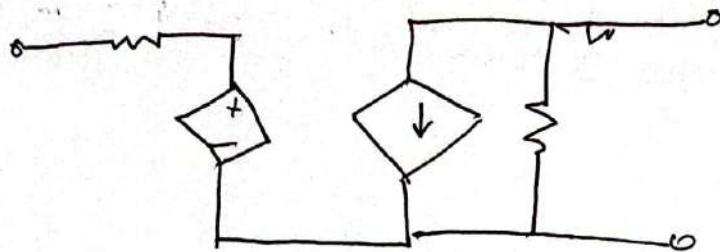
$$\begin{cases} v_i = h_{12} I_1 + h_{12} \frac{v_o}{r_2} \\ I_o = h_{21} I_o + h_{21} v_o \end{cases}$$

a. resistance = impedance
b. conductance = admittance

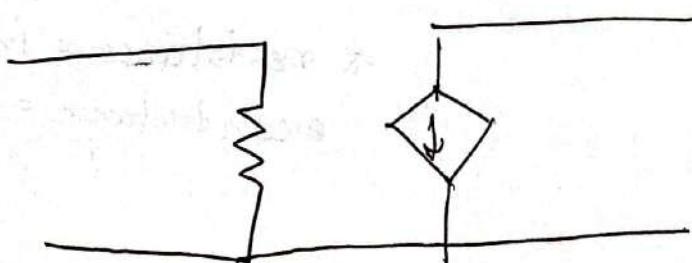


$$h_{11} =$$

* For CP:



* AC equivalent circuit is MUST



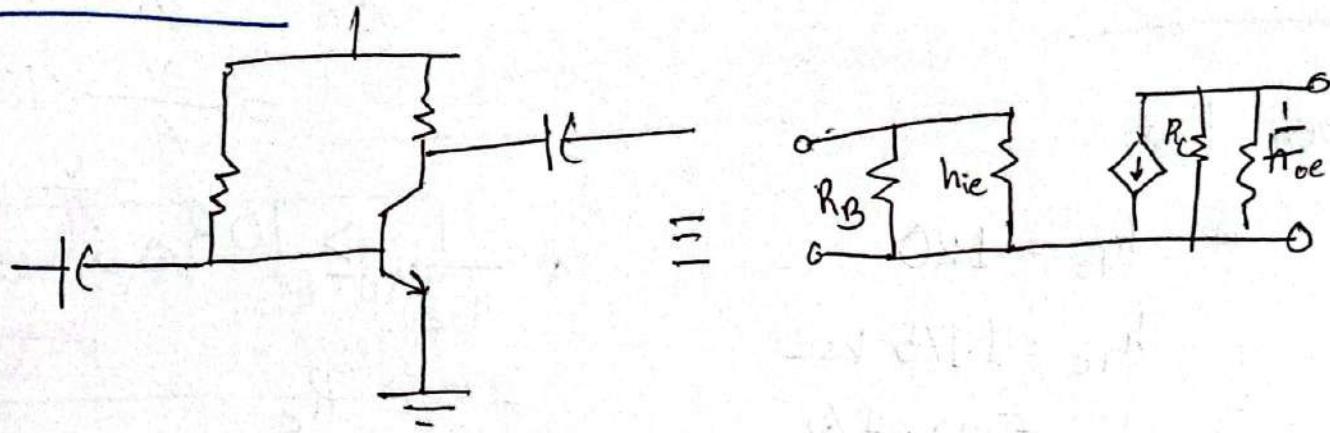
Approximate Hybrid Equivalent

* Using Comparison of r_e and hybrid

$$\boxed{\begin{aligned} h_{ie} &= \beta r_e \\ h_{fe} &= \beta \end{aligned}}$$

* You have to use brain
in exam

* Fixed Bias :



$$* z_i = R_B \parallel h_{ie}$$

$$* z_o = R_C \parallel \frac{1}{h_{oc}}$$

$$* V_o = -h_{fe} \times \frac{V_i}{h_{ie}} \times \left(R_C \parallel \frac{1}{h_{oc}} \right)$$

$$* A_v = -\frac{h_{fe}}{h_{ie}} \times \left(R_C \parallel \frac{1}{h_{oc}} \right)$$

$$* A_i = h_{fe}; R_B \uparrow$$

* Self Study : Do for the rest

Slide Math:

Given that,

$$h_{fe} = 120$$

$$h_{ie} = 1.175 \text{ k}\Omega$$

$$h_{oe} = 20 \mu\text{A/V}$$

Use formula $R_B = 330 \text{ k}\Omega$

$$R_C = 2.7 \text{ k}\Omega$$

$$V_{cc} = 8 \text{ V}$$

$$(i) Z_i = R_B \parallel h_{ie} = \frac{(330)(1.175)}{330 + 1.175} = 1.17 \text{ k}\Omega \text{ (Ans)}$$

$$(ii) Z_o = R_C \parallel \frac{1}{h_{oe}} = \frac{R_C \times \frac{1}{h_{oe}}}{R_C + h_{oe}} = \frac{(2.7)(\frac{1}{20})}{2.7 + \frac{1}{20}} =$$

$$(iii) \text{ Hence, } \frac{1}{h_{oe}} = \frac{1}{20 \mu\text{A/V}} = \frac{1 \text{ V}}{20 \times 10^{-6} \text{ A}} = \frac{10^5 \text{ V}}{20} \text{ k}\Omega$$

$$= 50 \text{ k}\Omega$$

$$\therefore Z_o = R_C \parallel \frac{1}{h_{oe}} = \frac{(2.7)(50)}{50 + 2.7} = 2.56 \text{ k}\Omega \text{ (Ans)}$$

$$(iv) A_v = - \frac{h_{fe} \times Z_o}{h_{ie}} = - \frac{(120)(2.56)}{1.175} = - 261.45 \text{ (Ans.)}$$

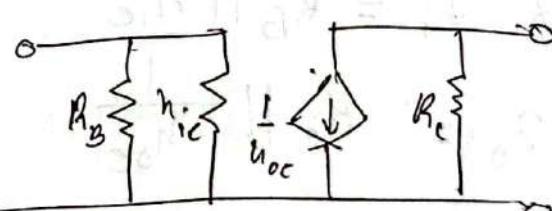
$$(v) A_i \approx h_{fe} = 120 \text{ (Ans.)}$$

$$\frac{V}{\mu\text{A}} = \frac{V}{A \times 10^6}$$

$$= \frac{V}{A} \times 10^6$$

$$* \frac{1}{h_{oe}} \geq 10R_C = \frac{V}{A} \times 10^3$$

$$Z_o \approx R_C$$



ANSWER

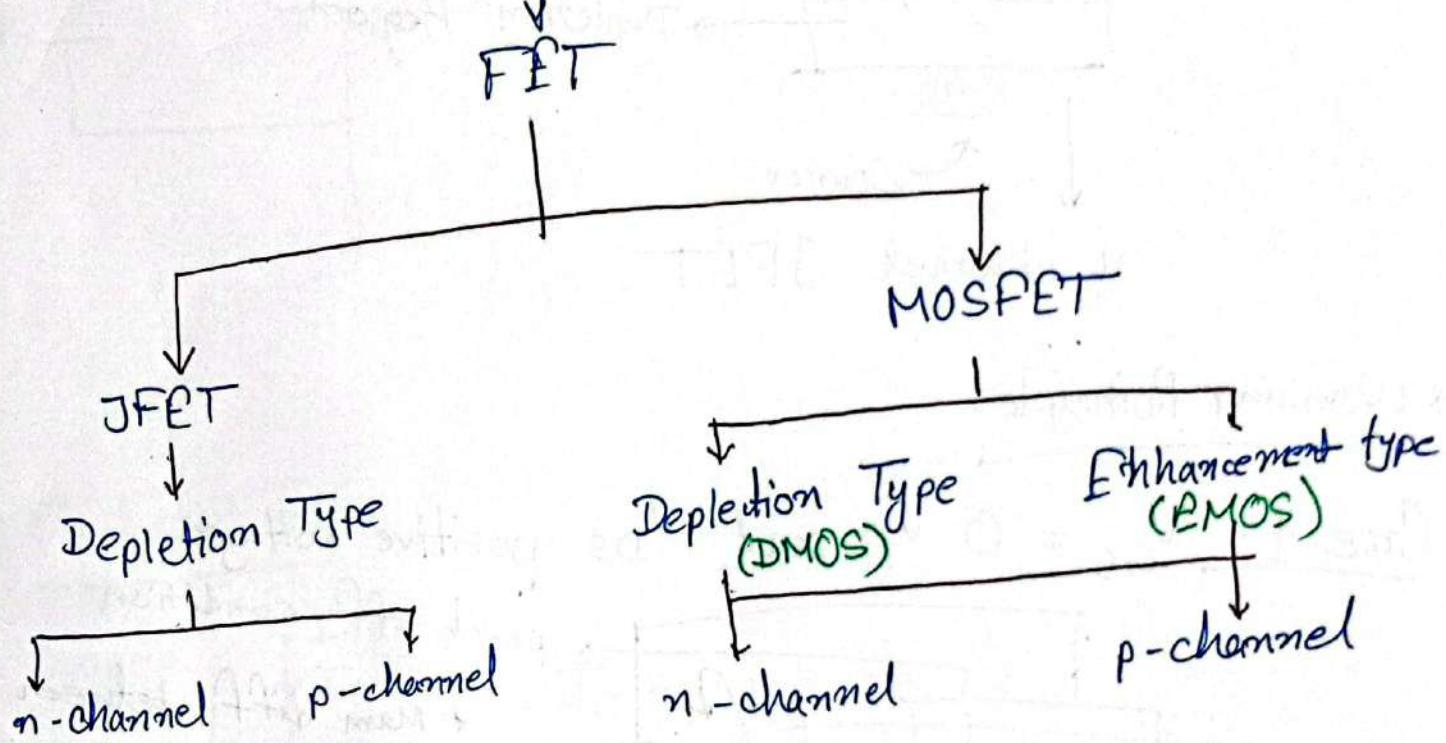
100
X 50
50
50
50
50

Field Effect Transistor Transistors

15/07/24
Q-4

Op-Amp
+ MOSFET

* Less Math, more theory
* More curve based question



* FET is voltage controlled device

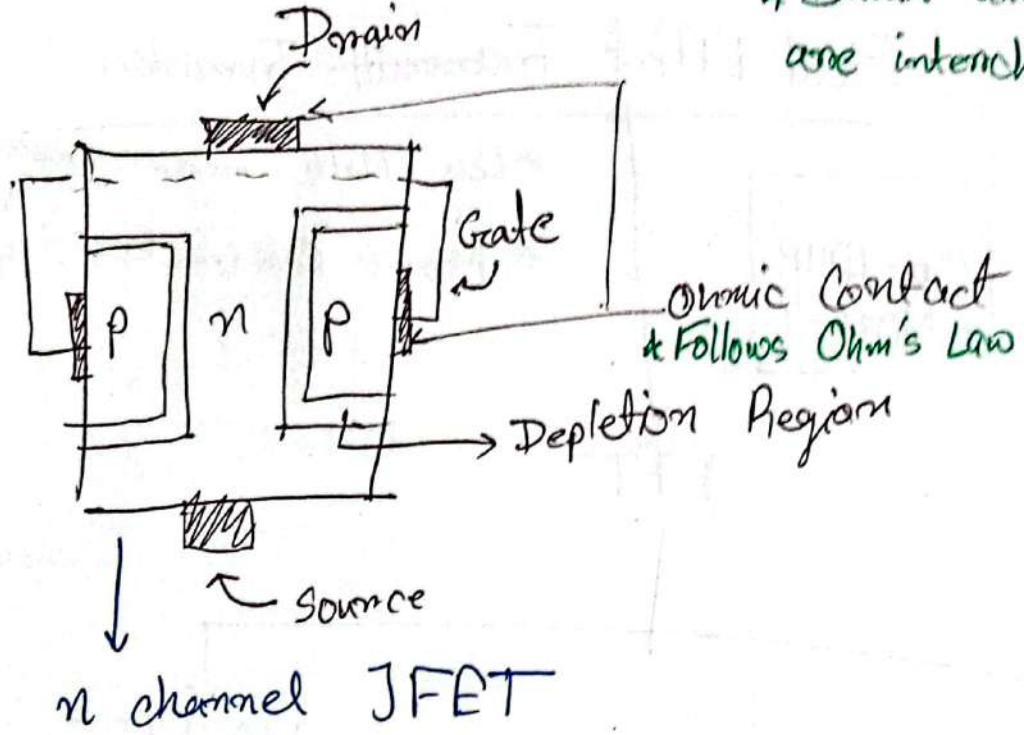
* $FET_{\text{sensitivity}} < BJT_{\text{sensitivity}}$

* FET is used more as switch than amplifiers.

* FET is less temperature sensitive

* $FET_{\text{size}} < BJT_{\text{size}}$

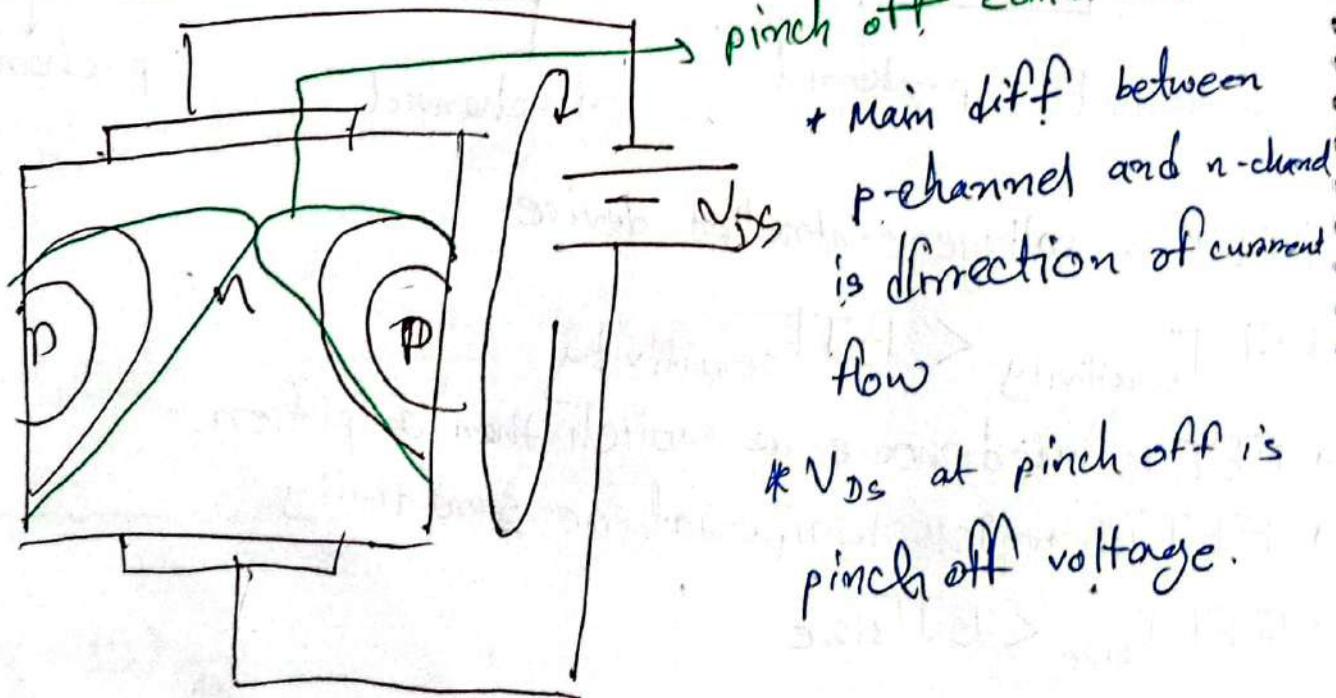
JFET:



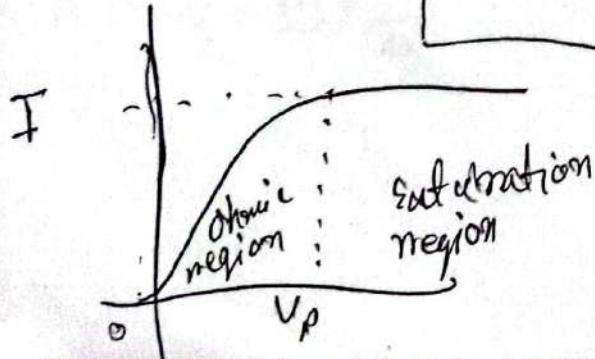
* Drain and source are interchangeable

* Working Principle:

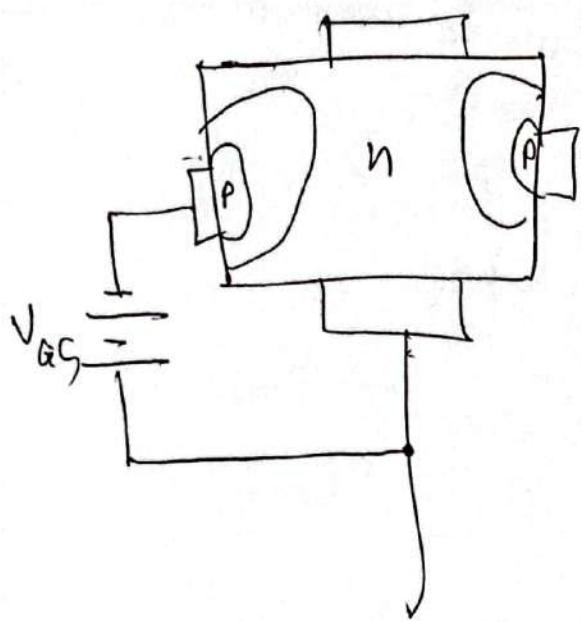
Case 1: $V_{GS} = 0 \text{ v}$ and V_{DS} positive voltage
pinch off condition



* V_{DS} at pinch off is pinch off voltage.



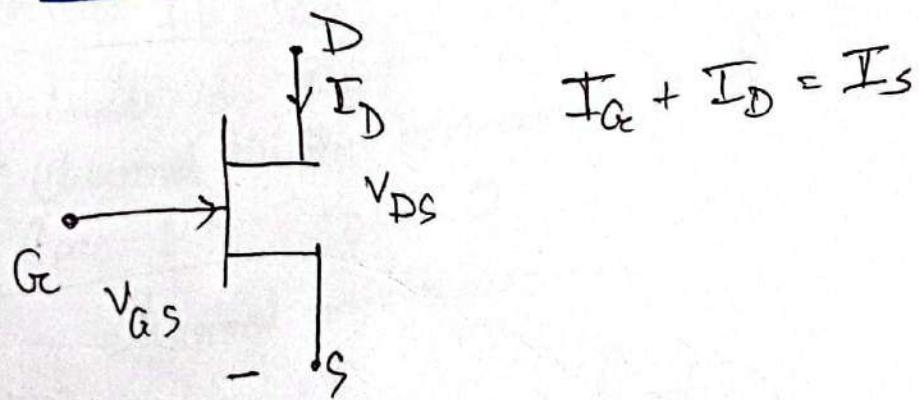
Case 2: $V_{GS} < 0V$



Idk why it keeps happening in EEP but just follow slides future me



JFET Symbol:



④ Transfer Characteristic:

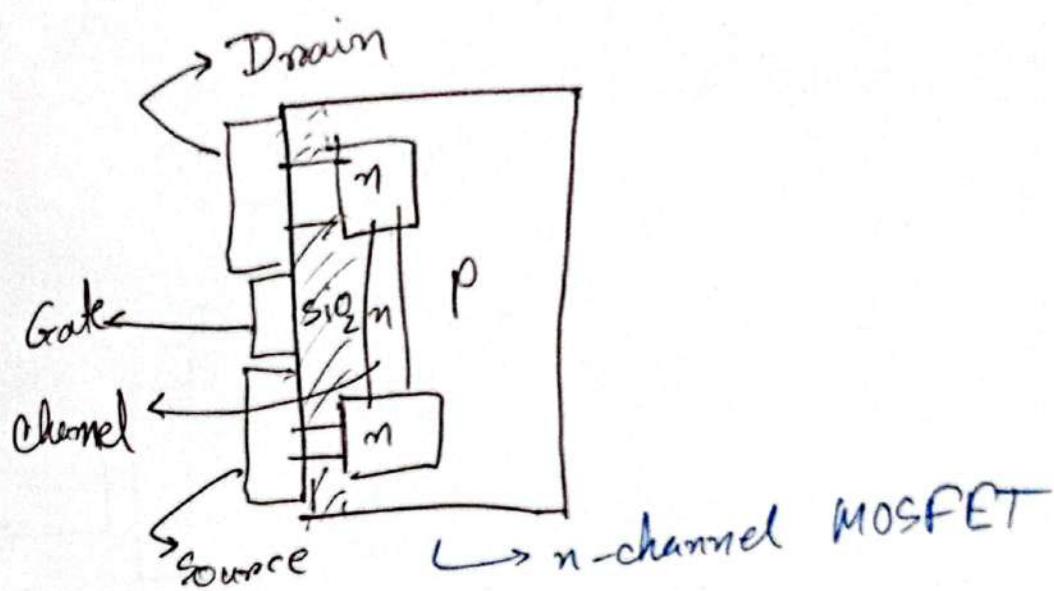
$$I_D = I_{DSS} \left(1 - \frac{V_{DS}}{V_P}\right)^2 + \text{Can be used to do math}$$

⑤ Summary:

[check slide]

MOSFET:

→ Metal-Oxide-Semiconductor FET



Working Principle:

* Case 1: $V_{GS} = 0$, $V_{DS} > 0$

* Similar to JFET

* Channel width increases

* Case 1.5: $V_{DS} < 0$

Channel width reduces

Saturation comes first

L-8 (W-10)

Exp - E

26/06/24

BJT - Biasing Ckt

1

→ Put Pot

→ Set it to 5 V

→ measure Res. $I_C = \frac{Pot}{R}$

→ Change BJT



Q 100kΩ

Q 10kΩ

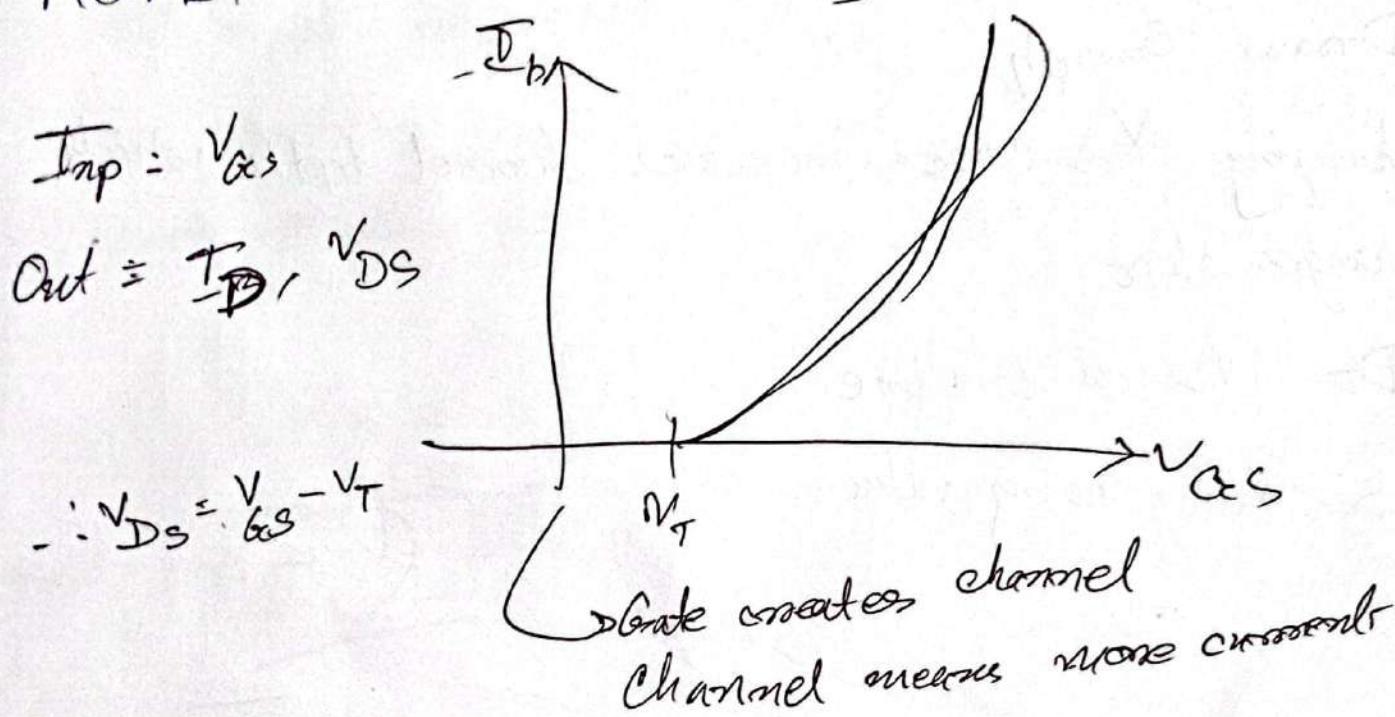
Q 2.2kΩ

Q 500Ω
(Ans)

Frequency Response of a CF Amplifier and Measured
of Input and Output Impedance

Exp - 8

MOSFET \rightarrow Used for Switching



Get $V_{GS} = 3 \text{ V}$

Put multimeter across DS



5

2.185

6

7

80

15

20

22

1. Draw Graph

2. Changing V_{AS} causes increases channel depth which changes slope

3. Do KVL and load line

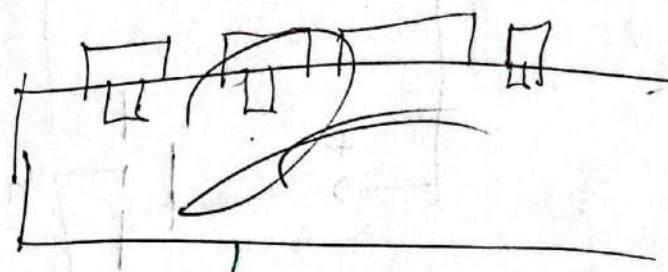
4. Saturation using value.

CMOS \rightarrow 2 E-type

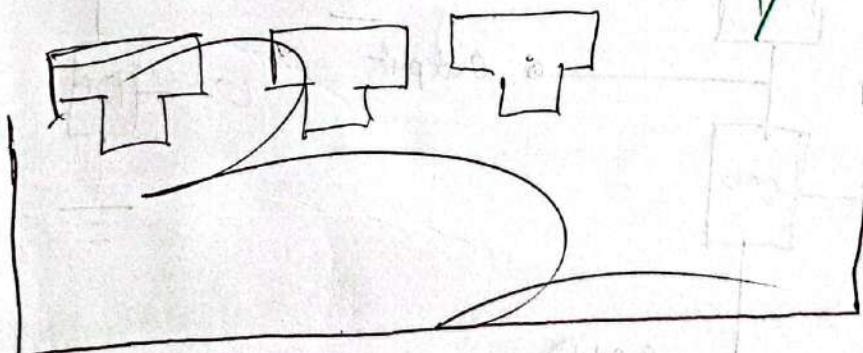
→ Complement MOSFET

Application:

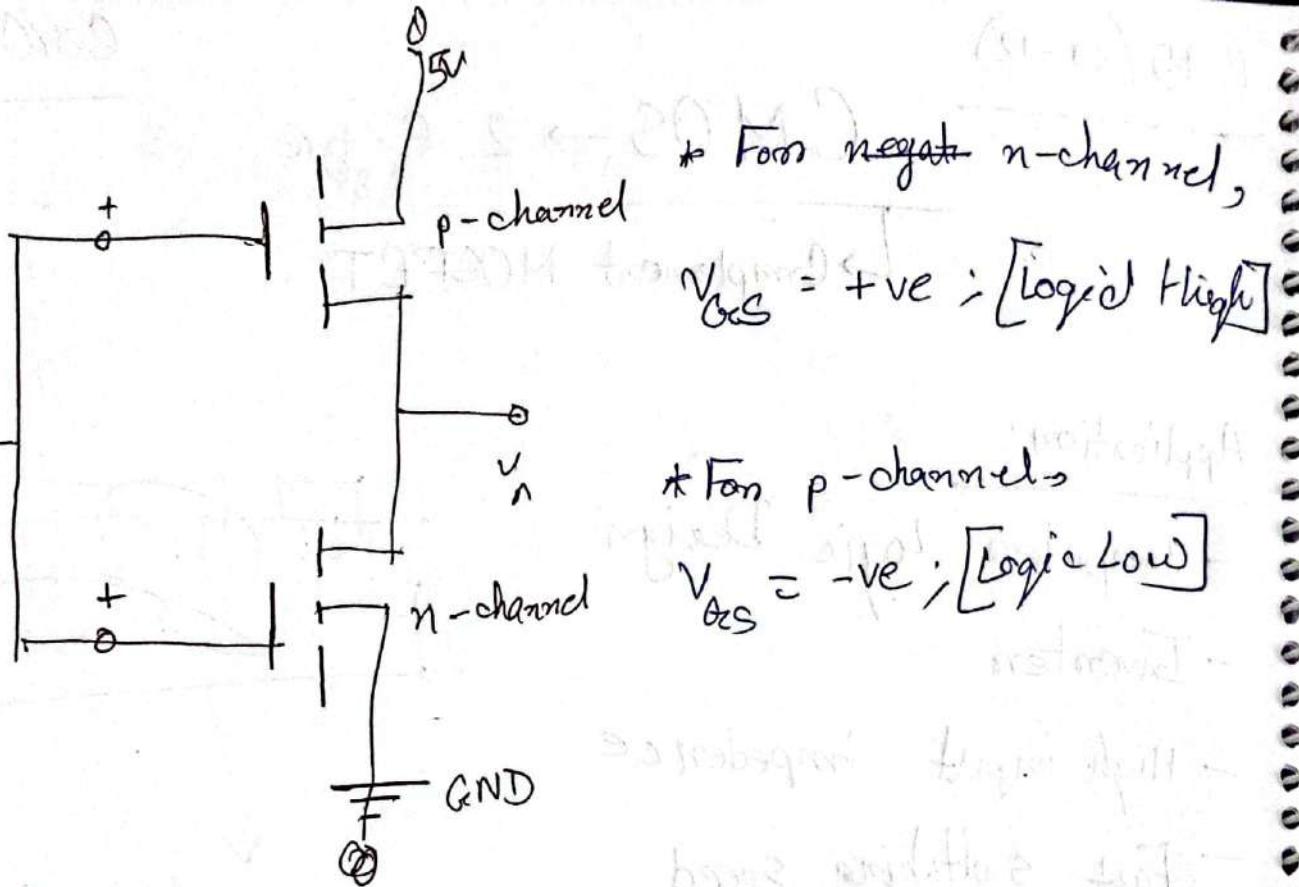
- Computer Logic Design
- Inverters
- High input impedance
- Fast switching speed
- Lower operating power level



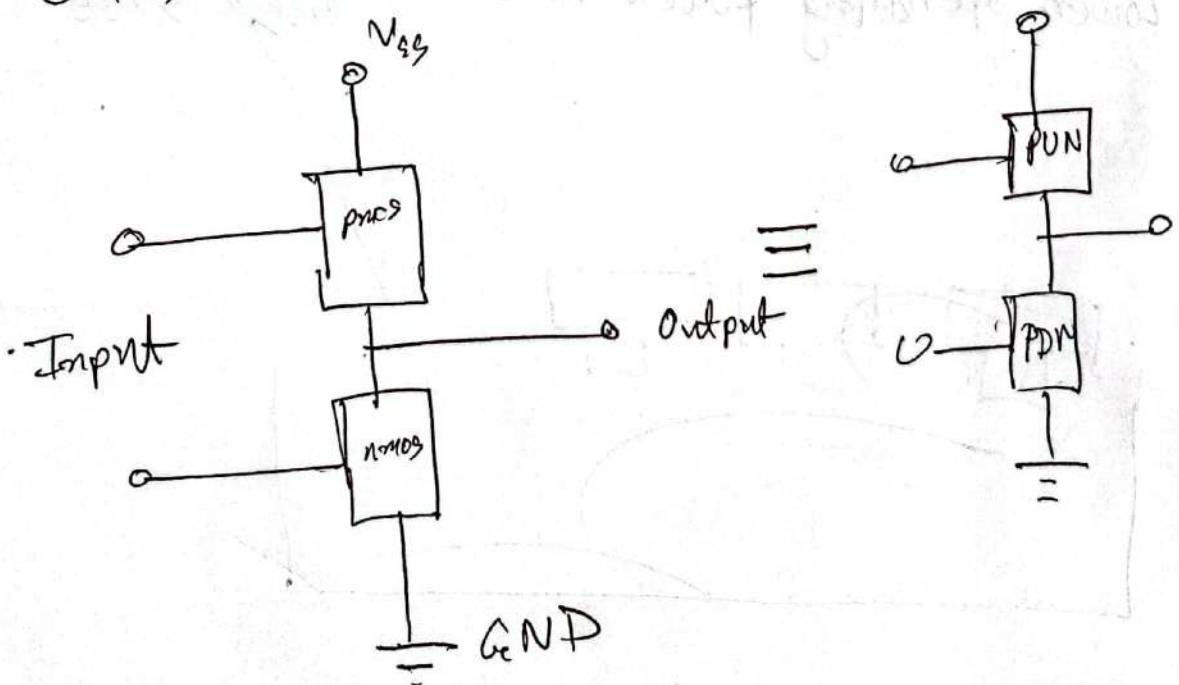
I can't draw this.
check slide



* 4 terminals.



CMOS



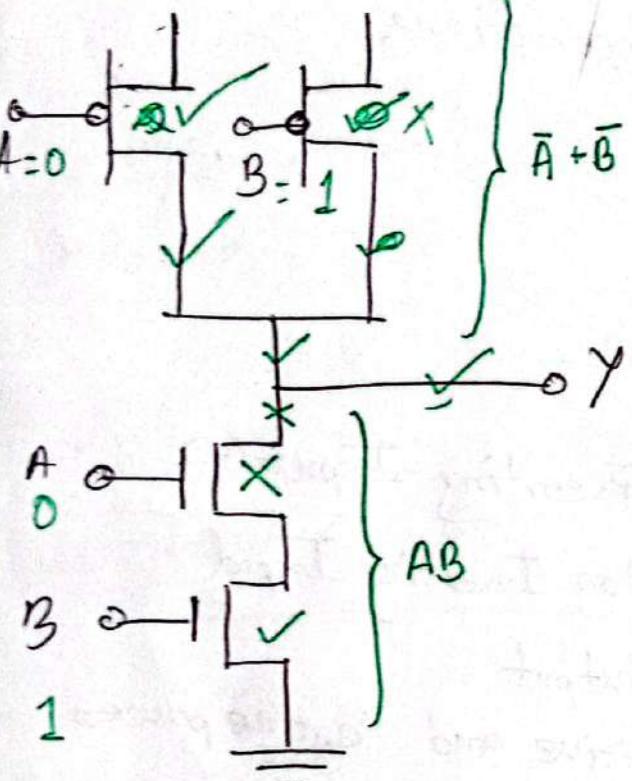
* PUN = Pull up network
 = Network of PMOS = (Expression)

* PDN = Pull down network
 = Network of NMOS = DeMoss (Expression)

* A · B = Series

* A + B = Parallel

NAND



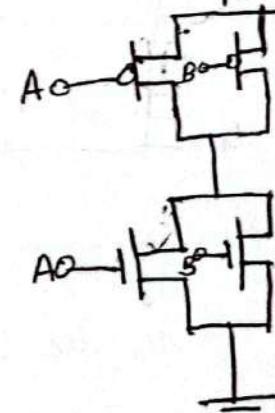
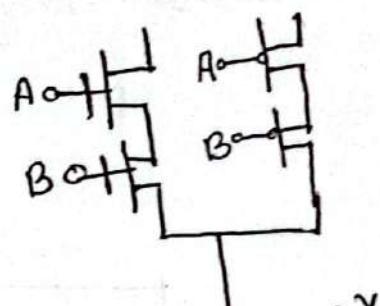
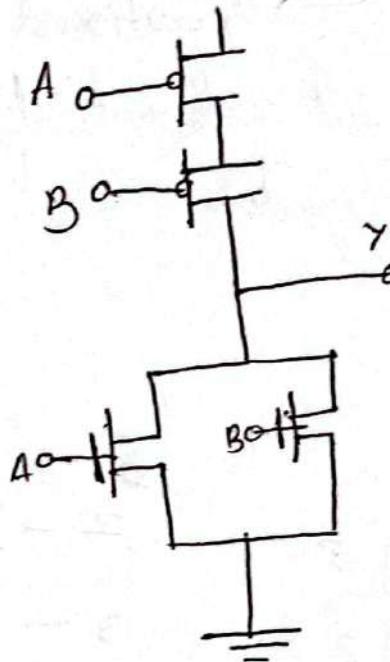
$$\begin{aligned} & \overline{A+B} \\ \therefore \text{PUN} &= \overline{A} \cdot \overline{B} \\ \therefore \text{PDN} &= \overline{A+B} \end{aligned}$$

Draw at home

$$\begin{aligned} X \text{NOR} &= A \circ B \\ &= (A+B)(\overline{A+B}) \end{aligned}$$

$$\therefore \text{PUN} = AB + \overline{AB}$$

$$\therefore \text{PDN} = \overline{(A+B)(A+B)}$$



$$Y = \overline{AB} \rightarrow \overline{A} + \overline{B}$$

$$\text{PDN} = \overline{(AB)} \rightarrow AB$$

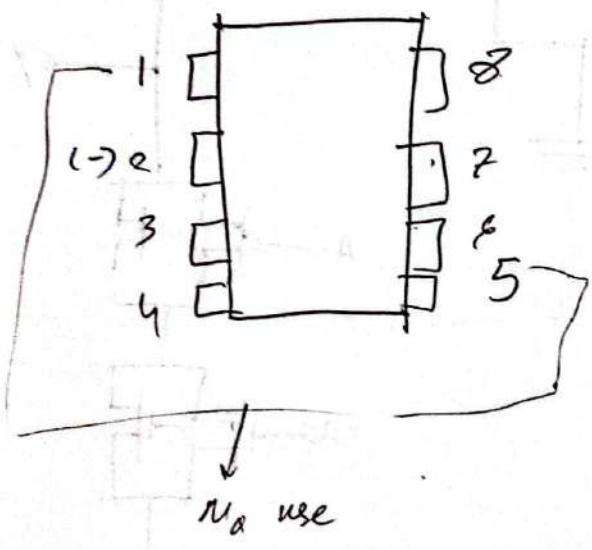
OP - AMP

↳ voltage controlled voltage source

↳ Operational Amplifiers

* can do almost all mathematical operations

↳ on analog signals



2 - Inverting Input (-)

3 - Non Inverting Input

6 - Output

7, 8 - Positive and Negative power supply

& Required: 2, 3, 4, 6, 7

→ High input impedance
Low output impedance

Output Voltage

$$V_o = A V_d = A(V_2 - V_1) \rightarrow \text{Ideal}$$

$A = \text{Open Loop Gain}$

$= \infty$ from an ideal op-amp

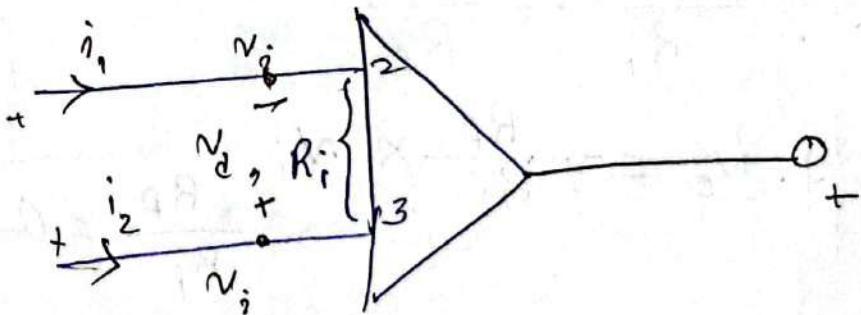
- * Higher $= +V_{sat}$
- * Lower $= -V_{sat}$

$$+ V_A \approx 1 \rightarrow +15V$$

$$- V_A \approx 1 \rightarrow -15V$$

Ideal Op-Amp

- i) $A = \infty$
- ii) $R_i = \infty$
- iii) $R_o = 0$



$$i_1 = 0$$

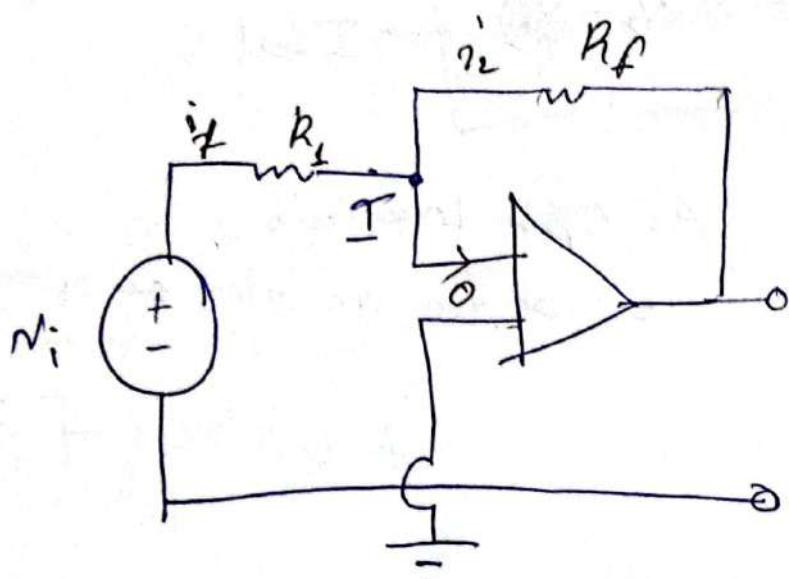
$$i_2 = 0$$

Inverting Amplifiers:

& If (feedback)

→ Closed loop

Configuration



$$i_1 = \frac{V_i - V_1}{R_i}$$

$$i_2 = \frac{V_1 - V_o}{R_f}$$

$$\therefore i_1 = i_2$$

$$\therefore \frac{V_i - V_1}{R_i} = \frac{V_1 - V_o}{R_f}$$

$$\therefore V_o = -\frac{R_f}{R_i} \times V_i \quad \rightarrow \frac{R_f}{R_i} = \text{Gain}$$

* Take graph
 * Make $\frac{R_f}{R_i}$ follow
 the graph

* Value comes from left/top/feedback connected end

* Best friend

* Inverts + Sets Ratio

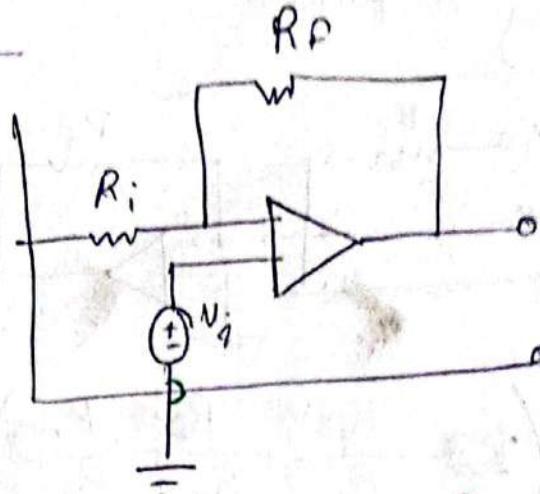
↳ feedback: R_f

\therefore For integers, $n_f > n_i$

* Use it for positive values at the end.

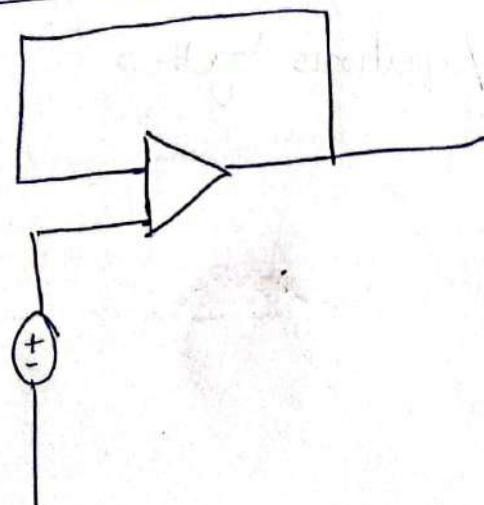
Non Inverting:

$$I_i = \frac{0 - V_i}{R_i}$$



- * Value comes from the non feedback bid
- * Third Best Friend (as less versatile)
- * Always $1 + \text{the ratio}$ and does not make it negative.
- ↳ use it for negative values at end

Buffer Op-Amp:

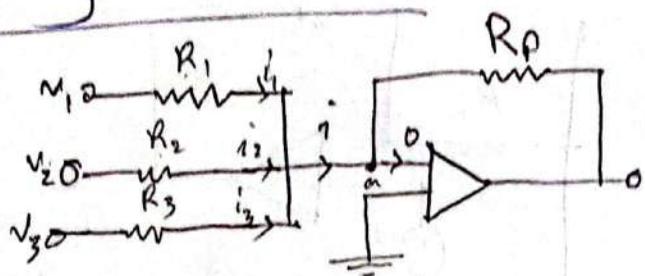


* Pointless for designing in exam
math incl

- * Keep an eye out just in case
- * No resistance

$$V_i = V_o$$

Summing Amplifiers:



$$v_0 = - \left(\frac{R_f \times v_1}{R_1} + \frac{R_f \times v_2}{R_2} + \frac{R_f \times v_3}{R_3} \right)$$

$$\begin{aligned} v_0 &= - \left(\frac{R_f}{R_1} \times v_1 + \frac{R_f}{R_2} \times v_2 + \frac{R_f}{R_3} \times v_3 \right) \\ &= -R_f \left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \dots + \frac{v_n}{R_n} \right) \end{aligned}$$

* Used for connecting multiple things/equations together

* Second best friend

* Can have multiple (n) connections

* Used for positive at the end

#slide

Gegeben steht,

$$\left. \begin{array}{l} V_1 = 1.5 \text{ V} \\ V_2 = 2 \text{ V} \\ V_3 = 1.2 \text{ V} \end{array} \right\} \begin{array}{l} R_1 = 20 \text{ k}\Omega \\ R_2 = 10 \text{ k}\Omega \\ R_3 = 6 \text{ k}\Omega \end{array}$$

B) $R_f = 8 \text{ k}\Omega$

$$R_o = 4 \text{ k}\Omega$$

$$\therefore V_o = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

$$\therefore V_o = -3.8 \text{ V}$$

$$I_o = \frac{V_o}{R_o} = \frac{-3.8}{4} = -0.95 \text{ A}$$

$$\therefore I_o = I_f - \frac{V_o}{4}$$

$$-1.425 = \frac{V_p}{R_p} - \frac{V_o}{4}$$

$$\text{on, } -1.425 = \frac{V_p}{8} - \frac{-3.8}{4}$$

$$\text{on, } -11.4 = V_f + 7.6$$

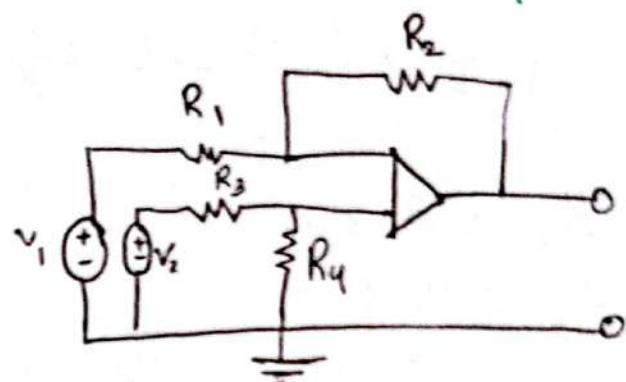
$$\therefore V_f = -19 \text{ V}$$

Difference Amplifiers:

$$V_o = \frac{R_2 \left(1 + \frac{R_1}{R_2}\right)}{R_1 \left(1 + \frac{R_3}{R_4}\right)} V_2 - \frac{R_2}{R_1} \times V_1 = \frac{R_2}{R_1} \left\{ \frac{\left(1 + \frac{R_1}{R_2}\right)}{\left(1 + \frac{R_3}{R_4}\right)} V_2 - V_1 \right\}$$

~~$\frac{R_2}{R_1}$~~

When $\frac{R_1}{R_2} = \frac{R_3}{R_4}$,



$$V_o = \frac{R_2}{R_1} (V_2 - V_1)$$

* Last Amp one will always be Inverting Amplifier

- * Used to make subtraction
- * $R_1 = R_i$, $R_2 = R_f$
- * $V_1 = V_{12}$, $V_2 = V_3 V_4$
- * One of the best friends
- * Two voltages

* Slide Math: $-5V_1 + 3V_2 = 3V_2 - 5V_1$

We know,

$$V_o = \frac{R_2 \left(1 + \frac{R_1}{R_2}\right)}{R_1 \left(1 + \frac{R_3}{R_4}\right)} V_2 - \frac{R_2}{R_1} V_1$$

$$\therefore \frac{R_2}{R_1} V_1 = -5$$

$$\therefore R_2 = 5R_1$$

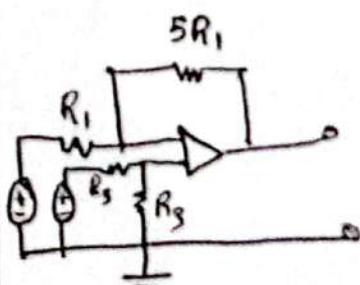
$$\therefore \frac{R_2}{R_1} \times \frac{\left(1 + \frac{R_1}{R_2}\right)}{\left(1 + \frac{R_3}{R_4}\right)} = 3$$

$$\text{or}, 5 \times \frac{1 + \frac{1}{5}}{1 + \frac{R_3}{R_4}} = 3$$

$$\text{or}, \frac{6}{3} = 1 + \frac{R_3}{R_4}$$

$$\text{or}, \frac{R_3}{R_4} = 1$$

$$\therefore R_3 = R_4$$



Frequency Response of a CE Amplifier Circuit, and Measurement of Input and Output Impedance

$$\left| I_C - \beta I_B \right|$$

→ Put small AC on base

→ ^{measure}
Collectors Volt

For (i)

input B

output C → beside capacitor

Find input impedance

Find d output "

V_{in} = until wave shape becomes just perfect (peak value)

Use multimeter to measure V across R_s

Calculate I_{in}

Use Thvenin to find R_o

- Calculate V_o
- Use Pot to get V_o/e
- Calculate R of Pot

100 N₂

$V_s = 1 \cdot V$

O — 100 k

O — 560

O — 1 k

+ O — 10 k

O — 33 k

O — 100

G-17(W-13)

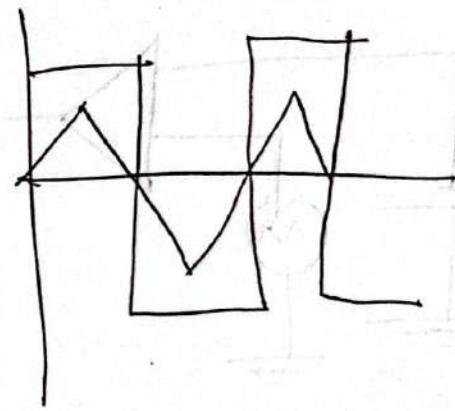
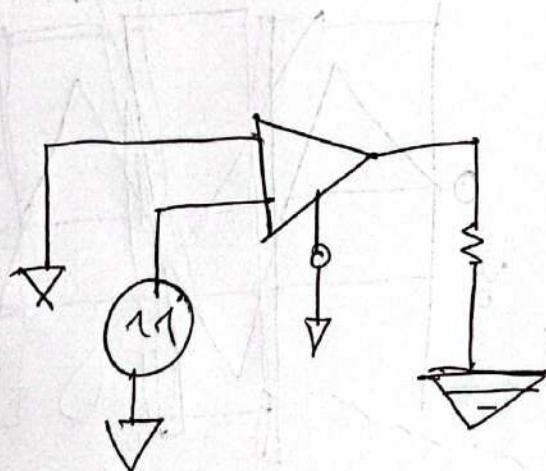
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Op - Amp as Comparator

Check slide

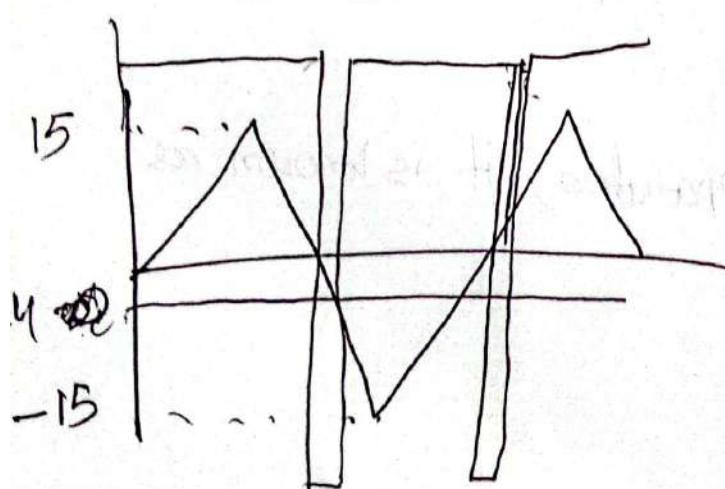
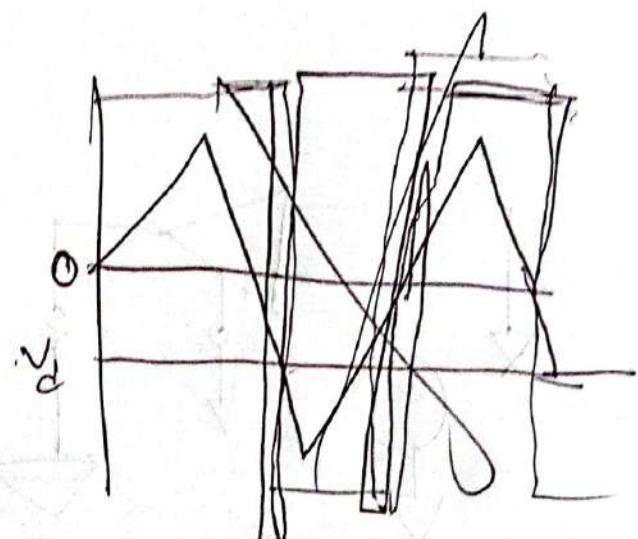
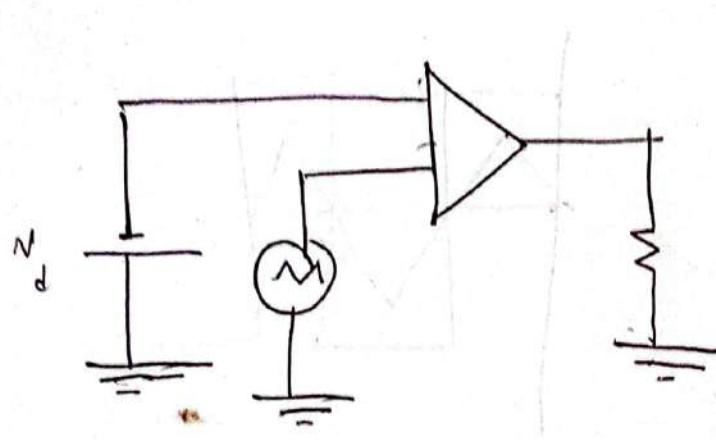
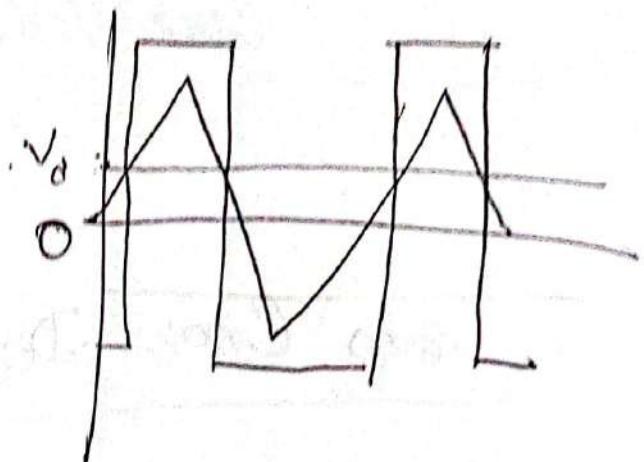
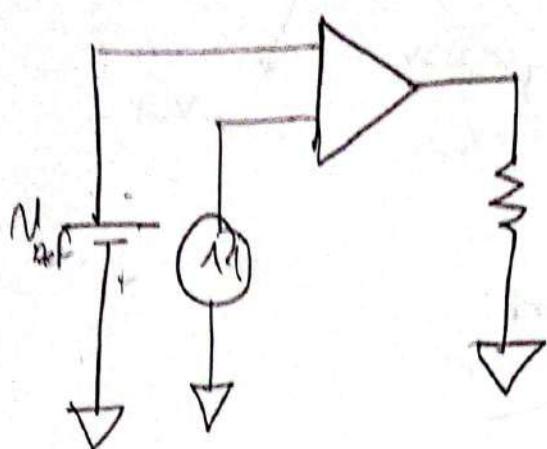
$$V_o = A V_d = A(V_2 - V_1)$$
$$V_2 > V_1 \quad V_o = +V_{sat}$$
$$V_2 < V_1 \quad V_o = -V_{sat}$$

Zero Cross Detector

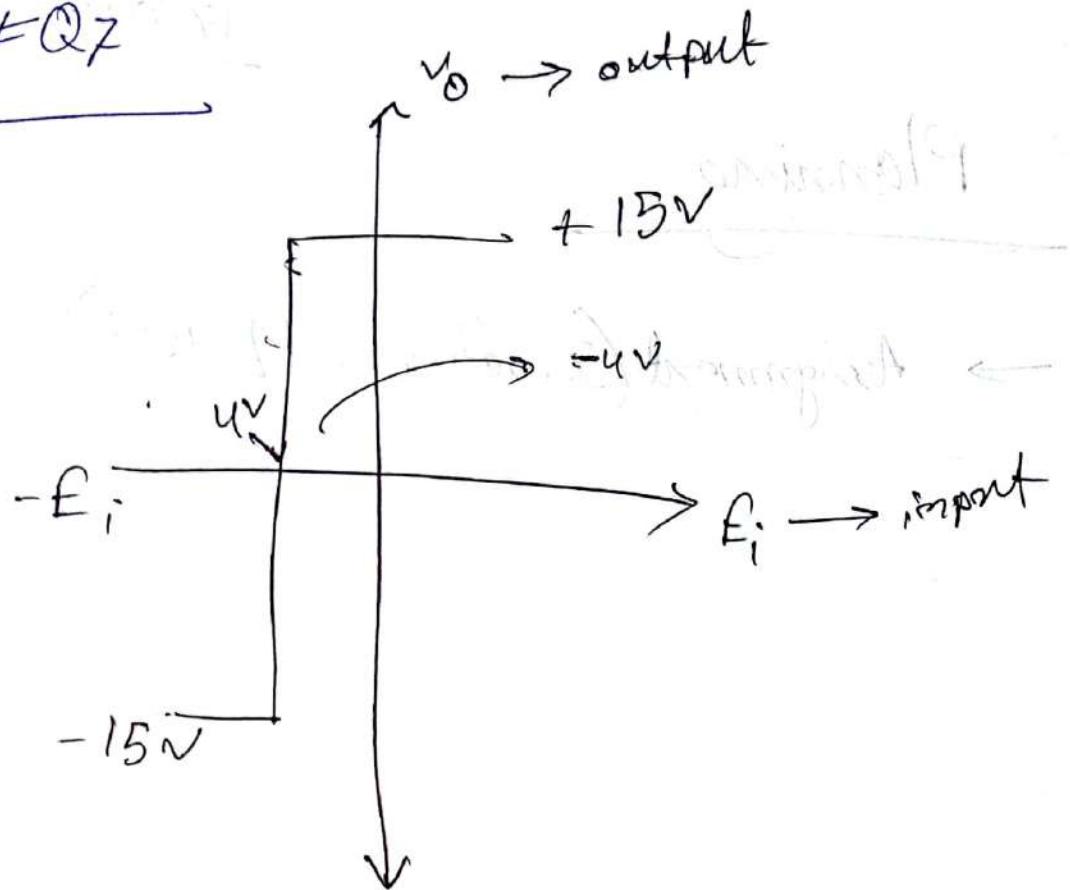


* When op-amp acts as a comparator, it is known as square wave generator.

Voltage Level Detection



#Q7



to Use voltage divider circuits to find the reactance
2 means graph line $-ve$

