(CS2.201a) Computer Systems Organization (Spring 2023) 01.04.2023

End-Semester Examination

Alloted time: 60 minutes Marks: 32

Instructions:

- There are four questions with sub-parts, printed over two sides of a sheet. Please check if your sheet has all the questions. Marks will be normalized by a factor of 10/32.
- Discussions amongst the students are not allowed. Any dishonesty shall be penalized heavily.
- Be clear in your arguments. Vague arguments shall not be given full credit.
- Please note that in class we discussed NASM x86 assembly and in assignments we discussed GNU x86 assembly. The main difference is in the order of operands. NASM uses destination first but GNU Assembly does not use destination as a first operand.

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1. Consider a 5-bit floating-point representation based on the IEEE floating-point format, with one sign bit, two exponent bits ($k = 2$), and two fraction bits ($n = 2$).

   (a) Compute the bias.

   (b) What is the binary representation of $-\frac{31}{8}$ and 56 in the above floating point representation.

   [2+3+3 marks]

2. Explain the given GNU x86 assembly snippet.

```
push   %ebp
mov    %esp,%ebp
mov    0x8(%ebp),%eax
# lea (%esi,%ebx,4), %edx corresponds to setting %edx to the address %esi+%ebx*4
lea    (%eax,%eax,4),%eax
lea    0xfffffff6(,%eax,4),%eax
mov    %ebp,%esp
pop    %ebp
ret
```

[8 marks]

3. The 5 stages of the processor have the following latencies:

	Fetch	Decode	Execute	Memory	Writeback
a.	300ps	400ps	350ps	550ps	100ps
b.	200ps	150ps	100ps	190ps	140ps

Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages.

(a) Non-pipelined processor: what is the cycle time? What is the latency of an instruction? What is the throughput?

(b) Fully Pipelined processor: What is the cycle time? What is the latency of an instruction? What is the throughput?

(c) If you could split one of the pipeline stages into 2 equal halves, which one would you choose? What is the new cycle time? What is the new latency? What is the new throughput?

[2+3+3 marks]

4. (a) For a direct-mapped cache design with a 32-bit address and byte-addressable memory, the following bits of the address are used to access the cache:

	Tag	Index	Offset
a.	31-10	9-5	4-0
b.	31-12	11-6	5-0

For each configuration (a and b):

i. What is the cache block size (in words)?

ii. How many entries (blocks) does the cache have?

[1.5+1.5 marks]

(b) You have a 2-way set associative L1 cache that is 8KB, with 4-word cache lines. Writing and reading data to L2 takes 10 cycles. You get the following sequence of writes to the cache – each is a 32-bit address in hexadecimal:

0x1000
0x1004
0x1010
0x11c0
0x2000
0x21c0
0x3400
0x3404
0x3f00
0x2004
0x1004

i. How many cache misses occur with an LRU policy?

ii. How many cache misses occur with a FIFO policy?

iii. Would the miss-rate increase or decrease if the cache was the same size, but direct-mapped (in above case)? Explain.

[2+1+2 marks]