



```
// File: 4bit_adder.v
// John Hubbard, 23 Jan 2015
// hw1 assignment for UCSC 30207: Digital Design with FPGA
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```
module add4(a, b, sum);
    input a, b;
    output sum;

    wire [3:0]a;
    wire [3:0]b;
    wire [4:0]sum;

    assign sum = a + b;
endmodule

module add4_struct(a, b, sum);
    input a, b;
    output sum;

    wire [3:0]a;
    wire [3:0]b;
    wire [4:0]sum;

    assign sum[0] = (!a[3]&!a[2]&!a[1]&!a[0]) & (!b[3]&!b[2]&!b[1]&b[0]) + (!a[3]&!a[2]&!a
[1]&!a[0]) & (!b[3]&!b[2]&b[1]&b[0]) + (!a[3]&!a[2]&!a[1]&!a[0]) & (!b[3]&b[2]&!b[1]&b[0])
+ (!a[3]&!a[2]&!a[1]&!a[0]) & (!b[3]&b[2]&b[1]&b[0]) + (!a[3]&!a[2]&!a[1]&!a[0]) & (b[3]&!
b[2]&!b[1]&b[0]) + (!a[3]&!a[2]&!a[1]&!a[0]) & (b[3]&!b[2]&b[1]&b[0]) + (!a[3]&!a[2]&!a[1]
&!a[0]) & (b[3]&b[2]&!b[1]&b[0]) + (!a[3]&!a[2]&!a[1]&!a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&!a[2]&!a[1]&a[0]) & (!b[3]&!b[2]&!b[1]&!b[0]) + (!a[3]&!a[2]&!a[1]&a[0]) & (!b[
3]&!b[2]&b[1]&!b[0]) + (!a[3]&!a[2]&!a[1]&a[0]) & (!b[3]&b[2]&!b[1]&!b[0]) + (!a[3]&!a[2]&
!a[1]&a[0]) & (!b[3]&b[2]&b[1]&!b[0]) + (!a[3]&!a[2]&!a[1]&a[0]) & (b[3]&!b[2]&!b[1]&!b[0]
) + (!a[3]&!a[2]&!a[1]&a[0]) & (b[3]&!b[2]&b[1]&!b[0]) + (!a[3]&!a[2]&!a[1]&a[0]) & (b[3]&
b[2]&!b[1]&!b[0]) + (!a[3]&!a[2]&!a[1]&a[0]) & (b[3]&b[2]&b[1]&!b[0]) +
    (!a[3]&!a[2]&a[1]&!a[0]) & (!b[3]&!b[2]&!b[1]&b[0]) + (!a[3]&!a[2]&a[1]&!a[0]) & (!b[3]
&!b[2]&b[1]&b[0]) + (!a[3]&!a[2]&a[1]&!a[0]) & (!b[3]&b[2]&!b[1]&b[0]) + (!a[3]&!a[2]&a[1]
&!a[0]) & (!b[3]&b[2]&b[1]&b[0]) + (!a[3]&!a[2]&a[1]&!a[0]) & (b[3]&!b[2]&!b[1]&b[0]) + (
!a[3]&!a[2]&a[1]&!a[0]) & (b[3]&!b[2]&b[1]&b[0]) + (!a[3]&!a[2]&a[1]&!a[0]) & (b[3]&b[2]&!
b[1]&b[0]) + (!a[3]&!a[2]&a[1]&!a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&!a[2]&a[1]&a[0]) & (!b[3]&!b[2]&!b[1]&!b[0]) + (!a[3]&!a[2]&a[1]&a[0]) & (!b[3]
&!b[2]&b[1]&!b[0]) + (!a[3]&!a[2]&a[1]&a[0]) & (!b[3]&b[2]&!b[1]&!b[0]) + (!a[3]&!a[2]&a[1]
&a[0]) & (!b[3]&b[2]&b[1]&!b[0]) + (!a[3]&!a[2]&a[1]&a[0]) & (b[3]&!b[2]&!b[1]&!b[0]) + (
!a[3]&!a[2]&a[1]&a[0]) & (b[3]&!b[2]&b[1]&!b[0]) + (!a[3]&!a[2]&a[1]&a[0]) & (b[3]&b[2]&!b
[1]&b[0]) + (!a[3]&!a[2]&a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&a[2]&!a[1]&!a[0]) & (!b[3]&!b[2]&!b[1]&b[0]) + (!a[3]&a[2]&!a[1]&!a[0]) & (!b[3]
&!b[2]&b[1]&b[0]) + (!a[3]&a[2]&!a[1]&!a[0]) & (!b[3]&b[2]&!b[1]&b[0]) + (!a[3]&a[2]&!a[1]
&!a[0]) & (!b[3]&b[2]&b[1]&b[0]) + (!a[3]&a[2]&!a[1]&!a[0]) & (b[3]&!b[2]&!b[1]&b[0]) + (
!a[3]&a[2]&!a[1]&!a[0]) & (b[3]&!b[2]&b[1]&b[0]) + (!a[3]&a[2]&!a[1]&!a[0]) & (b[3]&b[2]&!
b[1]&b[0]) + (!a[3]&a[2]&!a[1]&!a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&a[2]&a[1]&!a[0]) & (!b[3]&!b[2]&!b[1]&b[0]) + (!a[3]&a[2]&a[1]&!a[0]) & (!b[3]
&!b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&!a[0]) & (!b[3]&b[2]&!b[1]&b[0]) + (!a[3]&a[2]&a[1]
&a[0]) & (!b[3]&b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&!b[2]&!b[1]&b[0]) + (
!a[3]&a[2]&a[1]&a[0]) & (b[3]&!b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&!b
[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&a[2]&a[1]&a[0]) & (!b[3]&!b[2]&!b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (!b[3]&
&!b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (!b[3]&b[2]&!b[1]&b[0]) + (!a[3]&a[2]&a[1]
&a[0]) & (!b[3]&b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&!b[2]&!b[1]&b[0]) + (
!a[3]&a[2]&a[1]&a[0]) & (b[3]&!b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&!b
[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) +
```

[illegible]

```
assign sum[1] = (!a[3]&!a[2]&!a[1]&!a[0]) & (!b[3]&!b[2]&b[1]&!b[0]) + (!a[3]&!a[2]&!a[1]&a[0]) & (!b[3]&!b[2]&b[1]&b[0]) + (!a[3]&a[2]&!a[1]&!a[0]) & (!b[3]&b[2]&b[1]&!b[0]) + (!a[3]&a[2]&a[1]&!a[0]) & (!b[3]&b[2]&b[1]&b[0]) + (!a[3]&!a[2]&a[1]&a[0]) & (b[3]&!b[2]&b[1]&b[0]) + (!a[3]&!a[2]&!a[1]&a[0]) & (b[3]&!b[2]&!b[1]&b[0]) + (!a[3]&a[2]&!a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&!b[1]&b[0])
```

[illegible]

[illegible][illegible]

[illegible]

```
assign sum[3] = (!a[3]&!a[2]&!a[1]&!a[0]) & (b[3]&!b[2]&!b[1]&!b[0]) + (!a[3]&!a[2]&!a
```

[illegible]

[illegible]

```

assign sum[4] =
    (!a[3]&!a[2]&!a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&!a[2]&a[1]&!a[0]) & (b[3]&b[2]&b[1]&!b[0]) + (!a[3]&!a[2]&a[1]&!a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&!a[2]&a[1]&a[0]) & (b[3]&b[2]&!b[1]&b[0]) + (!a[3]&!a[2]&a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&a[2]&!a[1]&!a[0]) & (b[3]&b[2]&!b[1]&!b[0]) + (!a[3]&a[2]&!a[1]&!a[0]) & (b[3]&b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&!a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&a[2]&a[1]&a[0]) & (b[3]&!b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&!b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&a[2]&a[1]&!a[0]) & (b[3]&!b[2]&b[1]&!b[0]) + (!a[3]&a[2]&a[1]&!a[0]) & (b[3]&b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&!b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (!a[3]&a[2]&a[1]&a[0]) & (b[3]&!b[2]&!b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&!b[2]&b[1]&b[0]) + (!a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (a[3]&!a[2]&!a[1]&!a[0]) & (b[3]&!b[2]&!b[1]&!b[0]) + (a[3]&!a[2]&!a[1]&!a[0]) & (b[3]&!b[2]&!b[1]&b[0]) + (a[3]&!a[2]&!a[1]&!a[0]) & (b[3]&!b[2]&b[1]&b[0]) +
    (a[3]&!a[2]&!a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) + (a[3]&!a[2]&!a[1]&a[0]) & (b[3]&b[2]&!b[1]&b[0]) + (a[3]&!a[2]&!a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) +
    (a[3]&a[2]&a[1]&a[0]) & (!b[3]&b[2]&b[1]&b[0]) + (a[3]&a[2]&a[1]&a[0]) & (b[3]&!b[2]&!b[1]&b[0]) + (a[3]&a[2]&a[1]&a[0]) & (b[3]&!b[2]&b[1]&b[0]) +
    (a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&!b[1]&b[0]) + (a[3]&a[2]&a[1]&a[0]) & (b[3]&b[2]&b[1]&b[0]) +

```



```

// File: 4bit_adder_tb.v
// John Hubbard, 23 Jan 2015
// hw1 assignment for UCSC 30207: Digital Design with FPGA

// Steps to run in ModelSim:
//
// cd D:/git_wa/classes/ucsc/fpga_30207/hw1
// vlib work
// vlog -sv 4bit*.v
// vsim work.add4_tb.v
// add wave *
// run 10 ns
//

`timescale 1ns/1ns

module add4_tb();
    reg [3:0]a;
    reg [3:0]b;
    wire [4:0]sum;

    reg [3:0]a2;
    reg [3:0]b2;
    wire [4:0]sum2;

    reg [4:0]testSum;

    add4      X(a,  b,  sum);
    add4_struct Y(a2, b2, sum2);

    initial
    begin
        testSum = 0;
        a = 0;
        b = 0;

        for (a = 0; a < 16; a = a + 1)
            for (b = 0; b < 16; b = b + 1)
                begin
                    #1 testSum = a + b;

                    if (sum != testSum)
                        $display("ERROR: sum: %d != testSum: %d",
                                sum, testSum);
                    if (sum2 != testSum)
                        $display("ERROR: sum2: %d != testSum: %d",
                                sum2, testSum);
                end
            end
        end
    endmodule

```

```

// 4 bit adder program generator
// For UCSC Class 30207: Digital Design with FPGA
// John F. Hubbard, 18 Jan 2015
//

#define BIT_LENGTH_A      4
#define BIT_LENGTH_B      4
#define BIT_LENGTH_SUM    5

#include <stdio.h>

void print_binary(int x, int bitLength)
{
    int index;

    for (index = bitLength - 1; index >=0; index--)
    {
        if (x & (1 << index))
            printf("1");
        else
            printf("0");
    }
}

void print_algebraic(const char * digitName, int x, int bitLength, int bit)
{
    int index;

    for (index = bitLength - 1; index >=0; index--)
    {
        if (index == bitLength - 1)
            printf("(");

        if (x & (1 << index))
            printf("%s[%d]", digitName, index);
        else
            printf("!"%s[%d]", digitName, index);

        if (index == 0)
            printf(")");
        else
            printf("&");
    }
}

print_term(int a, int b, int sum, int bit)
{
    // if bit[n] of sum is set, print
    if (sum & (1 << bit))
    {
        print_algebraic("a", a, BIT_LENGTH_A, bit);
        printf(" & ");
        print_algebraic("b", b, BIT_LENGTH_B, bit);
        printf(" + ");
    }
}

```

```

    }
}

int main(int argc, char * argv[])
{
    int a;
    int b;
    int sum;
    int bit;

    printf("// 4-bit counter truth table: structural verilog");
    printf("\n\n");

    for (bit = 0; bit <= 5; bit++)
    {
        printf("assign sum[%d] = ", bit);

        for (a = 0; a < 16; a++)
        {
            for (b = 0; b < 16; b++)
            {
                sum = a + b;
                print_term(a, b, sum, bit);
            }
            printf("\n");
        }

        printf("0;\n\n");
    }
    return 0;
}

```