- 1) This is called a privilty circuit.
- 3) Using behavioral Verilog, 8 LUTS are required. However, it uses LUTS and LUT6, so it has an advantage, due to not being constrained to LUT4.
  - 4) Using structural Ver, Tog, 9 LUT4's arel required. It's hard to compare directly, but this is at least as good as the behavioral yer, Tag result and the tool-generated ctrcuit.