Hw # 4

Problem 3.9.4 – Testing switches & LEDs

1) This is called a priority circuit.

3) Using behavioral Verilog, 8 LUT's are required. But two of these

4) Using structural verilog, 9 LUT's ar required, if I am restricted to LUT4's.

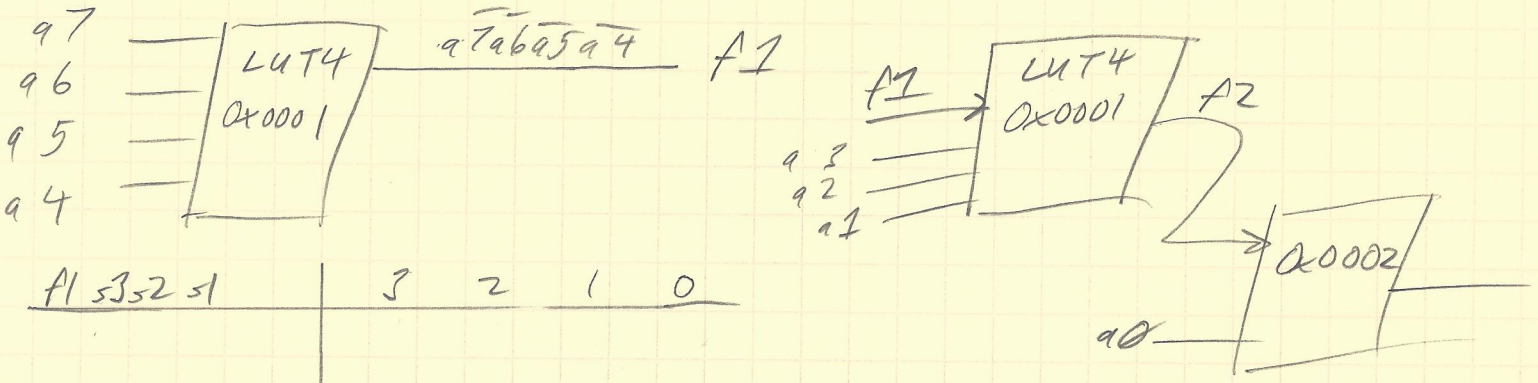
Led 7 = sw 7
Led 6 = sw 6 $\overline{\text{sw 7}}$
Led 5 = sw 5 $\overline{\text{sw 6}}$ $\overline{\text{sw 7}}$

sw 7	sw 6	sw 5	sw 4	led 7	led 6	led 5	led 4	led 3	led 2	led 1	led 0
0	0	0	0	0	0	0	0				
0	0	0	1	0	0	0	1				
0	0	1	0	0	0	1	0				
0	0	1	1	0	0	1	0				
0	1	0	0	0	1	0	0				
0	1	0	1	0	1	0	0				
0	1	1	0	0	1	0	0				
0	1	1	1	0	1	0	0				
1	0	0	0	1	0	0	0				
1	0	0	1	1	0	0	0				
1	0	1	0	1	0	0	0				
1	0	1	1	1	0	0	0				
1	1	0	0	1	0	0	0				
1	1	0	1	1	0	0	0				
1	1	1	0	1	0	0	0				
1	1	1	1	1	0	0	0				

LUT Mask: 16'hFF00 → 0x00F0 → 0x000C

Led 4: 0x0002

not required:
assign Led7 = sw7.



A1	s3	s2	s1	3	2	1	0
1	0	0	0			0	0
1	0	0	1			0	1
1	0	1	0			1	0
1	0	1	1			1	0
1	1	0	0	1			
1	1	0	1	1			
1	1	1	0	1			
1	1	1	1	1			

0200

0xF000

0C00