**TestPlan for 10 Gb/s Ethernet MAC block**

**Final Class Project for USCS 18966: SystemVerilog OOP Testbench (Instructor: Benjamin Ting)**

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# Description of Test Plan

This test plan exercises the 10 Gb/s Ethernet MAC block. That project may be found at <http://opencores.org/project,ethmac10g> . Throughout this document, the block will be referred to as either the “DUT” (Device Under Test), or the “Ethernet MAC block”.

At a high level, the Ethernet MAC block simply translates 64-bit packet data (plus control lines) to and from a serial bit stream, as shown in Figure 1 (which is lifted pretty much entirely from the Instructor’s lab workbook for this course):

**Fig. 1: Block Diagram of the verification environment**

And so, in order to test such a device, one of the first things to do it to put it into “loopback” mode, by cross-connecting the serial transmit and receive lines. Then the DUT will appear to send packets to itself, and we can verify that the parallel (non-serial) side works properly.

It is also important to verify that the serial bitstream is in accordance with specifications. However, doing so that is beyond the scope of this document, as our purpose in this course is primarily to build and use an OOP (Object Oriented Programming) test bench in SystemVerilog.

# Description of Test Cases

# Description of Driver, Monitor, Scoreboard (with block diagrams)

# Coverage: Code Coverage, Functional Coverage, Assertions