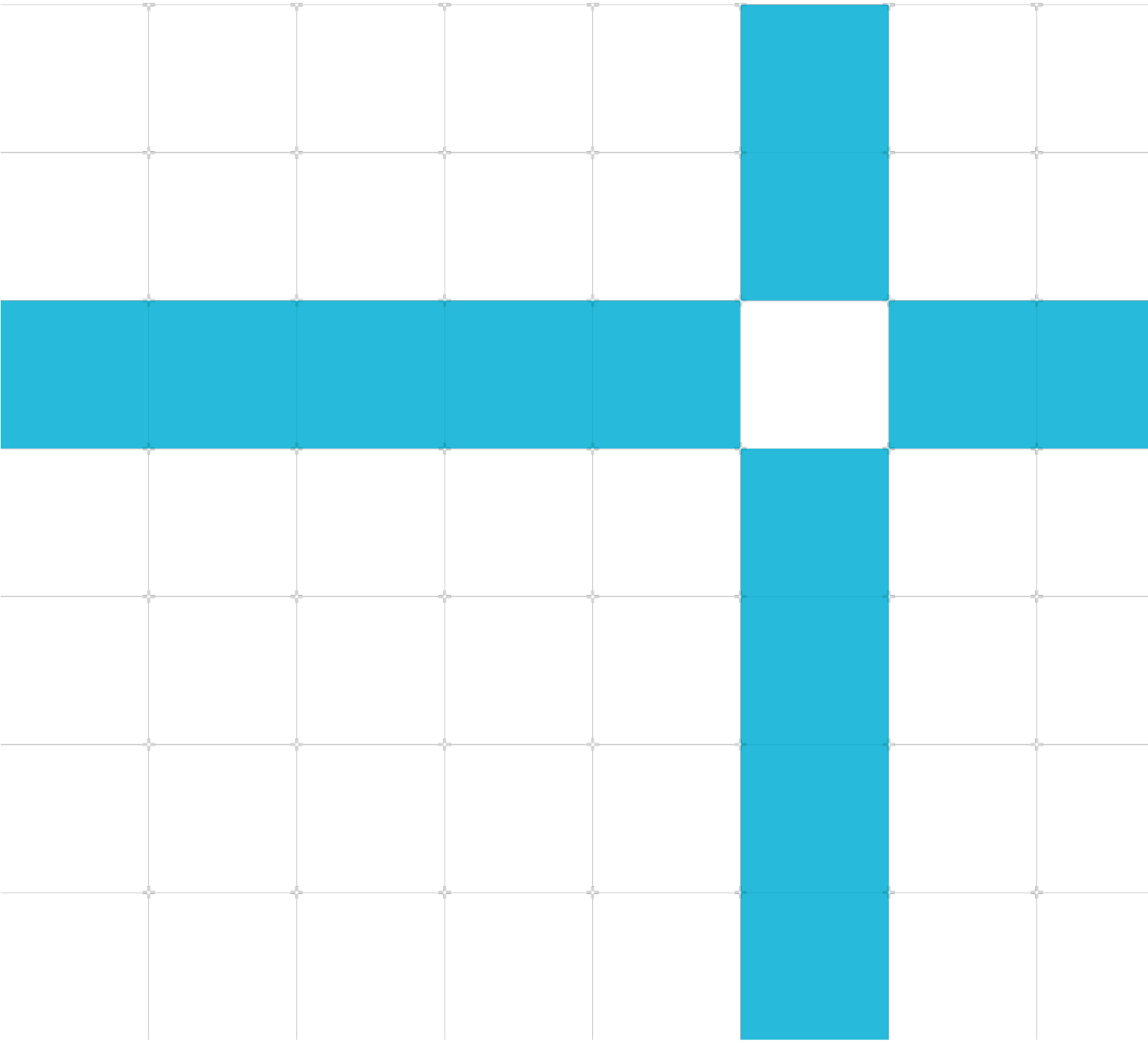
Arm® PC BSA Architecture Compliance

Revision: r0p5

Test Scenario

Non-Confidential

Issue 01
ARM040-1254092399-18632



Arm PC BSA Test Scenario Document

Release information

Document history

Issue	Date	Confidentiality	Change
01	11 December 2024	Non-Confidential	Alpha release 0.5.0

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Inclusive language commitment

Arm values inclusive communities. Arm recognizes that we and our industry have used terms that can be offensive. Arm strives to lead the industry and create change.

This document includes terms that can be offensive. We will replace these terms in a future issue of this document. If you find offensive terms in this document, please email **terms@arm.com**.

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Contents

1 Introduction

1.1 Product revision status

The *rmpn* identifier indicates the revision status of the product described in this book, for example, r*1*p*2*, where:

rm Identifies the major revision of the product, for example, r*1*.

pn Identifies the minor revision or modification status of the product, for example, p*2*.

1.2 Intended audience

This document is for engineers who are verifying an implementation of Arm® PC Base System Architecture 1.0.

1.3 Conventions

The following subsections describe conventions used in Arm documents.

1.3.1 Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: **https://developer.arm.com/glossary**.

1.3.2 Typographical Conventions

Convention	Use
italic	Introduces citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`monospace` **`bold`**	Denotes language keywords when used outside example code.
`monospace underline`	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the Arm® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

1.4 Useful resources

This document contains information that is specific to this product. See the following resources for other relevant information.

- Arm Non-Confidential documents are available on **developer.arm.com/documentation**. Each document link in the tables below provides direct access to the online version of the document.
- Arm Confidential documents are available to licensees only through the product package.

Arm products	Document ID	Confidentiality
Arm® PC Base System Architecture 1.0	DEN0151	Non-Confidential

Arm architecture and specifications	Document ID	Confidentiality
Arm® Architecture Reference Manual for A-profile architecture	DDI0487F	Non-Confidential

Non-Arm resources	Document ID	Organization
PCI Express Base Specification Revision 5.0, Version 1.0	NA	PCI-SIG
PCI-To-PCI Bridge Architecture Specification 1.2	NA	PCI-SIG

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1.5 Feedback

Arm welcomes feedback on this product and its documentation.

1.5.1 Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

1.5.2 Feedback on content

If you have comments on content, send an email to **support-systemready-acs@arm.com** and give:

- The title Arm Personal Computing Base System Architecture Scenario.
- The number ARM040-1254092399-18632.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.
- Arm also welcomes general suggestions for additions and improvements.

2 Personal Computing Base System Architecture

The PC Base System Architecture (PC-BSA) specifies a standard hardware system architecture for Personal Computers (PCs) that are based on the Arm 64-bit Architecture. PC system software, for example operating systems, hypervisors, and firmware can rely on this standard system architecture. PC-BSA extends the requirements specified in the Arm BSA.

Personal Computing Base System Architecture (PC BSA) specifies a hardware system architecture based on Arm 64-bit architecture, that system software such as operating systems, hypervisors, and firmware can rely on. The document addresses PE features and key aspects of system architecture. The primary goal of the document is to ensure sufficient standard system architecture to enable a suitably built single OS image to run on all the hardware compliant with the specifications.

Arm does not mandate compliance with this specification. However, Arm anticipates that OEMs, ODMs, cloud service providers, and software providers will require compliance to maximize Out-of-Box software compatibility and reliability.

2.1 PC-BSA ACS

The tests are divided into a hierarchy of subcategories depending on the runtime environment and the component submodules that are required for achieving the verification. The top level of a hierarchy is consistent with the target hardware subsystem which is validated by a test. A test may check for different parameters of the hardware subsystem.

The tests are classified as:

- PE
- Memory Map
- GIC
- SMMU
- PCIe

2.2 PE

Test number	Rule ID	Scenario	Algorithm
1, 2	P_L1PE_01	PEs must support 4KB translation granules at stage 1 and stage 2.	ID_AA64MMFR0_EL1 must indicate support for 4KB granules for all cores.
3	P_L1PE_02	PEs must implement 16-bit ASID support.	CPU system register field ID_AA64MMFR0_EL. ASIDBits must read b0010.
4	P_L1PE_03	PEs must implement AArch64 at all implemented Exception levels.	CPU system register ID_AA64PFR0_EL1 fields EL0, EL1, EL2 and EL3 must read non-zero value.
5	P_L1PE_04	PEs must comply with FEAT_LSE requirements as specified by B_PE_25 from Arm BSA	CPU system register ID_AA64ISAR0_EL1.Atomic = 0b0010 or 0b0011
6	P_L1PE_05	Base PC systems that make use of FEAT_LPA must support a functional system memory map which is wholly contained within the address range from 0 to 2^48-1	Check for FEAT_LPA presence, CPU System register ID_AA64MMFR0_EL1 bits [3:0] must read b0110. If FEAT_LPA is implemented, then ID_AA64MMFR0_EL1.TGran16 [23:20] must read 0b0010 or ID_AA64MMFR0_EL1.TGran4 [31:28] must read 0b001. If FEAT_LPA2 is also implemented along with FEAT_LPA, then all peripheral addresses have no restriction else all peripheral addresses should be contained inside 2^48 memory map.
7	P_L1PE_06	If the system contains persistent memory that is exposed to the OS, all PEs must support the clean to point of persistence instruction (DC CVAP). The instruction must be able to perform a clean to the point of persistence for all memory that is exposed as persistent memory to the OS	Check whether persistent memory exists in the system from using UEFI GetMemoryMap() service. If present, CPU System register field ID_AA64ISAR1_EL1.DPB must read b0001 or b0010 indicating DC CVAP instruction support.
8	P_L1PE_07	All PEs must implement FEAT_VMID16	CPU system register field ID_ AA64MMFR1_EL1.VMIDBits must read b0010.
9	P_L1PE_08	All PEs must implement FEAT_VHE.	CPU system register field ID_ AA64MMFR1_EL1.VH must read b0001

2.3 Memory Map

Test number	Rule ID	Scenario	Algorithm
101	P_L1MM_01	If a base PC system supports 64KB translation granules at stage 2 then it must ensure that: 1. All memory and peripherals can be mapped using 64KB stage 2 pages and must not require the use of 4KB pages at stage 2. 2. All peripherals that can be assigned to different virtual machines will be situated within different 64KB regions of memory. This rule applies to types of peripherals such as PCIe devices. Here is an indicative list of the peripherals that are exempt from this rule: • On-chip peripherals whose resources are not managed by PE software, for example system controllers or power management controllers. • Secure-world peripherals.	ID_AA64MMFR0_EL1 must indicate support for 64KB granules for all cores. If yes, then check whether all peripheral base addresses are 64KB apart from each other.

2.4 GIC

Test number	Rule ID	Scenario	Algorithm
201	P_L1GI_01	A base PC system must implement at least one interrupt controller that is compliant with the GICv3 or higher architecture	Check GIC version is 3. or greater than 3
203	P_L1GI_03	A GIC that implements Locality-specific Peripheral Interrupts (LPIs) should support clearing GICR_CTLR.EnableLPIs	Get ITS Address for current ITS. Check GITS_CTLR.Enabled = 0 and GITS_CTLR. Quiescent = 1

Test number	Rule ID	Scenario	Algorithm
204	P_L1GI_04	A GIC implementation that does not support clearing GICR_CTLR.EnableLPIs after it is set must not permit modification of GICR_PENDBASER when GICR_CTLR.EnableLPIs == 1.	Get RDBase Address for current PE, Check GICR_CTLR.EnableLPIs = 0 and GICR_CTLR.RWP = 0
202	P_L1PP_01	The Interrupt IDs must be the same as the recommended values specified by B_PPI_01, B_PPI_02, and B_PPI_03 from Arm BSA	Check for the reserved interrupt as mentioned in the interrupt table

2.5 SMMU

Test number	Rule ID	Scenario	Algorithm
301	P_L1SM_02	base PC system must support Stage 1 System MMU functionality. This must be provided by a System MMU that is compliant with the Arm SMMUv3, or higher, architecture revision.	The SMMU memory mapped register field SMMU_AIDR.ArchMajorRev ≥ 3 indicating SMMU is compliant with SMMUv3 or higher. And memory mapped register field SMMU_IDR0.S1P must read b1 indicating Stage 1 support
301	P_L1SM_03	A base PC system must support Stage 2 System MMU functionality. This must be provided by a System MMU that is compliant with the Arm SMMUv3, or higher, architecture revision	The SMMU memory mapped register field SMMU_AIDR.ArchMajorRev ≥ 3 indicating SMMU is compliant with SMMUv3 or higher. And memory mapped register field SMMU_IDR0.S2P must read b1 indicating Stage 2 support.
302	P_L1SM_04	The integration of the System MMUs must be compliant with rules SMMU_01 and SMMU_02, as specified in “SMMUv3 integration” section from Arm BSA	The SMMU memory mapped register field SMMU_IDR0.COHACC must read b1.

2.6 PCIe

Test number	Rule ID	Scenario	Algorithm
601	P_L1PCI_2	There must be no OS observable use of PCIe Enhanced Allocation	Pass if No EA Capability is present or check if "Enable" bit in Entry Type register is 0

Appendix A Revisions

This appendix describes the technical changes between released issues of this book.

Table A-1 Issue 01

Change	Location
First release	-