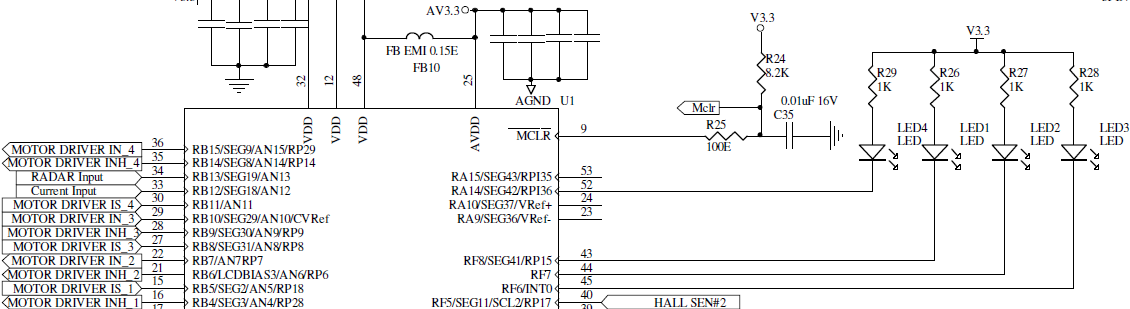
**Autonomous Tractor Safety System**

**Objective 3.0** To display the ADC value using four LEDs and a potentiometer(AN5) in ATSS PCB board

****

**TRISF** DATA DIRECTION REGISTER F: 0x0000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| TRISF15 | TRISF14 | TRISF13 | TRISF12 | TRISF11 | TRISF10 | TRISF9 | TRISF8 |
| I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
|  |  |  |  |  |  |  | 0 |
|  |  |  |  |  |  |  | Output |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| TRISF7 | TRISF6 | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 |
| I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
| 0 | 0 |  |  |  |  |  |  |
| Output | Output |  |  |  |  |  |  |

**TRISA** DATA DIRECTION REGISTER A: 0x0000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| TRISA15 | TRISA14 | TRISA13 | TRISA12 | TRISA11 | TRISA10 | TRISA9 | TRISA8 |
| I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
|  | 0 |  |  |  |  |  |  |
|  | Output |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 |
| I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

**LATF** OUTPUT LATCH REGISTER F: 0x01C0

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| LATF15 | LATF14 | LATF13 | LATF12 | LATF11 | LATF10 | LATF9 | LATF8 |
| I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
|  |  |  |  |  |  |  | 1 |
|  |  |  |  |  |  |  | LED1 off |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| LATF7 | LATF6 | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 |
| I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
| 1 | 1 |  |  |  |  |  |  |
| LED2 off | LED3 off |  |  |  |  |  |  |

**LATA** OUTPUT LATCH REGISTER A: 0x4000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| LATAF15 | LATA14 | LATA13 | LATA12 | LATA11 | LATA10 | LATA9 | LATA8 |
| I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
|  | 1 |  |  |  |  |  |  |
|  | LED4 off |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| LATA7 | LATA6 | LATA5 | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 |
| I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

**AD1CON1** ADC1 CONTROL REGISTER 1: 0x8474

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| ADON | - | ADSIDL | DMABM | DMAEN | MODE12 | FORM1 | FORM0 |
| ADC MODE |  | ADC STOP IN IDLE | DMA EXT BUFFER | DMA EXT BUFF EN | 10/12 BIT MODE | DATA O/P FORMAT | |
| 1 |  | 0 |  |  | 1 | 0 | 0 |
| OPERATING |  |  |  |  | 12 BIT | ABS DECIMAL,UNSIGNED, RIGHT JUSTIFIED | |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| SSRC3 | SSRC2 | SSRC1 | SSRC0 | - | ASAM | SAMP | DONE |
| SAMPLE CLK SOURCE SELECT | | | |  | ADC SAMPLE AUTO START | SAMPLING/ HOLDING | ADC STATUS |
| 0 | 1 | 1 | 1 |  | 0 | 1 | 0 |
| INT COUNTER ENDS SAMPLING & AUTO CONVERTS | | | |  | MANUAL | SAMPLING | IN PROGRESS |

**AD1CON2** ADC1 CONTROL REGISTER 2: 0x0078

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| PVCG1 | PVCG0 | NVCFG0 | OFFCAL | BUFREGEN | CSCNA | - | - |
| VREF+ |  | VREF- | OFFSET CALIBR MODE | BUFFER REG ENABLE | SCAN SAMPLEA FOR CH0+ |  |  |
| 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| AVDD |  | AVSS | NORMAL I/Ps FOR SAMPLE & HOLD | ADC RESULT BUFFER FIFO | NO SCAN |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| BUFS | SMPI4 | SMPI3 | SMPI2 | SMPI1 | SMPI0 | BUFM | ALTS |
| BUFFER FILL STATUS | NO. OF SAMPLES PER CONVERSION | | | | | BUFFER FILL MODE | ALT I/P SAMPLE MODE |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| USE DATA IN UPPER HALF | INTERRUPT AFTER END OF COVERTING EVERY 31st SAMPLE | | | | | SINGLE 26 WORD BUFFER FROM ADC1BUF0 | CH SELECTED ONLY FROM SAMPLE A |

**AD1CON3** ADC1 CONTROL REGISTER 3: 0x1E01

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| ADRC | EXTSAM | PUMPEN | SAMC4 | SAMC3 | SAMC2 | SAMC1 | SAMC0 |
| ADC CLK | EXT SAMPLING | CHARGE PUMP ENABLE | AUTO SAMPLE SELECT BITS | | | | |
| 0 | 0 |  | 1 | 1 | 1 | 1 | 0 |
| SYS CLK | NO SAMPLING AFTER SAMP=0 | DISABLED | 31 \* TAD | | | | |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| ADCS7 | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCS0 |
| ADC CLK CONVERSION SELECT BITS | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 \* TCY = TAD | | | | | | | |

**AD1CON4** ADC1 CONTROL REGISTER 4: 0x0000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| - | - | - | - | - | - | - | - |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| - | - | - | - | - | DMABL2 | DMABL1 | DMABL0 |
|  |  |  |  |  | DMA BUFFER SIZE SELECT | | |
|  |  |  |  |  | 0 | 0 | 0 |
|  |  |  |  |  | 1 WORD BUFFER FOR EACH ANALOG I/P | | |

**AD1CON5** ADC1 CONTROL REGISTER 5: 0x0006

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| ASEN | LPEN | CTMUREQ | BGREQ | - | - | ASINT1 | ASINT0 |
| AUTO SCAN ENABLE | LOW POWER ENABLE | CTMU REQUEST | BAND GAP REQUEST |  |  | AUTO SCAN THRESHOLD INTERRUPT | |
| 0 | 0 | 0 | 0 |  |  | 0 | 0 |
| DISABLED | DISABLED | DISABLED | DISABLED |  |  | NO INTERRUPT | |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| - | - | - | - | WM1 | WM0 | CM1 | CM0 |
|  |  |  |  | WRITE MODE | | COMPARE MODE | |
|  |  |  |  | 0 | 1 | 1 | 0 |
|  |  |  |  | CONVERT & SAVE | | MATCH OCCURS IF WITHIN BUFFER PAIR WINDOW | |

**AD1CHS** ADC1 CONTROL REGISTER: 0x0005

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CH0NB2 | CH0NB1 | CH0NB0 | CH0SB4 | CH0SB3 | CH0SB2 | CH0SB1 | CH0SB0 |
| SAMPLE B CH 0 –VE I/P SELECT | | | SAMPLE B CH 0 +VE I/P SELECT | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VREF-/AVSS | | | AN0 | | | | |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CH0NA2 | CH0NA1 | CH0NA0 | CH0SA4 | CH0SA3 | CH0SA2 | CH0SA1 | CH0SA0 |
| SAMPLE A CH 0 –VE I/P SELECT | | | SAMPLE A CH 0 +VE I/P SELECT | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| VREF-/AVSS | | | AN5 | | | | |

**ANCFG** ADC BAND GAP REFERENCE CONFIGURATION REGISTER: 0x0000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| - | - | - | - | - | - | - | - |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| - | - | - | - | - | VBG6EN | VBG2EN | VBGEN |
|  |  |  |  |  | ADC VBG/6 I/P EN | ADC VBG/2 I/P EN | ADC VBG I/P EN |
|  |  |  |  |  | 0 | 0 | 0 |
|  |  |  |  |  | DISABLED | DISABLED | DISABLED |

**AD1CHITH** ADC1 SCAN COMPARE HIT REGISTER (HIGH WORD): 0x0000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| - | - | - | - | - | - | CHH25 | CHH24 |
|  |  |  |  |  |  | ADC CMP HIT BIT | ADC CMP HIT BIT |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  |  |  |  |  |  | NO MATCH | NO MATCH |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CHH23 | CHH22 | CHH21 | CHH20 | CHH19 | CH18 | CHH17 | CHH16 |
| ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH |

**AD1CHITL** ADC1 SCAN COMPARE HIT REGISTER (LOW WORD): 0x0000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CHH15 | CHH14 | CHH13 | CHH12 | CHH11 | CHH10 | CHH9 | CHH8 |
| ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CHH7 | CHH6 | CHH5 | CHH4 | CHH3 | CHH2 | CHH1 | CHH0 |
| ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT | ADC CMP HIT BIT |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH | NO MATCH |

**AD1CSSH** ADC1 INPUT SCAN SELECT REGISTER (HIGH WORD): 0x0000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| - | CSS30 | CSS29 | CSS28 | CSS27 | CSS26 | CSS25 | CSS24 |
|  | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | SKIP | SKIP | SKIP | SKIP | SKIP | SKIP | SKIP |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CSS23 | CSS22 | CSS21 | CSS20 | CSS19 | CSS18 | CSS17 | CSS16 |
| ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SKIP | SKIP | SKIP | SKIP | SKIP | SKIP | SKIP | SKIP |

**AD1CSSL** ADC1 INPUT SCAN SELECT REGISTER (LOW WORD): 0x0000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CSS16 | CSS14 | CSS13 | CSS12 | CSS11 | CSS10 | CSS9 | CSS8 |
| ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SKIP | SKIP | SKIP | SKIP | SKIP | SKIP | SKIP | SKIP |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CSS7 | CSS6 | CSS5 | CSS4 | CSS3 | CSS2 | CSS1 | CSS0 |
| ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN | ADC SCAN |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SKIP | SKIP | SKIP | SKIP | SKIP | SKIP | SKIP | SKIP |

**AD1CTMENH ADC1** CTMU ENABLE REGISTER (HIGH WORD): 0x0000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| - | CTMEN30 | CTMEN29 | CTMEN28 | CTMEN27 | CTMEN26 | CTMEN25 | CTMEN24 |
|  | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CTMEN23 | CTMEN22 | CTMEN21 | CTMEN20 | CTMEN19 | CTMEN18 | CTMEN17 | CTMEN16 |
| CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED |

**AD1CTMENL ADC1** CTMU ENABLE REGISTER (LOW WORD): 0x0000

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CTMEN15 | CTMEN14 | CTMEN13 | CTMEN12 | CTMEN11 | CTMEN10 | CTMEN9 | CTMEN8 |
| CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CTMEN7 | CTMEN6 | CTMEN5 | CTMEN4 | CTMEN3 | CTMEN2 | CTMEN1 | CTMEN0 |
| CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN | CTMU EN |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED | DISABLED |

**Code Prg03.c**

/\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Source code file: Prg03.c

Author, version, date: PSS ver 1.0 01.11.24

Program function: ADC RF8 LED1 RF7 LED2 RF6 LED3 RA14 LED4

Simulation: PIC24FJ128GA308 MCU, MPLAB X IDE ver 6.05, XC16 ver 2.10

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/

#include <xc.h>

#include <libpic30.h>

uint16\_t pos**,** pot**;**

void initializeAdc **();**

uint16\_t readAdc **(**void**);**

int main**()**

**{**

initializeAdc**();** // Initialize ADC and analog inputs

**while** **(**1**)**

**{**

pot **=** readAdc**();** // Select the POT input and convert

pos **=** pot **>>** 8**;** // Reduce 12 bit value to a 4 bit value –

// dividing by 256 - right shift 8 times

LATFbits**.**LATF6 **=** **~(**pos **&** 0x0001**);**// Turn ON/OFF only one of the corresponding

// LEDs, LED3 RF6

LATFbits**.**LATF7 **=** **~(**pos **&** 0x0010**);**// LED2 RF7

LATFbits**.**LATF8 **=** **~(**pos **&** 0x0100**);**// LED1 RF8

LATAbits**.**LATA14 **=** **~(**pos **&** 0x1000**);**// LED4 RA14

**}**

**}**

void initializeAdc **()**

**{**

AD1CON1 **=** 0x8474**;** // ADON(1)-Turn ON ADC, MODE12(1)-12 bit

// operation, FORM(0,0)-Abs decimal unsigned right justified, SSRC(0111)-internal

// counter ands sampling and starts auto converting, ASAM(0)-manual sampling,

// SAMP(1)-start sampling after last conversion

AD1CON2 **=** 0x0078**;** // CSCNA(0)-No scan, ALTS(0)-use only ch A

// for sampling, SMPI(11110)-interrupt after every 31st sample conversion

AD1CON3 **=** 0x1E01**;** // SAMC(1111)-Auto Sample time = 31\*Tad,

// ADCS(00000001)-conversion clock-Tad = 2\*Tcy = 125 ns (Fcy = Fosc/2 = 16 MHz)

AD1CON4 **=** 0x0000**;**

AD1CON5 **=** 0x0006**;** // ASEN(0)-No autoscan, ASINT(00)-no

// interrupt, WM(01)-convert and save, CM(00)-less than mode (valid match when value

// is less than that in buffer register)

AD1CHS **=** 0x0005**;** // CH0NA(000)-Vref-/AVss, CH0SA(00101)-channel 5 AN5

ANCFG **=** 0x0000**;**

AD1CSSH **=** 0x0000**;**

AD1CSSL **=** 0x0000**;**

// AD1CHITH = 0x0000;

AD1CHITL **=** 0x0000**;**

AD1CTMENH **=** 0x0000**;**

AD1CTMENL **=** 0x0000**;**

TRISA **=** 0x0000**;** // RA14 is set in output mode

TRISF **=** 0x0000**;** // RF6, RF7, RF8 are set in output mode

LATF **=** 0x01C0**;** // Set all LEDs LOW initially

LATA **=** 0x4000**;** // All the LEDS are in common cathode configuration

**}**

uint16\_t readAdc **()**

**{**

**while** **(!**AD1CON1bits**.**DONE**);** // Wait to complete conversion

**return** ADC1BUF0**;** // Return the conversion result

**}**