Document No. Rev. 1.2
Product No.
Project Code
Model No.

WM-BN-BM-22 Application Note

SOURCE ORGANIZATION : USI WSS/WSS2/WP1/RD/HW

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Checked by： Date:

Approved by： Date :

Concurrence ： Date :

Change List

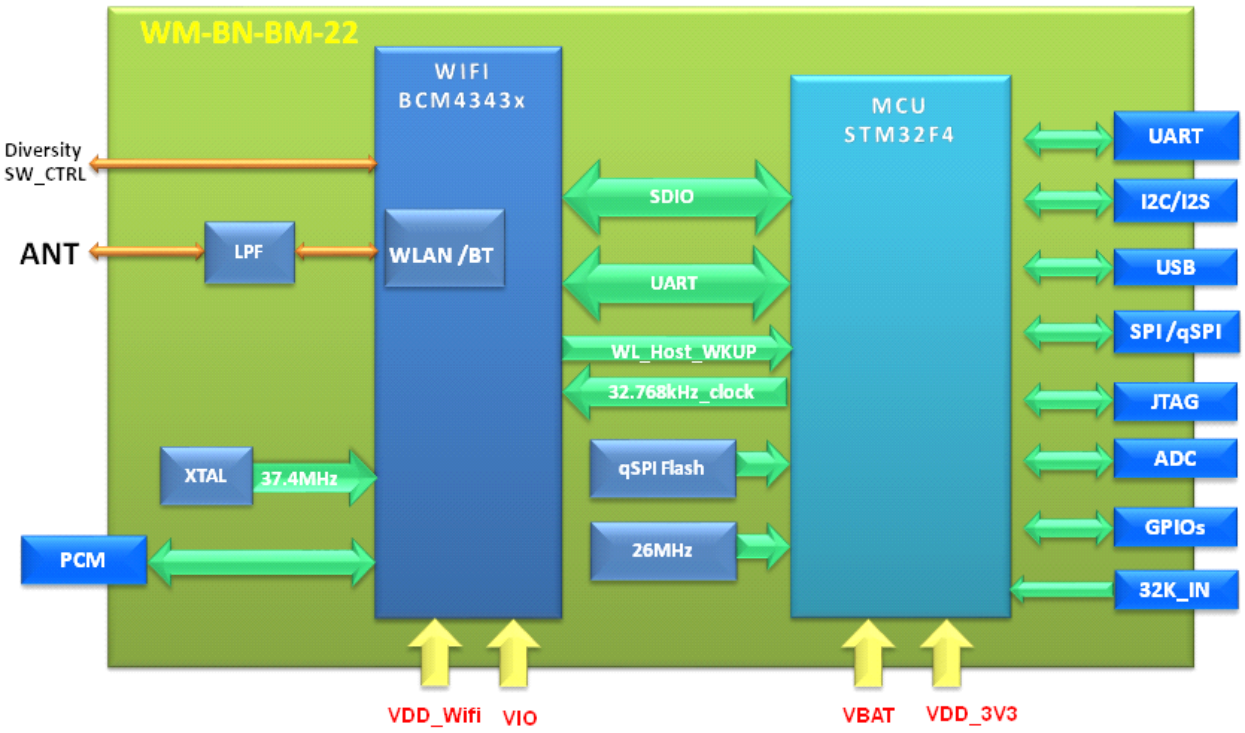
Rev.	Date	Description of change			Released by
		Page	Par		
1.0	2015-12-24	All	All	Initial release	Davis
1.1	2016-01-11	14,15		1. Add options on RTC 2. Add user instructions of EVB	Davis
1.2	2016-08-29	5,14, 15		1. Update RTC options 2. Update reference circuit 3. Update EVB instructions	Eason

Table of Contents

HW Application note for WM-BN-BM-22

1. Introduction

WM-BN-BM-22 is a WICED module includes WIFi/BT and Micro-processor. The WLAN is 2.4G single band that includes 802.11b/g/n function. The application note is composed of module power requirements, reference schematic description and the layout guideline for this module.



WM-BN-BM-22 Module

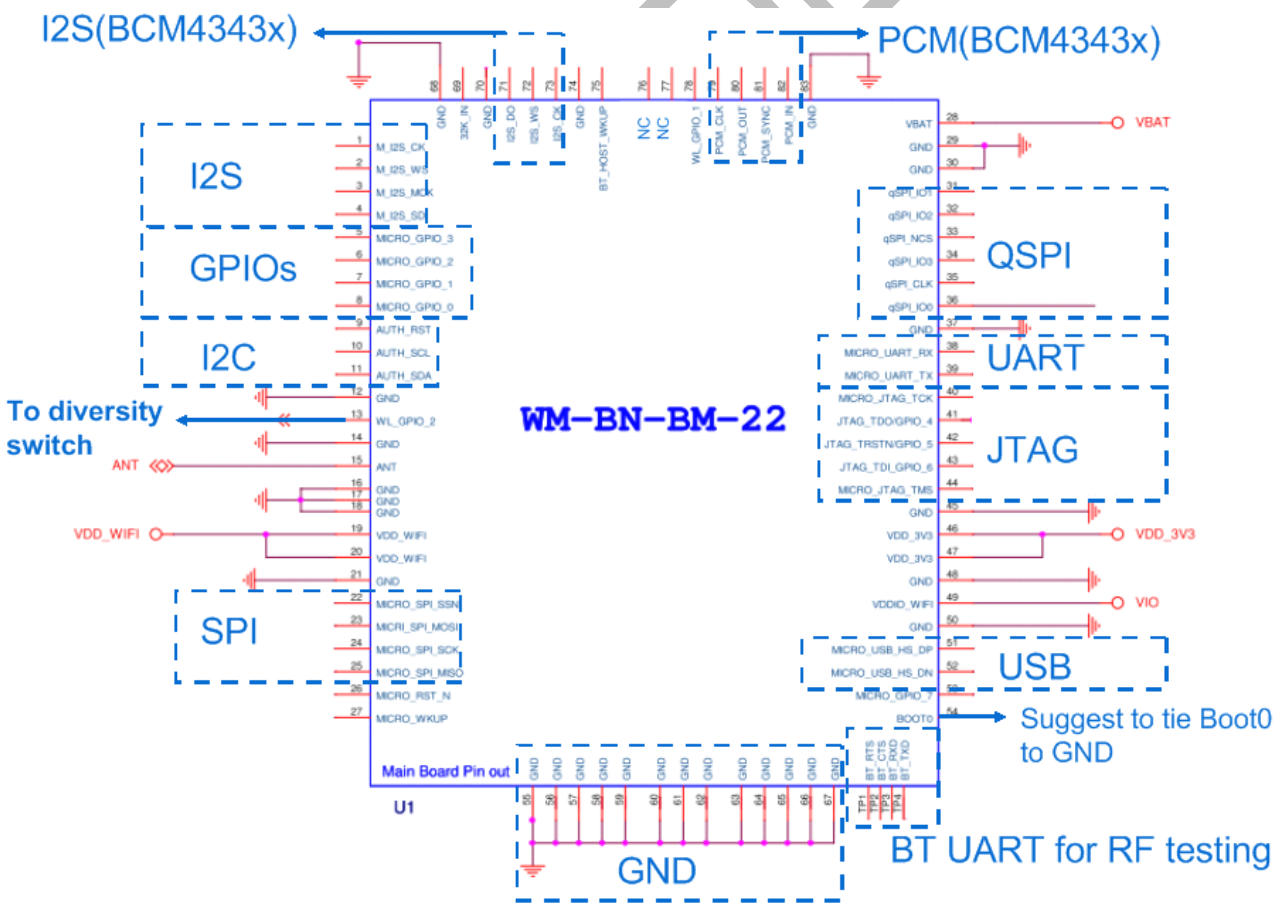
2. Power Supply

Power rails include VDD_WIFI, VDDIO_WIFI, MICRO_VDD_3V3 and VBAT. The recommended operational voltage is shown at below table.

Symbol	Parameter	Min	Typ	Max	Unit
VDD_WIFI*	power supply for BCM4343x	3.0	3.3	3.6	V
VDDIO_WIFI	host Interface power supply	3.0	3.3	3.6	V
VBAT	backup operating voltage	3.0	3.3	3.6	V
MICRO_VDD_3V3	power supply for MCU	3.0	3.3	3.6	V

Note: The BCM4343x is functional across this range of voltages. Optimal RF performance specified in this data sheet, however, is guaranteed only for 3.2V <VDD_WIFI<3.6V.

3. Reference Circuit



Note : 1. It is highly recommended that keeping the top layer of the module mounting area as GND-plane

2. Do not route any traces underneath the module

3. Cover the module with shielding case to avoid EMI issues.

4. Layout suggestion

DC power

Use wide traces for power supply lines. Understand the maximum current carried on each power supply trace, and make the trace widths proportionate to the current (especially for long trace lengths). If possible, fill large areas with copper to distribute the highest currents. These measures minimize IR drops, line inductance, and switching transients.

- Use several plated via holes to connect power supply traces between layers. The number of vias used should be proportional to the current being routed.
- Avoid loops in the supply distribution traces. Current-carrying loops are essentially antennas radiating electromagnetic fields that may corrupt transceiver performance or cause regulatory electromagnetic interference (EMI) test failures

- The bypass capacitors for power sources should be as close to module pin out as possible.
- If there are two different capacitors for signal power source, please placed the one with low capacitance to be closer to module pin out.

WM-BN-BM-22 Maximum current table

Power Consumption	MAX*
VDD_WIFI	310 mA
VIO	50 mA
VBAT	50 mA
VDD_3V3	120 mA

Table1.

Note: Preliminary data. Will update after performing complete quality verification.

5. IO Mappings

5.1 All IO Mappings

WM-BN-BM-22 pin mapping with STM32F412 as below:

Pin-No	Symbol	ST32F4xx
1	I2S_CK	G3(PB12)
2	I2S_WS	G6(PA4)
3	I2S_MCK	H4(PB10)
4	I2S_SD	A3(PC12)
5	MICRO_GPIO_3	C7(PC15)
6	MICRO_GPIO_2	F4(PB1)
7	MICRO_GPIO_1	H5(PB0)
8	MICRO_GPIO_0	F5(PA5)
9	AUTH_RST	B8(PC13)
10	AUTH_SCL	B5(PB6)
11	AUTH_SDA	A6(PB7)
12	GND	----------
13	RF_SW_CTRL	----------
14	GND	----------
15	ANT	----------
16	GND	----------
17	GND	----------
18	GND	----------
19	VDD_WIFI	----------
20	VDD_WIFI	----------
21	GND	----------
22	MICRO_SPI_SSN	B6(PB9)
23	MICRI_SPI_MOSI	D6(PC3)
24	MICRO_SPI_SCK	G2(PB13)
25	MICRO_SPI_MISO	E7(PC2)
26	MICRO_RST_N	D7

27	MICRO_WKUP	D5(PC0)
28	VBAT	----------
29	GND	----------
30	GND	----------
31	qSPI_IO1	E5(PA7)
32	qSPI_IO2	E4(PC4)
33	qSPI_NCS	B3(PC11)
34	qSPI_IO3	G5(PC5)
35	qSPI_CLK	G4(PB2)
36	qSPI_IO0	H6(PA6)
37	GND	----------
38	MICRO_UART_RX	D2(PA10)
39	MICRO_UART_TX	D1(PA9)
40	MICRO_JTAG_TCK	B2(PA14)
41	MICRO_JTAG_TDO	A5(PB3)
42	MICRO_JTAG_TRSTN	B4(PB4)
43	MICRO_JTAG_TDI	A2(PA15)
44	MICRO_JTAG_TMS	C2(PA13)
45	GND	----------
46	VDD_3V3	----------
47	VDD_3V3	----------
48	GND	----------
49	VDDIO_WIFI	----------
50	GND	----------
51	MICRO_USB_HS_DP	C1(PA12)
52	MICRO_USB_HS_DN	D3(PA11)
53	MICRO_GPIO_7	G1(PB14)
54	BOOT0	D4
55	GND	----------
56	GND	----------
57	GND	----------
58	GND	----------

59 ~ 67	GND	----------
68	GND	----------
69	32K_IN	C8(PC14)
70	GND	----------
71	BT_I2S_DO	----------
72	BT_I2S_WS	----------
73	BT_I2S_CLK	----------
74	GND	----------
75	BT_HOST_WKUP	----------
76	NC	----------
77	NC	----------
78	WL_GPIO_1	----------
79	BT_PCM_CLK	----------
80	BT_PCM_OUT	----------
81	BT_PCM_SYNC	----------
82	BT_PCM_IN	----------
83	GND	----------
TP1	BT_RTS	----------
TP2	BT_CTS	----------
TP3	BT_RXD	----------
TP4	BT_TXD	----------

5.2 Interface of SPI,UART, I2C,I2S and QSPI

PIN 22/23/24/25 pins for SPI interface. Table2. describes the SPI pins.

Table2. SPI Interface

Pin-No	Symbol	Pin Type	Description
22	MICRO_SPI_SSN	I/O	SPI_SS
23	MICRI_SPI_MOSI	I/O	SPI_MOSI
24	MICRO_SPI_SCK	I/O	SPI_SCK
25	MICRO_SPI_MISO	I/O	SPI_MISO

PIN 38/39 pins for UART interface. Table3. describes the UART pins.

Table3. UART Interface

Pin-No	Symbol	Pin Type	Description
38	MICRO_UART_RX	I/O	UART_RX
39	MICRO_UART_TX	I/O	UART_TX

PIN 9/10/11 pins for I2C interface. Table4. describes the I2C pins.

Table4. I2C Interface

Pin-No	Symbol	Pin Type	Description
9	AUTH_RST	O	I2C_RST pin
10	AUTH_SCL	O	I2C_SCL pin
11	AUTH_SDA	I/O	I2C_SDA pin

PIN 1/2/3/4 pins for I2S interface. Table5. describes the I2S pins.

Table5. I2S Interface

Pin-No	Symbol	Pin Type	Description
1	I2S_CK	I/O	I2S_CK pin
2	I2S_WS	I/O	I2S_WS pin
3	I2S_MCK	I/O	I2S_MCK pin
4	I2S_SD	I/O	I2S_SD pin

PIN 31~36 pins for qSPI interface. Table6. describes the SPI pins.

Table6. qSPI Interface

Pin-No	Symbol	Pin Type	Description
31	qSPI_IO1	I/O	qSPI_IO1 pin
32	qSPI_IO2	I/O	qSPI_IO2 pin
33	qSPI_NCS	O	qSPI_NCS pin
34	qSPI_IO3	I/O	qSPI_IO3 pin
35	qSPI_CLK	O	qSPI_CLK pin
36	qSPI_IO0	I/O	qSPI_IO0 pin

PIN 51/52 pins for qSPI interface. Table7. describes the USB pins.

Table7. USB Interface

Pin-No	Symbol	Pin Type	Description
51	MICRO_USB_HS_DP	I/O	USB_HS_DP
52	MICRO_USB_HS_DN	I/O	USB_HS_DN

6. JTAG Interface

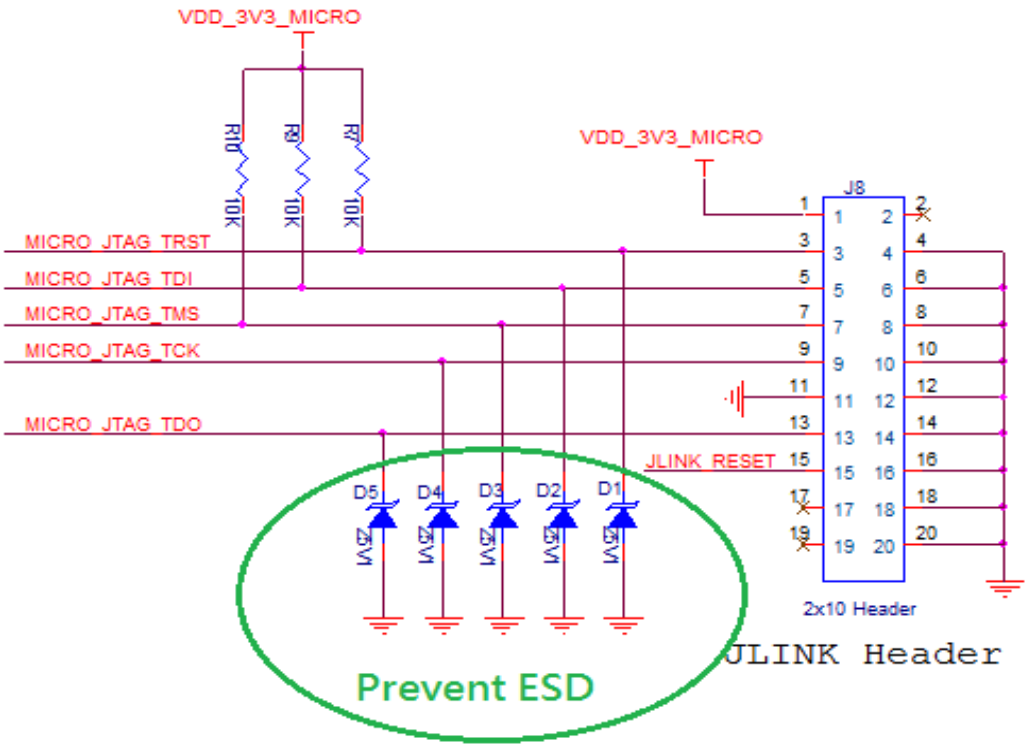
PIN 40~44 pins for JTAG interface that can be used for programming MCU. Table8. describes these JTAG pins.

Table8. JTAG Interface

Pin-No	Symbol	Pin Type	Description
40	MICRO_JTAG_TCK	I/O	JTAG_TCK

41	MICRO_JTAG_TDO	I/O	JTAG_TDO
42	MICRO_JTAG_TRSTN	I/O	JTAG_TRSTN
43	MICRO_JTAG_TDI	I/O	JTAG_TDI
44	MICRO_JTAG_TMS	I/O	JTAG_TMS

We suggest customer follow the EVB design shown below. All JTAG signals should connect to 2x10 header which can link to ST-LINK/OLIMEX ARM-USB-TINY-H cable to program MCU.



Please find detail information from link as below,
https://www.olimex.com/Products/ARM/JTAG/ARM-USB-TINY-H/

ARM-USB-TINY-H

Device summary

Part number	Order Code	Description
ST-LINK/V2	ST-LINK/V2	In-circuit debugger/programmer
	ST-LINK/V2-ISOL	In-circuit debugger/programmer with digital isolation

ST-LINK/V2

ST-LINK/V2-ISOL

ST-Link/v2 Utility :

http://www.st.com/st-web-ui/static/active/en/st_prod_software_internet/resource/technical/software/utility/stsw-link004.zip

ST-Link/v2 driver :

http://www.st.com/st-web-ui/static/active/en/st_prod_software_internet/resource/technical/software/driver/st-link_v2_usbdriver.zip

7. Boot Mode Options

In the STM32F412, three different boot modes can be selected through the BOOT0 pins shown below

At startup, boot pins are used to select one out of three boot options:

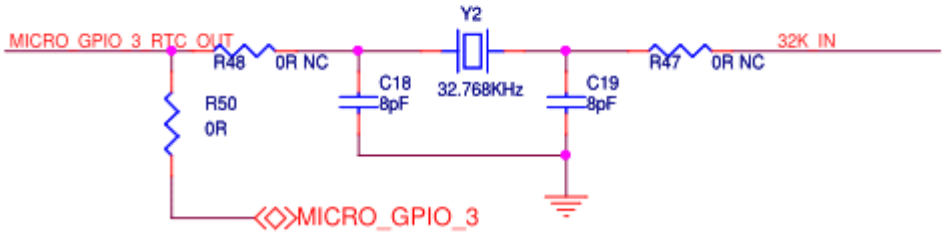
- Boot from user Flash memory
- Boot from system memory
- Boot from embedded SRAM

Suggest to tie the BOOT0 to GND, the Boot mode is from main flash memory. For more details, please refer to STM32F412 data sheet.

8. RTC Options

The default 32.768kHz could be from STM32F412. For more accurate RTC in sleep mode, please feed a 32.768kHz signal on pin#69(32K_IN) by OSC. If the RTC is from external source, please leave MICRO_GPIO_3 floating as the IO function is limited.
Another option is use crystal as following application circuit,

GPIO_3 could be RTC_OUT for 32.768K XTAL



Pin#5(MICRO_GPIO_3) could be 32K_OUT.
For detailed clock characteristics and crystal specs, please refer to STM32F412 data sheet.

9. EVB Instructions