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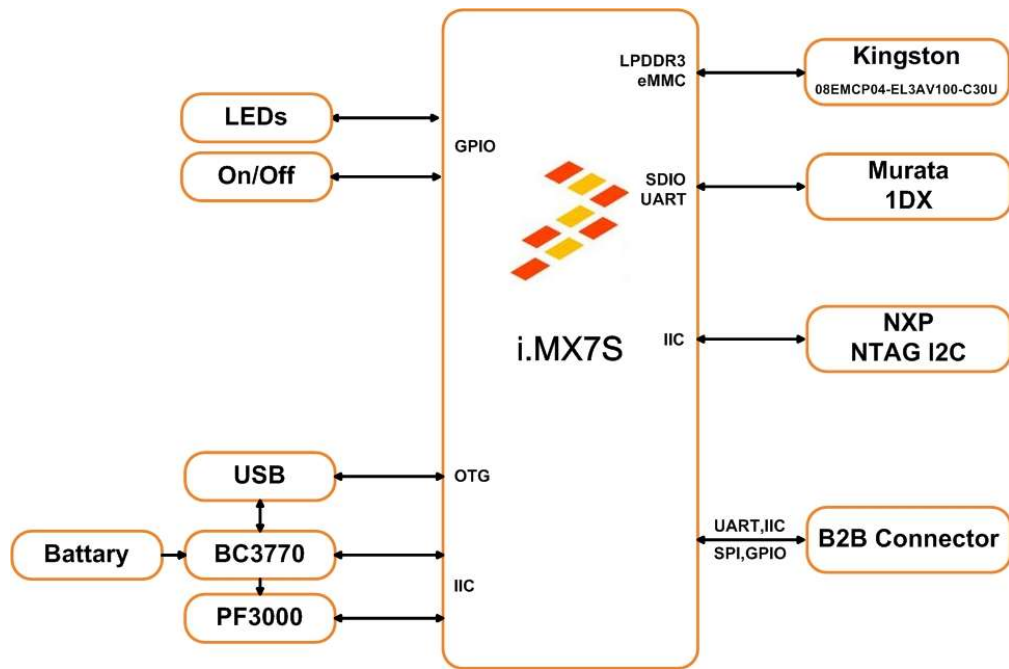
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Revision History

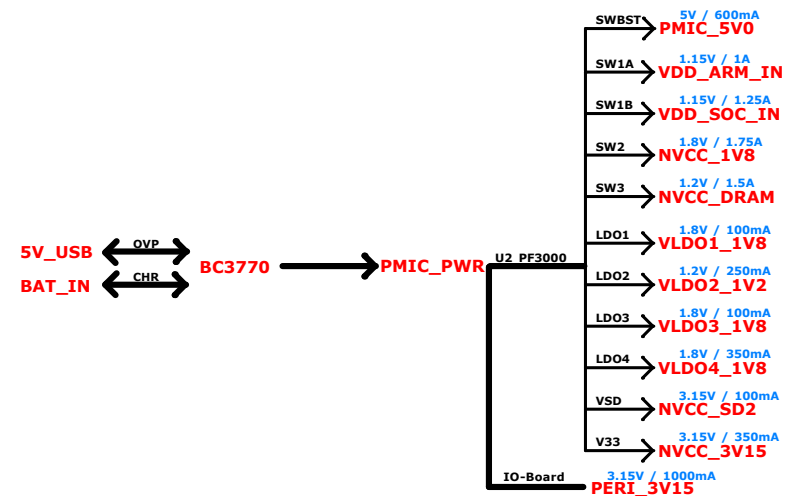
Rev. Code	Date	Description
V1.2	07/04/2015	Initial Draft

# WaRP7-CPU Board

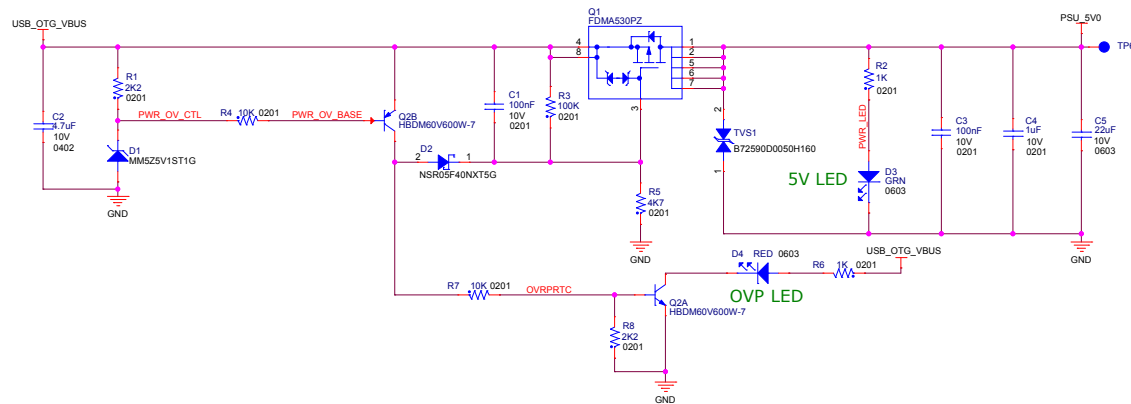
## Warp7 CPU Board Block Diagram



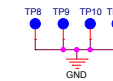
## Power Distribution Diagram



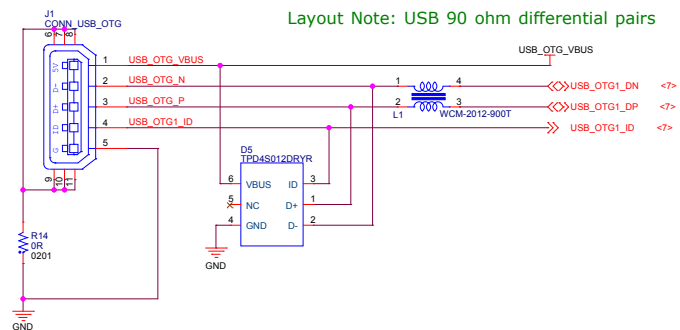
# OVER VOLTAGE INTICATOR



Note: The Drain and Source of MOSFET could exchange with each other. Provide power for the system when the USB OTG port acting as an OTG B-device. Or output 5V from BC3770 when the port is acting as an OTG A-device.

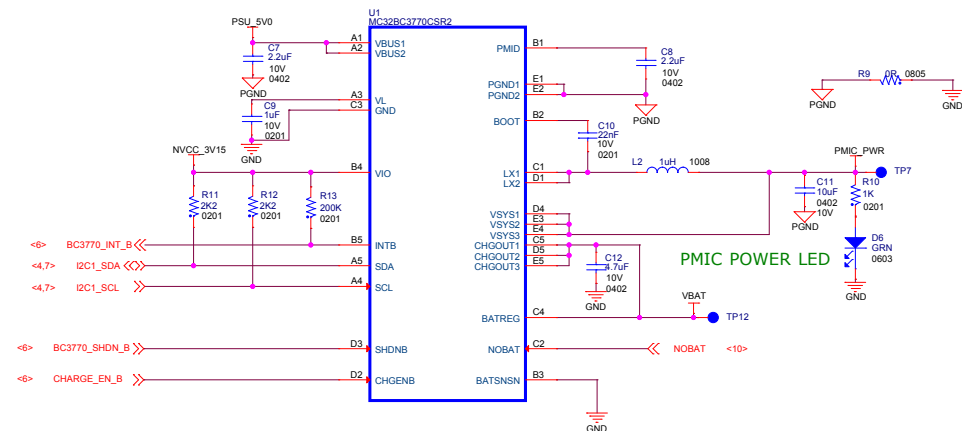


# USB OTG

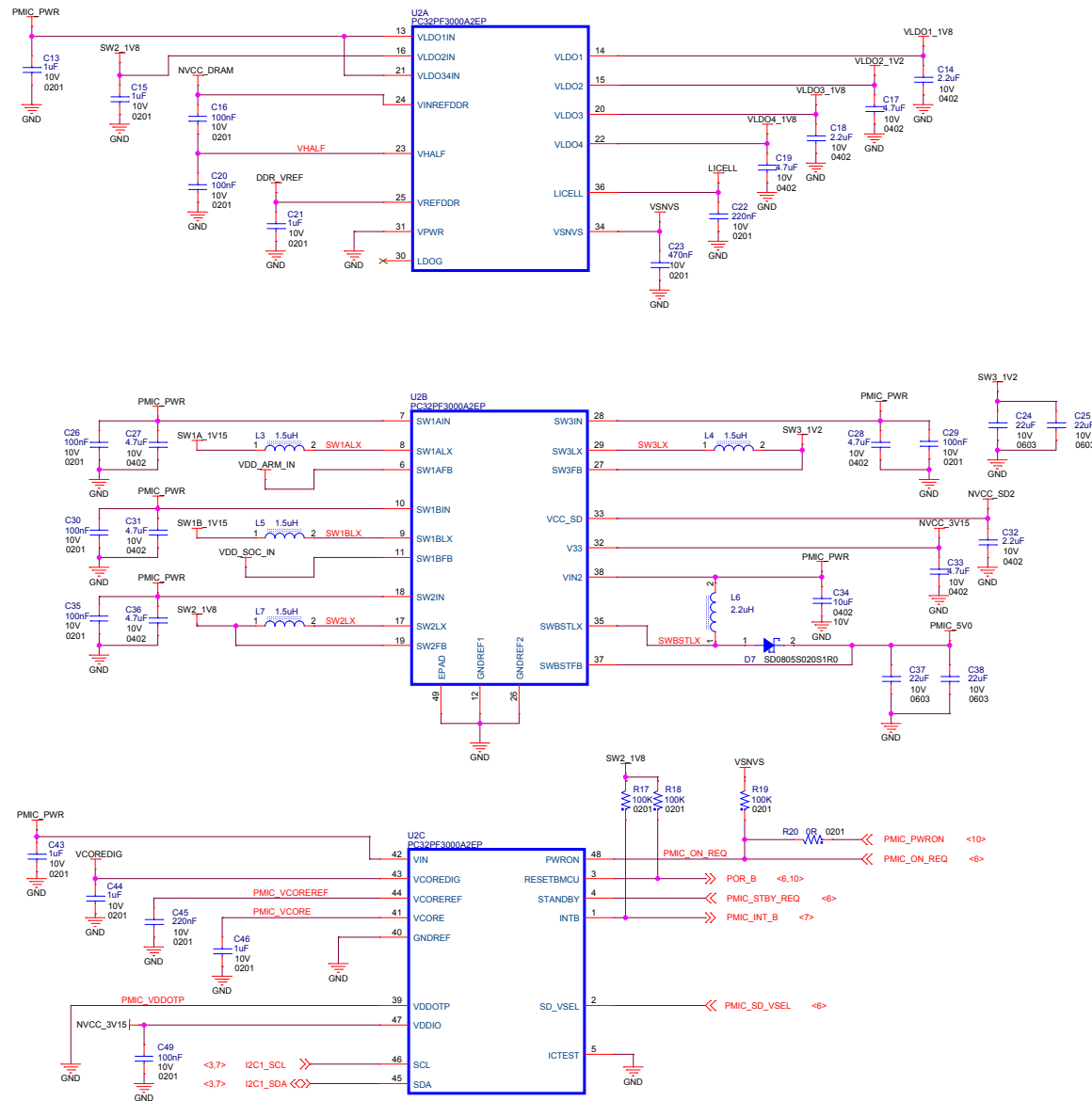


# BATTERY CHARGE

Note: Use the pin VBUS of BC3770 as 5V output in the OTG mode, the current limit is up to 900mA, and it will make interrupt signal to processor when the external system is overload.



# PMIC

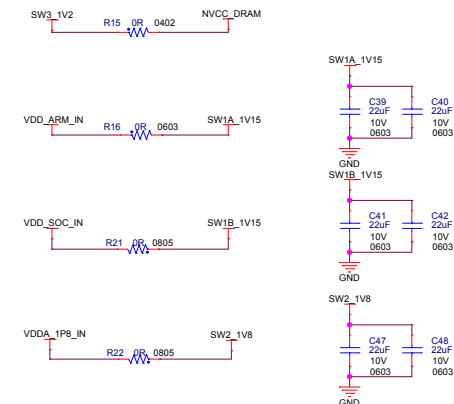


Note:

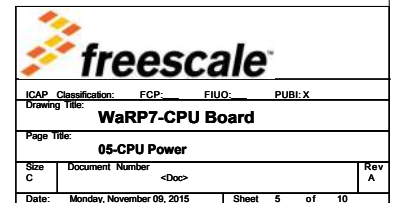
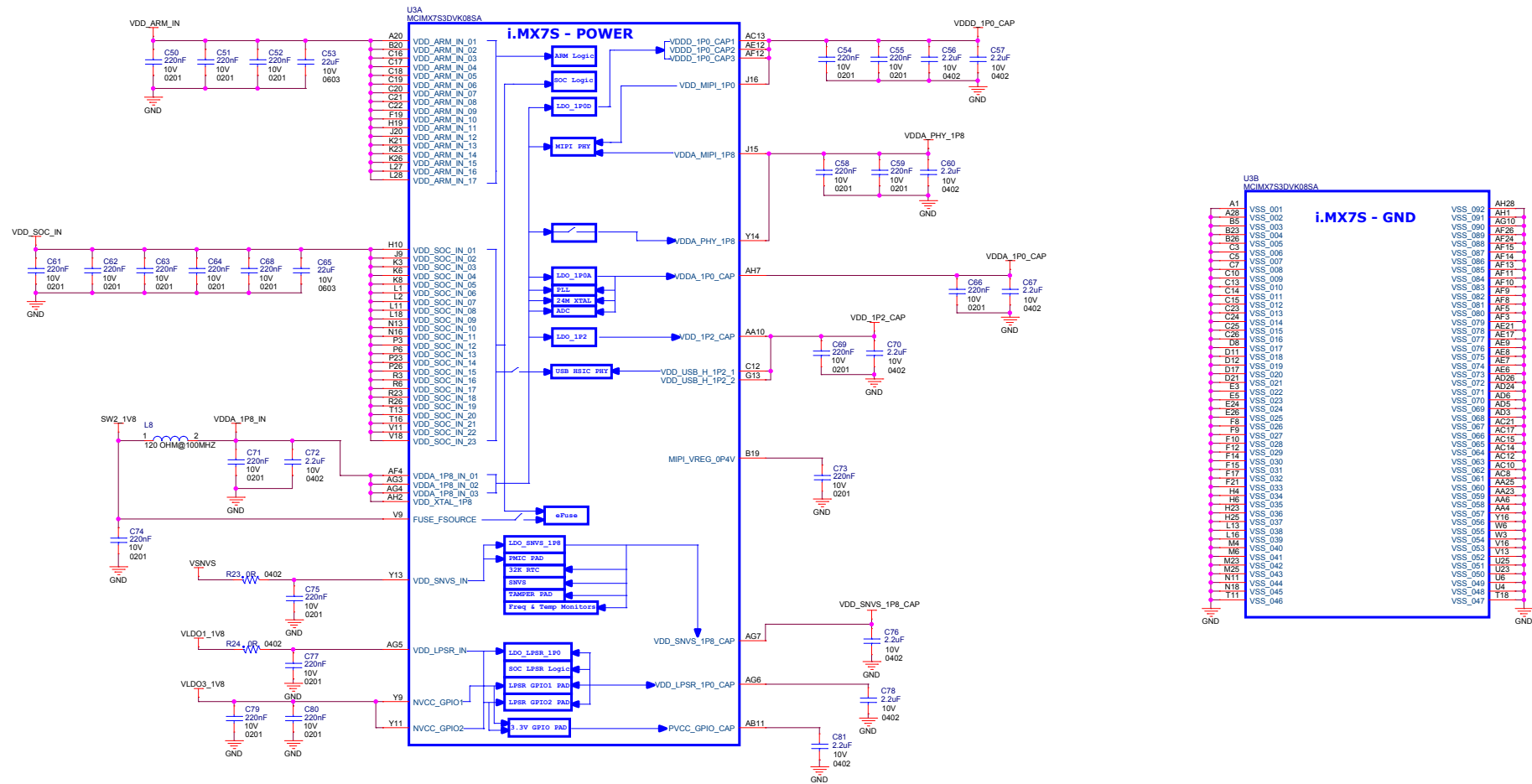
This device is factory configurable for voltage and timings.  
This reference design is configured to run from factory pre-programmed parts.  
Ordering selections with common i.MX7S voltages/timings are available.

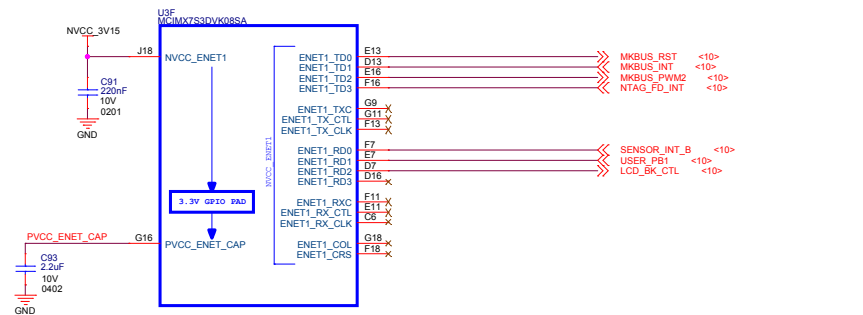
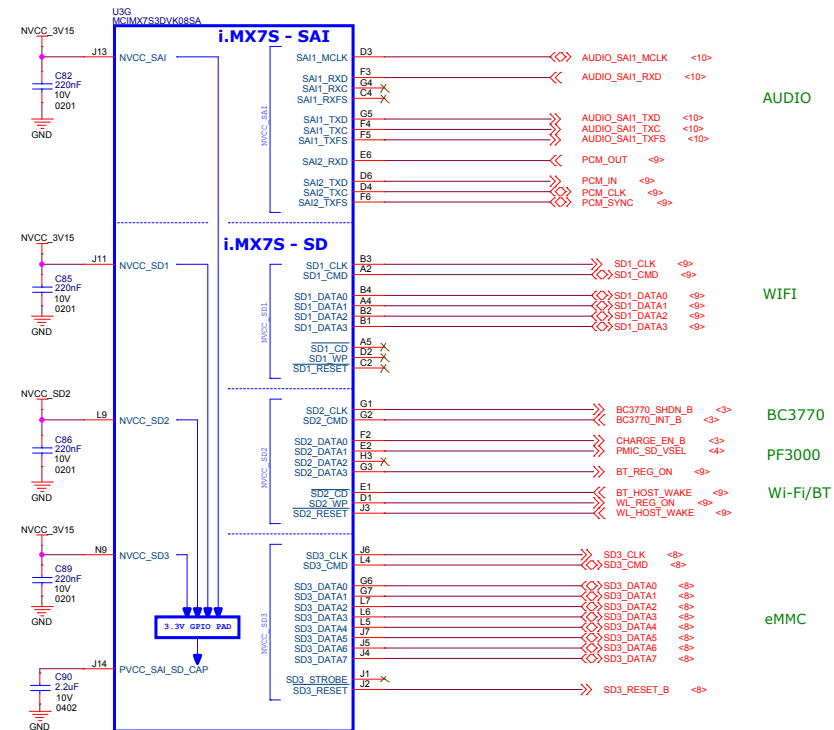
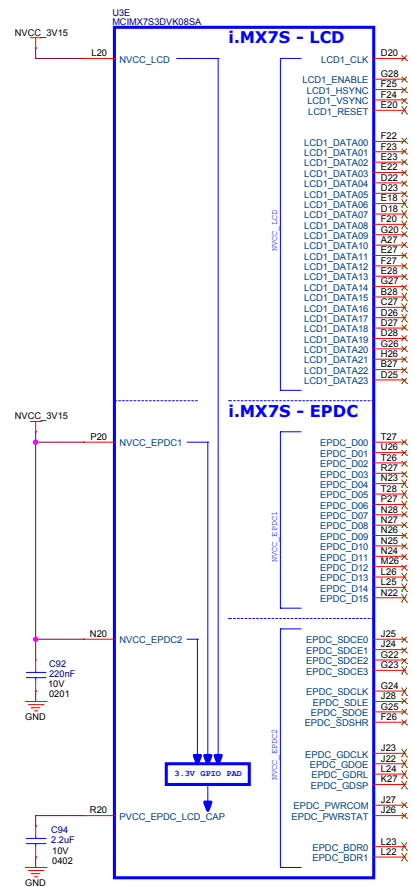
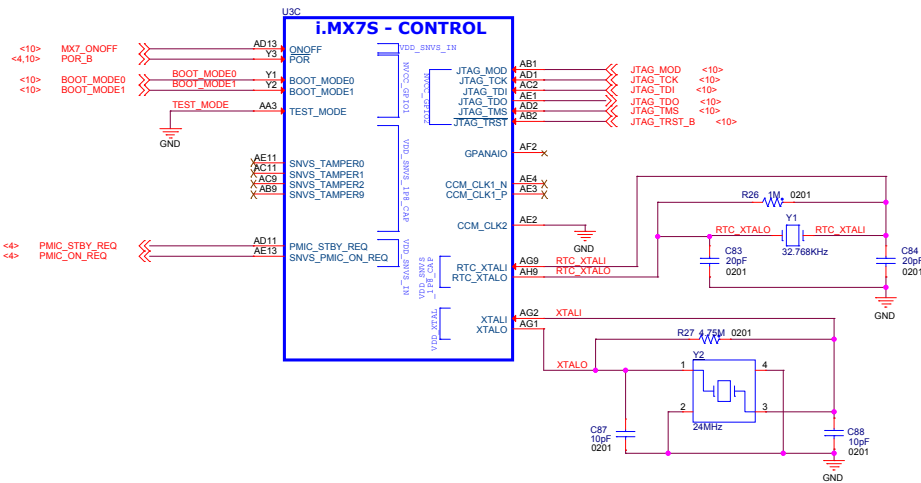
## PMIC Output Rails

PF3000	Voltage	Current	Sequence
SW1A	1.15V	1000mA	1
SW1B	1.15V	1750mA	1
SW2	1.8V	1250mA	2
SW3	1.2V	1500mA	3
VSNVS	3.0V	1mA	0
SWBST	-	600mA	-
VREFDDR		10mA	3
VLDO1	1.8V	100mA	2
VLDO2	1.2V	250mA	-
VLDO3	1.8V	100mA	2
VLDO4	1.8V	350mA	-
V33	3.15V	350mA	2
VCC_SD	3.15V	100mA	3



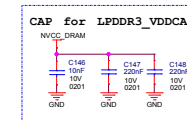
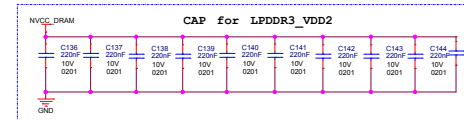
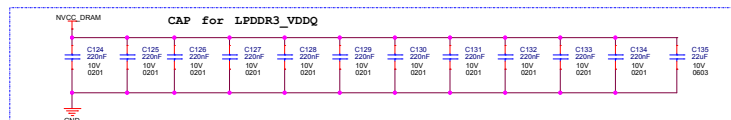
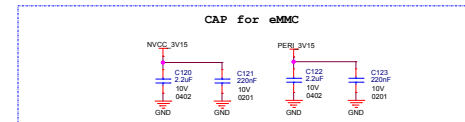
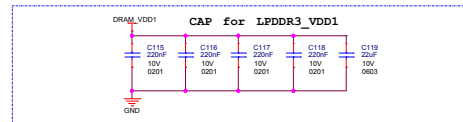
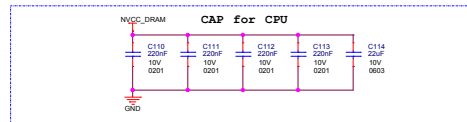
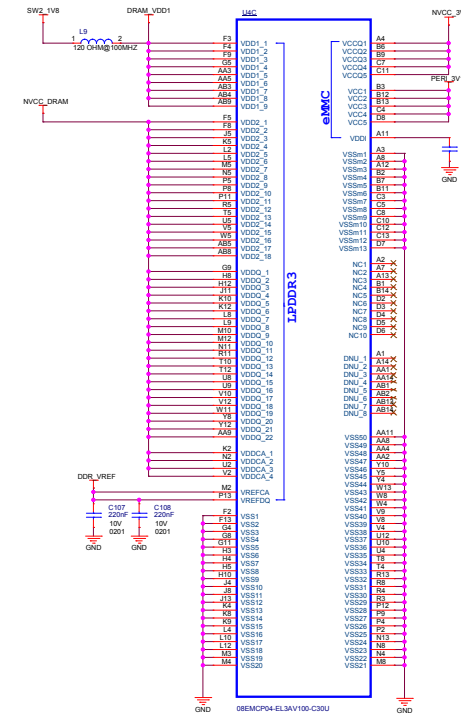
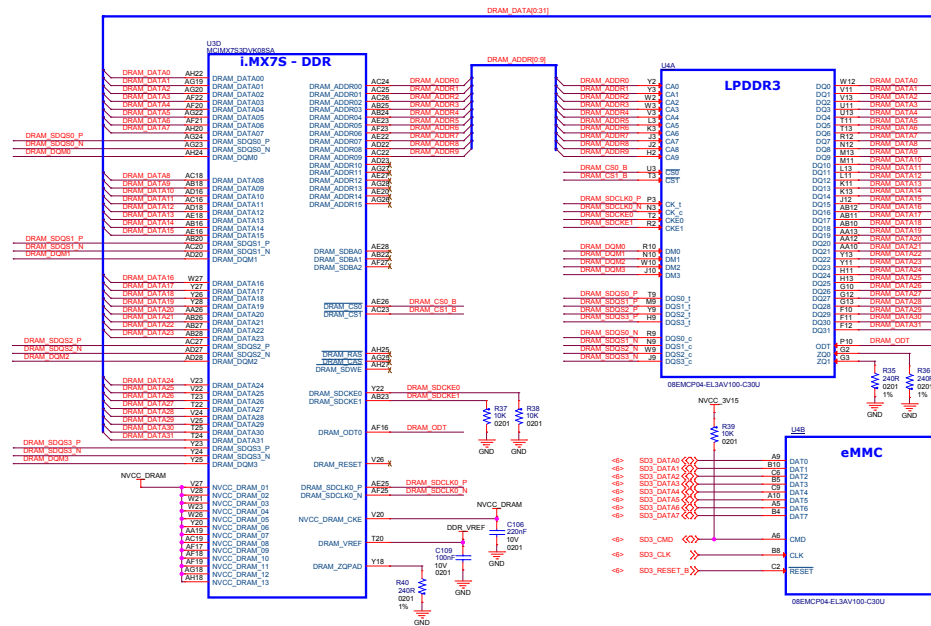
# CPU\_POWER







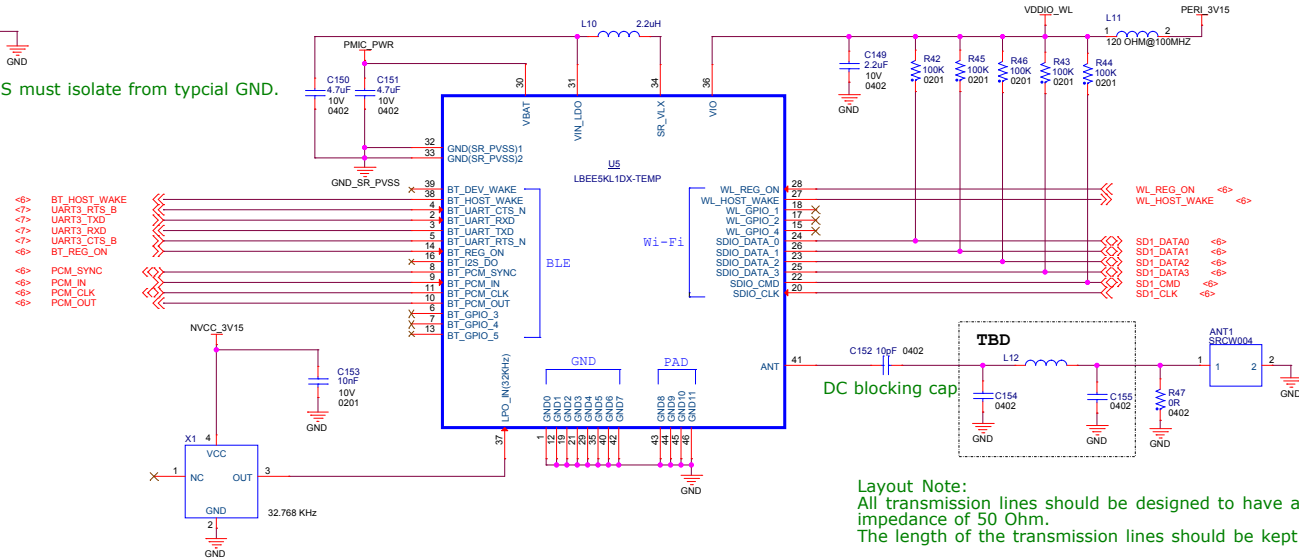
## LPDDR2 & eMMC



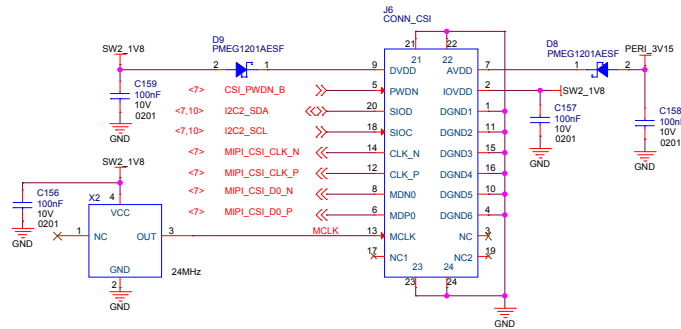


# Wi-Fi & Bluetooth

Note: GND\_SR\_PVSS must isolate from typical GND.



# CSI



Note: The camera module's IIC address is 0x6C(write), 0x6D(read).

# B2B Connector

Note: All clock signals are isolated to other signals with GND.

