

DATA SHEET

Wi-SUN/LECIM Compliant Transceiver

AXR100



DEVICE SPECIFICATION Ver.0.6

General Features

- Programmable Output Power up to +13.5dBm
- Receive Sensitivity Down to -107dBm (@ 12.5kbps, 128 packet length)
- Data rate: 12.5/25/50/150/200 kbps
- Frequency Bands: 902 ~ 928MHz (include KOREAN RFID/USN)
- HW AES128 Security Engine
- Automatic CCA and ACK
- MAX Payload size: 2048Bytes
- Package: QPN 48 pin package, 7mm X 7mm
- Temperature range: -25°C to +80°C
- Dual PHY:

IEEE802.15.4g (SUN, Smart Utility Network)

IEEE802.15.4k (LECIM, Low Energy Critical Infra structure Monitoring)

• Certificated with Wi-SUN Alliance

Applications

- Low-Power Wireless Applications Operating in the 902-928MHz ISM Band
- Automated Meter Reading
- Home and Building Automation
- Industrial Monitoring and Control
- Wireless Alarm and Security Systems
- IoT(Internet of Things)

Revision History

Author	Description of Changes	Date
A2U	Initial Draft	Oct. 2016
A2U	Add Test Result	Feb. 2017
A2U	Revision format	Sep. 2017

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Contents

1	Introduction	5
	1.1 Functional Block Diagram	5
2	Terminal Configuration and Functions	6
	2.1 Pin Diagram	6
	2.2 Pin Description	6
3	Specification	9
	3.1 General Characteristics	9
	3.2 Absolute Maximum Ratings	9
	3.3 Handling Ratings	9
	3.4 Recommended Operation Conditions	9
	3.5 Current Consumption	9
	3.6 Tx Current Consumption	10
	3.7 RX Current Consumption	10
	3.8 RF Receive Section	10
	3.8.1 General Receive Parameters	.10
	3.8.2 Receive Performance in 920.1 MHz bands	.11
	3.9 RF Transmit Section	13
	3.9.1 General Transmit Parameters	.13
	3.9.2 Adjacent Channel Leakage Ratio	.13
	3.10 Crystal Oscillator	14
	3.11 PLL Characteristics	14
	3.12 Wake-up and Timing	15
	3.13 I/O and Reset	15
4	Typical Performance characteristics	17



Abbreviations

AXR100 A2UICT RF Transceiver

AXP100 A2UICT Processor for IOT

AXT100 A2UICT Wi-SUN Antenna

AXM100 IEEE802.15.4g/k Compliant LPWAN Module

ACLR Adjacent channel leakage ratio

AES Advanced encryption standard

AGC Automatic gain control

AFC Automatic frequency control

FSK frequency shift keying

CAP contention access period

CCA clear channel assessment

CSMA-CA carrier sense multiple access with collision avoidance

FFD full-function device

GTS guaranteed time slot

ED energy detection

MAC medium access control

PHY physical layer

RSSI Received signal strength indicator

RF radio frequency

SAP service access point

SFD start-of-frame delimiter

WPAN wireless personal area network

1 Introduction

The AXR100 is a cost optimized sub-1 GHz RF transceiver for the 902–928 MHz frequency bands. The RF transceiver is integrated with a highly configurable baseband modem. The modem supports various data rates and has a configurable data rate up to 200 kbps.

1.1 Functional Block Diagram

Figure 1 shows a functional block diagram of the device.

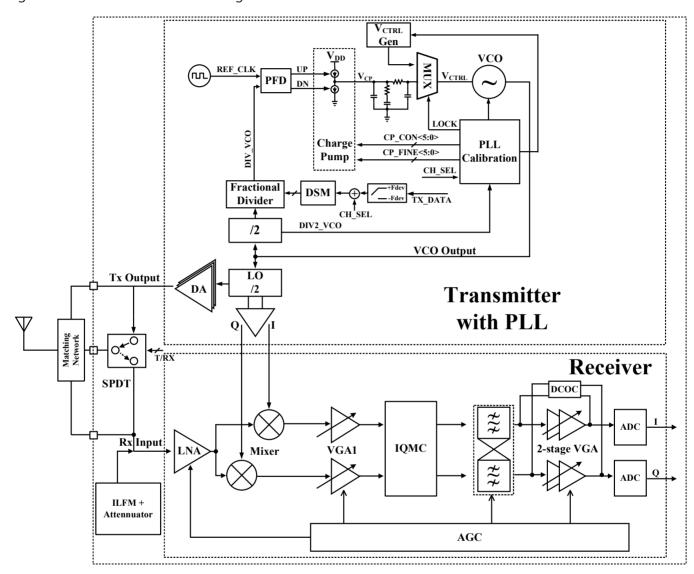


Figure 1 Functional Block Diagram

2 Terminal Configuration and Functions

2.1 Pin Diagram

Figure 2 shows pin names and locations for the AXR100 device.

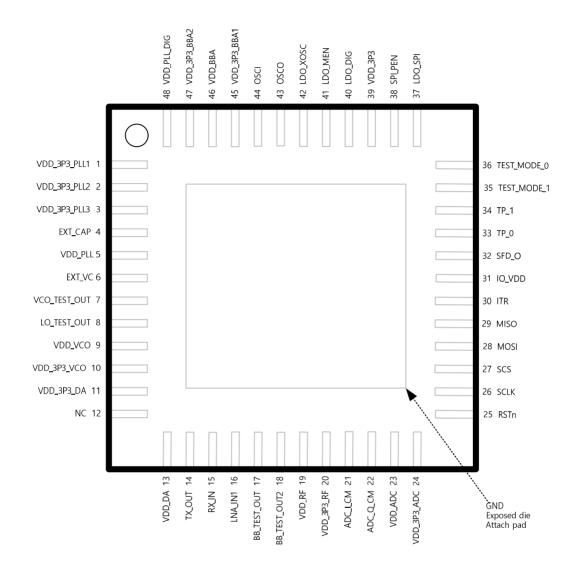


Figure 2 Pinout(Top View)

2.2 Pin Description

Pin No.	Pin Name	Signal Type (I/O/IO/P/G)	Descriptions					
1	VDD_3P3_PLL1	Р	Power for PLL 3.3V					
2	VDD_3P3_PLL2	Р	Power for PLL 3.3V					
3	VDD_3P3_PLL3	Р	Power for PLL 3.3V					
4	EXT_CP	IO	External Loop Filter component					
5	VDD_PLL	IO	Power for PLL					
6	EXT_VC	IO	External Loop Filter component					

7 VCO_TEST_OUT O Test output port for VCO 8 LO_TEST_OUT O Test output port for LO 9 VDD_VCO IO Decoupling Cap for VCO LDO 10 VDD_3P3_VCO P Power for VCO 3.3V 11 VDD_3P3_DA P Power for DA 3.3V 12 N.C - No connect 13 VDD_DA IO Decoupling Cap for DA LDO 14 TX_OUT O TX output port 15 RX_IN I Input for RX 16 LNA_IN I LNA Input 17 BB_TEST_OUTIB O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 18 BB_TEST_OUTIB O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 19 VDD_RF IO Decoupling Cap for Power for RF 20 VDD_3P3_RF P Power for RF 3.3V 21 ADC_LCM O Decoupling cap for ADC I common mode voltage 22 ADC_QCM O Decoupling cap for ADC Q common mode voltage		_				
9 VDD_VCO IO Decoupling Cap for VCO LDO 10 VDD_3P3_VCO P Power for VCO 3.3V 11 VDD_3P3_DA P Power for DA 3.3V 12 N.C - No connect 13 VDD_DA IO Decoupling Cap for DA LDO 14 TX_OUT O TX output port 15 RX_IN I Input for RX 16 LNA_IN I LNA Input 17 BB_TEST_OUTI O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 18 BB_TEST_OUTIB O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 19 VDD_RF IO Decoupling Cap for Power for RF 20 VDD_3R3 P Power for RF 3.3V 21 ADC_LCM O Decoupling cap for ADC I common mode voltage 22 ADC_QCM O Decoupling cap for ADC Q common mode voltage 23 VDD_ADC IO Decoupling cap for ADC LDO 24 VDD_3P3_ADC P Power for ADC 3.3V	7	VCO_TEST_OUT	0	Test output port for VCO		
10	8	LO_TEST_OUT	0	Test output port for LO		
11	9	VDD_VCO	IO	Decoupling Cap for VCO LDO		
12	10	VDD_3P3_VCO	Р	Power for VCO 3.3V		
TX_OUT	11	VDD_3P3_DA	Р	Power for DA 3.3V		
14 TX_OUT O TX output port 15 RX_IN I Input for RX 16 LNA_IN I LNA Input 17 BB_TEST_OUTI O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 18 BB_TEST_OUTIB O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 19 VDD_3F IO Decoupling Cap for Power for RF 20 VDD_3P3_RF P Power for RF 3.3V 21 ADC_I_CM O Decoupling cap for ADC I common mode voltage 22 ADC_Q_CM O Decoupling cap for ADC Q common mode voltage 23 VDD_ADC IO Decoupling cap for ADC Q common mode voltage 24 VDD_3P3_ADC P Power for ADC 3.3V 25 RSTn I Reset (Active Low) 26 SCLK I Serial Port Clock 27 SCS I Serial Port Chip Select (Active Low) 28 MOSI I Serial Port Master In/Slave Out 30 INTR IO MAC HW	12	N.C	-	No connect		
15 RX_IN I Input for RX 16 LNA_IN I LNA Input 17 BB_TEST_OUTI O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 18 BB_TEST_OUTIB O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 19 VDD_RF IO Decoupling Cap for Power for RF 20 VDD_3P3_RF P Power for RF 3.3V 21 ADC_I_CM O Decoupling cap for ADC I common mode voltage 22 ADC_Q_CM O Decoupling cap for ADC Q common mode voltage 23 VDD_ADC IO Decoupling cap for ADC LDO 24 VDD_3P3_ADC P Power for ADC 3.3V 25 RSTn I Reset (Active Low) 26 SCLK I Serial Port Clock 27 SCS I Serial Port Clop Serial Port Chip Select (Active Low) 28 MOSI I Serial Port Master Out/Slave In 29 MISO IO Serial Port Master In/Slave Out 30 INTR IO MAC HW Interrupt (Active High) 31 IO_VDD P Power for IO interface 32 SFD_OUT O Tx/Rx SFD Signal 33 TP[0] O Test Point 0 34 TP[1] O Test Point 0 35 TEST_MODE[1] I SCAN/BIST Mode Selection 36 TEST_MODE[0] I SCAN/BIST Mode Selection 37 LDO_SPI IO Decoupling cap for SPI LDO 38 SPI_PEN IO SPI LDO Enable 39 VDD_3P3 P Power for digital parts, XOSC 40 LDO_DIG IO Decoupling cap for SPI LDO 41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for Memory LDO	13	VDD_DA	IO	Decoupling Cap for DA LDO		
LINA_IN LINA Input	14	TX_OUT	0	TX output port		
17 BB_TEST_OUTI O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 18 BB_TEST_OUTIB O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 19 VDD_RF IO Decoupling Cap for Power for RF 20 VDD_3P3_RF P Power for RF 3.3V 21 ADC_I_CM O Decoupling cap for ADC I common mode voltage 22 ADC_Q_CM O Decoupling cap for ADC Q common mode voltage 23 VDD_ADC IO Decoupling cap for ADC LDO 24 VDD_3P3_ADC P Power for ADC 3.3V 25 RSTn I Reset (Active Low) 26 SCLK I Serial Port Clock 27 SCS I Serial Port Clock 28 MOSI I Serial Port Master Out/Slave In 29 MISO IO Serial Port Master In/Slave Out 30 INTR IO MAC HW Interrupt (Active High) 31 IO_VDD P Power for IO interface 32 SFD_OUT O Tx/Rx SFD Signal 33 TP[0] O Test Point 0 34 TP[1] O Test Point 1 35 TEST_MODE[1] I SCAN/BIST Mode Selection 36 TEST_MODE[0] I SCAN/BIST Mode Selection 37 LDO_SPI IO Decoupling cap for SPI LDO 38 SPI_PEN IO SPI LDO Ecoupling cap for SPI LDO 41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for Memory LDO 44 LDO_MEM IO Decoupling cap for Memory LDO	15	RX_IN	1	Input for RX		
18 BB_TEST_OUTIB O BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3 19 VDD_RF IO Decoupling Cap for Power for RF 20 VDD_3P3_RF P Power for RF 3.3V 21 ADC_ICM O Decoupling cap for ADC I common mode voltage 22 ADC_QCM O Decoupling cap for ADC Q common mode voltage 23 VDD_ADC IO Decoupling cap for ADC LDO 24 VDD_3P3_ADC P Power for ADC 3.3V 25 RSTn I Reset (Active Low) 26 SCLK I Serial Port Clock 27 SCS I Serial Port Chip Select (Active Low) 28 MOSI I Serial Port Master Out/Slave In 29 MISO IO Serial Port Master In/Slave Out 30 INTR IO MAC HW Interrupt (Active High) 31 IO_VDD P Power for IO interface 32 SFD_OUT O Test Point 0 33 TP[0] O Test Point 1 35 TEST_MODE[1] I SCAN/BIST Mode Selection	16	LNA_IN	1	LNA Input		
19VDD_RFIODecoupling Cap for Power for RF20VDD_3P3_RFPPower for RF 3.3V21ADC_I_CMODecoupling cap for ADC I common mode voltage22ADC_Q_CMODecoupling cap for ADC Q common mode voltage23VDD_ADCIODecoupling cap for ADC LDO24VDD_3P3_ADCPPower for ADC 3.3V25RSTnIReset (Active Low)26SCLKISerial Port Clock27SCSISerial Port Chip Select (Active Low)28MOSIISerial Port Master Out/Slave In29MISOIOSerial Port Master In/Slave Out30INTRIOMAC HW Interrupt (Active High)31IO_VDDPPower for IO interface32SFD_OUTOTest Point 034TP[1]OTest Point 135TEST_MODE[1]ISCAN/BIST Mode Selection36TEST_MODE[0]ISCAN/BIST Mode Selection37LDO_SPIIODecoupling cap for SPI LDO38SPI_PENIOSPI LDO Enable39VDD_3P3PPower for digital parts, XOSC40LDO_DIGIODecoupling cap for SPI LDO41LDO_MEMIODecoupling cap for Memory LDO42LDO_XOSCIODecoupling cap for XOSC LDO	17	BB_TEST_OUTI	0	BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3		
20	18	BB_TEST_OUTIB	0	BB test signal out for Mixer, VGA1, BPF,VGA2, VGA3		
21ADC_I_CMODecoupling cap for ADC I common mode voltage22ADC_Q_CMODecoupling cap for ADC Q common mode voltage23VDD_ADCIODecoupling cap for ADC LDO24VDD_3P3_ADCPPower for ADC 3.3V25RSTnIReset (Active Low)26SCLKISerial Port Clock27SCSISerial Port Chip Select (Active Low)28MOSIISerial Port Master Out/Slave In29MISOIOSerial Port Master In/Slave Out30INTRIOMAC HW Interrupt (Active High)31IO_VDDPPower for IO interface32SFD_OUTOTs/Rx SFD Signal33TP[0]OTest Point 034TP[1]OTest Point 135TEST_MODE[1]ISCAN/BIST Mode Selection36TEST_MODE[0]ISCAN/BIST Mode Selection37LDO_SPIIODecoupling cap for SPI LDO38SPI_PENIOSPI LDO Enable39VDD_3P3PPower for digital parts, XOSC40LDO_DIGIODecoupling cap for SPI LDO41LDO_MEMIODecoupling cap for Memory LDO42LDO_XOSCIODecoupling cap for XOSC LDO	19	VDD_RF	IO	Decoupling Cap for Power for RF		
ADC_Q_CM	20	VDD_3P3_RF	Р	Power for RF 3.3V		
VDD_ADC	21	ADC_I_CM	0	Decoupling cap for ADC I common mode voltage		
24VDD_3P3_ADCPPower for ADC 3.3V25RSTnIReset (Active Low)26SCLKISerial Port Clock27SCSISerial Port Chip Select (Active Low)28MOSIISerial Port Master Out/Slave In29MISOIOSerial Port Master In/Slave Out30INTRIOMAC HW Interrupt (Active High)31IO_VDDPPower for IO interface32SFD_OUTOTx/Rx SFD Signal33TP[0]OTest Point 034TP[1]OTest Point 135TEST_MODE[1]ISCAN/BIST Mode Selection36TEST_MODE[0]ISCAN/BIST Mode Selection37LDO_SPIIODecoupling cap for SPI LDO38SPI_PENIOSPI LDO Enable39VDD_3P3PPower for digital parts, XOSC40LDO_DIGIODecoupling cap for SPI LDO41LDO_MEMIODecoupling cap for Memory LDO42LDO_XOSCIODecoupling cap for XOSC LDO	22	ADC_Q_CM	0	Decoupling cap for ADC Q common mode voltage		
25 RSTn I Reset (Active Low) 26 SCLK I Serial Port Clock 27 SCS I Serial Port Chip Select (Active Low) 28 MOSI I Serial Port Master Out/Slave In 29 MISO IO Serial Port Master In/Slave Out 30 INTR IO MAC HW Interrupt (Active High) 31 IO_VDD P Power for IO interface 32 SFD_OUT O Tx/Rx SFD Signal 33 TP[0] O Test Point 0 34 TP[1] O Test Point 1 35 TEST_MODE[1] I SCAN/BIST Mode Selection 36 TEST_MODE[0] I SCAN/BIST Mode Selection 37 LDO_SPI IO Decoupling cap for SPI LDO 38 SPI_PEN IO SPI LDO Enable 39 VDD_3P3 P Power for digital parts, XOSC 40 LDO_DIG IO Decoupling cap for Memory LDO 41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for XOSC LDO	23	VDD_ADC	IO	Decoupling cap for ADC LDO		
26 SCLK I Serial Port Clock 27 SCS I Serial Port Chip Select (Active Low) 28 MOSI I Serial Port Master Out/Slave In 29 MISO IO Serial Port Master In/Slave Out 30 INTR IO MAC HW Interrupt (Active High) 31 IO_VDD P Power for IO interface 32 SFD_OUT O Tx/Rx SFD Signal 33 TP[0] O Test Point 0 34 TP[1] O Test Point 1 35 TEST_MODE[1] I SCAN/BIST Mode Selection 36 TEST_MODE[0] I SCAN/BIST Mode Selection 37 LDO_SPI IO Decoupling cap for SPI LDO 38 SPI_PEN IO SPI LDO Enable 39 VDD_3P3 P Power for digital parts, XOSC 40 LDO_DIG IO Decoupling cap for SPI LDO 41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for XOSC LDO	24	VDD_3P3_ADC	Р	Power for ADC 3.3V		
SCS I Serial Port Chip Select (Active Low)	25	RSTn	1	Reset (Active Low)		
MOSI I Serial Port Master Out/Slave In MISO IO Serial Port Master In/Slave Out MISO INTR IO MAC HW Interrupt (Active High) IO_VDD P Power for IO interface Tx/Rx SFD Signal TP[0] O Test Point 0 Test Point 1 SCAN/BIST Mode Selection TEST_MODE[1] I SCAN/BIST Mode Selection TEST_MODE[0] I SCAN/BIST Mode Selection SPI_DO_SPI IO Decoupling cap for SPI LDO SPI_DO_BODE VDD_3P3 P Power for digital parts, XOSC UDO_DIG IO Decoupling cap for SPI LDO LDO_MEM IO Decoupling cap for Memory LDO LDO_MEM IO Decoupling cap for Memory LDO Decoupling cap for Memory LDO Decoupling cap for XOSC LDO	26	SCLK	1	Serial Port Clock		
29 MISO IO Serial Port Master In/Slave Out 30 INTR IO MAC HW Interrupt (Active High) 31 IO_VDD P Power for IO interface 32 SFD_OUT O Tx/Rx SFD Signal 33 TP[0] O Test Point 0 34 TP[1] O Test Point 1 35 TEST_MODE[1] I SCAN/BIST Mode Selection 36 TEST_MODE[0] I SCAN/BIST Mode Selection 37 LDO_SPI IO Decoupling cap for SPI LDO 38 SPI_PEN IO SPI LDO Enable 39 VDD_3P3 P Power for digital parts, XOSC 40 LDO_DIG IO Decoupling cap for SPI LDO 41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for XOSC LDO	27	SCS	1	Serial Port Chip Select (Active Low)		
INTR IO MAC HW Interrupt (Active High)	28	MOSI	1	Serial Port Master Out/Slave In		
31 IO_VDD P Power for IO interface 32 SFD_OUT O Tx/Rx SFD Signal 33 TP[0] O Test Point 0 34 TP[1] O Test Point 1 35 TEST_MODE[1] I SCAN/BIST Mode Selection 36 TEST_MODE[0] I SCAN/BIST Mode Selection 37 LDO_SPI IO Decoupling cap for SPI LDO 38 SPI_PEN IO SPI LDO Enable 39 VDD_3P3 P Power for digital parts, XOSC 40 LDO_DIG IO Decoupling cap for SPI LDO 41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for XOSC LDO	29	MISO	IO	Serial Port Master In/Slave Out		
32 SFD_OUT O Tx/Rx SFD Signal 33 TP[0] O Test Point 0 34 TP[1] O Test Point 1 35 TEST_MODE[1] I SCAN/BIST Mode Selection 36 TEST_MODE[0] I SCAN/BIST Mode Selection 37 LDO_SPI IO Decoupling cap for SPI LDO 38 SPI_PEN IO SPI LDO Enable 39 VDD_3P3 P Power for digital parts, XOSC 40 LDO_DIG IO Decoupling cap for SPI LDO 41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for XOSC LDO	30	INTR	IO	MAC HW Interrupt (Active High)		
Test Point 0 Test Point 1 Test Point 1 Test Point 1 SCAN/BIST Mode Selection TEST_MODE[1] I SCAN/BIST Mode Selection TEST_MODE[0] I SCAN/BIST Mode Selection LDO_SPI IO Decoupling cap for SPI LDO SPI LDO Enable VDD_3P3 P Power for digital parts, XOSC LDO_DIG IO Decoupling cap for SPI LDO LDO_MEM IO Decoupling cap for Memory LDO LDO_XOSC IO Decoupling cap for XOSC LDO	31	IO_VDD	Р	Power for IO interface		
Test Point 1 Test Point 1 Test Point 1 Test Point 1 SCAN/BIST Mode Selection TEST_MODE[0] I SCAN/BIST Mode Selection TEST_MODE[0] I SCAN/BIST Mode Selection Decoupling cap for SPI LDO SPI LDO Enable Power for digital parts, XOSC LDO_DIG IO Decoupling cap for SPI LDO LDO_MEM IO Decoupling cap for Memory LDO LDO_XOSC IO Decoupling cap for XOSC LDO	32	SFD_OUT	0	Tx/Rx SFD Signal		
35 TEST_MODE[1] I SCAN/BIST Mode Selection 36 TEST_MODE[0] I SCAN/BIST Mode Selection 37 LDO_SPI IO Decoupling cap for SPI LDO 38 SPI_PEN IO SPI LDO Enable 39 VDD_3P3 P Power for digital parts, XOSC 40 LDO_DIG IO Decoupling cap for SPI LDO 41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for XOSC LDO	33	TP[0]	0	Test Point 0		
36TEST_MODE[0]ISCAN/BIST Mode Selection37LDO_SPIIODecoupling cap for SPI LDO38SPI_PENIOSPI LDO Enable39VDD_3P3PPower for digital parts, XOSC40LDO_DIGIODecoupling cap for SPI LDO41LDO_MEMIODecoupling cap for Memory LDO42LDO_XOSCIODecoupling cap for XOSC LDO	34	TP[1]	0	Test Point 1		
37LDO_SPIIODecoupling cap for SPI LDO38SPI_PENIOSPI LDO Enable39VDD_3P3PPower for digital parts, XOSC40LDO_DIGIODecoupling cap for SPI LDO41LDO_MEMIODecoupling cap for Memory LDO42LDO_XOSCIODecoupling cap for XOSC LDO	35	TEST_MODE[1]	1	SCAN/BIST Mode Selection		
38SPI_PENIOSPI LDO Enable39VDD_3P3PPower for digital parts, XOSC40LDO_DIGIODecoupling cap for SPI LDO41LDO_MEMIODecoupling cap for Memory LDO42LDO_XOSCIODecoupling cap for XOSC LDO	36	TEST_MODE[0]	1	SCAN/BIST Mode Selection		
39 VDD_3P3 P Power for digital parts, XOSC 40 LDO_DIG IO Decoupling cap for SPI LDO 41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for XOSC LDO	37	LDO_SPI	Ю	Decoupling cap for SPI LDO		
40 LDO_DIG IO Decoupling cap for SPI LDO 41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for XOSC LDO	38	SPI_PEN	Ю	SPI LDO Enable		
41 LDO_MEM IO Decoupling cap for Memory LDO 42 LDO_XOSC IO Decoupling cap for XOSC LDO	39	VDD_3P3	Р	Power for digital parts, XOSC		
42 LDO_XOSC IO Decoupling cap for XOSC LDO	40	LDO_DIG	IO	Decoupling cap for SPI LDO		
	41	LDO_MEM	IO	Decoupling cap for Memory LDO		
43 OSCO IO Crystal driver	42	LDO_XOSC	IO	Decoupling cap for XOSC LDO		
	43	OSCO	IO	Crystal driver		



44	OSCI	Ю	Crystal driver	
45	VDD_3P3_BBA	Р	Power for BBA 3.3V	
46	VDD_BBA	Ю	Decoupling cap for BBA LDO	
47	VDD_3P3_BBA	Р	Power for BBA 3.3V	
48	VDD_PLL_DIG	Ю	Decoupling cap for PLL digital parts	

^{*}Signal type definition (I: Input, O: Output, IO: Input Output, P: Power)

3 Specification

3.1 General Characteristics

PARAMETER	MIN	TYP.	MAX	UNIT	CONDITION
Frequency Range	902		928	MHz	NA-ISM, KOREA RFID/USN
Frequency Resolution		5.7		Hz	
Data rate	12.5		200	kbps	GFSK/2FSK(12.5/25/50/150/200)

3.2 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT	CONDITION
Supply Voltage	-0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	-0.3	3.9	V	
Voltage on the pins(RF Port)	-0.3	3.9	V	
Input RF Level		+10	dBm	

3.3 Handling Ratings

PARAMETER		MIN	MAX	UNIT
Storage temperature range, Tstg	(Default)	-40	125	$^{\circ}$
Valtage on any digital nin	Human Body Model(HBM)	-2	2	kV
Voltage on any digital pin	Machine Model (MM)	-200	200	V

3.4 Recommended Operation Conditions

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Voltage supply range	2.7		3.6	V	All supply pins must have the same voltage
Voltage on digital inputs	0		VDD	V	VDD=3.3V
Temperature range	-40		85	°C	

3.5 Current Consumption

 T_A =25°C, VDD=3.3V, fc= 920.1 MHz, if nothing else stated. All measurement results are obtained using user guide of AXR100.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
PHY SLEEP MODE		8.0		mA	
DEEP SLEEP MODE		-		mA	SPI
SLEEP MODE		-		mA	SPI, Memory, XOSC
IDLE MODE		-		mA	SPI, Memory, XOSC, Digital Core



READY MODE	19.5	mA	SPI, Memory, XOSC, Digital Core, PLL
			SPI, Memory, XOSC, Digital Core, PLL,
RX MODE	32.3	mA	RX
			(In wait state for packet reception)
			SPI, Memory, XOSC, Digital Core, PLL,
TX MODE	20.6	mA	TX (In wait state for packet
			transmission)

3.6 Tx Current Consumption

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX Current Consumption		20.6		mA	In wait state for packet transmission
TX Current Consumption @		F.C. 4		mΛ	At maximum transmit nower
+13.5 dBm		56.1		mA	At maximum transmit power
DA_CONT : 0x3074 [31:28]					
= [1111],					
DA_LDO : 0x3D28 [25:22]					
=[1111]					
TX Current Consumption @		445		Λ	DA CONT. 0.2074 [21.20] [1111]
+10 dBm		44.5		mA	DA_CONT : 0x3074 [31:28] = [1111],

3.7 RX Current Consumption

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
RX Current		32.3		mA	In wait state for packet reception
RX Peak Current	32.5	325		mA	Peak current consumption during
		32.3			packet reception at the sensitivity level.

3.8 RF Receive Section

TA = 25°C, VDD = 3.3 V, fc = 920.1 MHz, if nothing else stated. All RX measurements are made at the antenna connector, to a packet error rate (PER) limit of 10% with 250 bytes of packet length. Selectivity and blocking are measured with input power of desired signal 3dB greater than the sensitivity level of IEEE 802.15.4g/k standard.

3.8.1 General Receive Parameters

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Saturation		+10		dBm	RF frequency = 920.1 MHz
Channel Filter	00		200	1.11=	
Programmable Bandwidth	90		200	kHz	
IIP3 (LNA and Mixer)		-16.4		dBm	At maximum gain



			11		dBm	At minimum gain
D1 dD (LNIA and Missar)			-25	25 dBm At maximum gain		At maximum gain
PIUD (LINA and IVIIX	P1dB (LNA and Mixer)		2		dBm	At Minimum gain
	< 1GHz		-63		dBm	
Spurious Emission > 1GHz			-58		dBm	
Optimum Source Impedance			52-j16		Ω	RF_freq=920.1 MHz

3.8.2 Receive Performance in 920.1 MHz bands

Parameter	Min	Тур	Max	Units	Condition			
		-105		dBm	12.5kbps, 2-GFSK, DEV= 12.5 KHz, CHF= 100 KHz			
		-103		dBm	25kbps, 2-GFSK, DEV= 12.5 KHz, CHF= 100 KHz			
Sensitivity		-101		dBm	50kbps, 2-GFSK, DEV= 25KHz, CHF= 100KHz			
		-93		dBm	150kbps, 2-GFSK, DEV= 37.5KHz, CHF= 165KHz			
		-92		dBm	200kbps, 2-GFSK, DEV= 50KHz, CHF= 200KHz			
		33		dB	CW Interferer, - 200 kHz (adjacent channel)			
		33		dB	CW Interferer, + 200 kHz (adjacent channel)			
		40		dB	CW Interferer,- 400 kHz (alternate channel)			
		42		dB	CW Interferer, + 400 kHz (alternate channel)			
Selectivity and		33		dB	Modulated Interferer, - 200 kHz (adjacent channel)			
Blocking		33		dB	Modulated Interferer, + 200 kHz (adjacent channel)			
12.5 July 2.050V		40		dB	Modulated Interferer, - 400 kHz (alternate channel)			
12.5 kbps, 2-GFSK, 12.5 kHz deviation,		42		dB	Modulated Interferer, + 400 kHz (alternate channel)			
100 kHz channel		51		dB	CW Interferer, ± 1 MHz			
ilter		52		dB	CW Interferer, ± 2 MHz			
		71		dB	CW Interferer, ± 10 MHz			
		51		dB	Modulated Interferer, ± 1MHz			
		52		dB	Modulated Interferer, ± 2MHz			
		71		dB	Modulated Interferer, ± 10 MHz			
		31		dB	CW Interferer, - 200 kHz (adjacent channel)			
Selectivity and		31		dB	CW Interferer, + 200 kHz (adjacent channel)			
Blocking		38		dB	CW Interferer,- 400 kHz (alternate channel)			
3		40		dB	CW Interferer, + 400 kHz (alternate channel)			
25 kbps, 2-GFSK,		31		dB	Modulated Interferer, - 200 kHz (adjacent channel)			
12.5 kHz deviation,		31		dB	Modulated Interferer, + 200 kHz (adjacent channel)			
100 kHz channel		38		dB	Modulated Interferer, - 400 kHz (alternate channel)			
filter		40		dB	Modulated Interferer, + 400 kHz (alternate channel)			
		49		dB	CW Interferer, ± 1 MHz			

	50	dB	CW Interferer, ± 2 MHz				
	69	dB	CW Interferer, ± 10 MHz				
	49	dB	Modulated Interferer, ± 1MHz				
	50	dB	Modulated Interferer, ± 2MHz				
	69	dB	Modulated Interferer, ± 10 MHz				
	30	dB	CW Interferer, - 200 kHz (adjacent channel)				
	30	dB	CW Interferer, + 200 kHz (adjacent channel)				
	36	dB	CW Interferer,- 400 kHz (alternate channel)				
Selectivity and	37	dB	CW Interferer, + 400 kHz (alternate channel)				
Blocking	29	dB	Modulated Interferer, - 200 kHz (adjacent channel)				
	29	dB	Modulated Interferer, + 200 kHz (adjacent channel)				
50 kbps, 2-GFSK, 25	35	dB	Modulated Interferer, - 400 kHz (alternate channel)				
kHz deviation, 100 —— kHz channel filter ——	36	dB	Modulated Interferer, + 400 kHz (alternate channel)				
(Same modulation	46	dB	CW Interferer, ± 1 MHz				
format as 802.15.4g	48	dB	CW Interferer, ± 2 MHz				
Mandatory Mode)	66	dB	CW Interferer, ± 10 MHz				
	46	dB	Modulated Interferer, ± 1MHz				
	48	dB	Modulated Interferer, ± 2MHz				
	66	dB	Modulated Interferer, ± 10 MHz				
	16	dB	CW Interferer, - 400 kHz (adjacent channel)				
	21	dB	CW Interferer, + 400 kHz (adjacent channel)				
	32	dB	CW Interferer,- 800 kHz (alternate channel)				
	35	dB	CW Interferer, + 800 kHz (alternate channel)				
Selectivity and	16	dB	Modulated Interferer, - 400 kHz (adjacent channel)				
Blocking	21	dB	Modulated Interferer, + 400 kHz (adjacent channel)				
	31	dB	Modulated Interferer, - 800 kHz (alternate channel)				
150 kbps, 2-GFSK, —	35	dB	Modulated Interferer, + 800 kHz (alternate channel)				
37.5 kHz deviation, ————————————————————————————————————	33	dB	CW Interferer, ± 1 MHz				
filter	34	dB	CW Interferer, ± 2 MHz				
	59	dB	CW Interferer, ± 10 MHz				
	33	dB	Modulated Interferer, ± 1MHz				
	34	dB	Modulated Interferer, ± 2MHz				
	59	dB	Modulated Interferer, ± 10 MHz				
Selectivity and		dB	CW Interferer, - 400 kHz (adjacent channel)				
Blocking	-	dB	CW Interferer, + 400 kHz (adjacent channel)				
	_	dB	CW Interferer, + 400 kHz (adjacent channel)				
200 kbps, 2-GFSK,	_	dB	CW Interferer, + 800 kHz (alternate channel)				
-		G D	a.r. merierary . 300 km² (arternate charmer)				



50 kHz deviation,	-	dB	Modulated Interferer, - 400 kHz (adjacent channel)				
200 kHz channel	-	dB	Modulated Interferer, + 400 kHz (adjacent channel)				
filter	-	dB	Modulated Interferer, - 800 kHz (alternate channel)				
	-	dB	Modulated Interferer, + 800 kHz (alternate channel)				
	-	dB	CW Interferer, ± 1 MHz s				
	-	dB	CW Interferer, ± 2 MHz				
	-	dB	dB CW Interferer, ± 10 MHz				
	-	dB	Modulated Interferer, ± 1MHz				
	-	dB	Modulated Interferer, ± 2MHz				
	-	dB	Modulated Interferer, ± 10 MHz				
			Measured as image attenuation at the IF filter				
Image Channel	25	dB	output, carrier wave interferer at 500 kHz below the				
Attenuation			channel frequency, 100 kHz IF filter bandwidth				

3.9 RF Transmit Section

TA = 25°C, VDD = 3.3 V, fc = 920.1 MHz, if nothing else stated. All TX measurements are made at the antenna connector. Adjacent channel leakage ratio (ACLR) is measured when transmitter outputs +10 dBm of signal power.

3.9.1 General Transmit Parameters

Parameter	Тур	Units	Condition
Max. Output Power	13.5	dBm	RF freq = 920.1 MHz,
Min. Output Power	-33.5	dBm	RF freq = 920.1 MHz
Output Power Step Size	0.5	dB	Within fine step size range
Clock-Related Spur Level	-52	dBc	TX output power = +10 dBm,
	-32	UBC	Clock freq=24 MHz
Spurious Emissions			
(Excluding harmonics)			
< 1GHz	-55	dBm	TX output power = +10 dBm,
> 1GHz	-52	dBm	
Harmonics			
Second Harmonic	-37.9	dBm	TV output nower - 110 dPm
Third Harmonic	-51.5	dBm	TX output power = +10 dBm,
Fourth Harmonic	-49.3	dBm	
Optimum Load Impedance	25+j4	Ω	RF_freq=920.1 MHz

3.9.2 Adjacent Channel Leakage Ratio

Parameter	Тур	Units	Condition	

ACLR	-36.0	dBc	- 200 kHz (adjacent channel)
(12.5kbps, 2-GFSK, 12.5 KHz deviation,	-36.0	dBc	+ 200 kHz (adjacent channel)
200-kHz channel BW)	-45.4	dBc	- 400 kHz (alternate channel)
	-45.4	dBc	+ 400 kHz (alternate channel)
ACLR	-36.7	dBc	- 200 kHz (adjacent channel)
(25kbps, 2-GFSK, 12.5 KHz deviation,	-36.6	dBc	+ 200 kHz (adjacent channel)
200-kHz channel BW)	-45.2	dBc	- 400 kHz (alternate channel)
	-45.6	dBc	+ 400 kHz (alternate channel)
ACLR	-37.0	dBc	- 200 kHz (adjacent channel)
(50kbps, 2-GFSK, 25 KHz deviation,	-37.1	dBc	+ 200 kHz (adjacent channel)
200-kHz channel BW)	-45.6	dBc	- 400 kHz (alternate channel)
	-45.5	dBc	+ 400 kHz (alternate channel)
ACLR	-36.2	dBc	- 400 kHz (adjacent channel)
(150kbps, 2-GFSK, 37.5 KHz deviation,	-36.3	dBc	+ 400 kHz (alternate channel)
400-kHz channel BW)	-45.3	dBc	- 800 kHz (alternate channel)
	-45.5	dBc	+ 800 kHz (alternate channel)
ACLR	-34.8	dBc	- 400 kHz (adjacent channel)
(200kbps, 2-GFSK, 50 KHz deviation,	-34.9	dBc	+ 400 kHz (adjacent channel)
400-kHz channel BW)	-45.8	dBc	- 800 kHz (alternate channel)
	-45.5	dBc	+ 800 kHz (alternate channel)

3.10 Crystal Oscillator

T_A=25°C, VDD=3.3V if nothing else stated. All measurement results are obtained using user guide

Parameter	Min	Тур.	Max	Units	Condition
Crystal frequency		24		MHz	
Load Capacitance (CL)		17		pF	
ESR			80	Ω	
Start-up time		5		ms	Excluding LDO settling time

3.11 PLL Characteristics

TA = 25°C, VDD = 3.3 V, fc = 920.1 MHz if nothing else stated

Parameter	Тур	Units	Condition
	-79	dBc/Hz	± 1KHz offset
Phase Noise in 920.1 MHz Bands	-84	dBc/Hz	± 10KHz offset
100-KHz Loop Bandwidth setting	-89	dBc/Hz	± 100KHz offset
	-108	dBc/Hz	± 1MHz offset



	-134	dBc/Hz	± 10MHz offset
	-80	dBc/Hz	± 1KHz offset
Phase Noise in 920.1 MHz Bands	-85	dBc/Hz	± 10KHz offset
300-KHz Loop Bandwidth setting	-92	dBc/Hz	± 100KHz offset
300-KHZ LOOP Bandwidth Setting	-102	dBc/Hz	± 1MHz offset
	-132	dBc/Hz	± 10MHz offset
Frequency resolution	5.7	Hz	

3.12 Wake-up and Timing

TA = 25°C, VDD = 3.3 V, fc = 920.1 MHz if nothing else stated.

The turnaround behavior to and from RX and/or TX is highly configurable, and the time it takes will depend on how the device is set up.

now the device is set up.						
Parameter	Тур	Units	Condition			
PHY SLEEP to DEEP Sleep	6	ms	SPI ON			
DEEP SLEEP to SLEEP	5	ms	DEEP SLEEP + XOSC + Register			
SLEEP to IDLE	450	us	SLEEP + Digital Core			
IDLE to READY	470	us	IDEL+PLL/Calibration disabled			
IDLE TO READY	500	us	IDEL+PLL/Calibration enabled			
IDLE to RX	450	us				
IDLE to TX	450	us				
RX to IDLE	0	us				
TX to IDLE	0	us				
Minimum required number of	1.5	Dutos	ACC gottling time			
preamble bytes	1.5	Bytes	AGC settling time			
Time from start RX until valid						
RSSI Including gain settling						
(function of channel	260		AGC settling time + 1 symbol timing, 50kbps			
bandwidth. Programmable for	260	ms	mode			
trade-off between speed and						
accuracy)						

3.13 I/O and Reset

TA = 25°C, VDD = 3.3 V, fc = 920.1 MHz if nothing else stated

Parameter	Min	Тур	Max	Unit	Condition
Logic Input High Voltage	0.8*VDD			V	
Logic Input Low Voltage			0.2*VDD	V	
Logic Output High Voltage	0.8*VDD			V	



Logic Output Low Voltage		0.2*VDD	V	

4 Typical Performance characteristics

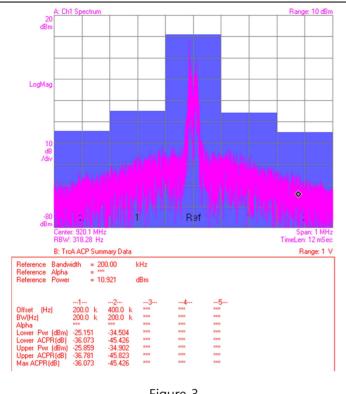


Figure 3

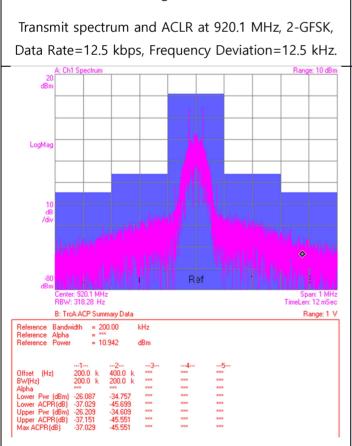


Figure 5

Transmit spectrum and ACLR at 920.1 MHz, 2-GFSK, Data Rate=50 kbps, Frequency Deviation=25 kHz.

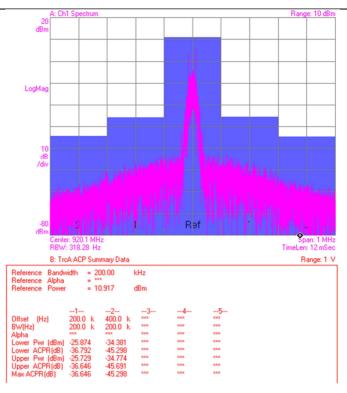


Figure 4

Transmit spectrum and ACLR at 920.1 MHz, 2-GFSK, Data Rate=25 kbps, Frequency Deviation=12.5 kHz.

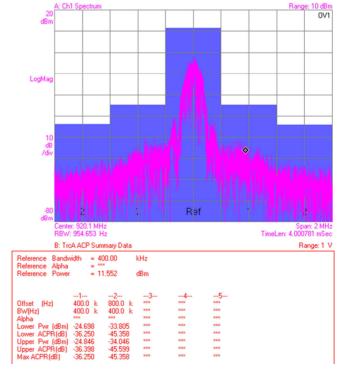
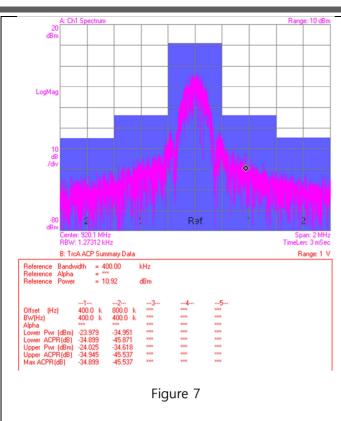
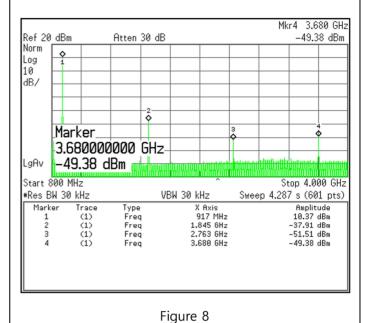


Figure 6

Transmit spectrum and ACLR at 920.1 MHz, 2-GFSK, Data Rate=150 kbps, Frequency Deviation=37.5 kHz.







Transmit spectrum and ACLR at 920.1 MHz, 2-GFSK, Data Rate=200 kbps, Frequency Deviation=50 kHz.

Transmitter Output Signal Spectrum with Harmonics.

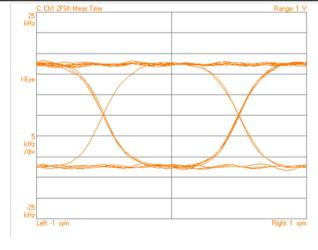


Figure 9

Transmit Eye at 920.1 MHz, 2-GFSK, Data Rate=12.5 kbps, Frequency Deviation=12.5 kHz.

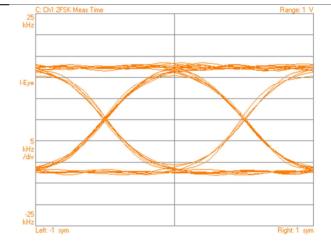


Figure 10

Transmit Eye at 920.1 MHz, 2-GFSK, Data Rate=25 kbps, Frequency Deviation=12.5 kHz.

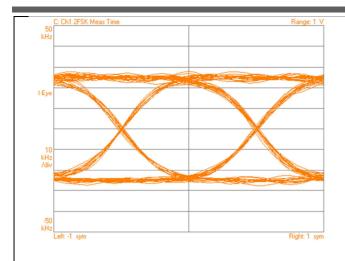


Figure 11

Figure 5-9. Transmit Eye at 920.1 MHz, 2-GFSK, Data Rate=50 kbps, Frequency Deviation=12.5 kHz.

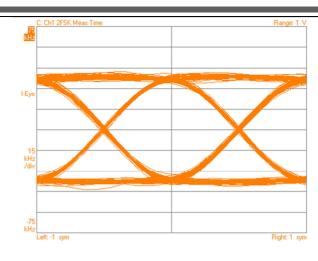


Figure 12

Figure 5-10. Transmit Eye at 920.1 MHz, 2-GFSK, Data Rate=150 kbps, Frequency Deviation=37.5 kHz.

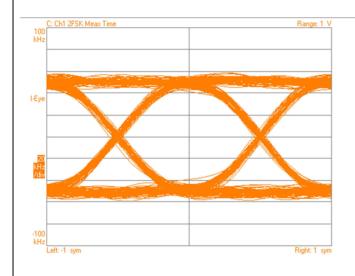


Figure 13

Transmit Eye at 920.1 MHz, 2-GFSK,
Data Rate=200 kbps, Frequency Deviation=50 kHz.

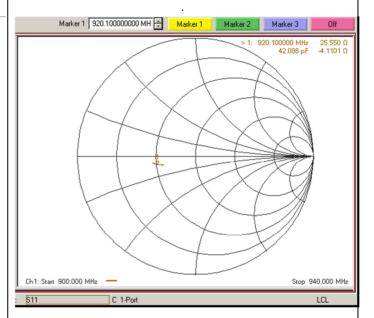


Figure 14

Transmitter Output Impedance at 920.1 MHz.

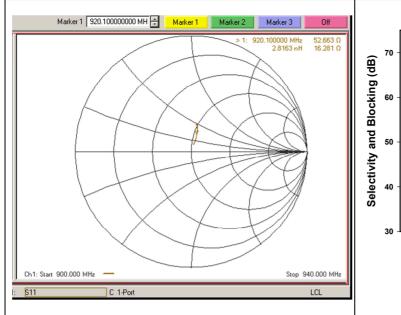


Figure 15

Receiver Input Impedance at 920.1 MHz.

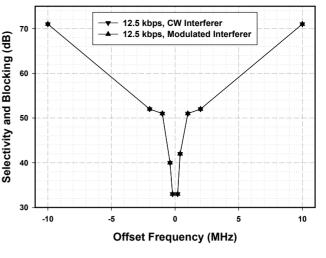


Figure 16

Selectivity and Blocking vs Offset Frequency (Data Rate=12.5 kbps, Frequency Deviation=12.5 kHz, IF=250 kHz, Channel Filter BW = 100 kHz)

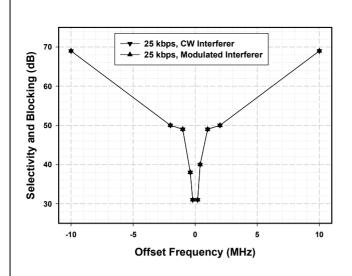


Figure 17

Selectivity and Blocking vs Offset Frequency (Data Rate=25 kbps, Frequency Deviation=12.5 kHz, IF=250 kHz, Channel Filter BW = 100 kHz)

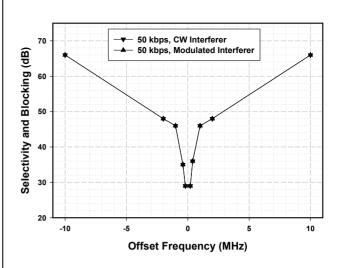


Figure 18

Selectivity and Blocking vs Offset Frequency (Data Rate=50 kbps, Frequency Deviation=25 kHz, IF=250 kHz, Channel Filter BW = 100 kHz)

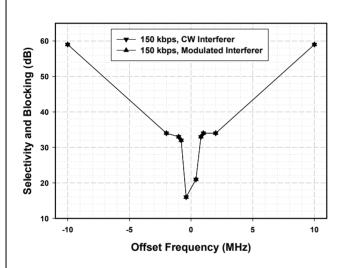


Figure 19

Selectivity and Blocking vs Offset Frequency (Data Rate=150 kbps, Frequency Deviation=37.5 kHz, IF=250 kHz, Channel Filter BW = 165 kHz)

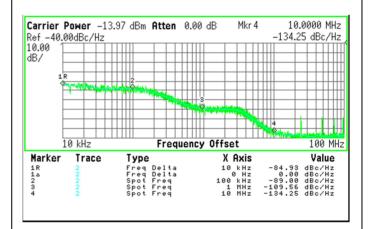


Figure 20

Phase Noise in 920.1 MHz Bands 100-KHz loop Bandwidth

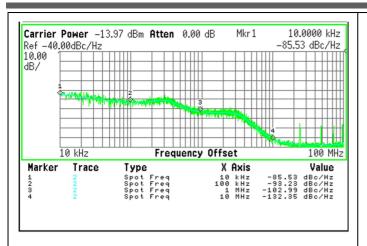


Figure 21

Phase Noise in 920.1 MHz Bands 300-KHz loop Bandwidth