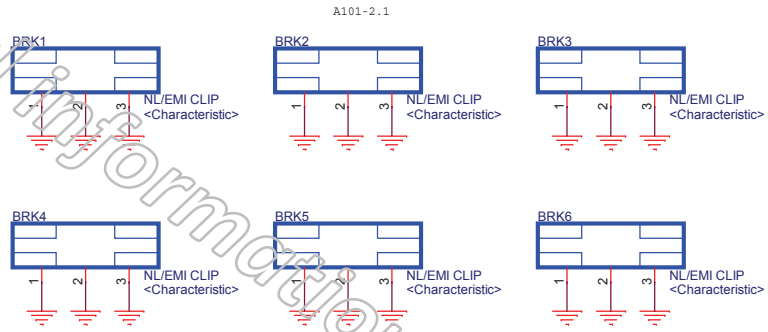
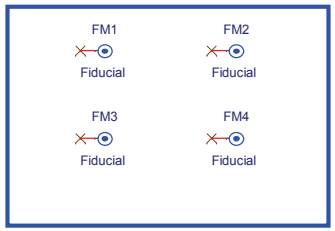
WISE-1530
A101-2





#IP ID	ADVANTECH	
Title	Title Page	
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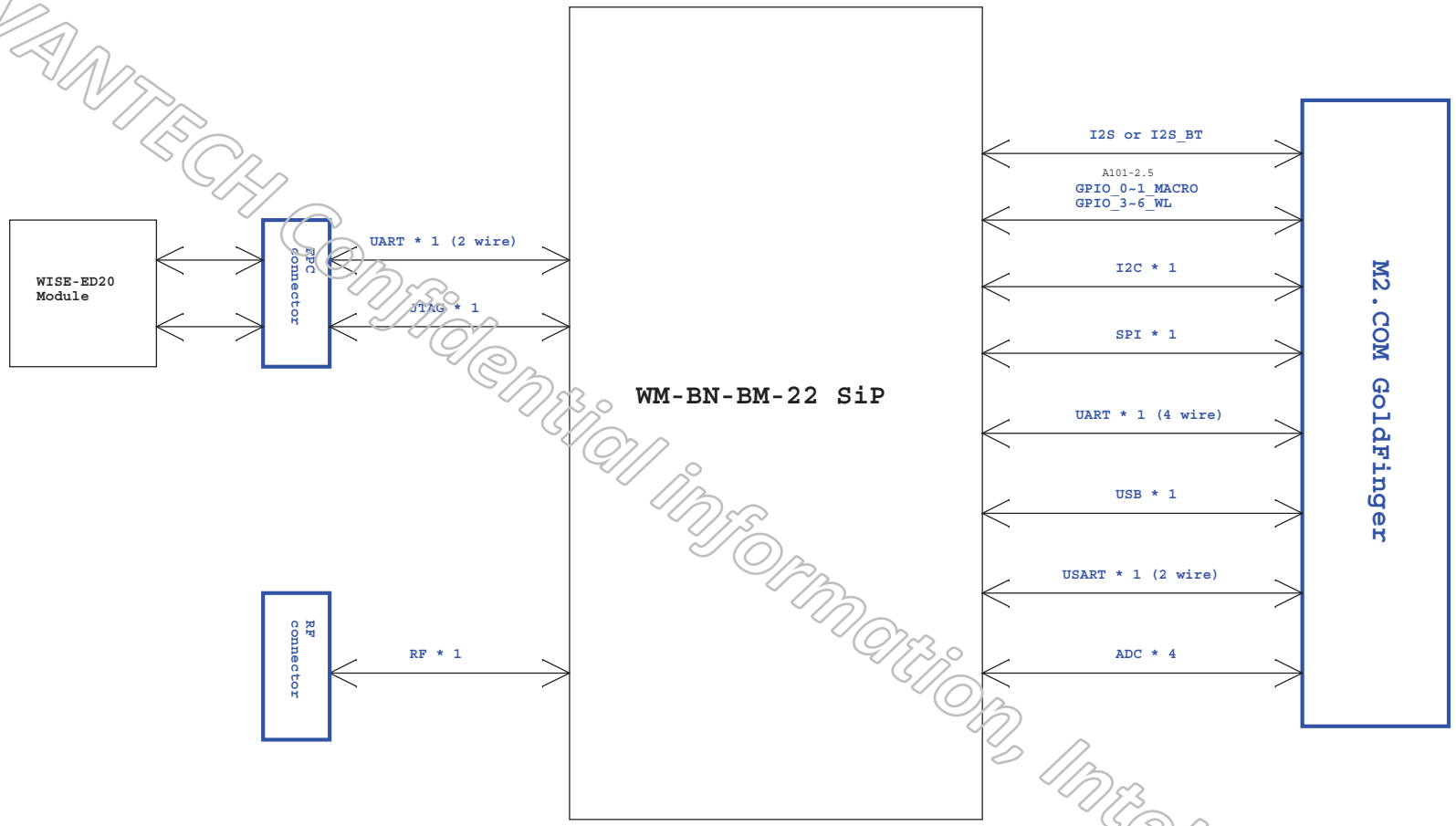
WISE-1530 A101-2 Block Diagram



Title	SYSTEM BLOCK DIAG.	
Size	Document Number WISE-1530	Rev A101-2
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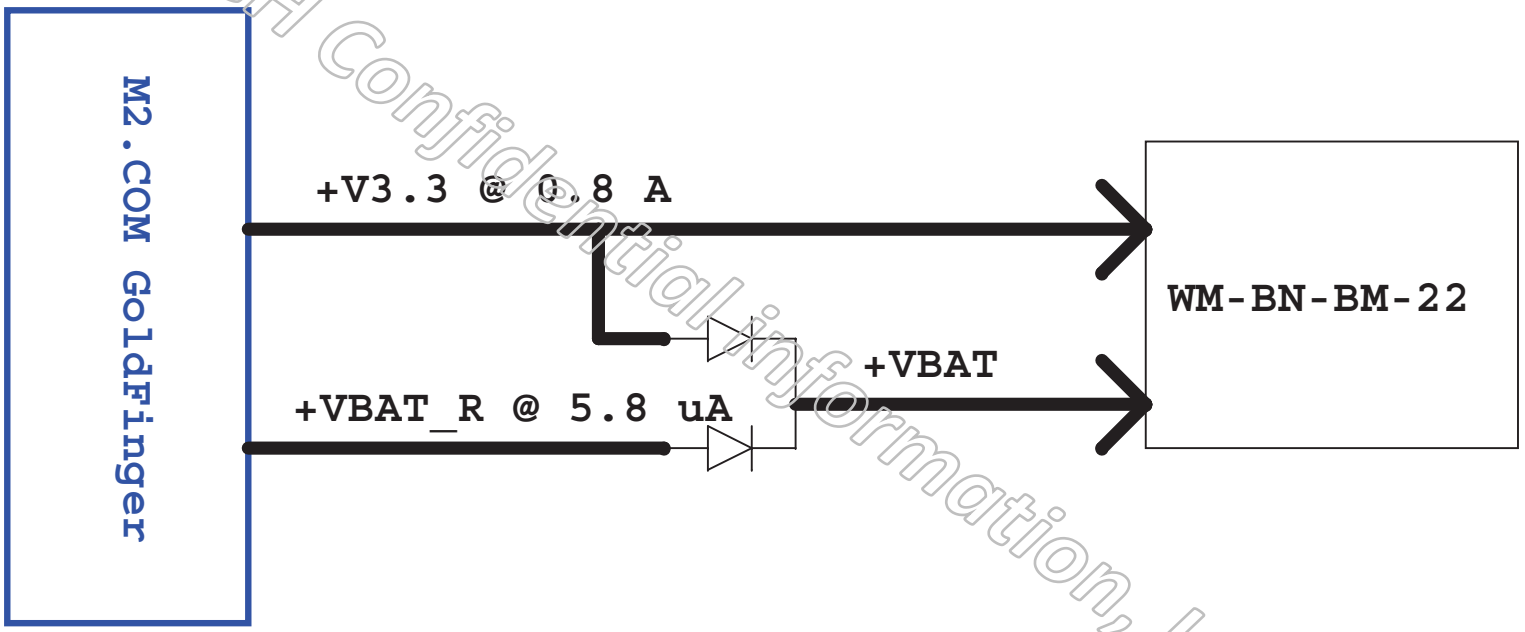

ADVANTECH		
Title	POWER BLOCK DIAG.	
Size	Document Number WISE-1530	Rev A101-2
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Title	POWER ON SEQ.	
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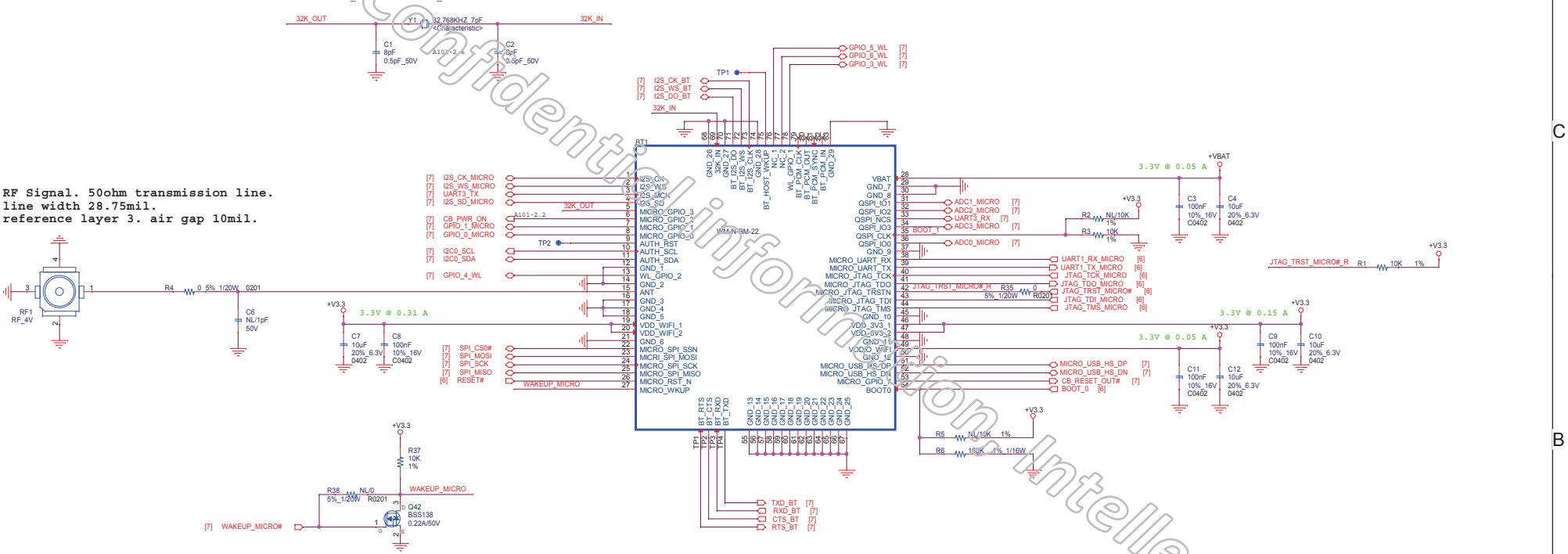
ST vendor recommended XTAL 7pF

GPIO_3 could be RTC_OUT for 32.768K XTAL

RF Signal. 50ohm transmission line.
line width 28.75mil.
reference layer 3. air gap 10mil.



Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as the boot space
0	1	System memory	System memory is selected as the boot space
1	1	Embedded SRAM	Embedded SRAM is selected as the boot space

ADVANTECH			
Title	WM-BN-BM-22		
Size	Document Number	WISE-1530	Rev A101-2
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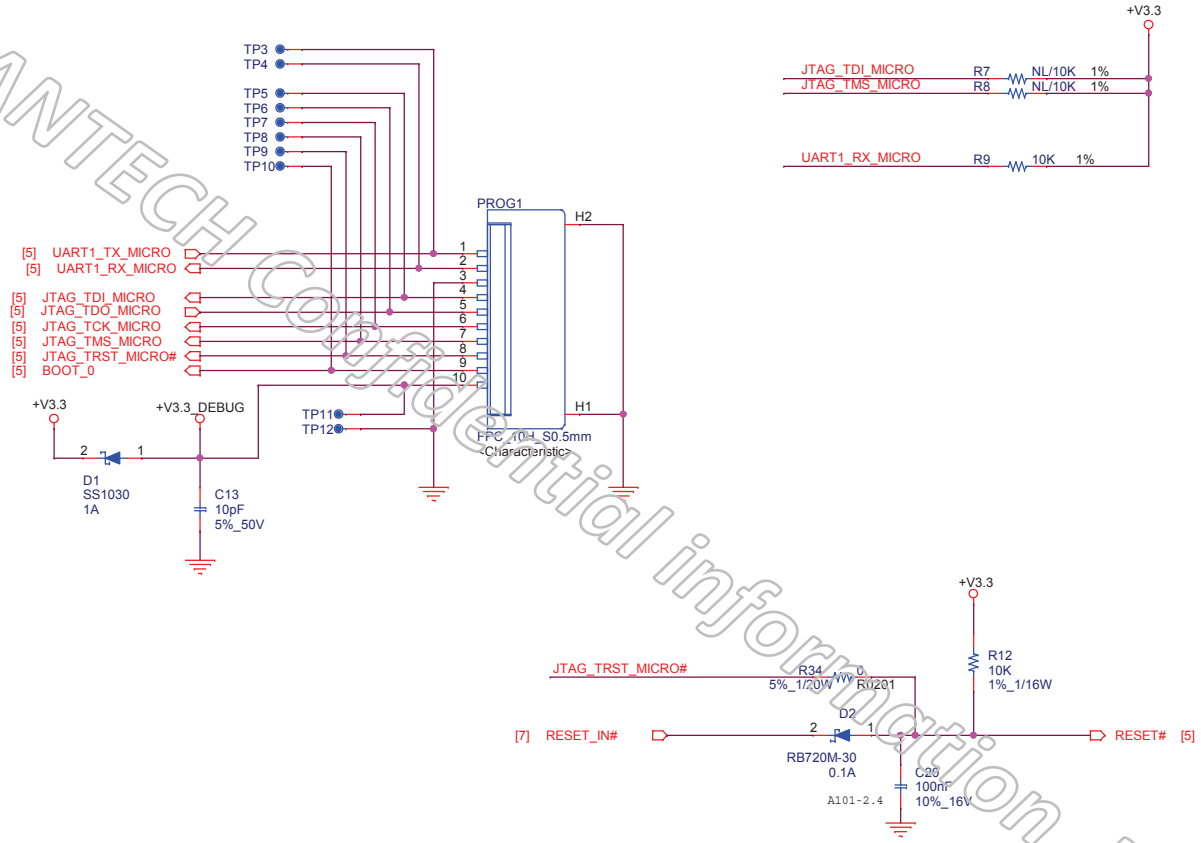
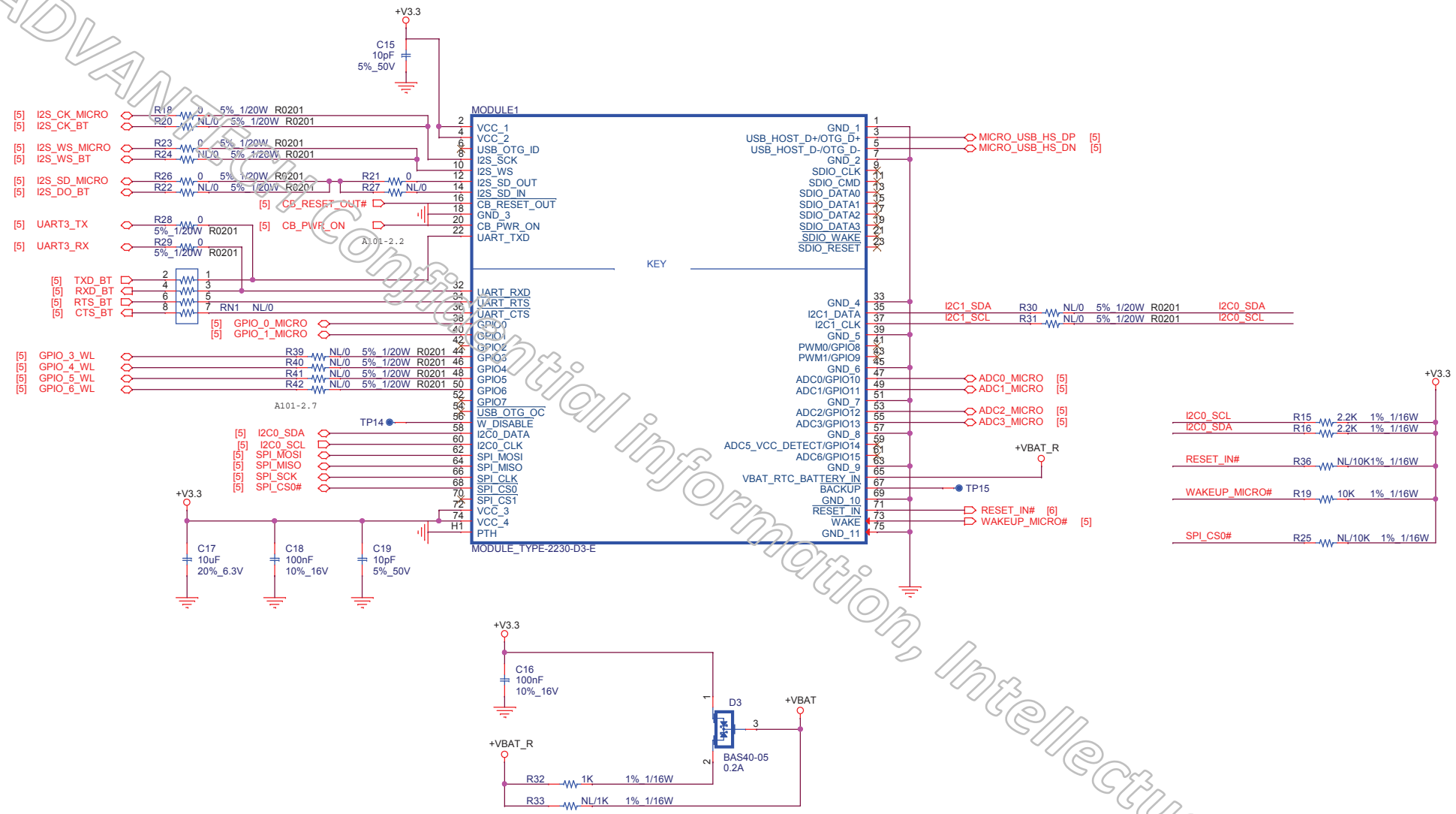


ADVANTECH		
Title	JTAG	
Size	Document Number WISE-1530	Rev A101-2
Date: Monday, April 24, 2017	Sheet 6 of 9	



Title	ADVANTECH M2.COM	
Size	Document Number WISE-1530	Rev A101-2
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USI / WM-BN-BM-22		STM32F412RG (LQFP64)						WISE-1530 Configuration		
Pin-No	Symbol	Pin-No	Pin Name (Funtion After Reset)	Pin Type	I/O Structure	Alternate Function	Additional Function	M2.COM Pin-No	S/W Prog.	Signal Name
1	I2S_CK	33	G3(PB12)	I/O	FT	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, SPI4_NSS/I2S4_WS, SPI3_SCK/I2S3_CK, USART3_CK, CAN2_RX, DFSDM1_DATIN1, FSMC_D13/FSMC_DA13, EVENTOUT	-	8	I2S3_CK	I2S_CK_MICRO
2	I2S_WS	23	G6(PA4)	I/O	FT	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, DFSDM1_DATIN1, FSMC_D6, EVENTOUT	ADC1_4	10	I2S3_WS	I2S_WS_MICRO
3	I2S_MCK	29	H4(PB10)	I/O	FT	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, I2S3_MCK, USART3_TX, I2CFMP1_SCL, SDIO_D7, EVENTOUT	-	22 (Option)	USART3_TX	USART_TX
4	I2S_SD	53	A3(PG12)	I/O	FT	SPI3_MOSI/I2S3_SD, USART3_CK, FSMC_D3, SDIO_CK, EVENTOUT	-	12	I2S3_SD	I2S_SD_MICRO
5	MICRO_GPIO_3	4	C7(PC15)	I/O	FT	EVENTOUT	OSC32_OUT	--	--	32K_OUT
6	MICRO_GPIO_2	27	F4(PB1)	I/O	FT	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, SPI5_NSS/I2S5_WS, DFSDM1_DATIN0, QUADSPI_CLK, EVENTOUT	ADC1_9	20	CB_PWR_ON	CB_PWR_ON
7	MICRO_GPIO_1	26	H5(PB0)	I/O	FT	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI5_SCK/I2S5_CK, EVENTOUT	ADC1_8	40	GPIO	GPIO_1_MICRO
8	MICRO_GPIO_0	21	F5(PA5)	I/O	FT	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, DFSDM1_CKIN1, FSMC_D7, EVENTOUT	ADC1_5	38	GPIO	GPIO_0_MICRO
9	AUTH_RST	2	B8(PC13)	I/O	FT	EVENTOUT	TAMP_1	--	--	--
10	AUTH_SCL	58	B5(PB6)	I/O	FT	TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, SDIO_D5, EVENTOUT	-	60	I2C0_SCL	I2C0_SCL
11	AUTH_SDA	59	A6(PB7)	I/O	FT	TIM4_CH2, I2C1_SDA, USART1_RX, FSMC_NL, EVENTOUT	-	58	I2C1_SDA	I2C0_SDA
12	GND		----------					GND		
13	RF_SW_CTRL		----------					46		GPIO_4_WL
14	GND		----------					GND		GND
15	ANT		----------							
16	GND		----------					GND		GND
17	GND		----------					GND		GND
18	GND		----------					GND		GND
19	VDD_WIFI		----------					VCC		+V3.3
20	VDD_WIFI		----------					VCC		+V3.3
21	GND		----------					GND		GND
22	MICRO_SPI_SSN	62	B6(PB9)	I/O	FT	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, I2C2_SDA, SDIO_D5, EVENTOUT	-	68	SPI2_NSS	SPI_CS0#
23	MICR1_SPI_MOSI	11	D6(PC3)	I/O	FT	SPI2_MOSI/I2S2_SD, FSMC_A0, EVENTOUT	ADC1_13	62	SPI2_MOSI	SPI_MOSI
24	MICRO_SPI_SCK	34	G2(PB13)	I/O	FT	TIM1_CH1N, I2CFMP1_SMBA, SPI2_SCK/I2S2_CK, SPI4_SCK/I2S4_CK, USART3_CTS, CAN2_TX, DFSDM1_CKIN1, EVENTOUT	-	66	SPI2_SCK	SPI_SCK
25	MICRO_SPI_MISO	10	E7(PC2)	I/O	FT	SPI2_MISO, I2S2ext_SD, DFSDM1_CKOUT, FSMC_NWE, EVENTOUT	ADC1_12	64	SPI2_MISO	SPI_MISO
26	MICRO_RST_N	7	D7	I/O	RST	-	NRST	71	NRST	RESET#
27	MICRO_WKUP	8	D5(PC0)	I/O	FT	EVENTOUT	ADC1_10, WKUP2	73	WKUP2	MODULE_WAKEUP#
28	VBAT		----------					65		+VBAT
29	GND		----------					GND		GND
30	GND		----------					GND		GND
31	qSPI_IO1	23	E5(PA7)	I/O	FT	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, QUADSPI_BK2_IO1, EVENTOUT	ADC1_7	49	ADC1_7	ADC1_MICRO
32	qSPI_IO2	24	E4(PC4)	I/O	FT	I2S1_MCK, QUADSPI_BK2_IO2, FSMC_NE4, EVENTOUT	ADC1_14	53	ADC1_14	ADC2_MICRO
33	qSPI_NCS	52	B3(PC11)	I/O	FT	I2S2ext_SD, SPI3_MISO, USART3_RX, QUADSPI_BK2_NCS, FSMC_D2, SDIO_D3, EVENTOUT	-	32	USART3_RX	USART_RX
34	qSPI_IO3	25	G5(PC5)	I/O	FT	I2CFMP1_SMBA, USART3_RX, QUADSPI_BK2_IO3, FSMC_NOE, EVENTOUT	ADC1_15	55	ADC1_15	ADC3_MICRO
35	qSPI_CLK	28	G4(PB2)	I/O	FT	DFSDM1_CKIN0, QUADSPI_CLK, EVENTOUT	BOOT1	NA	BOOT1	BOOT_1
36	qSPI_IO0	22	H6(PA6)	I/O	FT	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, I2S2_MCK, TIM13_CH1, QUADSPI_BK2_IO0, SDIO_CMD, EVENTOUT	ADC1_6	47	ADC1_6	ADC0_MICRO
37	GND		----------					GND		GND
38	MICRO_UART_RX	43	D2(PA10)	I/O	FT	TIM1_CH3, SPI5_MOSI/I2S5_SD, USART1_RX, USB_FS_ID, EVENTOUT	-	32 (Option)	USART1_RX	UART_RX_MICRO
39	MICRO_UART_TX	42	D1(PA9)	I/O	FT	TIM1_CH2, I2C3_SMBA, USART1_TX, USB_FS_VBUS, SDIO_D2, EVENTOUT	-	22 (Option)	USART1_TX	UART_TX_MICRO
40	MICRO_JTAG_TCK	49	E2(PA14)	I/O	FT	JTCK-SWCLK, EVENTOUT	-	NA	JTCK-SWCLK	JTAG_TCK_MICRO
41	MICRO_JTAG_TDO	55	A5(PB3)	I/O	FT	JTDO-SWO, TIM2_CH2, I2CFMP1_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, I2C2_SDA, EVENTOUT	-	NA	JTDO-SWO	JTAG_TDO_MICRO
42	MICRO_JTAG_TRSTN	56	B4(PB4)	I/O	FT	JTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, I2C3_SDA, SDIO_D0, EVENTOUT	-	NA	JTRST	JTAG_TRST_MICRO#
43	MICRO_JTAG_TDI	50	A2(PA15)	I/O	FT	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART1_TX, EVENTOUT	-	NA	JTDI	JTAG_TDI_MICRO
44	MICRO_JTAG_TMS	46	C2(PA13)	I/O	FT	JTMS-SWDIO, EVENTOUT	-	NA	JTMS-SWDIO	JTAG_TMS_MICRO
45	GND		----------					GND		GND
46	VDD_3V3		----------					VCC		+V3.3
47	VDD_3V3		----------					VCC		+V3.3
48	GND		----------					GND		GND
49	VDDIO_WIFI		----------					VCC		+V3.3
50	GND		----------					GND		GND
51	MICRO_USB_HS_DP	45	C1(PA12)	I/O	FT	TIM1_ETR, SPI5_MISO, USART1_RTS, USART6_RX, CAN1_TX, USB_FS_DP, EVENTOUT	-	3	USB_FS_DP	MICRO_USB_HS_DP
52	MICRO_USB_HS_DN	44	D3(PA11)	I/O	FT	TIM1_CH4, SPI4_MISO, USART1_CTS, USART6_TX, CAN1_RX, USB_FS_DM, EVENTOUT	-	5	USB_FS_DM	MICRO_USB_HS_DN
53	MICRO_GPIO_7	35	G1(PB14)	I/O	FT	TIM1_CH2N, TIM8_CH2N, I2CFMP1_SDA, SPI2_MISO, I2S2ext_SD, USART3_RTS, DFSDM1_DATIN2, TIM12_CH1, FSMC_D0, SDIO_D6, EVENTOUT	-	16	EVENTOUT	CB_RESET_OUT#
54	BOOT0	60	D4	I	B	-	VPP	NA		BOOT_0
55	GND		----------					GND		GND
56	GND		----------					GND		GND
57	GND		----------					GND		GND
58	GND		----------					GND		GND
59	GND		----------					GND		GND
60	GND		----------					GND		GND
61	GND		----------					GND		GND
62	GND		----------					GND		GND
63	GND		----------					GND		GND
64	GND		----------					GND		GND
65	GND		----------					GND		GND
66	GND		----------					GND		GND
67	GND		----------					GND		GND
68	GND		----------					GND		GND
69	32K_IN	3	C3(PC14)	I/O	FT	EVENTOUT	OSC32_IN	NA	OSC32_IN	32K_IN
70	GND		----------					GND		GND
71	BT_I2S_DO		----------					I2S_DO		I2S_DO_BT
72	BT_I2S_WS		----------					I2S_WS		I2S_WS_BT
73	BT_I2S_CLK		----------					I2S_CK		I2S_CK_BT
74	GND		----------					GND		GND
75	BT_HOST_WKUP		----------					NA		
76	NC		----------					48		GPIO_5_WL
77	NC		----------					50		GPIO_6_WL
78	WL_GPIO_1		----------					44		GPIO_3_WL
79	BT_PCM_CLK		----------					NA		
80	BT_PCM_OUT		----------					NA		
81	BT_PCM_SYNC		----------					NA		
82	BT_PCM_IN		----------					NA		
83	GND		----------					GND		
TP1	BT_RTS		----------					34		RTS_BT
TP2	BT_CTS		----------					36		CTS_BT
TP3	BT_RXD		----------					32		RXD_BT
TP4	BT_TXD		----------					22		TXD_BT

ADVANTECH
Mapping
Document Number: WISE-1530
Monday, April 24, 2017

WISE-1530 A101-1 PCB: 19A6153000-01 , 96 BOM: 9696W15300E , Date: 2016/12/20

1. First release.

WISE-1530 A101-2 PCB: 19A6153001-01 , 96 BOM: 9696W15300E , Date: 2017/04/24

A101-2.1. BOM: BRK remove.

A101-2.2. BT1 pin 6 (MICRO_GPIO2) connect to M2.COM pin 20 (CB_PWR_ON) for power on signal

A101-2.3. Update Mapping table

A101-2.4. Add C20 for delay reset signal

A101-2.5. Modify system block diag.

A101-2.6. Change 32.768KHz (Y1) cap to 8pF.

A101-2.7. add GPIO3~6_WL 0 ohm.

A101-2.8. Change R4, C6 to 0201 package, delete C5.

ADVANTECH		
Title: HISTORY		
Size	Document Number: WISE-1530	Rev: A101-2
Date: Tuesday, April 25, 2017	Sheet 9 of 9	