

# Practical real-time operating system security for the masses



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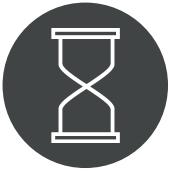
# Why is **microcontroller** security so hard ?

# Security + time = comedy

If a product is successful,  
it will be hacked

Who can't suppress snickering on seemingly dumb security bugs in other people's product? It's easy and delightful to declare developers of failed products as incompetent.

As old stuff has old bugs – we won't run out of entertainment anytime soon.



## Device lifetime

The security of a system is dynamic over its lifetime. Lifetimes of home automation nodes can be 10+ years.



## Attack scale well

The assumption of being hacked at some point requires a solid mitigation strategy for simple, reliable and inexpensive updates.

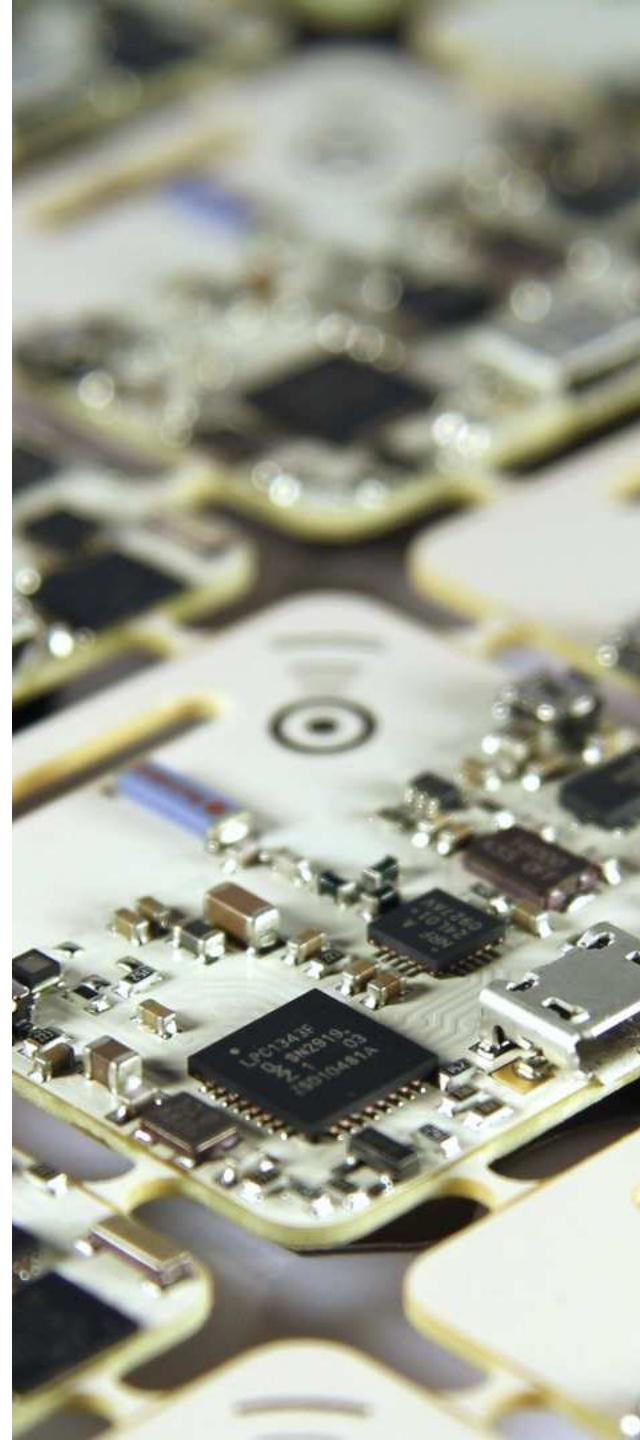
**Do our defenses scale with our attackers?**



## Assume you can't prevent it

Value of bugs is expressed by **value = number\_of\_installations x device\_value**. Increased value and large deployments drive attackers - especially in the IoT.

**Massively parallelized security** researchers/attackers vs. limited product development budgets and time frames.



# Flat memory models

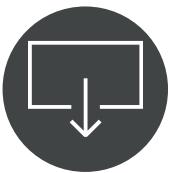
The 80's called, and they want their security model back

A flat address space as the result of lack of a memory management units (MMU) does not justify the absence of security. Many microcontrollers like ARM Cortex-M3/M4 provide a hardware memory protection unit (MPU) instead.



## No separation

Flat memory models and ignorance of MPUs blocks vital security models like “least privilege”.



## Escalation

Flat memory models enable escalation & persistence of bugs by uncontrolled writing to flash memories.



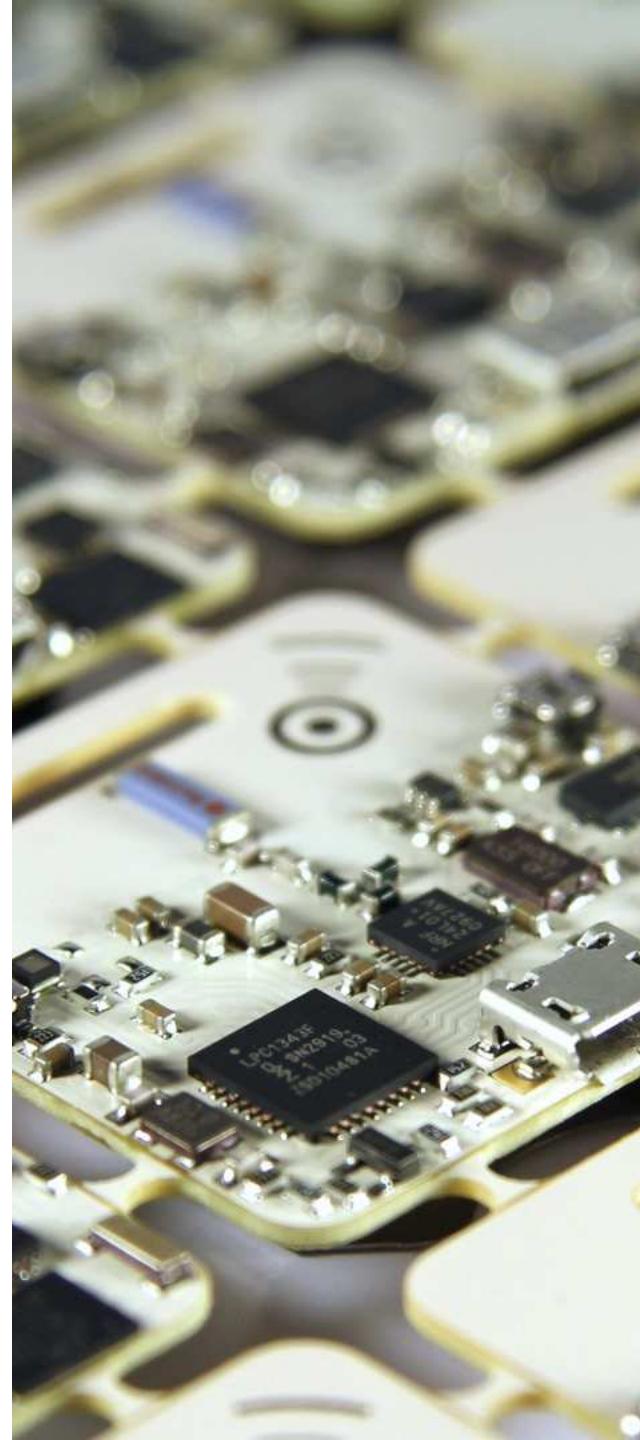
## Verification

Security verification impossible due to the immense attack surface and lack of secure interfaces between system components.



## Leakage

All your bases are belong to us – thanks to leakage of device secrets like identity keys or even class secrets.



# Resources matter

## Lack of abstraction is expensive

Point-solutions are easy to build for microcontrollers, but hard to maintain and to reason about. Abstractions are hard to build, but allow to amortize security verification across a large range of devices.

For crypto APIs highly portable abstractions are common now – yet OS independence is not common for many other security critical components.



## Public key cryptography

Public-key crypto is absent from many low end devices due to memory and speed constraints.



## Shortcuts

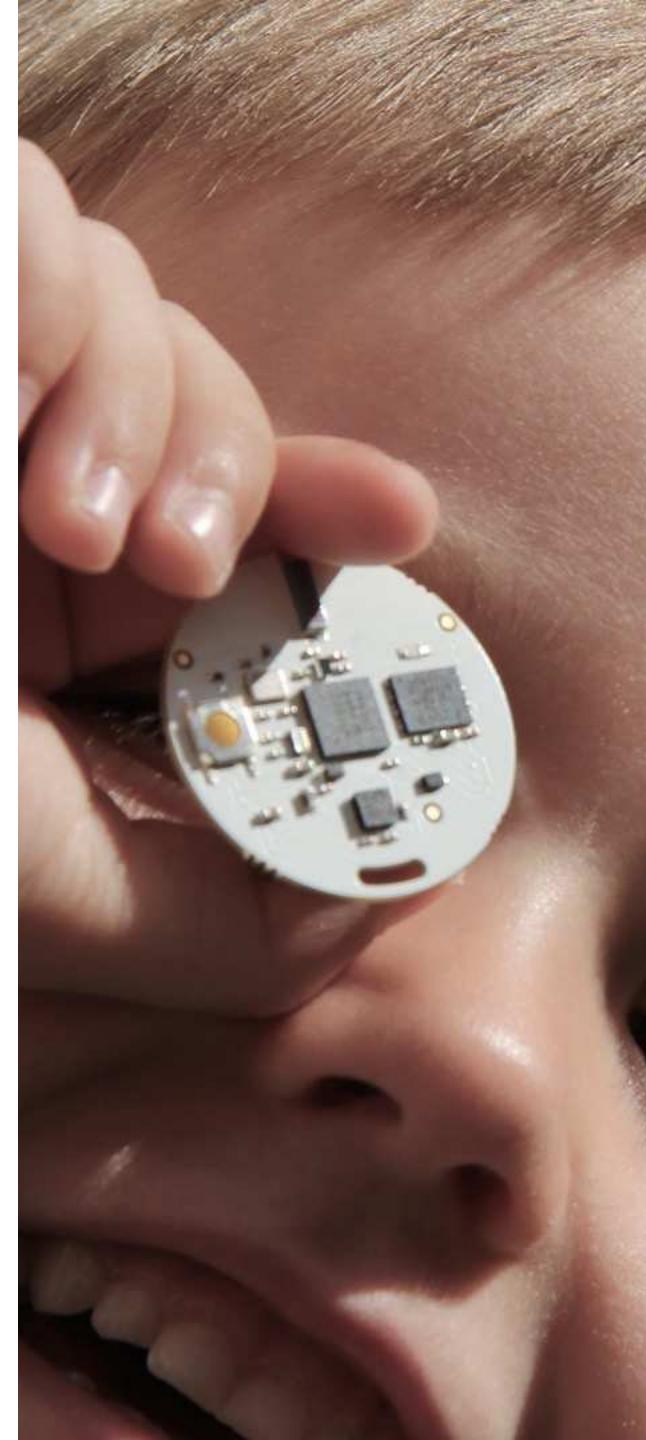
Vendors take compromises on security to reduce footprint. Think for example of commonplace class key usage versus supporting key provisioning and per-device secrets.



## Communication

Less abstraction requires more communication of limitations to developers.

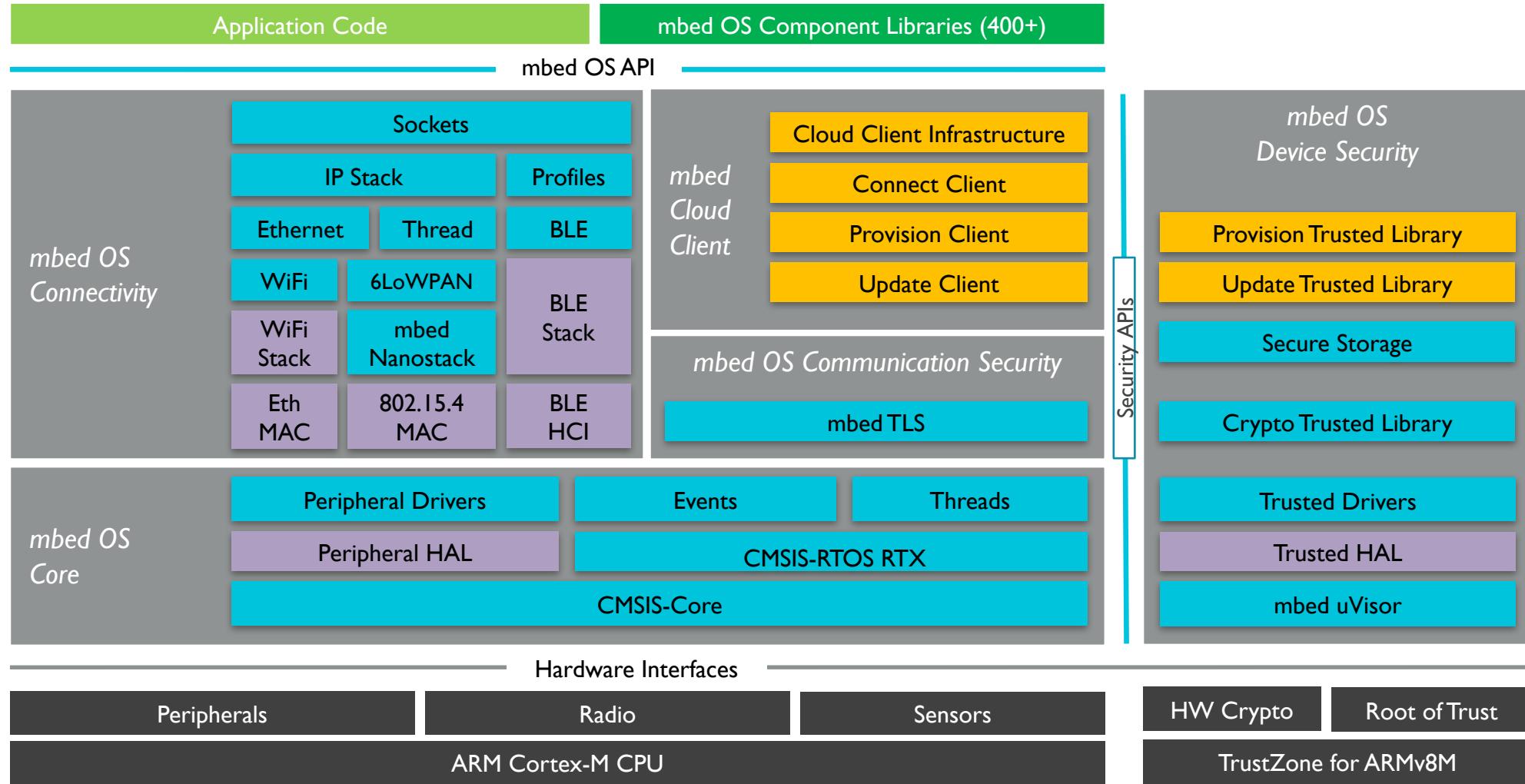
This usually results in higher level components having wrong assumptions about low level components. Think of flash config writing in the presence of a local attacker. Be scared.



# Enter ARM mbed ...

# ARM mbed™

# ARM mbed OS: architected platform security



# ARM mbed OS: architected platform security



**Lifecycle security**  
mbed Cloud secure identity, config and update



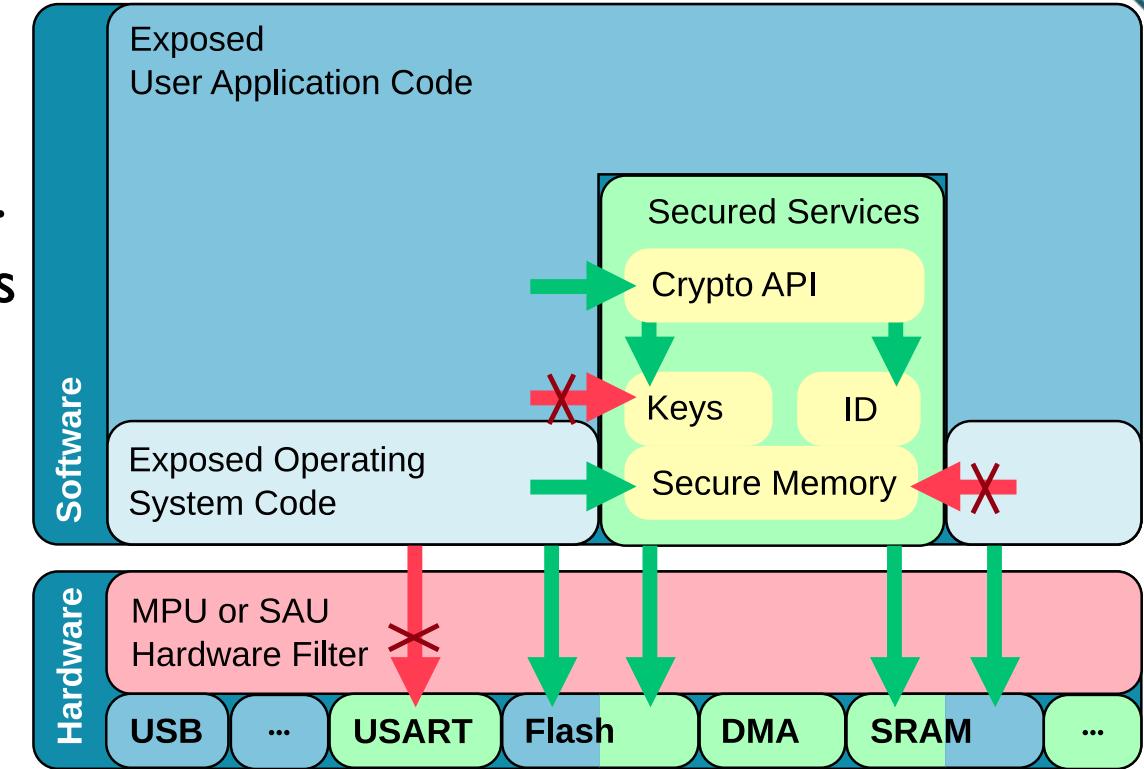
**Communication security**  
mbed TLS



**Secure code compartments**  
mbed uVisor on ARMv7-M & ARMv8-M MPU

# mbed uVisor hypervisor: Hardware security for microcontrollers

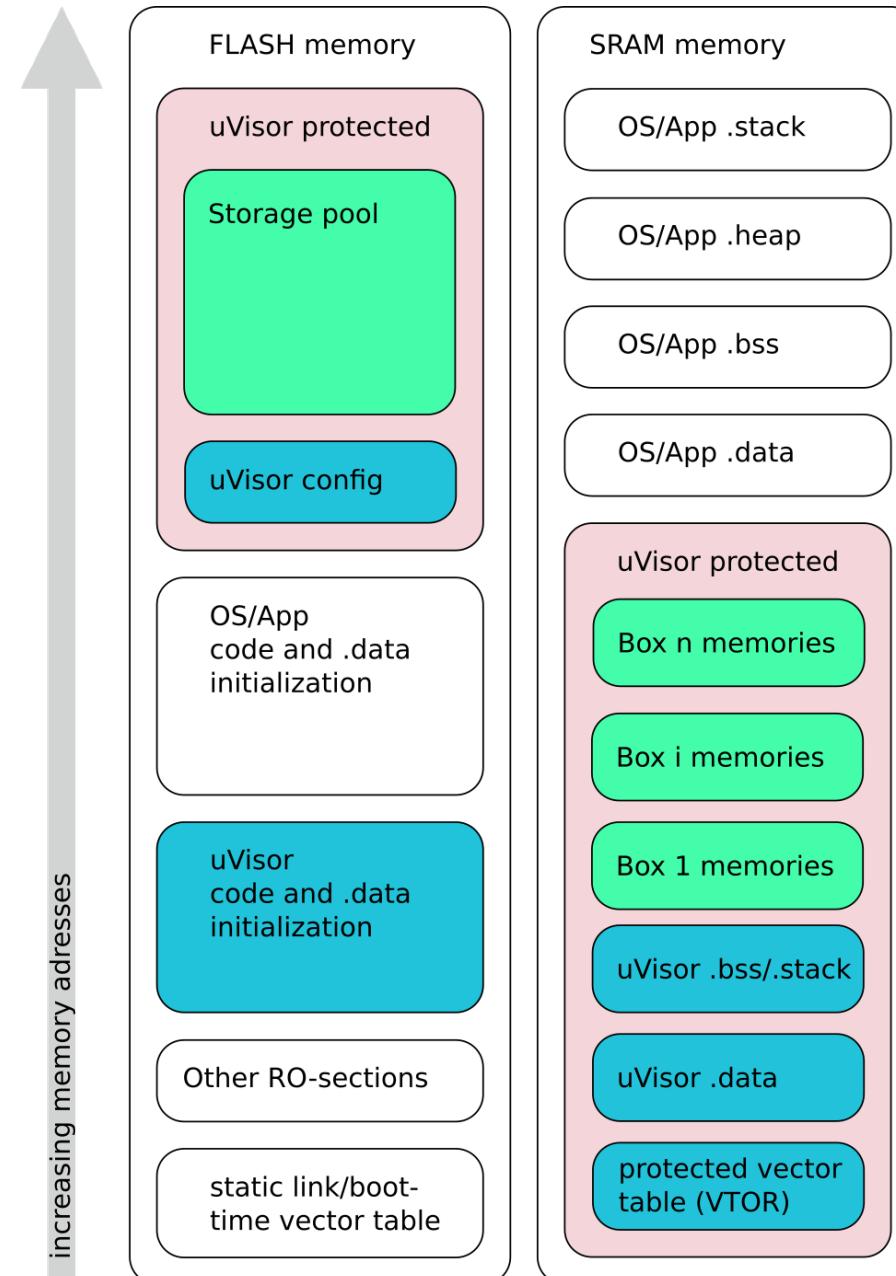
- Enables compartmentalization of threads and processes for microcontrollers.
- Developed on github under Apache license.
- mbed uVisor initialized first in boot process
- Private stack and data sections.
- Initialization of memory protection unit (MPU) based on box permissions:
  - Whitelist approach – only required peripherals are accessible to each box.
  - Each box has private .bss data and stack sections.
- De-privileges execution, continues boot unprivileged to initialize OS and libraries.



# System security model for microcontrollers

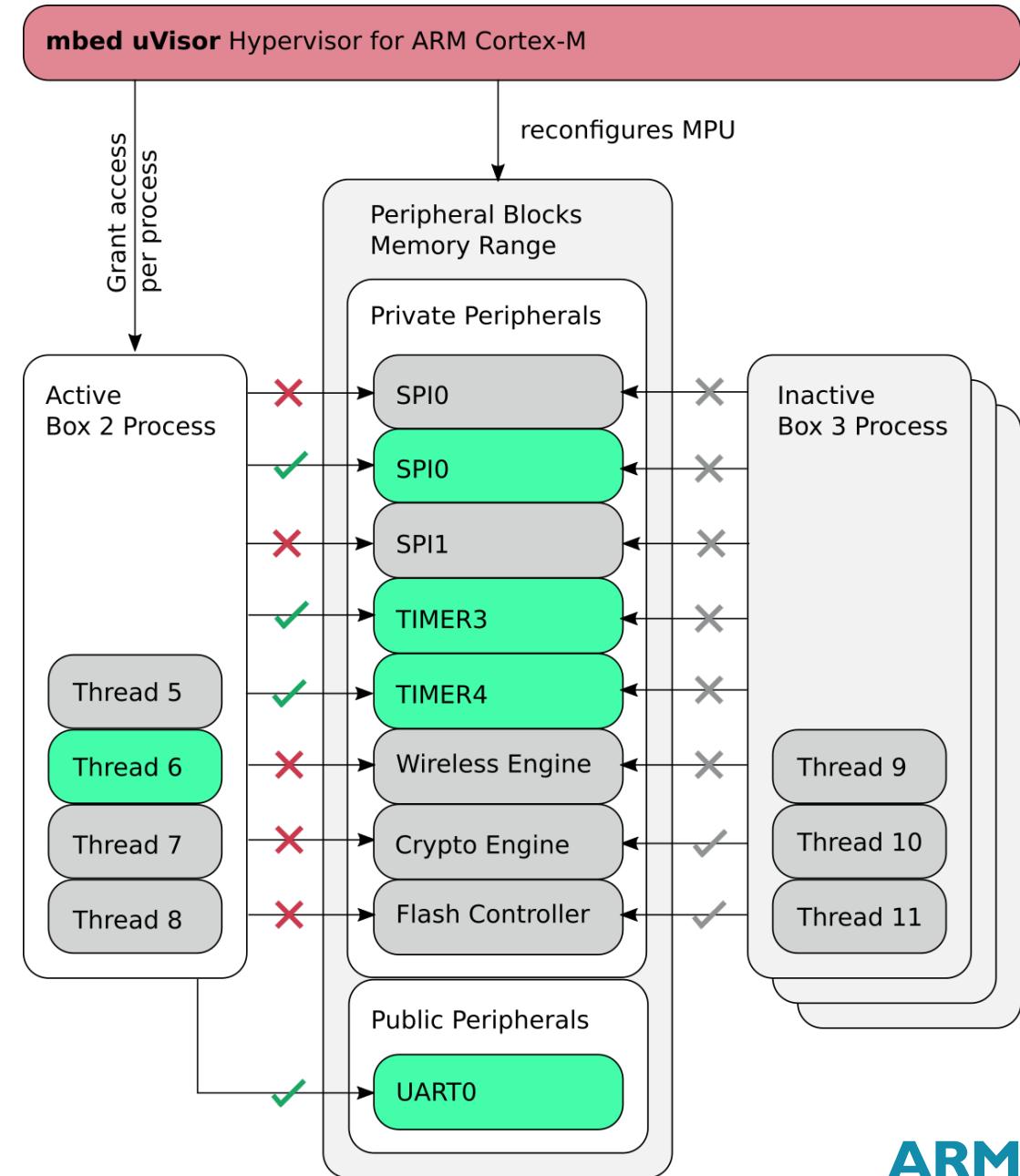
# mbed uVisor security

- Security model for ARM Cortex v7M/v8M microcontrollers compatible with Cortex A-class and server operating systems like Linux.
- mbed uVisor allocates protected per-box stacks and detects under-/overflows during operation.
- Public box memories accessible to all boxes for backward compatible APIs.
- Per-Box data sections are protected by default:
  - Secure per-box context memory, stack and heap.
  - Shared data/peripherals with other boxes on demand.
- mbed uVisor code sections visible to everybody
- Remaining flash memory is made available to the system as a persistent storage pool.
- **Write access to flash is only allowed through APIs of a dedicated flash-access box process.**



# Least privilege: Peripherals

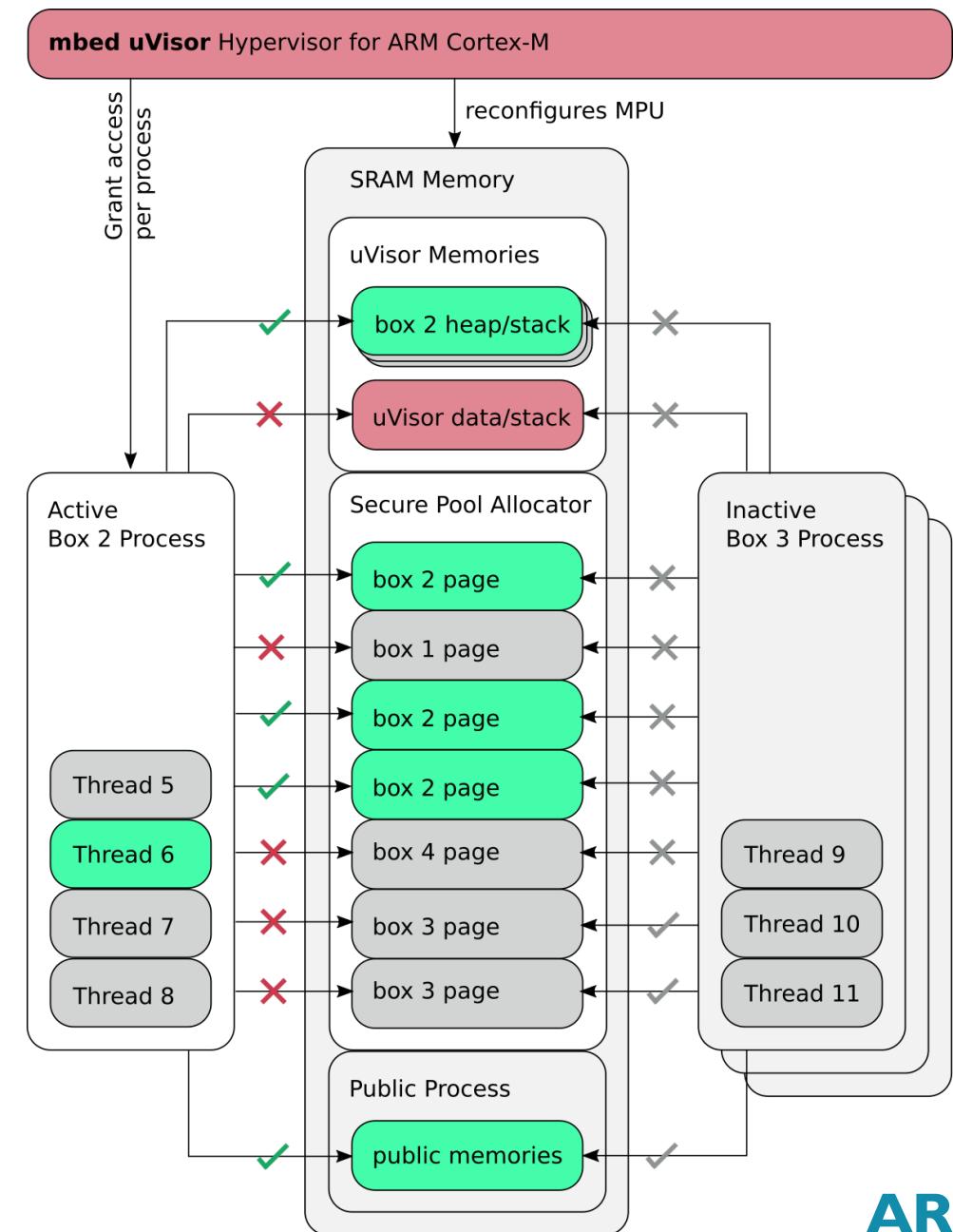
- **Mutually distrustful security model:**
  - “Principle of least privilege”
  - Boxes are protected against each other.
  - Boxes protected against malicious code from broken system components, driver or other boxes.
- **Per-box access control lists (ACL):**
  - Restrict access to selected peripherals on a “Need to use basis” for each box.
  - Public box peripherals are accessible to all boxes.
- **Hardware-enforced security sandboxes:**
  - mbed uVisor manages box-specific ACLs and reconfigures the MPU upon process switch.



# Least privilege: Memories

## Two-tier memory allocation

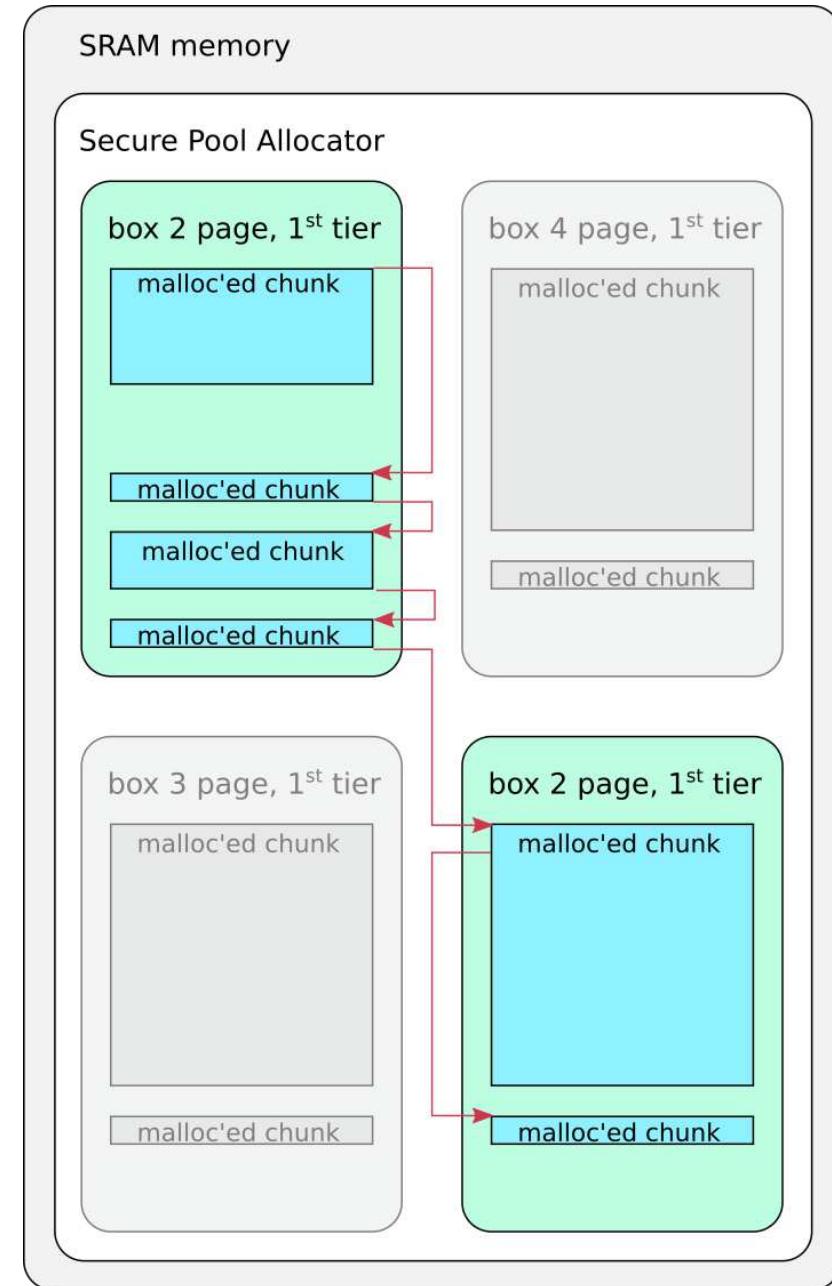
- **Static box memories:**
  - Boxes commit to heap/stack size of initial box thread using the link time box configuration.
  - All global variables end up in the default box, accessible to all boxes for backward compatibility.
  - The optional secure box context replaces secure global variables. The context size is specified in the box configuration macro.
- **Dynamic memories:**
  - Each box requests large pages from mbed uVisor.
  - After usage pages are returned to mbed uVisor.
  - **Secure box data must be copied across boxes or placed into the public box.**



# Pages for MMU-less systems

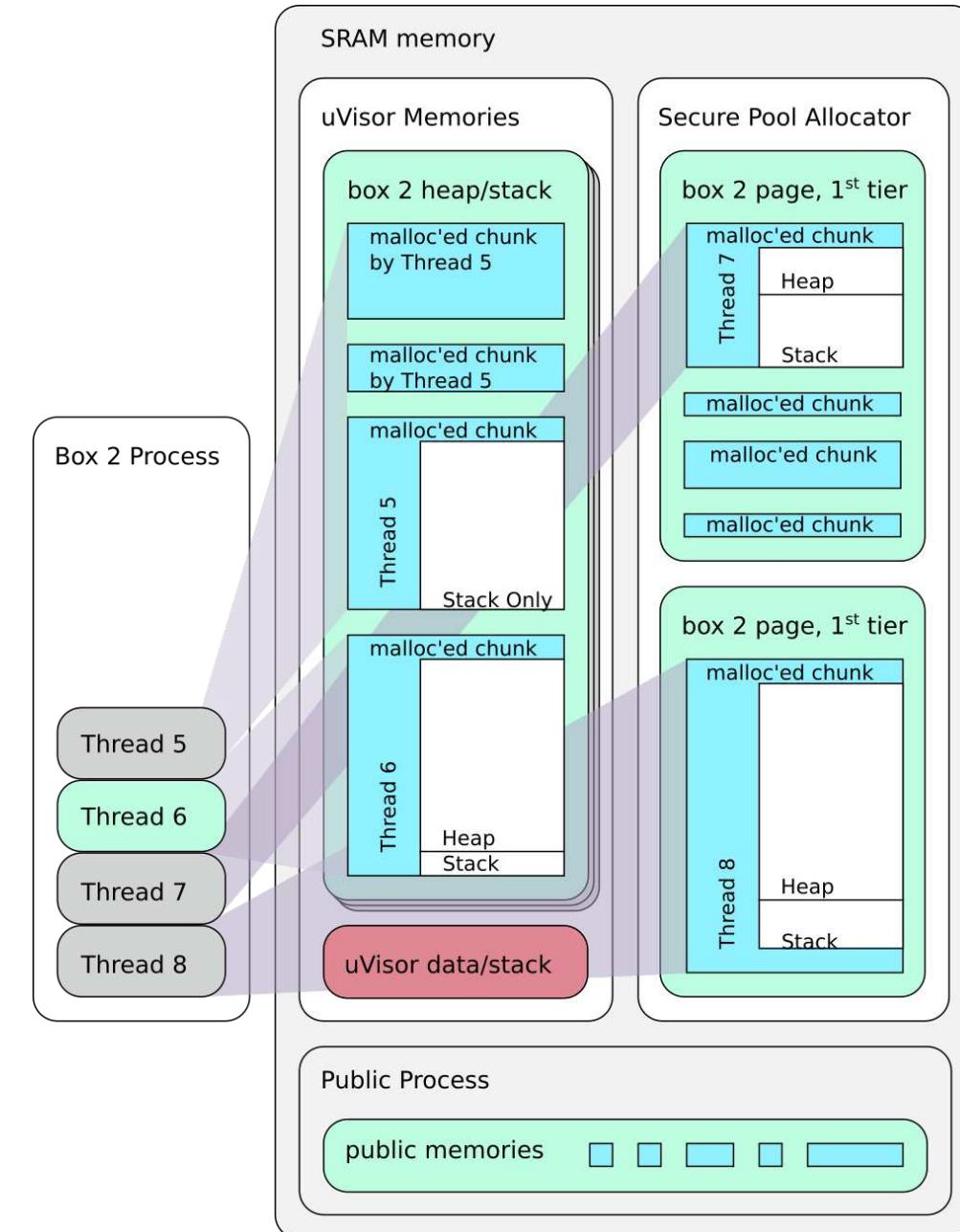
## Two-tier memory allocation

- 1<sup>st</sup> tier page pool is handled by mbed uVisor.  
Memory security is maintained on a per-page basis
- The guest OS manages the 2<sup>nd</sup> tier for fine grained allocations.
- 2<sup>nd</sup> tier allocations are guaranteed to be continuous for backward compatibility as long as they are smaller than the page size.
- mbed uVisor user mode libraries provide a default implementation for the 2<sup>nd</sup> tier memory allocator.
- The public box allocates pages from the bottom of the page pool to enable continuous allocations.
- Secure boxes allocate from the top of the pool.
- The default page size is SRAM\_SIZE divided 16, but can be configured during compile time.



# Defeating fragmentation

- Threads allocate stack and heap memories by default in the thread owners box heap.
- Short-lived high-memory threads like crypto libraries get a custom heap for their allocator.
- All 2<sup>nd</sup>-tier memory allocations are redirected into thread-specific protected heaps:
  - Thread-specific heaps can be allocated on the box heap.
  - Thread-heaps can optionally live in temporary 1<sup>st</sup> tier pages.
- mbed uVisor switches to the correct thread allocator upon thread switch.
- On thread termination all thread-memories can be released without fragmentation.



# “Hello world”

## Application example

# mbed uVisor peripheral sharing across boxes

- main.cpp enables mbed uVisor and configures the public heap size.
- All global variables are accessible to every box for backward compatibility.
- The access control list (ACLs) for the public box is initialized to allow access to non-security-critical system peripherals by the core OS.
- ACLs are white-listed – only listed peripherals are accessible by the public box.

```
17 #include "uvvisor-lib/uvvisor-lib.h"
18 #include "mbed.h"
19 #include "main-hw.h"
20
21 /* Create ACLs for main box. */
22 MAIN_ACL(g_main_acl);
23
24 /* Enable uVisor. */
25 UVISOR_SET_MODE_ACL(UVISOR_ENABLED, g_main_acl);
26 UVISOR_SET_PAGE_HEAP(8*1024, 5);
27
28 int main(void)
29 {
30     DigitalOut led1(MAIN_LED);
```

# Set up public peripheral ACLs for the main box

- ACLs are declared as arrays of memory start address, peripheral size and permissions.
- Permissions must be either non-overlapping between boxes or marked as shared in all boxes.
- Public peripherals are accessible across all boxes and declared in the public box through ACLs.
- **Memories can't be shared between secure boxes, only from public to secure boxes.**

```
32 #define MAIN_ACL(acl_list_name) \
33     static const UvisorBoxAclItem acl_list_name[] = {      \
34         {SIM,      sizeof(*SIM),      UVISOR_TACLDEF_PERIPH}, \
35         {OSC,      sizeof(*OSC),      UVISOR_TACLDEF_PERIPH}, \
36         {MCG,      sizeof(*MCG),      UVISOR_TACLDEF_PERIPH}, \
37         {PORTA,    sizeof(*PORTA),    UVISOR_TACLDEF_PERIPH}, \
38         {PORTB,    sizeof(*PORTB),    UVISOR_TACLDEF_PERIPH}, \
39         {PORTC,    sizeof(*PORTC),    UVISOR_TACLDEF_PERIPH}, \
40         {PORTD,    sizeof(*PORTD),    UVISOR_TACLDEF_PERIPH}, \
41         {PORTE,    sizeof(*PORTE),    UVISOR_TACLDEF_PERIPH}, \
42         {RTC,      sizeof(*RTC),      UVISOR_TACLDEF_PERIPH}, \
43         {LPTMR0,   sizeof(*LPTMR0),   UVISOR_TACLDEF_PERIPH}, \
44         {PIT,      sizeof(*PIT),      UVISOR_TACLDEF_PERIPH}, \
45         {SMC,      sizeof(*SMC),      UVISOR_TACLDEF_PERIPH}, \
46         {UART0,   sizeof(*UART0),   UVISOR_TACLDEF_PERIPH}, \
47         {I2C0,      sizeof(*I2C0),      UVISOR_TACLDEF_PERIPH}, \
48         {SPI0,      sizeof(*SPI0),      UVISOR_TACLDEF_PERIPH}, \
49     }
```

# Secure multithreading on CMSIS RTOS

# Define thread in a dedicated security context

- Set box Namespace to **NULL**:
  - Later used for RPC communication.
- Thread main heap is set to 8kb.
- Register **my\_box\_main** as thread entry point with normal priority.
- Set stack size to default stack size.
- Declare **my\_box\_context** type as secure box context.
- Declare name of this security context to be **my\_box**.
- No additional ACL's defined for peripherals in constant access control list (ACL).

```
21  typedef struct {
22      InterruptIn * sw;
23      DigitalOut * led;
24      RawSerial * pc;
25  } my_box_context;
26
27  static const UvisorBoxAclItem acl[] = {
28  };
29
30  static void my_box_main(const void *);
31
32  UVISOR_BOX_NAMESPACE(NULL);
33  UVISOR_BOX_HEAPSIZE(8192);
34  UVISOR_BOX_MAIN(my_box_main, osPriorityNormal, UVISOR_BOX_STACK_SIZE);
35  UVISOR_BOX_CONFIG(my_box, acl, UVISOR_BOX_STACK_SIZE, my_box_context);
```

# Secure thread initialization

```
48 static void my_box_main(const void *)
49 {
50     /* allocate serial port to ensure that code in this secure box
51      * won't touch handle in the default security context when printing */
52     RawSerial *pc;
53     if(!(pc = new RawSerial(USBTX, USBRX)))
54         return;
55     /* remember serial driver for IRQ routine */
56     uvisor_ctx->pc = pc;
```

- The `my_box_main` box entry point will be executed in the boxes security context
- First of al the RawSerial UART class is created in the thread.
- The memory allocation for the class creation is redirected to main thread heap and thus in a memory that is exclusive to `my_box_main`.
- Each process gets a `uvvisor_ctx pointer` for free at the box-specific type of `box_context`.
- Data stored in `uvvisor_ctx` is exclusive to the active box.

# Secure **interrupt** handling

# Secure mbed uVisor interrupt API

- Interrupt ownership is exclusive – multiple boxes cannot register for the same interrupt.
- Registration is based on first-come-first-serve: sharing IRQ's only possible via custom box service APIs .
- mbed uVisor remembers the association between each Interrupt handler and the box security context during registration: other boxes can't use that interrupt until it is released.
- Handlers are executed as unprivileged C functions within the process that registered the IRQ.

```
66     /* allocate a box-specific switch handler */
67     if(!(uvisor_ctx->sw = new InterruptIn(SW2)))
68         pc->printf("ERROR: failed to allocate memories for SW1\n");
69     else
70     {
71         /* register handler for switch SW1 */
72         uvisor_ctx->sw->mode(PullUp);
73         uvisor_ctx->sw->fall(my_box_switch_irq);
74
75         /* no problem to return here as everything is initialized */
76         return;
77     }
```

---

```
37 static void my_box_switch_irq(void)
38 {
39     /* flip LED state */
40     *uvisor_ctx->led = !*uvisor_ctx->led;
41
42     /* print LED state on serial port */
43     uvisor_ctx->pc->printf(
44         "\nPressed SW2, printing from interrupt - LED changed to %i\n\n",
45         (int)(*uvisor_ctx->led));
46 }
```

# Function calls across security domains

# RPC: secure remote procedure calls

- mbed uVisor forwards calls to boxes
- Both synchronous and asynchronous secure RPC calls are supported.

```
32 static uint32_t get_number(void);
33 static int set_number(uint32_t number);
34
35 /* Box configuration */
36 UVISOR_BOX_NAMESPACE(NULL);
37 UVISOR_BOX_HEAPSIZE(8192);
38 UVISOR_BOX_MAIN(number_store_main, osPriorityNormal, UVISOR_BOX_STACK_SIZE);
39 UVISOR_BOX_CONFIG(box_number_store, acl, UVISOR_BOX_STACK_SIZE, box_context);

41 /* Gateways */
42 UVISOR_BOX_RPC_GATEWAY_SYNC (box_number_store, secure_number_get_number, get_number, uint32_t, void);
43 UVISOR_BOX_RPC_GATEWAY_ASYNC(box_number_store, secure_number_set_number, set_number, int, uint32_t);
```

# RPC: secure remote procedure calls

- Callee verifies the caller identity by resolving the box namespace.
- Verification result is cached.
- Caller box-name can be only defined during compile time.
- Callee can impose arbitrary restrictions based on the caller ID and the ownership and origin of an object.

```
69 static int set_number(uint32_t number)
70 {
71     const int id = get_caller_id();
72
73     /* Cache the name verification result. This allows future checks to replace
74      * a relatively more expensive string compare with a cheaper integer
75      * comparison. */
76     if (uvisor_ctx->trusted_id == -1) {
77         char name[UVISOR_MAX_BOX_NAMESPACE_LENGTH];
78         memset(name, 0, sizeof(name));
79         uvisor_box_namespace(id, name, sizeof(name));
80         /* We only trust client a. */
81         static const char * trusted_namespace = "client_a";
82         if (memcmp(name, trusted_namespace, sizeof(*trusted_namespace)) == 0) {
83             uvisor_ctx->trusted_id = id;
84             printf("Trusted client a has box id %u\n", id);
85         } else {
86             return 1;
87         }
88     }
89     if (uvisor_ctx->trusted_id != id) {
90         /* This box is not allowed to write to the secret number. */
91         return 1;
92     }
}
```

# RPC: secure remote procedure calls

- Callee waits in one or more threads on remote function calls.
- Only one call executed at a time per thread to protect thread stack.
- Remote call executed thread-safe in waiting thread.
- Similar to Posix poll function – callee waits on array of function pointers.

```
103 static void number_store_main(const void *)
104 {
105     /* Today we only allow client a to write to the number. */
106     uvisor_ctx->trusted_id = -1;
107
108     /* The list of functions we are interested in handling RPC requests for */
109     static const TFN_Ptr my_fn_array[] = {
110         (TFN_Ptr) get_number,
111         (TFN_Ptr) set_number
112     };
113
114     while (1) {
115         int status;
116
117         /* NOTE: This serializes all access to the number store! */
118         status = rpc_fncall_waitfor(my_fn_array, 2, &uvisor_ctx->caller_id, UVISOR_WAIT_FOREVER);
119
120         if (status) {
121             printf("Failure is not an option.\r\n");
122             uvisor_error(USER_NOT_ALLOWED);
123         }
124     }
125 }
```

# Securely **shared** peripheral registers

# Security-agnostic register level access functions

- Fine grained peripheral access down to register/bit level:
  - Alternative method to peripheral ACL's – mbed uVisor executes access on behalf of the box.
  - Multiple boxes can have access to selected bits in one register.
  - Perfectly suitable for shared GPIO and clock registers to stop interference and DoS.
- Convenient portable wrapper functions:
  - SECURE\_WRITE(`address, value`)
  - SECURE\_READ(`address`)
  - SECURE\_BITS\_GET(`address, mask`)
  - SECURE\_BITS\_CHECK(`address, mask`)
  - SECURE\_BITS\_SET(`address, mask`)
  - SECURE\_BITS\_CLEAR(`address, mask`)
  - SECURE\_BITS\_SET\_VALUE(`address, mask, value`)
  - SECURE\_BITS\_TOGGLE(`address, mask`)

# Register level access security

- Limits access to specific register bits to the specific caller boxes.
- Call gateways only accepted by mbed uVisor from flash memory:
  - Attacker has no write access to flash controller, can't make up new gateways.
- Gateways verified during firmware update or before firmware signing.
- Metadata of register gateways at a fixed offset from mbed uVisor gateway context switch – a SVC supervisor call.
  - Contains pointer to register and access mask, guaranteed verification latency for cross-box calls.

```
119 #define uvisor_write(box_name, shared, addr, val, op, msk) \
120 { \
121     /* Instantiate the gateway. This gets resolved at link-time. */ \
122     __attribute__((aligned(4))) static TRegisterGateway const register_gateway = { \
123         .svc_opcode = UVISOR_SVC_OPCODE(UVISOR_SVC_ID_REGISTER_GATEWAY), \
124         .branch     = BRANCH_OPCODE(__UVISOR_OFFSETOF(TRegisterGateway, branch), \
125                                     __UVISOR_OFFSETOF(TRegisterGateway, bxlr)), \
126         .magic      = UVISOR_REGISTER_GATEWAY_MAGIC, \
127         .box_ptr    = (uint32_t) &box_name ## _cfg_ptr, \
128         .address    = (uint32_t) addr, \
129         .mask       = msk, \
130         .operation  = UVISOR_RGW_OP(op, sizeof(*addr), shared), \
131         .bxlr       = BXLR \
132     }; \
133     \
134     /* Pointer to the register gateway we just created. The pointer is \
135      * located in a discoverable linker section. */ \
136     __attribute__((section(".keep.uvisor.register_gateway_ptr"))) \
137     static uint32_t const register_gateway_ptr = (uint32_t) &register_gateway; \
138     (void) register_gateway_ptr; \
139     \
140     /* Call the actual gateway. \
141      * The value is passed as the first argument. */ \
142     ((void (*)(uint32_t)) ((uint32_t) ((uint32_t) &register_gateway | 1)))((uint32_t) (val)); \
143 }
```

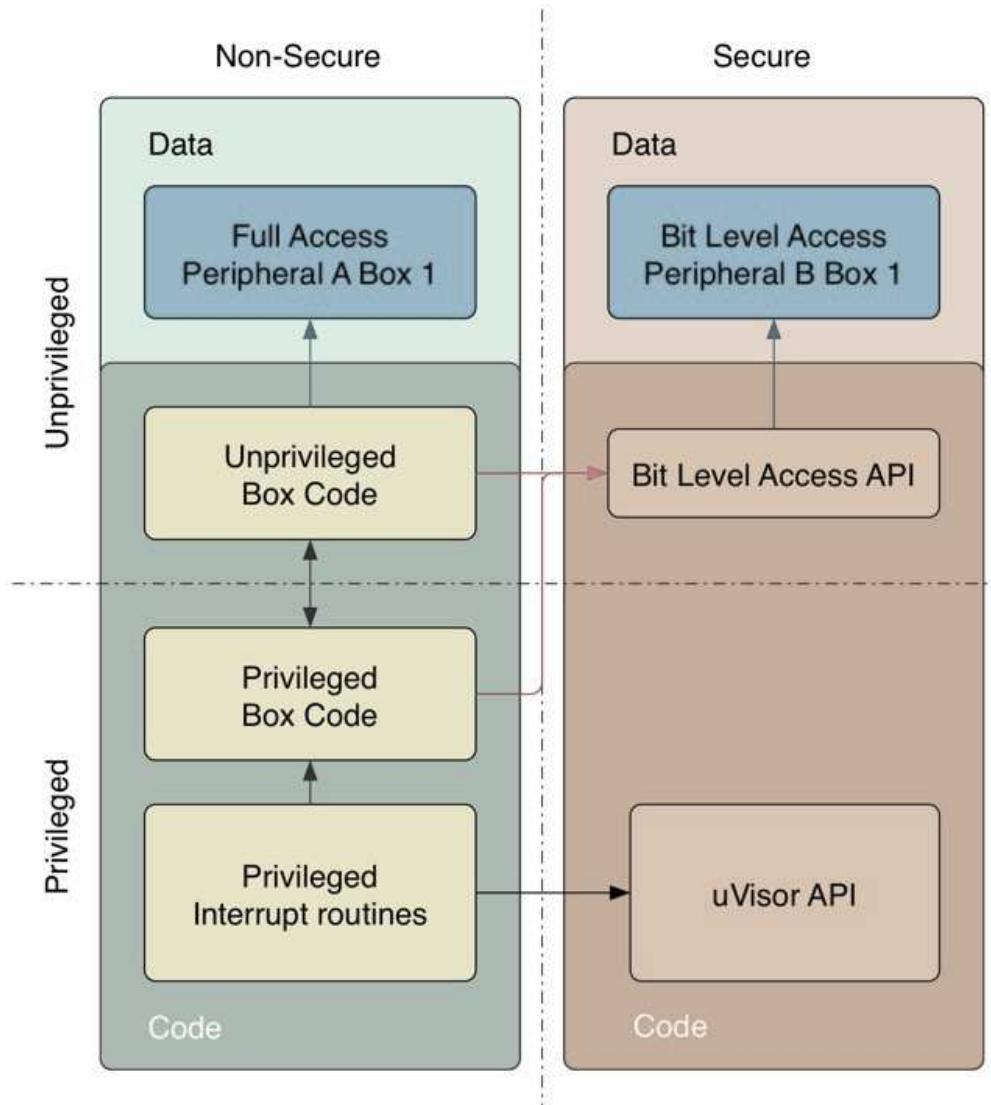
# mbed uvisor: Future outlook

# mbed uVisor on TrustZone-M

- ARM mbed uVisor application security model of TrustZone for ARMv8M is source-compatible with the ARMv7-M security model.
- Additionally TrustZone for ARMv8M enables bus level protection in hardware:
  - ARMv7-M requires software API filters for DMA access and other security critical operations.
  - ARMv8-M can filter for DMA access for requests initiated by unprivileged code on bus level.
- TrustZone for ARMv8M MPU banking reduces complexity of secure target OS:
  - Secure OS partition owns a private MPU with full control.
  - OS keeps the privileged mode for fast IRQs.
  - Fast interrupt routing and register clearing in hardware.
  - Fast cross-box calls on TrustZone for ARMv8M – optimized call gateways.

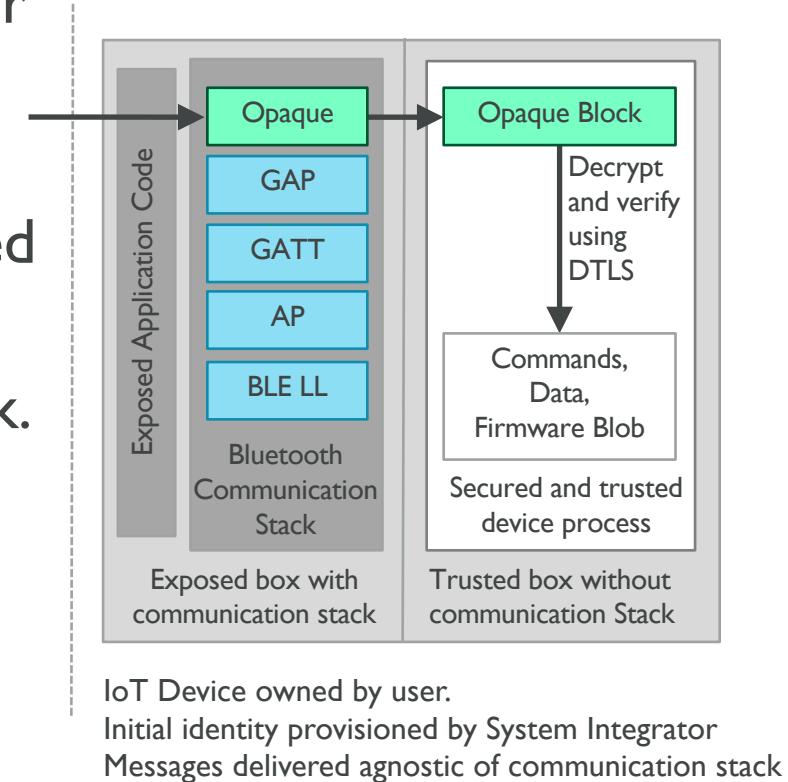
# Secure device services on TrustZone-M: SDS

- Use hardware-accelerated security context switching for low latency system services.
  - Secure Interrupt management
  - Secure GPIO access (pin-wise access)
  - Register Level / Bit Level access gateway
  - IPC
  - DMA-APIs
  - Shared Crypto Accelerators / Crypto API
  - Random Entropy Pool Drivers
  - Key Provisioning / Storage
  - Configuration Storage APIs
  - ... and many more



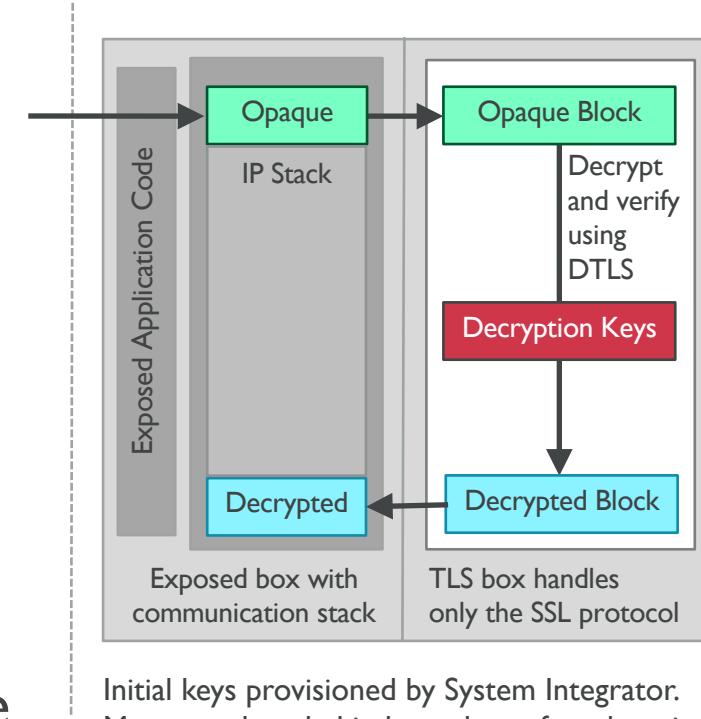
# Case study: Secure server communication

- Trusted messages contain commands, data or firmware parts.
- Box security not affected by communication stack exploits or infections outside of trusted box.
- Payload delivery is agnostic of protocol stack.
- Resilient box communication over the available channels:
  - Ethernet, CAN-Bus, USB, Serial
  - Bluetooth, Wi-Fi, ZigBee, 6LoWPAN



# Case study: Secure server communication

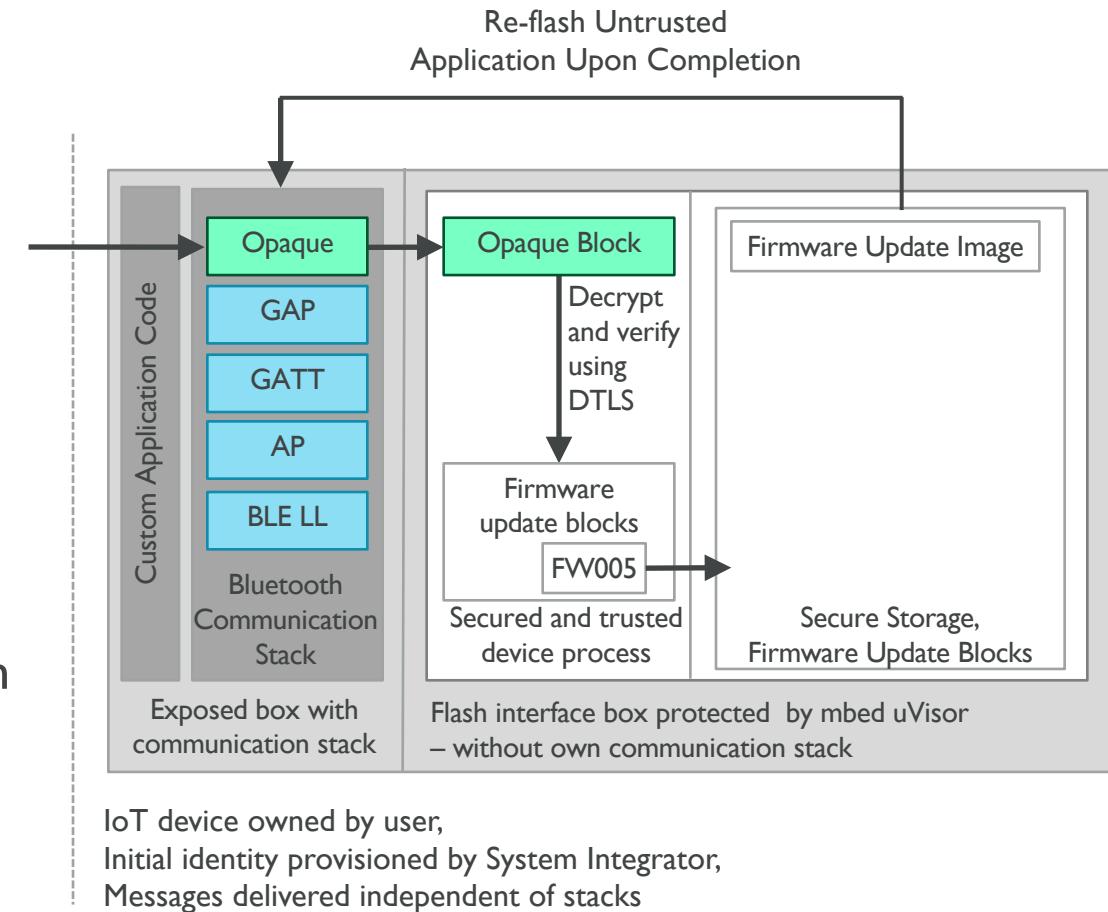
- Communication protected by mbed TLS.
- Raw message payloads decrypted and verified directly by protected code:
  - mbed TLS box not exposed to communication protocol stack bugs.
  - No interference by other boxes.
  - Low attack surface.
- Authentication and encryption keys are protected against malware.
- Malware can't interfere without knowing the encryption or signing keys.



Initial keys provisioned by System Integrator.  
Messages decoded independent of stacks using  
mbed TLS in separate security context

# Case study: Secure remote firmware update

- Delivery of firmware update must be decoupled from a protocol-independent firmware image verification.
- Bugs in communication stacks or cloud infrastructure must not compromise the firmware update:
  - End-to-end security for firmware updates between the firmware developer and the one secure box on the device with exclusive flash-write-access ACLs.
  - Box with flash controller ACLs only needs the public update key to verify validity of firmware.
  - Local malware can't forge a valid firmware signature to the firmware update box, the required private firmware signature key is not in the device.



# Case study: Controlled malware recovery

- Secure box can remotely recover from malware:
  - Enforces communication through the exposed side to the server.
  - Receives latest security rules and virus behaviour fingerprints for detection.
  - Shares detected pattern fingerprint matches with control server
  - Distributed detection of viruses and live infrastructure attacks.
  - Thanks to flash controller ACL restrictions, malware can't modify monitor code or install itself into non-volatile memories.
- When communication with the server breaks for a minimum time:
  - Parts of the device stack are reset to a known-good state.
  - Reset prevents malware from staying on the device.
  - Device switches to a safe mode to rule out network problems or to remotely update the firmware via reboot if needed.



<https://commons.wikimedia.org/wiki/File:Biohazard.svg>

“The mantra of any good security engineer is: “**Security is not a product, but a process**” It's more than designing strong cryptography into a system; it's designing the entire system such that all security measures, including cryptography, work together.”

– Bruce Schneier

# Thank you – Questions?

Get the latest information on mbed security...

<https://www.mbed.com/en/technologies/security/>

... follow live mbed uVisor development on github.com:

<https://github.com/ARMmbed/uvisor/>

More presentations and in-depth OS-level integration  
and porting documents can be found there as well.

Contact: Milosch Meriac <[milosch.meriac@arm.com](mailto:milosch.meriac@arm.com)>

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# Support slide: Getting started

# uVisor: development basics

- uVisor debugging is platform independent via Semi-hosting. Please ensure that your debugger of choice supports semihosting and that its turned on.
- Please use the [secure threaded blinky example](#) for starting uVisor development.
- For release builds, please enter:
  - mbed compile -m K64F\_SECURE -t GCC\_ARM -c
- When connecting a debugger, output can be seen on the debug console with a debug build:
  - mbed compile -m K64F\_SECURE -t GCC\_ARM -c -o debug-info
- Debug Alternatives for NXP FRDM-K64F:
  - [OpenSDA Users Guide](#): Follow instructions for updating the boot loader. The boot loader firmware image can be downloaded [here](#).
  - [Ozone](#) – J-Link compatible debugger, but CodeWarrior, Eclipse, Keil, IAR, KDS should be fine, too.
  - Serial console printf serial enabled at 9600 baud over CDC USB serial interface of the K64F
- For porting uVisor to new platforms, please refer to our [porting guide](#)
- You can download a docker-based pre-configured uVisor development [here](#)
- **Your device will freeze if your run a debug version of your app as it will wait for a debugger to connect!**

The screenshot shows the Ozone J-Link Debugger interface. The assembly window displays the main loop of the application, which includes printf statements and a main loop counter. The registers window shows CPU register values for R0 through R11. The memory window shows the stack and heap areas. The terminal window shows the printf output from the application.

The screenshot shows the Ozone J-Link Debugger interface. The assembly window displays the led\_main function, which handles LED toggling and memory access. The registers window shows CPU register values for R0 through R14. The memory window shows the stack and heap areas. The terminal window shows the printf output from the application.