Universidad Politécnica de Cartagena
Departamento de Electrónica, Tecnología de Computadoras y Proyectos

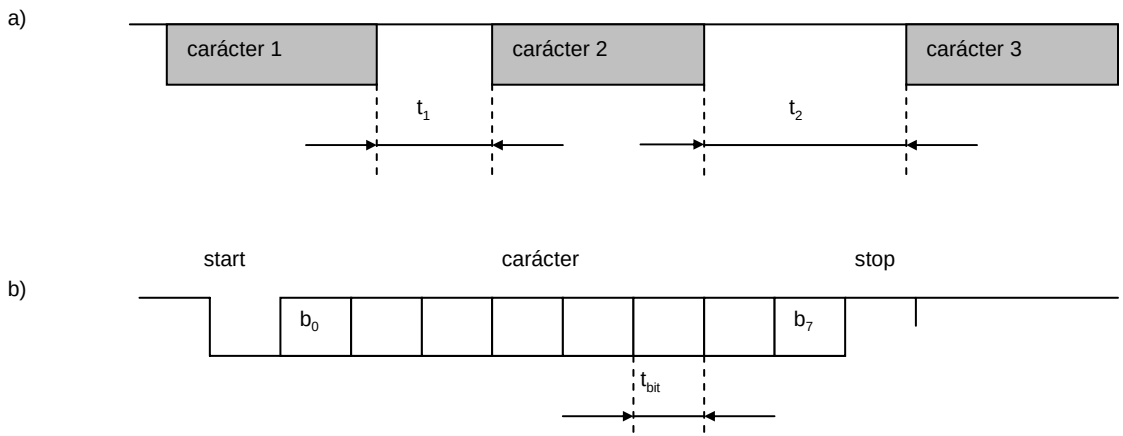
Práctica:

Comunicación por puerto serie

Titulación: Ingeniero de Telecomunicación
Asignatura: Arquitectura y Tecnología de Computadores

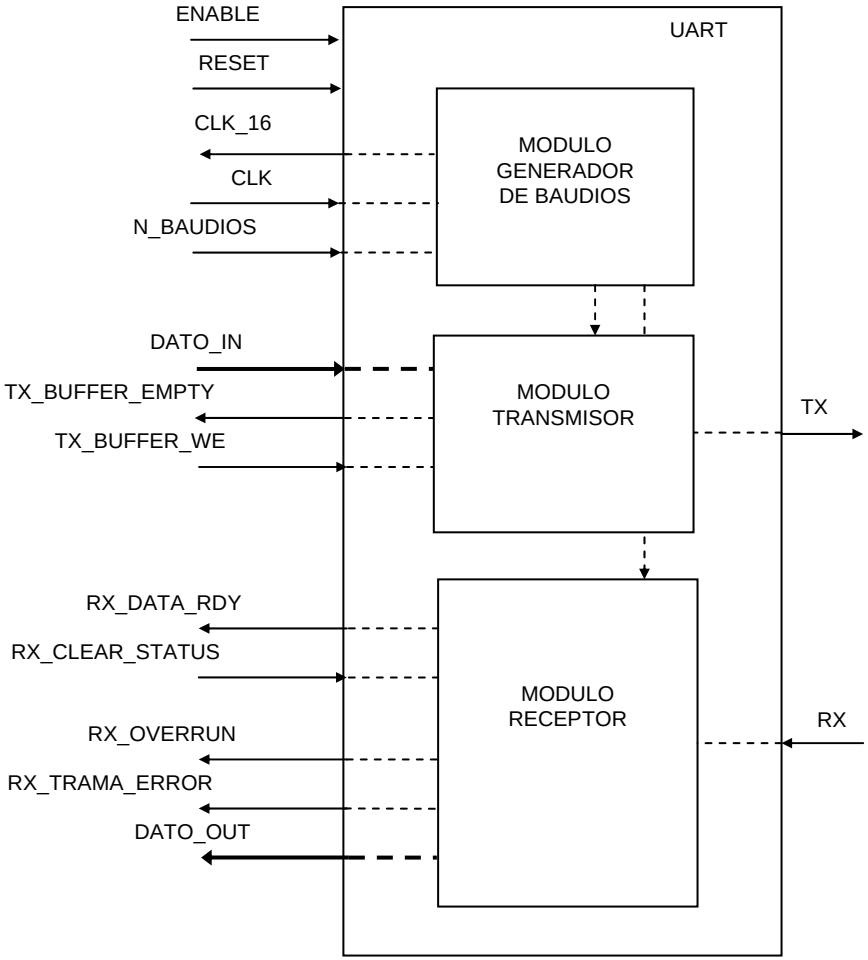
Transmisión serie asíncrona

- La unidad de transmisión es el carácter
- Tiempo entre caracteres arbitrario
- Temporización rígida dentro de cada carácter(t_{bit})
- Formato: 1 bit start – 8 bits datos – 1 bit stop
- Primero se transmite el bit de menor peso (b_0)



UART – Estructura general

- Estructura:



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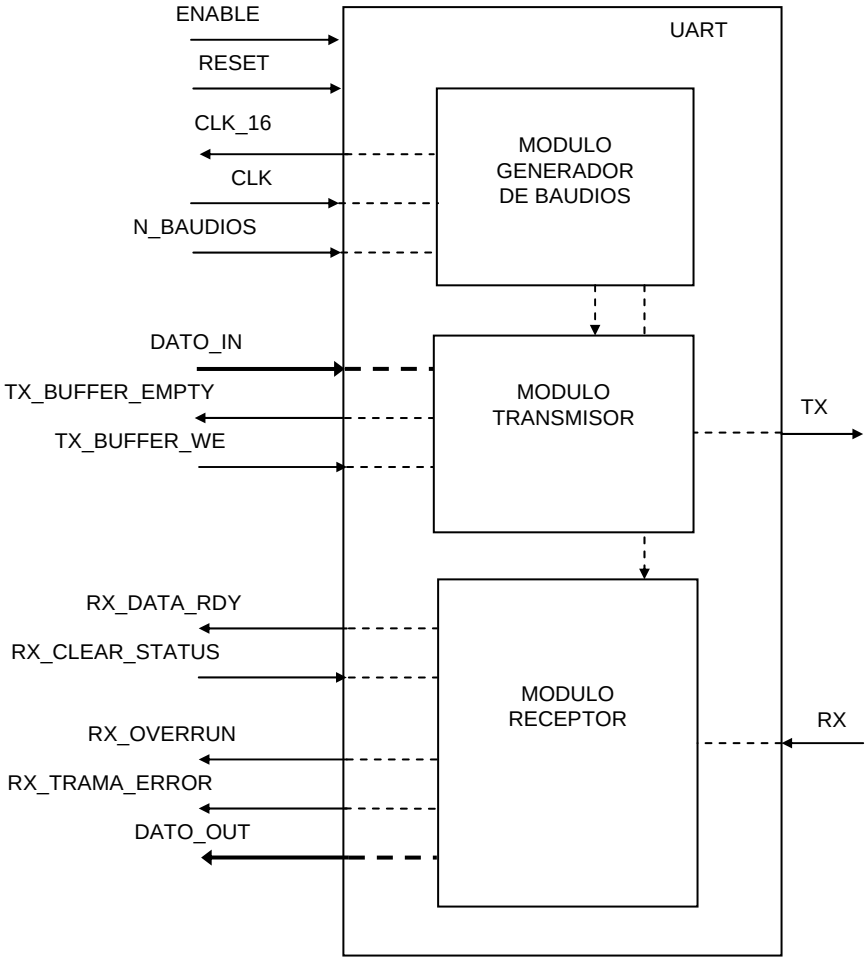
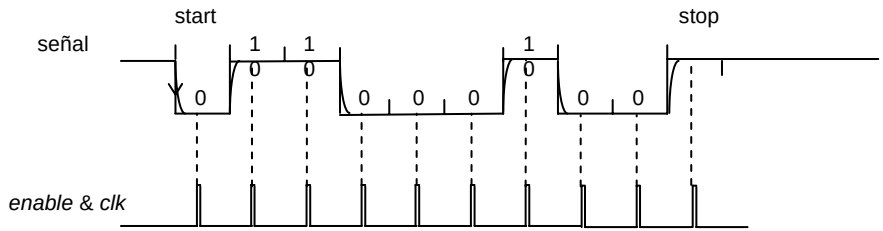


- Muestreo de datos:



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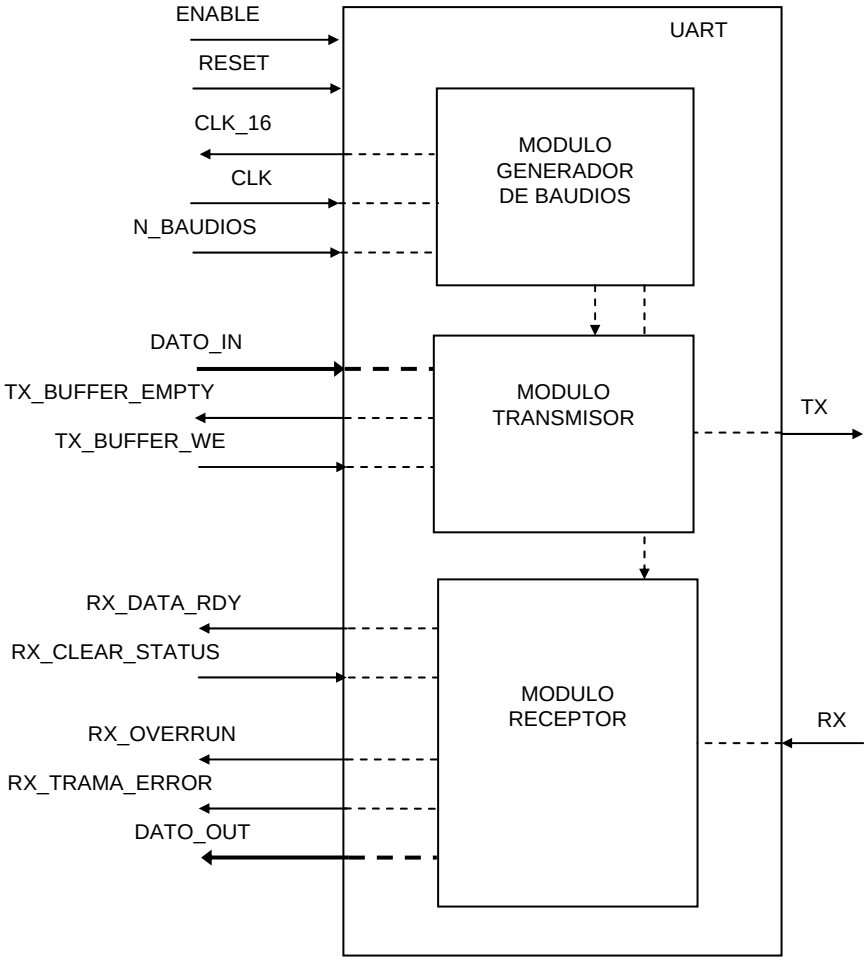

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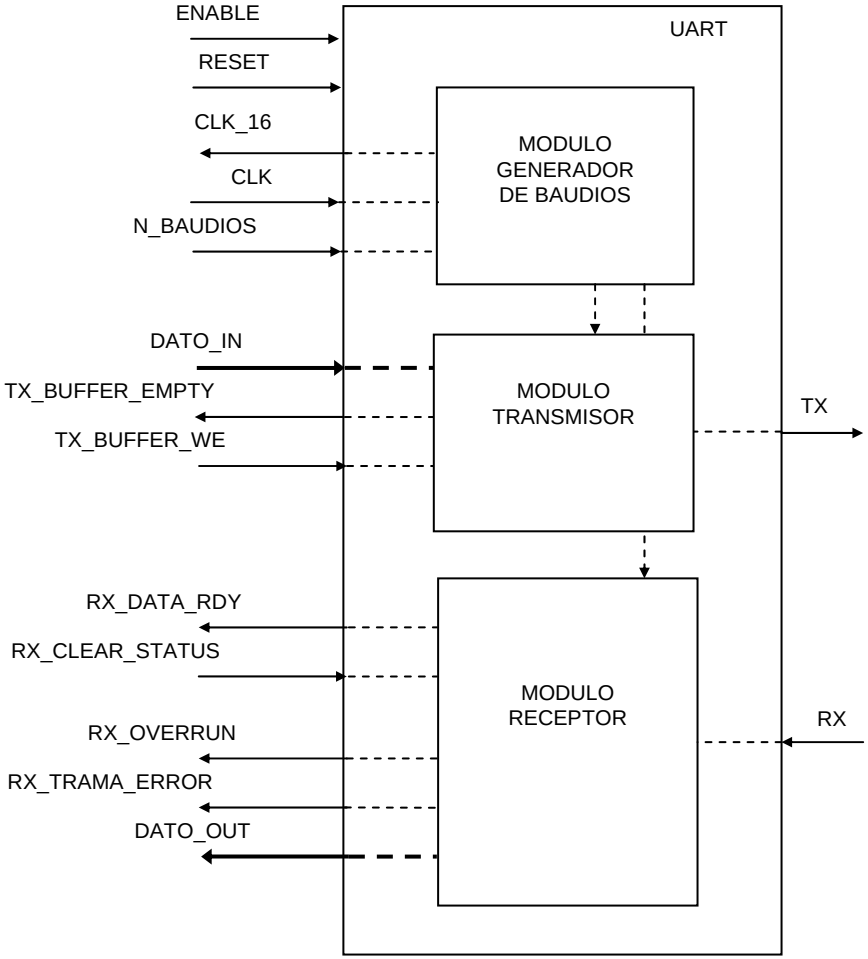
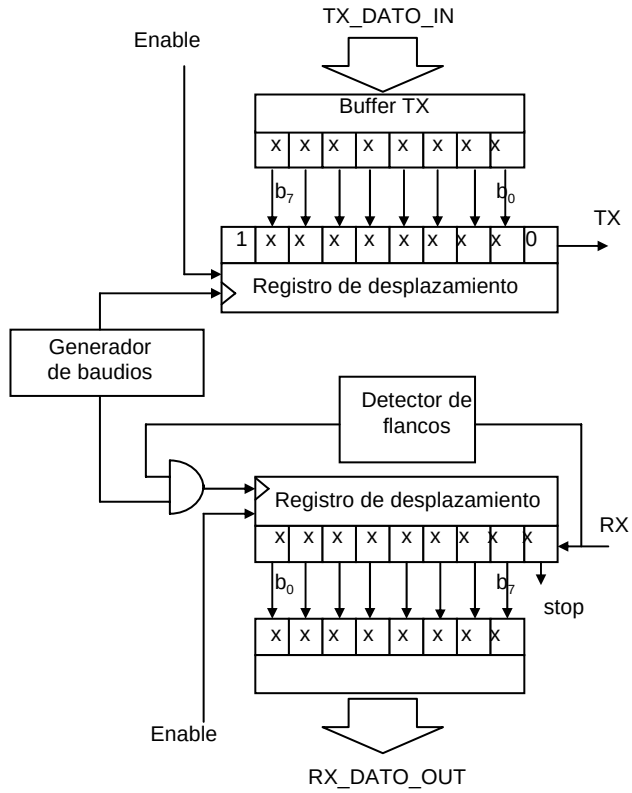
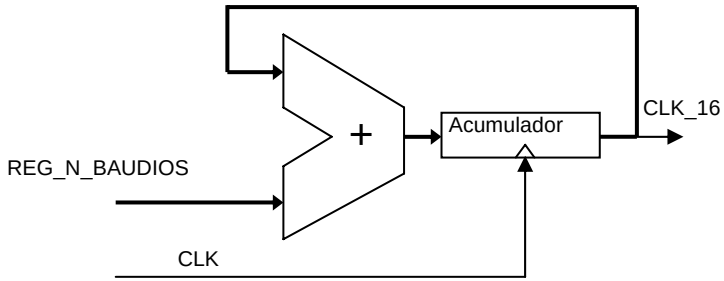


- Funcionamiento:



Módulo generador de baudios



$$REG\_N\_BAUDIOS = \left(2^n \times 16 \times BAUDIOS/frec_{CLK}\right)$$

$$REG\_N\_BAUDIOS = \left(2^{17} \times 16 \times 9600 / 60 \cdot 10^6\right) = 335.5443$$

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$$error\% = \left(\left(9613 - 9600\right) / 9600\right) \times 100 = 0.1354\%$$

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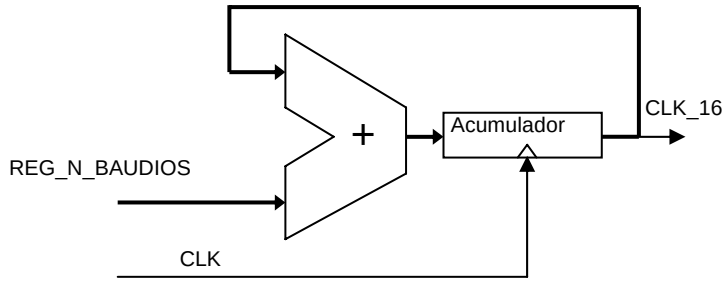

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CLK = 60MHZ, n = 17			
BAUDIOS	REG_N_BAUDIOS (decimal)	BAUDIOS REALES	ERROR %
115200	4027	115213,39	0,012
76800	2684	76789,86	0,013
57600	2013	57592,39	0,013
38400	1342	38394,93	0,013
28800	1007	28810,50	0,036
19200	671	19197,46	0,013
14400	503	14390,95	0,063
9600	336	9613,04	0,136
7200	252	7209,78	0,136
4800	168	4806,52	0,136
3600	126	3604,89	0,136
2400	84	2403,26	0,136
1800	63	1802,44	0,136
1200	42	1201,63	0,136
900	31	886,92	1,454
600	21	600,81	0,136

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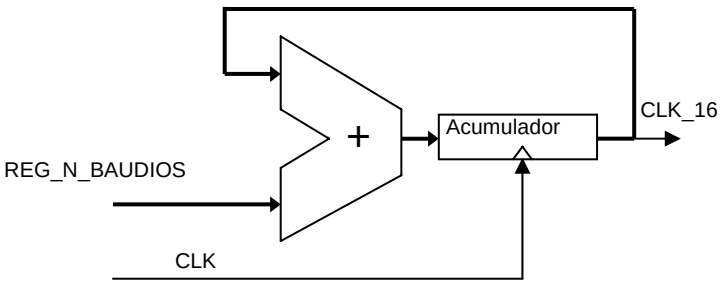
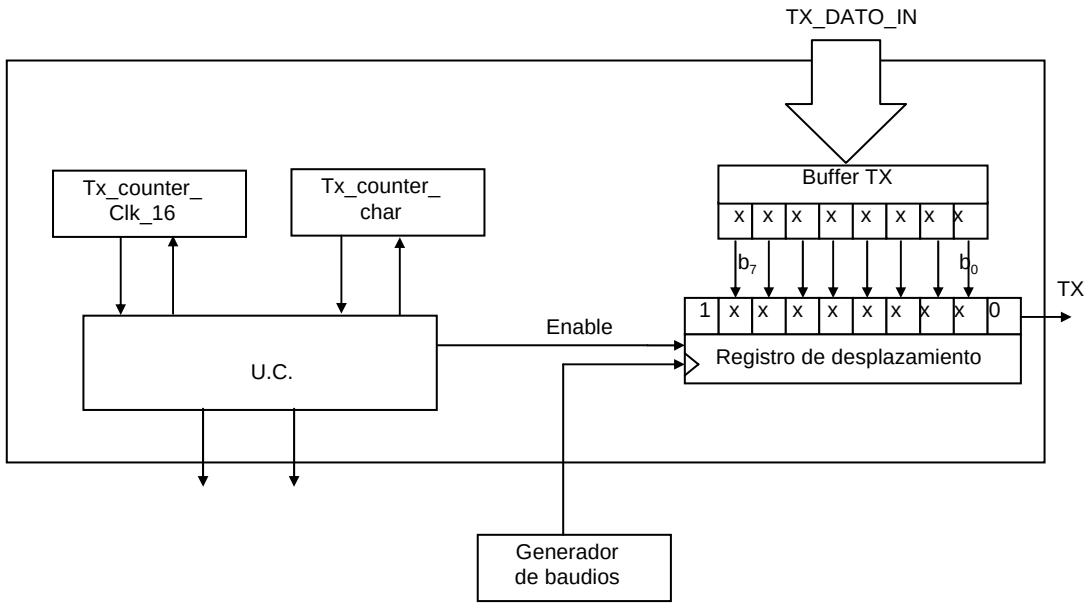
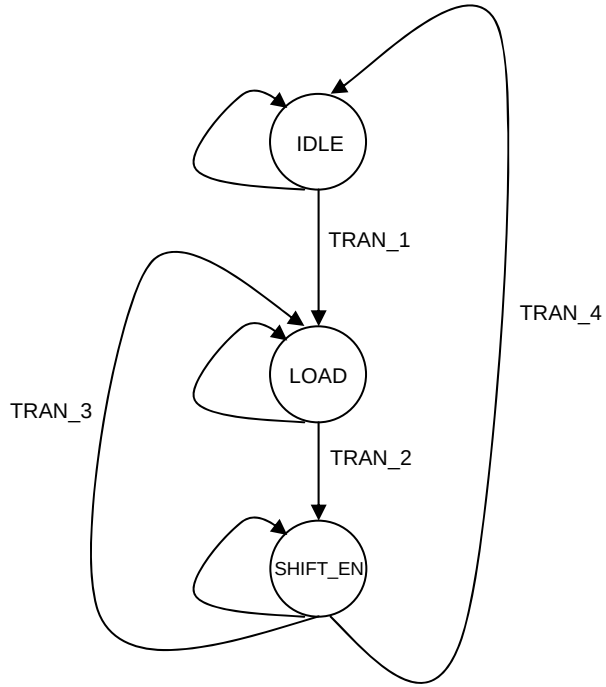


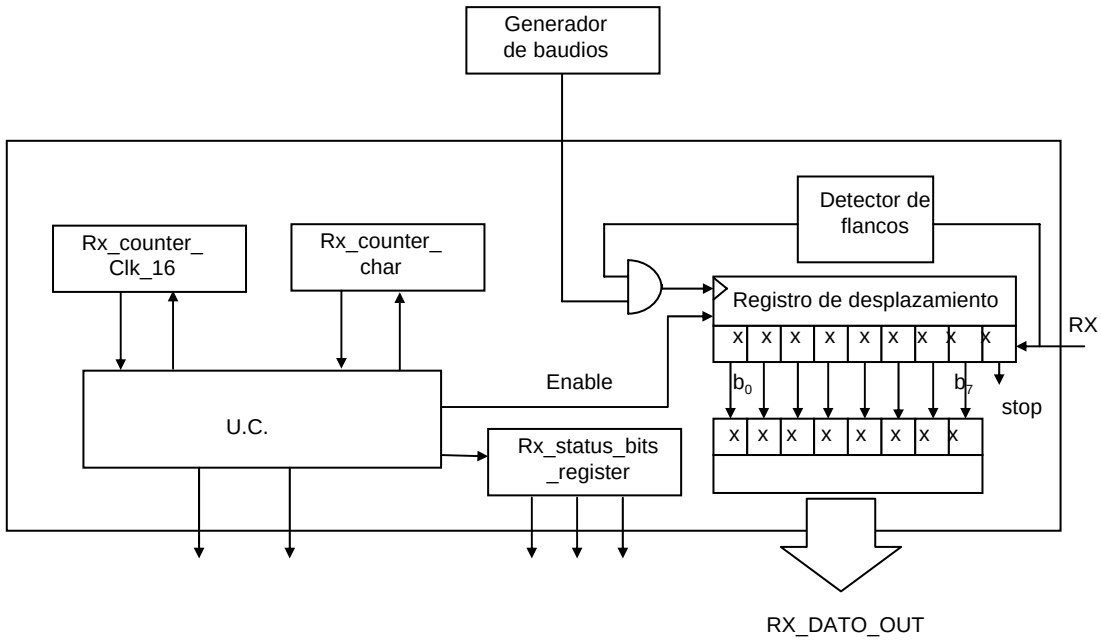

```
--- Generador de Baudios.
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.ALL;

entity generador_baudios is
    Generic ( dimension_acu: integer :=16 );
    Port  ( clk:  in std_logic;
              reset:  in std_logic;
              baudios: in std_logic_vector(15 downto 0);
              clk_16: out std_logic);
end generador_baudios;

architecture arc_generador_baudios of generador_baudios is

    signal acumulador: unsigned( dimension_acu downto 0);
    signal reg_n_baudios: unsigned( dimension_acu downto 0);

begin

    reg_n_baudios(baudios'length-1 downto 0) <= unsigned(baudios);
    reg_n_baudios(dimension_acu downto baudios'length) <= (others => '0');

    gen_baud: process (clk,reset)
    begin
         if (reset='1') then
           acumulador <= (others => '0');
         elsif (clk'event and clk='1') then
           acumulador <= acumulador+reg_n_baudios;
         end if;
    end process;

    clk_16 <= std_logic(acumulador(dimension_acu));

end arc_generador_baudios;
```

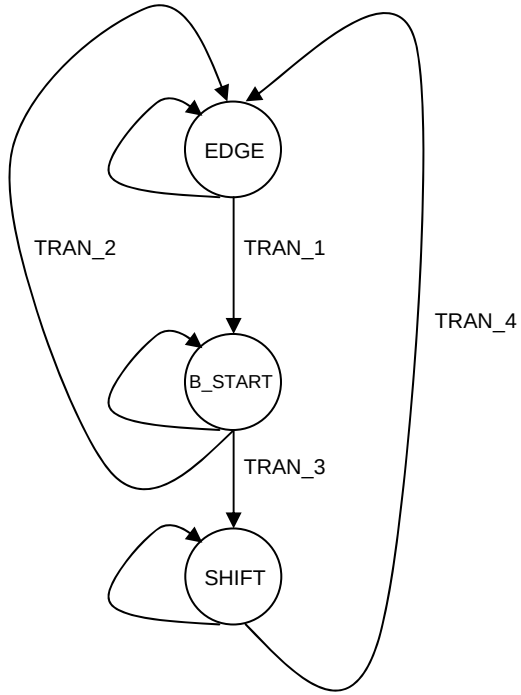
Módulo transmisor





Módulo receptor





Circuito de prueba