Faculty of Science, Engineering and Technology

Computer Systems

Week 4

Overview

In this laboratory session we start look at memory, encoders and stacks.

Purpose: To consolidate your knowledge of Flip Flops, and how they can be used.

Task:

Time: This lab is due by the start of your week 5 lab.

Assessment: This lab is worth 1% (up to a maximum of 5%) of your assessment for this unit, and only if demonstrated to your lab demonstrator in the week it is due.

Resources:

- Counters and Shift Registers:
  - Registers with D Flip Flops
  - Shift Registers with D Flip Flops
  - Ripple Counters (and HEX Display) with J-K Flip Flops

Submission Details

You must submit the following files to Canvas:

- A document containing all required work as described below.

Instructions

1. We are going to build a big-endian 3-bit ripple counter out of JK Flip-Flops. Yep ..I know - exciting! But first:
   - think about what big-endian means - where is the most significant bit going to be ? and what does this mean for the direction of your "ripple" ?
   - Chat with your lab demonstrator if you're not sure.
2. When you're comfortable, start wiring it up. Your counter should count from 000 to 111. Use LEDs to show the output "Q" from each Flip Flop. For this to work, you will also need to set your JK Flip Flops to Trigger with the clock's Falling Edge instead of its Rising Edge (click on each FF and set this in the Attributes Pane).
3. When complete, demonstrate your counter to your lab demonstrator.

Export your circuit as an image and include it in your submission document.

4. Save your circuit (you should always do this !).
5. Now build a big-endian 3-bit "count down" counter, that counts from 111 to 000. Review the week 3 lecture slides to get some hints on this, and discuss your plan with your lab demonstrator if you need to.
6. When complete, demonstrate to your lab demonstrator.

Export your circuit as an image and include it in your submission document.

7. Take your original counter from Step 2 and modify it so it now counts from 0 to 111 using a common clock. That is, each flip flop receives a clock pulse at the same time. Review the lectures if you need to.
8. When you've finished wiring it up, show your lab demonstrator.

Export your circuit as an image and include it in your submission document.

9. Now modify your clock from Step 7 so it counts from 0 to 5 (i.e, MOD 6), and then wraps around back to 0. Think about how you are going to detect the upper limit, and how you are then going to set things back to 0 when you reach 6 (110).

Hint: You will want to use an appropriate gate to detect this, with its output feeding into the re-set pins for the Flip Flops.

10. The circuit in Step 9 goes into a momentary illegal state (i.e, it displays the binary string 110 due to the delay between detection of the limit, and the eventual reset back to 0. In the lecture we discussed using D Flip Flops as a buffer, to hold the output state one extra clock pulse before showing (allowing time for any resetting to occur first).
    - 10.1. Modify your counter so that it resets after 5 (101) back to 0 (000) without the momentary illegal state.
    - 10.2. Why is handling such things important ?

11. Display your counter output using the HEX Digit Display. Note that the Logisim HEX Display uses a single pin input with a 4 bit width. That means a 4 bit integer is expected along a single wire. Because our wires are carrying only 1 bit at a time, we will require a "Splitter" (in reverse) to combine multiple bit streams into a 4-bit "wire bundle" that is fed into the HEX display. See the video tutorial linked at the top of this lab sheet for how to use the splitter to combine single bit streams into a single wire.

Export your circuit for Step 10 and 11 as images and include it in your submission document, along with your answer to 10.2.

When complete:

- Submit your answers (screen shots, etc) in a single document using **Canvas**
- Show your lab demonstrator your working circuits in class (you must do this to get the 1%). Your lab demonstrator may request you to resubmit if issues exist.