# LABVIEW FPGA IDFA FXCHANGE







**IDEA EXCHANGE** 

Search the community

# **Options**

- O Back to Idea Exchange (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas)
- < Previous Idea (/t5/LabVIEW-FPGA-Idea-Exchange/Unsupported-nodes-inside-for-loop-within-SCTL-should-result-in-a/idip/3959814)

Next Idea >

★ (HTTPS://FORUMS.NI.COM/T5/IDEAS/V3/IDEAPAGE.KUDOSBUTTONV2.KUDOENTITY:KUDOENTITY/KUDOSABLE-GID/3894849?T:AC=BLOG-ID/LVFPGAIDEAS/ARTICLE-ID/732&T:CP=KUDOS/CONTRIBUTIONS/



(/t5/user/viewprofilepage/user-id/150310) Math Error in Lattice Bubble Sort in High-Performance FPGA

Developer's Guide 1.1 %

Submitted by \_\_\_\_ Ken Brey (https://forums.ni.com/t5/user/viewprofilepage/user-id/150310) on 02-19-2019 11:56 AM • Comment (/t5/LabVIEW-FPGA-Idea-Exchange/Math-Error-in-Lattice-Bubble-Sort-in-High-Performance-FPGA/idi-p/3894849#comment-on-this)

\* Status: New (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/new)

The document High Performance FPGA Devleoper's (http://www.ni.com/tutorial/14600/en/) guide lists a parallelized bubble sort. I tried this out, and found that it actually doesn't work. This this matrix successfully gets the max value on top, and the minimum value on the bottom, it doesn't completely sort the values between.

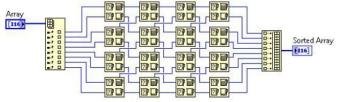
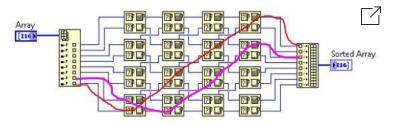


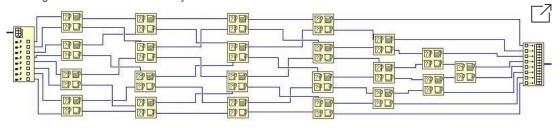


Figure 62. This bubble sort algorithm, implemented in lattice form, leverages partial parallelism and operation associativity to process a fixed size in one clock cycle.

In this example, if the highest value started at the end of the array (red), and the 2nd highest value started 2nd from the end (pink), the high value ends up at the top, and the 2nd highest value ends up 3rd from the top.



This lattice can be completed to sort the middle sections by adding 3 more columns, one with 3 Min/Max blocks comparing the center 6 values, one with 3 Min/Max blocks comparing the center 4, and a final Min/Max operation comparing the middle 2. This will complete the sort, but will take 7 sequential steps instead of the 4 listed. The following works to sort the entire array:





Labels: Analysis & Computation (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/analysis%20%26%20computation)

Execution & Performance (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/execution %20%26%20 performance)

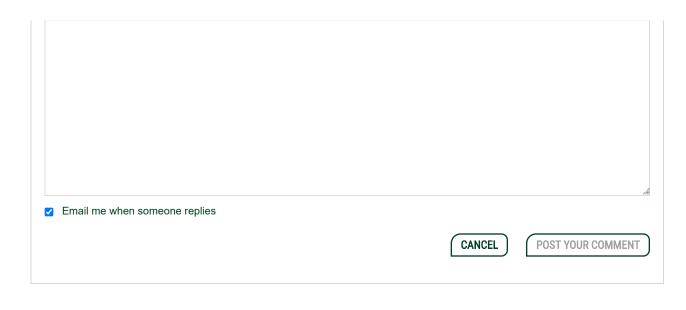
Add tags

VIEW-FPGA-IDEA-EXCHANGE/MATH-ERROR-IN-LATTICE-BUBBLE-SORT-IN-HIGH-PERFORMANCE-FPGA/IDI-P/3894849#COMMENT-ON-THIS)

- O Back to Idea Exchange (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas)
- < Previous Idea (/t5/LabVIEW-FPGA-Idea-Exchange/Unsupported-nodes-inside-for-loop-within-SCTL-should-result-in-a/idi-p/3959814)

Next Idea >





# VIEW IDEAS...

# **Active**

New (http://forums.ni.com/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/new)

Most Recent (http://forums.ni.com/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/tab/most-recent)

Top Kudoed (http://forums.ni.com/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/tab/most-kudoed)

In Development (http://forums.ni.com/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/indevelopment)

In Beta (http://forums.ni.com/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/inbeta)

### Inactive

Completed (http://forums.ni.com/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/completed)

<u>Already Implemented (http://forums.ni.com/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-</u>

key/alreadyimplemented)

<u>Duplicate (http://forums.ni.com/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/duplicate)</u>

<u>Unspecified (http://forums.ni.com/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/unspecified)</u>

# ABOUT LABVIEW FPGA IDEA EXCHANGE



- 1. Does your idea apply to LabVIEW in general? Get the best feedback by posting it on the original <u>LabVIEW Idea Exchange</u> (<a href="http://forums.ni.com/t5/LabVIEW-Idea-Exchange/idb-p/labviewideas">http://forums.ni.com/t5/LabVIEW-Idea-Exchange/idb-p/labviewideas</a>).
- 2. Browse by label or search in the LabVIEW FPGA Idea Exchange to see if your idea has previously been submitted. If your idea exists be sure to vote for the idea by giving it kudos to indicate your approval!
- 3. If your idea has not been submitted click New Idea (http://forums.ni.com/t5/forums/postpage/board-id/lvfpgaideas) to submit a product idea to the LabVIEW FPGA Idea Exchange. Be sure to submit a separate post for each idea.
- 4. Watch as the community gives your idea kudos and adds their input.
- 5. As NI R&D considers the idea, they will change the idea status.
- 6. Give kudos to other ideas that you would like to see in a future version of LabVIEW FPGA!

# Analysis & Computation (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/analysis%20%26%20computation) 14 Compile Process (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/compile%20process) 59 Debugging (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/debugging) 32 Execution & Performance (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/execution%20%26%20performance) 41 HW Connectivity (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/hw%20connectivity) 18 Installation & Upgrade (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/installation%20%26%20upgrade) 2 IP or Function Needs (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/ip%20or%20function%20needs) 29 Simulation (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/simulation) 8 SubVI (IP) reusability (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/simulation) 13 Third party integration & APIs (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/third%20party%20integration%20%26%20apis) 10 UI & Usability (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/label-name/ui%20%26%20usability) 95

# **IDEA STATUSES**

New (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/new) 208

In Development (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/indevelopment) 1

In Beta (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/inbeta) 0

Completed (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/completed) 7

<u>Duplicate (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/duplicate)</u> 1

Already Implemented (/t5/LabVIEW-FPGA-Idea-Exchange/idb-p/lvfpgaideas/status-key/alreadyimplemented) 2

UNREAD TOPICS >

# Unified Functions Palettes (/t5/LabVIEW-FPGA-Idea-Exchange/Unified-Functions-Palettes/idi-p/4083111) 🔄

# Multi-core Compiling (/t5/LabVIEW-FPGA-Idea-Exchange/Multi-core-Compiling/idi-p/1085808)

- [ 1 (/t5/LabVIEW-FPGA-Idea-Exchange/Multi-core-Compiling/idi-p/1085808)
- 2 (/t5/LabVIEW-FPGA-Idea-Exchange/Multi-core-Compiling/idi-p/1085808/page/2)
- 3 (/t5/LabVIEW-FPGA-Idea-Exchange/Multi-core-Compiling/idi-p/1085808/page/3)
- 4 (/t5/LabVIEW-FPGA-Idea-Exchange/Multi-core-Compiling/idi-p/1085808/page/4)
- 5 (/t5/LabVIEW-FPGA-Idea-Exchange/Multi-core-Compiling/idi-p/1085808/page/5)

Improved Search Scope for IO and Memory X-Nodes (/t5/LabVIEW-FPGA-Idea-Exchange/Improved-Search-Scope-for-IO-and-Memory-X-Nodes/idi-p/1228351)

Another way to import the board support configuration (/t5/LabVIEW-FPGA-Idea-Exchange/Another-way-to-import-the-board-support-configuration/idi-p/4081469)

add support for the 903x series of cRIO in LabVIEW NXG (/t5/LabVIEW-FPGA-Idea-Exchange/add-support-for-the-903x-series-of-cRIO-in-LabVIEW-NXG/idi-p/4080982)

# figga (/t5/tag/figga/tg-p/board-id/lvfpgaideas) compile (/t5/tag/compile/tg-p/board-id/lvfpgaideas) bitfile (/t5/tag/bitfile/tg-p/board-id/lvfpgaideas) compilation (/t5/tag/LabVIEW/tg-p/board-id/lvfpgaideas) Loop (/t5/tag/Loop/tg-p/board-id/lvfpgaideas) bitfile (/t5/tag/bitfile/tg-p/board-id/lvfpgaideas) compilation (/t5/tag/compilation/tg-p/board-id/lvfpgaideas) Conditional Disable (/t5/tag/Conditional Disable/tg-p/board-id/lvfpgaideas) Debugging (/t5/tag/Debugging/tg-p/board-id/lvfpgaideas) FIFO (/t5/tag/FIFO/tg-p/board-id/lvfpgaideas) IRQ (/t5/tag/IRQ/tg-p/board-id/lvfpgaideas) LVFPGA (/t5/tag/LVFPGA/tg-p/board-id/lvfpgaideas) MAX (/t5/tag/MAX/tg-p/board-id/lvfpgaideas) recompile (/t5/tag/recompile/tg-p/board-id/lvfpgaideas) sbRIO (/t5/tag/sbRIO/tg-p/board-id/lvfpgaideas) source (/t5/tag/recompile/tg-p/board-id/lvfpgaideas) target (/t5/tag/tag/tg-p/board-id/lvfpgaideas) Immed (/t5/tag/tming/tg-p/board-id/lvfpgaideas) source (/t5/tag/Timing/tg-p/board-id/lvfpgaideas) type (/t5/tag/type/tg-p/board-id/lvfpgaideas) units (/t5/tag/units/tg-p/board-id/lvfpgaideas) 64-bit (/t5/tag/G4-bit/tg-p/board-id/lvfpgaideas) Absolute (/t5/tag/absolute/tg-p/board-id/lvfpgaideas) Duild (/t5/tag/Adapt/tg-p/board-id/lvfpgaideas) Angry\_(/t5/tag/Angry/tg-p/board-id/lvfpgaideas) Atlys\_(/t5/tag/Atlys/tg-p/board-id/lvfpgaideas) build (/t5/tag/build/tg-p/board-id/lvfpgaideas) Build Specification (/t5/tag/Build%20Specification/tg-p/board-id/lvfpgaideas)



### Solutions

Semiconductor (//www.ni.com/en-us/innovations/semiconductor.html) / Automotive (//www.ni.com/en-us/innovations/automotive.html) / Aerospace, Defense, & Government (//www.ni.com/en-us/innovations/aerospace-defense.html) / Academic & Research (//www.ni.com/en-us/innovations/academic-research.html) / Wireless (//www.ni.com/en-us/innovations/wireless.html) / Electronics (//www.ni.com/en-us/innovations/electronics.html) / Energy (//www.ni.com/en-us/innovations/electronics.html) / Energy (//www.ni.com/en-us/innovations/electronics.html) / Heavy Equipment (//www.ni.com/en-us/innovations/transportation-and-heavy-equipment.html) / Partners (//www.ni.com/en-us/partners.html)

## Orders

Order Status and History (//www.ni.com/status/) / Order by Part Number (/en-us/shop/cart) / Activate a Product (//sine.ni.com/myproducts/app/main.xhtml) / Retrieve a Quote (//sine.ni.com/apps/utf8/niwq.retrieve\_quote) / Terms of Service (//www.ni.com/en-us/about-ni/legal/service-terms.html)

# Company

Leadership (//www.ni.com/en-us/about-ni/leadership.html/) / Careers (//www.ni.com/en-us/about-ni/careers.html) / Investor Relations (//investor.ni.com/) / Newsroom (//www.ni.com/en-us/about-ni/newsroom.html) / Corporate Responsibility (//www.ni.com/en-us/about-ni/corporate-responsibility.html) / Supply Chain & Quality (//www.ni.com/en-us/about-ni/corporate-quality.html) / Events (//www.ni.com/en-us/events.html)

### Support

Downloads (//www.ni.com/en-us/support/downloads.html) / Product Documentation (//www.ni.com/manuals/) / Discussion Forums (//forums.ni.com/t5/Discussion-Forums/ct-p/discussion-forums) / Submit a Service Request (//sine.ni.com/srm/app/getassistance) / Site Feedback

(//www.facebook.com/NationalInstruments/)

(//twitter.com/Nlglobal) in (//www.linkedin.com/company/national-instruments/) (//www.youtube.com/nationalinstruments)

© 2020 NATIONAL INSTRUMENTS CORP. ALL RIGHTS RESERVED.

(877) 388-1952 (877) 388-1952

LEGAL (//www.ni.com/en-us/about-ni/legal.html) | PRIVACY (//www.ni.com/en-us/about-ni/legal/privacy-statement.html)

United States (https://www.ni.com/global-gateway?rtrn=https%3A%2F%2Fforums.ni.com%2Ft5%2FLabVIEW-FPGA-Idea-Exchange%2FMath-Error-in-Lattice-Bubble-Sort-in-High-Performance-FPGA%2Fidi-p%2F3894849)