System 0

Core
(AJIT)
1x1x32

AJIT

Master

System bus

Ethernet

sgmii

Network
Inter
face

?

master

Mem
i/face

Mem Controller

MEM
(DRAM)

NIC_0

MAC

Xilinx   NIC

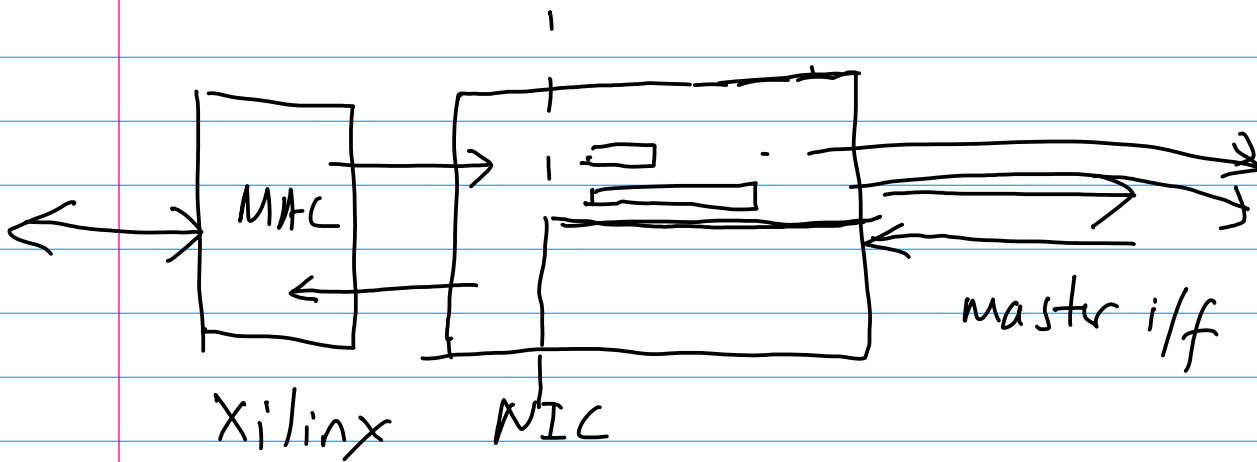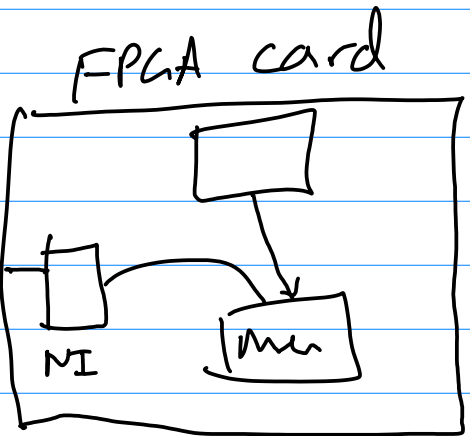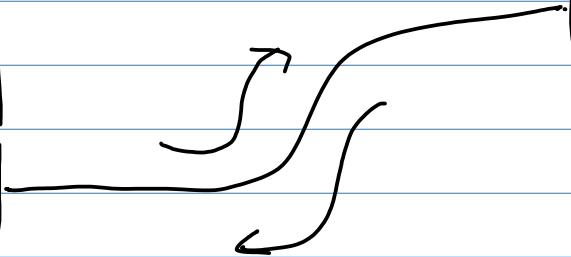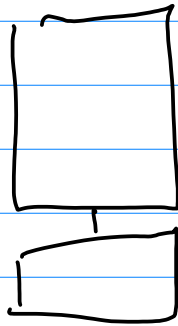mastr i/f

upper
half

① WRITE HEADER
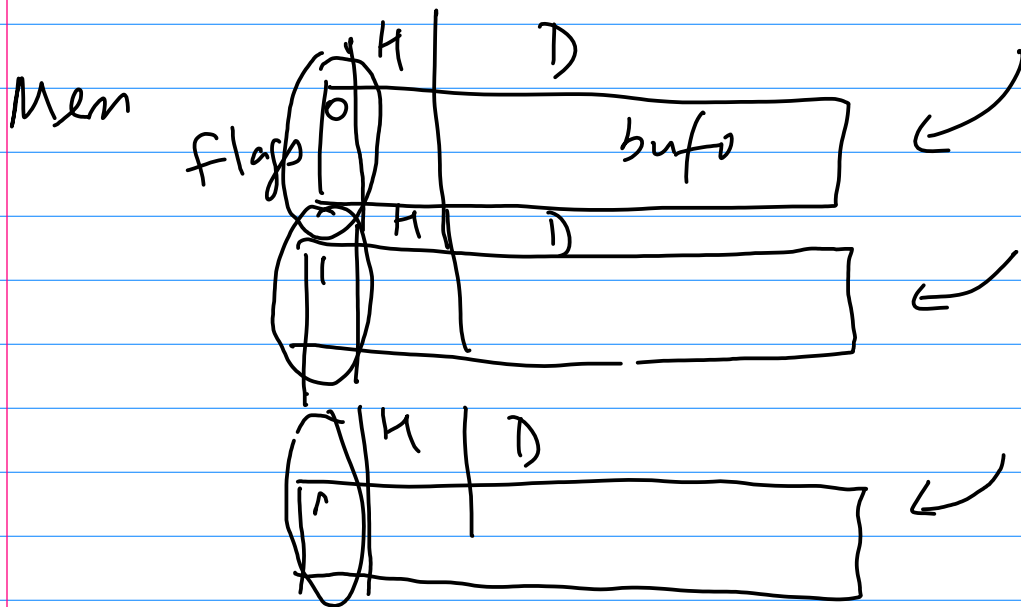② set header flag
③ WRITE PACKET
④ write packet flag
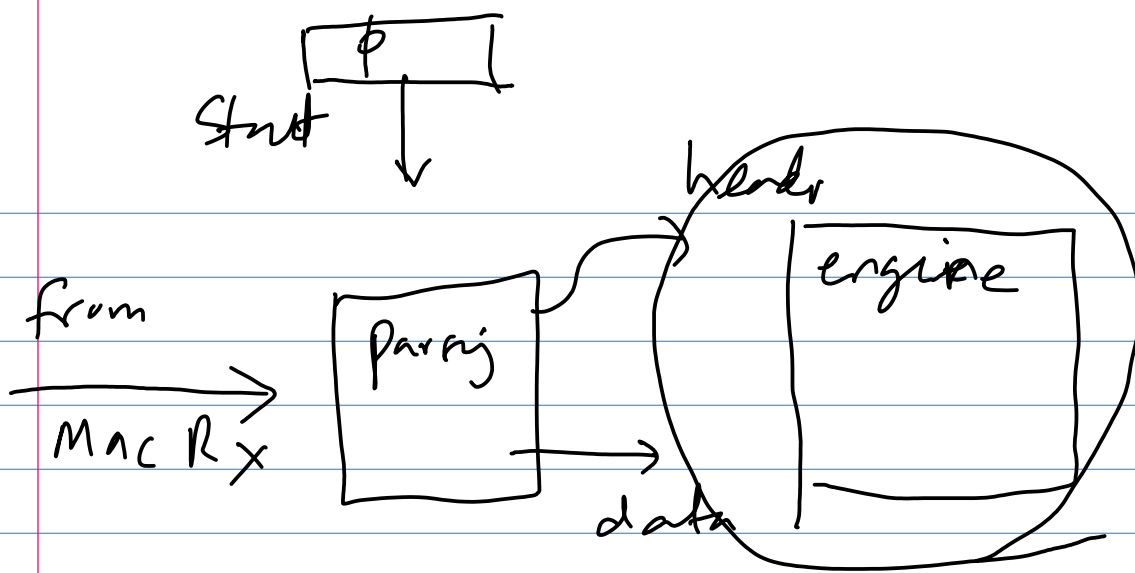
lower
half

poll cpu decision
read back packet
      from mem.
send packet

GOAL_0

demo

FPGA card

MI

Strut

ϕ | 1

from
MAC Rx

Parsg

hdendr

engine

data

Mem

flags

H | D

0 | bufo

H | 1

H | D

r

---

lower
eyie

Mem

| . | | / 0 |

flag   data   → cpu

V_L

fill

modifies

V_R

Decision X / P

$\underline{V_L \quad V_R}$

0   0

MAC
Pkt   fill
rcv   pkt xmitted

1   0
    modifies   cpu pkt redy

1 1

Swap

P1

P2

R

read — lock
write

Mem   R   0   1