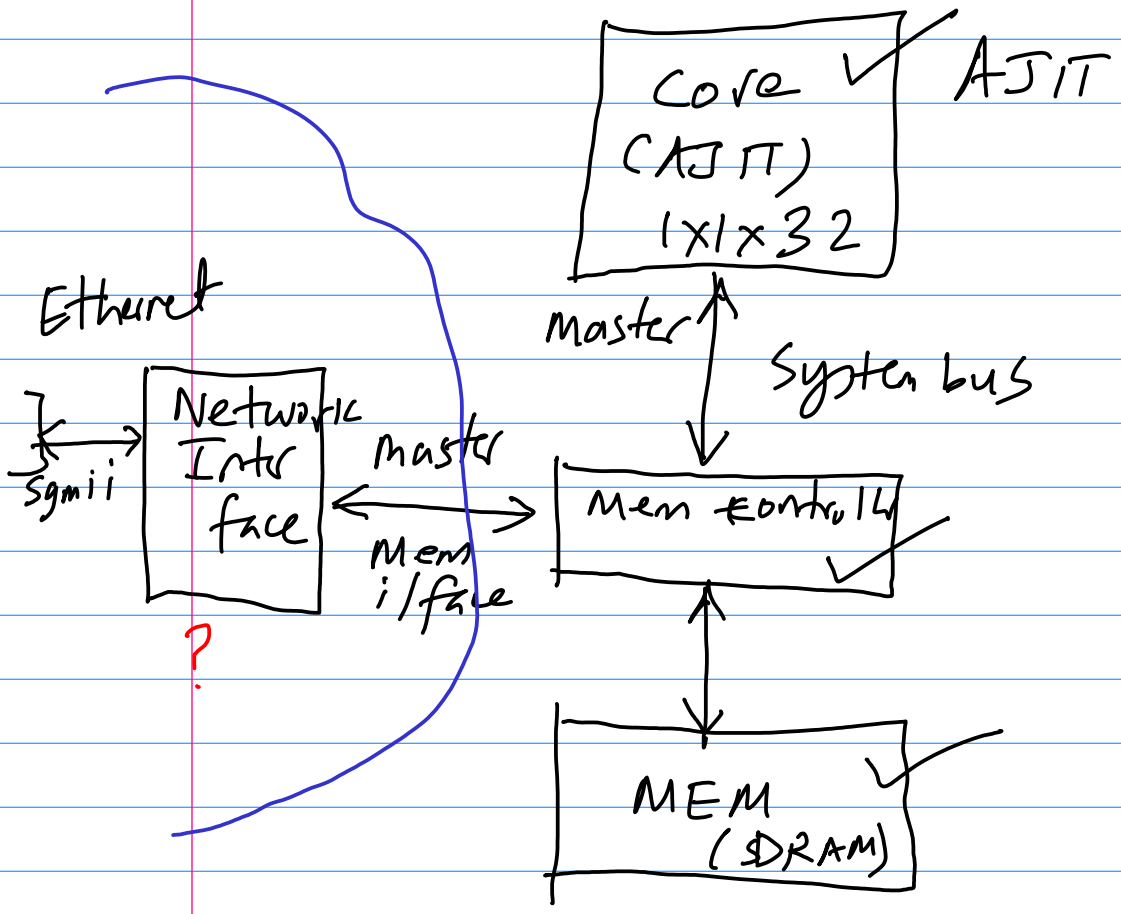
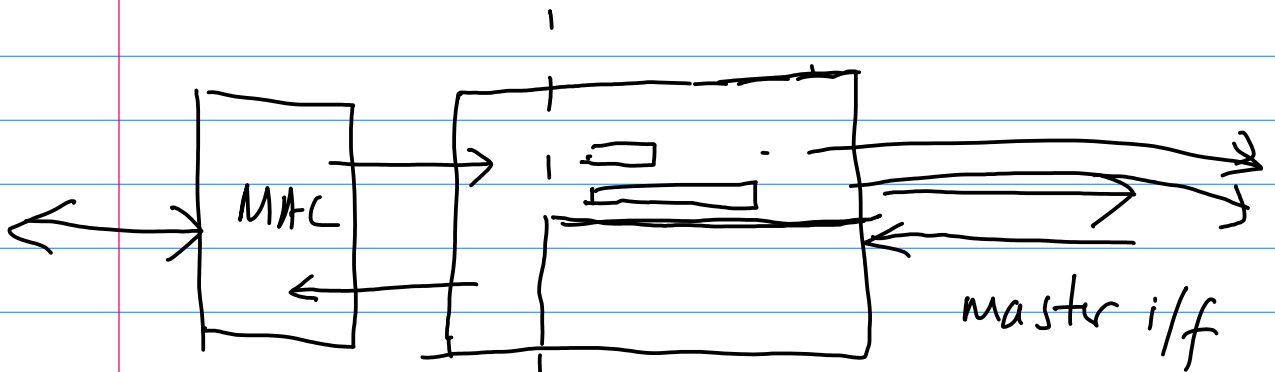
System 0


Core
(AJIT)
1x1x32
AJIT
Master
System bus
Ethernet
Sgmii
Network
Interface
Master
Mem i/face
Mem Controller
MEM
(SDRAM)
?

NIC_0



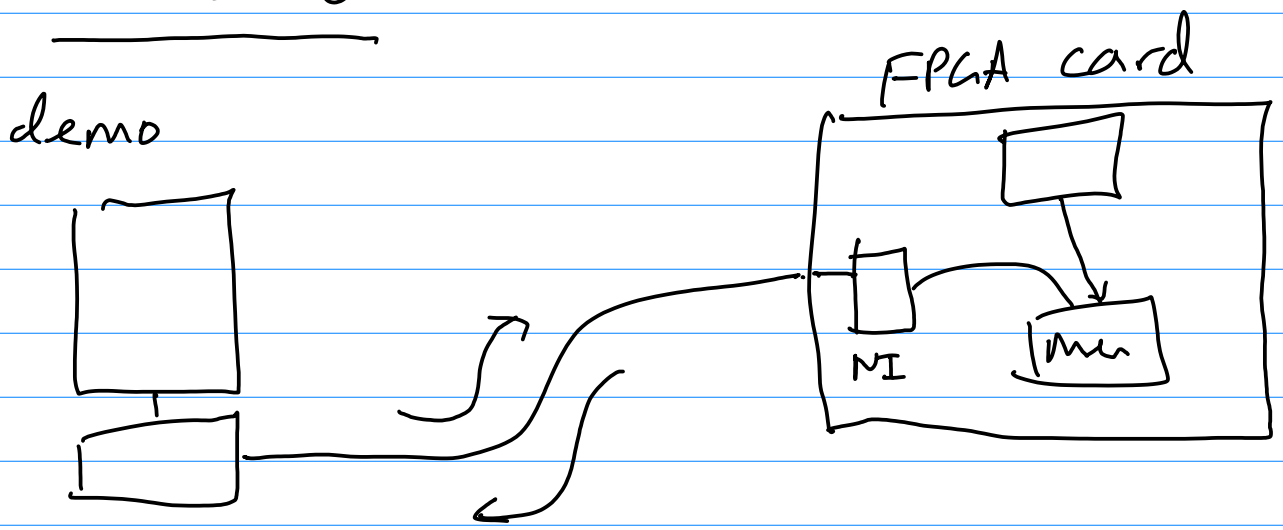
upper half

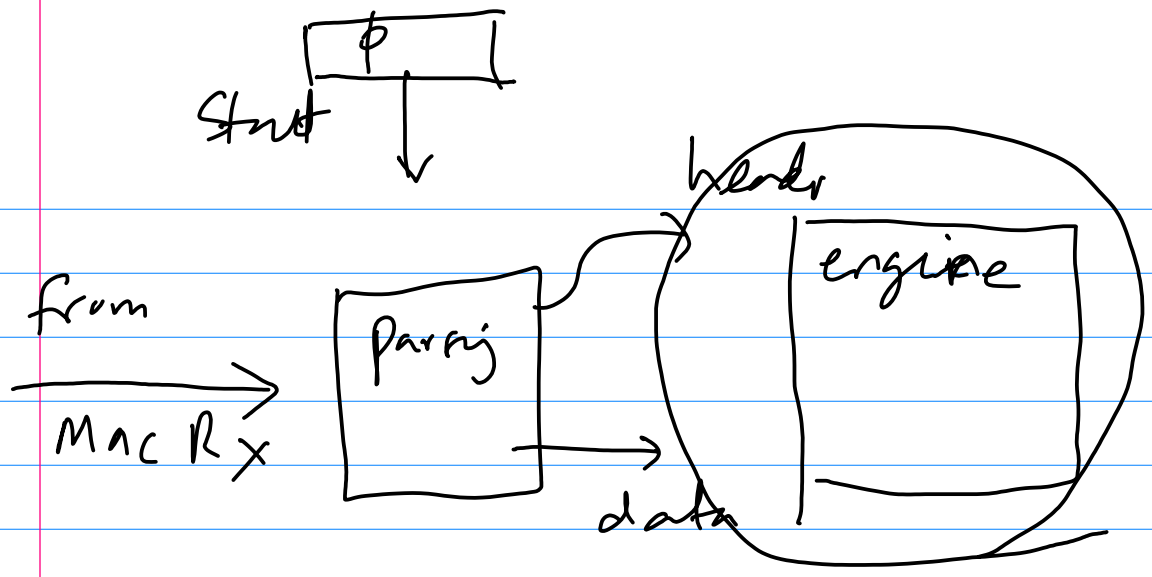
(1) WRITE HEADER
(2) set header flag
(3) WRITE PACKET
(4) write packet flag

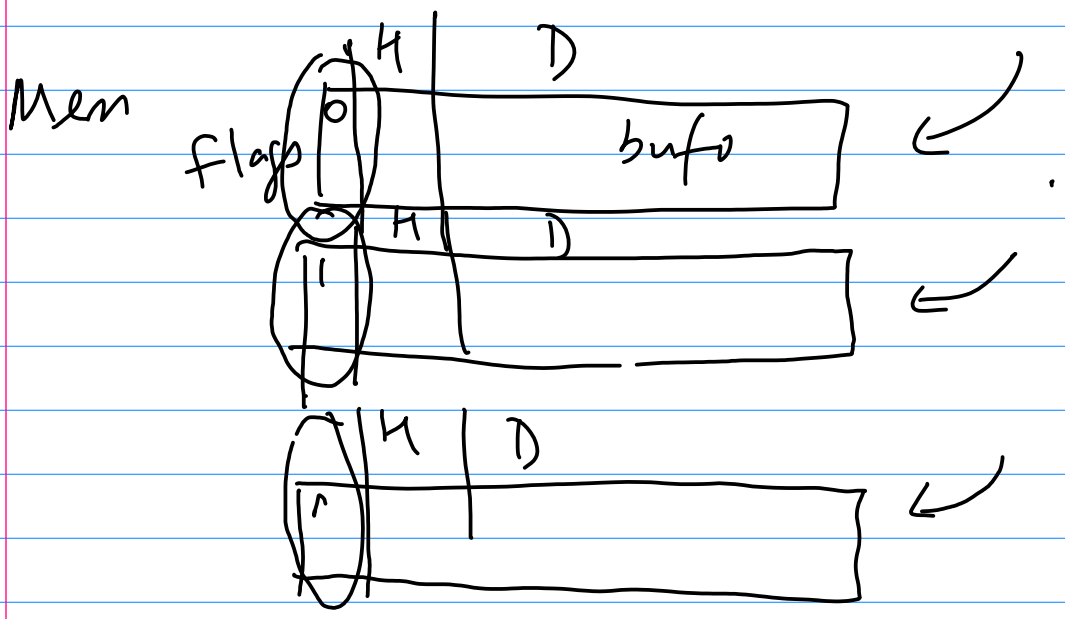
lower half

poll cpu decision
read back packet from mem.
Send packet

GOAL_0



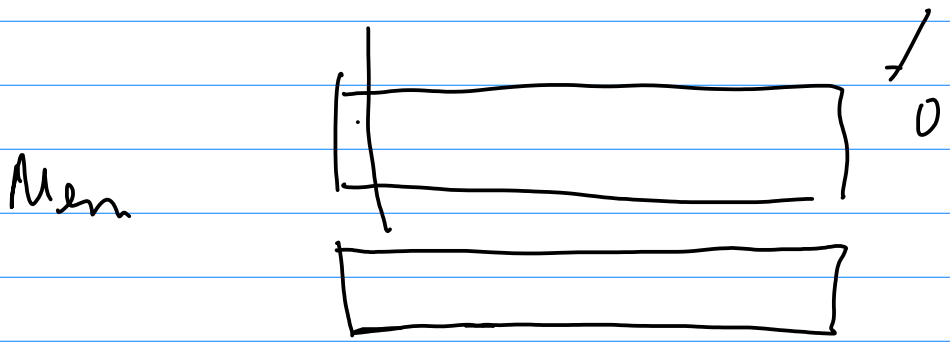

p
Struct
header
engine
from
Mac Rx
Parsj
data

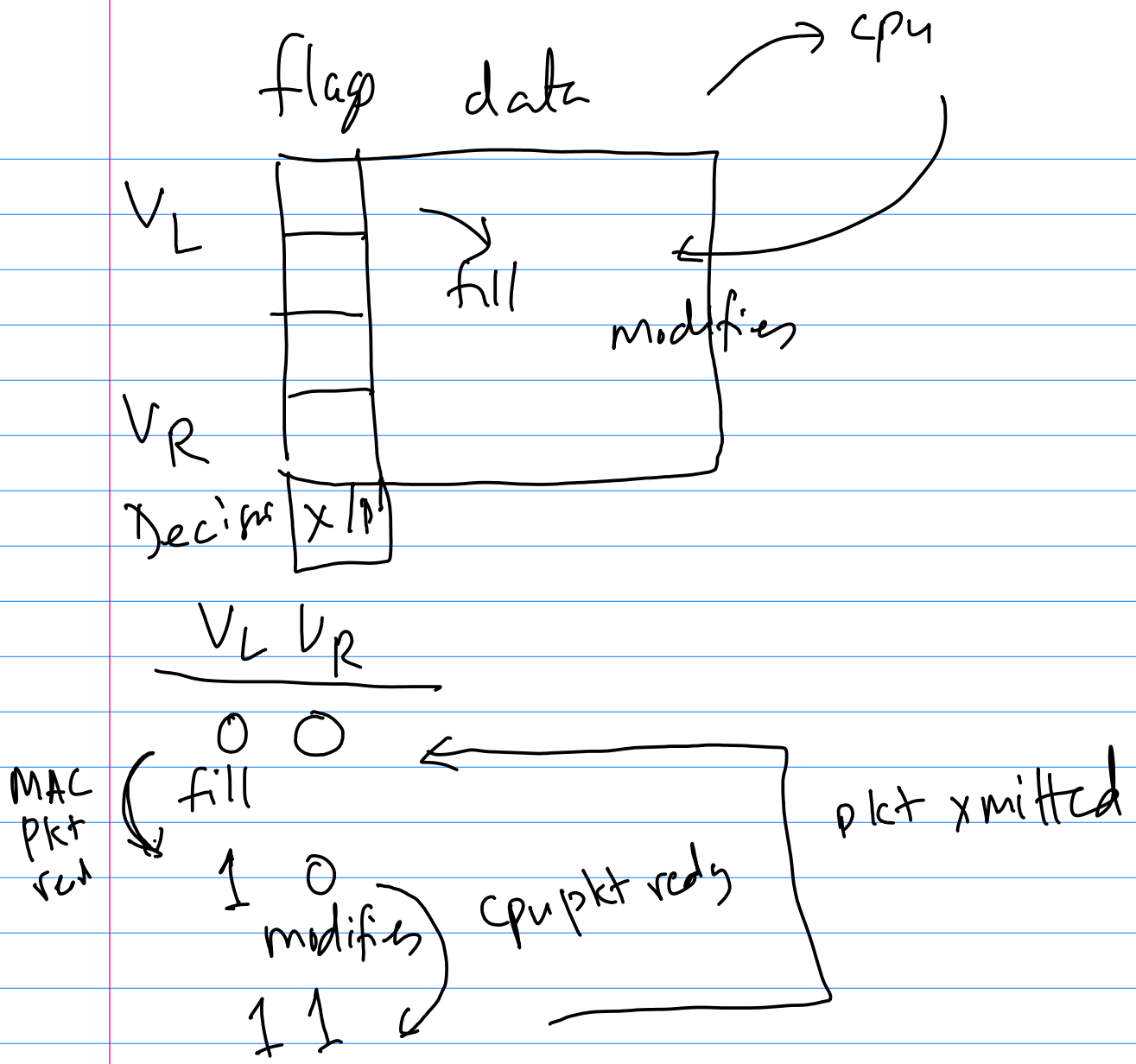

Mem
H
D
flag
0
bufo
H
D
1
H
D
1

---

lower

eye


Mem
0



V_L V_R

0 0

MAC pkt rcvd

fill

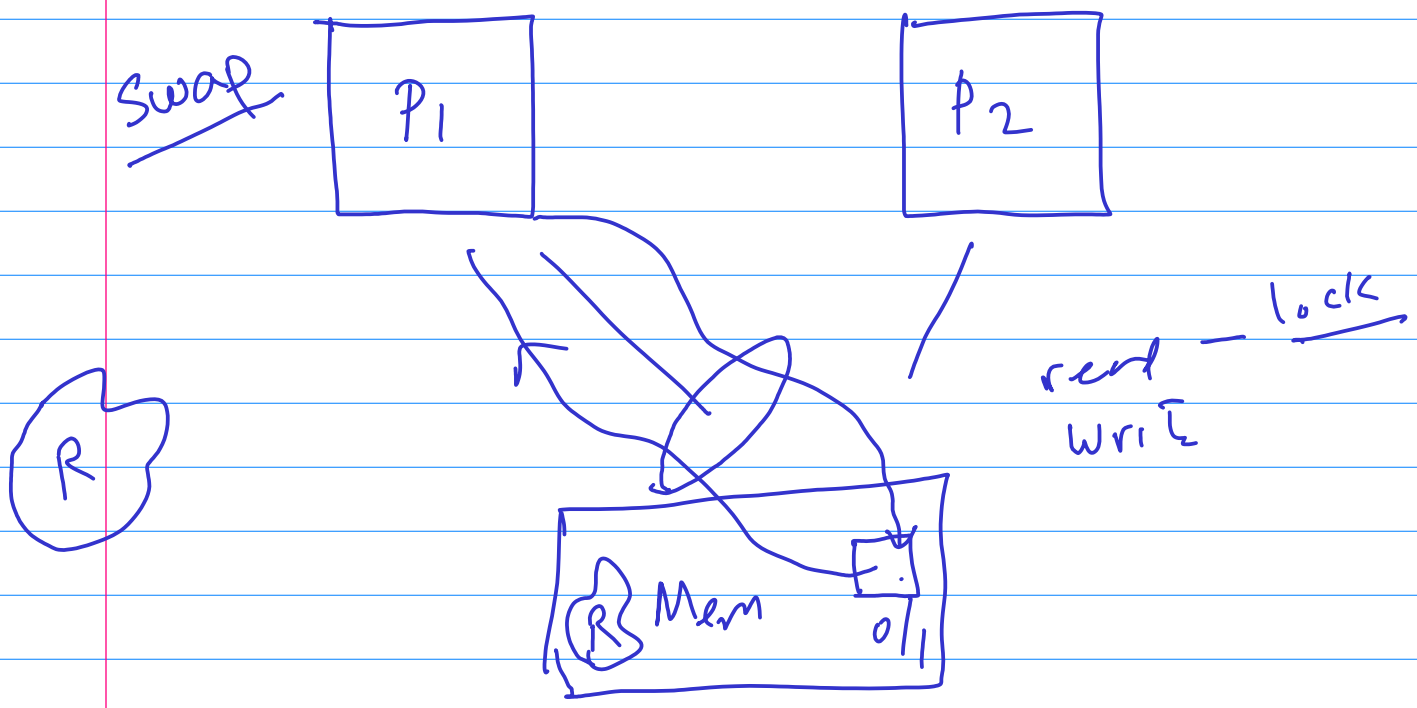
1 0

modifies

1 1

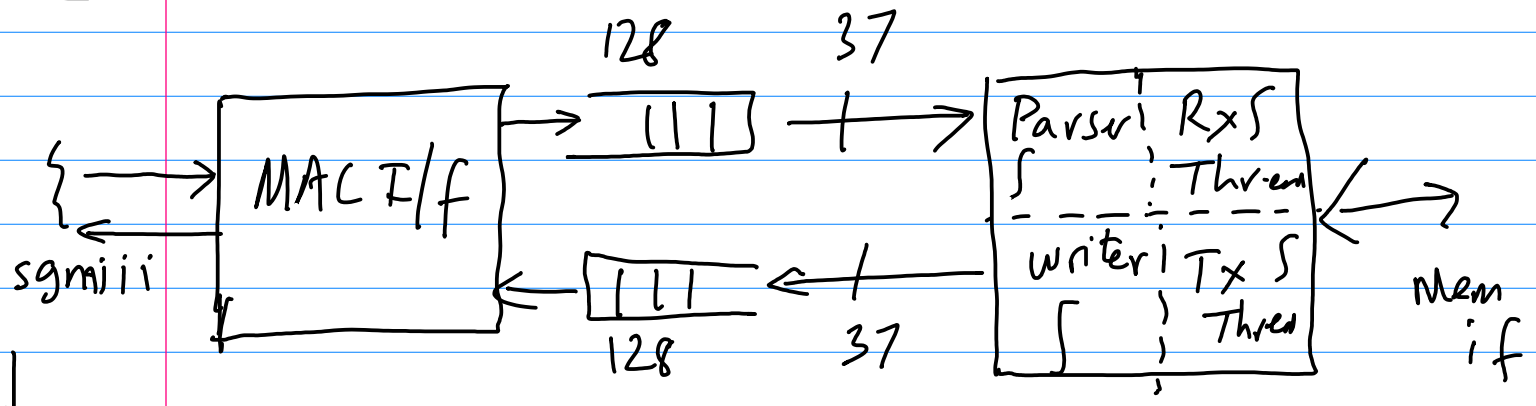
cpu pkt rdy

pkt xmitted


swap
P1
P2
lock
read
write
R
R
Mem
0
1

Ethernet

host



Xilinx IP core?

① MAC/IF 37 bit format [Add Bad]

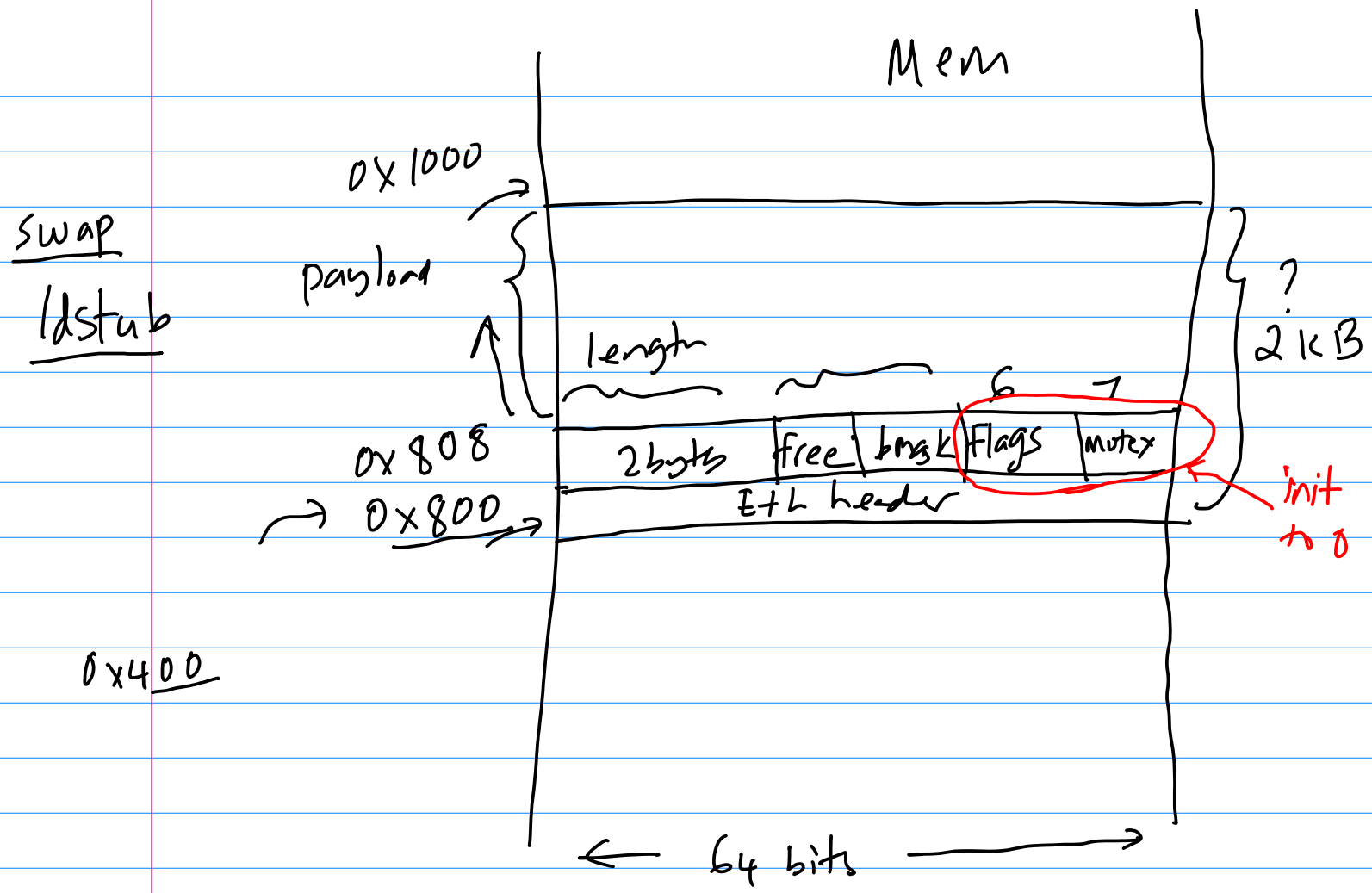
② NiC

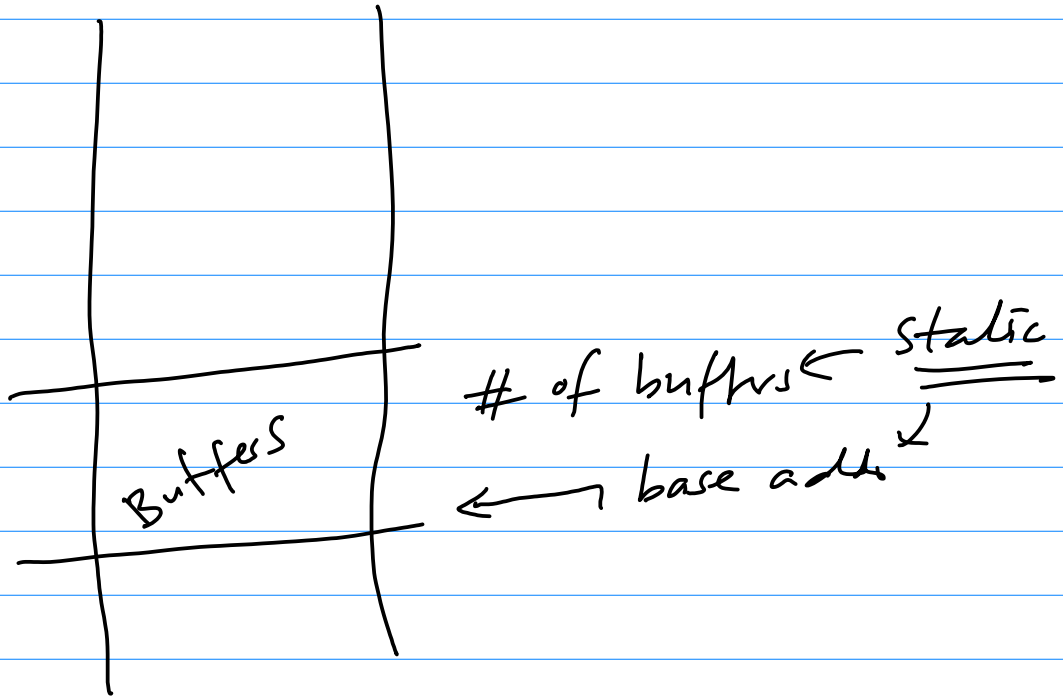
parser: xtract E-header from MAC
data payload fm MAC
forward to Rx

```
Rx:   I ← 0
      while(1)
      {  B ← getBuffr(I)
         fillBuffer(h, payload)
         set flags if pkt ok
      }  I++
```

```
Tx:   I ← 0
      while(1)
      {  checkPktStatus(I)
         if xmit
            Read pkt, header
            Fwd to xmit if
         clear flags, I++
      }
```

```
write
{
   recv 64
   split x2
   send words
      based on last
}
```


Mem
0x1000
swap
ldstub
payload
length
?
2 kB
6
7
0x808
2 bytes
free
break
Flags
mutex
0x800
Eth header
init to 0
0x400
64 bits


Buffers
# of buffers
static
base addr.