Ethernet Interface : For AJIT processor

Harshad Bhausaheb Uagle

Overview

Objective

To provide a faster interface to AJIT processor and eventually providing networking capabilities To AJIT processor.

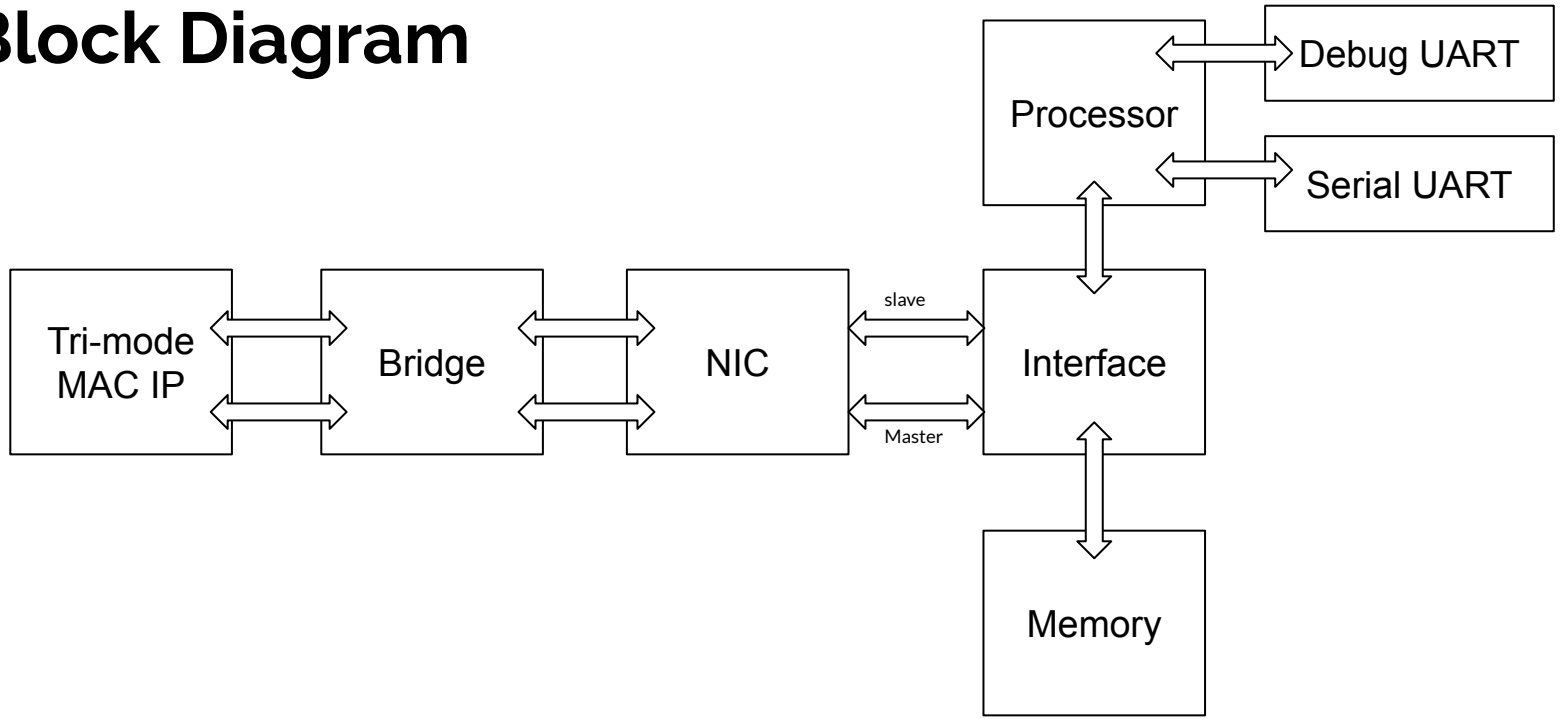
Major Features

- Run time configuration of link speed
- 10Mbps and 100Mbps link speeds

System Overview

- Processor
- Network Interface Card
- Tri mode Ethernet MAC IP
- Memory
- Dual clock fifos and Queues

Block Diagram



Processor and its working

- 1x1x32 AJIT Processor
- Allocates Buffers for storage of packets
- Initialize queues (free,tx,rx)
- Program NIC registers
- Poll rx queue for packet
- Process packet and push to tx queue

Network Interface card (NIC)

- Three Major Daemons
- 64 programmable registers
- Interfaces
  - Data in
  - Data out
  - Master
  - Slave

Tri Mode Ethernet MAC IP

- 10/100/1000Mbps link speeds
- Interfaces
  - AXI-Lite : for link speed configuration
  - AXI serial Rx
  - AXI serial Tx
  - Resets and Clocks

IP generation steps will be given in IP documentation

Queues

1. Free Queue :

   Holds address of Free buffers

2. Rx Queue :

   Holds address of Buffers which are to be processed

3. Tx Queue :

   Holds address of buffers which are processed

NIC Registers

Reg Id	Name	Offset	Function
0	Control	0x00	To Enable NIC (enabled if control[0] == 1)
1	Servers	0x04	Holds number of servers
2 : 9	Rx queue addr	0x08 - 0x24	Holds address of all rx queues
10 : 17	Tx queue addr	0x28 - 0x44	Holds address of all tx queues
18	Free queue addr	0x48	Holds address of free queue
19:63	For Debug	0x4c - 0xfc	For debugging

APIs

To read and write NIC reg value.

```
#define NIC_START_ADDR 0x10000000

uint32_t  NIC_REG = NIC_START_ADDR;

uint32_t readNicReg(uint32_t index); // for reading

void writeNicReg(uint32_t index, uint32_t value);
```

TO DO

- Adding Error check mechanism
- 1000Mbps link

Thank You