A proposal for the development of the networking device for implementation of private 5G networks

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1 Aims and Objective of the Project

The aim of the project is to build a trusted hardware platform which can be configured to form the core of a private 5G network.

Networked devices, and devices that connect to other computing devices are vulnerable to tampering and malicious compromise through both their software and hardware.

In our proposal, we will build a trusted hardware platform around a core technology of the AJIT multi-threaded multi-core processor. This processor has been developed at IIT Bombay, and has been used successfully in the implementation of an IRNSS + GPS base-band receiver system. Innovations such as route caching and packet flow interpreters will be integrated into the fabric of the proposed hardware platform.

Further, the trusted hardware will run software which is completely open to user inspection and oversight. The software is based on open source computations and will be ported to the hardware platform.

2 Novelty of the proposed project

The novelty of the project can be summarized in three ways

- Trust: The key elements in establishing trust are:
  - the identity of the developer institution and personnel, in this case led by IIT-Bombay.
  - the transparency and documentation of the technology.
- Made in India: Implies control over technology, longevity of the technology, cost advantages, independence and spin-offs.

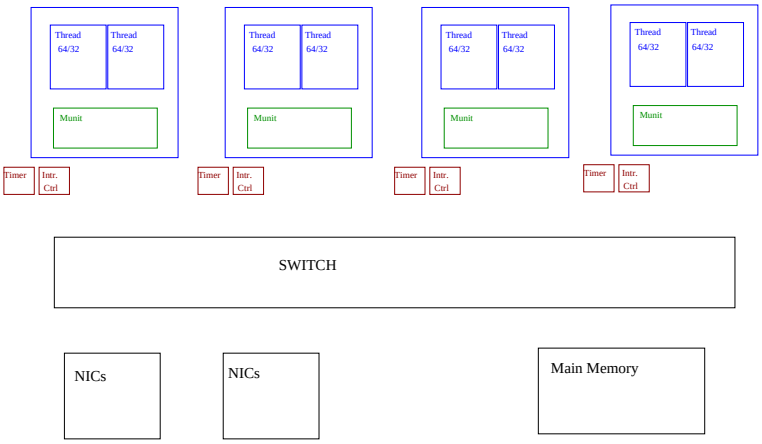

Figure 1: Router platform: phase 1

- Non-proprietary software: Completely auditable, based on open standards, and with source code completely visible and shared.

With that background, we propose a program of developing and deploying private 5G subsystems. Our target deployment is the critical national infrastructure such as military establishments, power grids, refineries, railways, shipyards, ordnance and armament factories, etc.

The hardware for such systems will be based on the work at IIT Bombay. The software will be from Niral Networks who have been developing software-based communication systems.

3 Detailed Description of the project: hardware platform

The project involves the development of a hardware network router using the AJIT multi-threaded multi-core processor, and the porting and customization of software from Niral Networks on to this router.

The hardware network router will be built using a multi-threaded multi-core 64-bit AJIT processor, with four cores and eight threads. The hardware router will be constructed in three phases over an 18 month period.

3.1 Phase 1

In phase 1, a basic router which integrates the multi-core processor with four network interfaces will be built (See Figure 1):

The features of this platform are as follows:

- Vanilla NICs.

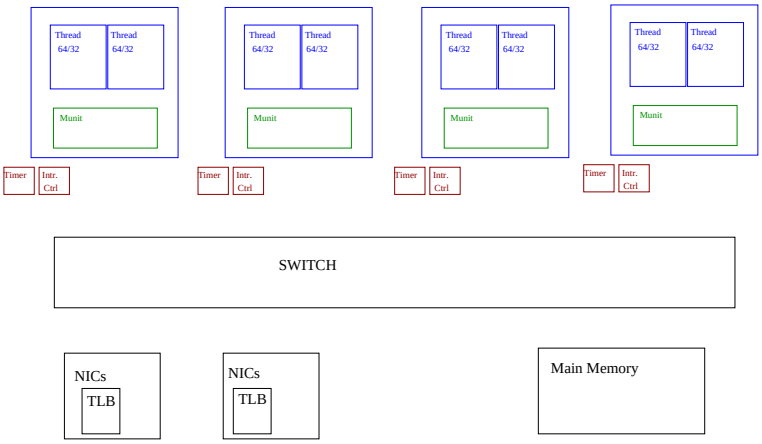

Figure 2: Router platform: phase 2

  - NIC and main memory communicate directly.
  - NIC to NIC direct paths are provided.

- Processor cores handle route lookup.
- Software optimization.

3.2 Phase 2

In phase 2 (see Figure 2, the router will be enhanced with the following features:

- NICs with lookup caches.
  - NIC and main memory communicate directly.
  - NIC to NIC communication is possible using common switch.
  - On lookup cache hit, NIC to NIC packet movement.
  - Packet modification in NIC.
- Processor cores handle non-hit route lookups.

These enhancements aim at a 5X improvement over the Phase 1 router.

3.3 Phase 3

In the phase 3 router, further enhancements will be incorporated into the router platform.

- NICs with lookup caches and embedded EBPF interpreter.
  - NIC and main memory communicate directly.

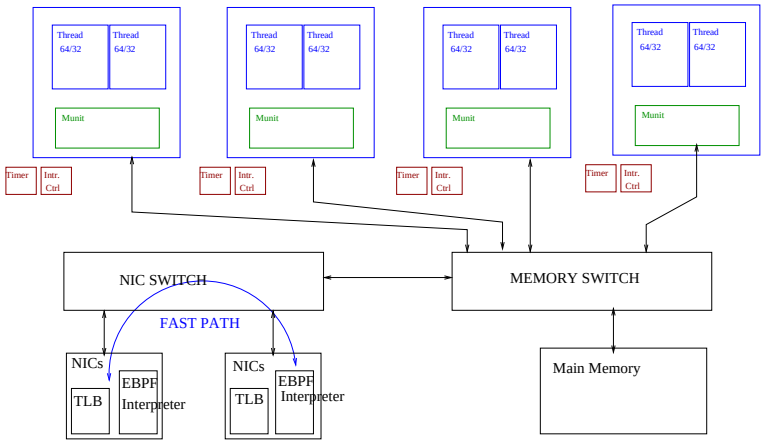

Figure 3: Router platform: phase 3

  - NIC to NIC high performance direct paths are provided via separate switch.
  - Packet processing in NIC using EBPF interpreter.
  - On lookup cache or interpreter hit, NIC to NIC packet movement.
- Processor cores handle remaining route lookups.

As a result of these enhancements, we target a 5X performance improvement over the Phase 2 router.

3.4 Development process

- Phase 1 (6 months): port forwarding engine to 4-core 8-thread platform with vanilla NICs.
- Phase 2 (6 months): Control plane software port, add TLBs to NICs.
- Phase 3 (6 months): MPLS software port, add BPF interpreter to NICs.
- On FPGA platform, demonstrate 1.6Gbps on Stage 1, 8 Gbps on Stage 2, 16 Gbps on Stage 3.
- After FPGA validation, implement router ASIC (22nm, 1.2GHz, 10W). Implementation will take 6-9 months.
  - Target 100-200 Gbps in ASIC based router.

4 Detailed Description of the project: software platform

The software platform will be Release-15 compliant 5G Core for Private 5G Deployment, with support for

- User Plane Private 5G Network Functions: UPF
- IPv4, IPv6, MPLS and L3-VPN Forwarding.
- Private 5G Control Plane functions: AMF, SMF, AUSF.
- Routing Protocols like OSPF, ISIS, BGP, LDP

The software platform will be developed in two phases.

4.1 Phase 1

Integrate the User Plane of 5G Core and IP MPLS Router in the AJIT Hardware. At this point, the platform contains the 5G UPF and IP/ MPLS Packet Forwarding.

4.2 Phase 2

Integrate the Control Plane of 5G Core and IP MPLS Router in the AJIT Hardware. So, it contains the 5G control plane component such as SMF, AMF, AUSF, etc. and the IP/ MPLS Routing Protocols.

4.3 Prototype deployment

A prototype 5G router platform will be deployed on the FPGA platform of the hardware outlined above. Use plane processing will be deployed as part of phase 1, and control plane processing as part of phase 2.