

# Fixed-Point MAC Peripheral Design Proposal

## Design Specification

Our team proposes to design a fixed-point Multiply-Accumulate (MAC) peripheral specifically optimized for the 8-bit RISC CPU architecture. This peripheral will enhance the computational capabilities of the base CPU by providing hardware acceleration for multiplication and accumulation operations.

### Key Design Features:

- Implementation of an  $8 \times 8 \rightarrow 16$ -bit fixed-point MAC unit with **multi-cycle operation**
- Custom memory-mapped interface with optimized register layout
- Configurable accumulator behavior with saturation protection
- Status flags for operation completion and overflow detection
- Debug output ports for real-time monitoring

## System Implementation

### MAC Architecture

Our MAC implementation will feature:

1. **Enhanced Input Buffering:** Dual-buffered input registers that enable pipelined operation by allowing new operands to be loaded while the current multiplication is still in progress. This allows back-to-back MAC operations with minimal latency between operations.
2. **Configurable Accumulation Modes:**
3. Standard mode:  $\text{acc} += A \times B$
4. Clear-and-multiply mode:  $\text{acc} = A \times B$
5. Saturating accumulation to prevent overflow
6. **Status Register:** Provides operation status including overflow flag and ready signal

7. **Operation Latency:** Exactly 2 clock cycles from start signal to result availability

## Fixed-Point Number Format

Our MAC peripheral will implement the following fixed-point format:

- **Input Format:** Q7.0 (8-bit signed integers)
  - 1 sign bit + 7 magnitude bits
  - Range: -128 to +127
- This format maximizes the dynamic range while maintaining compatibility with the 8-bit CPU architecture
- **Accumulator Format:** Q15.0 (16-bit signed integers)
  - 1 sign bit + 15 magnitude bits
  - Range: -32,768 to +32,767
- Provides sufficient headroom for accumulating multiple products without overflow
- **Saturation Logic:** When enabled, results exceeding the 16-bit range will saturate at the maximum/minimum values rather than wrapping around

## CPU Interface Protocol

The MAC peripheral interfaces with the 8-bit RISC CPU through a simple memory-mapped protocol:

### 1. Handshake Mechanism:

2. The CPU initiates operations by writing to the control register with the start bit set
3. The MAC peripheral asserts the ready signal when computation is complete
4. The CPU can poll the ready signal by reading the status register (bit 7 of 0xF4)
5. No interrupt mechanism is implemented; the CPU must poll the ready signal

### 6. Data Transfer:

7. Standard memory-mapped writes for input data and control
8. Standard memory-mapped reads for results and status
9. No DMA or burst transfer modes are supported

### 10. Timing Requirements:

11. The CPU must wait for the ready signal before reading results
12. The CPU can load new operands while an operation is in progress

13. The CPU must set the start bit to begin a new operation

## Memory-Mapped Interface

Our memory map design uses five addresses:

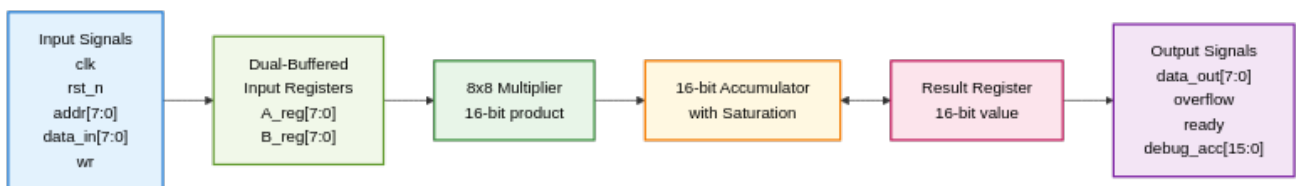
- 0xF0: Input Register A (write-only)
- 0xF1: Input Register B (write-only)
- 0xF2: Control Register (bit 0: start, bit 1: reset, bit 2: mode select)
- 0xF3: Result Low Byte (read-only)
- 0xF4: Result High Byte and Status Flags (read-only, bits 0-6: high byte bits 6-0, bit 7: overflow)

## Dual-Buffered Operation

The dual-buffered input design enables efficient pipelined operation:

1. While the MAC unit is processing the current operation, new A and B values can be written to the input registers
2. Once the current operation completes (ready signal asserts), setting the start bit will begin the next operation immediately
3. This allows for continuous operation with a throughput of one MAC operation every 2 cycles after the initial latency

## Block Diagram



## I/O Definition Table

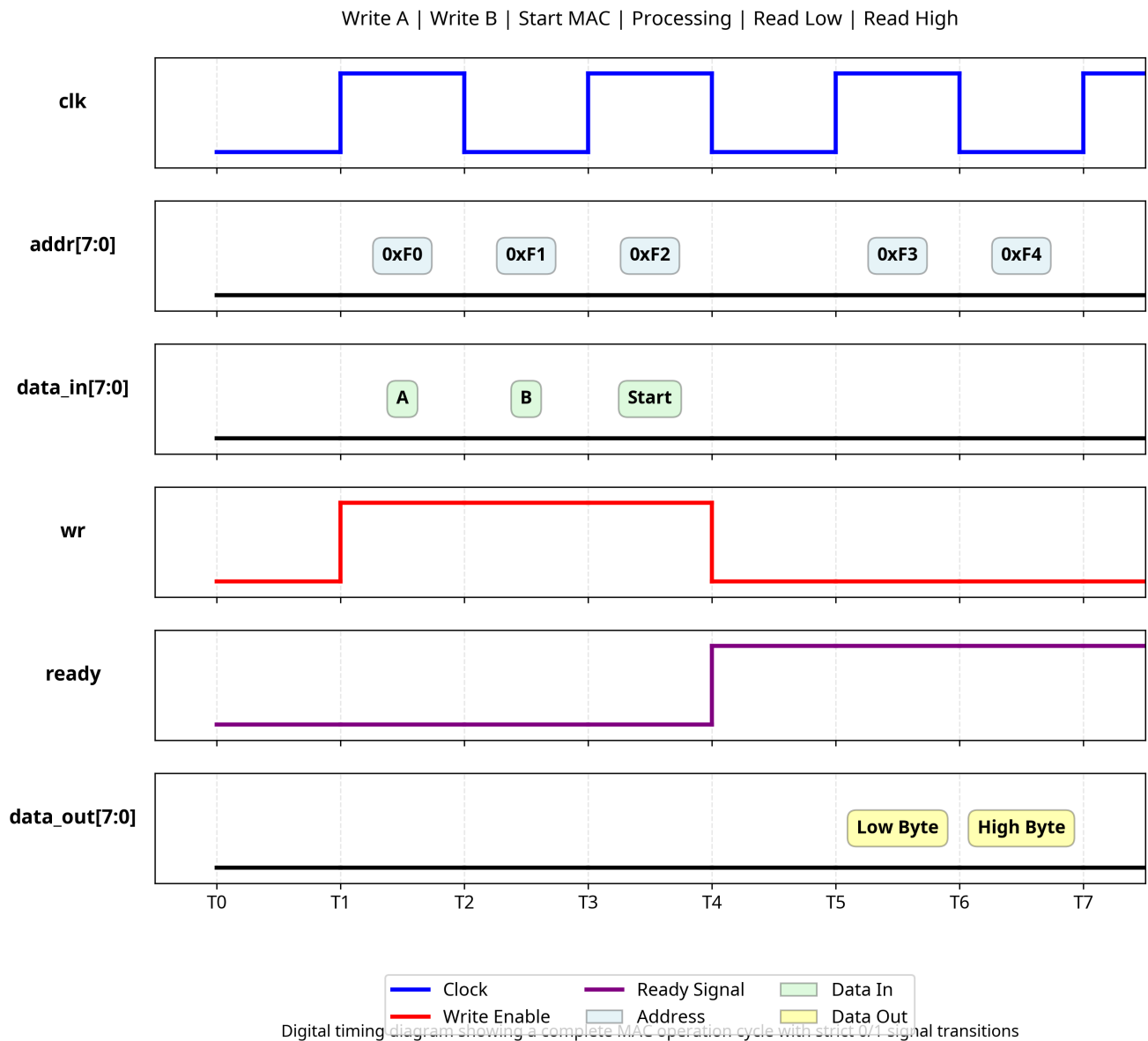
Signal Name	Direction	Width (bits)	Description
clk	Input	1	System clock (max 50MHz)
rst_n	Input	1	Active-low global reset from TinyTapeout
addr	Input	8	Address bus

Signal Name	Direction	Width (bits)	Description
data_in	Input	8	Data input bus
wr	Input	1	Write enable
data_out	Output	8	Data output bus
overflow	Output	1	Overflow indicator
ready	Output	1	Result ready flag (asserts when computation is complete)
debug_acc	Output	16	Debug: Current accumulator value

## Timing Diagram

The following timing diagram illustrates the key time events in our MAC peripheral design:

## MAC Peripheral Timing Diagram



The diagram shows a complete MAC operation cycle:

1. CPU writes operand A to register 0xF0
2. CPU writes operand B to register 0xF1
3. CPU writes to control register 0xF2 with start bit set
4. MAC unit processes the operation (multiplication and accumulation) over exactly 2 clock cycles
5. Ready signal asserts when result is available
6. CPU reads result low byte from register 0xF3
7. CPU reads result high byte from register 0xF4

# Test Plan

## Key Function Tests

1. **Core MAC Operation**
2. Test basic multiplication with positive and negative inputs
3. Verify 2-cycle latency from start signal to ready signal
4. Confirm correct result reading sequence (low byte then high byte)
5. **Accumulation Modes**
6. Verify standard accumulation mode ( $\text{acc} += A \times B$ )
7. Test clear-and-multiply mode ( $\text{acc} = A \times B$ )
8. Confirm saturation behavior with large values
9. **Control and Status**
10. Validate ready signal assertion timing
11. Test overflow detection with boundary values
12. Verify reset functionality

## Test Implementation

- Simple Verilog testbench focusing on key functions
- Results will be visually verified through waveform analysis