MANCHESTER 1824
The University of Manchester

Mixed Signal PCB Design for Data Converters

Third Year Individual Project – Final Report

2024/04

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Contents

Contents 2

Abstract 4

Declaration of Originality 5

Intellectual Property Statement 6

Acknowledgements 7

1 Introduction 8

1.1 Background and Motivation 8

1.2 Aims and Objectives 9

1.3 Report Structure 10

2 Literature Review 10

2.1 Introduction 10

2.2 Detail 11

2.3 Summary 13

3 Methods 13

3.1 Theoretical Development 13

3.1.1 PCB Layout Specification 13

3.1.2 PCB Components Specification 14

3.2 Project Design 14

3.2.1 PCB Schematic 14

3.2.2 PCB Layout 23

3.3 Project Implementation 27

3.3.1 PCB Manufacturing 27

3.3.2 PCB Programming 27

3.3.3 PCB Testing 28

3.4 Summary 29
4 Results and discussion 30
4.1 Introduction 30
4.2 Individual Tests 30
4.2.1 Single Pin Disturbance Source 30
4.2.2 Single Sample Datasets 31
4.2.3 Time Domain Experiment 32
4.2.4 Frequency Domain Experiment 35
4.3 Discussion/Summary 37
5 Conclusions and Future Work 37
5.1 Conclusions 37
5.2 Future work 38
References 38
Appendices 39

Word count: 12105

Abstract

This project explored and demonstrated the creation and use of two almost identical bespoke mixed signal printed circuit boards, creating an experiment where these two PCBs could provide quantitative evidence on the effect of crosstalk when using two different specific ground plane techniques. It aimed to provide data on an area of study lacking quantitative evidence, providing a unique and novel study in which a PCB is developed in stages, all described within the report. It covers the research required for the PCB's creation, its development schematically and in terms of a PCB layout. It also provides the development of the physical PCB and research results based on the operation of the PCB with set functionality.

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Acknowledgements

Dr Paul Wright is acknowledged in this report for providing excellent guidance and technical knowledge when developing the project.

1 Introduction

1.1 Background and Motivation

Printed Circuit Boards (PCBs) are an integral part of the design of mixed-signal electronic circuits, providing an organised and versatile method of connecting different electronic components together. PCBs were historically used as a cheaper alternative to hand-wiring between components, however now the advantage of reliability and repeatability in circuit manufacturing has become more important, along with implementation of connectivity [1]. Reliability and versatility are demonstrated through PCB layer configurations, providing important advantages over hand-wiring. One advantage is the ability to use one layer or more layers as the system ground. Using an entire layer as a ground reduces the impedance of the ground, however the application of this ground layer can vary between digital and mixed signal designs, introducing problems when implemented incorrectly (as described in Henry Ott's "Partitioning and layout of a mixed-signal PCB") [2].

In this project, a mixed signal design will be implemented, which includes both analogue and digital signals on the same PCB. This introduces the problem of crosstalk between the digital and analogue signals. Although crosstalk between two digital signals (due to mutual inductance) is predictable, allowing for quantitative crosstalk modelling of this interaction [3], accurate modelling of crosstalk between analogue and digital signals is not feasible in general use cases [4]. The analogue signal is more susceptible to crosstalk than the digital signal, which, in combination with an unpredictable coupling between the signals, causes model unfeasibility [4].

There are differences in ground plane design recommendations when creating a mixed signal design, relative to a purely digital design. In a digital design, using a ground plane (or power plane) as a 'reference plane', adjacent to the layer containing the digital signal traces, is a good practice for controlled signal impedance due to the return current flowing in the reference plane, providing a good path for the return signal with tightly coupled electrical and magnetic fields [3]. Mixed signal design complicates this grounding problem as the analogue and digital components of the design must be separated without harming the signal quality. In mixed signal design, shared power or ground planes are potential sources of crosstalk, due to the return current of the stronger, more 'aggressive' digital signals interfering with the weaker, more susceptible analogue signals [4].

In the context of a mixed signal converter circuit using an analogue-to-digital converter (ADC), this could result in the alteration of the voltage value of an analogue signal entering the ADC, causing the digital output of the ADC to be increased erroneously by one least-significant-bit (LSB) value or more, including sub-LSBs which can still affect the output of the ADC, leading to inaccurate output data.

One ground plane recommendation for mixed signal designs historically made by manufacturers is the separation of the ground plane. During literature research, authorities on the subject such as Henry Ott explain that a bad ground plane configuration, such as a split ground plane with no connecting bridge, can cause the crosstalk and radiation emitted by the circuit to increase greatly [2]. This is supported by Dr Paul Wright's Mixed Signal Design work, which shows that incorrect application of a split ground plane causes digital return currents to be allowed to flow through the analogue ground partition, or in some cases, the analogue return current travelling through the digital ground partition [4]. The solution being tested in this project therefore involved the creation of two ground plane designs, with one of them containing a bridge between the analogue and digital partitions just under the ADC, and a full ground plane design, in order to measure the crosstalk effects on either design.

The main motivation for the project is derived from the lack of quantitative evidence of the effectiveness of split and continuous ground plane crosstalk performance, with component suppliers providing questionable PCB layout guidance. This motivation consists of the collection of quantitative evidence through the use of custom-designed printed circuit boards to support or oppose these manufacturer claims.

1.2 Aims and Objectives

This project aims to address the lack of quantitative evidence comparing the mixed signal crosstalk performance of split and continuous PCB ground planes. It aims to develop two PCB designs capable of providing equivalent sampling and digital threat generation (generation of controlled noise signals) with different ground layouts, to allow direct comparison of performance.

Five primary objectives for this project were decided:

- Develop two PCB designs capable of equivalent sampling and threat detection, one with a split ground plane with a single connecting bridge and another using a full ground plane.

- Measuring the difference in analogue-to-digital converter output data due to crosstalk.
- Measuring and comparing crosstalk behaviour using the time domain and frequency domain.
- Measuring and comparing crosstalk on the analogue signal when different patterns of digital signal threat currents are applied (different magnitudes of load currents).
- Comparison of the effectiveness of the single ground bridge and full ground plane designs at splitting the analogue and digital currents based on the previous objectives' findings.

A basic overview of the main project methodology:

- Design PCB schematic.
- Create component list from schematic.
- Create PCB layouts for single-bridge and double-bridge ground plane designs.
- Manufacture PCB layouts.
- Program microcontroller to produce required digital signals and sample signals from the ADC.
- Compare measured signals with digital signal waveforms as described in the objectives.
- Evaluate gathered evidence to obtain a conclusion.

1.3 Report Structure

This report is separated into 5 main chapters, with Chapter 1 describing the background, motivation for the project and aims and objectives, whilst Chapter 2 contains a review of literature relevant to mixed signal PCB design. Chapter 3 includes the development of the PCB in terms of theoretical development, project design and implementation of the project. Chapter 4 reports on the testing of the two PCB designs, providing analysis of data and comparison between the performance of the two designs, whilst Chapter 5 completes the report with a conclusion based on the project as a whole and suggestions on improvements for future work.

2 Literature Review

2.1 Introduction

Mixed signal PCB designs are a type of PCB design used for a wide range of applications such as data conversion circuits. When creating a project based on these mixed signal circuits, research relevant to the creation of mixed signal circuits must be reviewed. Available research for mixed signal designs is lacking in comparison to other areas of PCB design such as electromagnetic interference testing or pure digital signal designs, therefore the literature to review is mainly

focussed on the ground plane layout and component placement rather than the specific components required to develop the two PCBs needed to complete the project aims.

2.2 Detail

One main aspect of this is the concept of interaction between the digital and analogue signals that are involved in mixed signal designs. Within a mixed signal PCB design, the properties of the digital and analogue parts of the circuit have different characteristics, which lead to difficulty in separating the two circuits successfully. Analogue circuits often contain low voltage level signals or high impedance signals, whilst digital circuits contain large rates of change of voltage and current, leading to digital circuits being classed as 'aggressors' and analogue circuits being classed as 'victims' [1]. In the context of this project, this means the PCB design will need to physically separate the digital and analogue components sufficiently to prevent unwanted crosstalk, however if crosstalk is to be measured between the two partitions, there must be some intentional mechanism to cause a measurable amount of crosstalk. This could be implemented as a controlled digital threat which could be operated by a microcontroller or FPGA to provide multiple threats with different characteristics from one source.

Splitting the electrical ground has been historically recommended by manufacturers of mixed signal parts, however sources from experts such as Henry Ott the split plane is said to be useable but problematic [2]. One problem is that a route cannot be made over a split in the plane as radiation and crosstalk greatly increases, this is said to be due to the return current having to flow in a large loop, which at high frequencies produces high ground inductance and radiation. In addition, Ott explains that low-level analogue currents are susceptible to interference when flowing in large loops. Dr Wright supports this, as mixed signal designs with split ground planes may be good circuits, however, good performance from PCBs including this technique may not be effective due to this technique, but rather the correct partitioning of analogue and digital signal components – with correct routing being the main reason for good PCB performance [1]. For this project, this clearly shows that there could be some usefulness from split-planes, but it requires effective testing to obtain quantitative evidence of its effectiveness. This suggests two PCB designs should be created for the project – one design with a whole ground plane and another design with a split ground plane that has a connection underneath a mixed signal component. Walt Kester's "Mixed-signal and DSP Design Techniques" reinforces the idea of using a continuous ground plane

as it is shown to provide much lower impedance than a singular ground track – in his example the ground track would cause a 10% error in signal voltage for a 2 V signal when a transient current with a slew rate of 10 mA/ns travels through a #22 gauge wire [5]. Kester also recommends keeping at least 75% of the board area on one side for the ground plane [5], indicating that the split used on one of the PCB designs should be narrow to maintain a sufficiently sized ground plane.

The effectiveness of split-planes is further questioned when multiple mixed signal devices are included on the PCB. In the case of using multiple ADCs on one PCB, the technique to split the analogue and digital ground planes is less effective than using no splitting at all [4]. If the analogue plane is split into two and both analogue sections are connected just to the digital ground plane, the analogue return current is forced into the digital section of the ground plane if passed between the analogue planes, causing large noise disturbances to the analogue signal. If there is only a single analogue plane connected to the digital plane under each data converter, the digital return current can travel through the bridges between the analogue and digital planes and through the analogue ground plane, causing electrical noise to be transferred to the analogue signal through shared impedance [1]. It is further shown that when using multiple ADCs, if each ADC has a bridge in the ground plane the two partitions are no longer isolated. Kester reinforces this idea as he explains that a ground plane bridge acts as a “star” ground point for the mixed signal PCB when using just one mixed signal component, however the use of multiple ADCs would make the “star” ground point impossible due to the analogue and digital ground planes being joined at multiple points, leading to ground loops [5]. This ties into the second potential aim of the project which compares the difference in interference or effectiveness when using multiple ground plane bridges – Ott suggests using a single ground plane partitioned into analogue and digital sections as the analogue and digital ground pins are connected together through a low impedance ground, along with not creating unintentional loops [2]. The effect of having multiple bridges between the two partitions is shown in literature to be significant qualitatively, however this provides the opportunity to test the crosstalk in the ground plane of the split-plane design, therefore meaning a method to add bridges to the ground plane of one of the PCBs should be available as part of the design of the PCB.

2.3 Summary

With a lack of quantitative evidence on the effectiveness of a split-ground plane in preventing crosstalk between digital and analogue circuits, it is therefore vital that the PCB specifications and design includes mechanisms to allow multiple tests to be taken with the same PCBs, with a focus on comparison between the split-ground plane design and the non-split-ground plane design. A mechanism is required to be able to add more connections between the split in the split-ground design, whilst a mechanism to provide a controlled digital threat must be included to be able to compare crosstalk in a repeatable, controlled manner. As the two PCBs will be compared, it is also vital that the majority of the top layer of both PCBs is identical, in order to provide a more valid set of experimental data.

3 Methods

3.1 Theoretical Development

3.1.1 PCB Layout Specification

The first stage in project execution consisted of the theoretical development of the PCB. A specification was created that explained the requirements of the PCB design in order to allow effective measurement of the crosstalk between the analogue and digital partitions of the PCB after it had been designed and manufactured.

The specification produced from the literature review research described the layout of the ground plane for each of the PCB designs – in one of the designs a full plane with no split was to be created, whilst the design with the split plane was to be created with a bridge the width of the ADC, directly underneath the ADC. This would then allow the effects of the split on controlling return current flow to be measured, and quantitative evidence of the ground being split between the two partitions.

Another aspect of the PCB which was included in the specification is the partitioning of components on the top layer – analogue components and digital components had to be grouped based on their electrical characteristics, with analogue-only components being placed in the analogue partition of the board and digital-only components being placed in the digital partition of the board. In addition, the ADC being used to convert the analogue input signals to digital signals

was classed as a mixed signal device due to interacting with both digital and analogue signals. This meant the ADC would have to be placed along the boundary that separates the digital components and signals from the analogue components and signals, the mixed signal boundary.

3.1.2 PCB Components Specification

Like the specification for the layout of the PCB, a specification for the components required in the circuit was created. A set of components would have to be selected to operate the ADC, along with support components for controlling the microcontroller used in the design. The initial literature research concluded that the ADC's analogue supporting components consisted of a voltage reference, positive and negative analogue inputs, a ground connection and an analogue voltage source. The analogue input further required a voltage buffer and divider to provide an input voltage of exactly half of the reference voltage. The ADC's main digital supporting component was the microcontroller used to control the operation of the ADC using an SPI connection.

3.2 Project Design

Following the completion of the literature review and theoretical development, steps had to be taken to design the project (schematic and PCB design) according to the needs set out in the literature review and PCB specification. This entailed the creation of multiple key tasks and deliverables in order to be able to conduct an effective and productive project. From the literature review and PCB specification, it was clear that two PCBs must be made and used for testing. This meant the main deliverables would mostly be related to the PCB design process itself. This would start with a schematic, which was then used in the creation of a PCB layout. This layout would have to be manufactured into a physical PCB design, which would then have to be assembled and programmed. This process needed to take place for both PCB designs, although the designs were mostly identical for fair testing. In addition to the PCB-based deliverables, the PCBs needed to be tested and results collected as a core deliverable.

3.2.1 PCB Schematic

After creating the specification for the PCB, the schematic design for both the non-split and split-ground plane PCB variations was created.

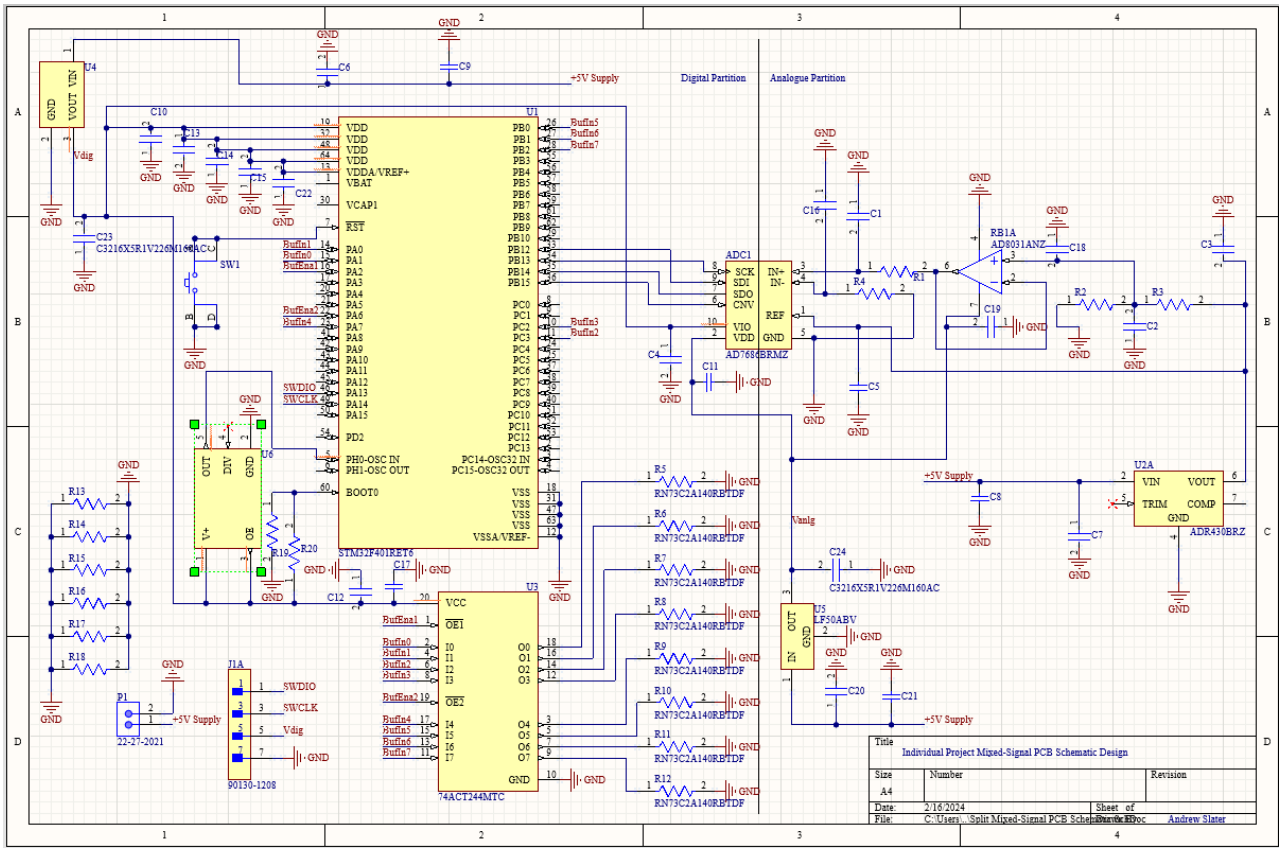


Figure 3.1: Full schematic design of PCB connectivity.

This was undertaken by careful selection of components and an iterative design method. Although not making a functional difference in the schematic, the schematic was split visually into an analogue and digital partition. This was done to simplify the schematic's design as it closer reflects the design in the PCB layout.

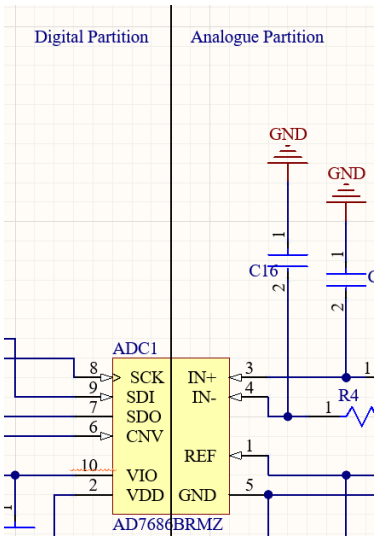


Figure 3.2: Visual 'partitioning' technique employed in the schematic.

For the digital side of the schematic, the microcontroller, digital clock, transmission line buffer and 3.3 V voltage regulator would have to be connected correctly, along with headers used for the power supply and programmer for the microcontroller. As the main purpose of the microcontroller was to configure the operation of the transmission line buffer and the sampling of the ADC, the microcontroller required 10 connections to the transmission line buffer and 4 connections to the ADC.

For the transmission line buffer, 8 transmission line input connections were made from the microcontroller to the buffer as these controlled the logic state of each line, whilst 2 more connections were made from the microcontroller to the transmission line buffer to control the output enable pins of the buffer component. This transmission line buffer was then connected to 8 identical resistors through the transmission line buffer output pins to create the transmission lines. More specifically, the transmission line buffer used was the 74AC244MTC, as according to the datasheet, the output current of each output pin was rated at 24 mA [6], which when multiplied by 8, provided a large enough current to act as a simulated digital noise source with sufficient current to provide what should be measurable crosstalk voltage. By using 24 mA source transmission lines, it also allowed for a wide range of electrical pulse sequences whilst providing enough current to generate significant crosstalk. The transmission lines themselves required termination resistors of a specified resistance. This was calculated to be approximately 140 Ω, however the resistors had additional specifications to fulfil – the resistor RN73C2A140RBTDF was selected as the termination resistor as it had a 0.1% component tolerance [7] which was essential to ensure the crosstalk produced by each transmission line, as isolated components, were equal. It also helped ensure the maximum crosstalk produced by the summation of the transmission lines was equal between the two PCBs when not accounting for the split-ground plane feature, ensuring fairer measurement and comparison.

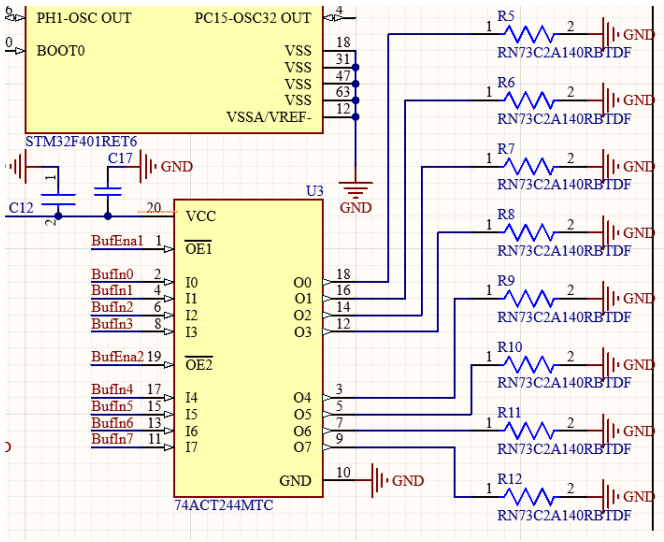


Figure 3.3: Transmission line buffer schematic design.

Although the 74AC244MTC transmission line buffer was chosen for the PCB design, the schematic and PCB layout used the 74ACT244MTC as it shared the same footprint as the 74AC244MTC whilst the 74AC244MTC did not have an available footprint or schematic component in the PCB designer. Decoupling capacitors were also connected to the transmission line buffer's voltage input pin to act as a bank of charge that can counteract voltage drops in the input.

For the ADC the 4 connections from the microcontroller (STM32F401RE) to the ADC controlled the clock input, digital input, digital output and sample enable lines. These allowed the microcontroller to control the ADC, although the main connection of importance was the sample enable connection. The ADC selected for the two PCB designs required a moderately high resolution and sample rate. This resolution, in conjunction with the reference voltage, determined the smallest possible voltage that resulted in an increase in the digital output value. The equation for the smallest possible voltage representative of one least significant bit of a digital ADC output is:

$$V_{REF}/2^N \qquad (1.1)$$

Where V_{REF} is the reference voltage and N is the resolution of the ADC in bits.

The ADC used was the AD7686 as it was a 16-bit analogue-to-digital converter with a 500 kSPS (500,000 samples per second) sample rate [8]. As shown from the literature review, a moderately high frequency signal must have been used in order to produce a large amount of crosstalk in the analogue partition of the ground plane – the ADC therefore needed to have a high sample rate in order to measure samples at a moderately high frequency. With a chosen reference voltage of

2.048 V, this meant the smallest detectable change in voltage by the ADC was 31.25 µV. This, in operation with the transmission line buffer, provided a controllable digital threat which could be used to test the level of crosstalk from the digital side to the analogue side of the ground plane in terms of digital output changes.

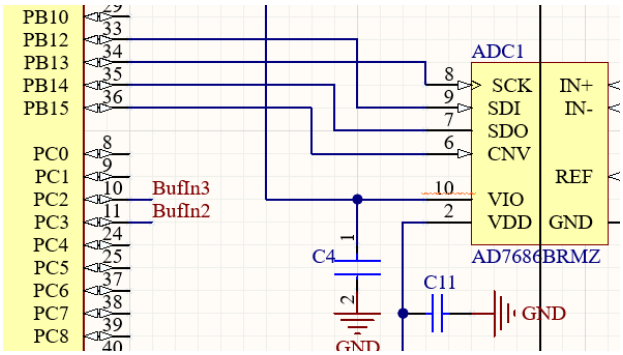


Figure 3.4: Schematic design of ADC-Microcontroller connection.

As with the transmission line buffer, decoupling capacitors were connected to the voltage input pins VIO and VDD of the ADC.

The 3.3 V voltage regulator had to be connected to each of the digital components in order to power them and required decoupling capacitors between the supply and the voltage regulator to provide a bank of charge. The decoupling capacitors were implemented as a tiered system, with a large and a small capacitor (10 µF and 100 nF) connected to the input of the voltage regulator. The smaller capacitor provided charge up to higher frequencies than the larger capacitor due to storing less charge, reducing the time taken to charge or discharge. These capacitors helped provide a stable voltage input to the regulator. The output pin of the voltage regulator, along with being connected to the inputs of the digital components, was connected to a large bulk capacitor of 20 µF – this large capacitor was used to help stabilise the output voltage to the digital components, as the greater capacitance of the capacitor provided a large amount of charge to mitigate changes in the load voltage, due to fluctuations in the loads of the digital components. Each of the digital components required a 3.3 V connection, meaning that only a single voltage regulator was required to provide power to each component.

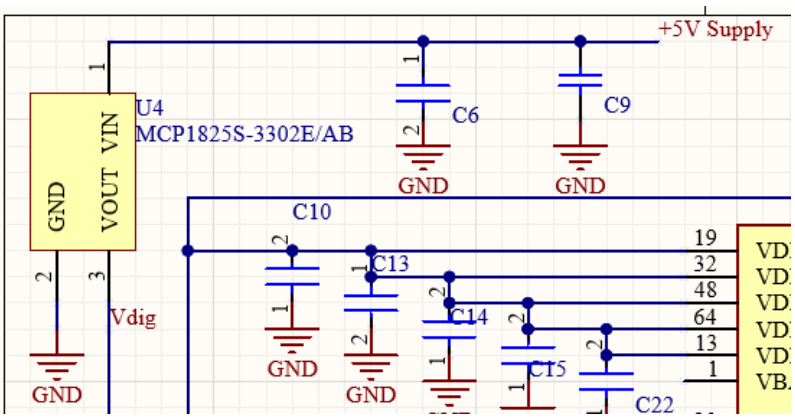


Figure 3.5: Schematic design of 3.3 V voltage regulator.

The voltage regulator selected for the digital components was the MCP1825S-3302E/AB. This was selected as it provided the required 3.3 V output whilst being able to receive a 5 V input from the 5 V supply. It also provided a 500 mA current output which was sufficient to power all of the digital components. Another aspect of the voltage regulator which was taken into account was the thermal resistance of the component and the temperature it would reach when in use. As the voltage regulator output 3.3 V with a 5 V input, with a 500 mA output current, the power dissipation of the device would be 0.85 W due to the 1.7 V difference and 0.5 A output current. The thermal resistance of the device was rated at 29.4 °C/W, therefore with a 0.85 W dissipation, the temperature increase would be approximately 25 °C. This was within the rated operating temperature of the device [9].

The clock used in the PCB schematic was connected to the microcontroller's external clock input pin to provide a high enough frequency clock signal to the microcontroller. The clock device chosen to provide a clock signal to the microcontroller was the LTC6905IS5-80#TRMPBF which was chosen as its operating frequency of 40 MHz was equal to the maximum clock speed of the microcontroller with a low frequency error of 0.5% [10].

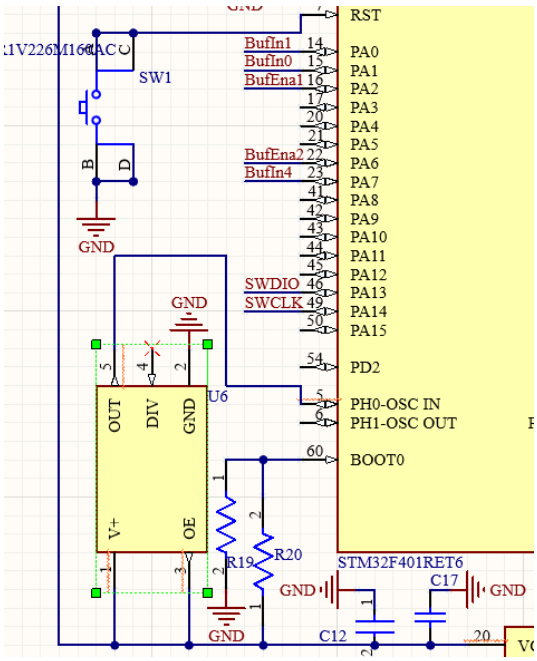


Figure 3.6: Schematic design of clock source and reset button.

To be able to program the microcontroller, a 4-pin connector was added to the schematic and connected to the pins on the microcontroller that allow communication between a programmer and the microcontroller itself.

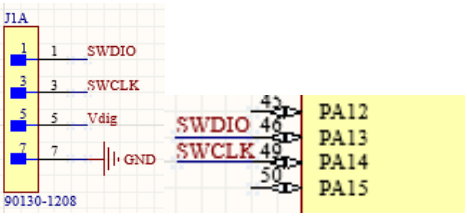


Figure 3.7: Pin connections for microcontroller programmer in schematic design.

The microcontroller also required connections to the boot pin for the purposes of booting up correctly during use, along with connections for a reset button and programmer connection lines.

The analogue ‘partition’ of the schematic required the previously mentioned voltage reference, voltage buffer and RC filter, however it also required the correct voltage regulator, as separate voltage sources were to be used for either partition, with the analogue partition being powered from a single 5 V voltage source. A wide range of decoupling capacitors were also implemented at the inputs to each analogue component to act as a reservoir of charge, whilst an additional larger capacitor was implemented at the output of the voltage regulator to provide a large reservoir of charge for the analogue partition.

The voltage regulator chosen was the LF50ABV as its datasheet stated that it provided a 5 V output voltage as was required by the components used in the analogue partition, whilst also providing 500 mA output current which was sufficient for all of the components in the analogue partition of the PCB [11]. The voltage drop across the regulator was stated to be 400 mV. It was vital to select a regulator with these specifications as all of the components used in the analogue partition of the PCB required a 5 V power supply.

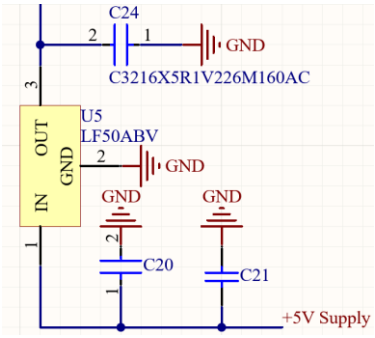


Figure 3.8: Analogue power supply schematic design.

The analogue power supply implementation consisted of a direct connection from the 5 V external supply to the input port of the 5 V regulator, with 10 µF and 100 nF capacitors connected between the 5 V supply and ground connection. The implementation of the smaller capacitor was required as it operated at a higher frequency and could provide a bank of charge to the input of the voltage regulator when there was fluctuation in the external power supply, whilst the larger capacitor was implemented in order to provide a larger bank of charge to support the input of the voltage regulator when larger fluctuations in the 5 V supply occurred. A 20 µF capacitor was implemented at the output port of the voltage regulator to act as a relatively large bank of charge and provided stabilisation of the output voltage which would ensure the analogue components maintain their expected performance. The 5 V regulated output voltage was connected to the VDD pin of the ADC and the and the voltage buffer.

The circuitry required for the reference and voltage inputs for the ADC were more complex to implement, with a voltage buffer being required to maintain good signal quality for the positive ADC input. The reference voltage component used in the design was the ADR430BRZ, which provided a constant output voltage of 2.048 V [12]. This reference voltage was chosen as the voltage level for the least significant bit of the ADC's digital output is proportional to the reference

voltage, meaning that a lower reference voltage allows the ADC to detect smaller changes in input voltage, raising the sensitivity of the ADC to mixed signal crosstalk. This allows for more precise testing of crosstalk voltage through the change in ADC output value.

For the analogue input to the ADC, the reference voltage was divided by 2 using a potential divider circuit as this provided a constant analogue input which resides in the middle of the ADC voltage range. This potential divider circuit was then connected to the input of the voltage buffer component which was selected to be an AD8031ANZ. This component was selected as it provided 80 MHz small signal bandwidth with sufficient slew rate for the frequency used with the ADC [13]. This component was also recommended by the manufacturer of the ADC as a supporting component. Between the voltage buffer and the ADC, an RC circuit was implemented, using a 30 nF capacitor connected to ground and a 33 Ω resistor, which was also copied and reused for the negative ADC input which connected to ground. This RC circuit provides a storage of charge for the input of the ADC whilst also separating the feedback loop connected between the input and output of the voltage buffer from the positive input to the ADC.

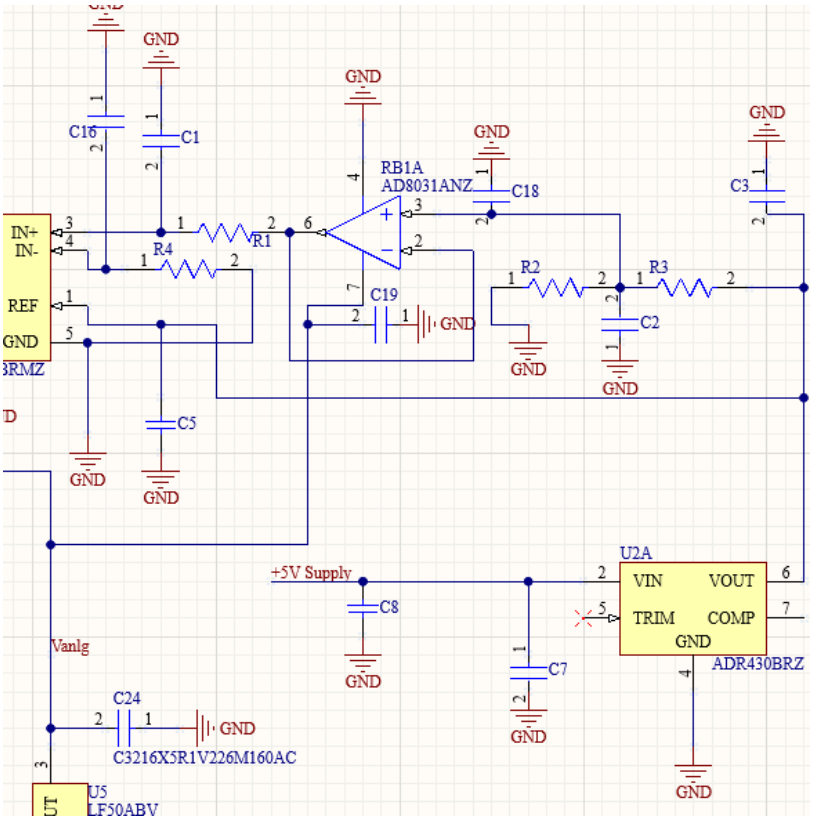


Figure 3.9: Schematic design for voltage reference, potential divider and positive voltage input to ADC.

Once the entirety of the PCB schematic was created, the PCB layout could then be developed, however changes to the input pins of the microcontroller had to be made to be able to accommodate the geometry of the traces used in the PCB design.

For the split-ground design, the stitching resistors footprints that were to be included in the PCB design had to be implemented in the schematic. As these resistor footprints were not going to use any resistor components and were to act as bridges in the ground plane, these resistors were just connected to each other and the ground.

3.2.2 PCB Layout

The main focus of the project consisted of the ground plane's layout and the effectiveness at minimising crosstalk between the analogue and digital signals within a PCB device. In order to successfully test this, the PCB design required an identical top layer layout and differing ground plane layouts. The design of the layout of the ground planes had to focus on providing a clear difference between the behaviour of a split-ground design and non-split-ground design on the level of crosstalk between the analogue and digital partitions of the PCB.

The selected method to achieve this was to split the ground plane vertically down the middle of the PCB, providing a bridge to connect the two sides underneath the ADC used on the PCB. This allowed a symmetrical design on the ground plane layer, increasing the validity of the measurements that were to be taken from this ground plane. This plane design was also chosen as it provided the least restriction on where the digital and analogue components could be located, as both the analogue and digital components were provided a large section of the top layer of the PCB to be placed within.

Along with testing the difference between a full ground plane and a split-ground plane with a bridge at reducing crosstalk between digital and analogue components, another point of interest with regards to the literature review was the effectiveness of the split-ground plane design at preventing crosstalk when multiple bridges were included. To incorporate this into the design of the PCB, a mechanism to allow multiple bridges to be used on the ground plane was necessary. This was implemented within the split-ground plane by providing resistor footprint stitches which act as solderable bridges, so the split-ground plane PCB could be tested against the non-split design and then soldered to allow the measurement of crosstalk in comparison to its own previous configuration.

To provide a correctly partitioned mixed signal PCB design, the analogue components were grouped to the right of the mixed signal boundary, which ran along the split in the ground plane. The digital components were grouped to the left of the mixed signal boundary. The ADC was placed on the middle of the mixed signal boundary, with its digital pins being in the digital partition and its analogue pins being in the analogue partition. For the non-split design, the ground plane was one complete plane, whilst in the split design the resistor footprints were included along the mixed signal boundary, below the ADC where the digital transmission lines were. The minimum width and gap width of the traces were 0.254 mm to prevent crosstalk between the digital traces. The traces connected to the voltage regulator from the supply voltage had a width of 1 mm instead of the minimum 0.254 mm to provide reduced impedance.

When implementing power regulation to the board, the 5 V supply connector was implemented at the top of the board, connected to both partitions to act as a global ground point, with sufficient distance from the analogue and digital components so it didn't affect the crosstalk between the digital threats and the analogue signals. Traces then branched out from the supply connector to the analogue voltage regulator and the digital voltage regulator. Between the supply connector and each regulator, a 10 µF and 100 nF capacitor were connected to ground as required in the schematic, with the larger capacitor being placed closer to the 5 V supply, and the smaller capacitor being placed closer to the voltage regulator. This is done as the smaller capacitor operates at a higher frequency and therefore should be closer to the voltage input pin of the regulator to be able to counteract changes in the voltages at a sufficient level and speed. 20 µF capacitors were then placed below the regulators, connected between the output pin of the regulator and the voltage buffer, connected to ground using a thermal relief via.

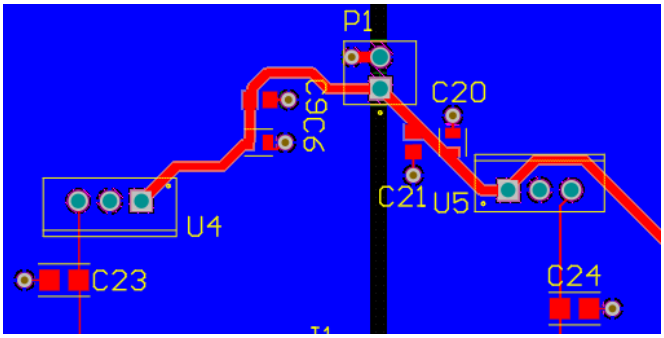


Figure 3.10: PCB layout design for voltage regulation.

On the analogue side of the mixed signal boundary, the analogue components were placed relatively close together to reduce the length of each trace and keep the PCB design compact. Decoupling capacitors were placed close to component pins as was done with the voltage regulator – this allows each component to have its own bank of charge to stabilise the voltage at the voltage input pins. Each component, including capacitors and resistors, were connected to the ground plane using thermally relieved vias as this would help ease soldering during the manufacturing process of the PCB. The components were connected as required in the schematic, ensuring no components or traces were crossing the mixed signal boundary except for the ADC. Unlike the voltage buffer, which was powered by a connection from the voltage regulator, the voltage reference was powered straight from the 5 V supply. This was done as the voltage reference component itself regulates its output voltage to 2.048 V so a connection from the voltage regulator was not necessary for the component.

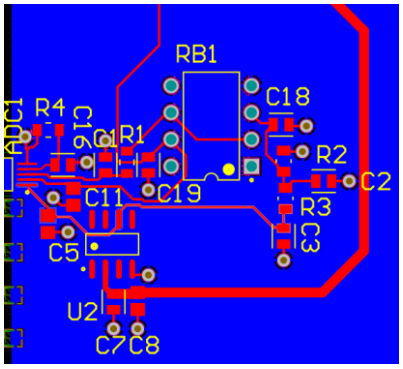


Figure 3.11: PCB layout design of analogue partition of the PCB.

On the digital side of the mixed signal boundary, the digital components were grouped and placed together, in order to reduce board space and maintain correct partitioning. The microcontroller used in the project – the STMF401RE – was connected to the ADC control pins as required in the schematic, whilst its also connected to the transmission line buffer as described in the PCB schematic. The microcontroller was connected to the programmer connector header and reset switch as required in the schematic. The BOOT0 pin used by the microcontroller to decide how it behaves on boot up was provided two options for soldering when manufactured – resistor footprints were made available for connecting the BOOT0 pin to either ground or 5 V if needed. The clock generator component was also connected to the microcontroller.

When placing the transmission line buffer in the PCB design, due to the routing constraints posed by a two-layer plated through-hole PCB design, the pins of the microcontroller the buffer

connected to were altered iteratively until all pins of the buffer could be controlled by the pins of the microcontroller without traces intersecting. The traces connected to the outputs of the transmission line buffer were then routed towards the mixed signal boundary and terminated using termination resistors. By bringing the transmission lines close to the mixed-signal boundary, the effect of the digital signals produced by the transmission lines on the analogue signals in the analogue partition could be measured more clearly. Each transmission line connected to the ground plane by a via connecting each termination resistor to the ground plane. Decoupling capacitors were connected to each voltage input pin on the microcontroller and other digital components, with the same placement scheme used with the analogue components.

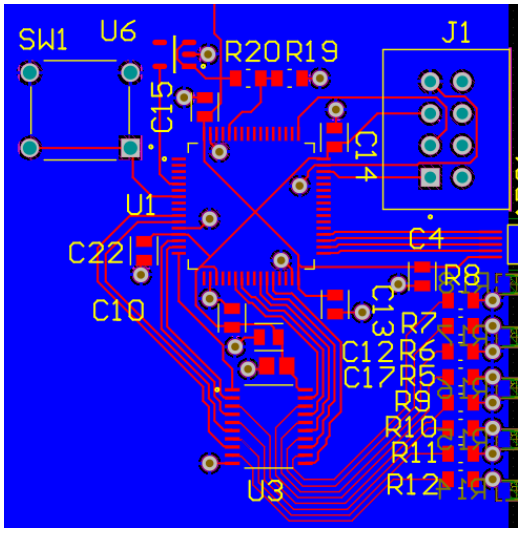


Figure 3.12: PCB layout design of digital partition of the PCB.

The overall design of the PCB layout provided a fair experimental platform for measuring the crosstalk between the digital and analogue signals, by ensuring that the top layer components had the exact same placement between the two PCB layouts (non-split and split) with the only differentiating design feature being the ground plane design, increasing the validity of the tests when the PCB was manufactured and tested.

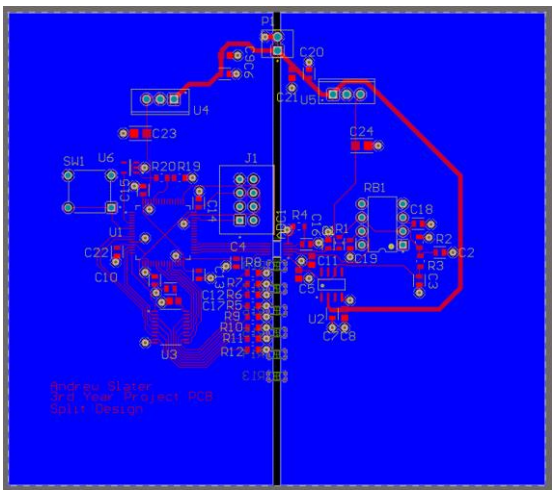


Figure 3.13: Full PCB layout design for split-ground PCB design.

With the PCB schematic and layout fully designed to the requirements of the literature review and specification, it was then possible to proceed with the manufacturing of the PCB.

3.3 Project Implementation

Once the PCB had been designed, it was then possible to start implementing the design into a physical, working experimental PCB. This required multiple steps to achieve, mainly manufacturing, programming and then testing the PCB design.

3.3.1 PCB Manufacturing

The PCB had to be manufactured as a 2-layer plated through-hole design and the University of Manchester's in-house PCB manufacturing capabilities permitted this. The PCB design had to be altered to fit the requirements of the PCB manufacturing rules, however the functionality of the PCB shouldn't have been affected by these changes. Some changes that were made included widening holes for through-hole components to ensure there was sufficient tolerance to allow the pins of the trough-hole components to pass through the PCB.

3.3.2 PCB Programming

Once the PCB had been manufactured, the last core task to complete before being able to test the PCB was to program the PCB. According to the requirements set out by the literature review and PCB specification, multiple tests would have to take place within the same board, causing the programming of the PCB's microcontroller to include multiple functions.

One major function of the microcontroller was to control the operation of the ADC. This entailed controlling the sampling timing of the ADC. The ADC samples on every rising edge, therefore the microcontroller had to be programmed to continuously pulse the CNV pin of the ADC at an acceptable rate in order to retrieve samples at a high frequency. The clock provided to the microcontroller was a 40 MHz clock which could provide a clock speed up to the limit of the STM32F401RE. This clock speed could then be utilised by the microcontroller to sample using the ADC whilst also executing other functions.

Another function of the microcontroller was to control the operation of the transmission line buffer and transmission lines. The microcontroller would act as the controller for the transmission line pulses, continuously pulsing the transmission lines in a specific sequence set during programming. As the microcontroller directly controlled the transmission line buffer, it was possible to program a set of transmission line electrical pulse patterns, treating it as if it was an 8-bit value. This allowed electrical threats of both large current pulses and sporadic smaller pulses which could both be tested for crosstalk with the analogue signals. Each pattern could be set to repeat multiple times before cycling to the next pattern which could be repeated as needed.

3.3.3 PCB Testing

To gather quantitative evidence of the effectiveness of a split-ground plane design on separating the analogue and digital PCB partitions, multiple tests covering different aspects and effects of the crosstalk were to be conducted.

One test was a comparative test directly between the non-split-ground PCB design and the split-ground PCB design. In this test, the same electrical threat would be present near the mixed signal boundary on both PCBs, and measurements for voltage would be taken at the same point on both PCB designs. This would show the difference in crosstalk voltage when a full ground plane is used in comparison to a split-ground plane, helping to prove/disprove the effectiveness of a split-ground plane. This test could also include the ADC as the digital output of the ADC could be read by the microcontroller on each PCB and the digital value outputted by the ADCs could be compared.

Another test was an observation test based on the behaviour of the crosstalk in comparison to the electrical threat signal. As shown in literature, it would be expected that the crosstalk in the analogue circuit would spike when the digital electrical threat signal changed from low to high or

high to low voltage. This behaviour could be observed on both PCB designs and the amplitude of the crosstalk spike could be compared to be able to conclude whether the split-ground plane reduced the crosstalk spike amplitude in comparison to the non-split-ground plane PCB.

A test specifically using the split-ground PCB could also be conducted. As there were available resistor footprints on the underside of the split-ground PCB, these footprints could be soldered together, intentionally creating more connections between the two PCB partitions. This allowed the observation of a change in crosstalk due to digital return currents potentially passing through the analogue partition, potentially causing increased crosstalk. The number of bridges could be altered to obtain measurements of crosstalk based on the number of bridges connecting the two partitions.

These tests could then be used to create conclusions on the experiment based on the results found, and how they relate to the main aims of the project.

3.4 Summary

The development of the PCB was the largest part of the project, extending from the creation of a PCB specification and parts specification, up to manufacturing and testing the PCB. Creating the PCB specification allowed the creation of the PCB schematic. This schematic, through iterative design, provided the basis for a suitable PCB design to allow for the sampling of data and threat generation. The schematic included the circuitry to perform the sampling and threat generation on a connectivity basis, however implementing it into a PCB layout provided the correct partitioning and positioning in order to be able to consider the PCB design as a viable design. The PCB layout separated the digital and analogue components into two sections based on their electrical characteristics, with the ADC in the middle along the mixed signal boundary line. The PCB layout expanded on the split power source provided in the schematic by allowing the voltage regulators to be placed towards the top of the board, whilst also allowing for ideal capacitor positioning for each connected component. With the PCB layout created, the PCB manufacturing could take place, with the PCBs being soldered and then electrically tested for hardware faults. Once fully developed and manufactured, the PCB was then viable for experimental tests.

4 Results and discussion

4.1 Introduction

After construction and electrical testing of the PCB design, all necessary hardware and software to undertake the required series of experiments was present, allowing individual tests on both PCB designs for the purposes of comparison.

4.2 Individual Tests

4.2.1 Single Pin Disturbance Source

The first test conducted consisted of measuring the 10%-90% rise time of the transition of one of the transmission line signals from low to high, which could show if the single pin disturbance source could cause an EMC test failure if used on a PCB without shielding such as the PCB developed for this project.

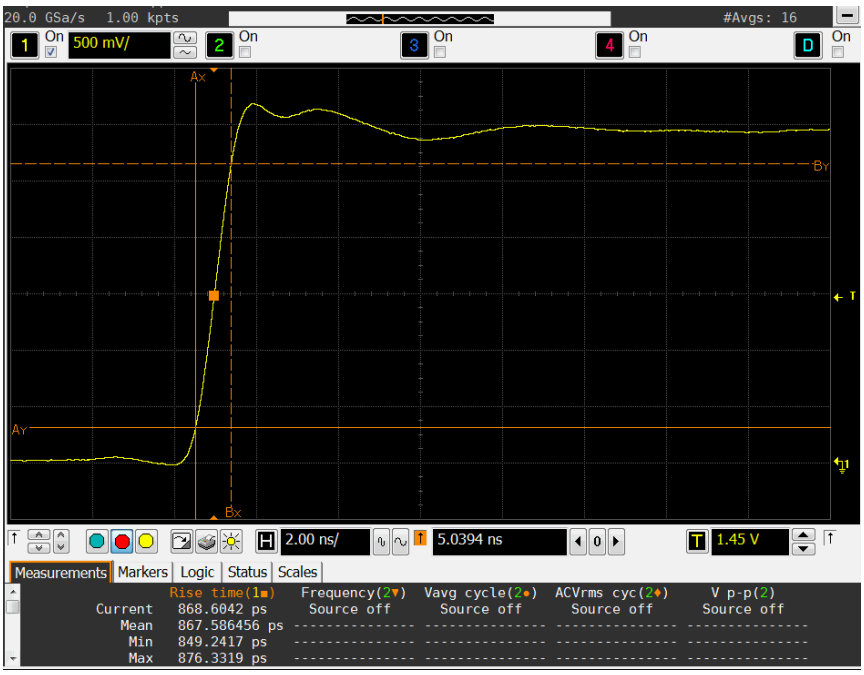


Figure 4.1: Rise time screen capture of one transmission line pin transition.

A measurement system consisting of a 1 GHz oscilloscope and 500 MHz probe was used to measure the minimum measurable transmission line rise time, calculated as approximately 0.753 ns. This was calculated by converting the bandwidth of each of the measurement components into rise times and combining them using the equation below:

$$T_{total}^2 = T_{scope}^2 + T_{probe}^2 \quad (4.2)$$

T_{scope} was calculated to be 0.339 ns, whilst T_{probe} was calculated to be 0.672 ns. Using equation (4.2), the total rise time was calculated as 0.753 ns.

The rise time shown in Figure 4.1 shows an observed 0.868 ns rise time which is longer than the system limit, whilst also being within the expected rise time of approximately 1 ns of AC logic with a small amount of capacitive load. At this rise time, the pins would cause EMC test failure if left unshielded by outer ground or power plane layers, if used in an application such as a high frequency clock source.

4.2.2 Single Sample Datasets

The second test conducted with the two PCBs were single sample dataset tests, each consisting of a set of data conversions in which a transmission line pulse would be toggled immediately after starting each ADC conversion. By taking the average value of the entire dataset of approximately 10000 samples and repeating the experiment 10 times, an average DC shift in the output code could be detected. This experiment was repeated for the two PCB designs, with one set of data involving the generated noise and the other set of data without the generated noise. This allowed the comparison of the change in voltage between the dataset with the added noise and the dataset without the added noise, regardless of any DC offset between the two PCBs.

Table 4.1: Averaged ADC output values in decimal form for the disturbed and undisturbed single sample experiments for both the non-split ground plane PCB and the split-ground plane PCBs.

Sample Set:	**Undisturbed Signal Non-Split PCB**	**Disturbed Signal Non-Split PCB**	**Undisturbed Signal Split PCB**	**Disturbed Signal Split PCB**
1	32702.3	32701.9	32781.9	32779.3
2	32703.8	32701.9	32782.0	32777.9
3	32703.9	32700.8	32781.4	32777.9
4	32703.9	32701.2	32780.5	32778.3
5	32703.8	32701.4	32780.6	32781.7
6	32703.9	32701.4	32779.1	32780.6
7	32702.6	32701.5	32782.1	32781.7

8	32700.9	32701.5	32782.2	32781.8
9	32703.9	32700.6	32782.2	32781.7
10	32703.9	32700.8	32782.1	32781.8
Average	32703.3	32701.3	32781.4	32780.3

From the data shown in Table 4.1, the change in average ADC output is approximately 2 codes for the non-split ground PCB design and approximately 1.1 codes for the split ground PCB design. This corresponds to a DC shift of 61 µV and 34 µV respectively. This could suggest that the digital threat DC current is restricted in the split ground design by the bridge from entering the analogue region in the same magnitude as the non-split design. This, however, may not be certain as the standard deviation for the sets of sampled data varied between the datasets: 1.04 and 1.74 for the non-disturbed and disturbed sample sets for the split ground plane design, and 0.45 and 1.04 for the non-disturbed and disturbed sample sets for the non-split ground plane design. It is therefore possible that the DC shift caused in the two PCB designs was not caused by the DC current flow from the digital partition into the analogue partition.

4.2.3 Time Domain Experiment

The third experiment to be undertaken involved the collection of data using a similar method to the previous experiment, except the digital threat signal was controlled as a 25 kHz pulse signal or as a step signal instead of occurring synchronously with every single ADC sample. This intended to allow the time domain series of the undisturbed and disturbed models of the two PCBs to be compared.

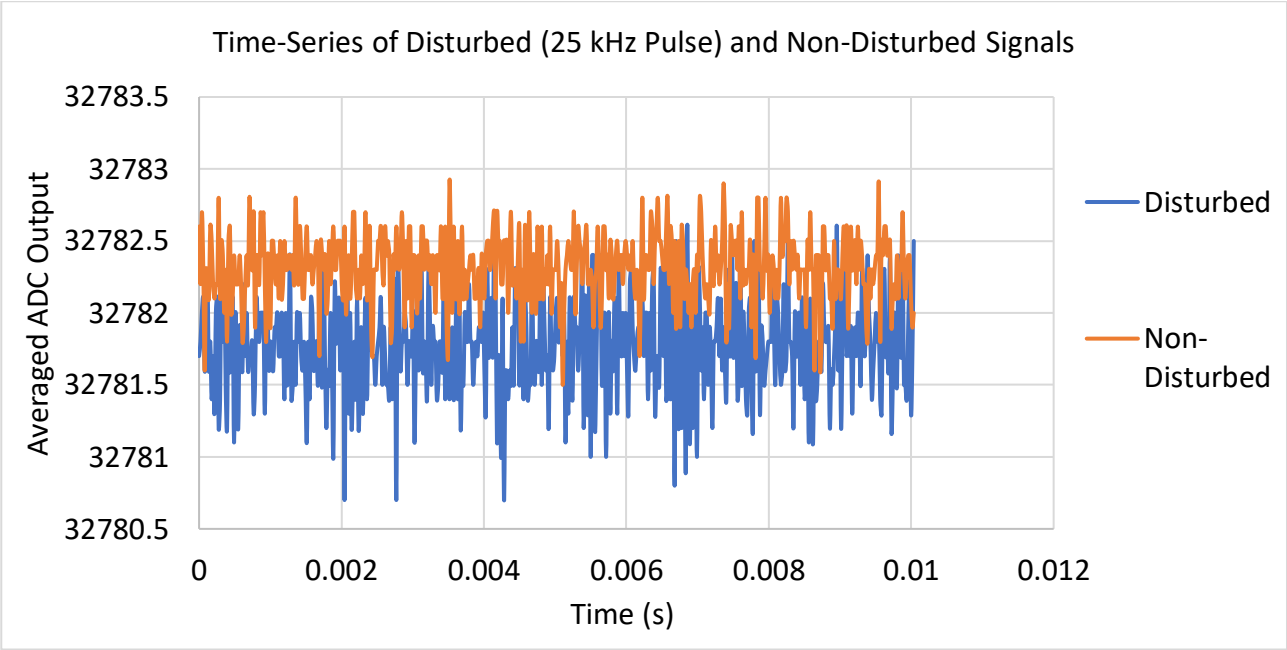


Figure 4.2: Time domain graph for split design with 25 kHz pulse noise source.

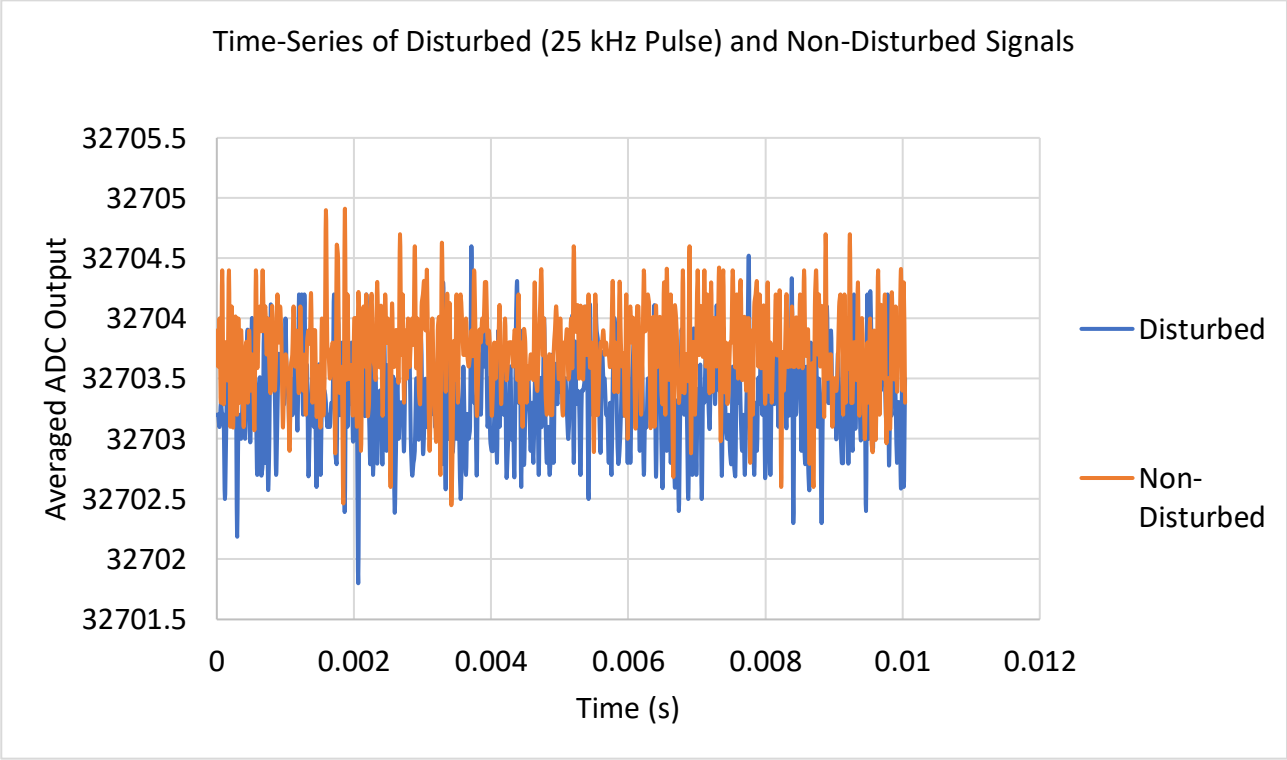


Figure 4.3: Time domain graph for non-split design with 25 kHz pulse noise source.

The time domain signals in Figure 4.2 and Figure 4.3 are shown to contain a large amount of noise, with larger swings in ADC output when using the pulsed disturbance. These graphs show a larger average DC offset in the split-ground design, although the ADC output difference did not vary. The

lack of a meaningful difference between the disturbed and undisturbed time domain series graphs for the two PCBs indicates that the DC shift is not due to current flow from the digital threat into the analogue partition of the ground plane. This would have been explainable by the split in the ground plane usually being beneficial towards these situations. As there is not a meaningful difference between the two PCB designs and DC current flow from the digital threat is unlikely to be the cause of the DC shift, it is possible that the physical separation between the analogue and digital components due to the partitioning scheme and physical separation distance may provide a large enough distance between the digital and analogue components to the point where the current flow does not reach the analogue side of the partition.

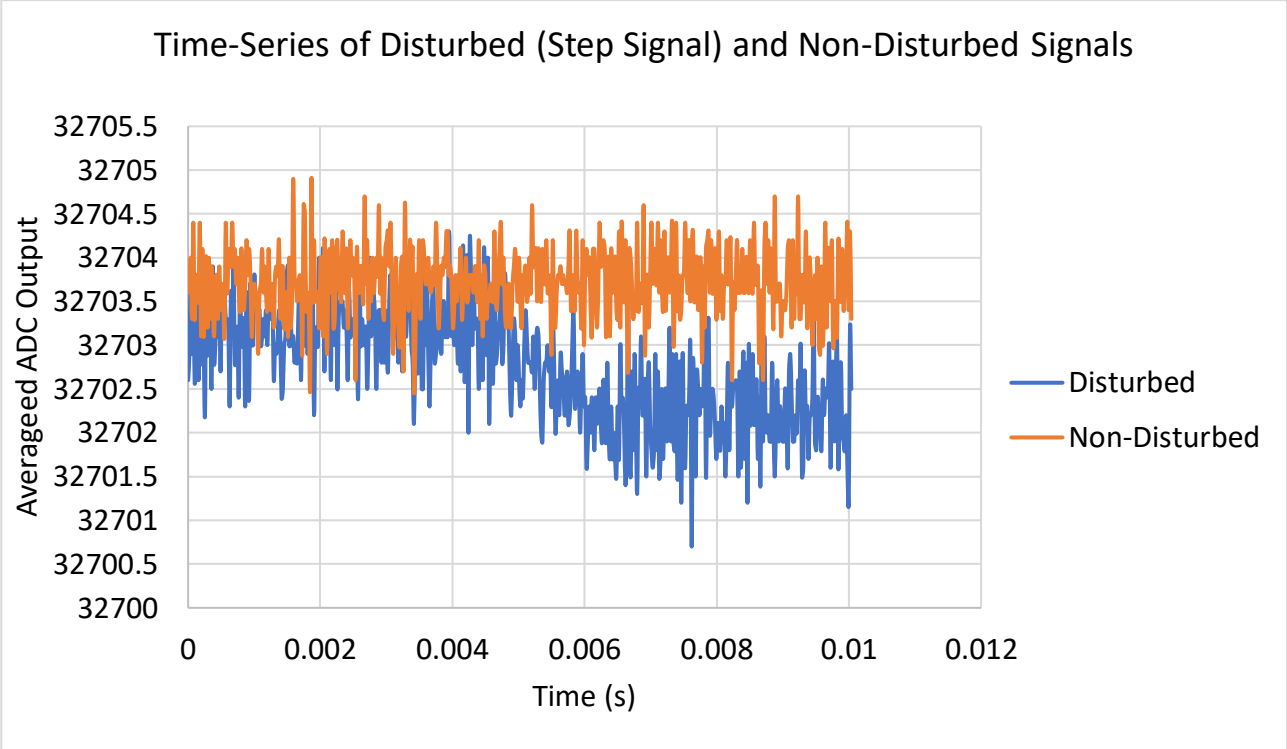


Figure 4.4: Time domain graph for non-split design with step signal noise source.

The time domain experiment was also conducted using a step signal which transitions during the middle of the time sample. The shape of the Figure 4.4 clearly displays the effect of the step signal on the DC offset of the analogue input signal, with the disturbed values reducing with the introduction of the step signal. As the step signal transitions from low to high the DC offset increases, causing the average ADC output do decrease. This could be due to the fact the reference pin is closer to the noise source than the input pins, meaning it is offset more than the input values, which would lead to an overall lower ADC output value. This is consistent with the

data obtained from Figure 4.3 as the digital threat is closer to being uniformly present in the pulsed threat experiment, leading to a DC offset across the entire time domain in comparison to the offset occurring half-way through the time domain for the step function threat experiment.

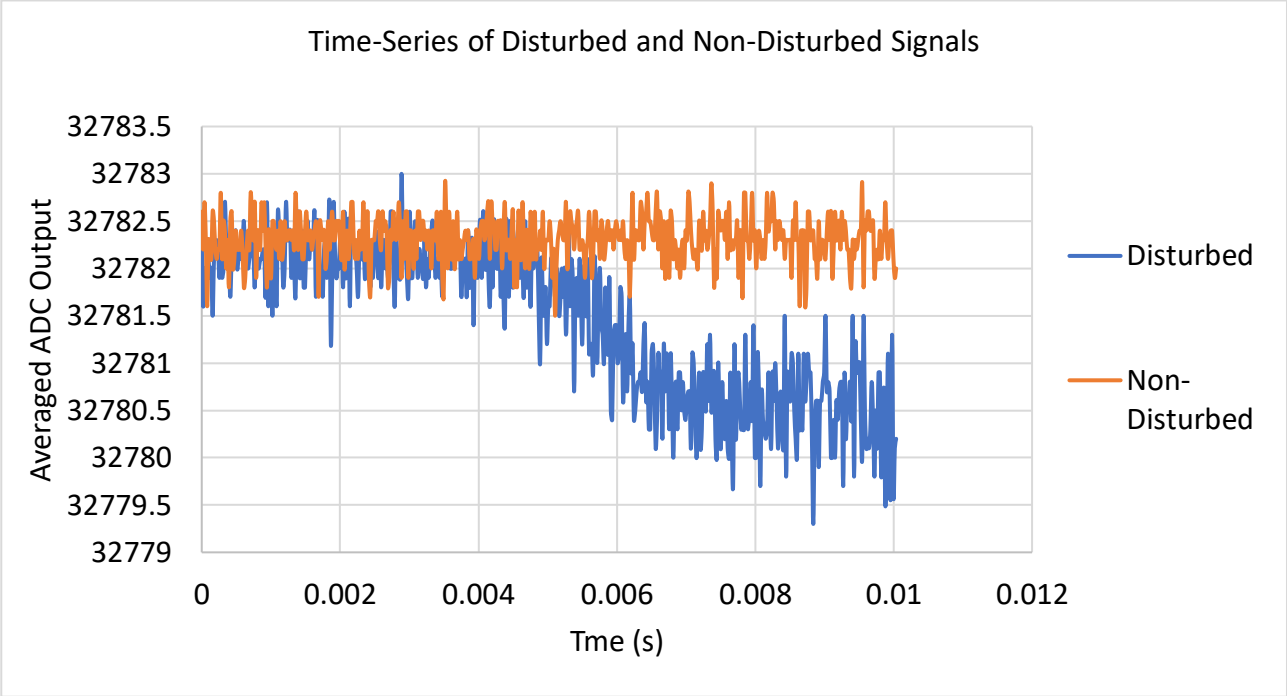


Figure 4.5: Time domain graph for split design with step signal noise source.

Figure 4.5 shows a similar shape to Figure 4.4, with a similar 2 code offset when disturbed, further reinforcing the findings found in the single sample dataset. Although these graphs provide data on changes in quasi-DC voltage between the two PCB designs for the disturbed and undisturbed models, they do not provide conclusive data on the dynamic changes in the digital outputs.

4.2.4 Frequency Domain Experiment

The last experiment carried out on the PCBs was the frequency domain experiment, which used the previously gathered time series data and converted it into the frequency domain using the Fast Fourier Transform in Excel. The Fast Fourier Transform was performed on the pulsed threat data for both the non-split and split ground design PCBs.

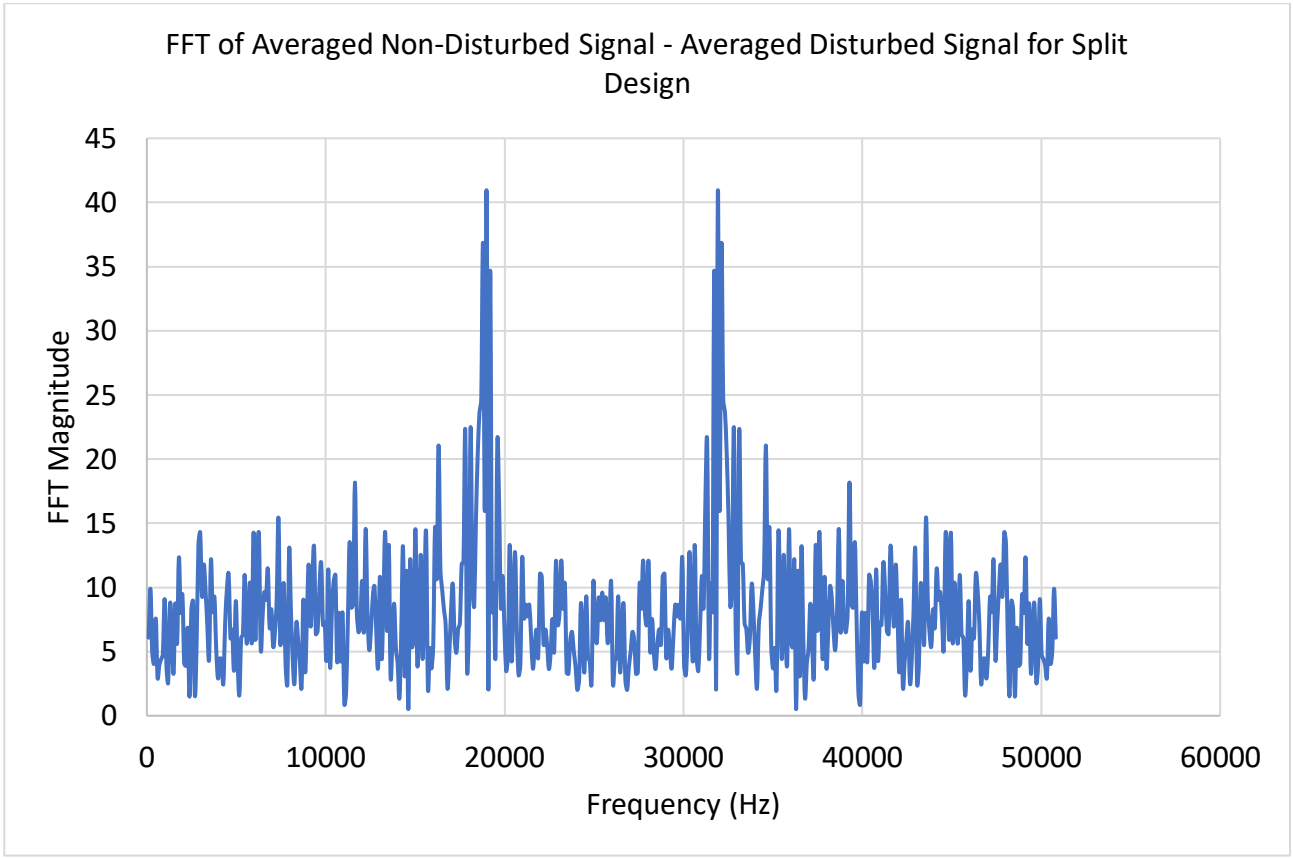


Figure 4.6: Frequency domain graph for split design with 25 kHz pulse signal noise source.

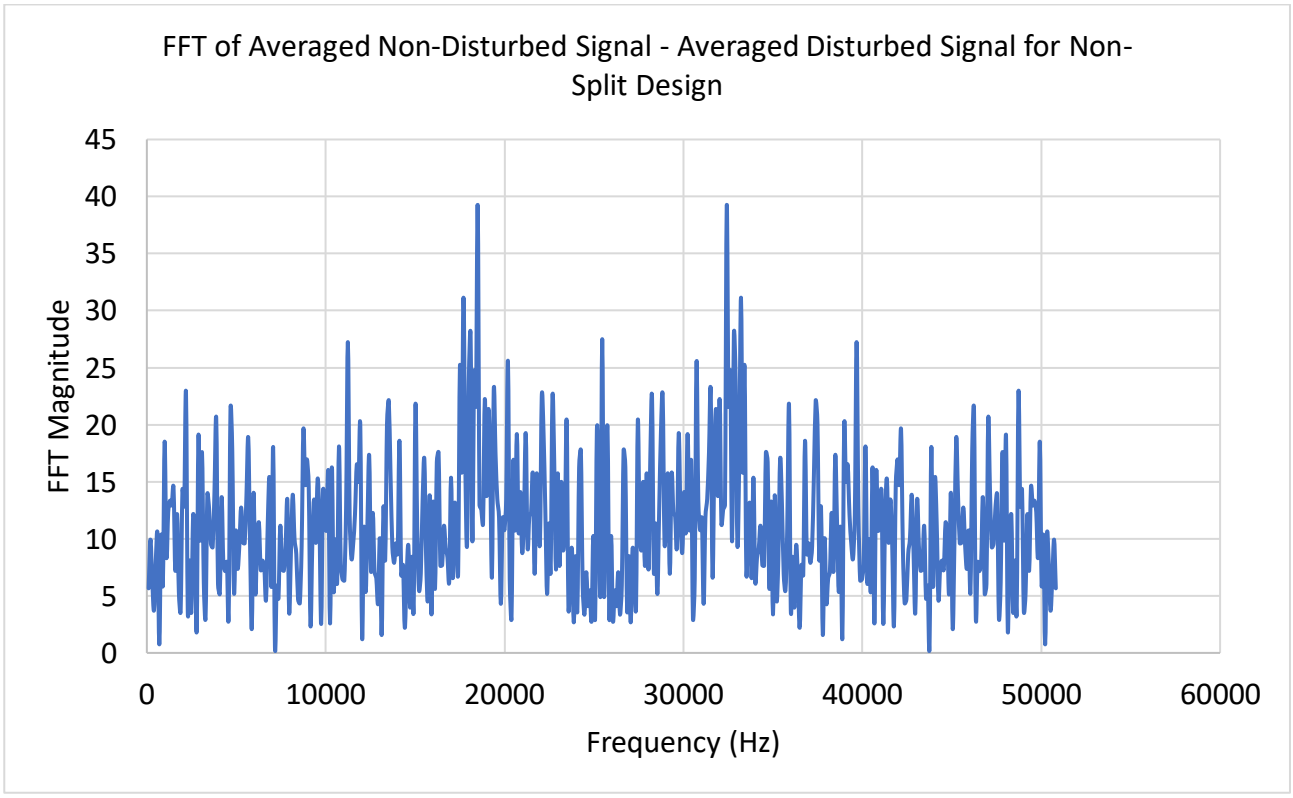


Figure 4.7: Time domain graph for non-split design with 25 kHz pulse signal noise source.

Figure 4.6 and Figure 4.7 both provide a peak frequency of approximately 18 kHz, however these graph are relatively inconclusive as evidence of the dynamic change in voltage. The sample rate for the PCB was measured to be consistently 25 kHz, however this low sample rate could have caused the inconsistency in FFT data.

4.3 Discussion/Summary

Overall, the PCB has shown to be extremely capable of sampling data and providing a sizeable digital threat, with the two PCBs' similar results indicating that the sampling is equivalent between the two PCBs. The consistency in code error between the two PCBs also indicates the success of the PCB's ability to provide an equivalent digital threat as the offset was consistently equal between the two designs for the time domain and frequency domain responses. There were some shortcomings with the data, as it was inconclusive in terms of dynamic changes, however this could be improved through the use of a higher sample rate to improve the validity of the results. Being able to simultaneously switch all of the transmission lines would also provide a more effective and clear set of results as the injected noise would be more likely to appear amongst the noise already within the system. The project was created with an uncertain outcome due to the lack of quantitative evidence of PCB ground plane design effectiveness, however the development of the PCB was highly successful as it performed or had the capability to perform all the actions required in the aims of the project.

5 Conclusions and Future Work

5.1 Conclusions

The main outcome of the research in this report concludes that it is possible to obtain quantitative data on mixed signal crosstalk using a bespoke PCB design and that it is possible to control equivalent circuits whilst providing equivalent digital threats. It also concludes that research studies on mixed signal PCB ground plane testing is sparse but viable when using an effective research PCB.

5.2 Future work

If this project was to be undertaken again using similar methods as shown within this report, multiple alterations to the design of PCB would be advisable to improve the performance of the methods used.

One clear improvement for future work includes the adoption of a four-layer PCB stack design to allow more complex routeing from the microcontroller used in the design with the other digital components, specifically the ADC and transmission line buffer. By using a four-layer design, microcontroller pins from one port of the microcontroller could be used by routeing traces between them and the transmission line buffer, allowing a larger simultaneous burst of electrical noise as the entire port's pins can be toggled at the same time – this is restricted in the two-layer design as port pins were not grouped physically on the microcontroller, therefore the pin allocation had to be compromised to use multiple ports.

Another improvement that could be made during future work would be the implementation of either a faster microcontroller or use of an FPGA in the control of the ADC and transmission line buffer. The microcontroller used in the design was limited in clock speed and a faster microcontroller with a compatible pin layout would improve the data sample rate.

This relates to another aspect to consider for future work, which is a repeat of the experiments in the report but using a short sample size. This shorter sample size would allow for more sensitivity to the dynamic changes in the digital threat, providing more accurate and conclusive Fast Fourier Transform data.

References

[1] Dr. P. Wright, Class Lecture, "High Speed Digital and Mixed Signal Design - Topic 3 – Fundamentals", EEEN30071, University of Manchester, 2020.

[2] H. W. Ott, "Partitioning and Layout of a Mixed-Signal PCB", Printed Circuit Design, 2001.

[3] Dr. P. Wright, Class Lecture, "High Speed Digital and Mixed Signal Design - Topic 2 – High Speed Digital Design", EEEN30071, University of Manchester, 2020.

[4] Dr. P. Wright, Class Lecture, “High Speed Digital and Mixed Signal Design - Topic 3 – Mixed Signal Design”, EEEN30071, University of Manchester, 2020.

[5] W. Kester, “Mixed Signal and DSP Design Techniques”, 2003.

[6] ON Semiconductor, 74AC244, 74ACT244 Datasheet, 1988. [Online]. Available: 74AC244, 74ACT244 Octal Buffer/Line Driver with 3-STATE Outputs (farnell.com).

[7] Holsworthy, RN73C2A140RBTDF Datasheet, 2024. [Online]. Available: product-1676185-2.datasheet.pdf (te.com).

[8] Analog Devices, AD7686 Datasheet, 2014. [Online]. Available: AD7686 (Rev. C) (analog.com).

[9] Microchip, MCP1825/MCP1825S Datasheet, 2008. [Online]. Available: 500 mA, Low Voltage, Low Quiescent LDO Regulator (microchip.com).

[10] Linear Technology, LTC6905-XXX Series Datasheet, 2005. [Online]. Available: LTC6905-XXX Series - Fixed Frequency SOT-23 Oscillator (ciiva.com)

[11] STMicroelectronics, LFXX Datasheet, 2017. [Online]. Available: Very low drop voltage regulator with inhibit function (farnell.com)

[12] Analog Devices, ADR430/ADR431/ADR433/ADR434/ADR435 Datasheet, 2018. [Online]. Available: ADR430/ADR431/ADR433/ADR434/ADR435 (Rev. N) (analog.com)

[13] Analog Devices, AD8031/AD8032 Datasheet, 2014. [Online]. Available: AD8031/AD8032 (Rev. G) (analog.com).

Appendices

A Project Outline

1. Background of the Project

The background of this project consists of the techniques developed and used in mixed signal PCB design in order to improve the performance of the circuits. These performance increases consist of partitioning the PCB design into separate sections for analogue and digital signals and splitting the PCB ground plane into two sections, with a bridge connecting the two, located under an analogue-

to-digital converter. This is done to reduce the interference on the analogue signals from the digital signals to reduce error during conversion and therefore gathering evidence to show the effectiveness of splitting the ground is main focus for the project.

2. Motivation for the Project

Historically, manufacturers of integrated circuit components have advised circuit layout designers to split the ground plane when designing a mixed signal PCB, however this advice has been shown to be misleading as although effective circuits can be made using ground plane splitting, many potential problems are introduced. My main motivation for this project is to provide evidence through experimental testing to quantitatively show the benefit of this split-ground design. This project was chosen in order to improve my knowledge and skill in implementing mixed signal PCB designs, whilst being able to provide supporting evidence for PCB techniques recommended by manufacturers. With mixed-signal design being more sparsely researched than areas of PCB design such as electromagnetic compatibility design, another motivation is to provide a unique study that can aid people who want to undertake mixed-signal PCB design.

3. Overall Aims

The main aim of the project involves testing two different ground layouts – one layout including a single bridge between a split ground plane and another including two bridges between the split ground plane. By doing this I aim to show the difference in effect on the interactions of the digital and analogue signals between these two designs. I aim to use different digital threats, one of these being a high current, medium speed, quickly changing signal, in order to generate a large noise within the circuit and observe and measure the effect of this current on the analogue signal for the two different split ground designs. The other digital threat would be controlled digital loops which could produce bursts of digital noise simultaneously, being controlled by a PLD connected to a microcontroller which is used to control the pattern, speed and intensity of the electrical signals.

4. Provisional Project Plan

4.1. Initial Research (and Methodology Research)

This deliverable includes researching the techniques used for effective PCB design, including the techniques being tested as part of the project aims. A document will be made including the

research obtained from multiple academic sources and component manufacturer sources. This information will then be used to decide what components must be used in the PCB design in order to test the effect of the different split-ground designs as accurately as possible, as per the project aims.

4.2. Circuit Component List

The second main deliverable for the project is a circuit component list. This is a small deliverable that includes the required components and planned use for each component within the experimental circuit, along with associated problems or potential difficulties with each component and cost. This is required in order to complete the PCB schematic effectively as it provides a guide on which connections are made between electrical components. It is also required in order to accurately estimate and keep track of the cost of the project as the majority of the project costs are due to the PCBs designed and tested.

4.3. Experimental Mixed-Signal PCB Design

The schematic design largely focusses on the top layer of the PCB, displaying the connectivity of the components required in the circuit. This schematic does not show the details of where the tracks and components will be placed on the PCB, however it is vital as part of the planning stage for the PCB design as it is easier to alter than later stages in the PCB design. The PCB layout designs provide the design for the physical PCBs which will be manufactured and tested. These designs will include the connections required by the schematic with the components shown in the schematic and components list, whilst also including the design techniques previously researched. This deliverable should provide a PCB which incorporates the required digital threats, analogue signal connections, split ground plane designs and a method of extracting the required data, a method of controlling the digital signals, and all supporting electrical components. After the PCB has been manufactured, the logic components on the printed circuit board must be programmed.

4.4. Draft Introduction

This should contain the same introduction structure as the final report, providing an overview of the project and the background and motivation for the project.

4.5. PCB Testing

The PCB should be tested to measure the difference the two split-ground PCB designs have on the effect of the digital threat currents have on the analogue signals in the analogue partition of the

PCB. The change in the magnitude of the noise when the switching threat is active should be measured and then matched up to the waveforms provided by the switching component. In addition, the spikes in noise when the switching component switches from low to high current should also be tracked, measured and compared to the input current waveform. The effect of the current from the simultaneous, fast digital threat from the programmable logic device should also be measured by measuring the waveforms of the input signal and the analogue signal at the same timeframe for different controlled digital signals.

4.6. Draft Project Methodology

This should consist of the methods, developments, designs and implementations used within the project, with justification for actions taken within the project. Links to background information and motivations for the project should also be included.

4.7. Draft Final Report

This should include the previous draft introduction and draft methodology deliverables, along with results obtained from the measurements taken during the project. It should also include conclusions and information about future work.

4.8. Final Report

This should be the same as the draft final report but with amendments and improvements based on the feedback from the project supervisor, adhering to presentation requirements.

4.9. Final Presentation

The technical achievements of the project should be presented and then questions must be answered. Preparation for the final demonstration should be done by preparing an effective script and rehearsing.

4.10. Project Risks

Due to the project involving PCB design and testing, the majority of the risks are associated with the PCB design and production, rather than other external risks. One main risk is that the PCB could require a redesign in some aspect – this can use up a substantial amount of time due to manufacturing timeframes but can be reduced by checking the PCB design with the project supervisor before it is manufactured. Another main risk is that the PCB is manufactured incorrectly – this can be reduced by providing all necessary manufacturing information as clearly as possible.

A third risk is that I or my supervisor could be temporarily unwell or unavailable for a meeting in the usual time slot during the project, which could cause deliverables to be under more time pressure due to a reduction in working speed or face-to-face communication – this can be reduced by starting work on deliverables and submitting them earlier than required to provide a time buffer. Meetings can also be rearranged when required.

B Risk Assessment

MANCHESTER 1824
The University of Manchester

General Risk Assessment Form

Date: (1)	**Assessed by:** (2)	**Checked / Validated* by:** (3)	**Location:** (4)	**Assessment ref no** (5)	**Review date:** (6)
15/10/2023			MECD Engineering Building A + B		

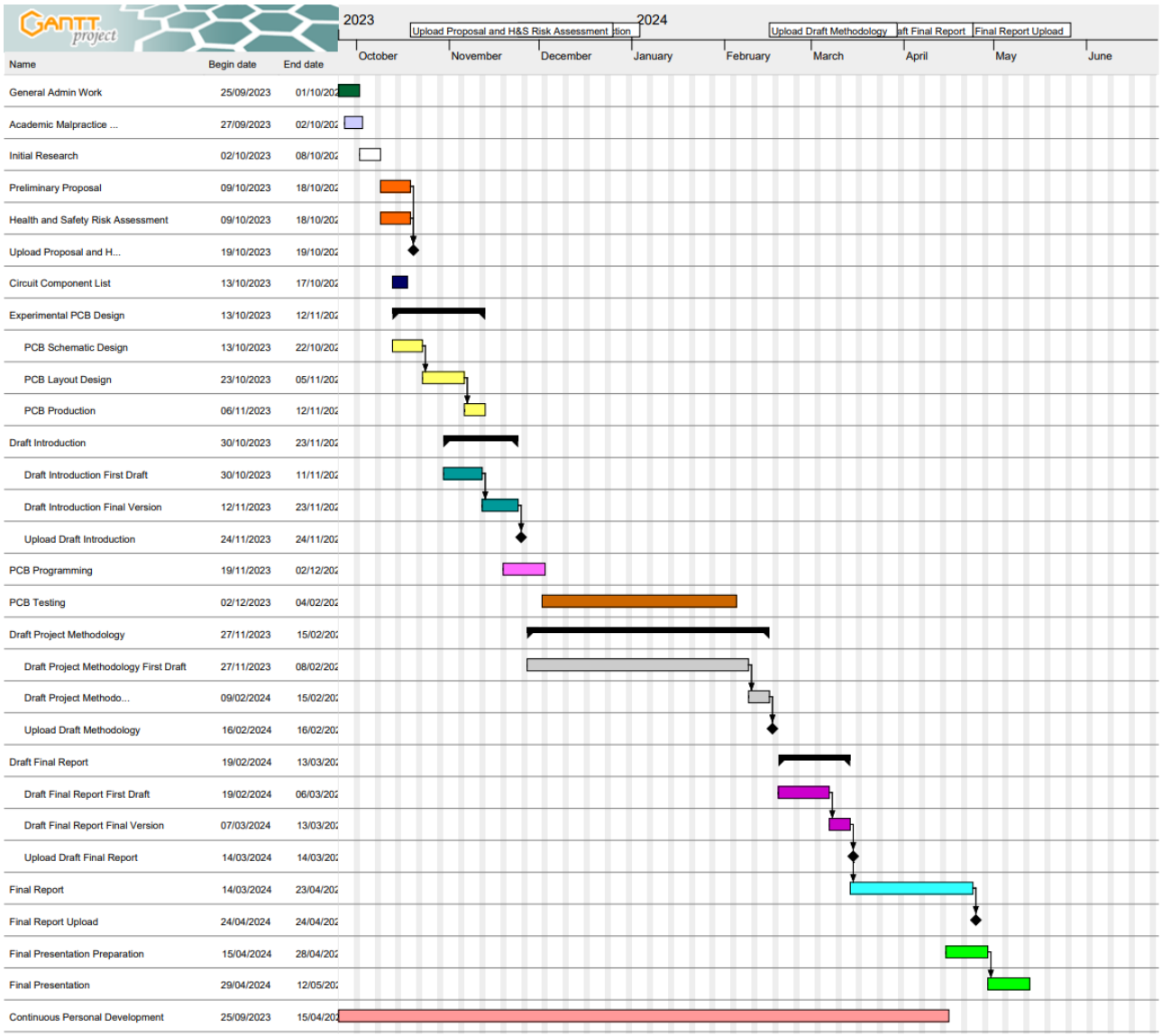
Task / premises: (7)
Use of the dry lab, maker areas, PC clusters and computer workstations.

Activity (8)	**Hazard** (9)	**Who might be harmed and how** (10)	**Existing measures in place to control the risk** (11)	**Risk rating** (12)	**Result** (13)
Use of computers.	Long exposure to computer screen, long period of sitting without movement.	Computer users may be harmed through neck and back pain, eye strain.	A chair with changeable position and height is provided, with enough lighting provided in areas containing computer workstations.	LOW	A
Moving through the computer clusters and maker spaces.	Tripping hazards such as loose wires.	Computer cluster and maker space users may be harmed by tripping over wires used in connecting parts of the cluster.	Cables are kept away from walking areas, obstacles are removed from the floor, bins are provided for garbage, room is sufficiently lit so the computer cluster and maker space users can see any potential obstacles clearly.	LOW	A

Activity (8)	**Hazard** (9)	**Who might be harmed and how** (10)	**Existing measures in place to control the risk** (11)	**Risk rating** (12)	**Result** (13)
Soldering.	Hot soldering iron, fumes from solder, toxic material (lead).	Soldering iron user could receive minor or more serious burns from the soldering iron due to its high temperature. Soldering iron user or nearby people could also be irritated by the fumes produced when soldering or potentially get an asthma attack from exposure to the fumes.	A fume extractor is provided in the dry lab to remove solder fumes. To reduce the chance of burning, increased caution can be exercised when handling the soldering iron to reduce the chance of contact with the soldering iron. The soldering irons also have soldering iron holders to place the tool in when not currently being used.	LOW	A
PCB Assembling.	Polarised electrical components such as electrolytic capacitors	The PCB assembler could receive a burn from components that explode due to incorrect polarity when current is applied.	Datasheets are checked before implementing electrical components to check for the correct component orientation. Eye protection can also be used to reduce chance of injury to eyes.	LOW	A
Testing and measuring electrical signals.	Large current electrical signals.	There is a potential risk of electric shock to the person taking measurements from the PCB.	Careful handling of live PCB during testing reduces the risk of electric shock.	LOW	A
Use of cutters/ pliers.	Sharp blades on tools.	There is a risk of the user's skin being cut or pierced by cutters.	Careful handling of cutters and other sharp tools reduces the chance of accidentally cutting oneself.	LOW	A

Activity (8)	Hazard (9)	Who might be harmed and how (10)	Existing measures in place to control the risk (11)	Risk rating (12)	Result (13)
Lone Working.	Distance from potential help or other people in case of an emergency.	The person lone working may not be able to receive assistance in a sufficient amount of time due to a lack of nearby support.	E-mail and telephone access to help and first aid is provided by the University Security through information provided on the back of student ID cards. The health and safety induction lecture also provided information on what to do during in an emergency such as a fire emergency.	LOW	A
Working from home.	Same hazards to working at a computer cluster or workstation.	The person working at home may be harmed by the same hazards described in the use of computers activity.	The same safety procedures can be employed as used for working in the university environment. If soldering at home, components are soldered in a ventilated area, using non-leaded solder.	LOW	A
Moving through the dry lab.	Tripping/falling over or into other people.	Anyone using the dry lab.	Metal lockers are provided for temporary storage of bags and coats whilst using the dry lab. Any tools or equipment being used in the dry lab is placed in a safe area on the desks.	LOW	A

C Project Plan (GANTT Chart)



D Risk Register

Group Number:			Submission Date:	26/04/2024	
Group Members:	Andrew Slater				

Project Risk	Severity			Potential			Score (Severity x Potential)	Mitigation Measures	Owner
	L	M	H	L	M	H	L=1, M=2, H=3		
PCB isn't constructed on-time		x			x		4	Build PCB in advance	PCB developer
PCB does not function correctly and has to be replaced			x		x		6	Build back-up PCBs	PCB Developer
Data gathered from PCB is not valid		x			x		4	Use multiple methods of testing	PCB Developer
Components for PCB cannot be sourced		x		x			2	Use alternative parts if ideal ones are unavailable	PCB Developer
PCB components break		x			x		4	Purchase spare components	PCB Developer

E Code Used in PCB Design

This code was used when sampling the data using a pulsed digital threat. The same code was used for the step signal and single sample programs, however there was a loop around the GPIO pin toggling sections based on the required toggling pattern.

```
/* USER CODE BEGIN Header */
/**
  ******************************************************************************
  * @file           : main.c
  * @brief          : Main program body
  ******************************************************************************
  * @attention
  *
  * Copyright (c) 2024 STMicroelectronics.
  * All rights reserved.
  *
  * This software is licensed under terms that can be found in the LICENSE file
  * in the root directory of this software component.
  * If no LICENSE file comes with this software, it is provided AS-IS.
  *
  ******************************************************************************
  */
/* USER CODE END Header */
/* Includes ------------------------------------------------------------------*/
#include "main.h"

/* Private includes ----------------------------------------------------------*/
/* USER CODE BEGIN Includes */

/* USER CODE END Includes */

/* Private typedef -----------------------------------------------------------*/
/* USER CODE BEGIN PTD */

/* USER CODE END PTD */

/* Private define ------------------------------------------------------------*/
/* USER CODE BEGIN PD */
#define BUFSIZE 10000
/* USER CODE END PD */
```

```
/* Private macro -------------------------------------------------------------*/
/* USER CODE BEGIN PM */

/* USER CODE END PM */

/* Private variables ---------------------------------------------------------*/
SPI_HandleTypeDef hspi2;

TIM_HandleTypeDef htim3;
int toggleTL = 0;
   int toggleCNV = 0;
   int toggleSCK = 0;
   int CNVcounter = 0;
   uint16_t rxdata[BUFSIZE];
   uint8_t txdata1[2];
   uint8_t txdata2[2];
   uint8_t buffer[6];
   int toggleReceive = 0;
   int j = 3;
   int bufCounter = 0;
   int tempVal1 = 0;
   int tempVal2 = 0;
/* USER CODE BEGIN PV */

/* USER CODE END PV */

/* Private function prototypes -----------------------------------------------*/
void SystemClock_Config(void);
static void MX_GPIO_Init(void);
static void MX_TIM3_Init(void);
static void MX_SPI2_Init(void);
/* USER CODE BEGIN PFP */

/* USER CODE END PFP */

/* Private user code ---------------------------------------------------------*/
/* USER CODE BEGIN 0 */

/* USER CODE END 0 */

/**
  * @brief  The application entry point.
  * @retval int
  */
int main(void)
{
 /* MCU Configuration--------------------------------------------------------*/

  /* Reset of all peripherals, Initializes the Flash interface and the Systick. */
  HAL_Init();


  /* Configure the system clock */
  SystemClock_Config();


  /* Initialize all configured peripherals */
  MX_GPIO_Init();
```

```
  MX_TIM3_Init();
  MX_SPI2_Init();

  txdata1[0] = 0xFF;
  txdata1[1] = 0xFF;
  txdata1[2] = 0x00;
  txdata1[3] = 0x00;
  txdata1[4] = 0xFF; //0xFF
  txdata1[5] = 0xFF; //0xFF
  txdata2[0] = 0x00;
  txdata2[1] = 0x00;

  GPIOB->BSRR |= (GPIO_PIN_12);


  while (1)
  {
        GPIOB->BSRR |= (GPIO_PIN_15);
        GPIOB->BSRR |= (GPIO_PIN_15);
        GPIOB->BSRR |= (GPIO_PIN_15);
        GPIOB->BSRR |= (GPIO_PIN_15);
        GPIOB->BSRR |= (GPIO_PIN_15);
        GPIOB->BSRR |= (GPIO_PIN_15);
        GPIOB->BSRR |= (GPIO_PIN_15);
        GPIOB->BSRR |= (GPIO_PIN_15) << 16;
        HAL_SPI_Receive(&hspi2, (uint8_t *)buffer, 1, HAL_MAX_DELAY);
        if (bufCounter < 10000){rxdata[bufCounter] = ((buffer[1]<<8) | buffer[0]);}
        bufCounter++;

        GPIOB->BSRR |= (GPIO_PIN_15);
        GPIOC->BSRR |= (GPIO_PIN_2 | GPIO_PIN_3);
        GPIOB->BSRR |= (GPIO_PIN_0 | GPIO_PIN_1 | GPIO_PIN_2);
        GPIOA->BSRR |= (GPIO_PIN_0 | GPIO_PIN_1 | GPIO_PIN_7);
        GPIOC->BSRR |= (GPIO_PIN_2 | GPIO_PIN_3) << 16;
        GPIOB->BSRR |= (GPIO_PIN_0 | GPIO_PIN_1 | GPIO_PIN_2) << 16;
        GPIOA->BSRR |= (GPIO_PIN_0 | GPIO_PIN_1 | GPIO_PIN_7) << 16;
        GPIOB->BSRR |= (GPIO_PIN_15) << 16;
        HAL_SPI_Receive(&hspi2, (uint8_t *)buffer, 1, HAL_MAX_DELAY);
        if (bufCounter < 10000){rxdata[bufCounter] = ((buffer[1]<<8) | buffer[0]);}
        bufCounter++;

    /* USER CODE END WHILE */

    /* USER CODE BEGIN 3 */
  }
  /* USER CODE END 3 */
}

/**
  * @brief System Clock Configuration
  * @retval None
  */
void SystemClock_Config(void)
{
  RCC_OscInitTypeDef RCC_OscInitStruct = {0};
  RCC_ClkInitTypeDef RCC_ClkInitStruct = {0};

  /** Configure the main internal regulator output voltage
  */
```

```
  __HAL_RCC_PWR_CLK_ENABLE();
  __HAL_PWR_VOLTAGESCALING_CONFIG(PWR_REGULATOR_VOLTAGE_SCALE2);

  /** Initializes the RCC Oscillators according to the specified parameters
  * in the RCC_OscInitTypeDef structure.
  */
  RCC_OscInitStruct.OscillatorType = RCC_OSCILLATORTYPE_HSI;
  RCC_OscInitStruct.HSIState = RCC_HSI_ON;
  RCC_OscInitStruct.HSICalibrationValue = RCC_HSICALIBRATION_DEFAULT;
  RCC_OscInitStruct.PLL.PLLState = RCC_PLL_ON;
  RCC_OscInitStruct.PLL.PLLSource = RCC_PLLSOURCE_HSI;
  RCC_OscInitStruct.PLL.PLLM = 8;
  RCC_OscInitStruct.PLL.PLLN = 80;
  RCC_OscInitStruct.PLL.PLLP = RCC_PLLP_DIV4;
  RCC_OscInitStruct.PLL.PLLQ = 3;
  if (HAL_RCC_OscConfig(&RCC_OscInitStruct) != HAL_OK)
  {
    Error_Handler();
  }

  /** Initializes the CPU, AHB and APB buses clocks
  */
  RCC_ClkInitStruct.ClockType = RCC_CLOCKTYPE_HCLK|RCC_CLOCKTYPE_SYSCLK
                              |RCC_CLOCKTYPE_PCLK1|RCC_CLOCKTYPE_PCLK2;
  RCC_ClkInitStruct.SYSCLKSource = RCC_SYSCLKSOURCE_PLLCLK;
  RCC_ClkInitStruct.AHBCLKDivider = RCC_SYSCLK_DIV1;
  RCC_ClkInitStruct.APB1CLKDivider = RCC_HCLK_DIV1;
  RCC_ClkInitStruct.APB2CLKDivider = RCC_HCLK_DIV1;

  if (HAL_RCC_ClockConfig(&RCC_ClkInitStruct, FLASH_LATENCY_1) != HAL_OK)
  {
    Error_Handler();
  }
}

/**
  * @brief SPI2 Initialization Function
  * @param None
  * @retval None
  */
static void MX_SPI2_Init(void)
{

  /* USER CODE BEGIN SPI2_Init 0 */

  /* USER CODE END SPI2_Init 0 */

  /* USER CODE BEGIN SPI2_Init 1 */

  /* USER CODE END SPI2_Init 1 */
  /* SPI2 parameter configuration*/
  hspi2.Instance = SPI2;
  hspi2.Init.Mode = SPI_MODE_MASTER;
  hspi2.Init.Direction = SPI_DIRECTION_2LINES;
  hspi2.Init.DataSize = SPI_DATASIZE_16BIT;
  hspi2.Init.CLKPolarity = SPI_POLARITY_LOW;
  hspi2.Init.CLKPhase = SPI_PHASE_2EDGE;
  hspi2.Init.NSS = SPI_NSS_SOFT;
  hspi2.Init.BaudRatePrescaler = SPI_BAUDRATEPRESCALER_2;
```

```
  hspi2.Init.FirstBit = SPI_FIRSTBIT_MSB;
  hspi2.Init.TIMode = SPI_TIMODE_DISABLE;
  hspi2.Init.CRCCalculation = SPI_CRCCALCULATION_DISABLE;
  hspi2.Init.CRCPolynomial = 10;
  if (HAL_SPI_Init(&hspi2) != HAL_OK)
  {
    Error_Handler();
  }
  /* USER CODE BEGIN SPI2_Init 2 */

  /* USER CODE END SPI2_Init 2 */

}

/**
  * @brief TIM3 Initialization Function
  * @param None
  * @retval None
  */
static void MX_TIM3_Init(void)
{

  /* USER CODE BEGIN TIM3_Init 0 */

  /* USER CODE END TIM3_Init 0 */

  TIM_ClockConfigTypeDef sClockSourceConfig = {0};
  TIM_MasterConfigTypeDef sMasterConfig = {0};

  /* USER CODE BEGIN TIM3_Init 1 */

  /* USER CODE END TIM3_Init 1 */
  htim3.Instance = TIM3;
  htim3.Init.Prescaler = 0;
  htim3.Init.CounterMode = TIM_COUNTERMODE_UP;
  htim3.Init.Period = 0;
  htim3.Init.ClockDivision = TIM_CLOCKDIVISION_DIV1;
  htim3.Init.AutoReloadPreload = TIM_AUTORELOAD_PRELOAD_DISABLE;
  if (HAL_TIM_Base_Init(&htim3) != HAL_OK)
  {
    Error_Handler();
  }
  sClockSourceConfig.ClockSource = TIM_CLOCKSOURCE_INTERNAL;
  if (HAL_TIM_ConfigClockSource(&htim3, &sClockSourceConfig) != HAL_OK)
  {
    Error_Handler();
  }
  sMasterConfig.MasterOutputTrigger = TIM_TRGO_RESET;
  sMasterConfig.MasterSlaveMode = TIM_MASTERSLAVEMODE_DISABLE;
  if (HAL_TIMEx_MasterConfigSynchronization(&htim3, &sMasterConfig) != HAL_OK)
  {
    Error_Handler();
  }
  /* USER CODE BEGIN TIM3_Init 2 */

  /* USER CODE END TIM3_Init 2 */

}
```

```c
/**
  * @brief GPIO Initialization Function
  * @param None
  * @retval None
  */
static void MX_GPIO_Init(void)
{
  GPIO_InitTypeDef GPIO_InitStruct = {0};
/* USER CODE BEGIN MX_GPIO_Init_1 */
/* USER CODE END MX_GPIO_Init_1 */

  /* GPIO Ports Clock Enable */
  __HAL_RCC_GPIOH_CLK_ENABLE();
  __HAL_RCC_GPIOC_CLK_ENABLE();
  __HAL_RCC_GPIOA_CLK_ENABLE();
  __HAL_RCC_GPIOB_CLK_ENABLE();

  /*Configure GPIO pin Output Level */
  HAL_GPIO_WritePin(GPIOC, GPIO_PIN_2, GPIO_PIN_RESET);

  /*Configure GPIO pin Output Level */
  HAL_GPIO_WritePin(GPIOA, GPIO_PIN_0|GPIO_PIN_1|GPIO_PIN_2|GPIO_PIN_3
                          |GPIO_PIN_6|GPIO_PIN_7, GPIO_PIN_RESET);

  /*Configure GPIO pin Output Level */
  HAL_GPIO_WritePin(GPIOB, GPIO_PIN_0|GPIO_PIN_1|GPIO_PIN_2|GPIO_PIN_12
                          |GPIO_PIN_15, GPIO_PIN_RESET);

  /*Configure GPIO pin : PC2 */
  GPIO_InitStruct.Pin = GPIO_PIN_2;
  GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
  GPIO_InitStruct.Pull = GPIO_NOPULL;
  GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
  HAL_GPIO_Init(GPIOC, &GPIO_InitStruct);

  /*Configure GPIO pins : PA0 PA1 PA2 PA3
                           PA6 PA7 */
  GPIO_InitStruct.Pin = GPIO_PIN_0|GPIO_PIN_1|GPIO_PIN_2|GPIO_PIN_3
                          |GPIO_PIN_6|GPIO_PIN_7;
  GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
  GPIO_InitStruct.Pull = GPIO_NOPULL;
  GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
  HAL_GPIO_Init(GPIOA, &GPIO_InitStruct);

  /*Configure GPIO pins : PB0 PB1 PB2 PB12
                           PB15 */
  GPIO_InitStruct.Pin = GPIO_PIN_0|GPIO_PIN_1|GPIO_PIN_2|GPIO_PIN_12
                          |GPIO_PIN_15;
  GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
  GPIO_InitStruct.Pull = GPIO_NOPULL;
  GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
  HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);

/* USER CODE BEGIN MX_GPIO_Init_2 */
/* USER CODE END MX_GPIO_Init_2 */
}

/* USER CODE BEGIN 4 */
```

```c
/* USER CODE END 4 */

/**
  * @brief  This function is executed in case of error occurrence.
  * @retval None
  */
void Error_Handler(void)
{
  /* USER CODE BEGIN Error_Handler_Debug */
  /* User can add his own implementation to report the HAL error return state */
  __disable_irq();
  while (1)
  {
  }
  /* USER CODE END Error_Handler_Debug */
}

#ifdef  USE_FULL_ASSERT
/**
  * @brief  Reports the name of the source file and the source line number
  *         where the assert_param error has occurred.
  * @param  file: pointer to the source file name
  * @param  line: assert_param error line source number
  * @retval None
  */
void assert_failed(uint8_t *file, uint32_t line)
{
  /* USER CODE BEGIN 6 */
  /* User can add his own implementation to report the file name and line number,
     ex: printf("Wrong parameters value: file %s on line %d\r\n", file, line) */
  /* USER CODE END 6 */
}
#endif /* USE_FULL_ASSERT */
```