

Basics of Active and Nonlinear High-Frequency Electronics



UNIVERSITÀ
DEGLI STUDI
DI BRESCIA

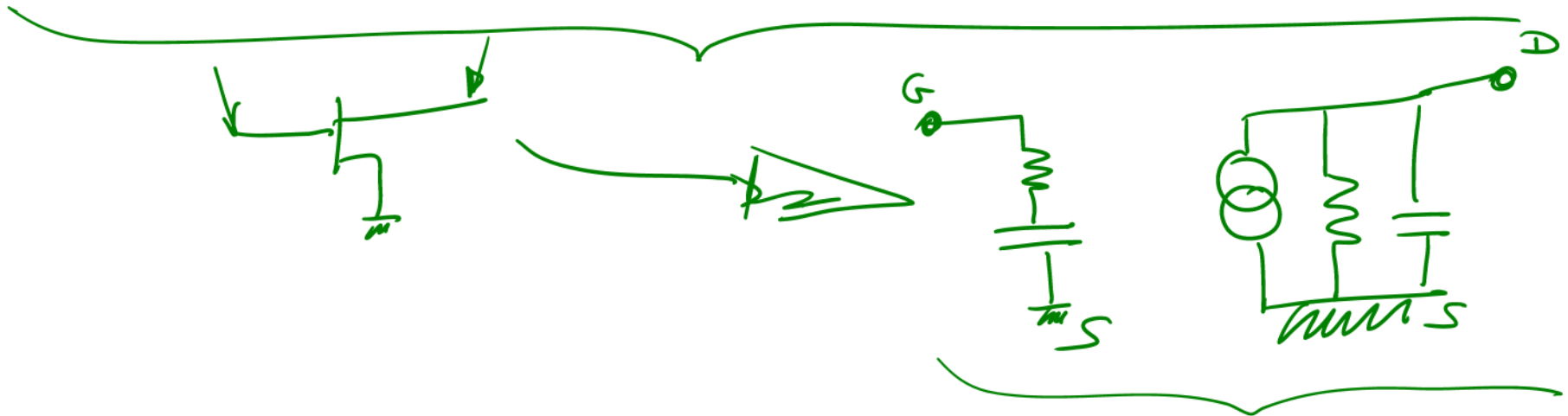


Basics of Active and Nonlinear High-Frequency Electronics

- ❑ Chapter I : Introduction to active high-frequency circuits in communication systems
- ❑ Chapter II : Introduction to the Non-linear Electrical Modeling of microwave transistors
- ❑ Chapter III : Design method of narrow-band power amplifiers
- ❑ Chapter IV : Architectures of high-frequency mixers
- ❑ Chapter V : Architectures of wideband resistive and distributed power amplifiers
- ❑ Chapter VI : Architectures of non-linear active circuits controlled by cold HEMTs

Chapter II :

Introduction to the Non-linear Electrical Modeling of microwave transistors

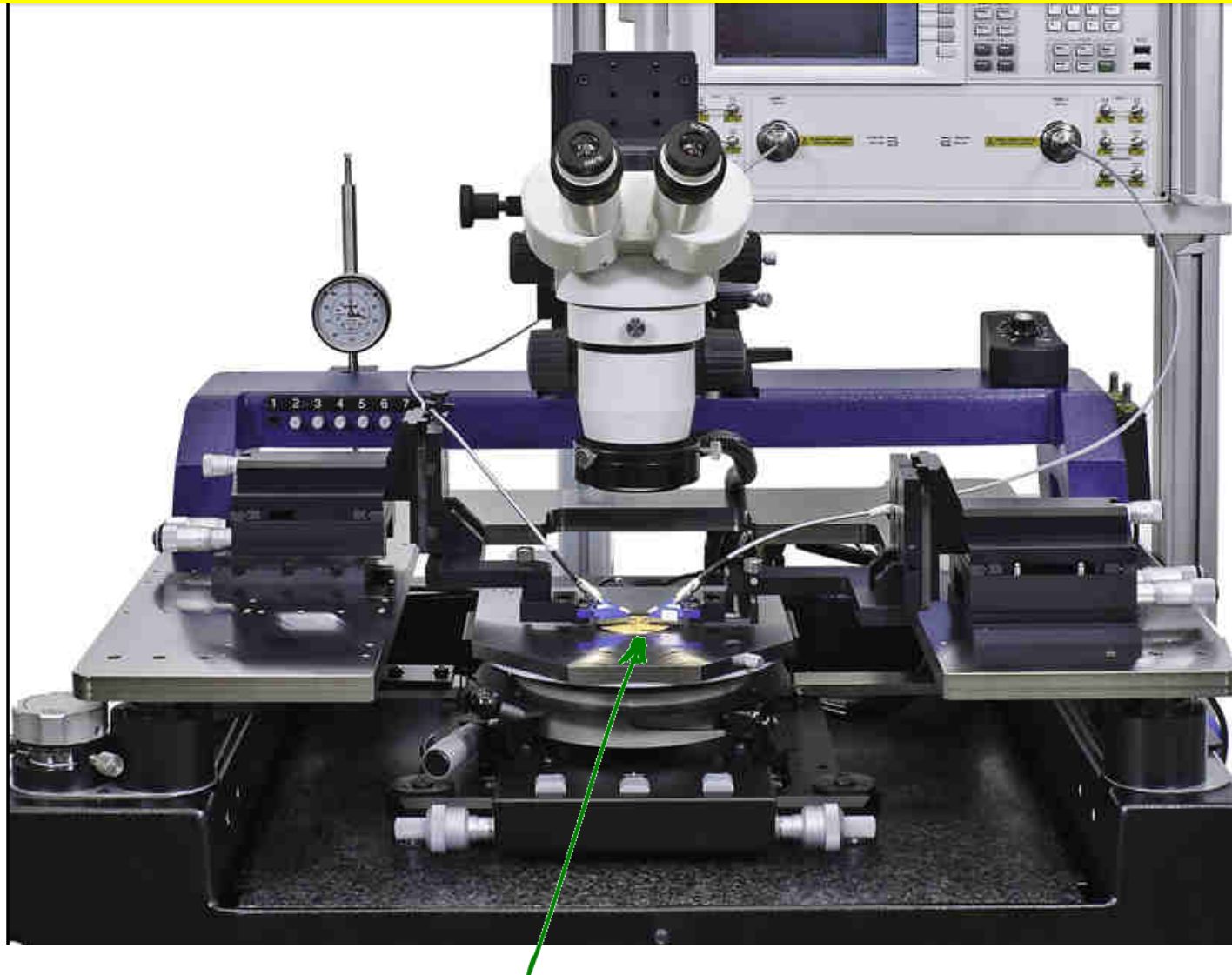


High-frequency Pulsed Measurement Systems

{ On-wafer Probing Stations
for RF/Microwave circuits

E(rasmus) M(undus) on Innovative Microwave Electronics and Optics

On-wafer probing stations



E(rasmus) Mundus on Innovative Microwave Electronics and Optics On-wafer probing stations

DUT

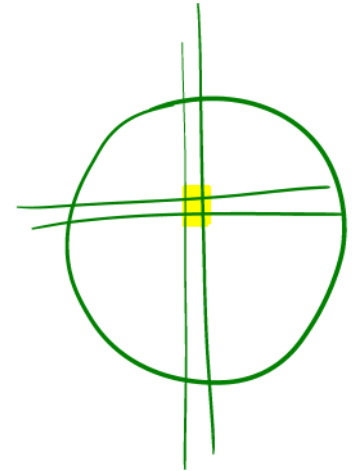
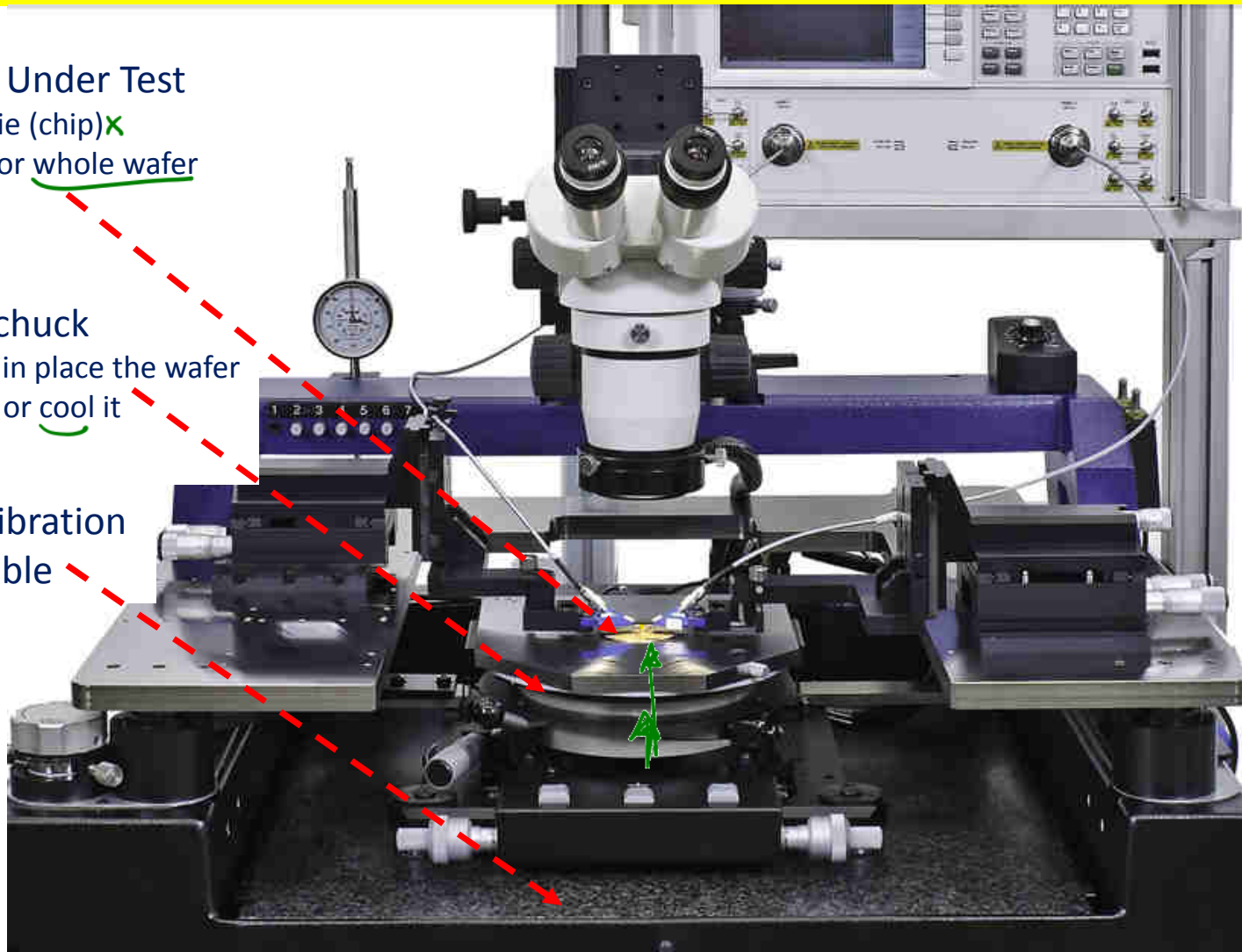
Device Under Test

- small die (chip) ~~x~~
- partial or whole wafer

Wafer chuck

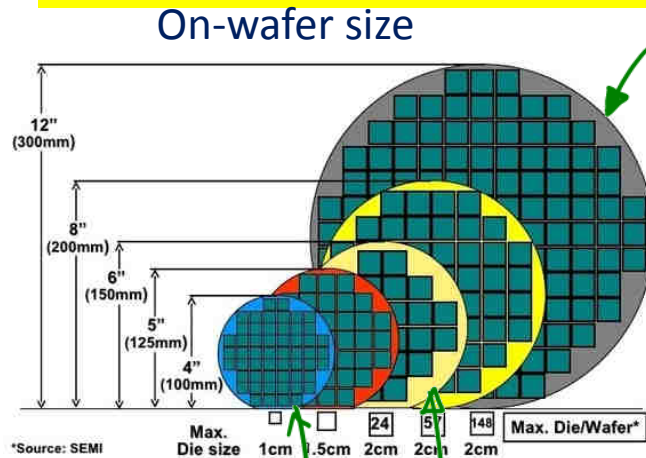
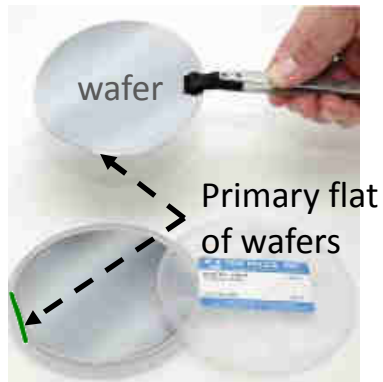
- to hold in place the wafer
- to heat or cool it

Anti- Vibration
Table

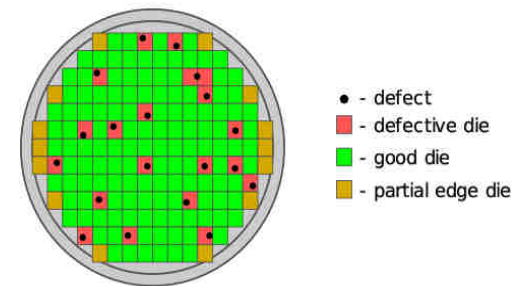


400 k€ "wafer run"

Wafer chuck and Anti-vibration table

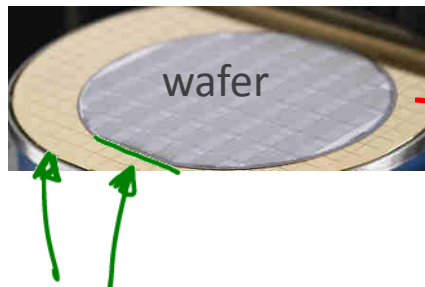
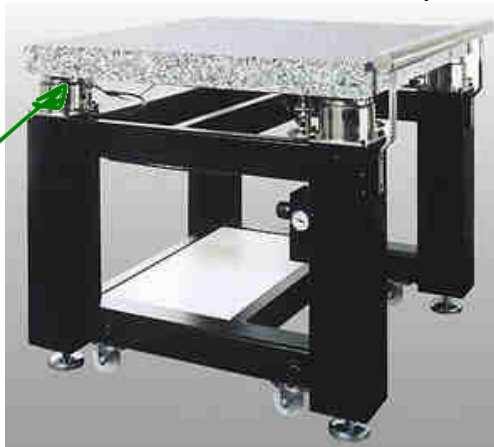


On-wafer test and sorting



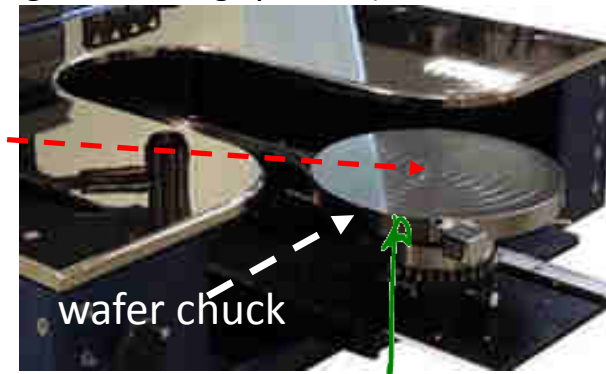
Vibration Isolation Table (Marble)

- keep high mechanical stability
- reliable sub-micron stability

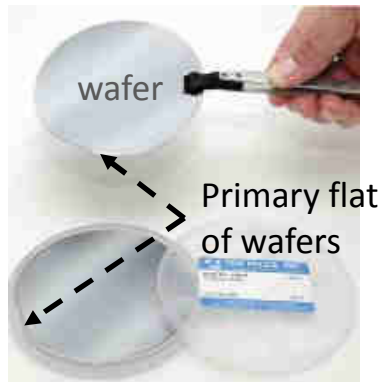


Wafer Chuck → Thermal chuck (-60°C → 300°C) Thermal enclosure

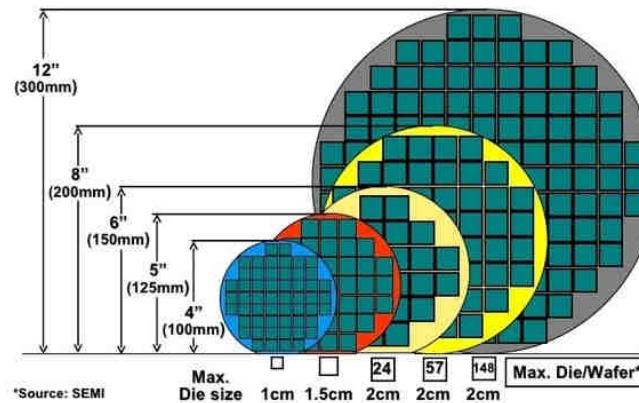
- hold wafers in place while they are being probed
- apply a small amount of vacuum to the wafer backside
- can hold small die and partial or whole wafer
- cooling and heating systems (air flow conditioning)



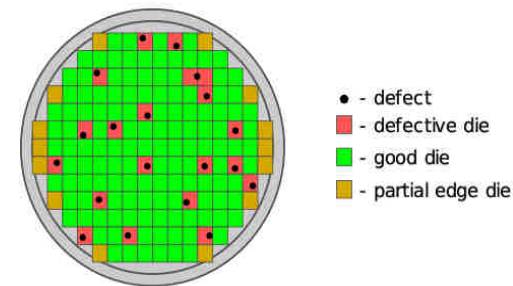
Wafer composition



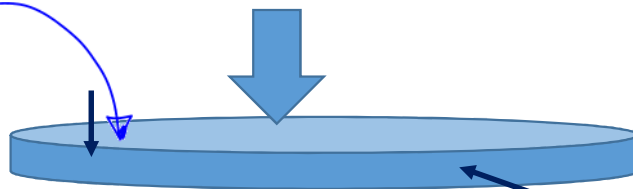
On-wafer size



On-wafer test and sorting



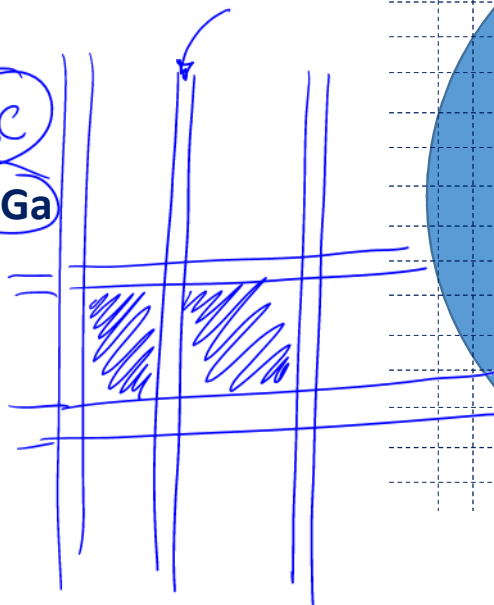
Front side of the wafer



H (Height of wafer)
Example 100-200µm

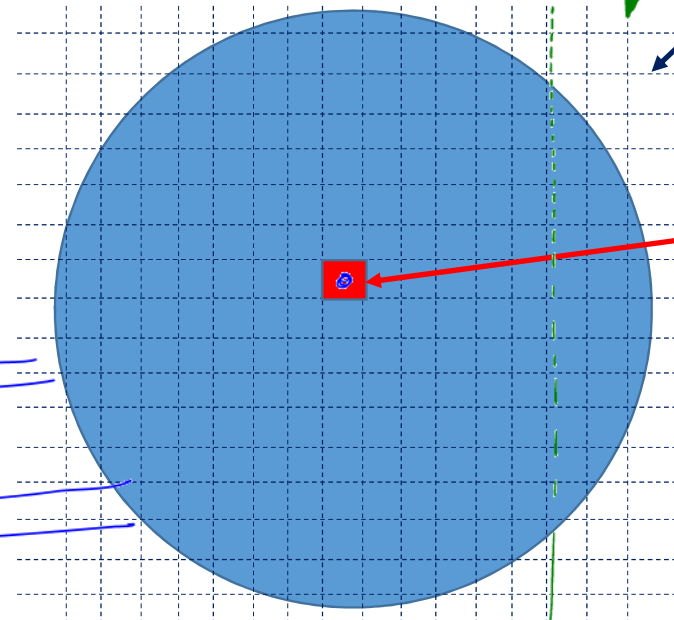
Backside of the wafer

SiC
AsGa
Si
...

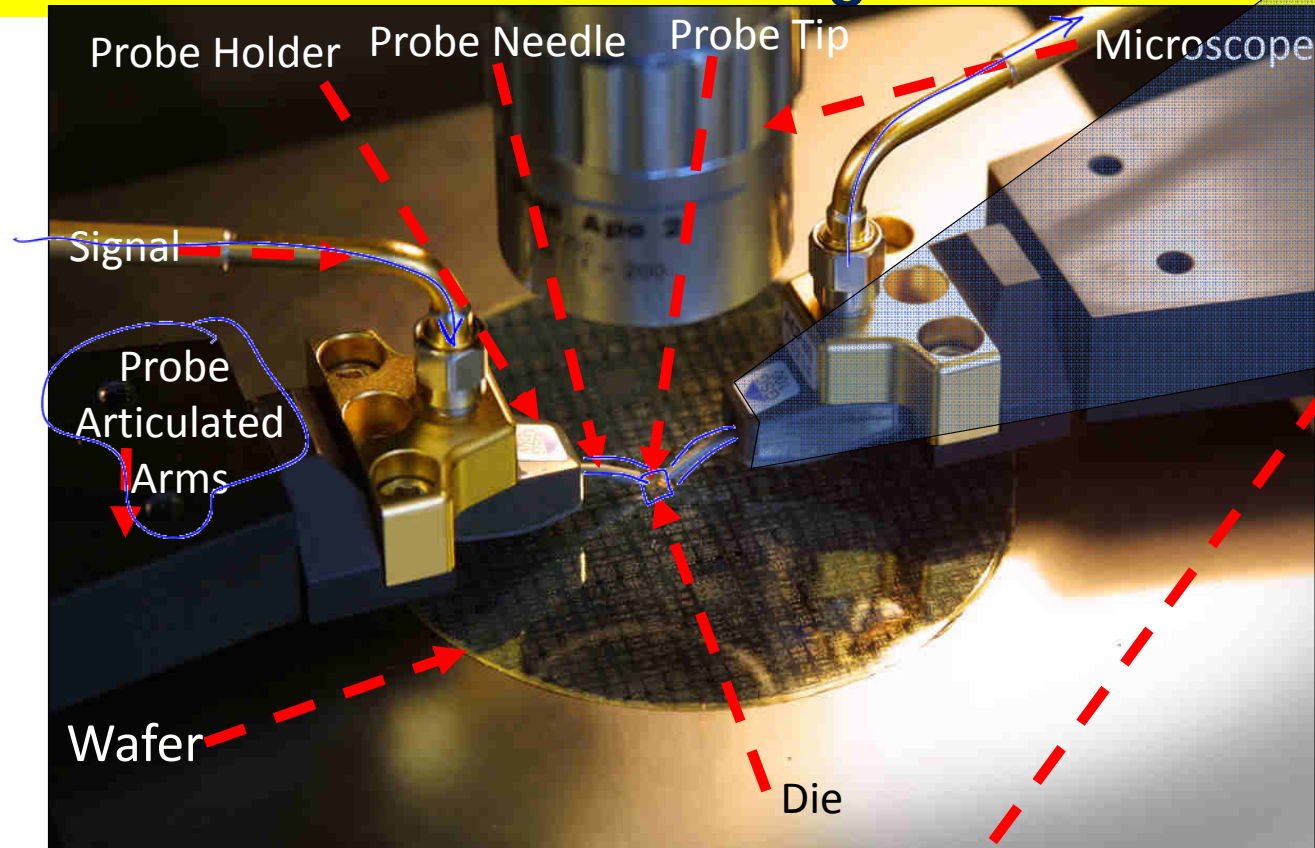


Dicing streets

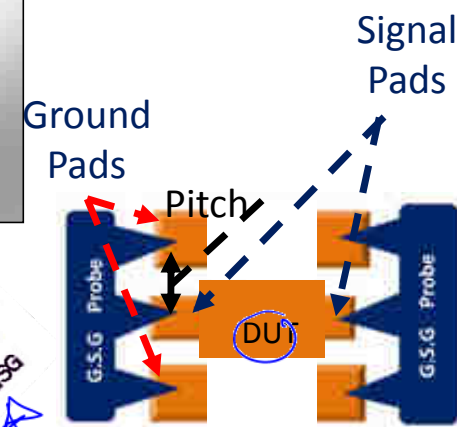
Chip (die)



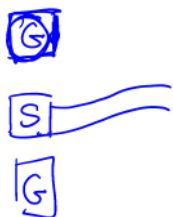
On-Wafer Probing



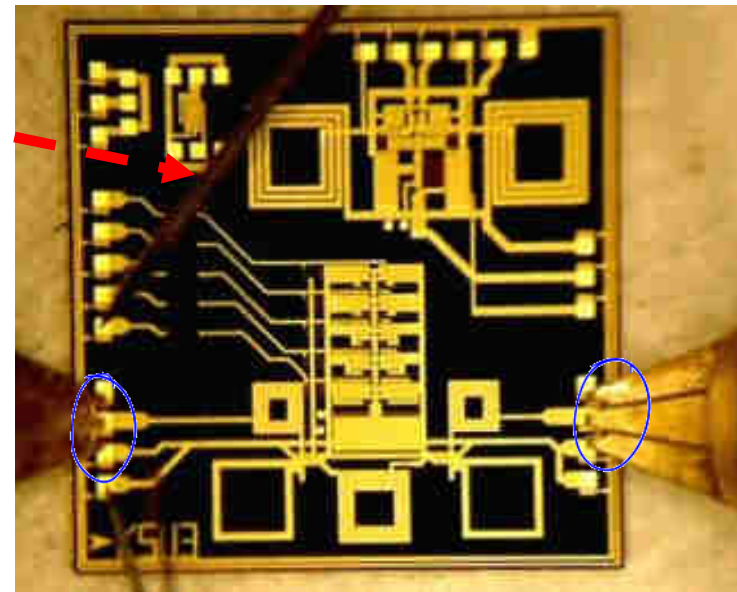
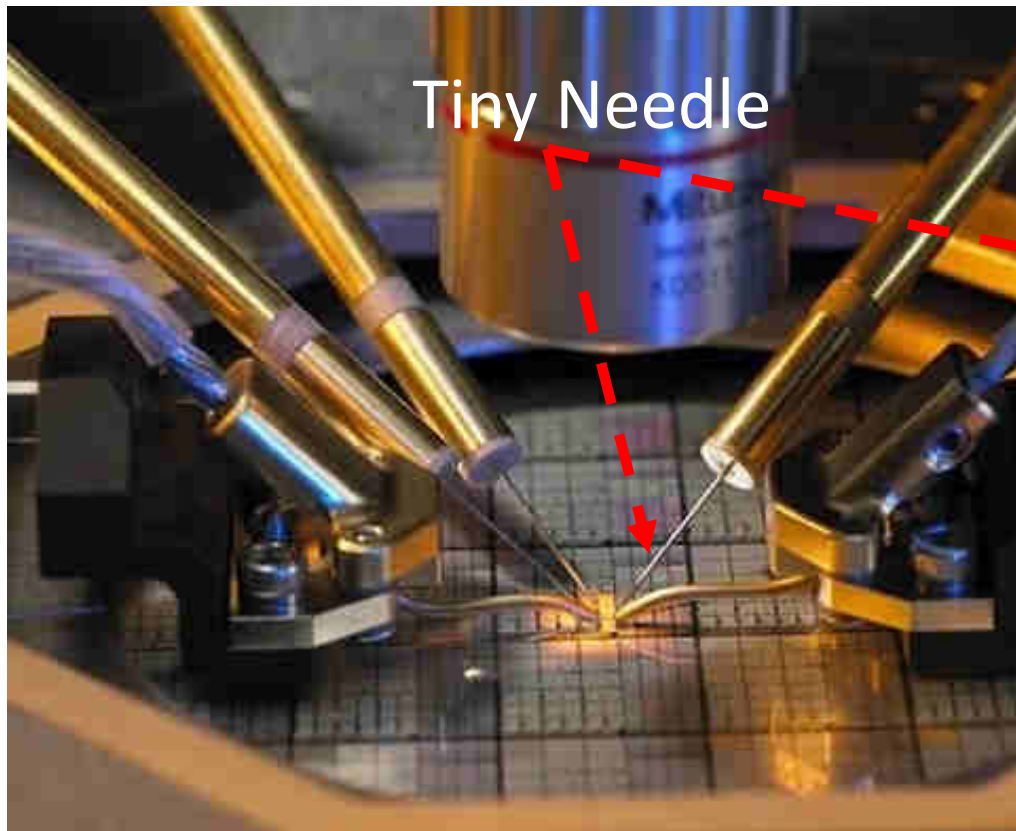
GSG is the most common type of RF probe. Many standard pitches



GSG probes



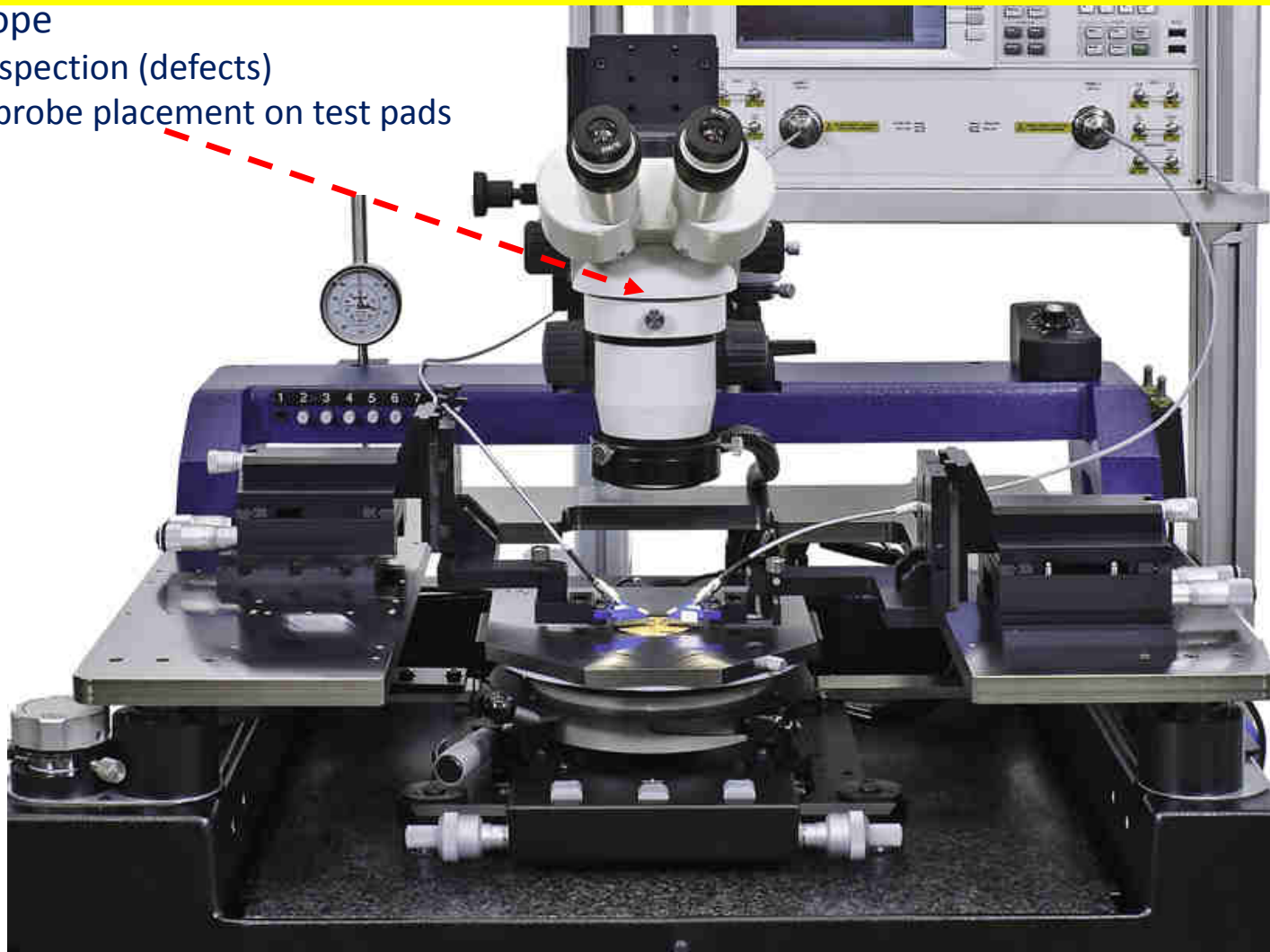
On-Wafer Probing



HF probe stations On-wafer Probing System

Microscope

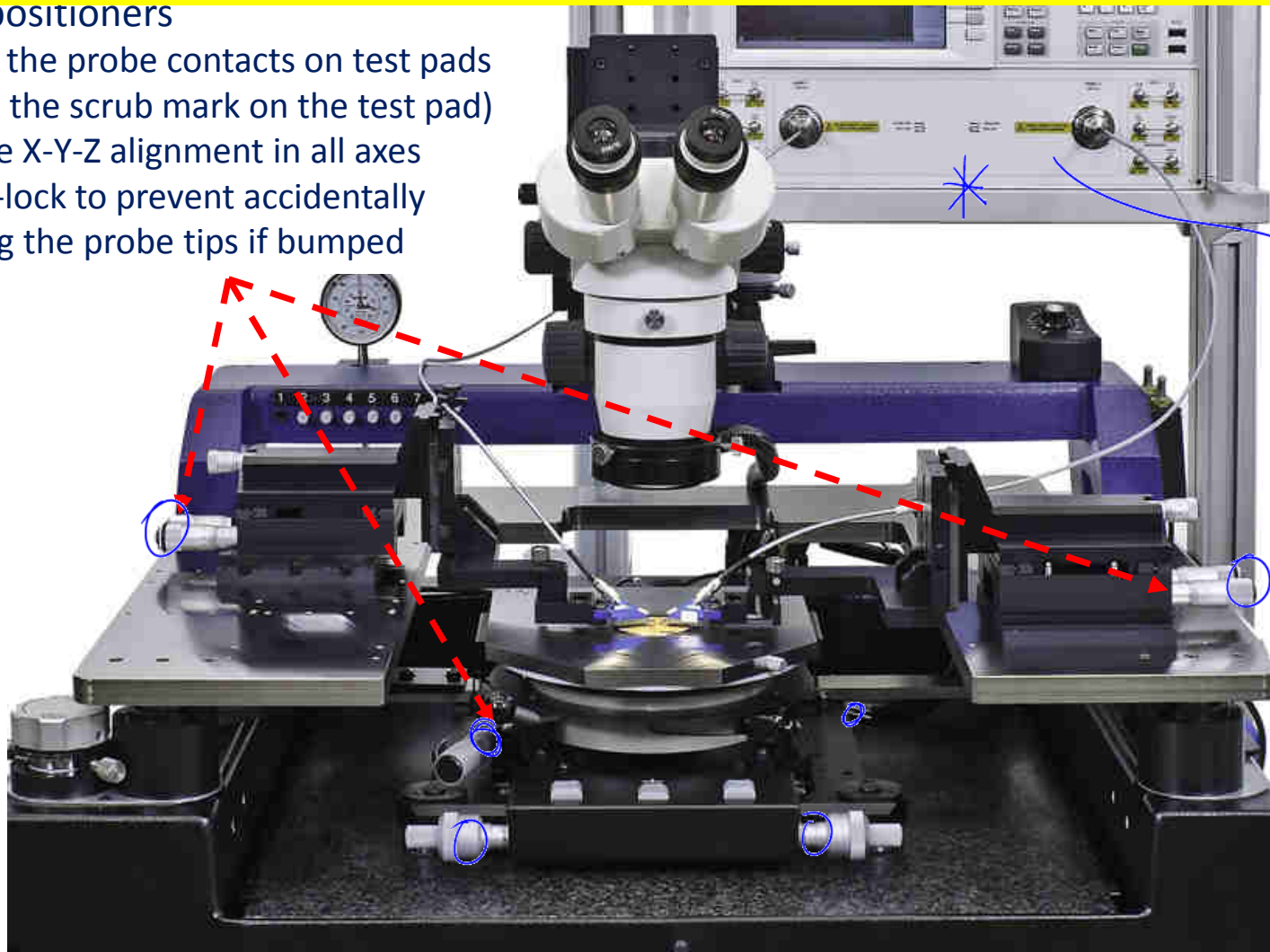
- wafer inspection (defects)
- precise probe placement on test pads



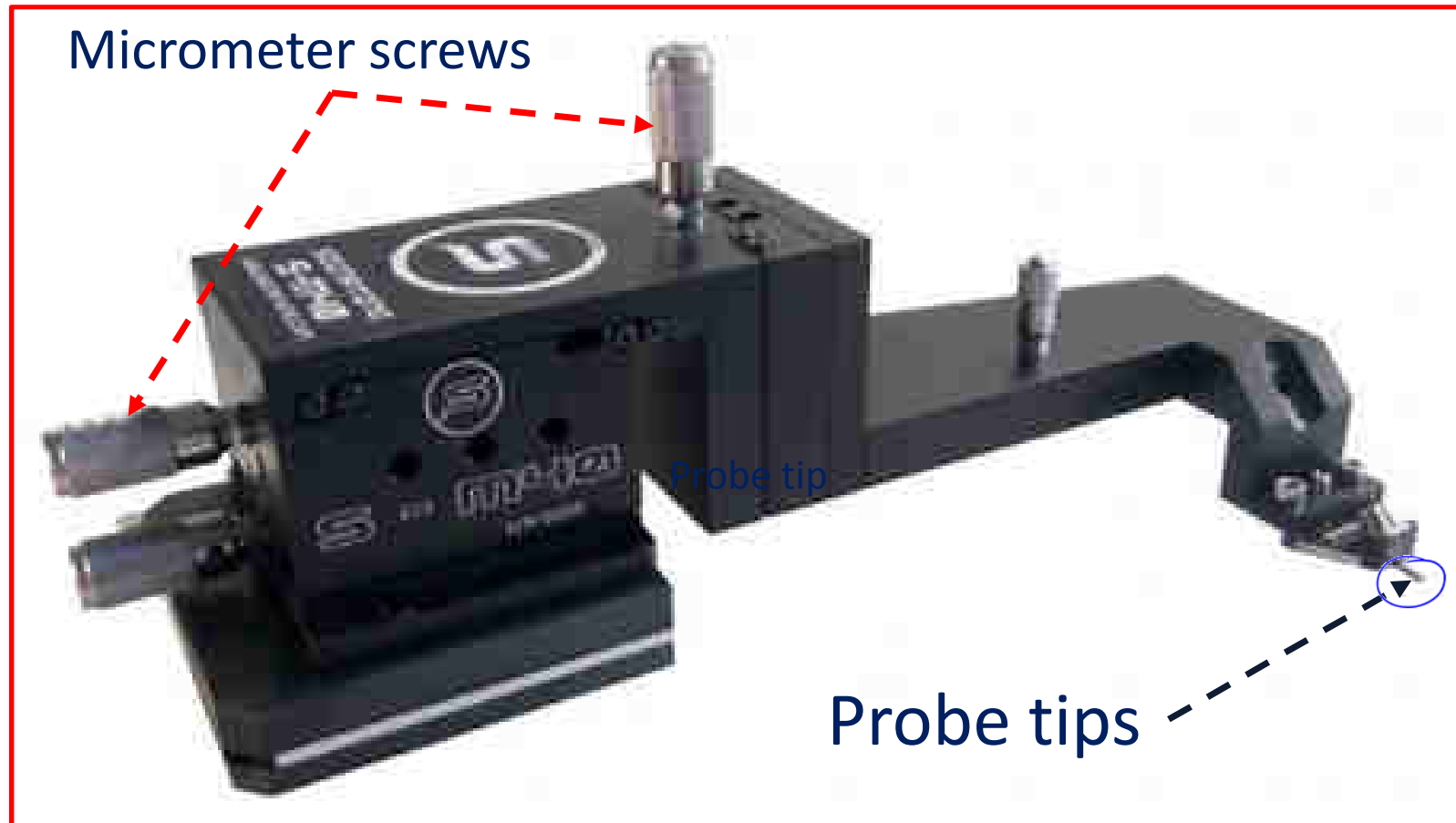
HF probe stations On-wafer Probing System

Micropositioners

- adjust the probe contacts on test pads (check the scrub mark on the test pad)
- precise X-Y-Z alignment in all axes
- screw-lock to prevent accidentally moving the probe tips if bumped



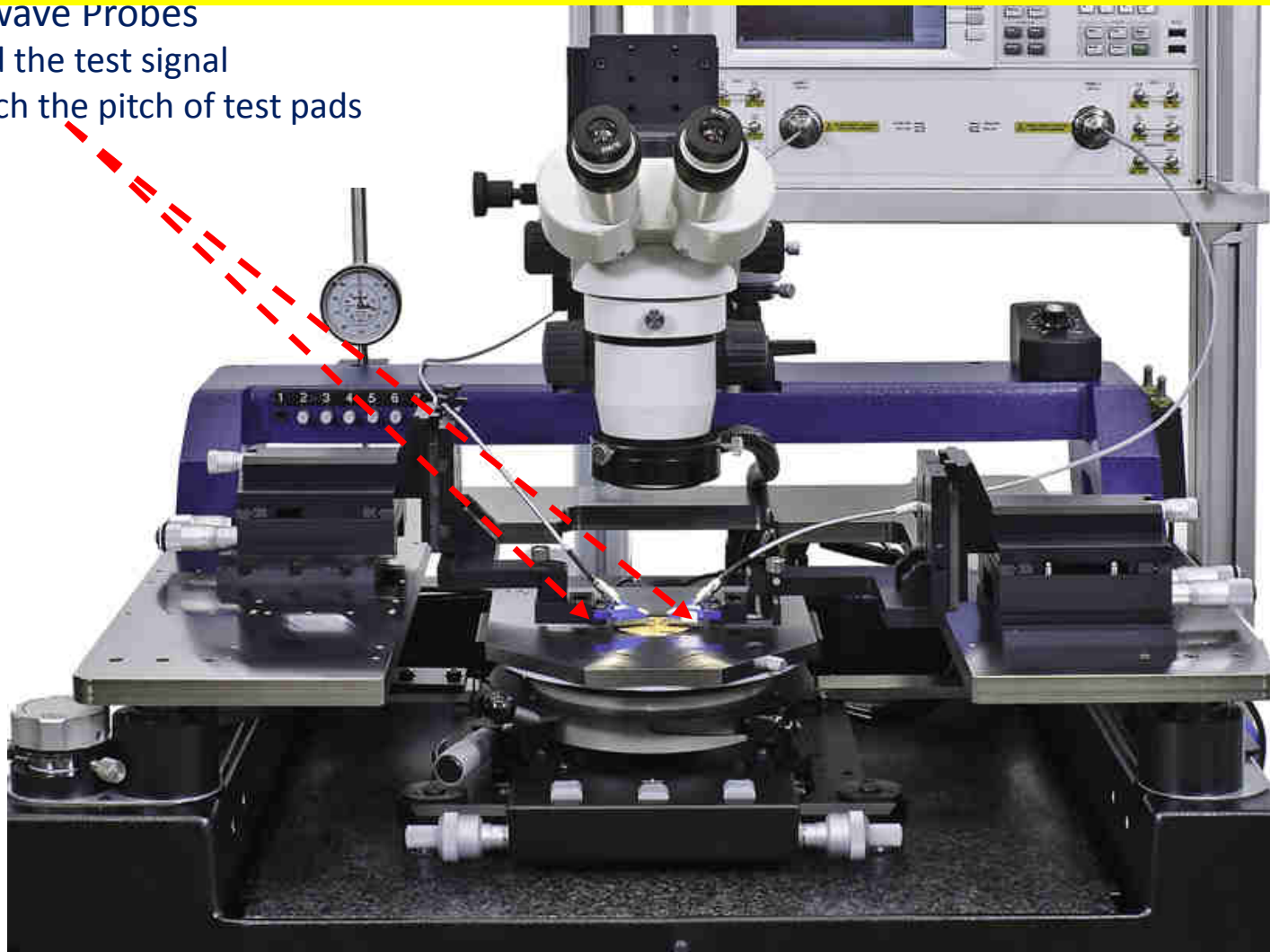
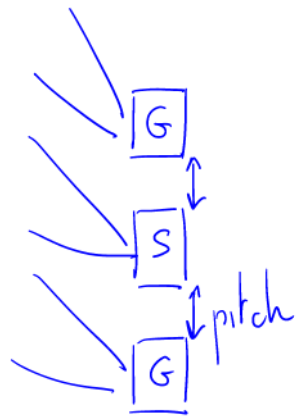
Micropositioner of probe tips



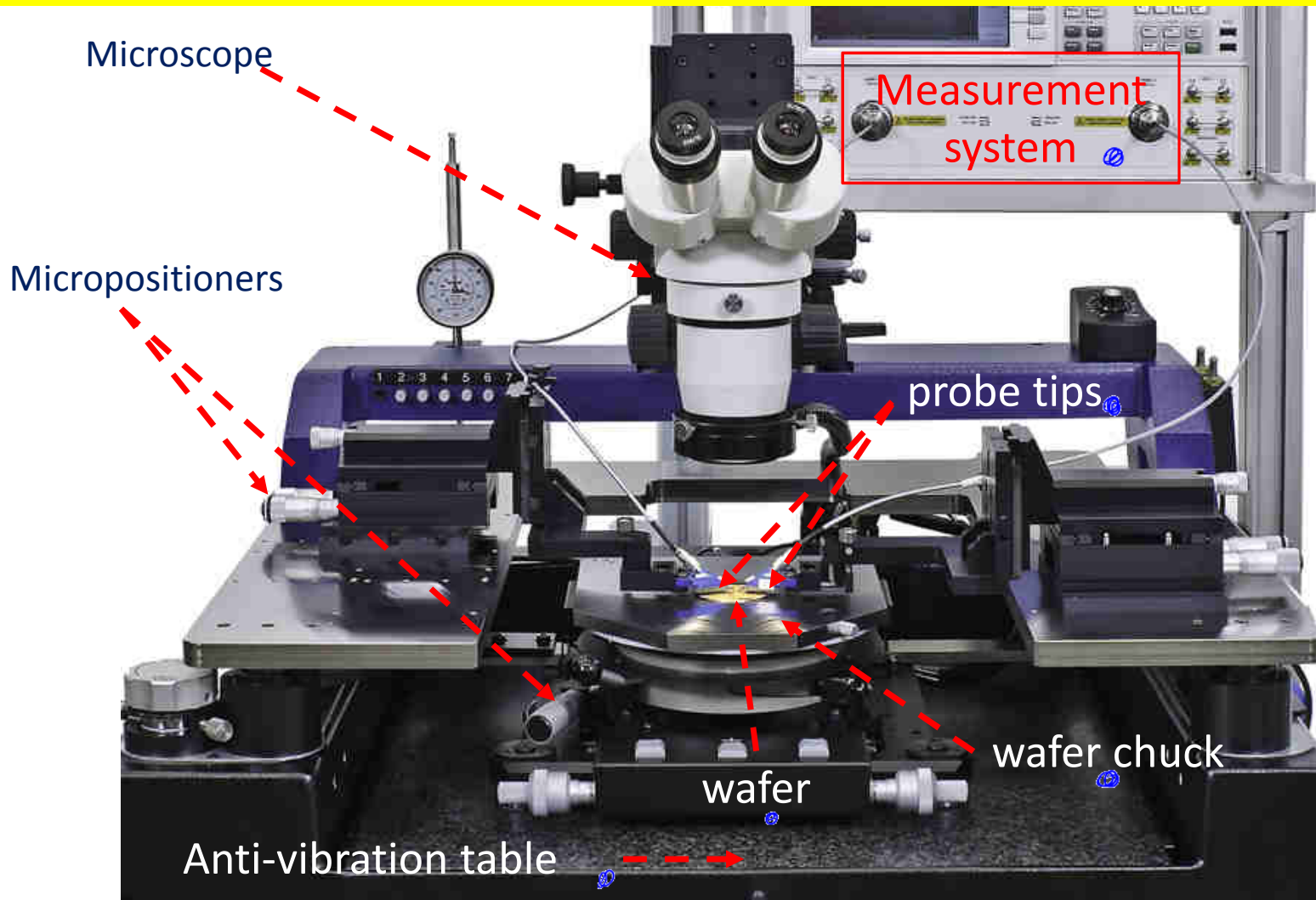
HF probe stations On-wafer Probing System

Microwave Probes

- Feed the test signal
- Match the pitch of test pads



HF probe stations On-wafer Probing System



I – Basics of MESFET operation

HEMT \Rightarrow Same model topology.

* Low-Frequency Bipolar transistors are based on the well-known PN Junction (P-type-SC / N-type-SC)

* High-Frequency MESFET (MEtal Semiconductor Field Effect Transistor) based on Schottky Junction (Metal / N-type-SC)

\downarrow HEMT

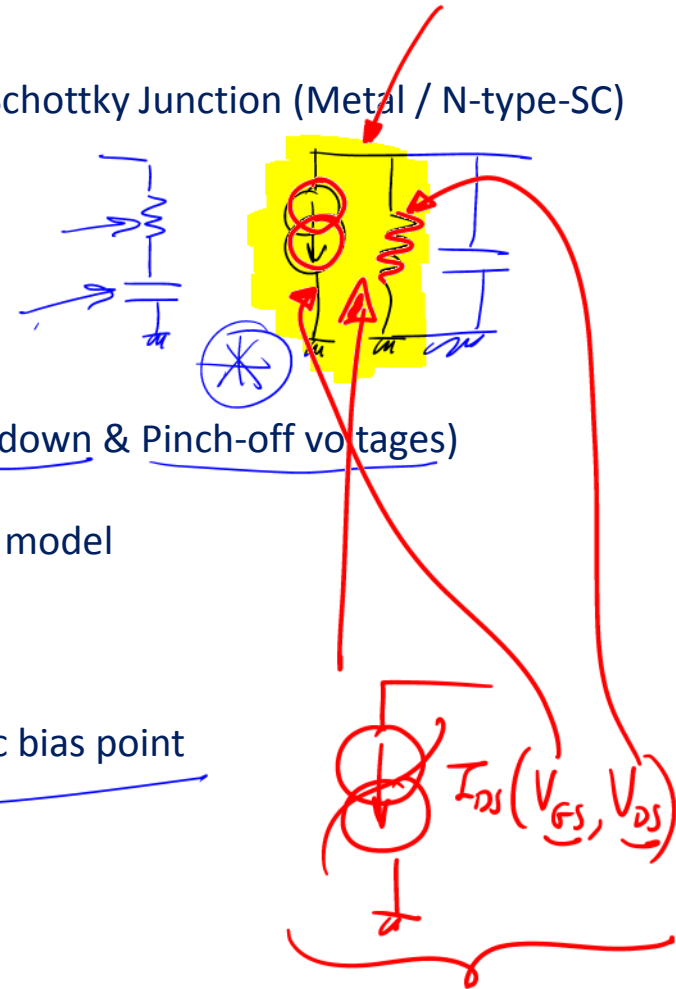
• \rightarrow Simplified planar representation of FETs

• \rightarrow I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)

\rightarrow Localization of electrical equivalent elements that gives the nonlinear electrical model

\rightarrow Successive simplification to derive the simplified linear electrical FET model *

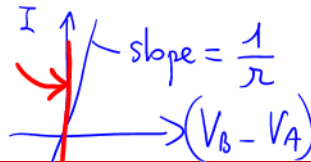
\rightarrow Small-signal equivalent of the nonlinear drain current (g_m , g_d) around a specific bias point



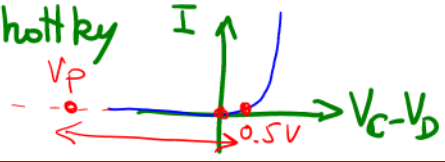
ohmic contact



Wire
($\rho=0$)



Schottky



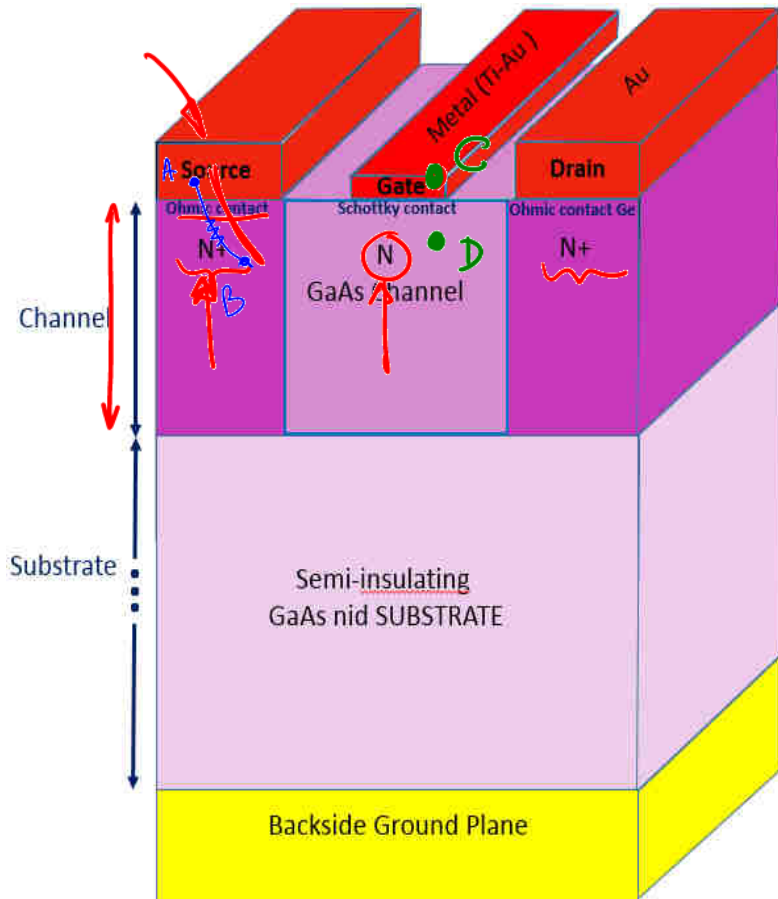
EMIMEO

E(rasmus) Mundus on Innovative Microwave Electronics and Optics

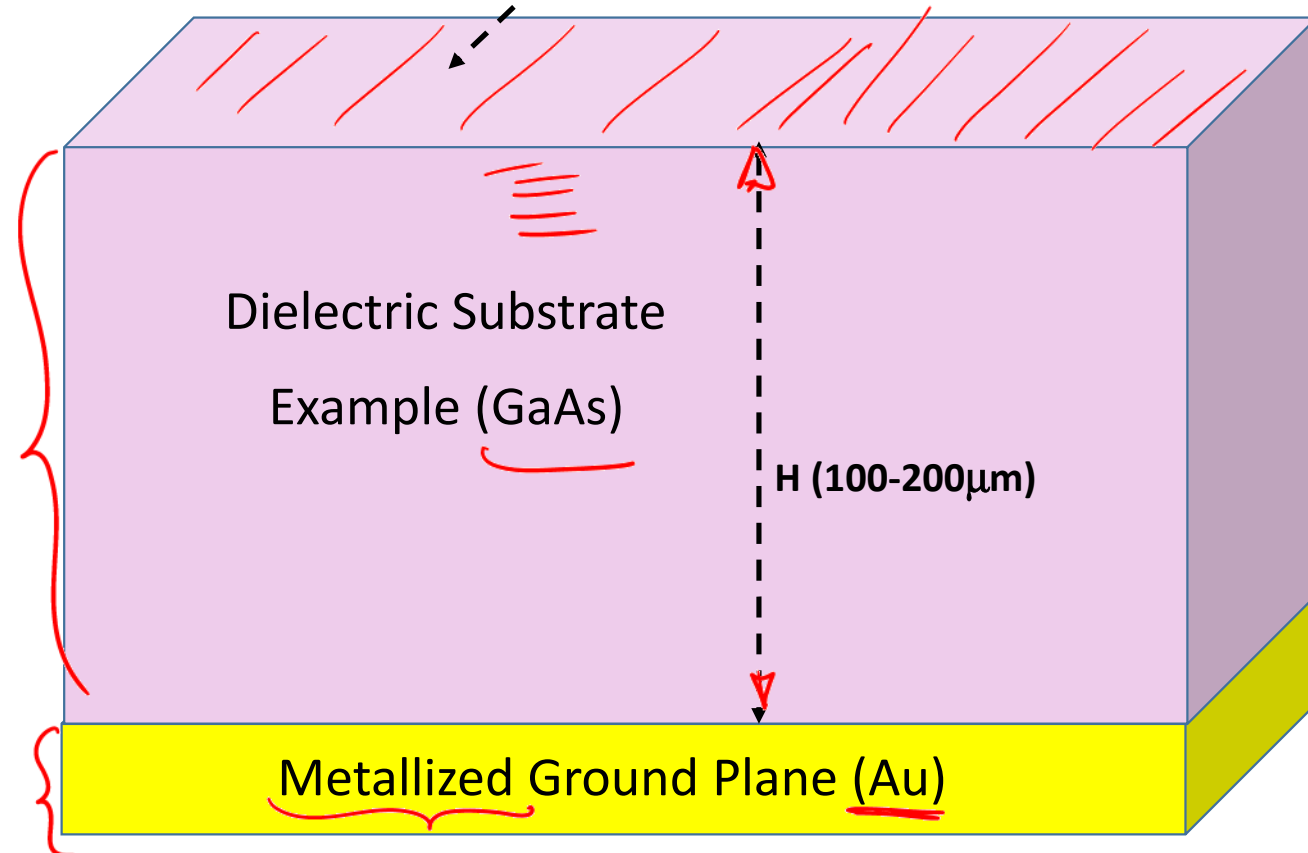


I – Basics of MESFET operation


→ Simplified planar representation of FETs (Depletion Mode)





Front Side of the wafer
where active and passive elements
are placed



Operating principles (FET / HEMT)

 **FET** → Gate voltage controls the flow of drain current by modifying the available section W of the doped channel (Impurities, Ionized scattering → Low mobility)

Schottky Junction (Metal/ SC_N) in reverse mode I_{DS}


 **HEMT** → Gate voltage controls the flow of drain Current by modifying the carrier density n_s of a 2DEG in the undoped channel (no impurities → Very high mobility)

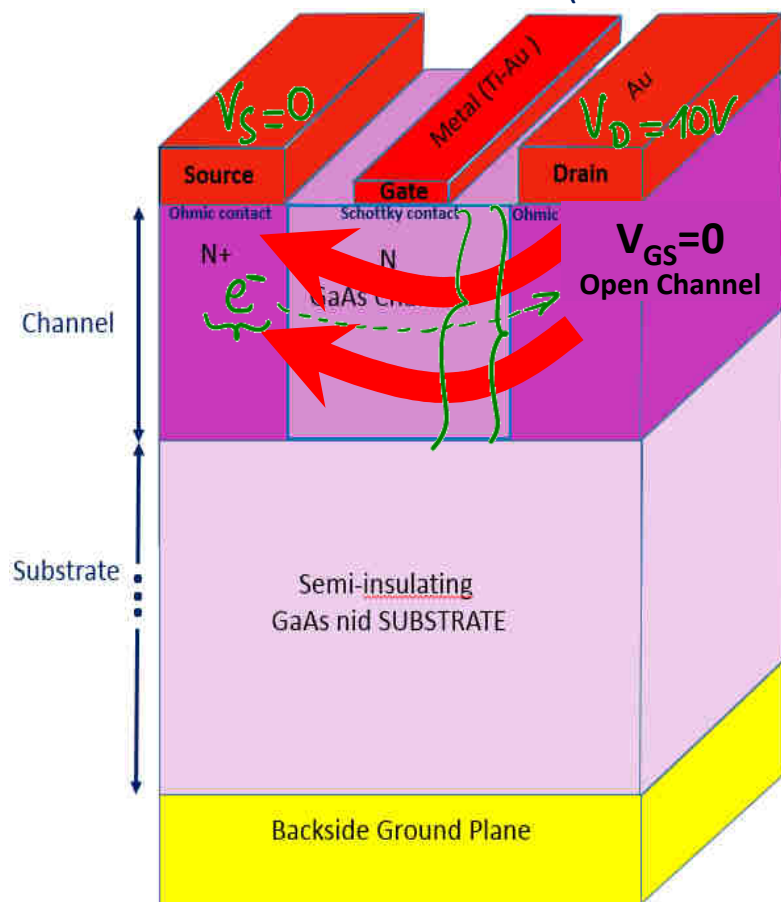
The (two-dimensional Electron Gas) **2DEG** is located at the **heterojunction** between a **wide bandgap semi-conductor (AlGa_N)** and a **narrow bandgap semi-conductor (Ga_N)**.

The electrons of the 2 DEG are free to move in a two-dimensional plane (x, z) but tightly confined in the 3rd dimension (y) because they are trapped in a potential well created at the heterojunction surface

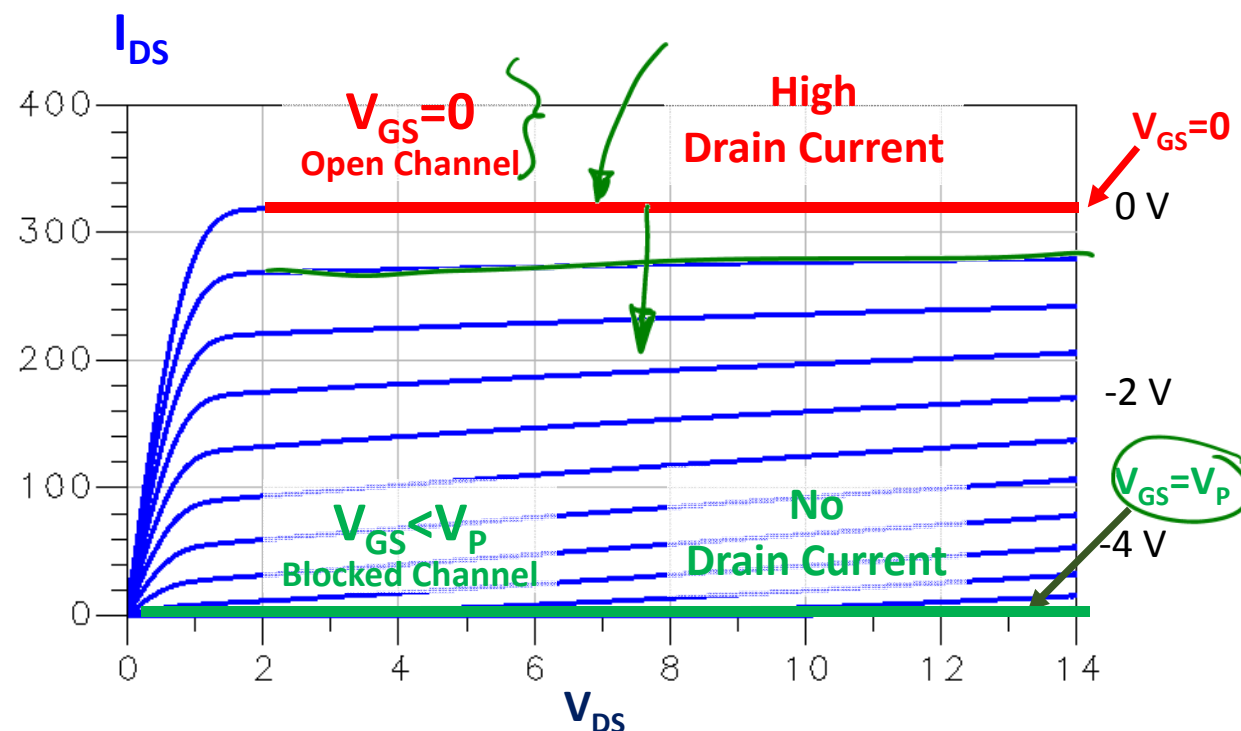
heterostructure (Wide bandgap SC / Narrow bandgap SC) 

I – Basics of MESFET operation


→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)




FET → Gate voltage controls the flow of drain current by modifying the available section W of the doped channel (Impurities, Ionized scattering → Low mobility)



Operating principles (FET / HEMT)

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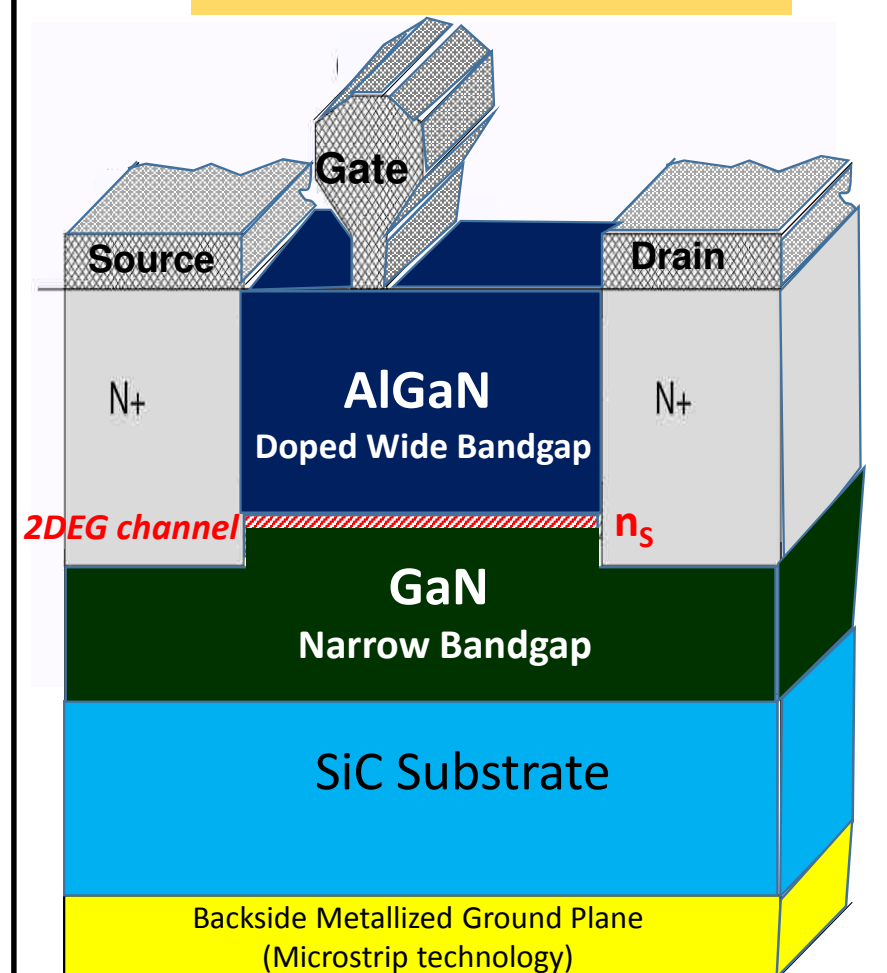
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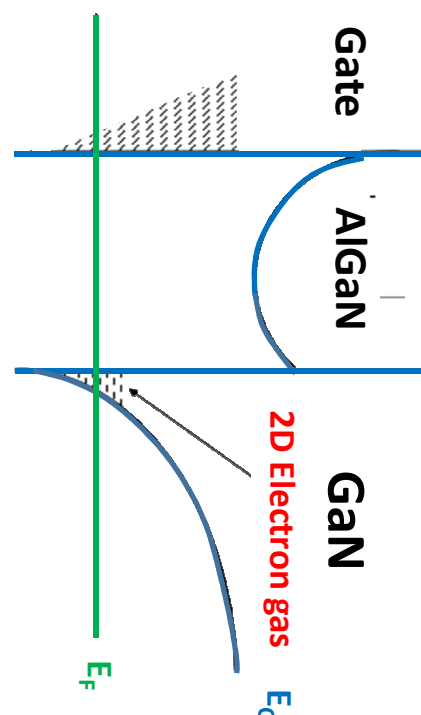
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because they are trapped in a potential well created at the heterojunction surface

I – Basics of HEMT operation → Same Electrical Circuit Model than FET

AlGaIn/GaN HEMT on SiC



HEMT → Gate voltage controls the flow of drain current by modifying the carrier density n_s of a 2DEG in the undoped channel (no impurities → Very high mobility)

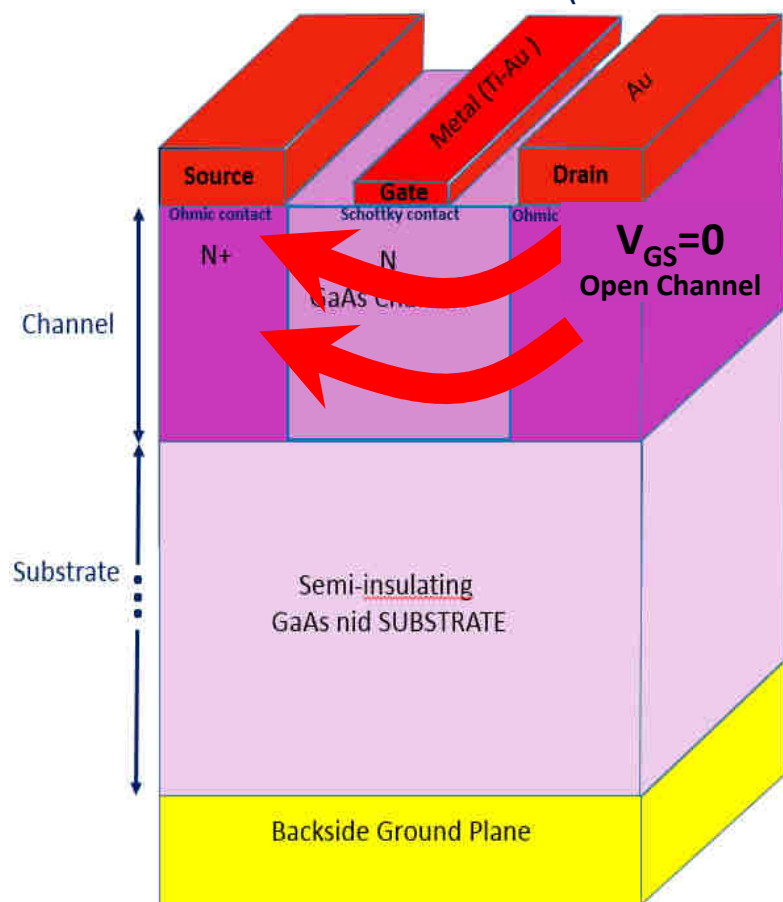


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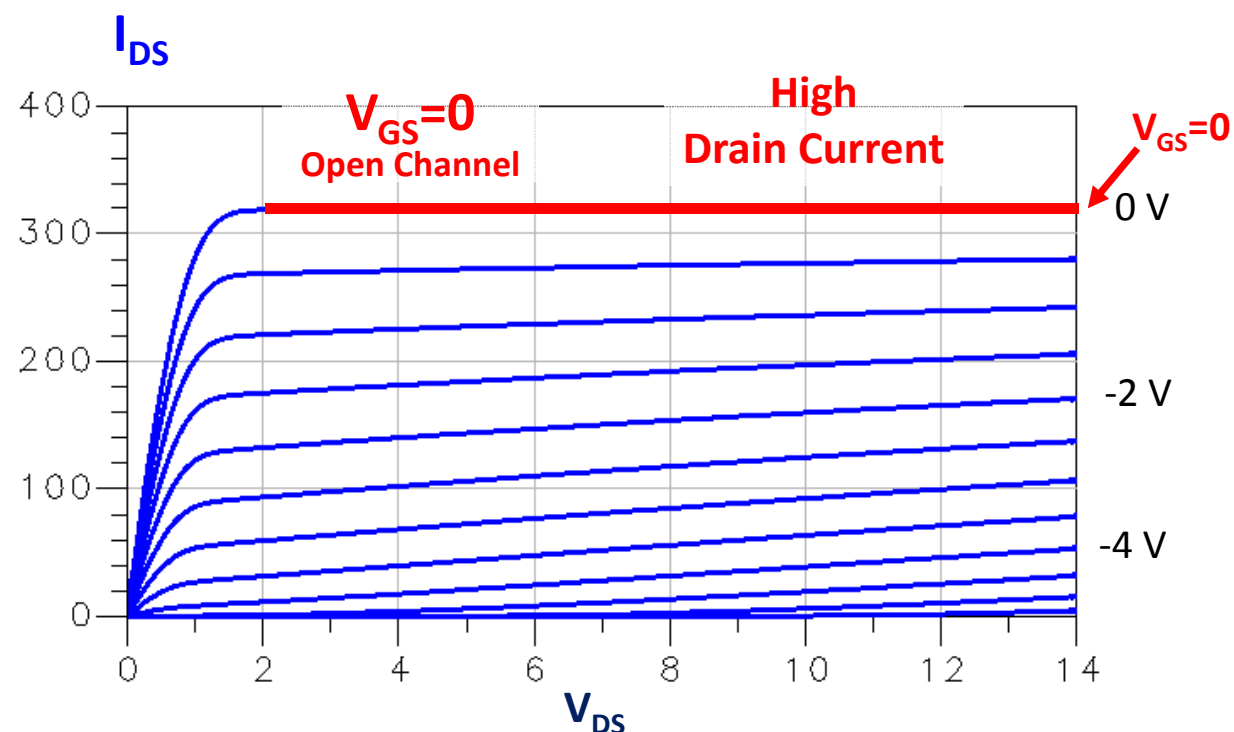
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I – Basics of MESFET operation

→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)

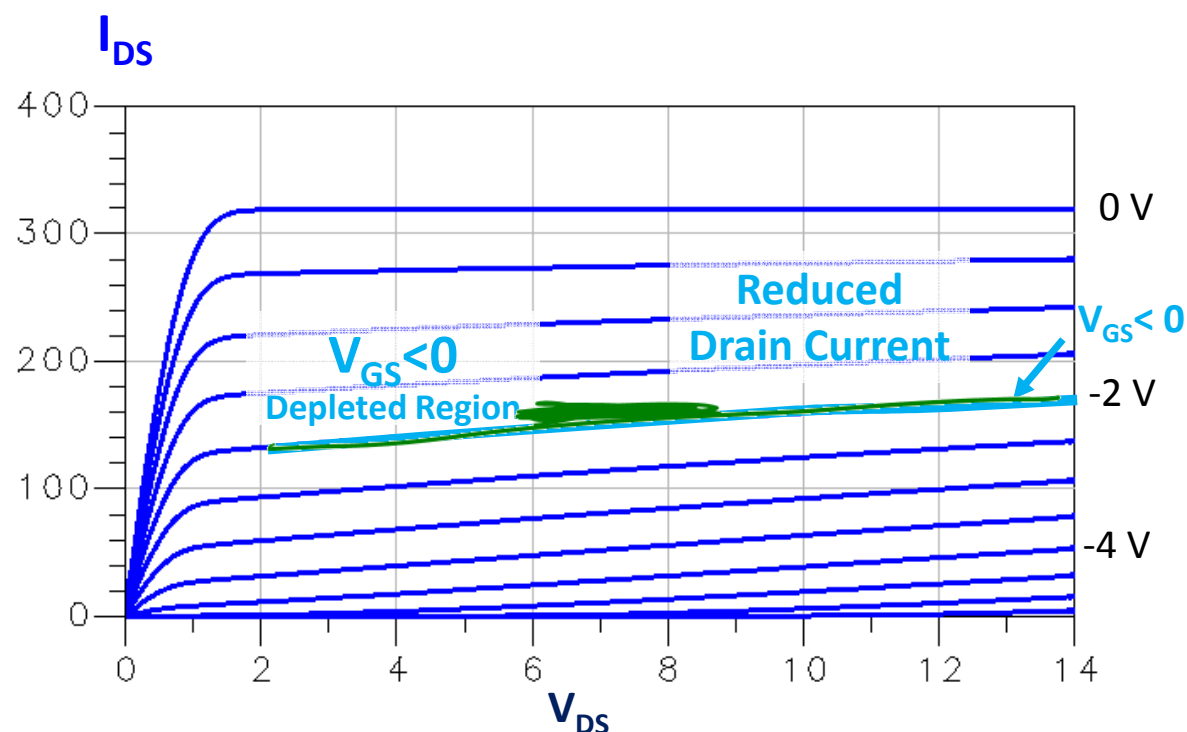
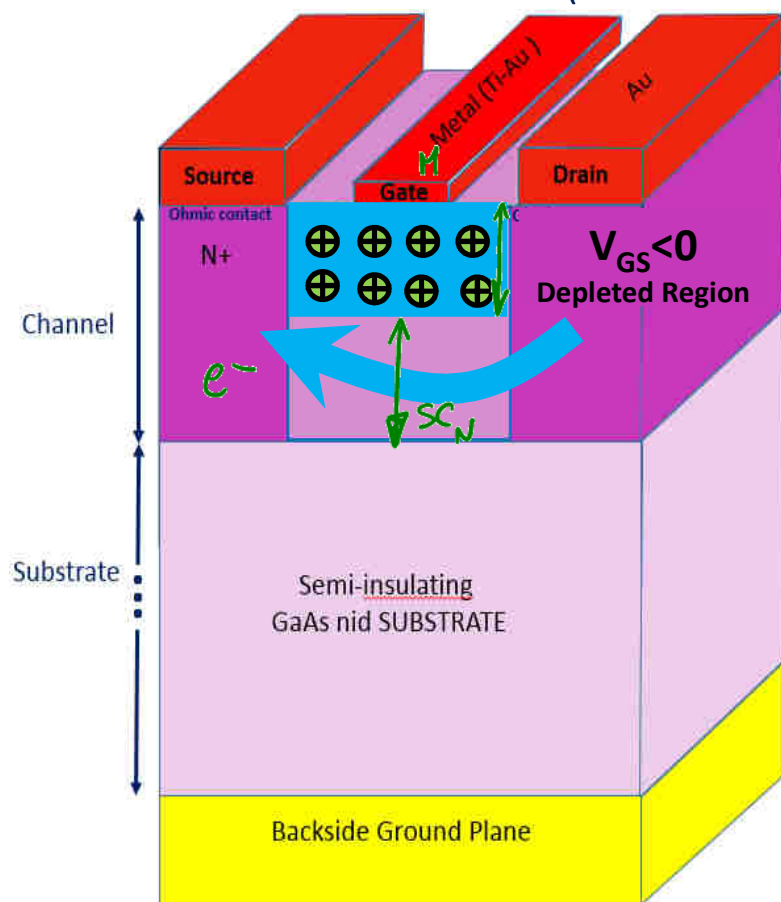


FET → Gate voltage controls the flow of drain current by modifying the available section W of the doped channel (Impurities, Ionized scattering → Low mobility)



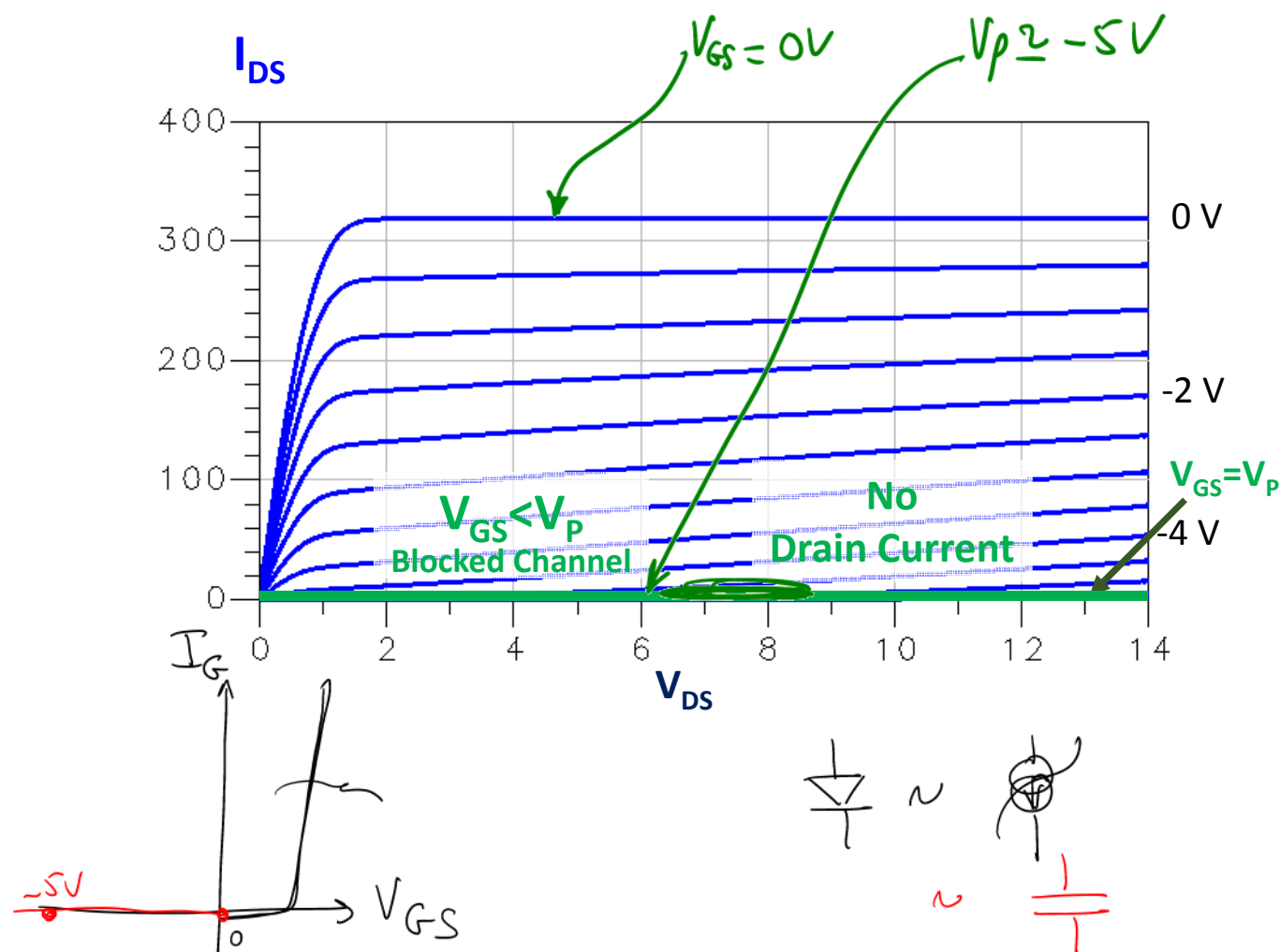
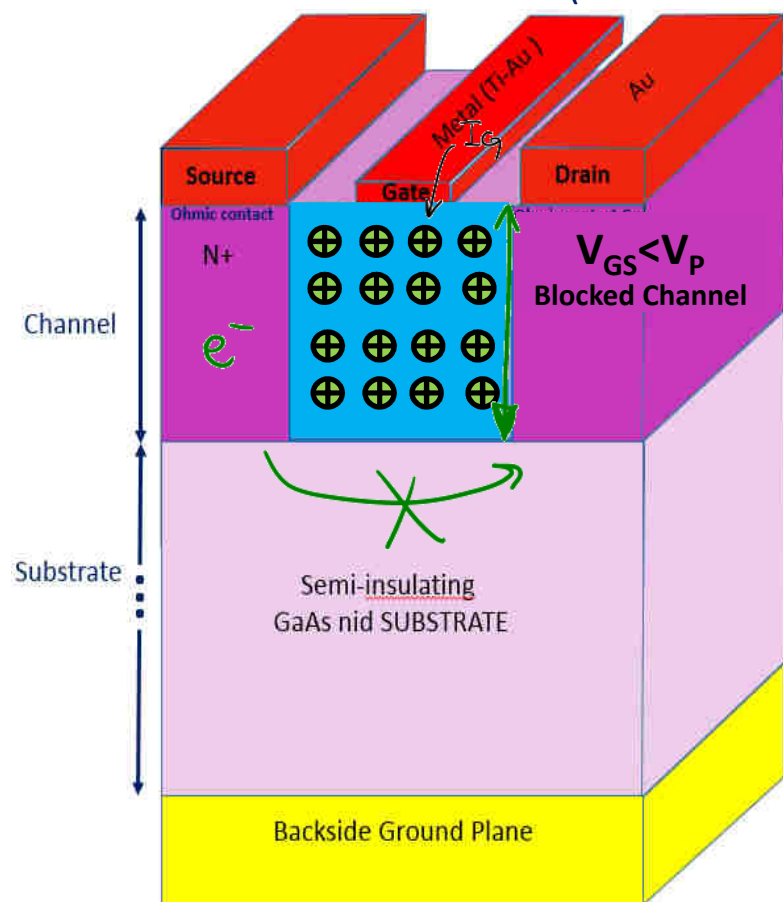
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→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)



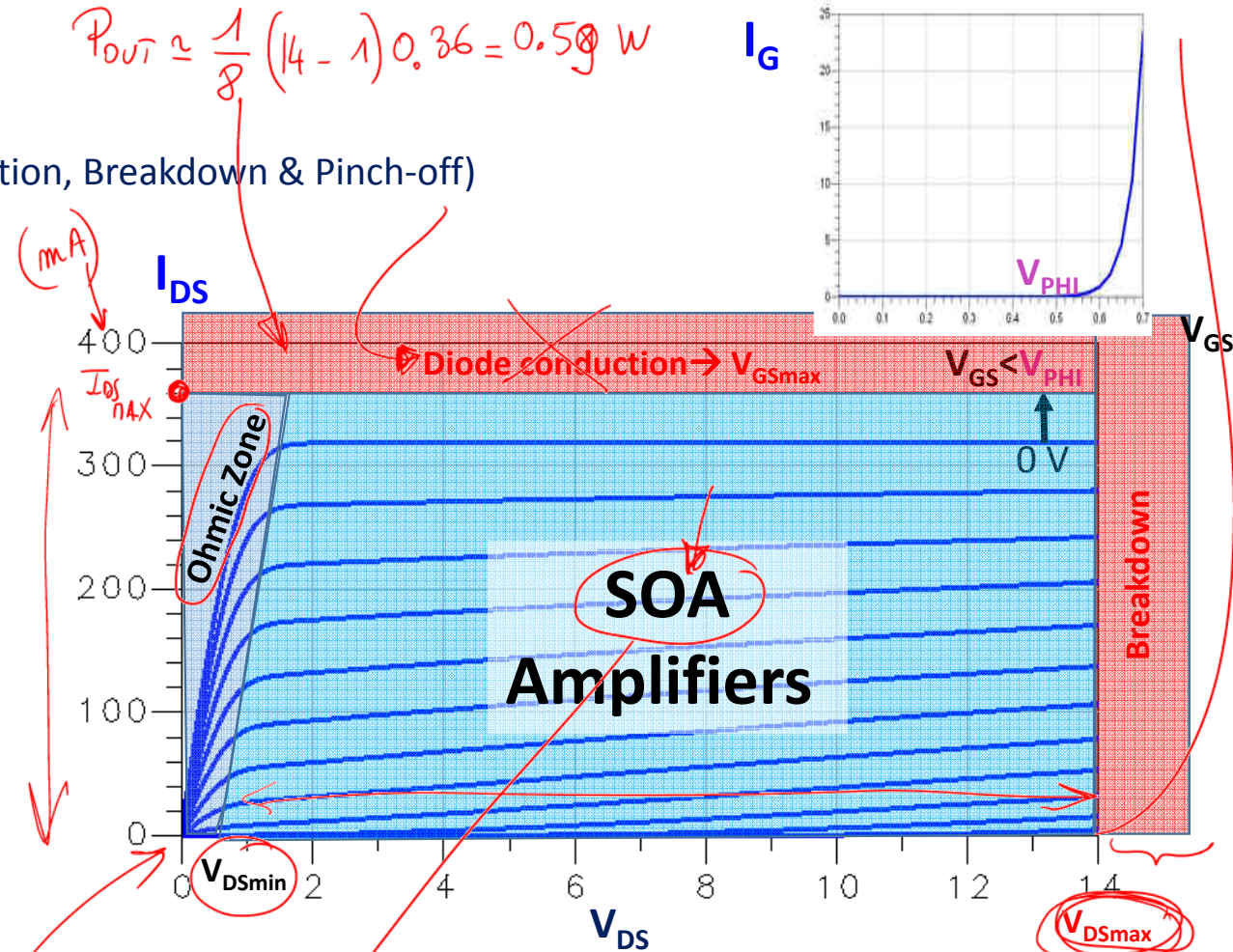
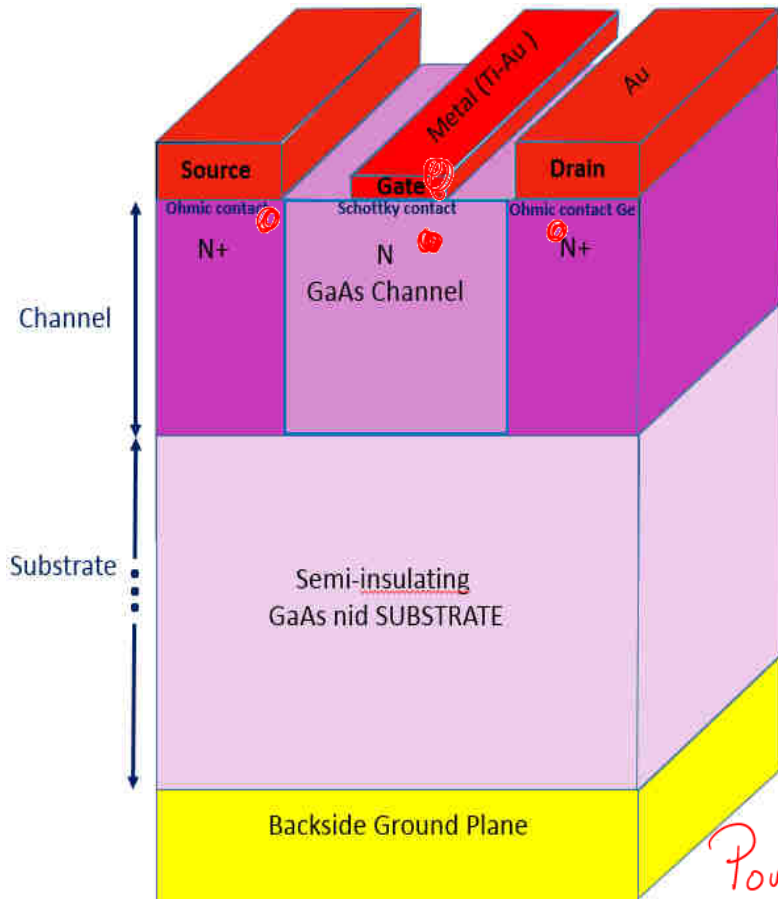
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→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)



I – Basics of MESFET operation

→ I-V regions (Ohmic, Saturated, Diode conduction, Breakdown & Pinch-off)



Handwritten formula for $P_{out max}$:

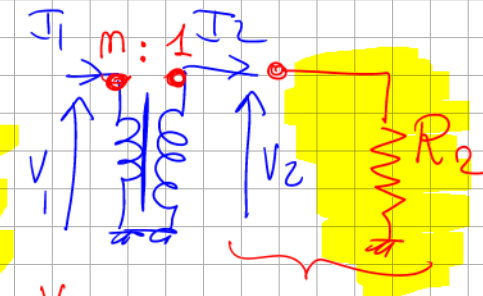
$$P_{out max} \approx \frac{1}{2} \times \frac{V_{DSmax} - V_{DSmin}}{2} \times \frac{I_{DSmax}}{2}$$

Safe Operating Area

FET → $V_{DSmax} \approx 20 \text{ V}$
 HEMT → $V_{DSmax} \approx 100 \text{ V}$

IMC
Input Matching Circuit

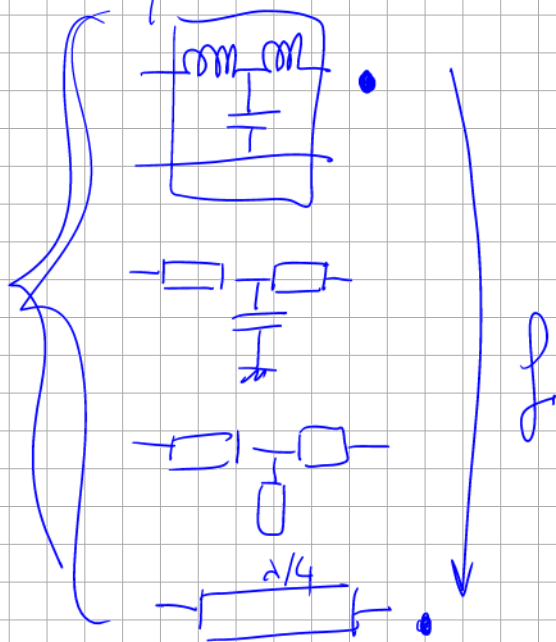
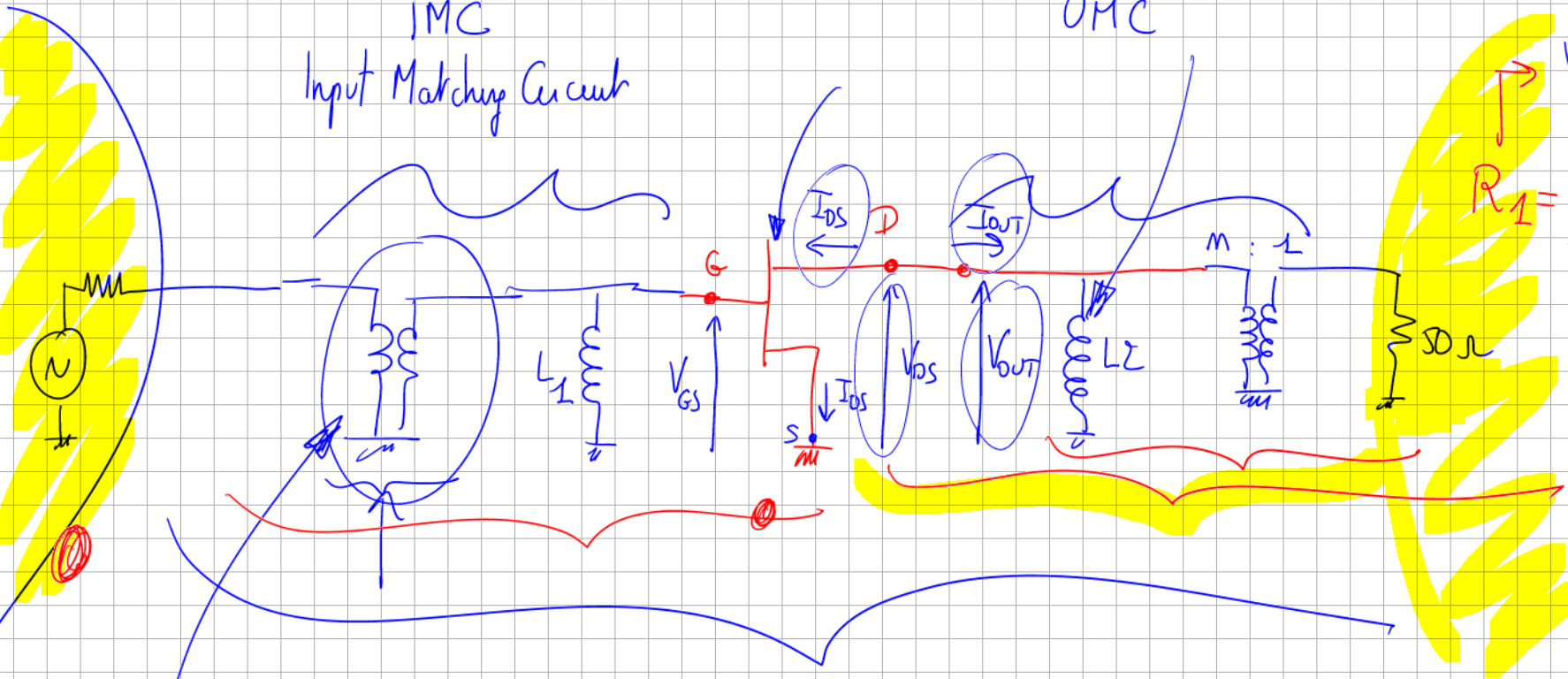
OMC



$$R_1 = \frac{V_1}{I_1}$$

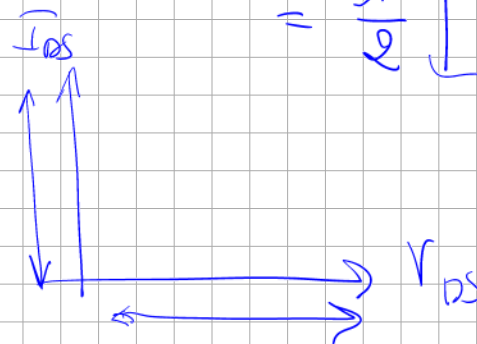
$$m = \frac{m_2}{m_1}$$

$$m = \sqrt{\frac{R_2}{R_1}}$$

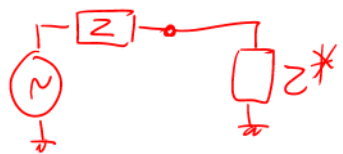


$$P_{out} = \frac{1}{2} \operatorname{Re} (V_{out} \times I_{out}^*)$$

$$= \frac{1}{2} |V_{out}| |I_{out}| \cos(\phi_{V_{out}} - \phi_{I_{out}})$$



①

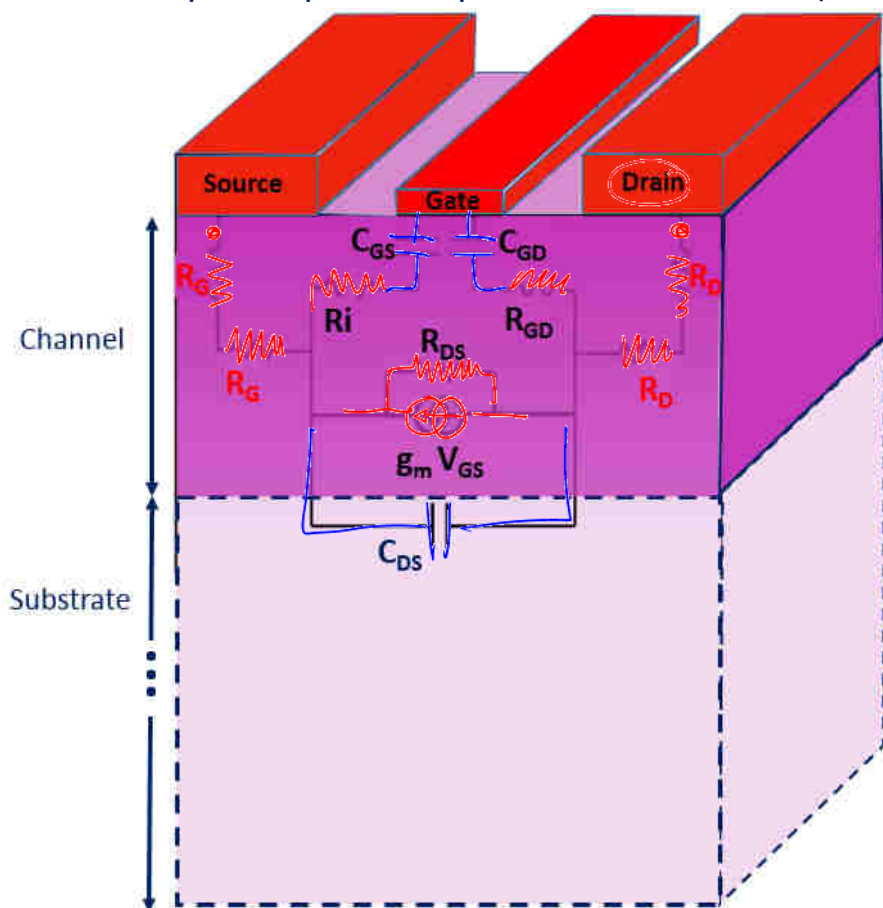


$R_E \gg R$ voltage matching



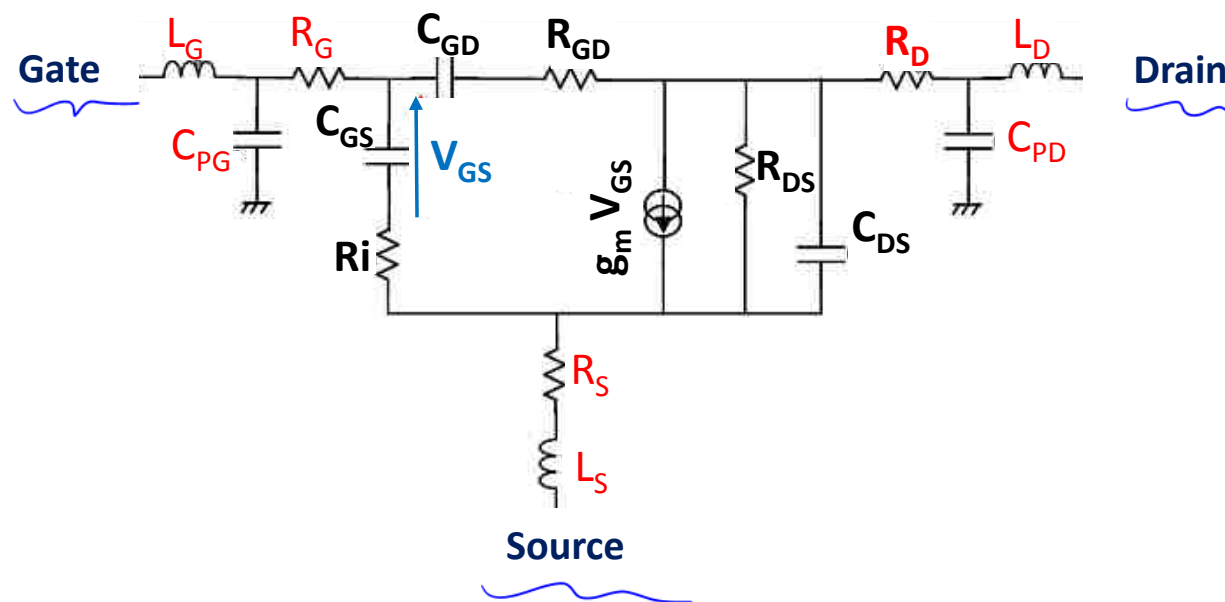
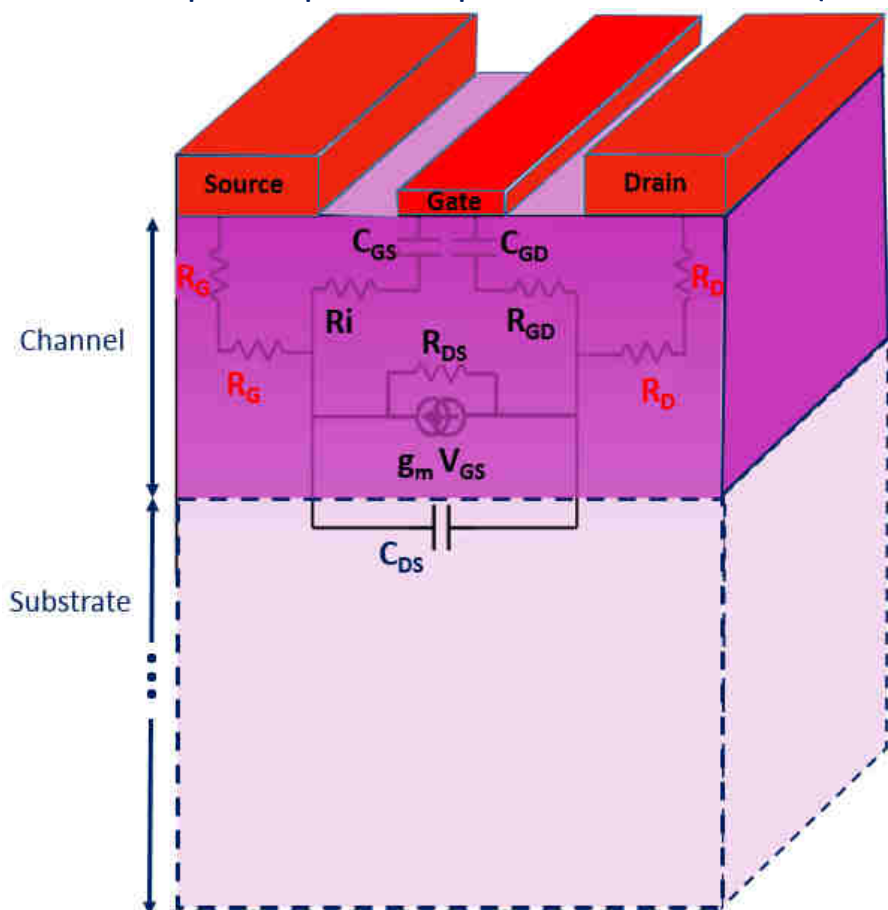
I – Basics of MESFET operation

→ Simplified planar representation of FETs (localization of electrical lumped elements)



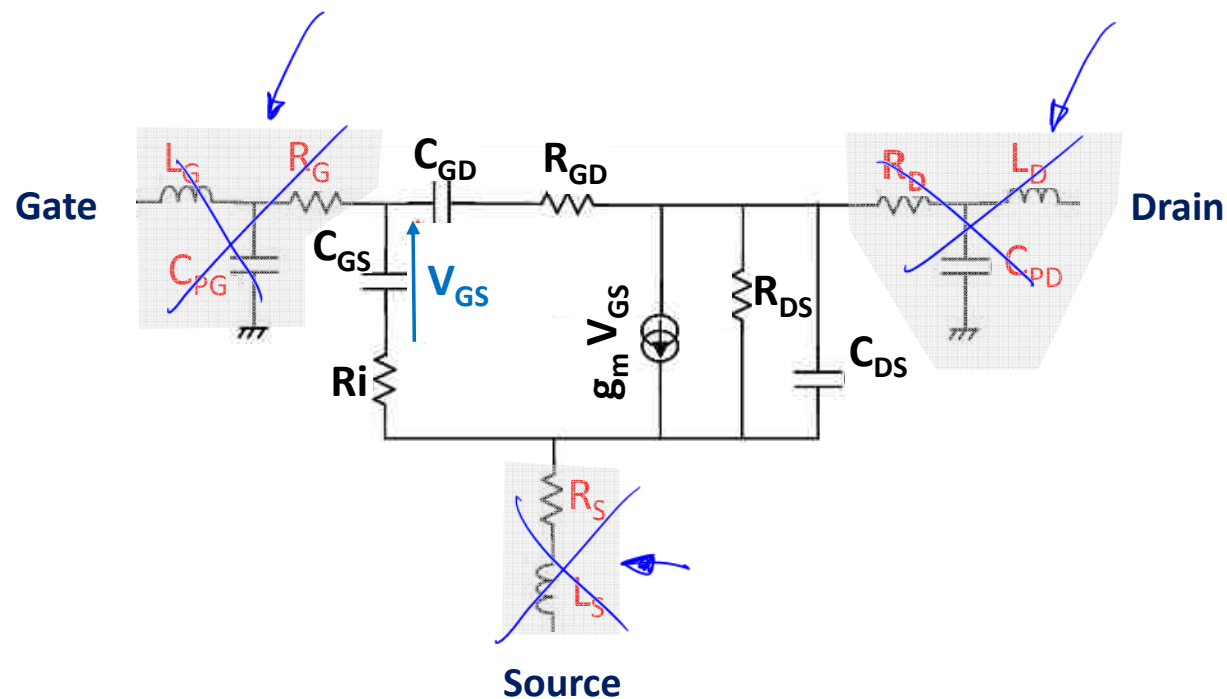
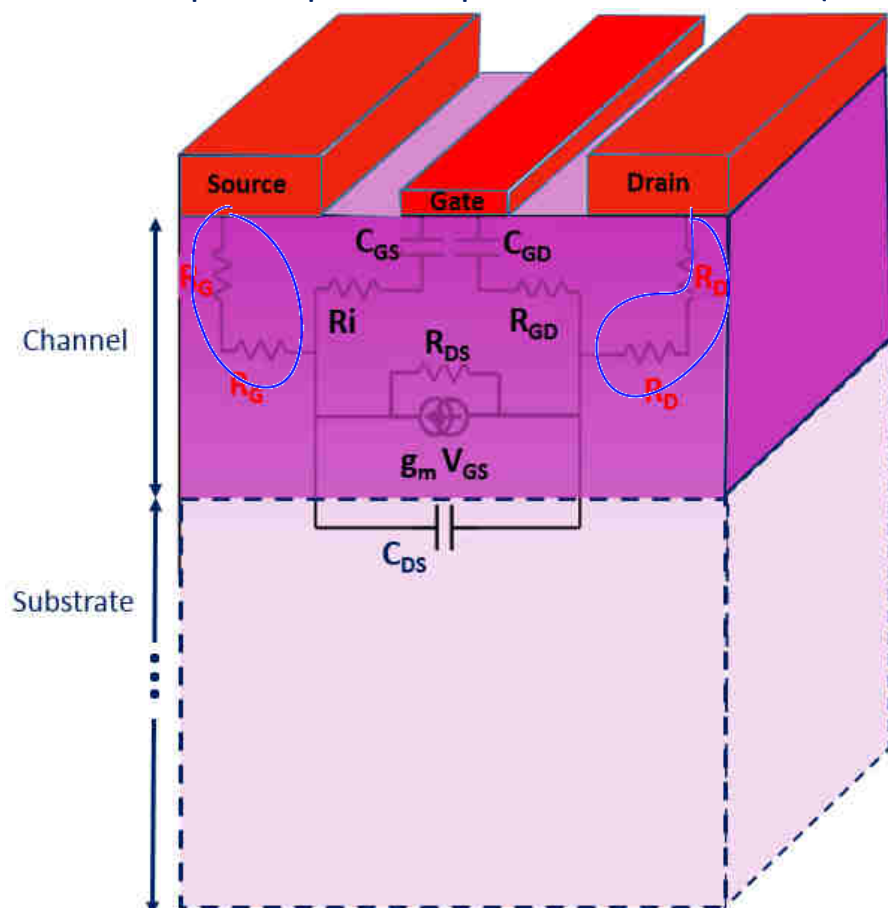
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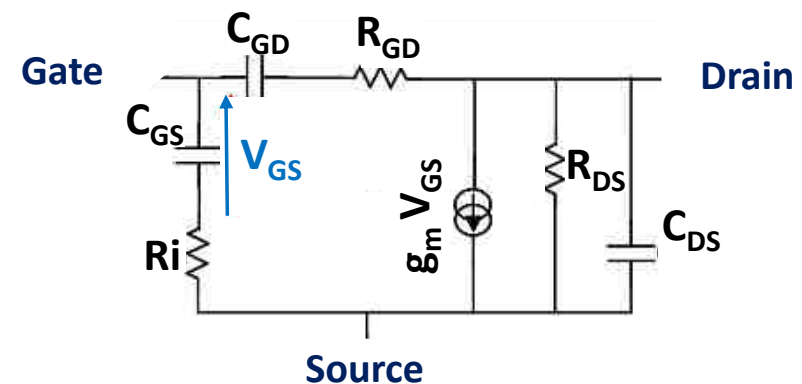
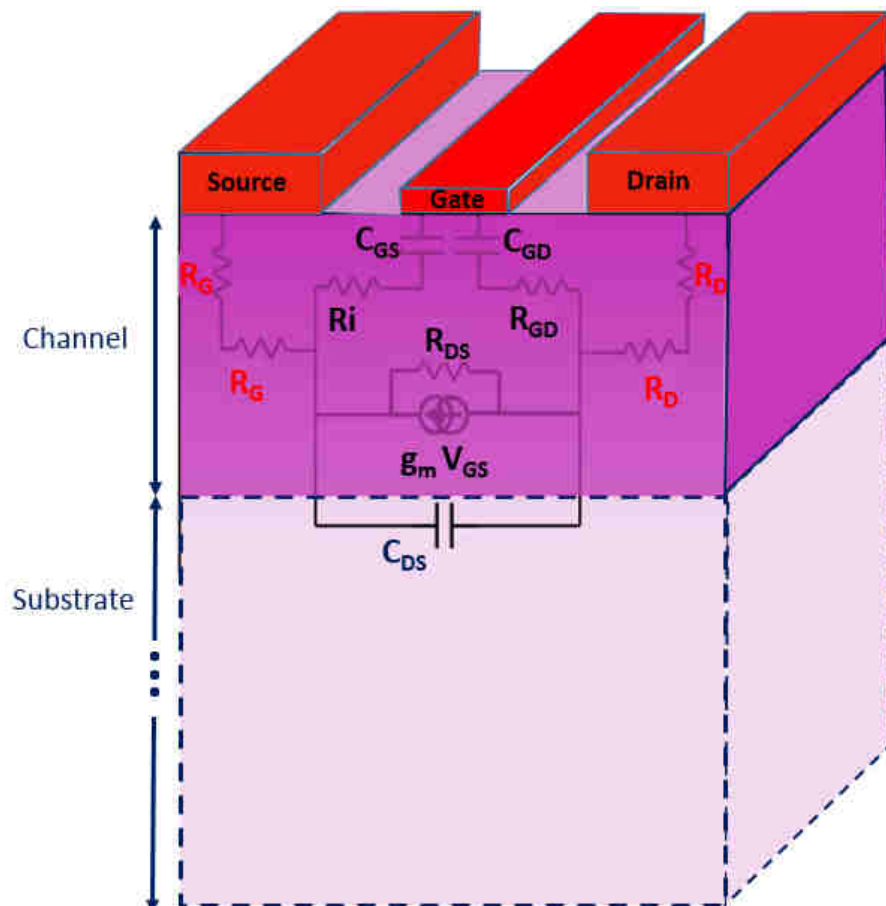


Extrinsic elements are the first ones that can be neglected when compared to other elements

$$G = 14 \text{ dB} \quad \begin{matrix} 15 \\ 13 \end{matrix}$$

I – Basics of MESFET operation

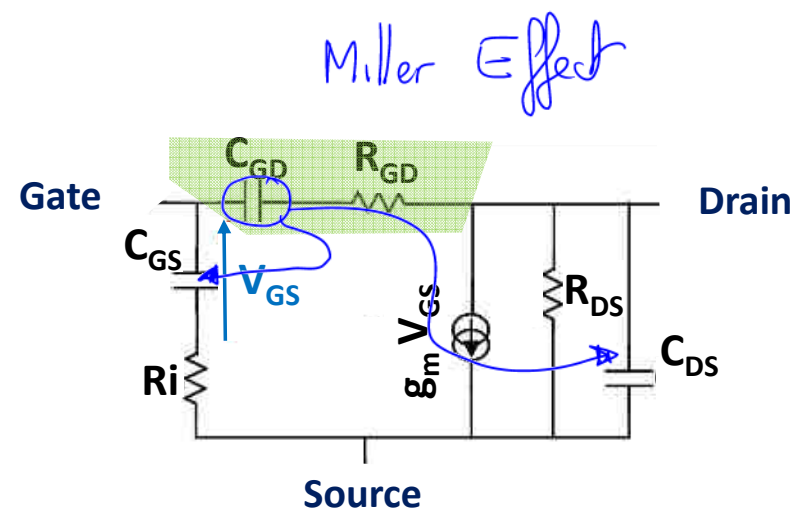
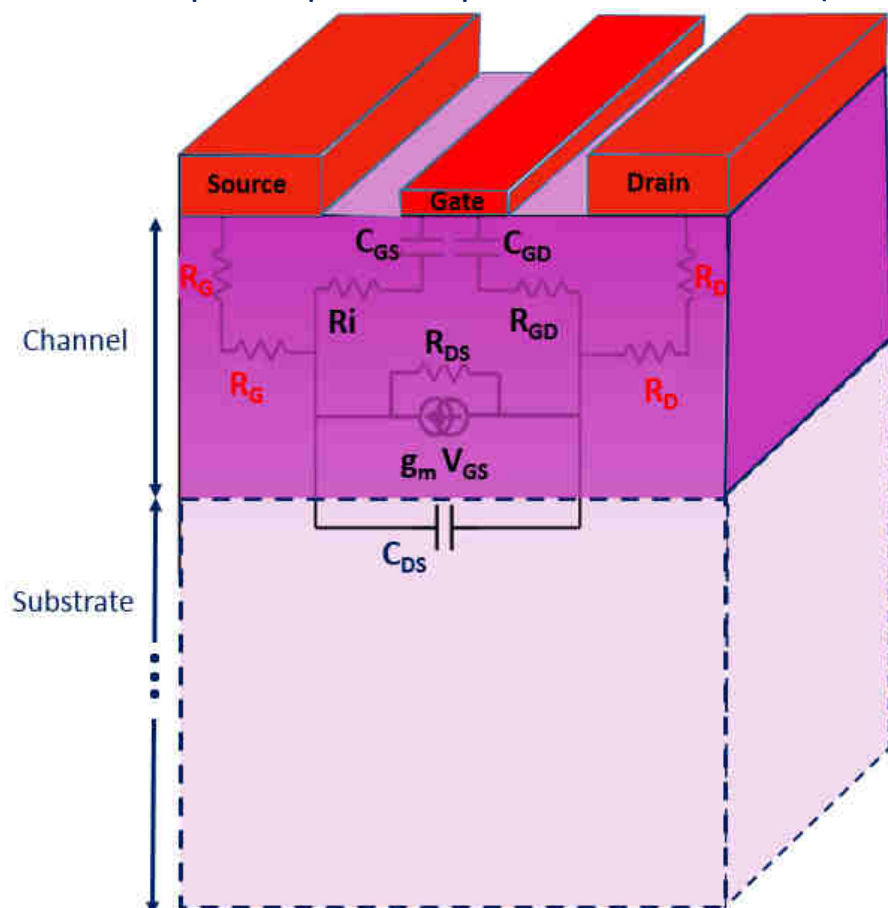
→ Simplified planar representation of FETs (localization of electrical lumped elements)



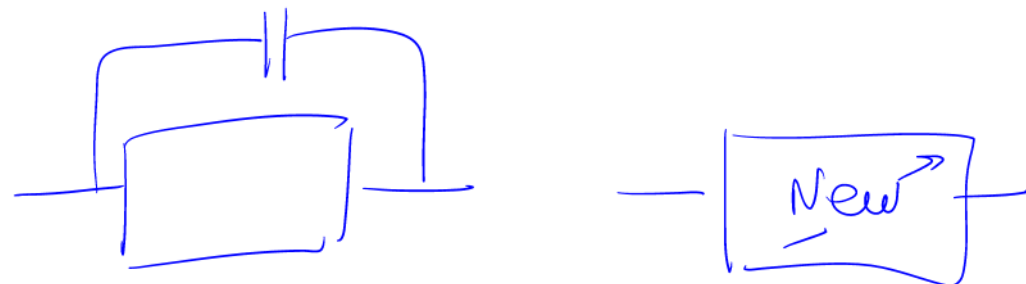
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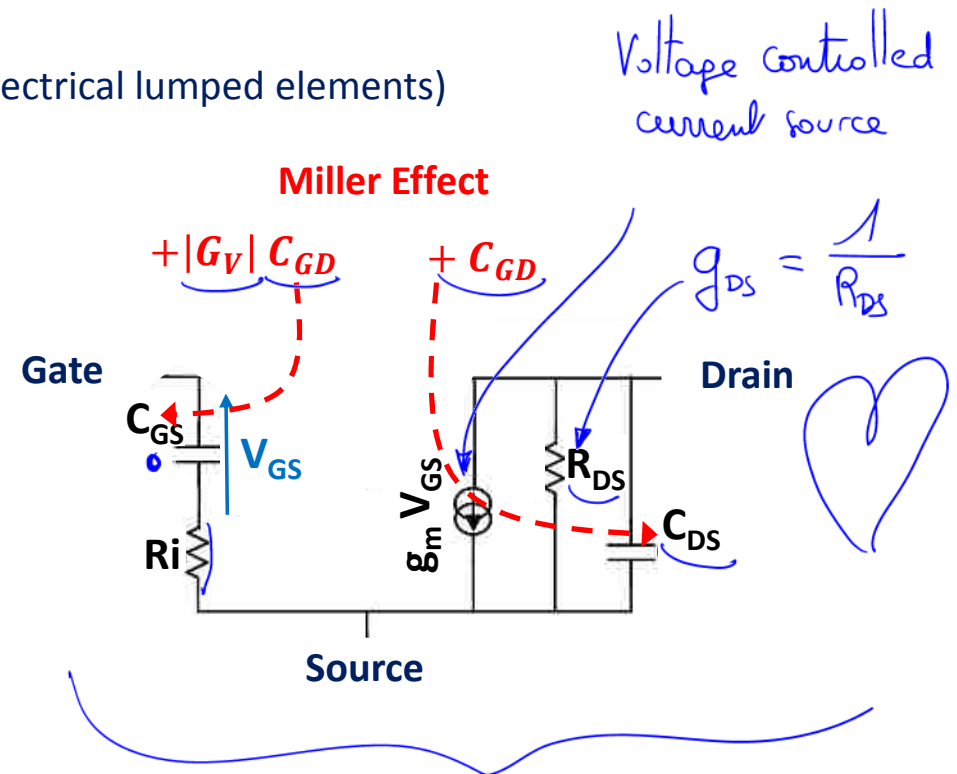
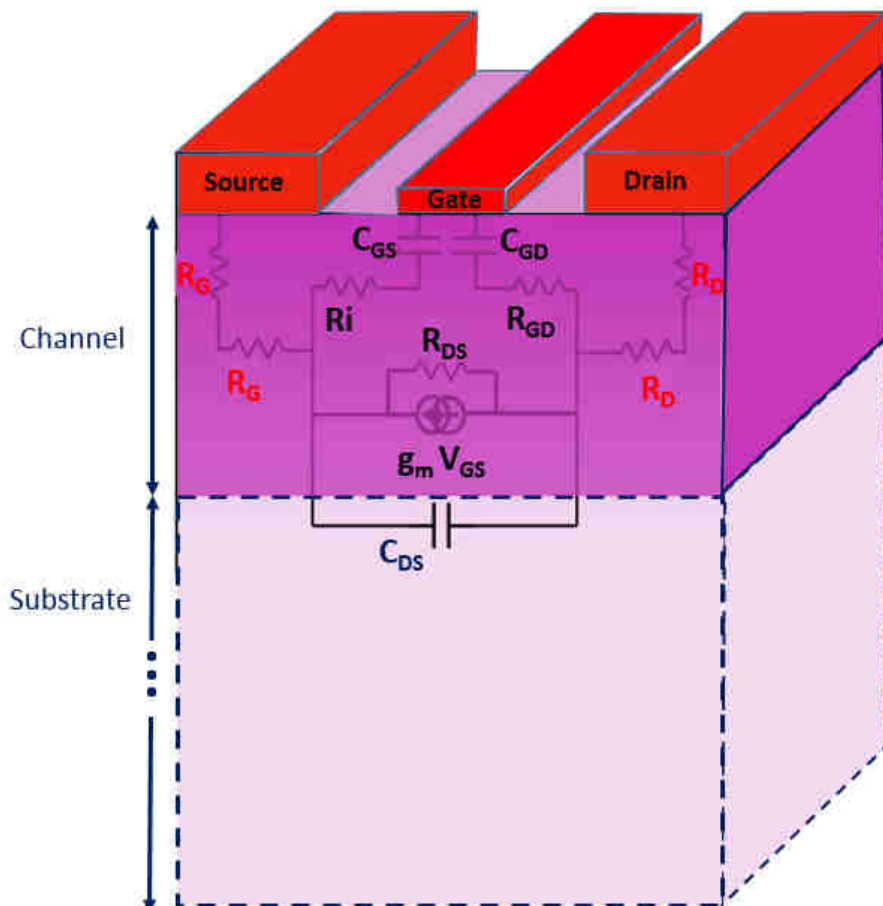


Feedback elements Gate-to-Drain can also be neglected.



I – Basics of MESFET operation

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Feedback elements Gate-to-Drain can also be neglected.

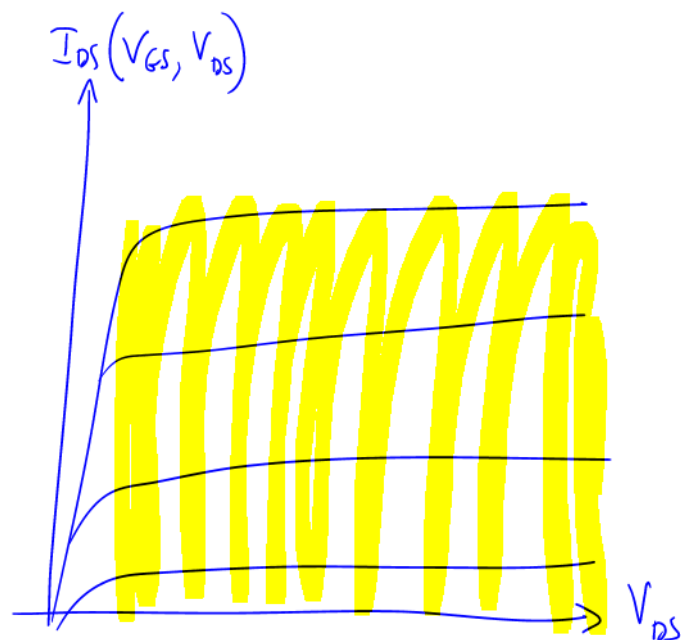
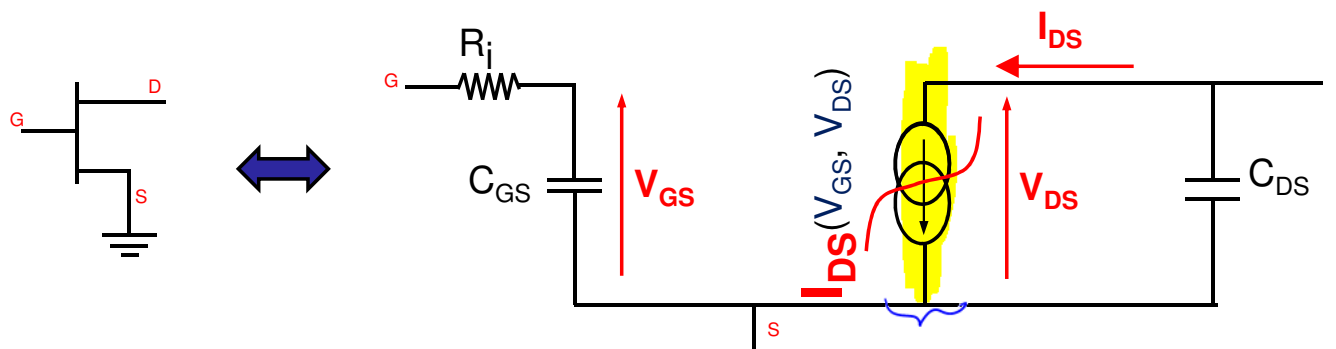
However, the capacitive feedback is taken into account by **Miller Effect**

$$V = RI$$

$$I = GV \quad \text{with } G = 1/R$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (g_m , g_d) around a specific bias point

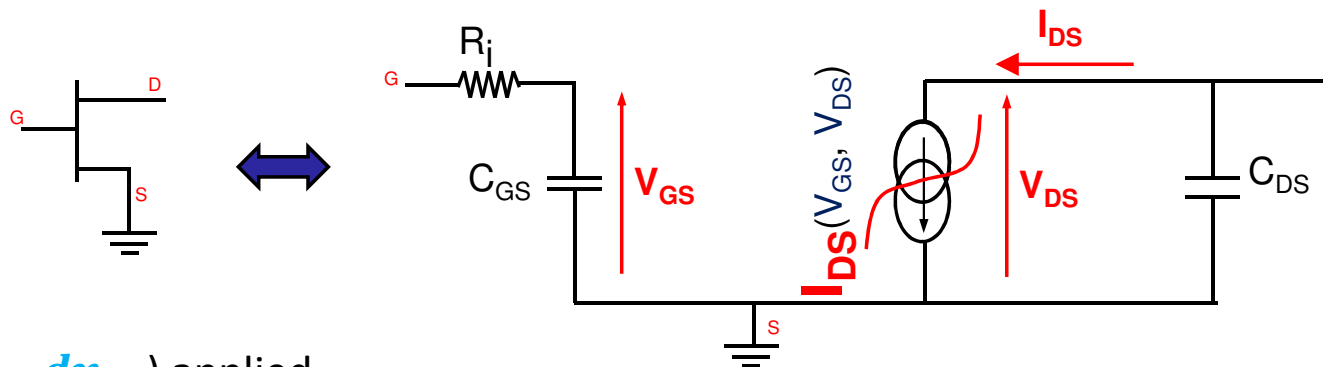


$$I_{DS} = I_{DSS} \left(1 - \left(\frac{V_{GS}}{V_P} \right)^2 \right) \left(1 + K V_{GS} \right)$$

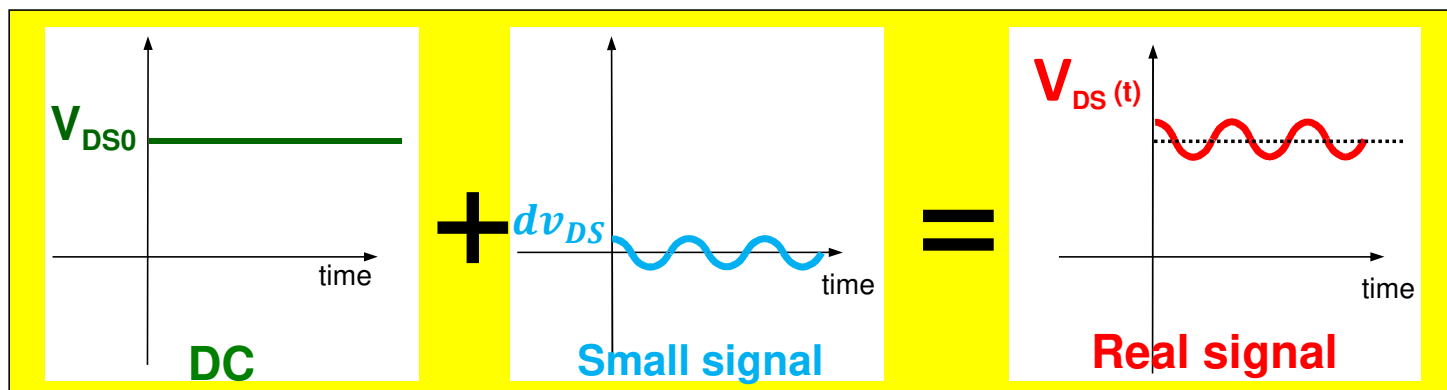
$$I_{DS}(t) = I_{DSS0} + \underbrace{I_{DS1}}_{\text{fundamental}} \cos(\omega t + \varphi) + \underbrace{I_{DS2}}_{\text{second harmonic}} \cos(2\omega t + \varphi)$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (g_m, g_d) around a specific bias point

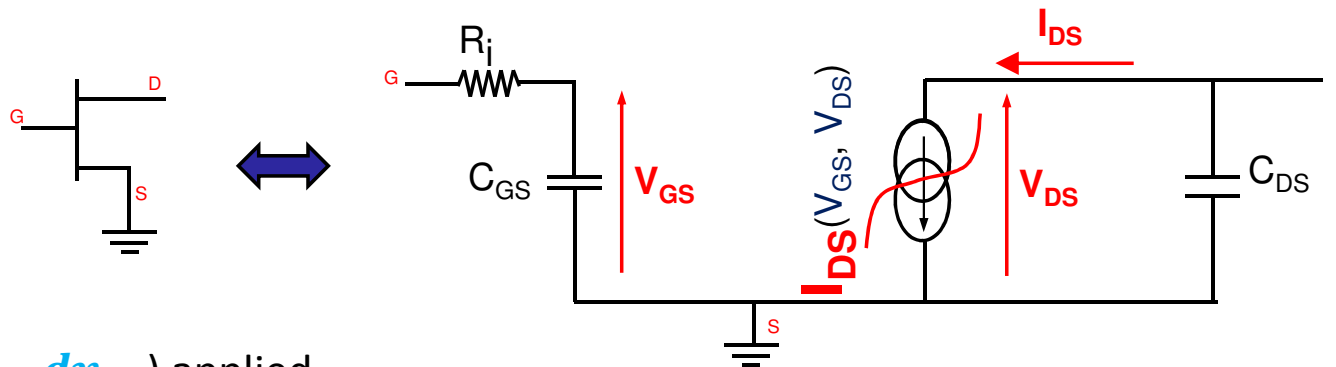


Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:



I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (g_m, g_d) around a specific bias point



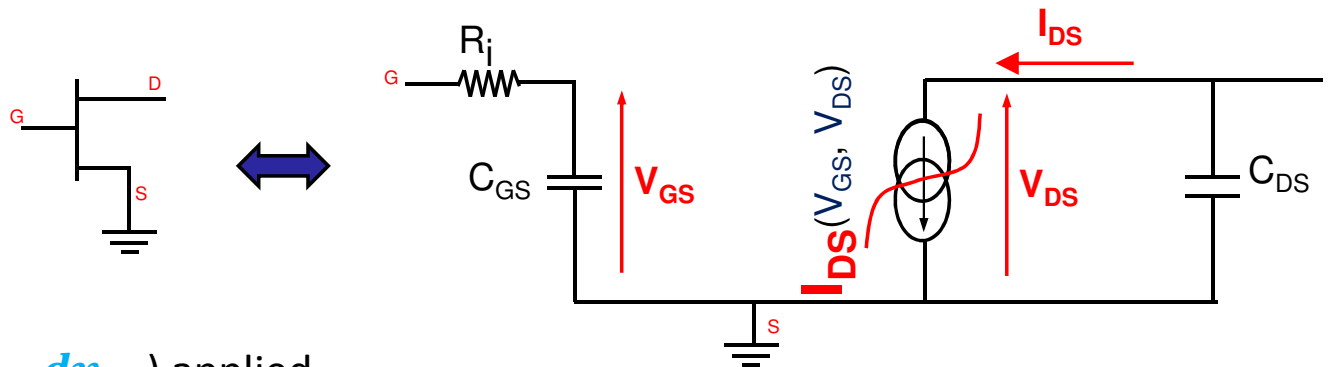
Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

$$V_{GS}(t) = V_{GS0} + dv_{GS}(t)$$

$$V_{DS}(t) = V_{DS0} + dv_{DS}(t)$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (g_m, g_d) around a specific bias point



Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

$$\begin{aligned}
 V_{GS}(t) &= V_{GS0} + \underline{dv_{GS}(t)} \\
 V_{DS}(t) &= V_{DS0} + \underline{dv_{DS}(t)}
 \end{aligned}
 \quad \Rightarrow \quad
 \begin{aligned}
 I_{DS}(t) &= F_{NL}(V_{GS}, V_{DS}) = F_{NL}(V_{GS0}, V_{DS0}) + \underline{dF_{NL}} \\
 &= I_{DS0} + \underline{dF_{NL}} \\
 I_{DS}(t) &= I_{DS0} + \underline{di_{DS}}
 \end{aligned}$$

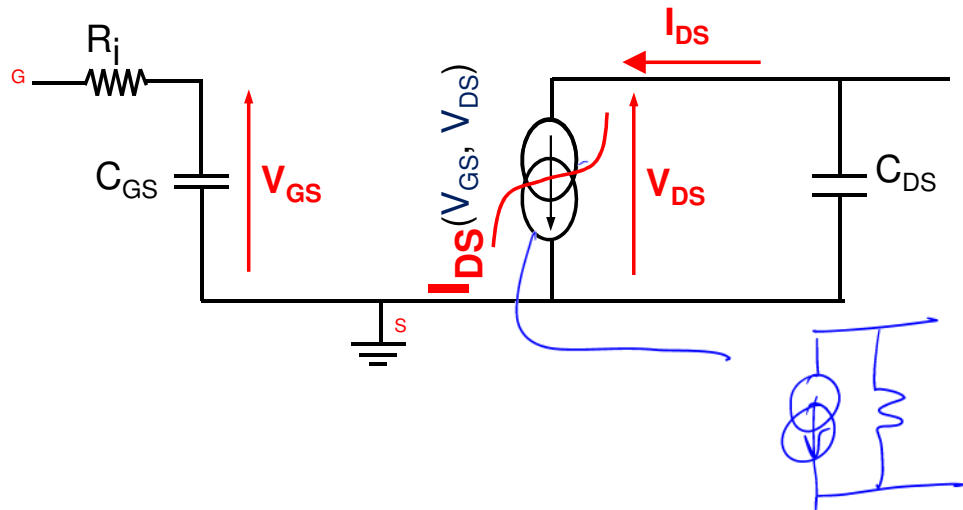
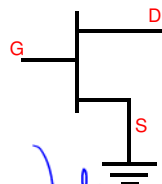
Taylor expansion

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (g_m , g_d) around a specific bias point

$$f(x, y)$$

$$df = \left(\frac{\partial f}{\partial x} \right) dx + \left(\frac{\partial f}{\partial y} \right) dy$$



Small signals (dv_{GS} , dv_{DS}) applied around the bias point (V_{GS0} , V_{DS0}) give:

$$V_{GS}(t) = V_{GS0} + dv_{GS}(t)$$

$$V_{DS}(t) = V_{DS0} + dv_{DS}(t)$$



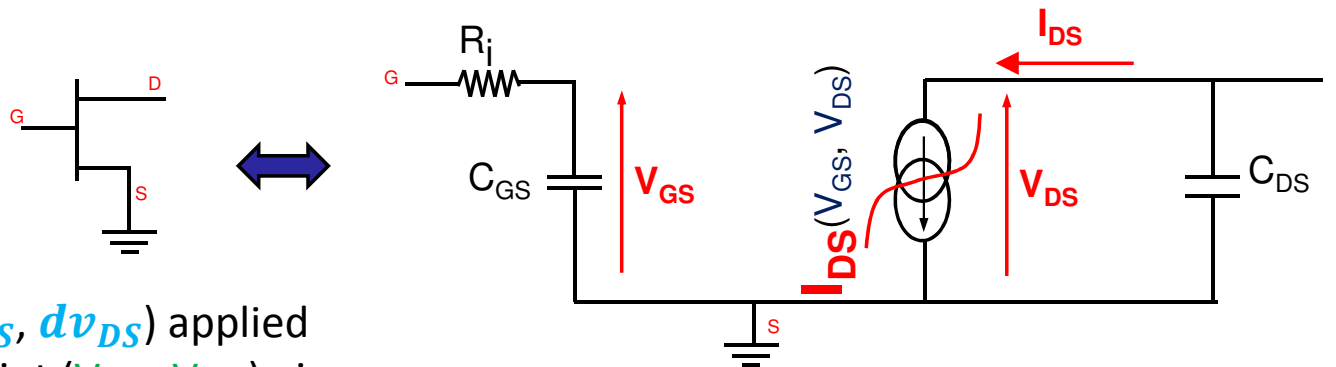
$$I_{DS}(t) = I_{DS0} + di_{DS}$$

Taylor expansion

$$di_{DS} = dF_{NL} = \underbrace{\left(\frac{\partial I_{DS}}{\partial V_{GS}} \right)_{(V_{GS0}, V_{DS0})}}_{g_m} \cdot dv_{GS} + \underbrace{\left(\frac{\partial I_{DS}}{\partial V_{DS}} \right)_{(V_{GS0}, V_{DS0})}}_{g_d = 1/R_{os}} \cdot dv_{DS}$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (g_m, g_d) around a specific bias point



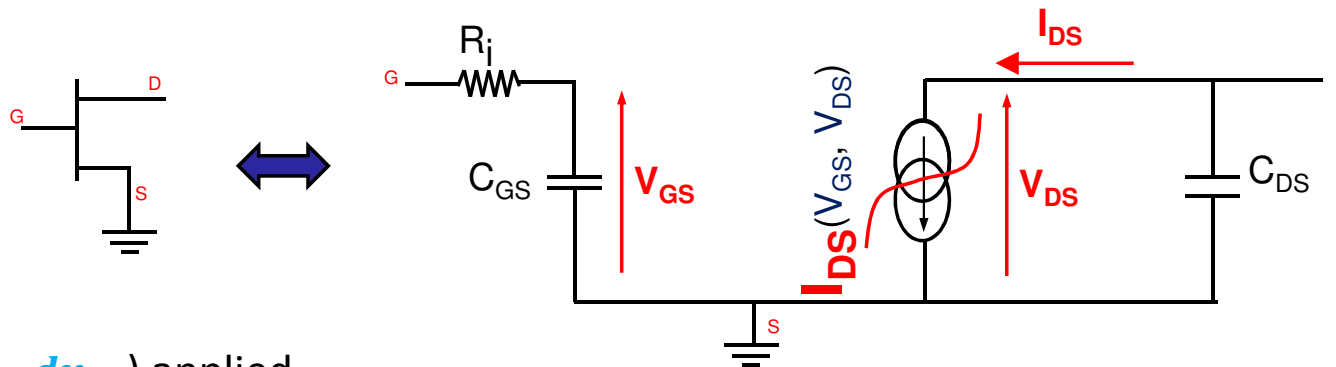
Small signals (dv_{GS} , dv_{DS}) applied around the bias point (V_{GS0} , V_{DS0}) give:

$$\begin{matrix} dv_{GS}(t) \\ dv_{DS}(t) \end{matrix} \longrightarrow I_{DS}(t) = I_{DS0} + di_{DS}$$

$$di_{DS} = dF_{NL} = \left. \left(\frac{\partial I_{DS}}{\partial V_{GS}} \right) \right|_{(V_{GS0}, V_{DS0})} \cdot dv_{GS} + \left. \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right) \right|_{(V_{GS0}, V_{DS0})} \cdot dv_{DS} = g_m \cdot dv_{GS} + g_{DS} \cdot dv_{DS}$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (g_m , g_d) around a specific bias point



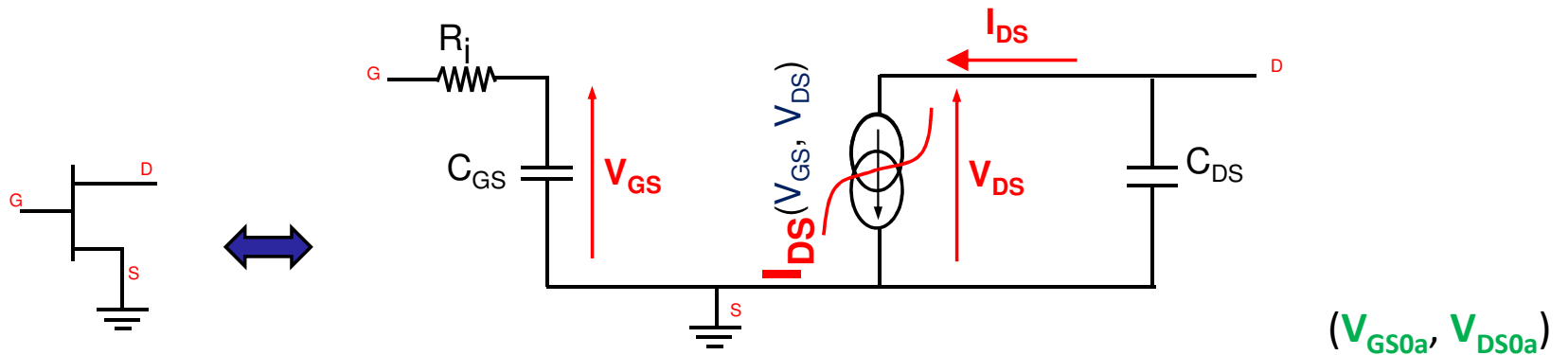
Small signals (dv_{GS} , dv_{DS}) applied around the bias point (V_{GS0} , V_{DS0}) give:

$$\begin{matrix} dv_{GS}(t) \\ dv_{DS}(t) \end{matrix} \longrightarrow di_{DS} = g_m \cdot dv_{GS} + g_{DS} \cdot dv_{DS}$$

$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right) \bigg|_{(V_{GS0}, V_{DS0})}$$

$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}} \right) \bigg|_{(V_{GS0}, V_{DS0})}$$

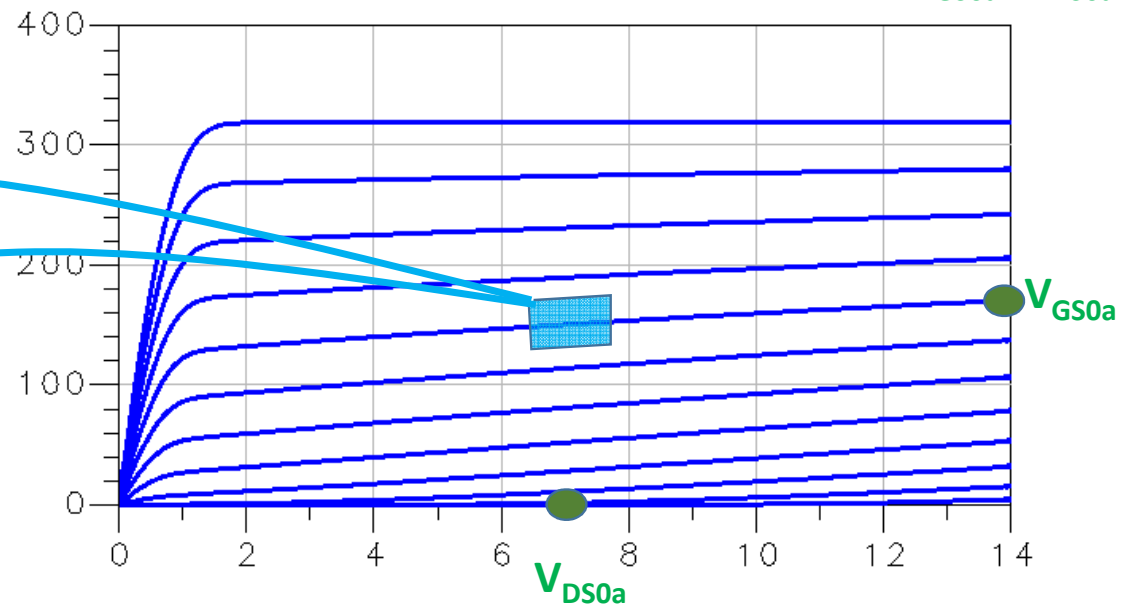
I – Basics of FET operation



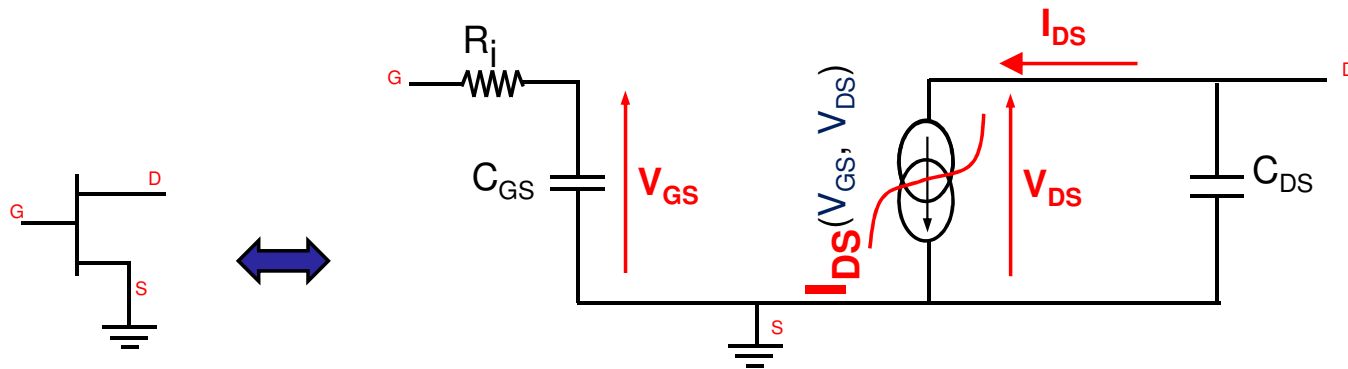
Small signals (dv_{GS} , dv_{DS}) applied around the bias point (V_{GS0} , V_{DS0}) give:

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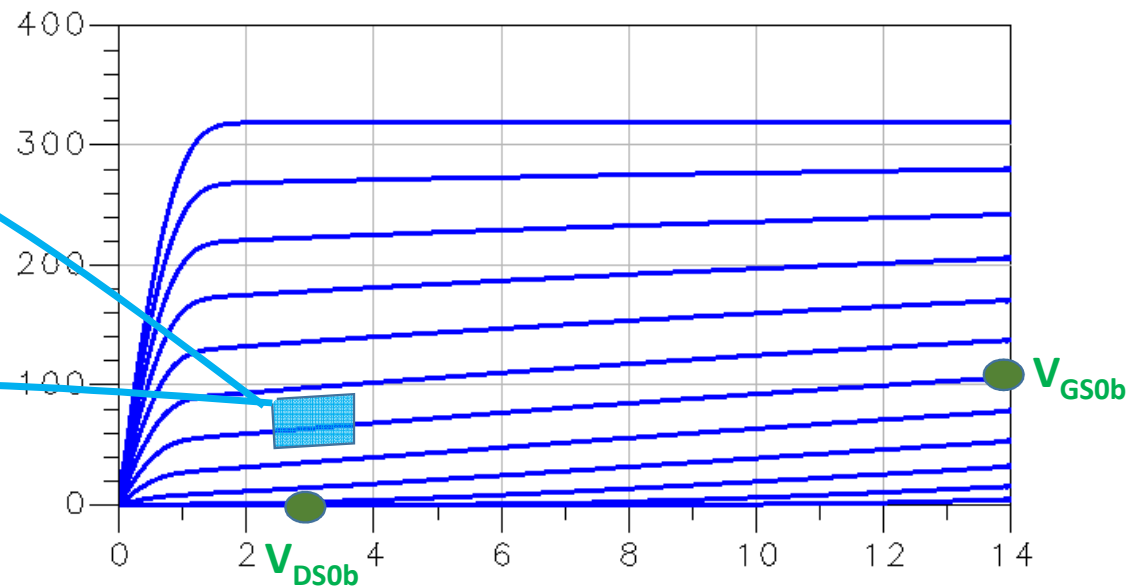
I – Basics of FET operation



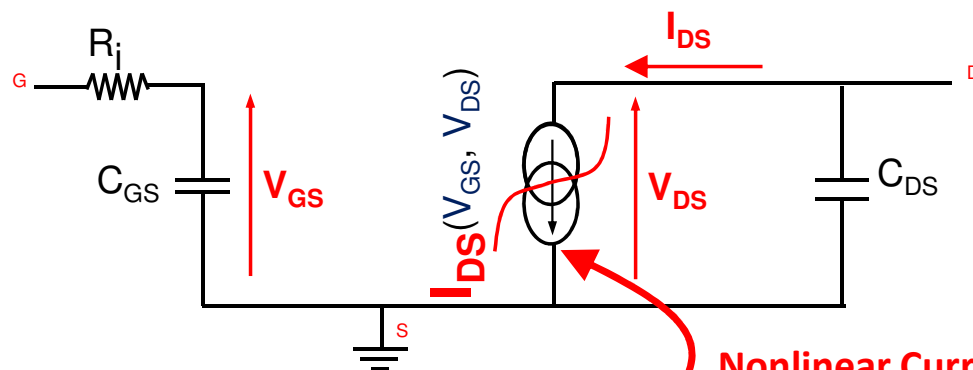
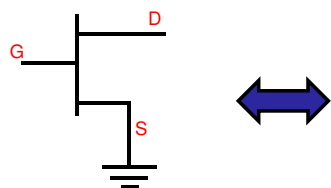
Small signals (dv_{GS} , dv_{DS}) applied around the bias point (V_{GS0} , V_{DS0}) give:

$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right) \bigg|_{(V_{GS0}, V_{DS0})}$$

$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}} \right) \bigg|_{(V_{GS0}, V_{DS0})}$$



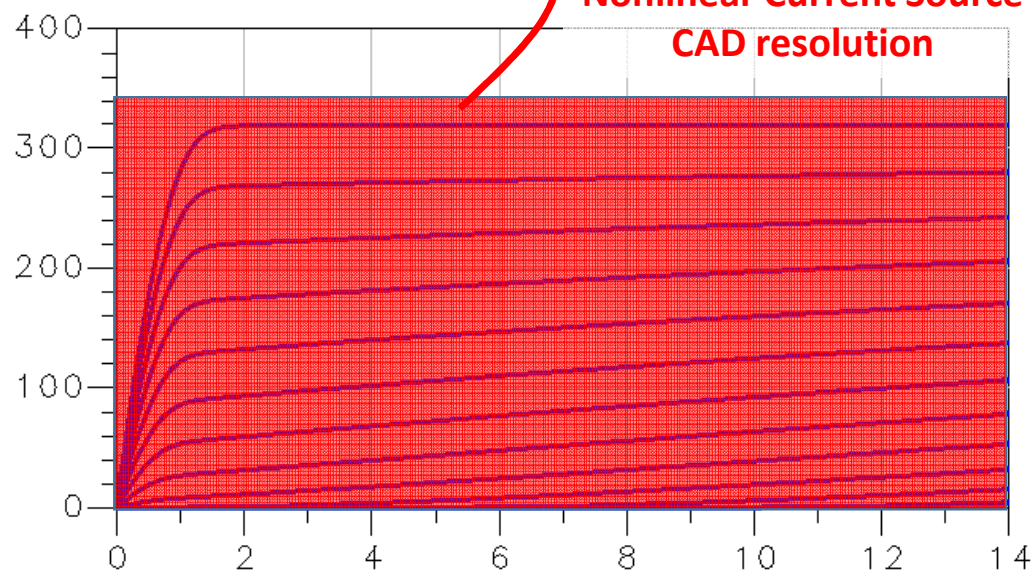
I – Basics of FET operation



Large signals (ΔV_{GS} , ΔV_{DS}) applied around the bias point (V_{GS0} , V_{DS0}) give:

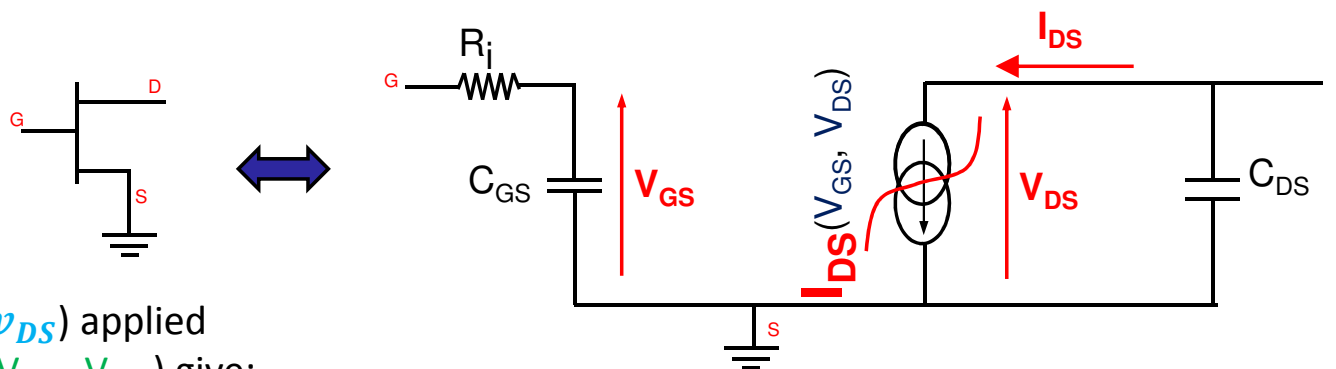
~~$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right) \bigg|_{(V_{GS0}, V_{DS0})}$$~~

~~$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}} \right) \bigg|_{(V_{GS0}, V_{DS0})}$$~~



I – Basics of FET operation

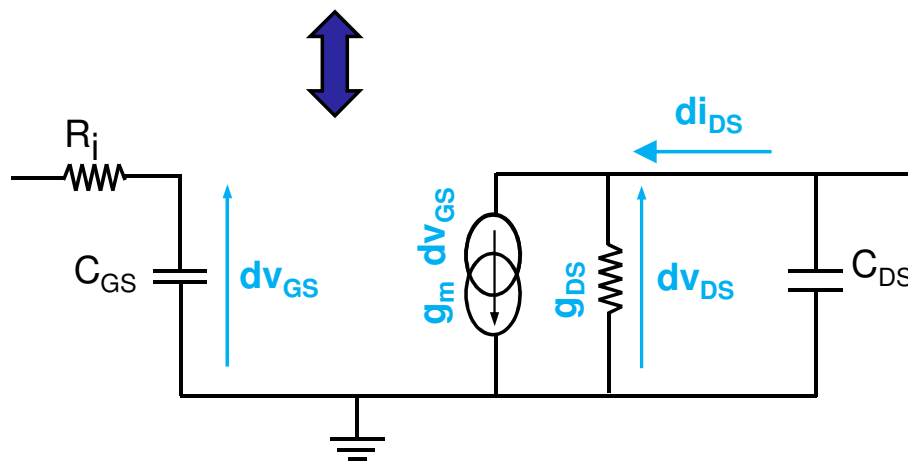
→ Simplified Small-signal equivalent of the nonlinear drain current (g_m , g_d) around a specific bias point



Small signals (dv_{GS} , dv_{DS}) applied around the bias point (V_{GS0} , V_{DS0}) give:

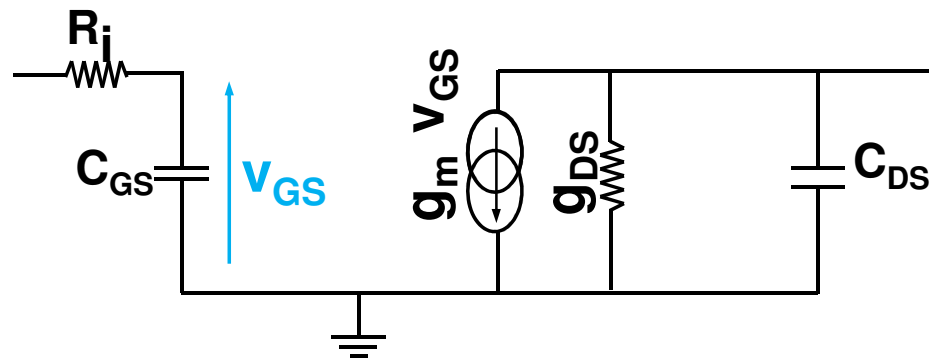
$$V_{GS} = V_{GS0} + dv_{GS}$$

$$V_{DS} = V_{DS0} + dv_{DS}$$



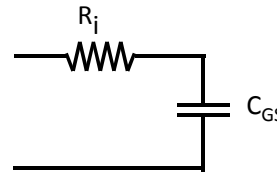
I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (g_m , g_d) around a specific bias point



II – Intrinsic figures of merit for FETs

1) Low-Pass Frequency (Low-Pass Input RC circuit)



$$f_{LP} = \frac{1}{2\pi R_i C_{GS}}$$

The FET is efficiently used at frequencies $f \ll f_{LP} \rightarrow R_i C_{GS} \omega \ll 1$

2) Cutoff frequency of gain current

Current Gain in Short-Circuit

$$G_{iSC} = \frac{I_{OUTSC}}{I_{IN}} = \frac{g_m V_{GS}}{j C_{GS} \omega V_{GS}} = \frac{g_m}{j C_{GS} \omega} \rightarrow |G_{iSC}(f_c)| \stackrel{\text{def}}{=} 1 \Leftrightarrow \frac{g_m}{C_{GS} \omega_c} = 1 \Leftrightarrow \omega_c = \frac{g_m}{C_{GS}}$$

$$f_c = \frac{g_m}{2\pi C_{GS}}$$

f_c is widely used to compare FETs with each other

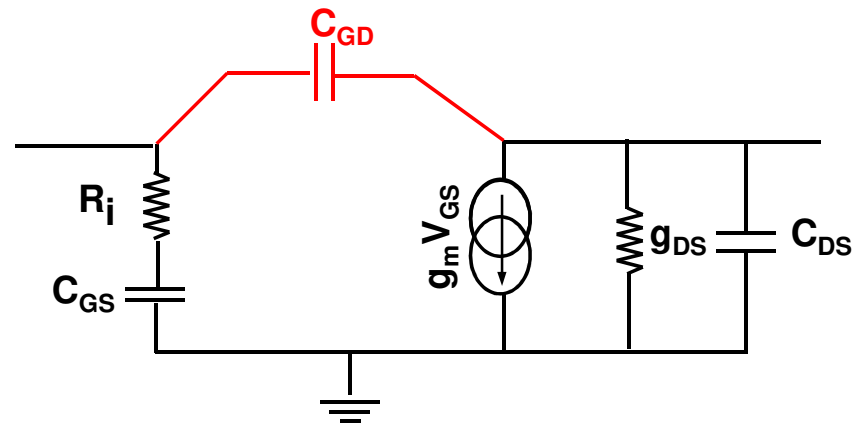
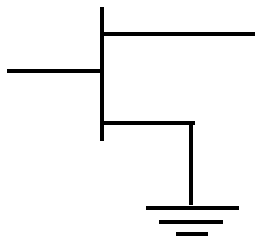
→ Narrowband equivalence between (series RC) and (parallel RC) circuit at the FET input



$$G_{IN}(\omega) = R_i C_{GS}^2 \omega^2$$

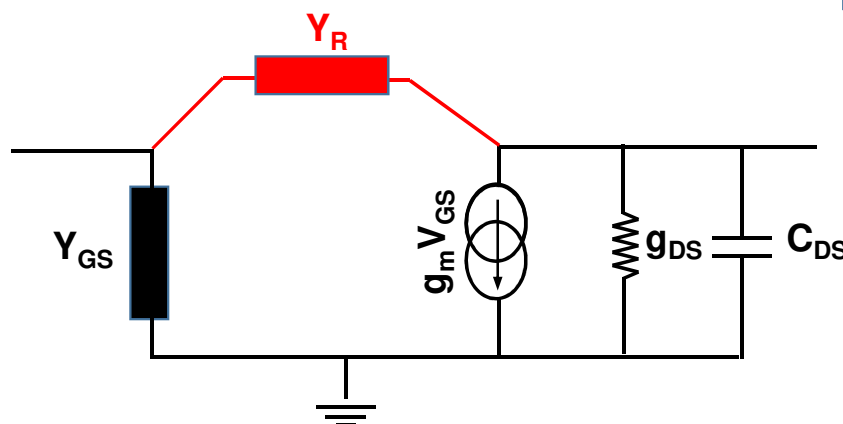
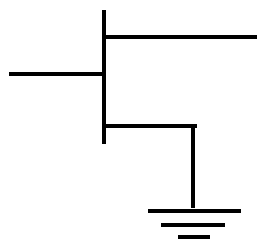
II – Intrinsic figures of merit for FETs

3) **Miller Effect** (Feedback admittance Y_R and conductance load G_L)



II – Intrinsic figures of merit for FETs

3) **Miller Effect** (Feedback admittance Y_R and conductance load G_L)

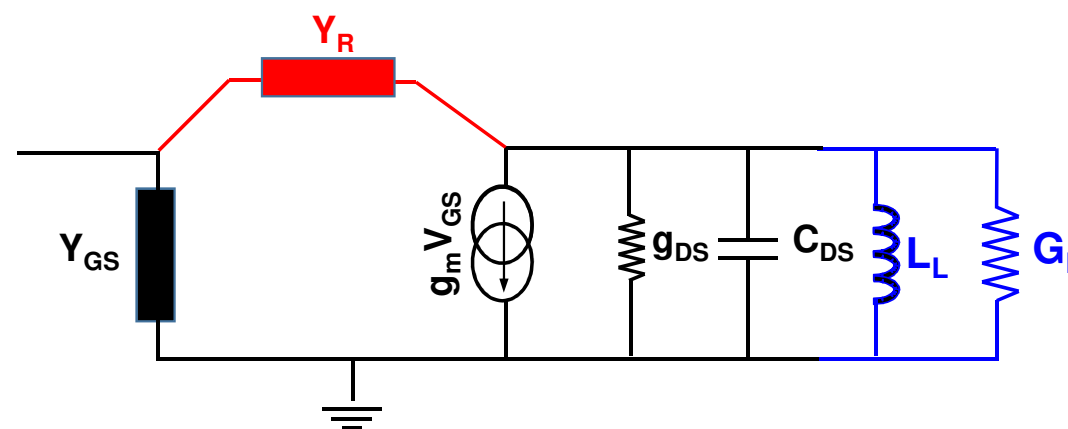
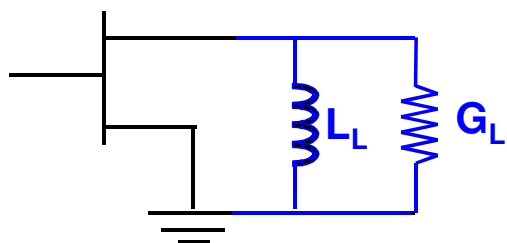
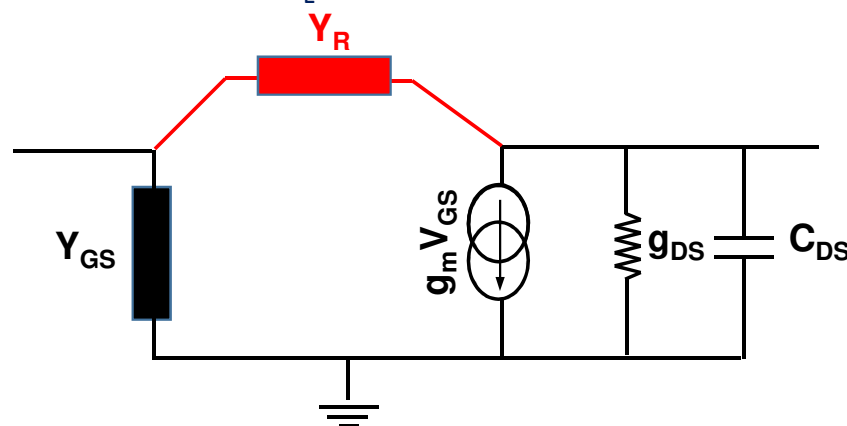
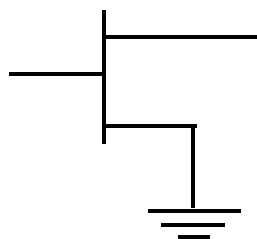


$$Y_R = j C_{GD} \omega$$

$$Y_{GS} = \frac{1}{R_i + \frac{1}{j C_{GS} \omega}}$$

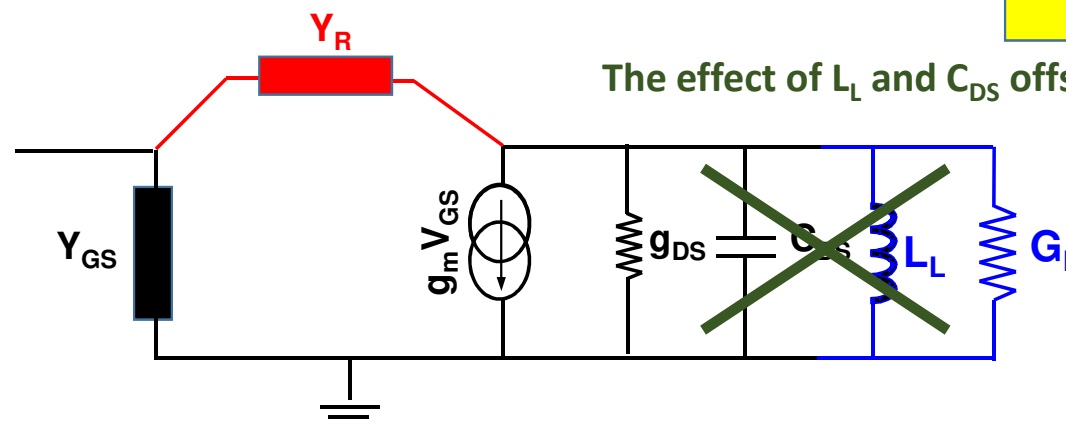
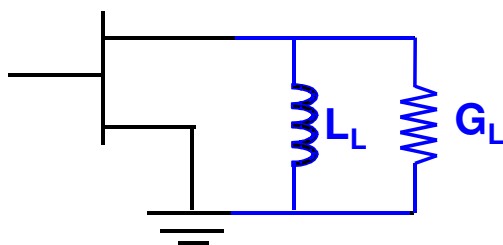
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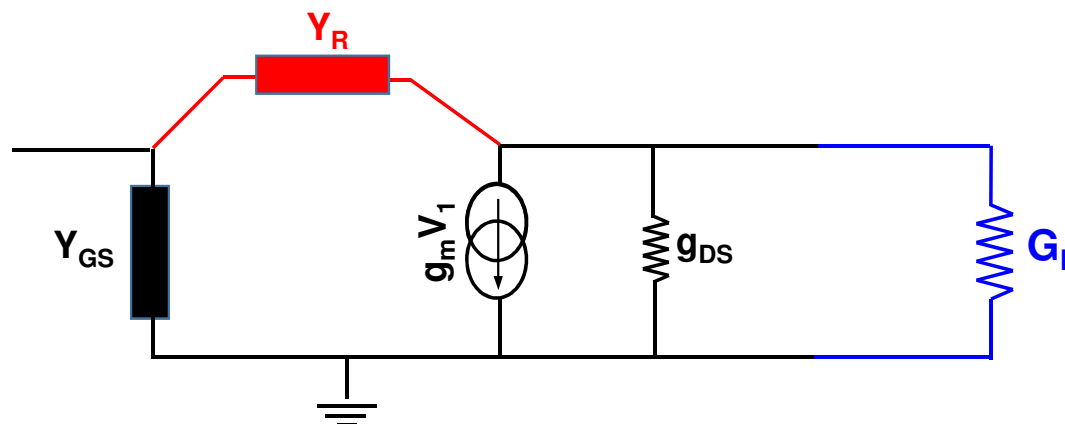
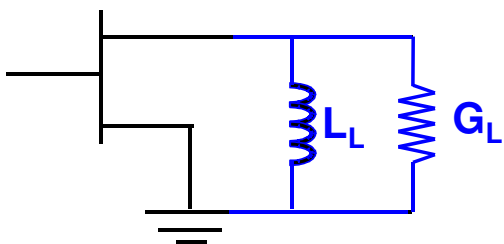


$$L_L C_{DS} \omega_o^2 = 1 \rightarrow L_L = \frac{1}{C_{DS} \omega_o^2}$$

The effect of L_L and C_{DS} offset each other

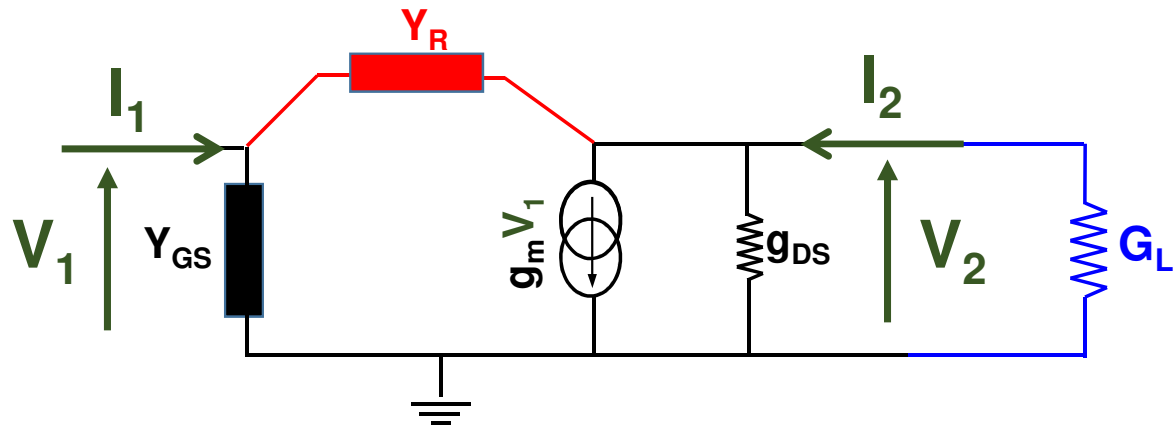
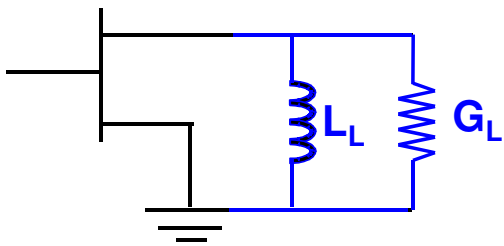
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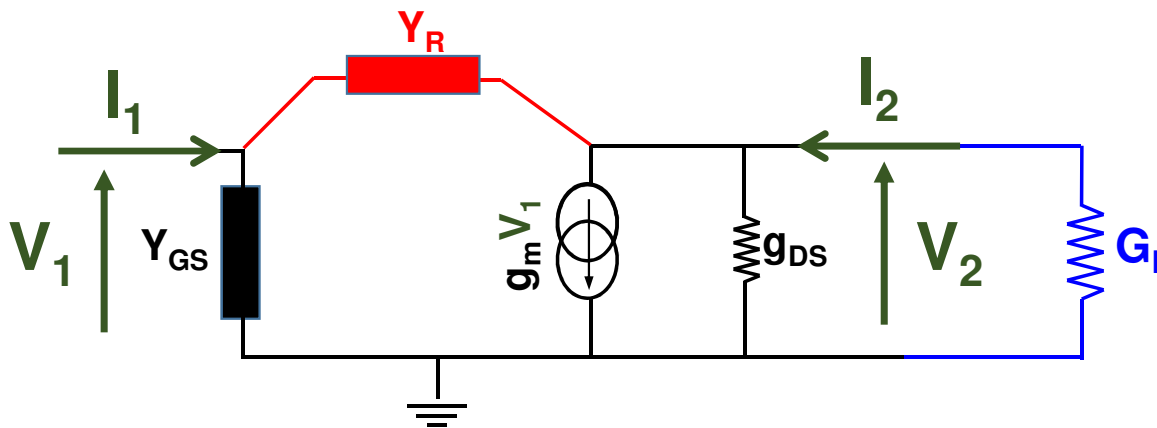
II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

a) Voltage gain G_V

$$G_V = \frac{V_2}{V_1} = -\frac{g_m - Y_R}{g_{DS} + G_L + Y_R} \rightarrow -\frac{g_m}{g_{DS} + G_L} \rightarrow -\frac{g_m}{2g_{DS}}$$

TUTORIAL

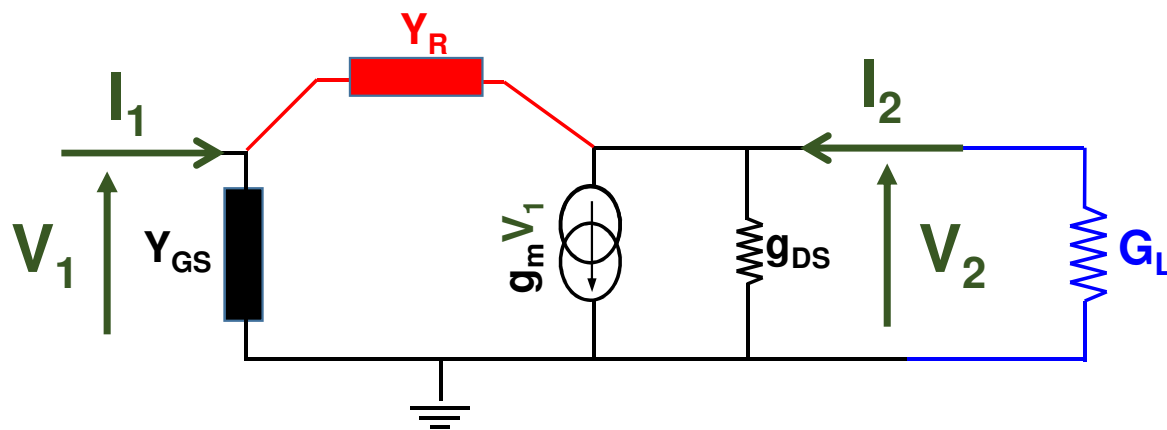


II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

b) Input admittance Y_{IN}

$$Y_{IN} = \frac{I_1}{V_1} = Y_{GS} + Y_R[1 - G_V]$$



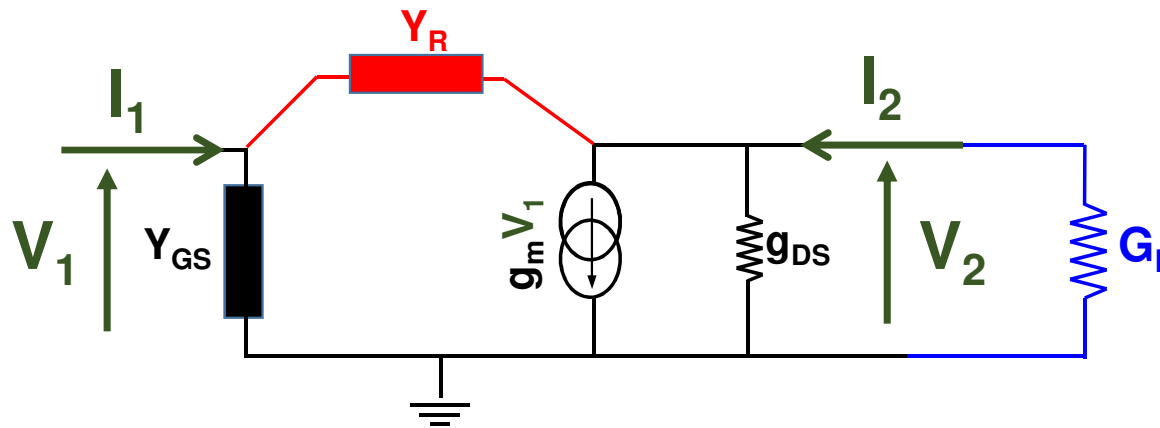
TUTORIAL

II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

c) Output admittance seen by the drain current source Y_{OUT}

$$Y_{OUT} = \frac{-g_m V_1}{V_2} = g_{DS} + G_L + Y_R \left[1 - \frac{1}{G_V} \right]$$



TUTORIAL

II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

b) Input admittance Y_{IN}

$$Y_{IN} = Y_{GS} + Y_R [1 - G_V]$$

$$\rightarrow Y_{GS} + Y_R |G_V|$$

$$G_V < 0 \quad \text{and} \quad |G_V| \gg 1$$



c) Output admittance seen by the drain current source Y_{OUT}

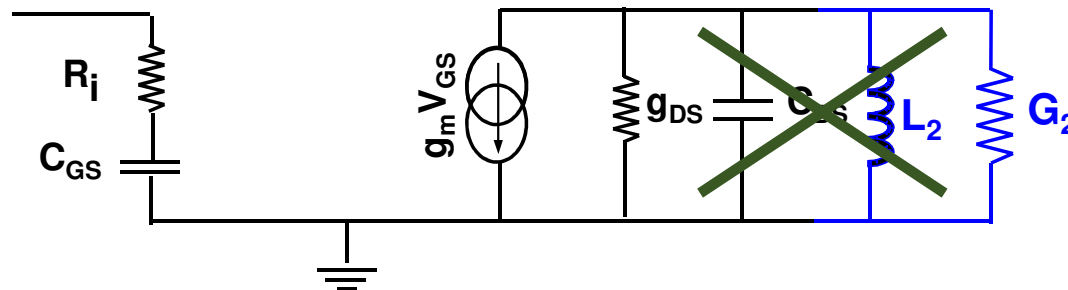
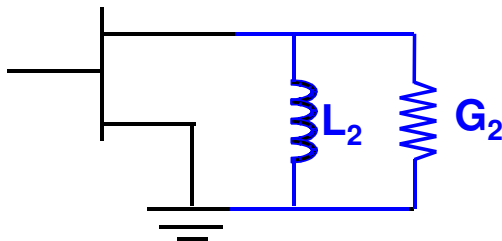
$$Y_{OUT} = g_{DS} + G_L + Y_R \left[1 - \frac{1}{G_V} \right]$$

$$\rightarrow g_{DS} + G_L + Y_R$$

II – Intrinsic figures of merit for FETs

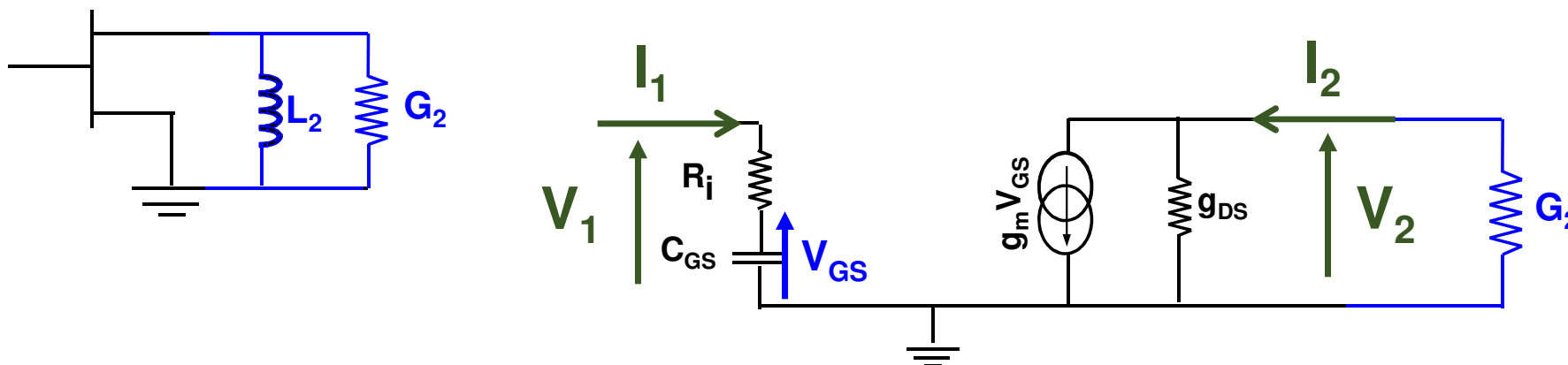
3) Maximum Power Gain G_{MAX} → Simplified Electrical Small-Signal FET Model

$$L_2 C_{DS} \omega^2 = 1 \rightarrow L_2 = \frac{1}{C_{DS} \omega^2}$$



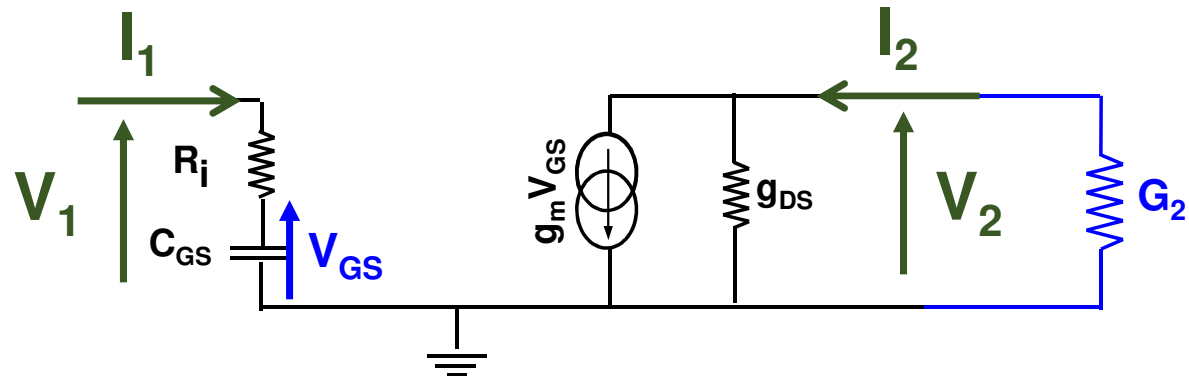
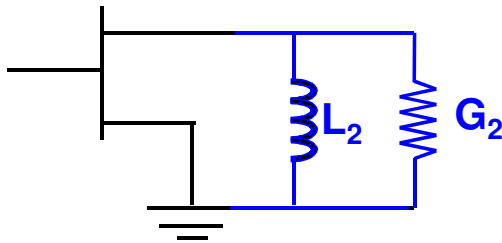
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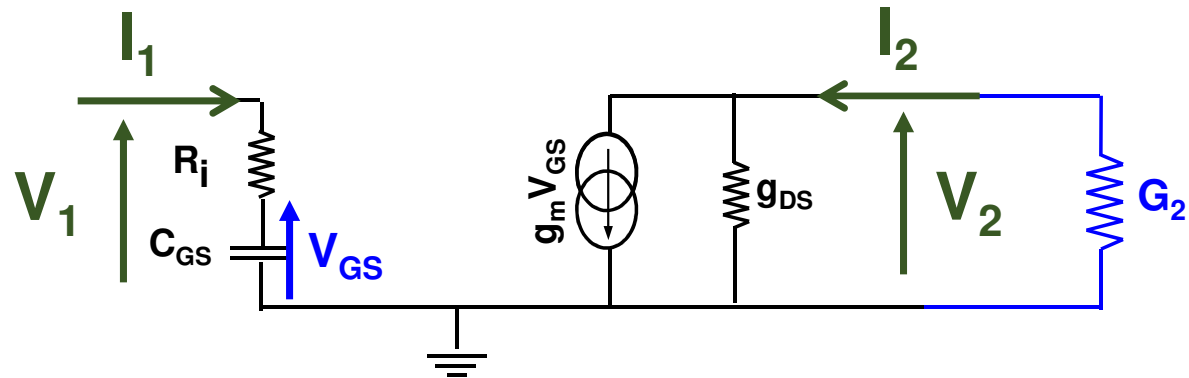
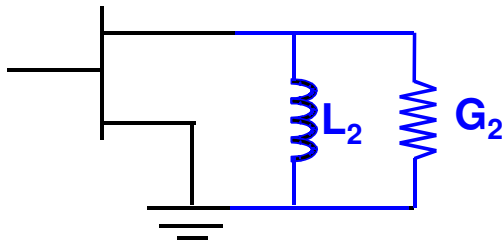
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General case ($G_2 \neq g_{DS}$) → Not maximum Power Gain G_P

$$G_P = \frac{G_2}{[G_2 + g_{DS}]^2} g_m^2$$

II – Intrinsic figures of merit for FETs

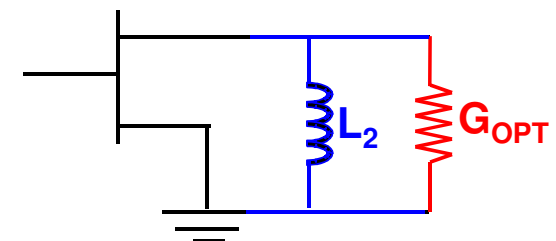
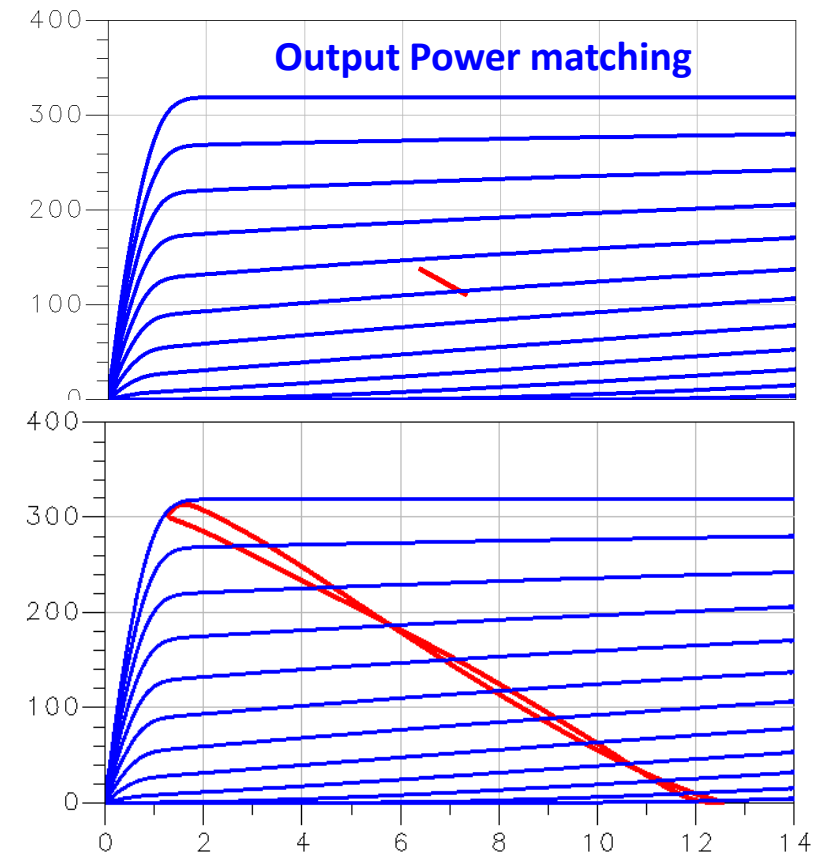
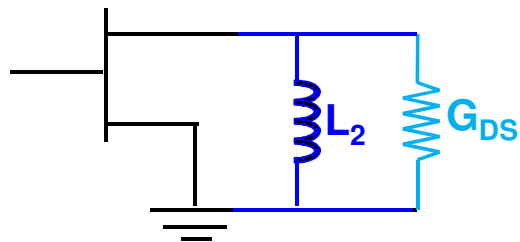
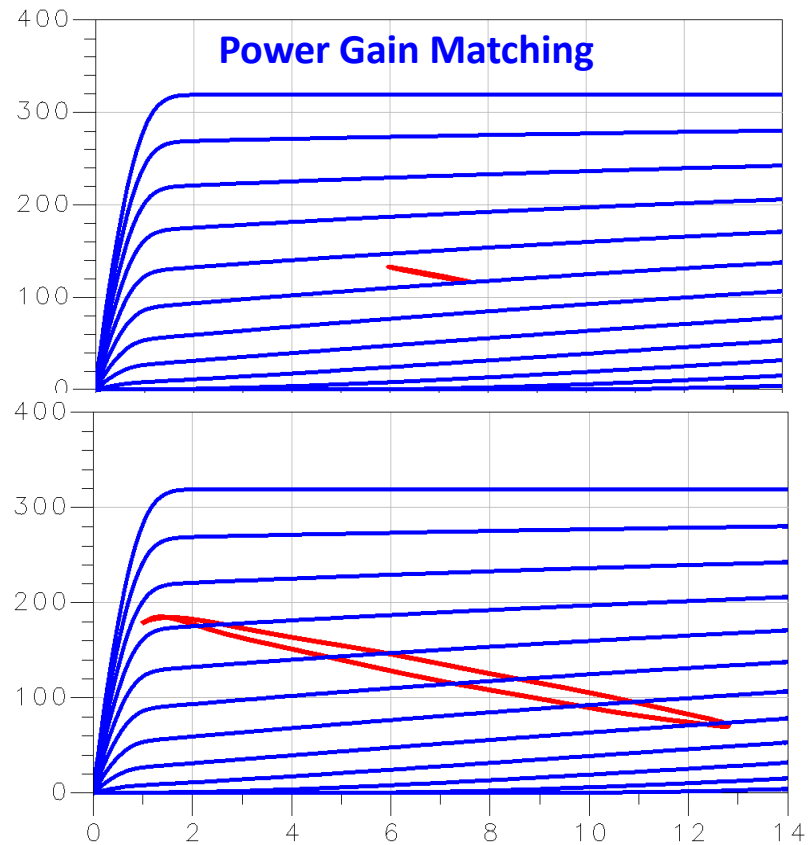
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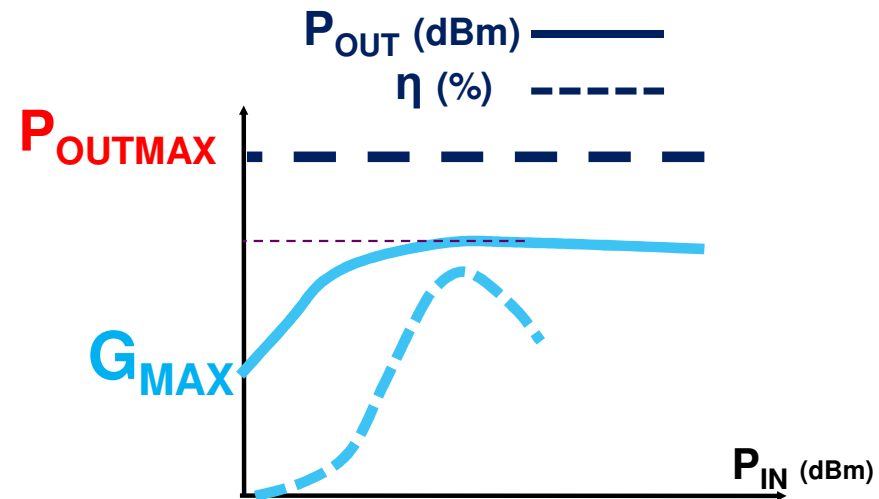
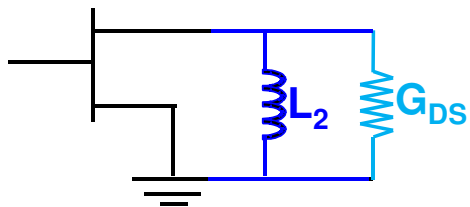
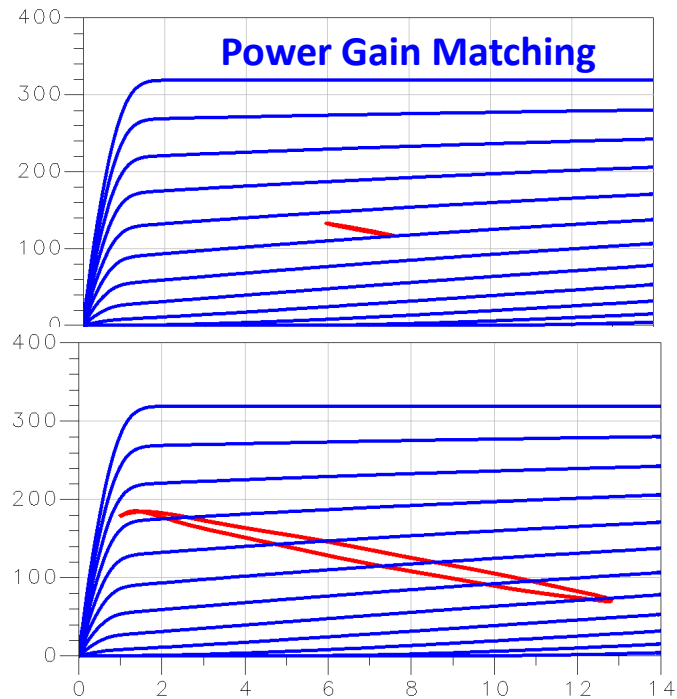


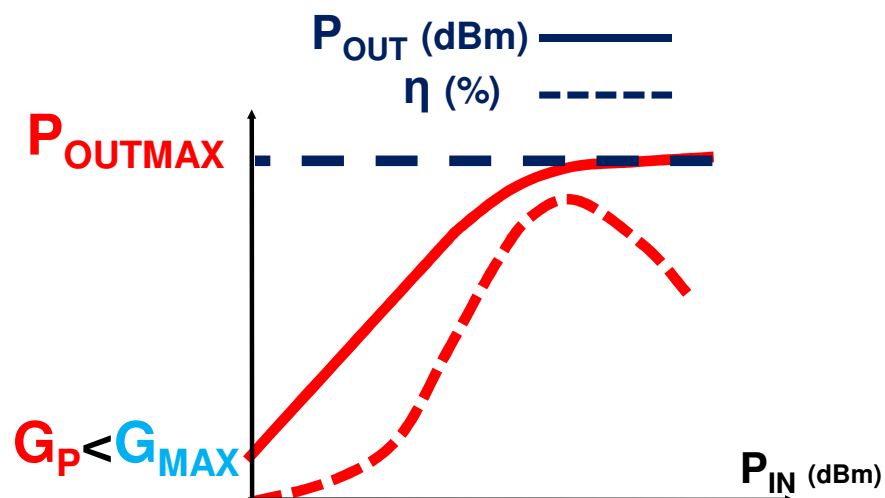
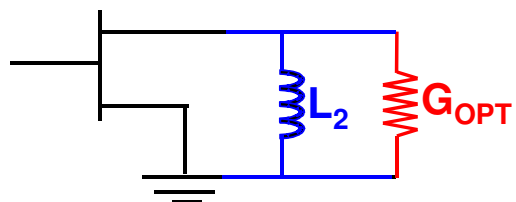
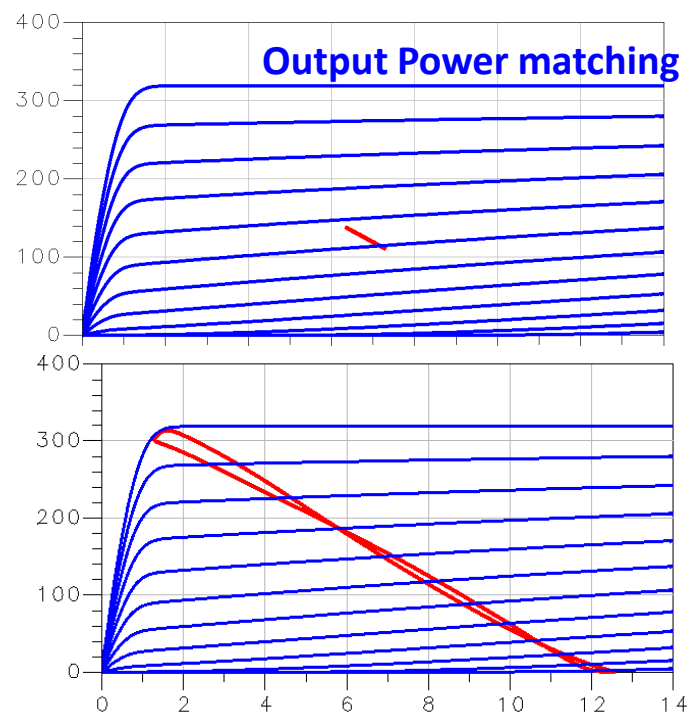
TUTORIAL

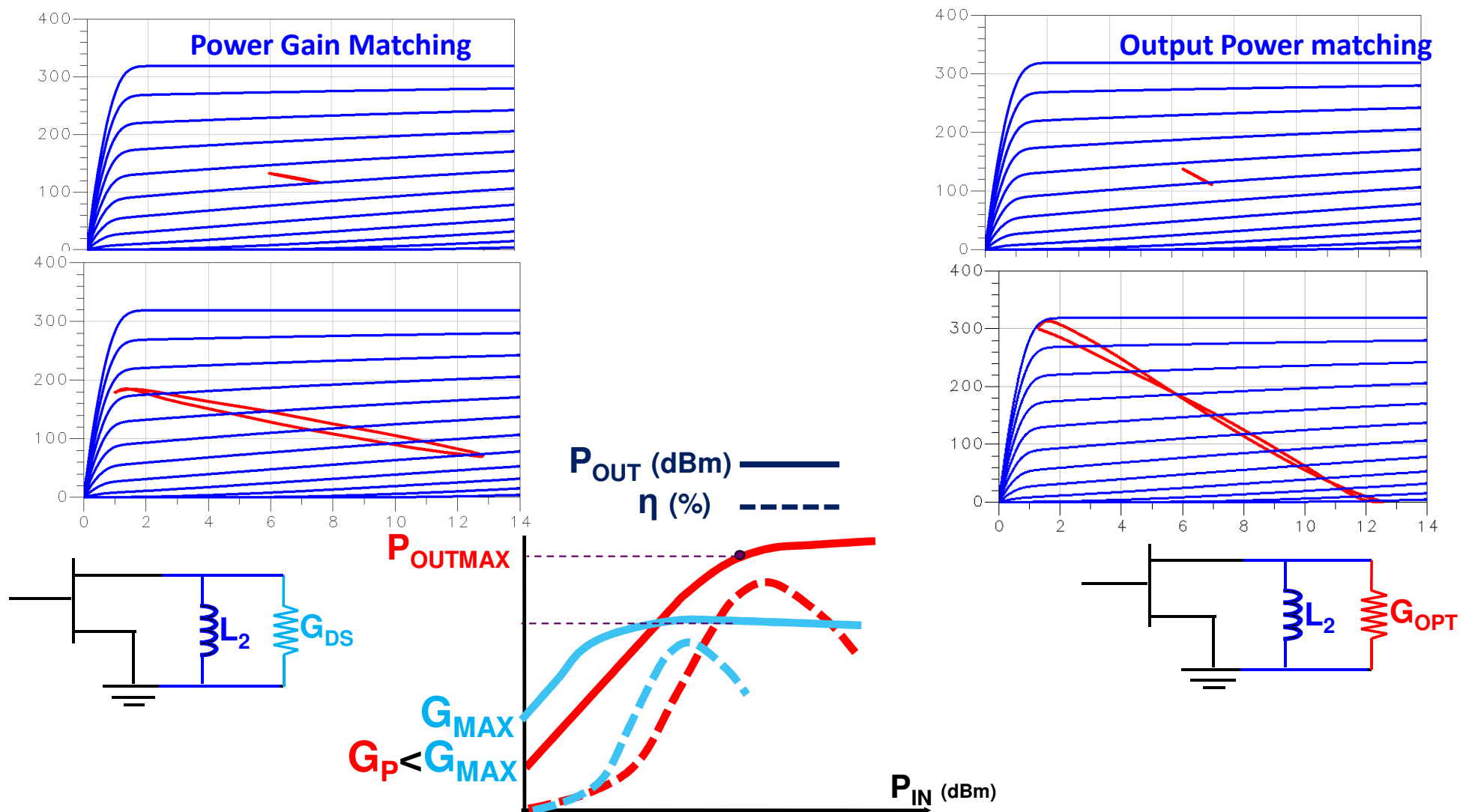
Optimum case ($G_2 = g_{DS}$) → Not maximum Power Gain G_{max}

$$G_{max} = \frac{g_m^2}{4 g_{DS} R_i C_{GS}^2 \omega^2}$$



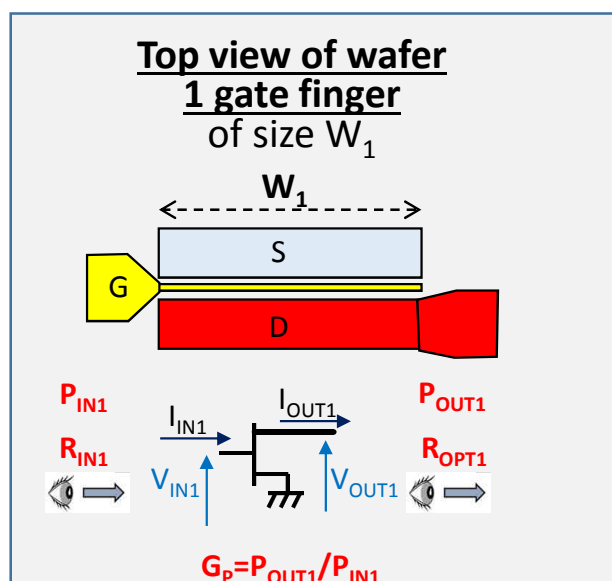






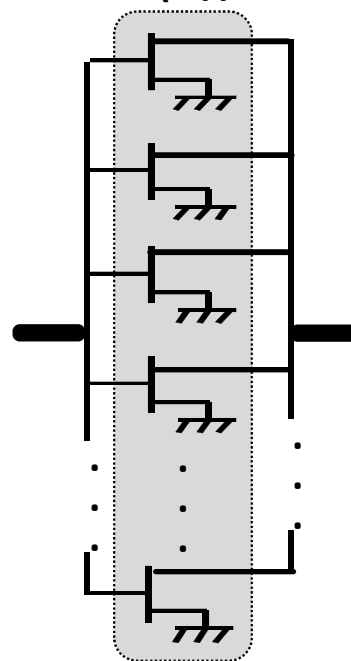
Power combination (Power Bars) and power matching

Illustration of critical issues in power matching

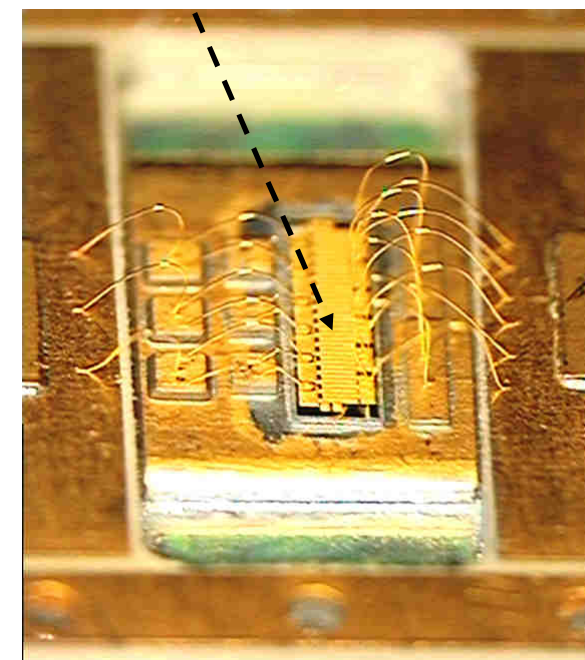


Increase device size
to increase power

Power bar (n // devices)

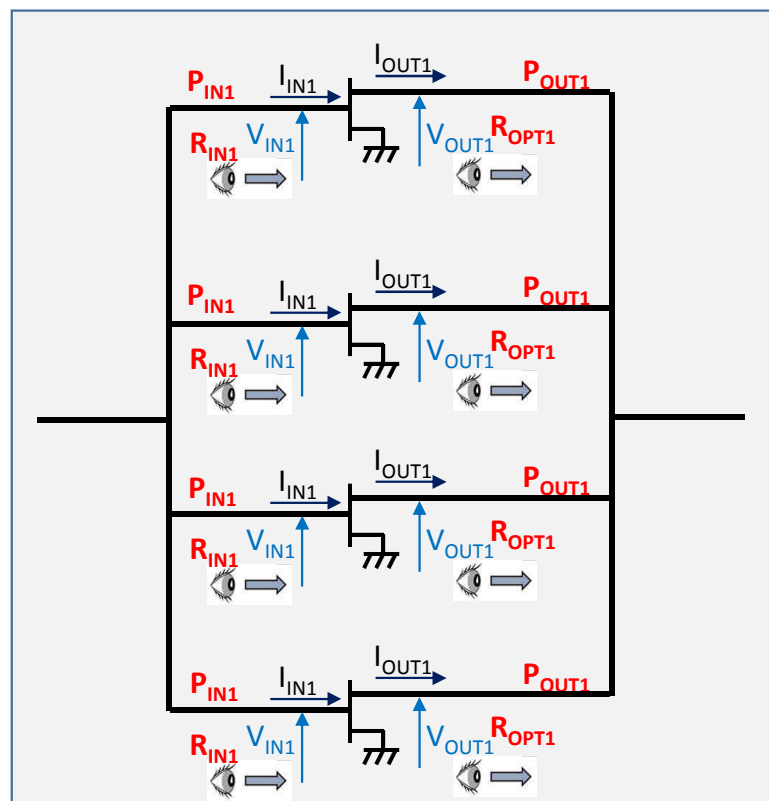
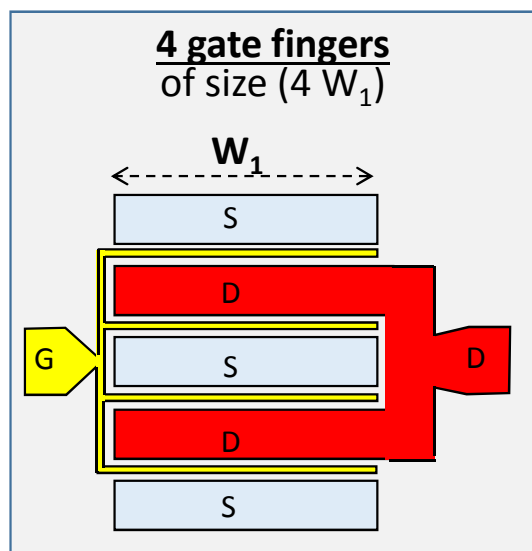


Power bar (matching in package)



Power combination (Power Bars) and power matching

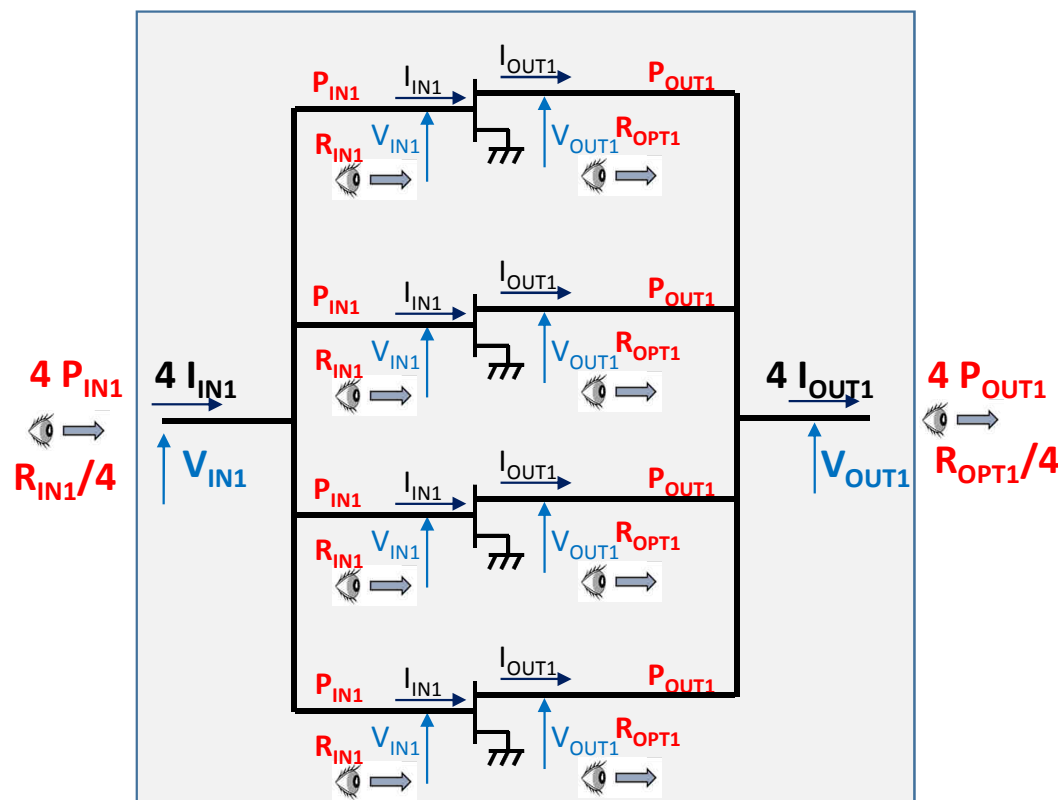
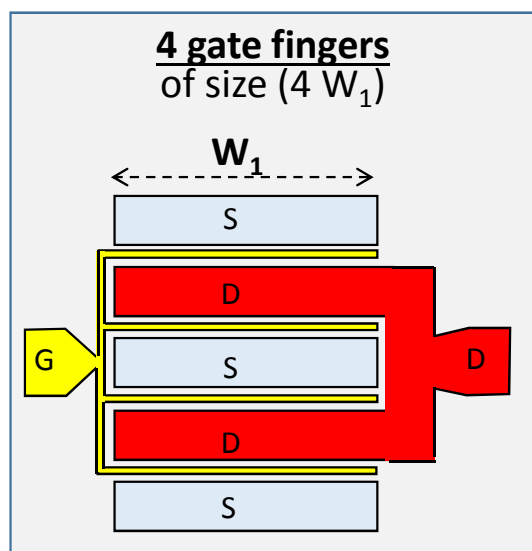
■ Illustration of critical issues in power matching



Device size = Total gate width = (N° of // gates) \times (gate width) = **4 \times W_1**

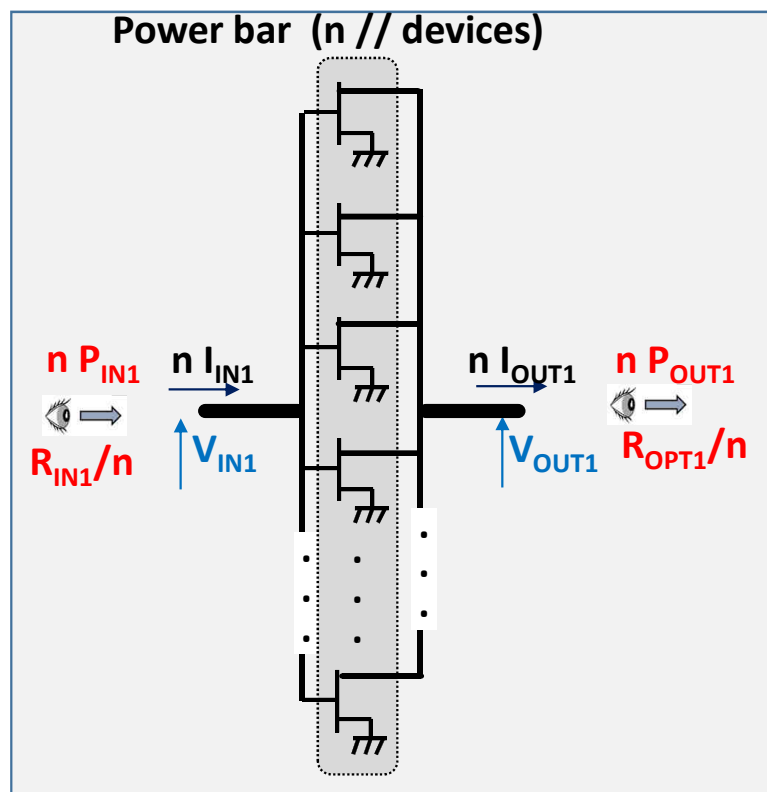
Power combination (Power Bars) and power matching

■ Illustration of critical issues in power matching

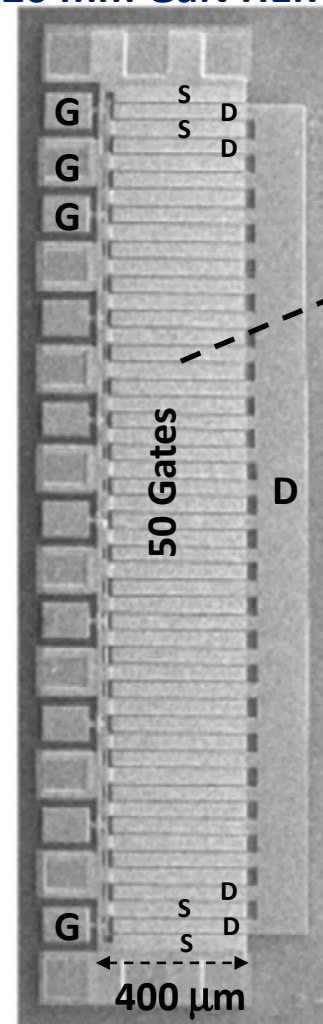


Power combination (Power Bars) and power matching

■ Illustration of critical issues in power matching



20 mm GaN HEMT die



■ Device Size

$$\begin{aligned}
 &= \text{Total Gate Width} \\
 &= (\text{N}^\circ \text{ of // gates}) \times (\text{Gate width}) \\
 &= 50 \times 400 \mu\text{m} = \mathbf{20 \text{ mm}}
 \end{aligned}$$

■ Scaling Rules:

■ Drain Current
 $I_{DS} \text{ (mA/mm)}$

■ Voltages
 $V_{GS} \text{ and } V_{DS} \text{ (V)}$

■ Output Power
 $P_{OUT} \text{ (W/mm)}$

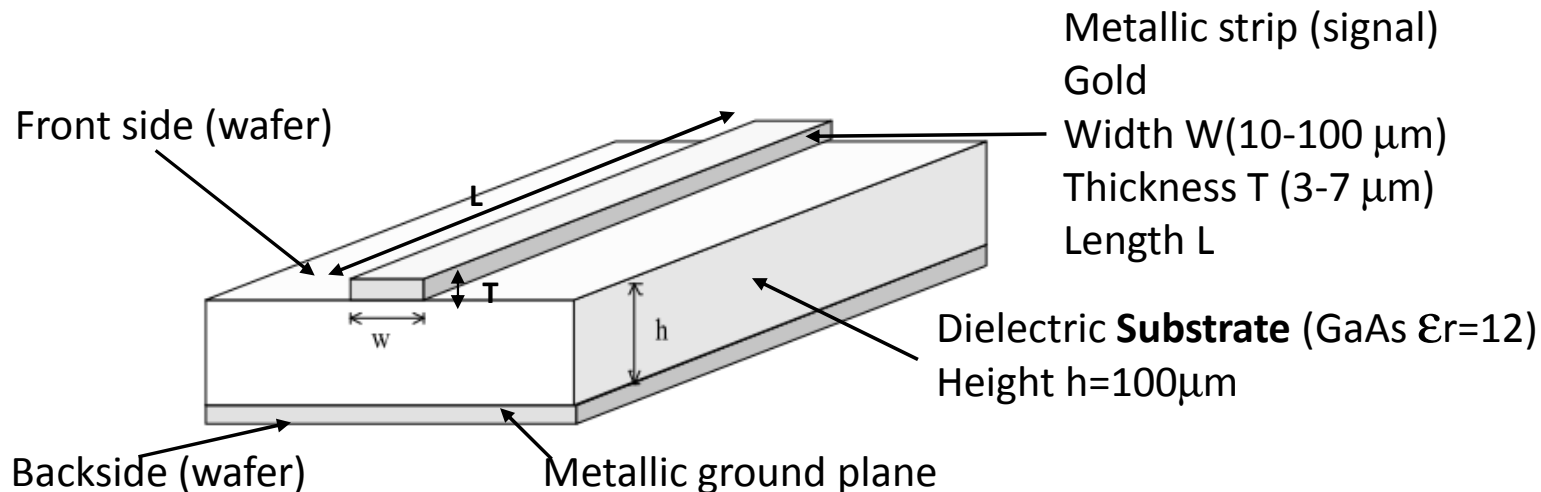
■ Optimum Output Load
 $R_{OPT} \text{ (}\Omega \cdot \text{mm)}$

Main transmission lines and Passive elements used in MMIC designs

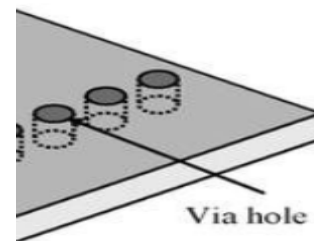
MMIC (Monolithic Microwave and Millimeterwave Integrated Technology)

- Recall on Transmission lines
- Microstrip inductors/capacitors/resistors
- Harmonic loading and bias using $\lambda/4$ lines
- Matrix chain of a line and impedance transformation

Microstrip lines

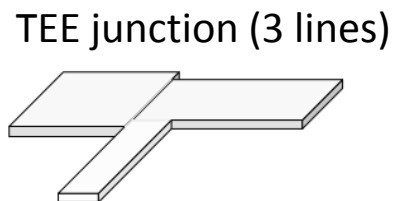
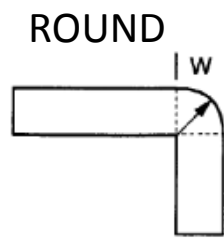
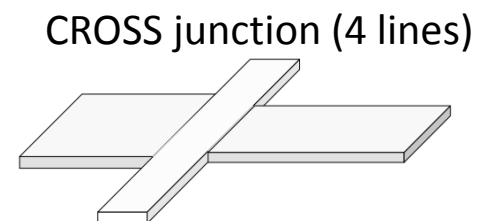
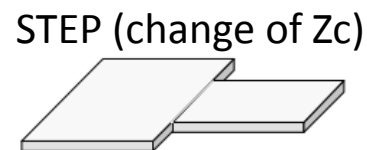
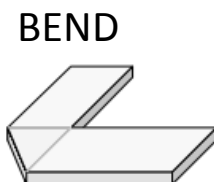
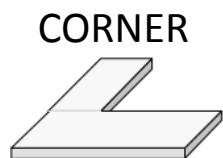


- ❑ Requirement of **metallized via holes** through the substrate to connect electrical elements from the front side to the metallic ground plane
 - expensive backside process after the front side process 😞
 - easier design of the signal paths on the front side when compared to coplanar
 - the most effective integrated technology at high frequencies 😊

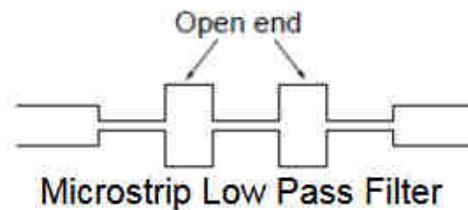


Microstrip lines

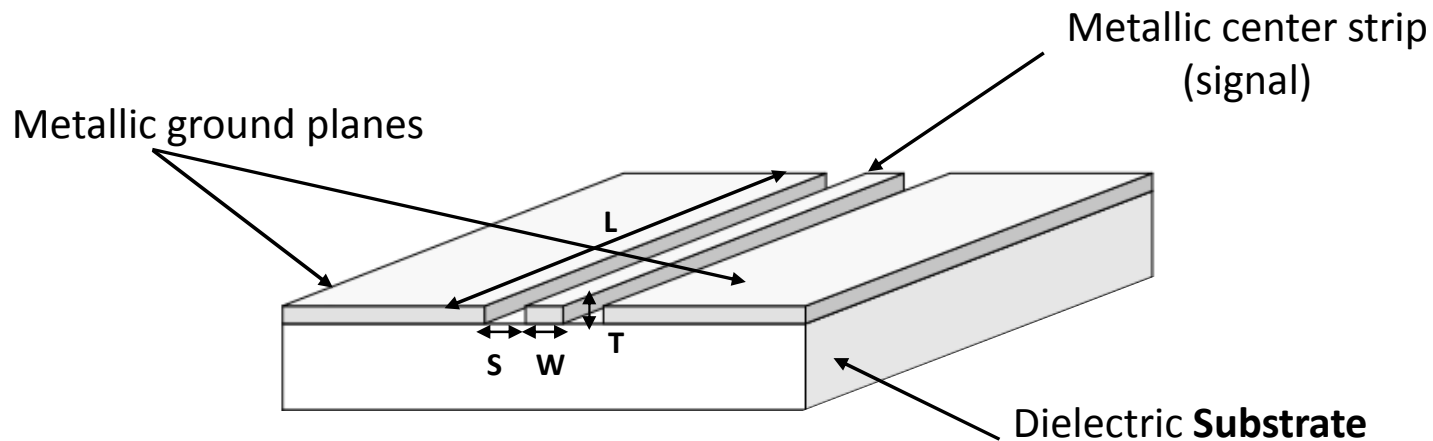
In order to drive the signal, these are some of the main shapes of line connections



In order to design passive circuits → Narrow Lines (Inductive) Wide Lines (Capacitive)



Coplanar lines



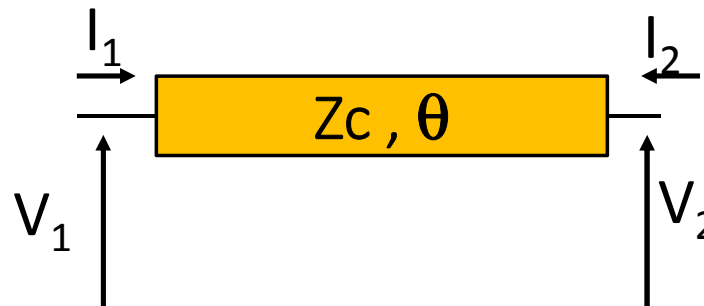
- ❑ No requirement of metallized via holes through the substrate to connect electrical elements from the front side to the metallic ground plane
 - no expensive backside process after the front side process 😊
 - complex design of the signal paths on the front side 😞
 - lower performances than microstrip designs 😞

Line = Matrix chain

Propagation constant $\Gamma = \alpha + j\beta \rightarrow$ Attenuation constant α and Phase constant β

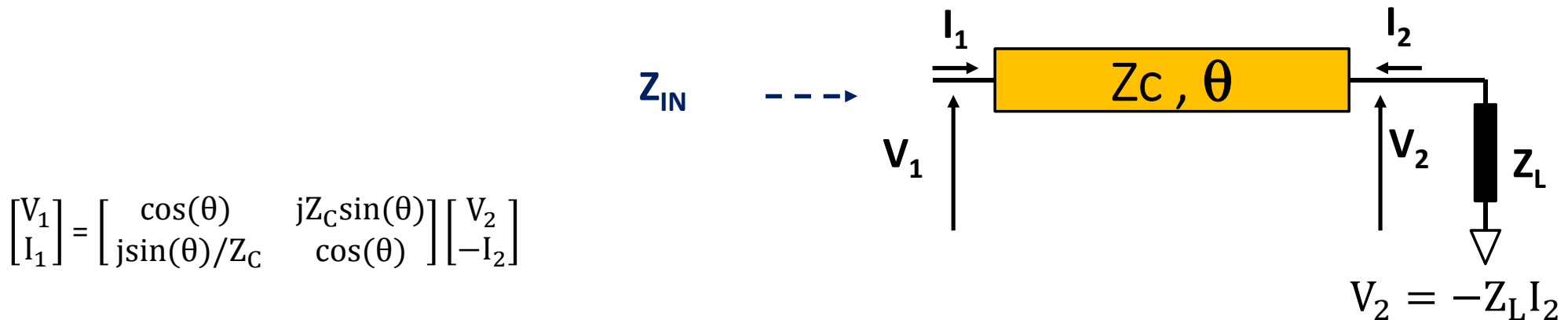
$$\beta = 2\pi/\lambda$$

$$\theta = \beta L$$



$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_c \sin(\theta) \\ j\sin(\theta)/Z_c & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

Equivalent input impedance of a loaded line

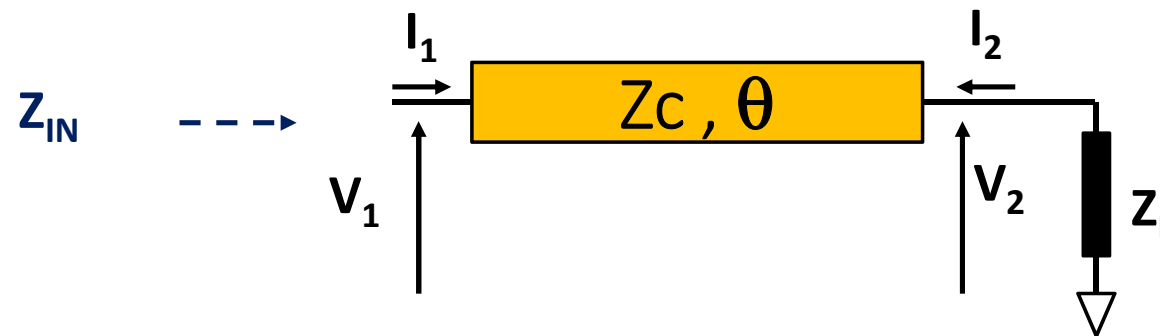


$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_C \sin(\theta) \\ j\sin(\theta)/Z_C & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

$$Z_{IN} = \frac{V_1}{I_1} = \frac{\cos(\theta) V_2 - jZ_C \sin(\theta) I_2}{\left(\frac{j\sin(\theta)}{Z_C}\right) V_2 - \cos(\theta) I_2} = \frac{\cos(\theta) (-Z_L I_2) - jZ_C \sin(\theta) I_2}{\left(\frac{j\sin(\theta)}{Z_C}\right) (-Z_L I_2) - \cos(\theta) I_2}$$

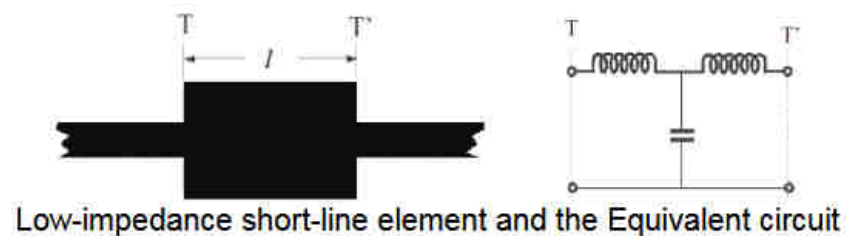
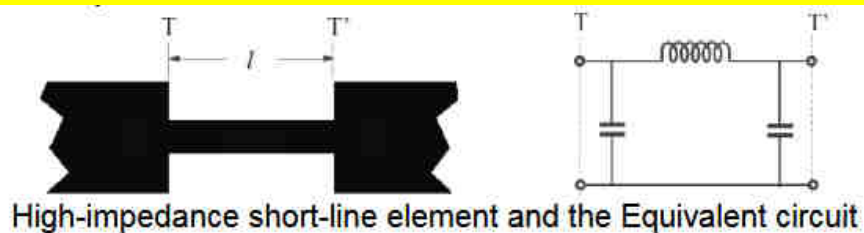
$$Z_{IN} = \frac{\cos(\theta) (Z_L) + jZ_C \sin(\theta)}{\left(\frac{j\sin(\theta)}{Z_C}\right) (Z_L) + \cos(\theta)} = Z_C \frac{Z_L \cos(\theta) + jZ_C \sin(\theta)}{jZ_L \sin(\theta) + Z_C \cos(\theta)}$$

Equivalent input impedance of $\lambda/4$ and $\lambda/2$ loaded lines

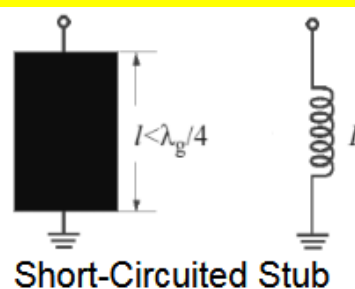
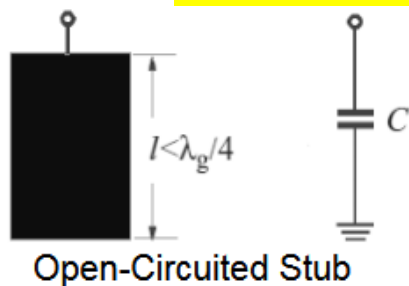


$$Z_{IN} = Z_C \frac{Z_L \cos(\theta) + jZ_C \sin(\theta)}{jZ_L \sin(\theta) + Z_C \cos(\theta)} \begin{cases} \text{if } L = \frac{\lambda}{4} \rightarrow \theta = \frac{2\pi L}{\lambda} = \frac{\pi}{2} \rightarrow Z_{IN} = \frac{Z_C^2}{Z_L} \text{ Impedance inverter} \\ \text{if } L = \frac{\lambda}{2} \rightarrow \theta = \frac{2\pi L}{\lambda} = \pi \rightarrow Z_{IN} = Z_L \end{cases}$$

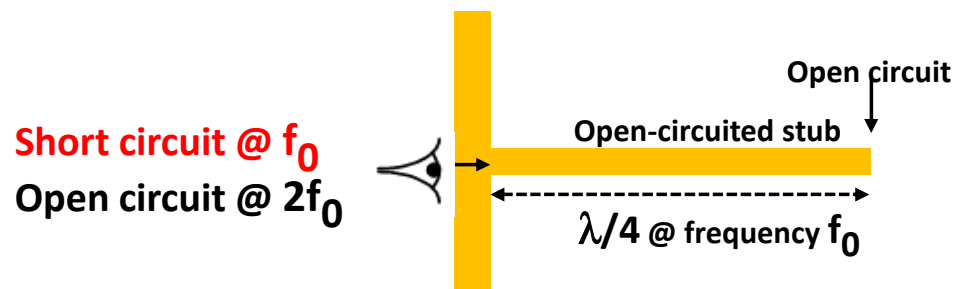
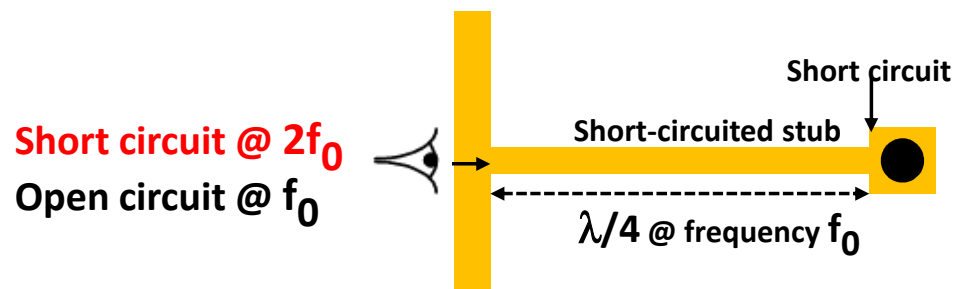
High- and Low-impedance short lines (Inductive or capacitive)



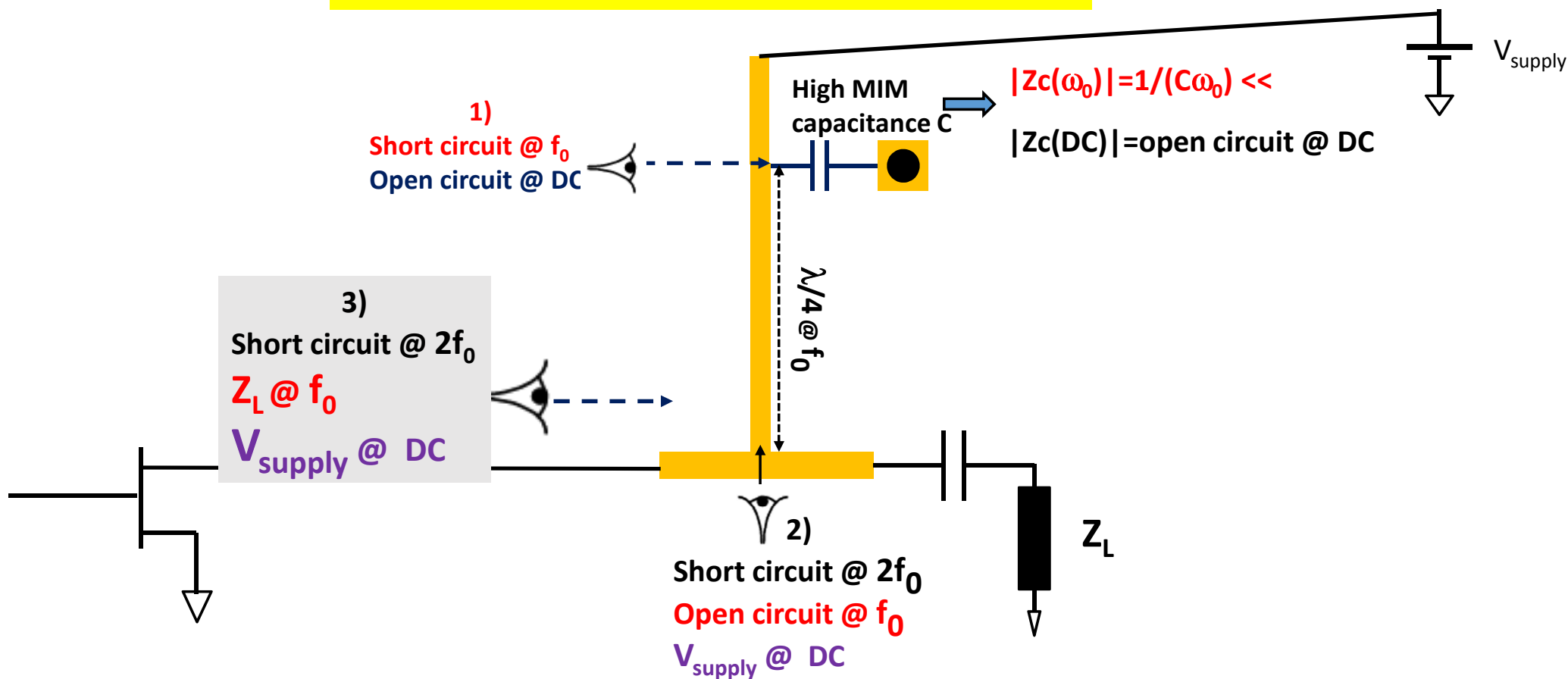
Open and short-circuited stubs



Narrowband Harmonic loading using quarter wavelength line ($\lambda/4$)



Bias network decoupling using quarter wavelength line ($\lambda/4$)

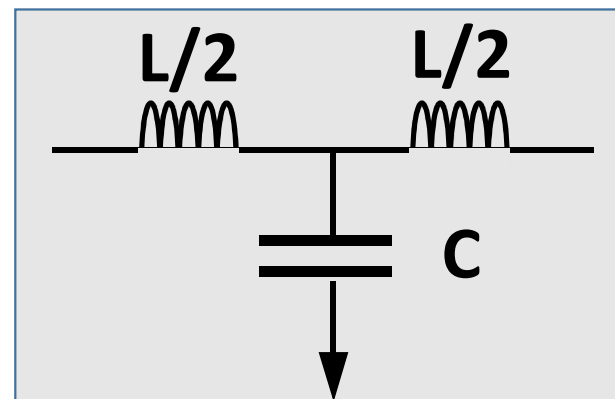


**Reminder = Electrical lumped equivalent (RLC)
of transmission lines**

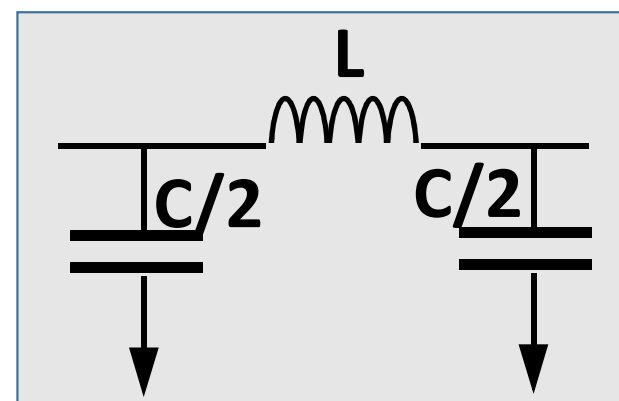
Electrical lumped equivalent (LC) of a lossless line (Z_c, θ)



T cell



π cell

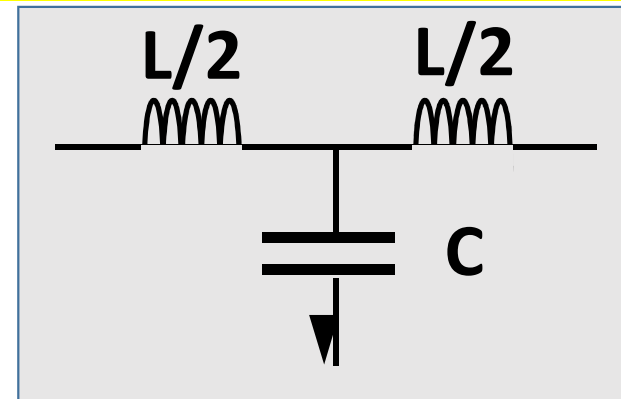


Electrical lumped equivalent (LC) of a lossless line (Z_c , θ)

Cut-off frequency

$$f_c = \frac{1}{\pi\sqrt{LC}}$$

T cell



Characteristic Impedance

$$Z_c = \sqrt{\frac{L}{C}} \sqrt{1 - \left[\frac{f}{f_c}\right]^2}$$

Phase Shift

$$\theta = \omega\sqrt{LC} \sqrt{1 - \left[\frac{f}{f_c}\right]^2}$$

$$\sqrt{1 - \left[\frac{f}{f_c}\right]^2} > 0.9 \Leftrightarrow f < 0.44 f_c$$

Electrical lumped equivalent (LC) of a lossless line (Z_c, θ)



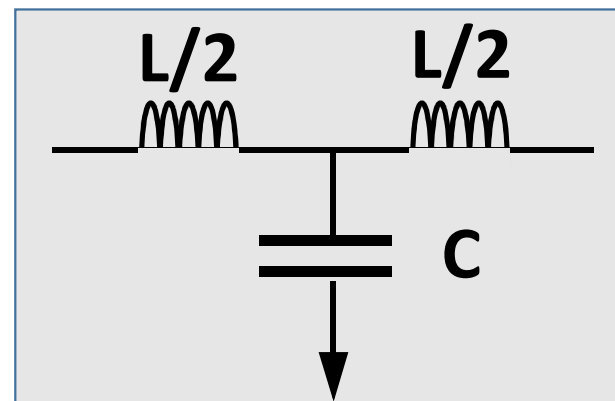
Cut-off frequency

$$f_c = \frac{1}{\pi\sqrt{LC}}$$

Characteristic Impedance

If $f \ll f_c \rightarrow Z_c \approx \sqrt{\frac{L}{C}}$
 $f < 0.44 f_c$

T cell

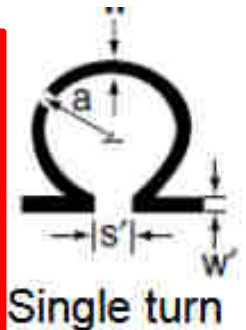
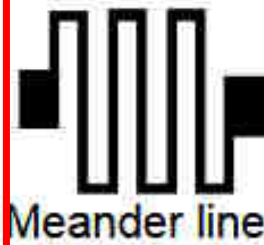
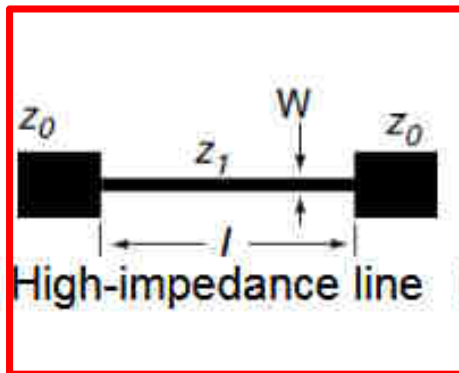


Phase Shift

If $f \ll f_c \rightarrow \theta \approx \omega\sqrt{LC}$

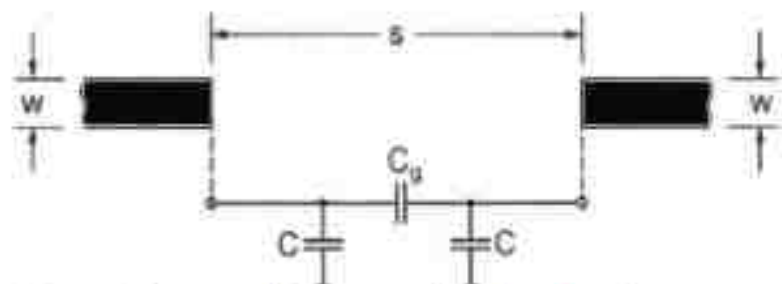
Microstrip passive inductors, capacitors and resistors

Microstrip Inductors

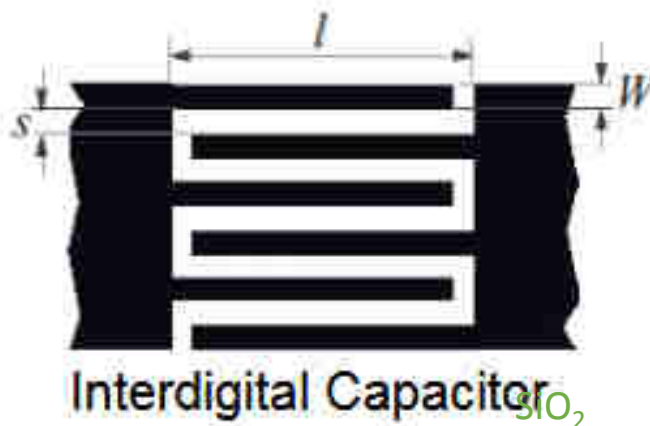


Only used at lower frequencies up to 3-4GHz because of very high losses
Achievable values up to few nH

Microstrip Capacitors (MIM : Metal Insulator Metal)



Gap Capacitor and Equivalency



Interdigital Capacitor



$$C = \epsilon \frac{S}{d} = \epsilon \frac{l \times W}{d}$$

$$C = \frac{\epsilon}{d} (l \times W)$$

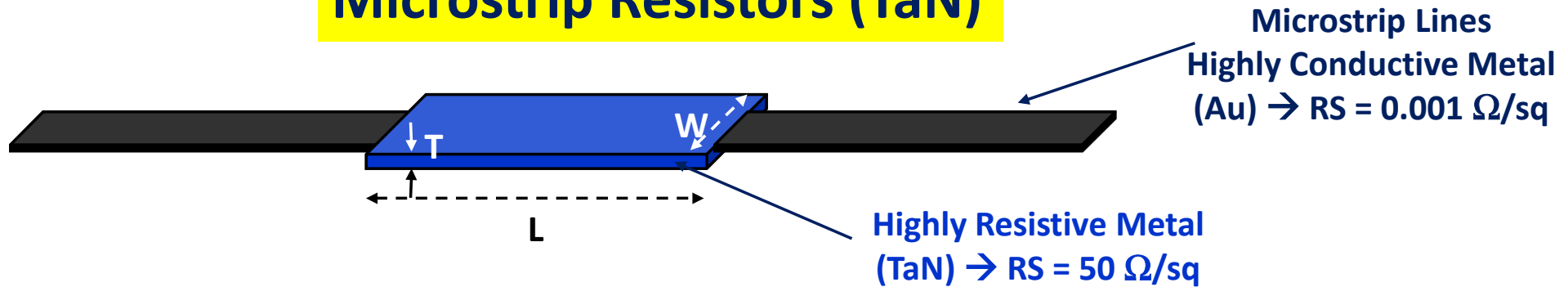
$$C = CD \times S$$

$$CD = \frac{\epsilon}{d}$$

Capacitance density (F/m²)

Ex : 300 pF/mm² → Achievable values 0.2pF → 20pF

Microstrip Resistors (TaN)



$$R = \rho_{\text{TaN}} \frac{L}{S} = \rho_{\text{TaN}} \frac{L}{T \times W}$$

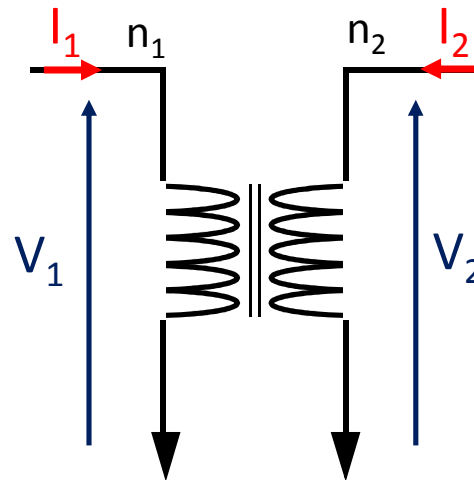
$$R = \frac{\rho_{\text{TaN}}}{T} \frac{L}{W} = R_S \frac{L}{W}$$

$$R_S = \frac{\rho_{\text{TaN}}}{T}$$

Sheet resistance R_S (Ω/sq)
($\Omega/$)

$$R = R_S \frac{L}{W}$$

Reminder = Ideal Electrical transformers
How are they realized at high frequencies ?



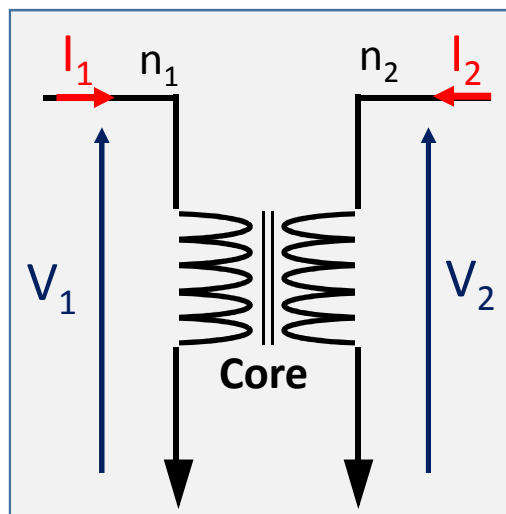
Reminder = Ideal Electrical transformer

$$\frac{V_2}{V_1} = \frac{n_2}{n_1}$$

$$\frac{I_2}{I_1} = -\frac{n_1}{n_2}$$

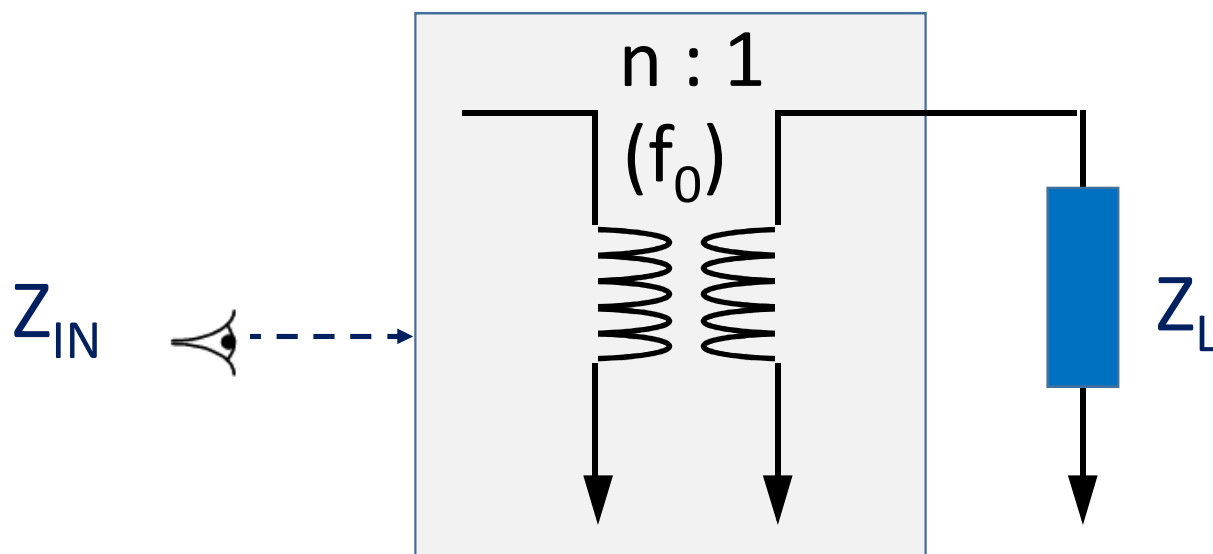
Conservation of energy

Primary Winding
(n_1 turns)



Secondary Winding
(n_2 turns)

Reminder = Impedance transformation



Criterion

- Transformation ratio
- Bandwidth
- Technology

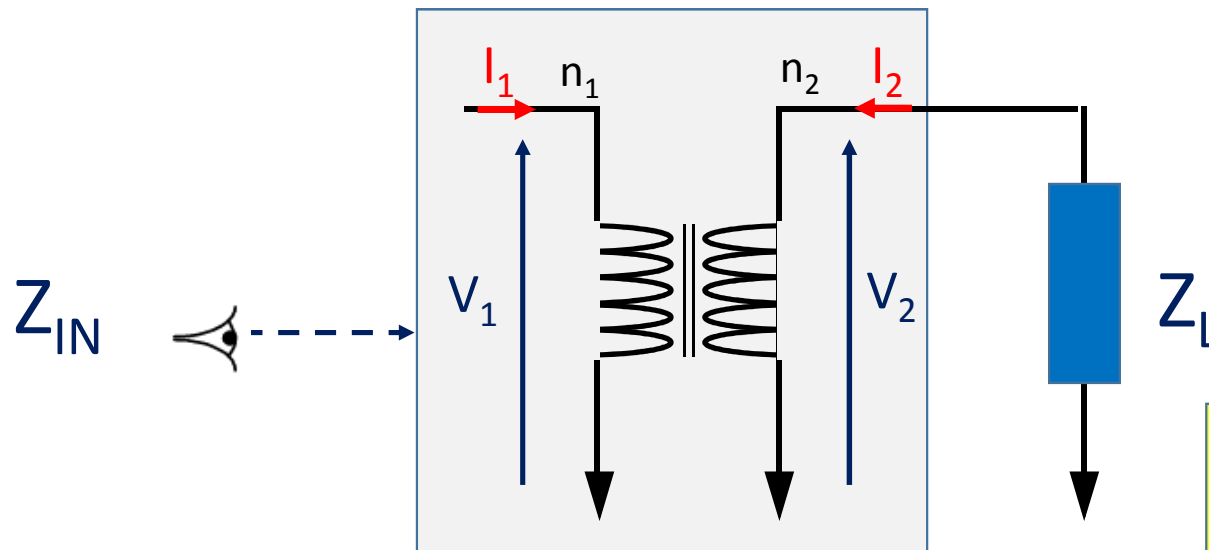
$$Z_{IN} = n^2 Z_L$$

$$n = \sqrt{\frac{Z_{IN}}{Z_L}}$$

Reminder = Impedance transformation

$$\frac{V_2}{V_1} = \frac{n_2}{n_1}$$

$$\frac{I_2}{I_1} = -\frac{n_1}{n_2}$$



Load

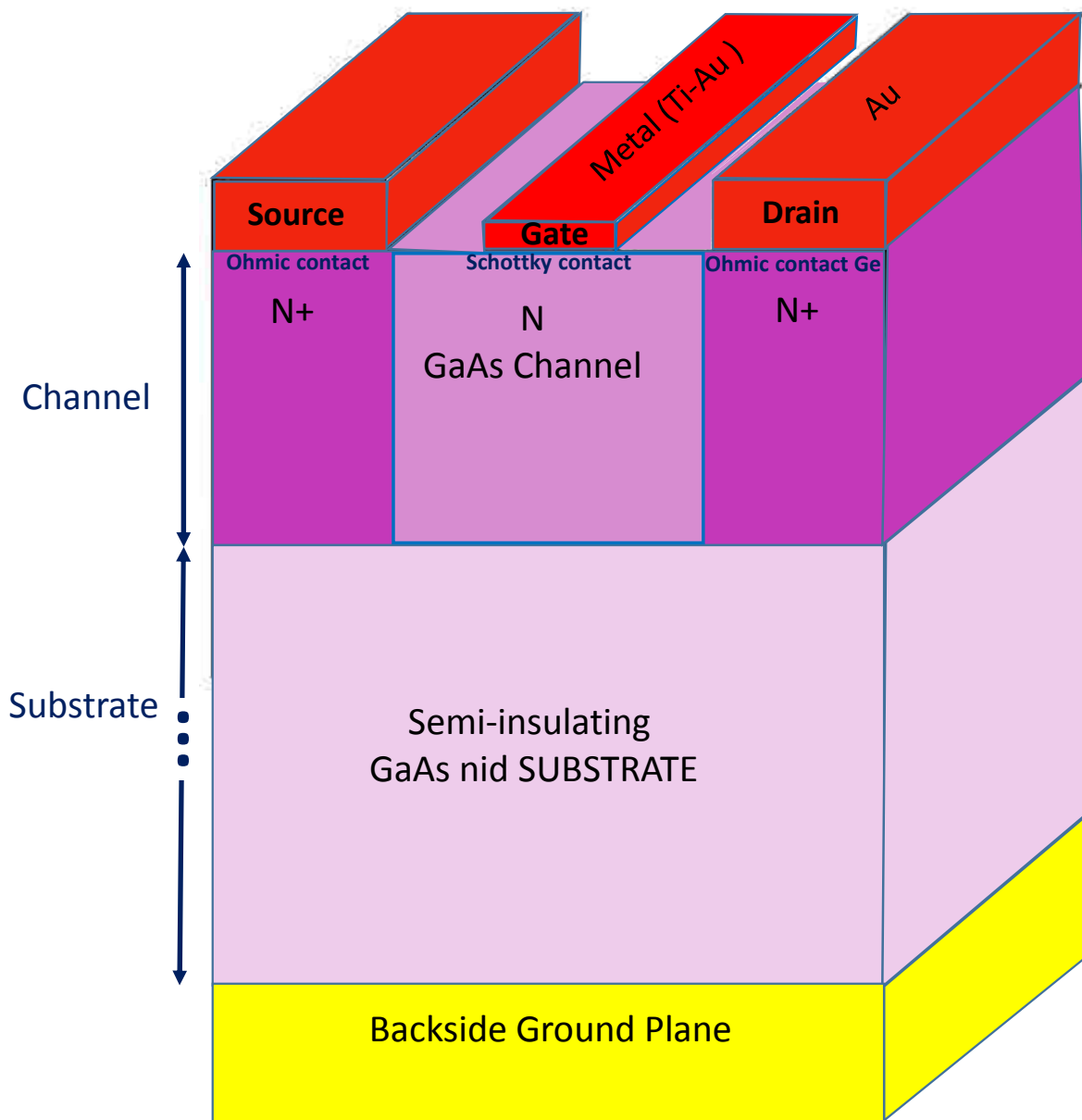
$$V_2 = -Z_L I_2$$

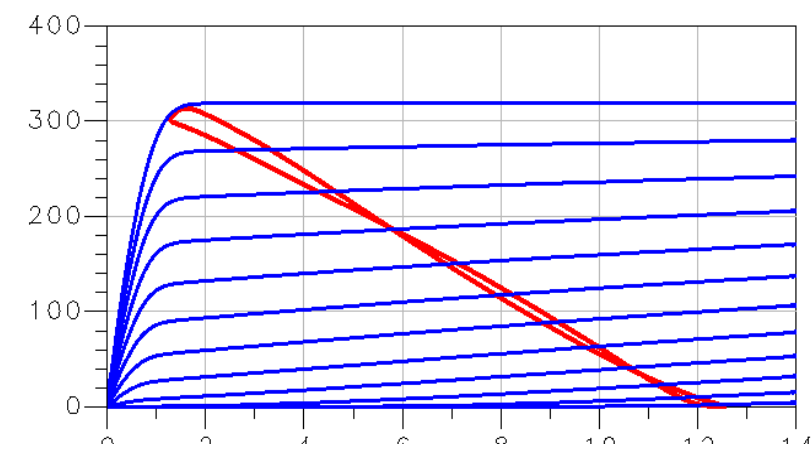
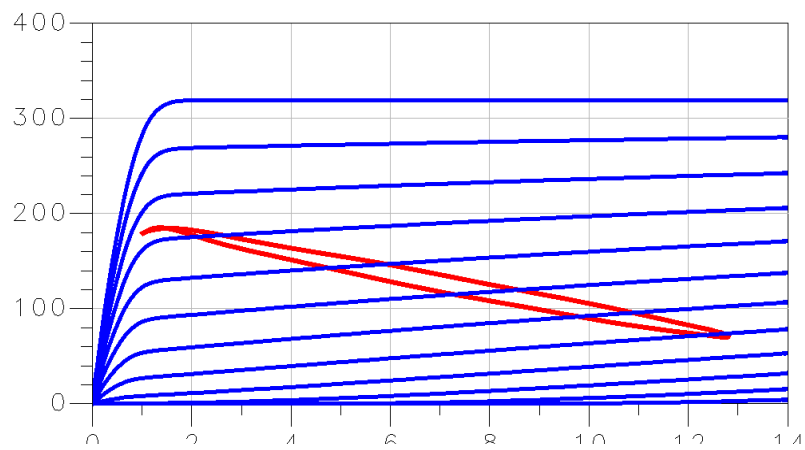
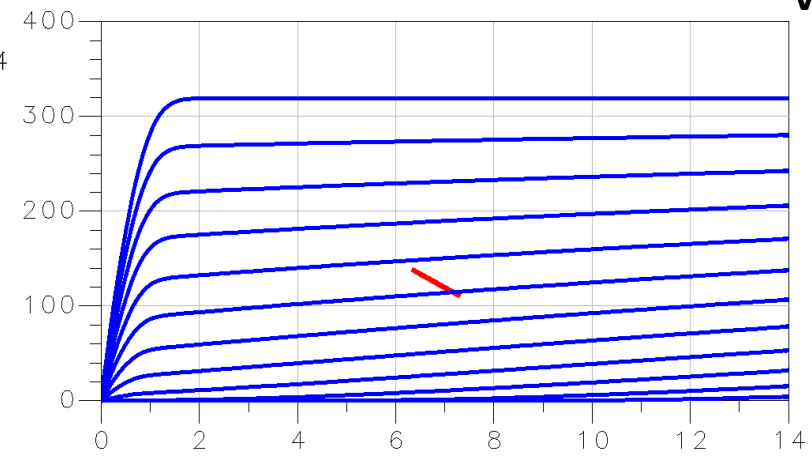
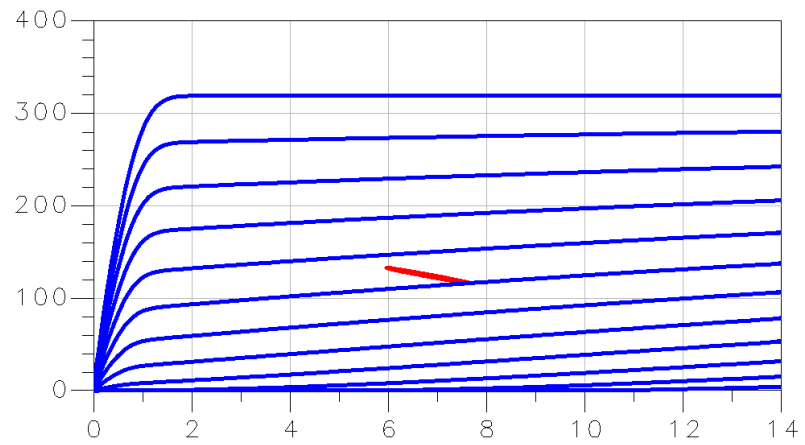
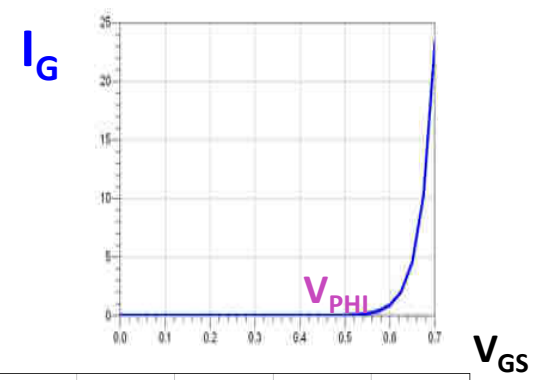
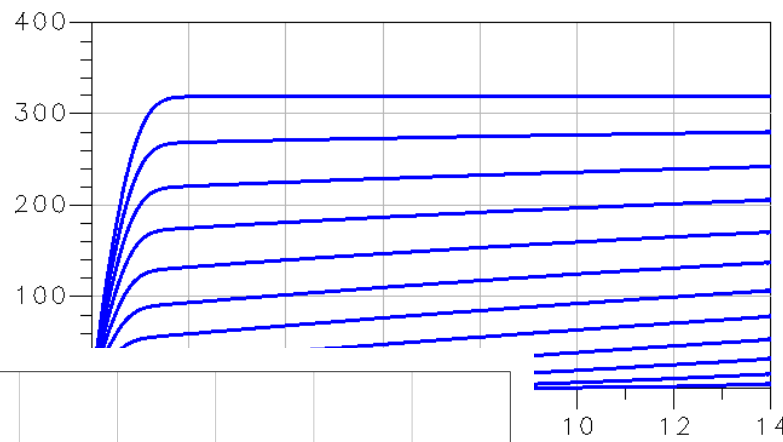
$$Z_{IN} = \frac{V_1}{I_1} = \frac{V_1}{V_2} \frac{V_2}{I_2} \frac{I_2}{I_1} = \frac{n_1}{n_2} (-Z_L) \frac{-n_1}{n_2} = \left[\frac{n_1}{n_2} \right]^2 Z_L$$

$$Z_{IN} = \left[\frac{n_1}{n_2} \right]^2 Z_L$$

$$n = \left[\frac{n_1}{n_2} \right]_{cv} = \sqrt{\frac{Z_{IN}}{Z_L}}$$

Additional Slides





I – Basics of HEMT operation → Same Electrical Circuit Model

