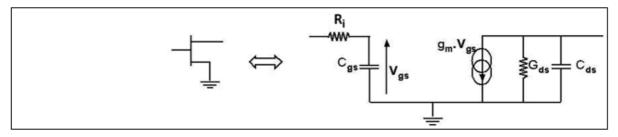
# E(rasmus) Mundus on Innovative Microwave Electronics and Optics Master



# **Basics of Active and Nonlinear HF Electronics – Tutorial 2**

# A) Power gain matching of a single-stage narrow-band amplifier

This figure represents the simplified electrical model of an FET.



The model parameters are given at a bias point of ( $V_{GS0} = -2 \text{ V}$  and  $V_{DS0} = 20 \text{ V}$ )

Ri = 
$$5\,\Omega$$
 ;  $C_{GS}$  =  $0.5\,pF$  ;  $g_m$  =  $100\,ms$  ;  $R_{DS}$  =  $200\,\Omega$  ;  $C_{DS}$  =  $0.15\,pF$ 

The amplifier environment is :  $R_G = 50 \Omega$  ;  $R_L = 50 \Omega$  ;  $f_0 = 10 \text{ GHz}$ 

- 1) Determine the expression of G<sub>MAX</sub>: maximum power gain of the transistor as a function of frequency
- 2) We consider the design of a linear amplifier, which is loaded by a resistor R<sub>L</sub>, while the input generator has an internal resistor R<sub>G</sub>.
  - a) Draw the ideal input and output matching circuits of a narrow-band amplifier which is matched to its maximum power gain  $G_{MAX}$  at  $f_0$ .
  - b) Determine the expressions of each passive matching elements as a function of  $f_0$ , the model parameters and the  $R_G$  and  $R_L$  resistors.
- 3) Determine the expressions of the input and output quality factors, Q<sub>IN</sub> and Q<sub>OUT</sub>, respectively.



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## B) Power gain matching of a two stage narrow-band amplifier

### Main pecifications of the narrow-band amplifier:

Output Power  $P_{OUT} > 1 \text{ W}$ ; Center frequency  $f_0 = 15 \text{ GHz}$ ; Power Gain  $G_P > 15 \text{ dB}$ 

#### Selected MMIC foundry (0.15 μm GaAs HEMT) :

Power Density PD = 1 W/mm ; Measured Gain G<sub>MAX(@10GHz)</sub> = 16 dB ;

Saturated Drain Current IDSS = 800 mA/mm; Drain Voltage range (VDSmin=1V and VDSmax=11V)

Pinch-off Voltage: VP = -4 V

Optimum load impedance  $R_{OPT} = 12.5 \Omega.mm$ 

<u>Small-signal model:</u>  $C_{GS} = 2.7 \text{ pF/mm}$ ; Ri =1  $\Omega$ .mm;  $g_m = 200 \text{ mS/mm}$ ;

 $R_{DS} = 125 \Omega.mm$ ;  $C_{DS} = 0.6 pF/mm$ 

Selected device size @ 15 GHz = 4x75 μm GaAs HEMT

- 1) Given the required specifications and the selected transistor technology, determine the initial sizing of the power amplifier (number of stages, number of amplifying cells per stage, power gain and input/output powers of each stage) using the selected device size ( $4x75 \mu m$ ) as the unitary amplifying cell.
- 2) Given that only the last stage should be matched to its optimum output power while all the preceding stages should be matched to their maximum power gain, draw the input and output matching circuits of this two-stage narrow-band amplifier and calculate the values of each matching elements.
- 3) Calculate the input and output quality factors of each stage to assess what will be the bandwidth behavior.
- 4) Can you comment on the power limitations and the power added efficiency of this two-stage amplifier?