Faculté des Sciences & Techniques — Université de Limoges — EMIMEO Erasmus Mundus

1st session – December 11, 2020

Master 1 EMIMEO - Exam of "Basics of active and nonlinear electronics" (M. Campovecchio)

A- Narrow-band power amplifier (2 stages)

Specifications:

Output Power $\mathbf{P_{OUT}}$ > 2 W ; Center frequency $\mathbf{f_0}$ = 20 GHz ;
Total power gain $\mathbf{G_P}$ > 20 dB ; Source and Load resistors $\mathbf{R_G = R_L}$ = R_{50} = 50 Ω

MMIC technology (0.25 µm GaAs HEMT foundry**) :**

Power density **PD =** 1 W/mm ; Measured maximum gain @ 20 GHz $\mathbf{G_{MAX(@20GHz)}}$ = 16 dB ≈ 40 ;
Maximum drain current $\mathbf{I_{DSmax}}$ = 800 mA/mm; Limits of V_{DS} voltage ($\mathbf{V_{DSmin}}$=1 V and $\mathbf{V_{DSmax}}$=11 V)
Optimum power resistance: $\mathbf{R_{OPT}}$ = 12,5 Ω.mm
Linear electrical model : $\mathbf{C_{GS}}$ = 2,7 pF/mm ; $\mathbf{C_{DS}}$ = 0,6 pF/mm ; **Ri =** 1 Ω.mm ; $\mathbf{R_{DS}}$ = 125 Ω.mm
Selected transistor (unitary size **T1 of 0.6mm**) @ 20 GHz = **8x75 µm** GaAs HEMT

In the problem ($\mathbf{C_{GS1}}$; $\mathbf{C_{DS1}}$; $\mathbf{Ri_1}$; $\mathbf{R_{IN1}}$; $\mathbf{R_{DS1}}$; $\mathbf{R_{OPT1}}$) stand for the values of transistor **T1** = 8x75µm = **0.6 mm**

In this problem, **each stage has to be matched to its optimum power load** $\mathbf{R_{OPT_A}}$ **and** $\mathbf{R_{OPT_B}}$

1) Using scaling rules, calculate the numerical values ($\mathbf{C_{GS1}}$; $\mathbf{C_{DS1}}$; $\mathbf{Ri_1}$; $\mathbf{R_{DS1}}$; $\mathbf{R_{OPT1}}$; $\mathbf{R_{IN1}}$ @ 20GHz) of T1.

2) Power gain :

- $\mathbf{G_P(R_{OPT})}$ is the power gain of a transistor T when it is loaded by its optimum power load ($\mathbf{L_{OPT}//R_{OPT}}$).
- $\mathbf{G_{MAX}}$= $\mathbf{G_P(R_{DS})}$ is the maximum power gain of T when it is loaded by its optimum gain load ($\mathbf{L_{OPT}//R_{DS}}$).

In both cases, $L_{OPT}=1/(C_{DS}\,\omega^2)$.

It can be demonstrated that the power gain $G_P(R_{OPT})$ can be expressed as a function of G_{MAX} by:

$$\mathbf{G_P(R_{OPT})} = R_{OPT}\left[\frac{R_{DS}}{R_{DS}+R_{OPT}}\right]^2 \frac{g_m^2}{R_i\, C_{GS}^2\, \omega^2} = \mathbf{4\, R_{OPT}} \frac{\mathbf{R_{DS}}}{[\mathbf{R_{DS}}+\mathbf{R_{OPT}}]^2}\, \mathbf{G_{MAX}}$$

Using this equation and the measured value of $\mathbf{G_{MAX(@20GHz)}}$=16dB=40, determine the expression of $G_{P1}(R_{OPT1})$ for the transistor T1 when it is matched to its optimum power load R_{OPT1}. Demonstrate that the numerical value of G_{P1} at 20GHz is $\mathbf{G_{P1(@20GHz)}}$ =13,2=11,2dB.

3) Using the specifications of output power and the technological data of power density, determine the sizing of the 2-stage amplifier (**size** of each stage with numbers $\mathbf{n_B}$ and $\mathbf{n_A}$ of transistors T1 per stage / optimum load resistance required by each stage $\mathbf{R_{L_B}}$ and $\mathbf{R_{L_A}}$ as a function of R_{OPT1} / output power $\mathbf{P_{OUT}}$ of 2nd stage/ gain of 2nd stage $\mathbf{G_{P_B}= G_{P_1}}$/ inter-stage power $\mathbf{P_{IN_B}=P_{OUT_A}}$ / gain of 1st stage $\mathbf{G_{P_A}= G_{P_1}}$/ input power $\mathbf{P_{IN}}$=P_{IN_A}).

4) On the amplifier schematic (next page), indicate the numerical values of each stage when the amplifier operates at the maximum output power of the last stage.

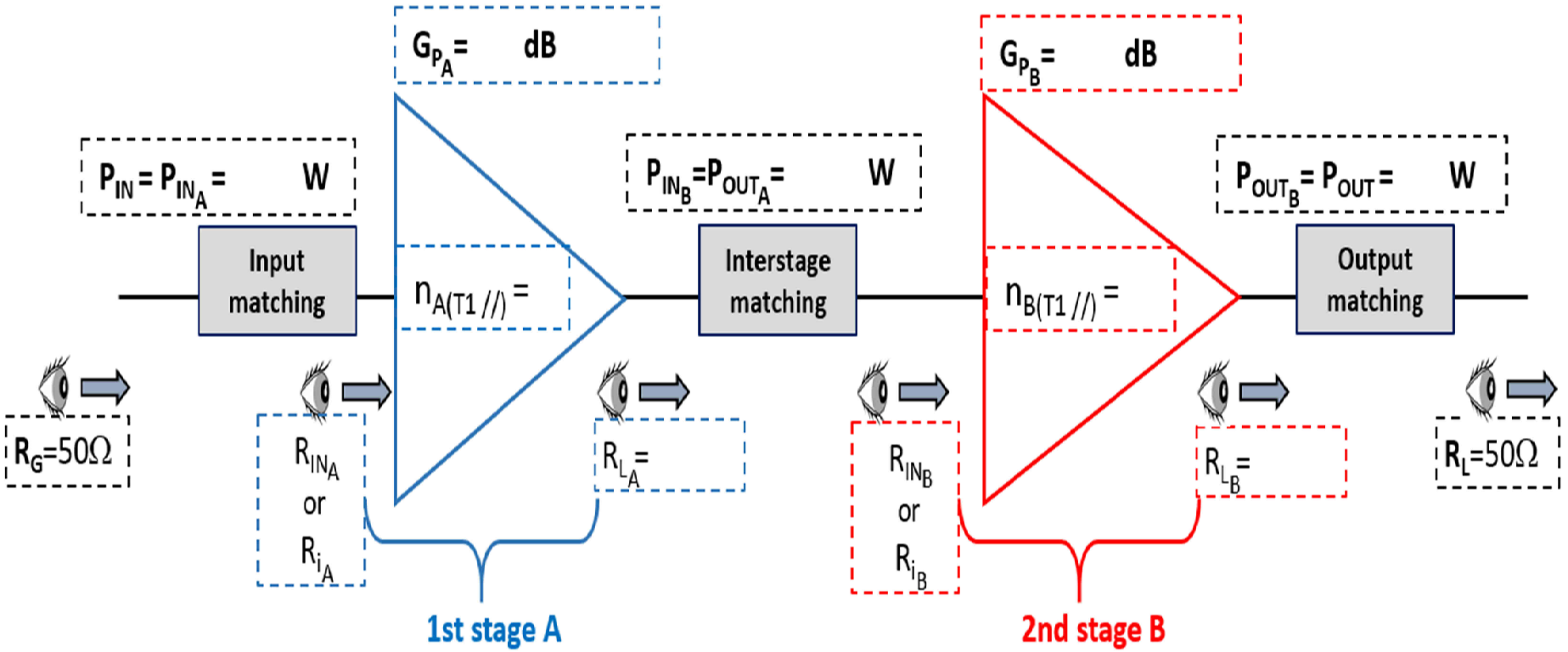
5) Input and inter-stage matching
   a) Calculate the equivalent series input resistances $\mathbf{R_{i_A}}$ and $\mathbf{R_{i_B}}$ of each stage.
   b) Calculate the equivalent parallel input resistances $\mathbf{R_{IN_A}}$ and $\mathbf{R_{IN_B}}$ of each stage at 20GHz.

6) Draw the electrical matching circuits (inductors and transformers) of the two-stage amplifier when matched to R_G=R_L=50Ω and determine the expression of matching elements **without calculating numerical values**. For the sake of simplicity, you can use the notations:

$$L_1 = 1/(C_{GS1}\,\omega_0^2) \text{ and } L_2 = 1/(C_{DS1}\,\omega_0^2)$$

7) If both stages operate in class-A, calculate the total DC power to determine the maximum PAE of the amplifier? Why is-it less than 50%?

Name:


G_{P_A} = dB
G_{P_B} = dB
$P_{IN} = P_{IN_A}$ = W
$P_{IN_B} = P_{OUT_A}$ = W
$P_{OUT_B} = P_{OUT}$ = W
Input matching
Interstage matching
Output matching
$n_{A(T1\,//)}$ =
$n_{B(T1\,//)}$ =
R_G=50Ω
R_{IN_A} or R_{i_A}
R_{L_A} =
R_{IN_B} or R_{i_B}
R_{L_B} =
R_L=50Ω
1st stage A
2nd stage B