# Basics of Active and Nonlinear High-Frequency Electronics

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# Basics of Active and Nonlinear High-Frequency Electronics

# Chapter II :

# Introduction to

# the Non-linear Electrical Modeling of microwave transistors

High-frequency Pulsed Measurement Systems

On–wafer Probing Stations

for RF/Microwave circuits

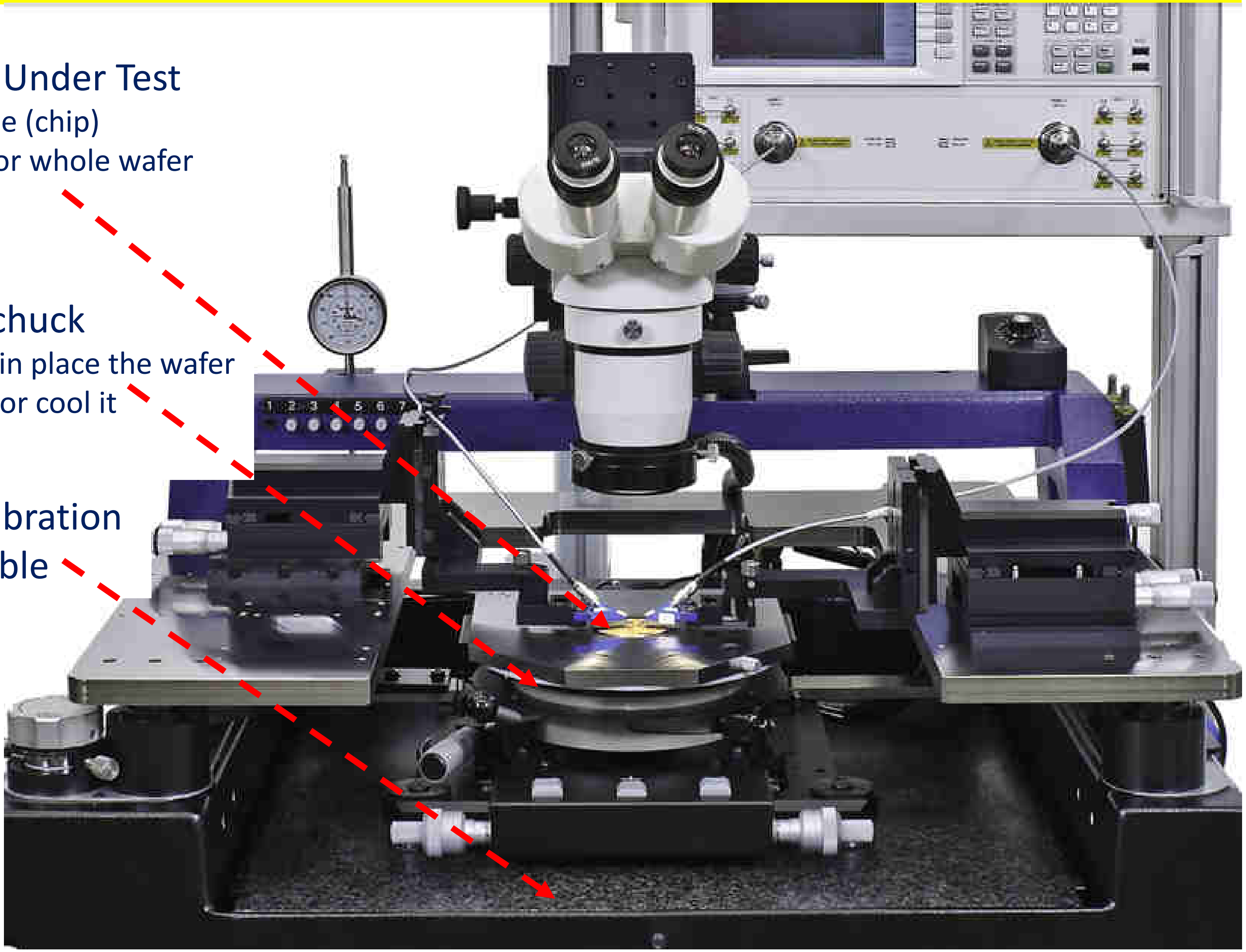
# On-wafer probing stations

# On-wafer probing stations

Device Under Test
- small die (chip)
- partial or whole wafer

Wafer chuck
- to hold in place the wafer
- to heat or cool it

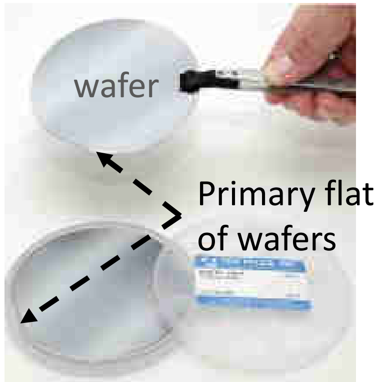
Anti- Vibration Table



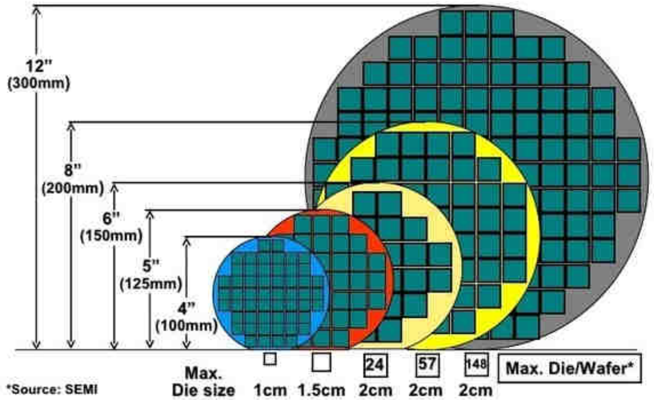
EMIMEO

E(rasmus) Mundus on Innovative Microwave Electronics and Optics

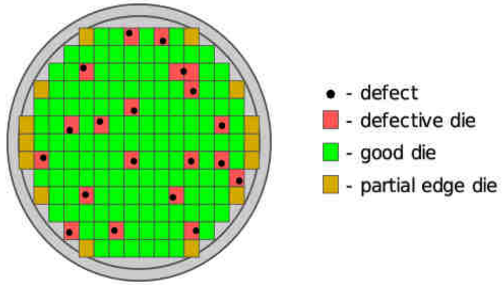
# Wafer chuck and Anti-vibration table




On-wafer size

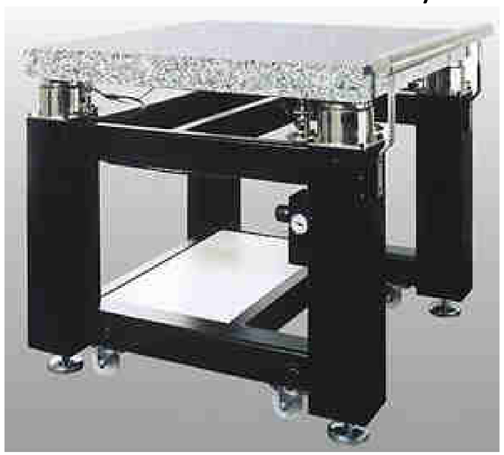



On-wafer test and sorting




Vibration Isolation Table (Marble)

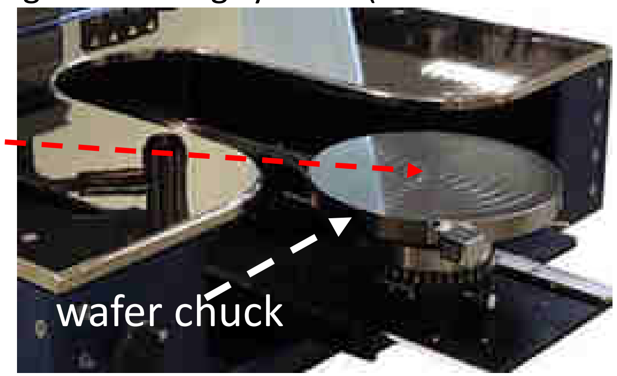
- keep high mechanical stability
- reliable sub-micron stability



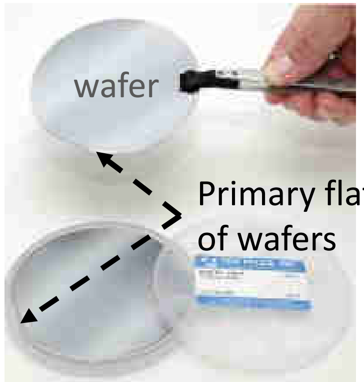
Wafer Chuck → Thermal chuck (-60°C →300°C)

Thermal enclosure

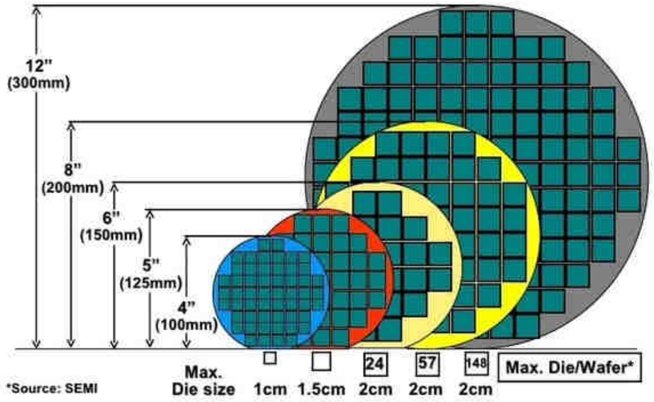
- hold wafers in place while they are being probed
- apply a small amount of vacuum to the wafer backside
- can hold small die and partial or whole wafer
- cooling and heating systems (air flow conditioning)

# Wafer composition




On-wafer size

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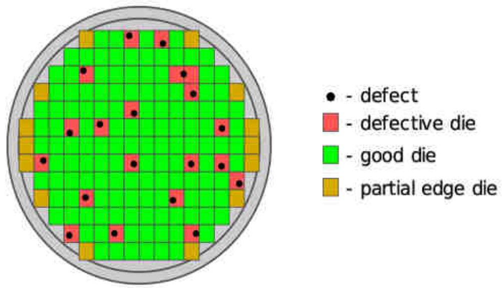
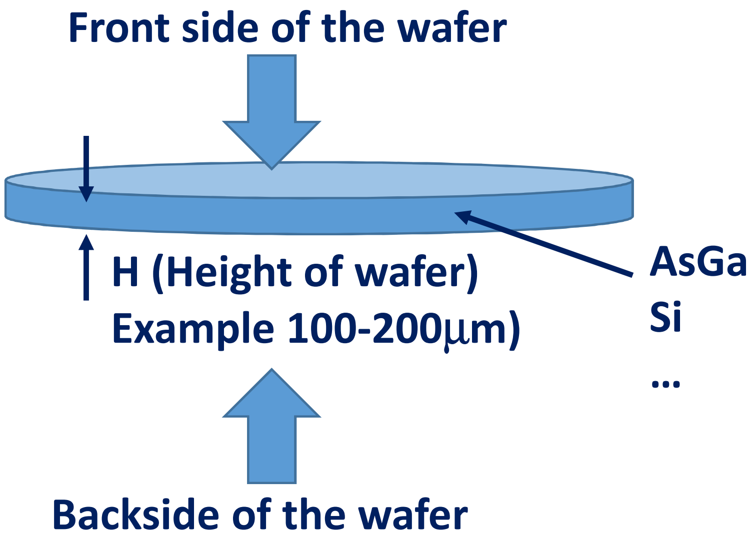
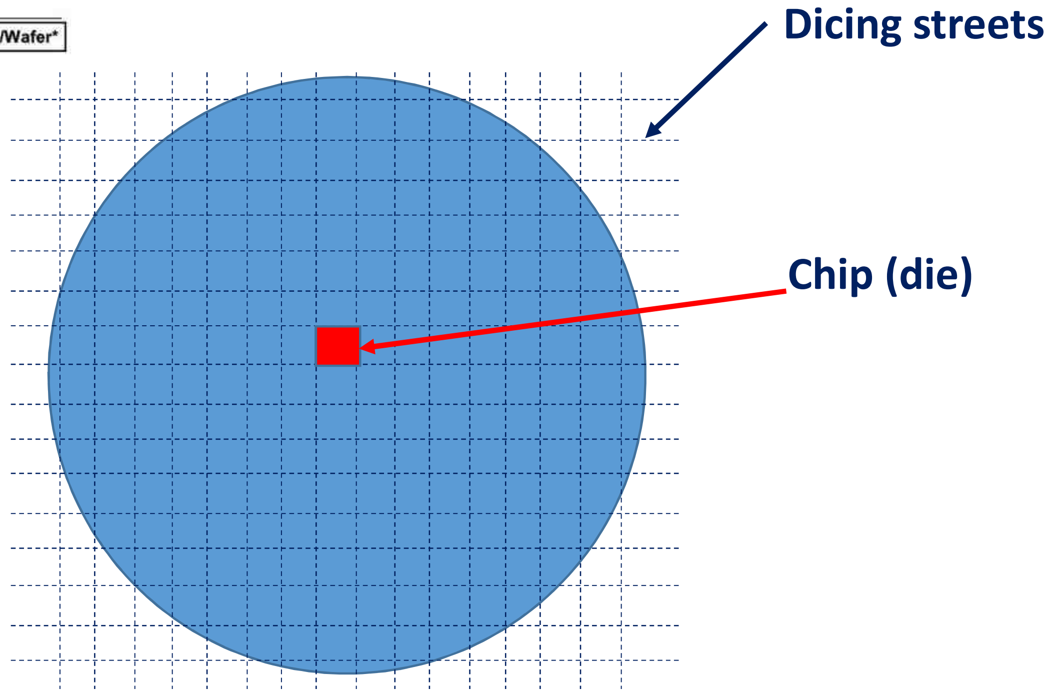
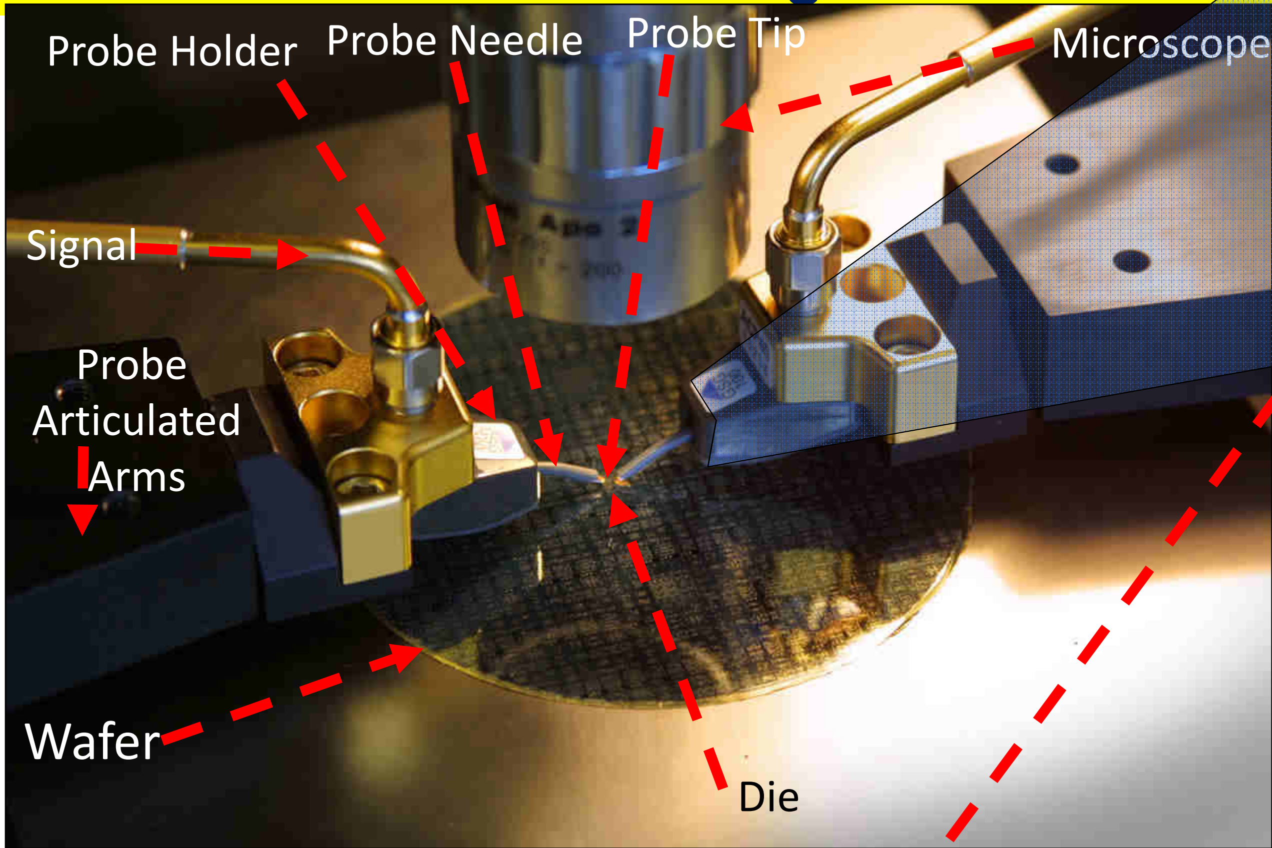


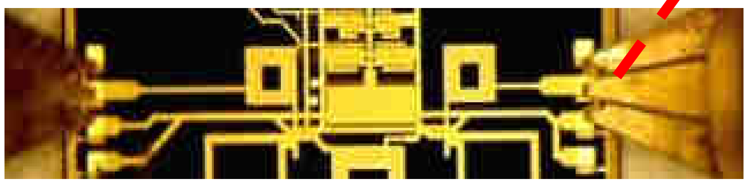



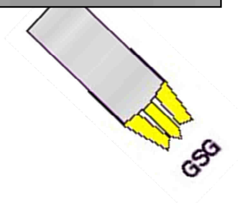
# On-Wafer Probing

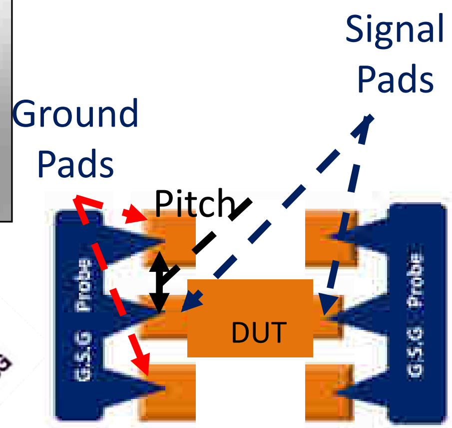



GSG
Probe Tip

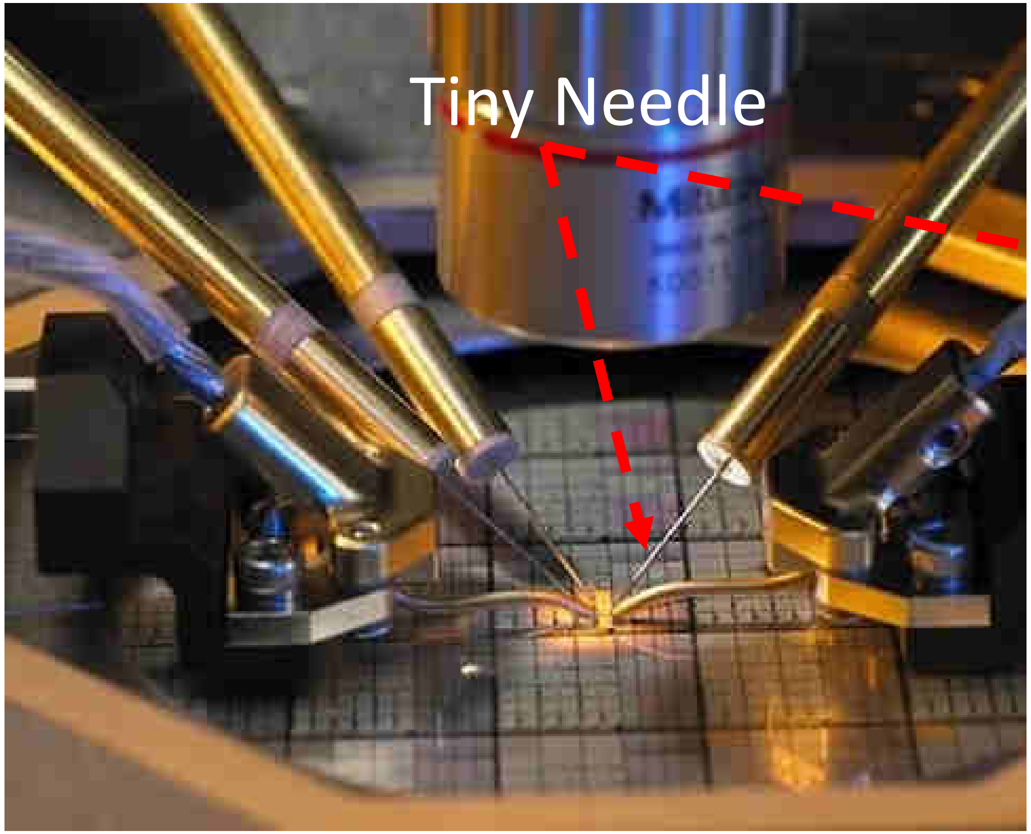
GSG is the most common type of RF probe.
Many standard pitches

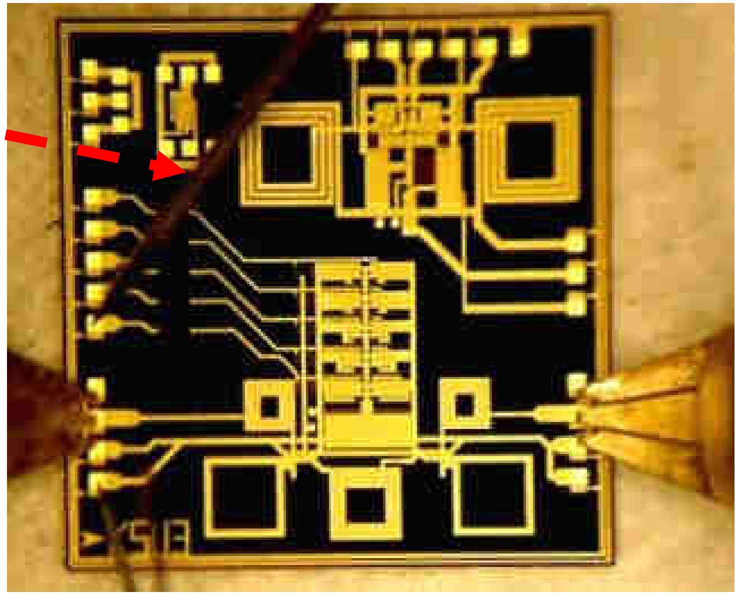




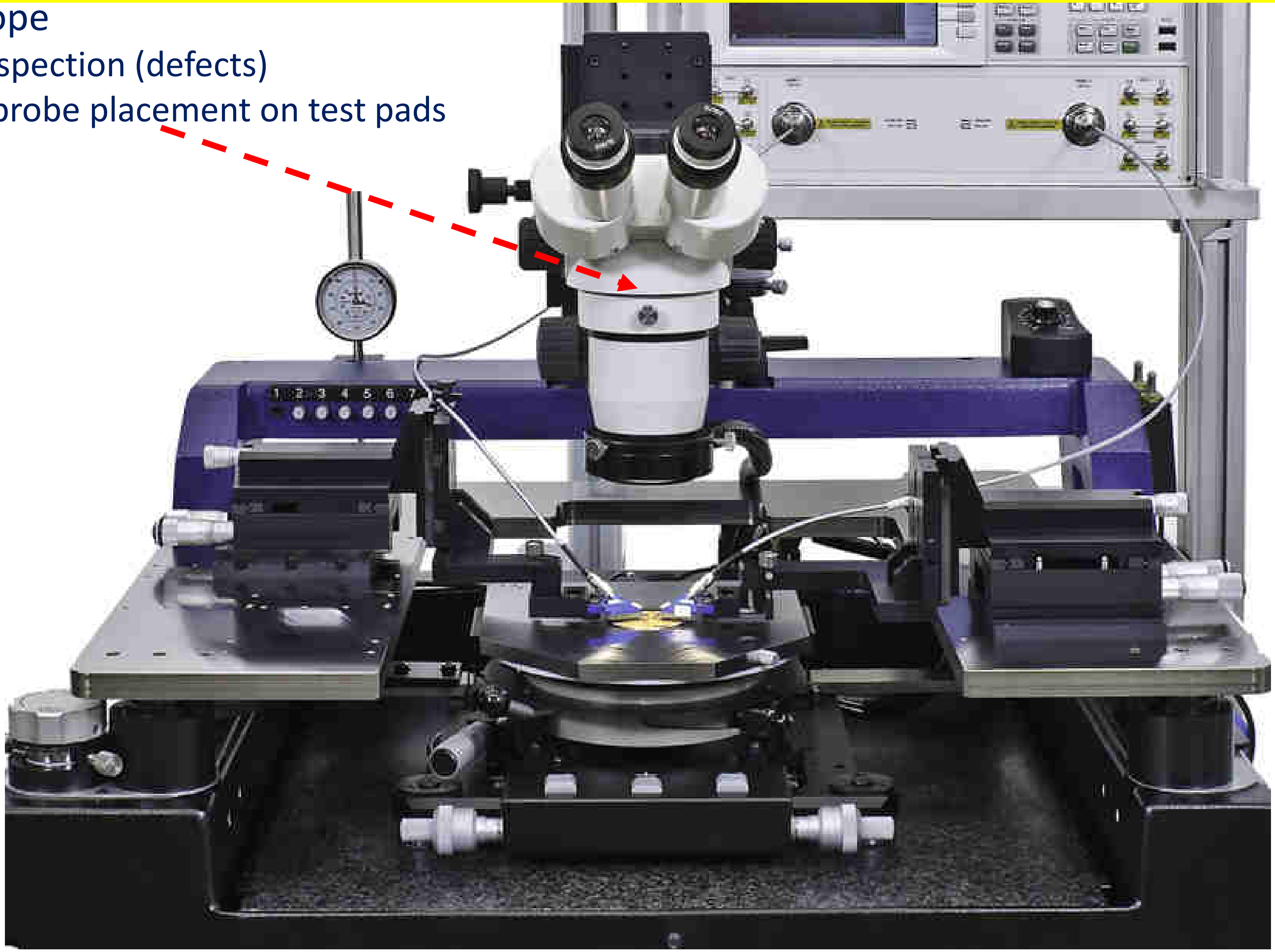
# On-Wafer Probing



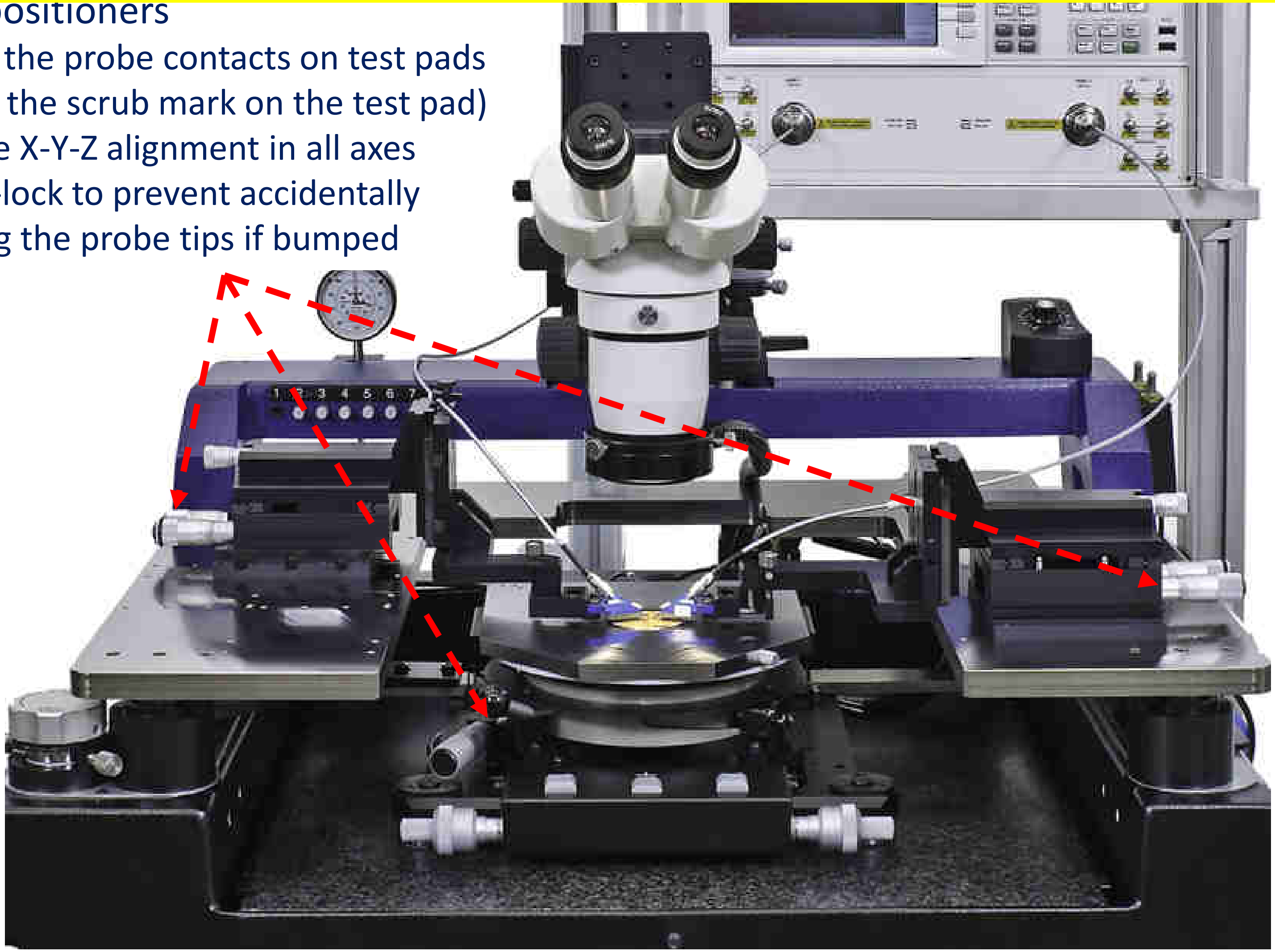
## HF probe stations   On-wafer Probing System

Microscope
- wafer inspection (defects)
- precise probe placement on test pads

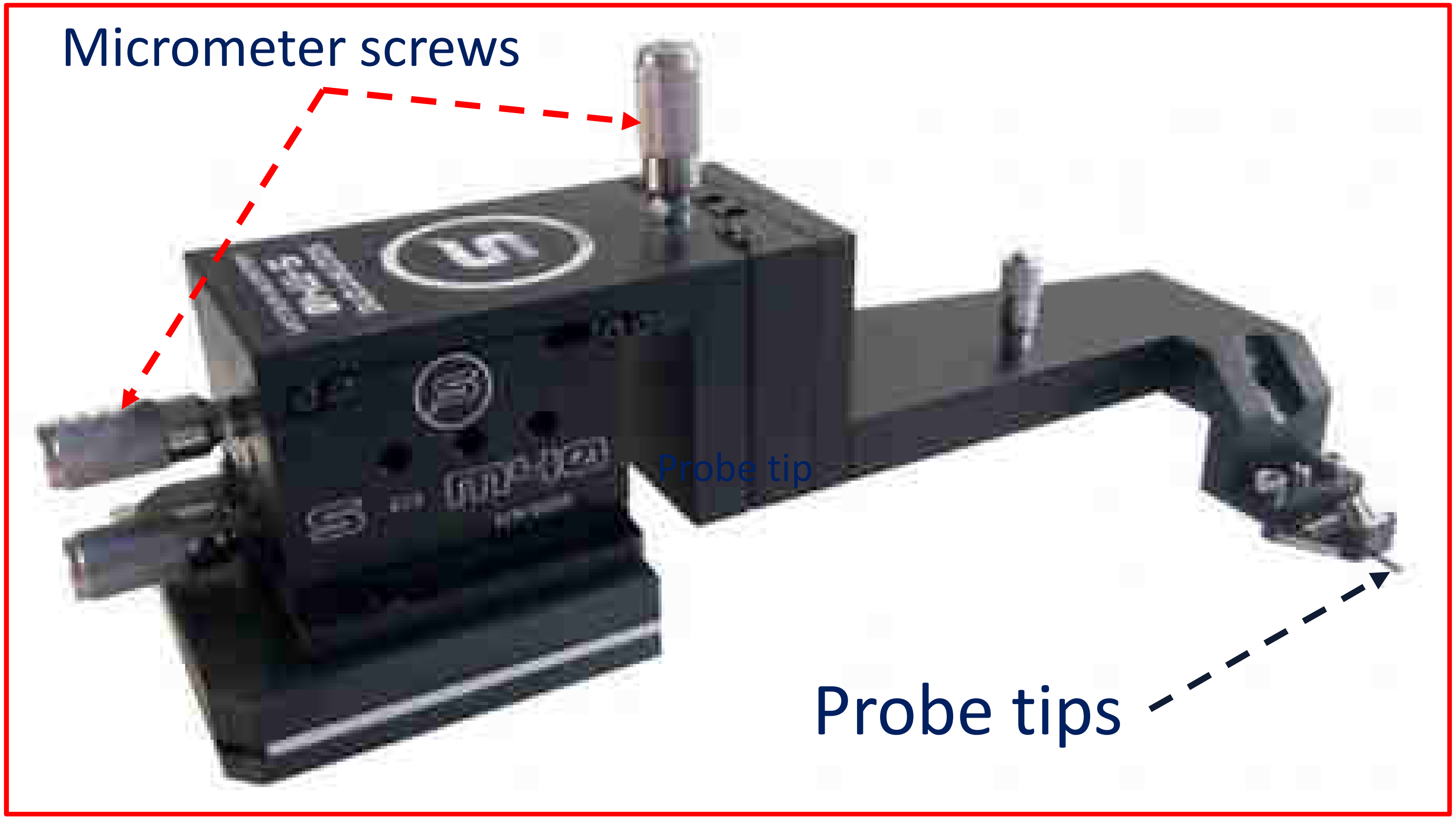


# HF probe stations On-wafer Probing System

Micropositioners
- adjust the probe contacts on test pads (check the scrub mark on the test pad)
- precise X-Y-Z alignment in all axes
- screw-lock to prevent accidentally moving the probe tips if bumped



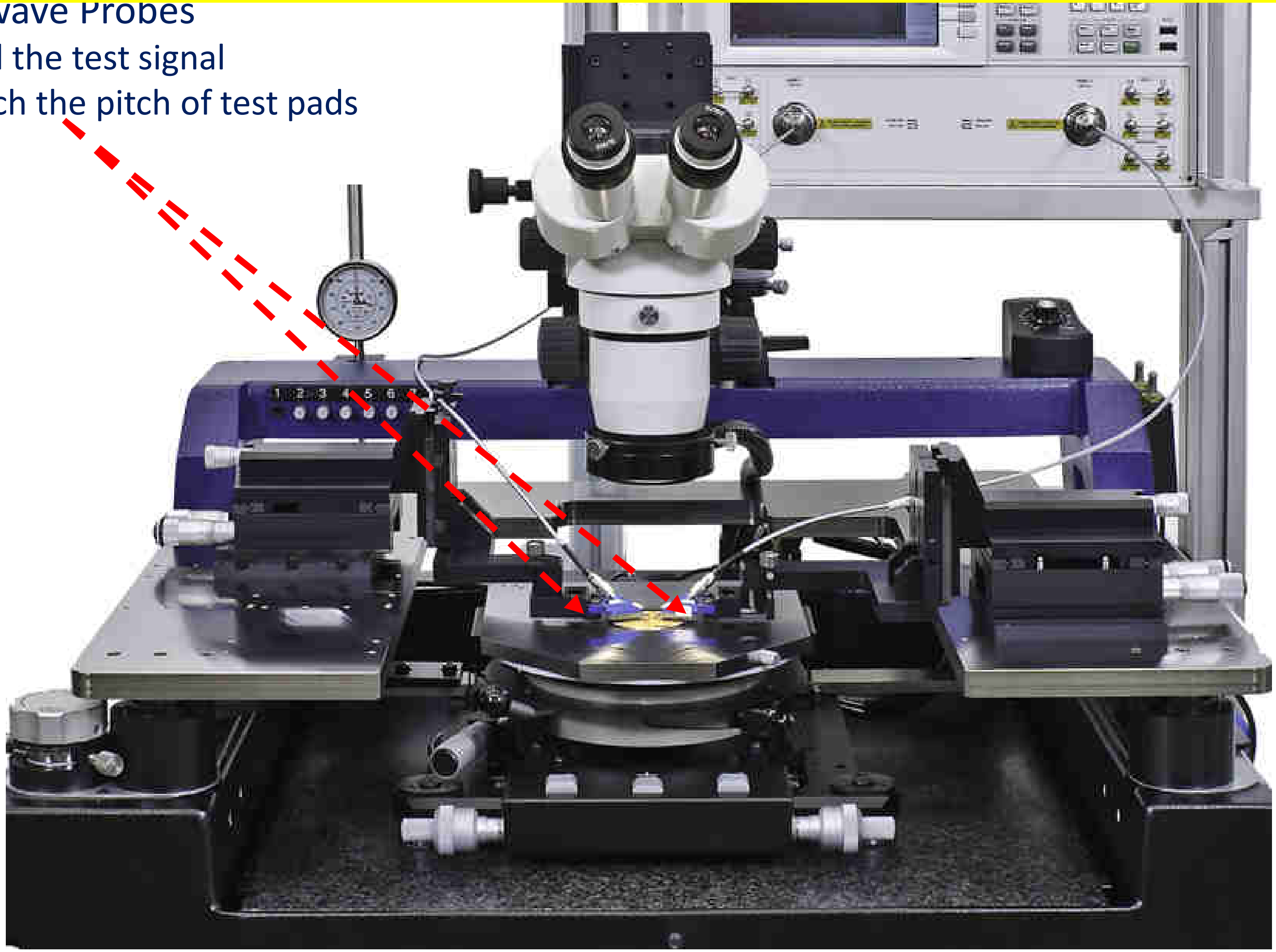
# Micropositioner of probe tips



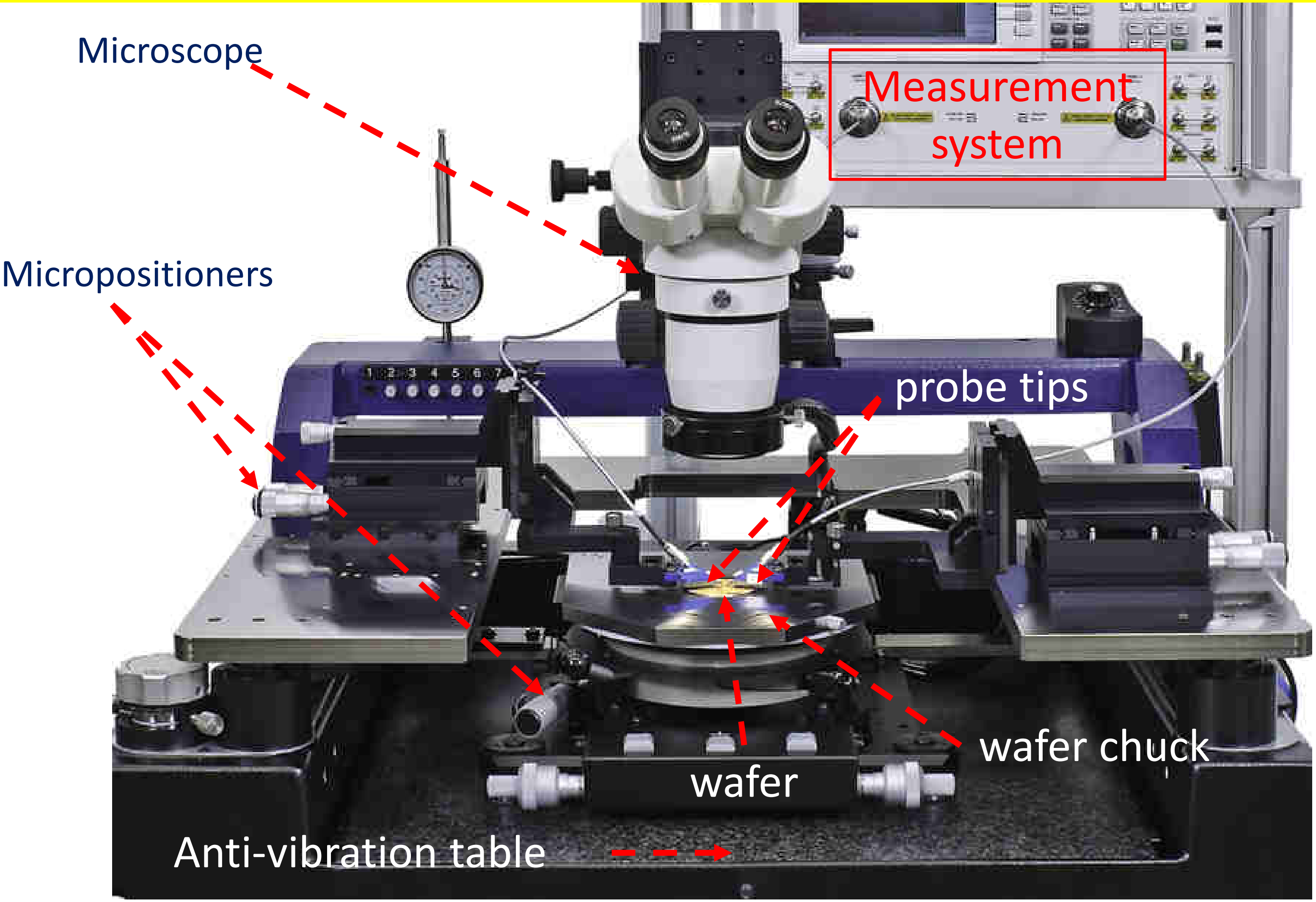
# HF probe stations On-wafer Probing System

Microwave Probes

- Feed the test signal
- Match the pitch of test pads



## HF probe stations  On-wafer Probing System



# I – Basics of MESFET operation

- Low-Frequency Bipolar transistors are based on the well-known PN Junction (P-type-SC / N-type-SC)

- High-Frequency MESFET (MEtal Semiconductor Field Effect Transistor) based on Schottky Junction (Metal / N-type-SC)

→ Simplified planar representation of FETs

→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)

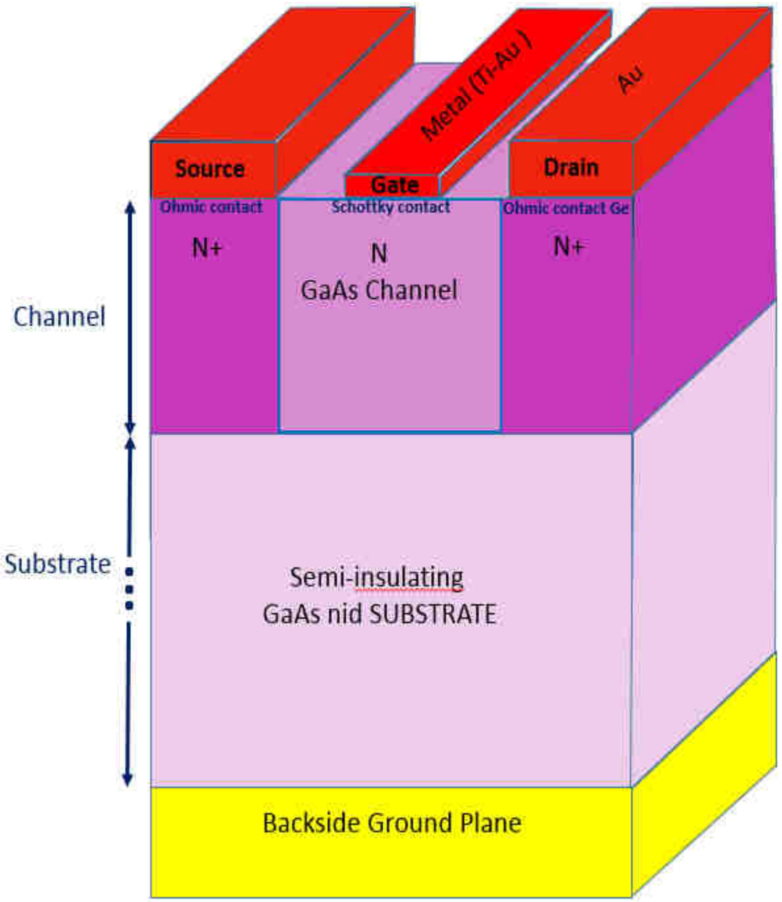
→ Localization of electrical equivalent elements that gives the nonlinear electrical model

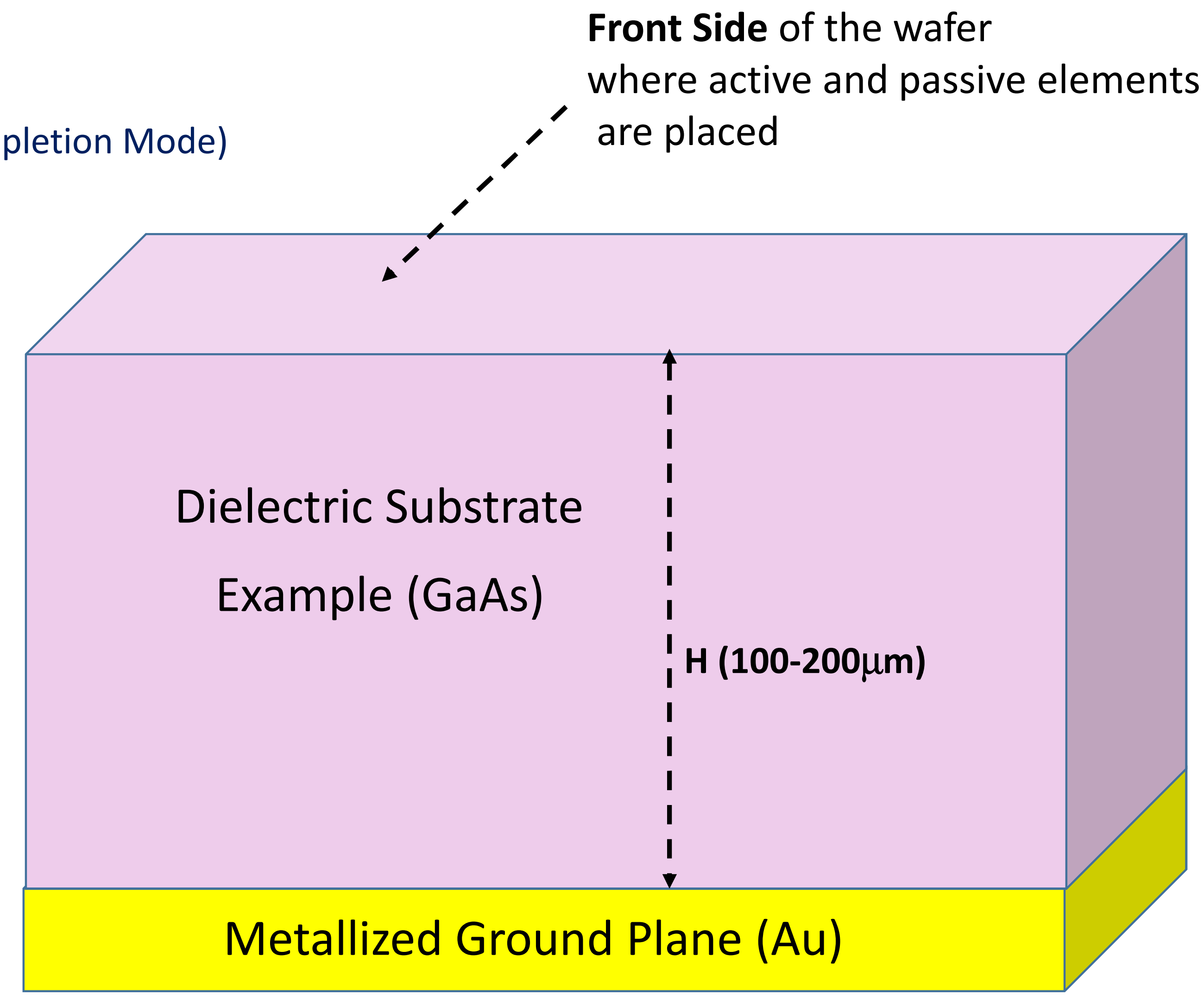
→ Successive simplification to derive the simplified linear electrical FET model

→ Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point

# I – Basics of MESFET operation

→ Simplified planar representation of FETs (Depletion Mode)



# Operating principles (FET / HEMT)

- **FET** → Gate voltage controls the flow of drain current by modifying the available section W of the doped channel (Impureties, Ionized scattering → Low mobility)

- **HEMT**→ Gate voltage controls the flow of drain Current by modifying the carrier density $n_S$ of a 2DEG in the undoped channel (no impureties → Very high mobility)

The (two-dimensional Electron Gas) **2DEG** is located at the **heterojunction** between a **wide bandgap semi-conductor (AlGaN)** and a **narrow bandgap semi-conductor (GaN).**

The electrons of the 2 DEG are free to move in a two-dimensional plane (x,z)
but tightly confined in the 3rd dimension (y)
because they are trapped in a potential well created at the heterojunction surface

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by modifying the available section W of the doped channel
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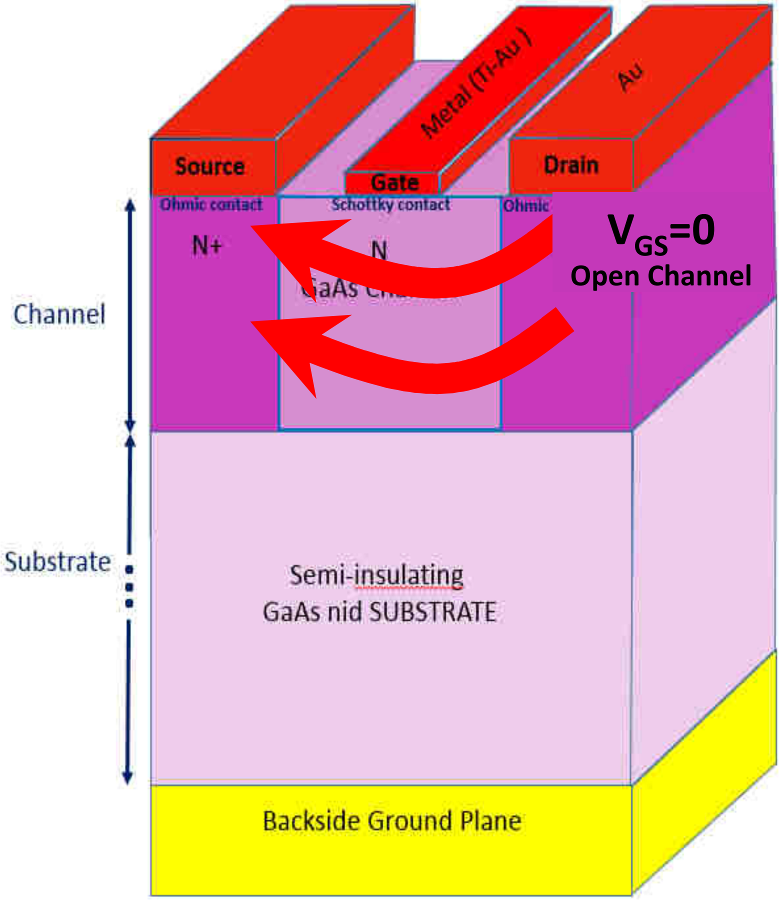
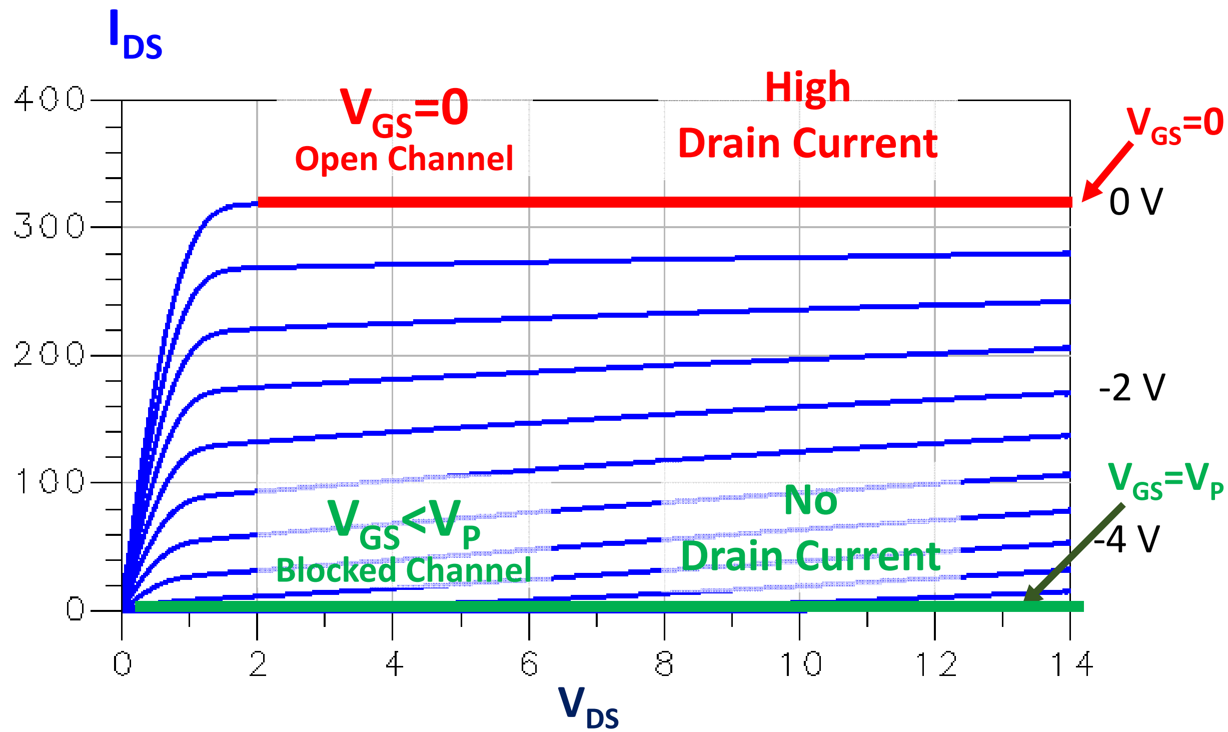
→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)



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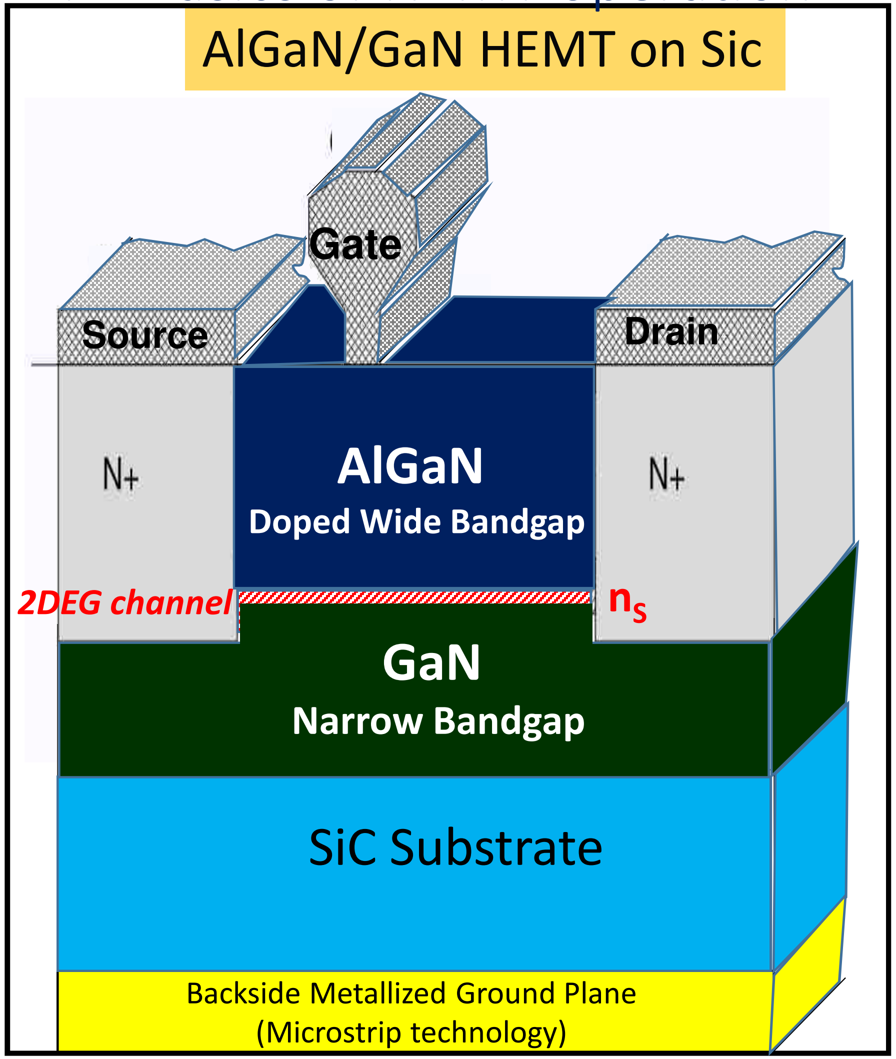
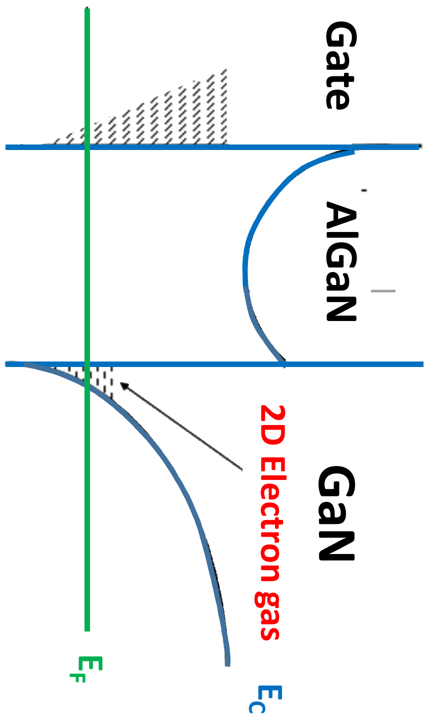
# I – Basics of HEMT operation → Same Electrical Circuit Model than FET

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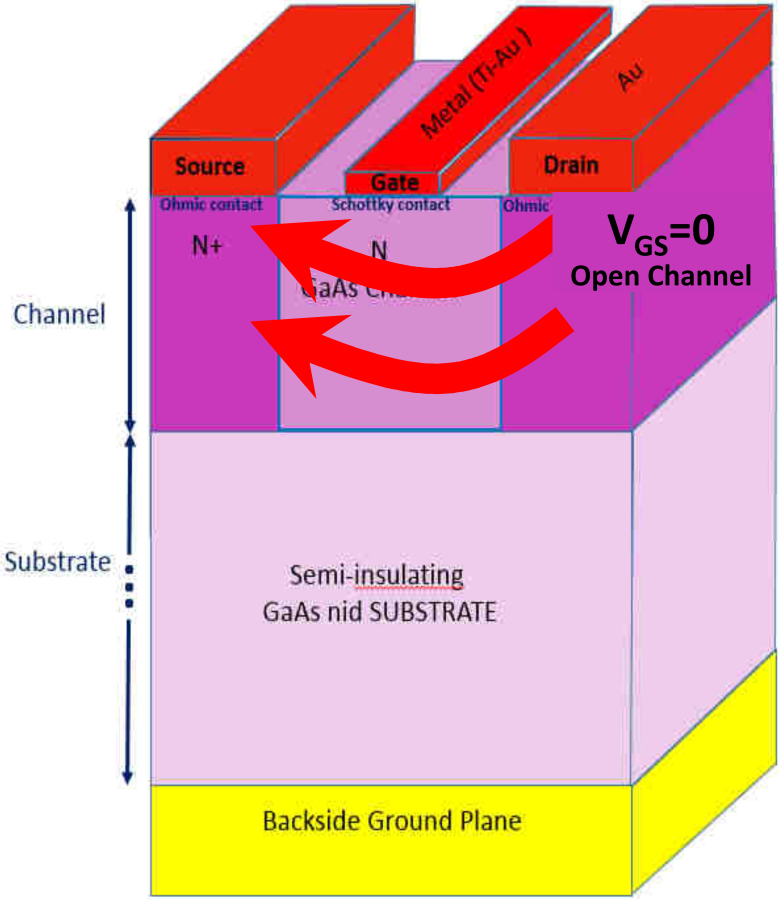
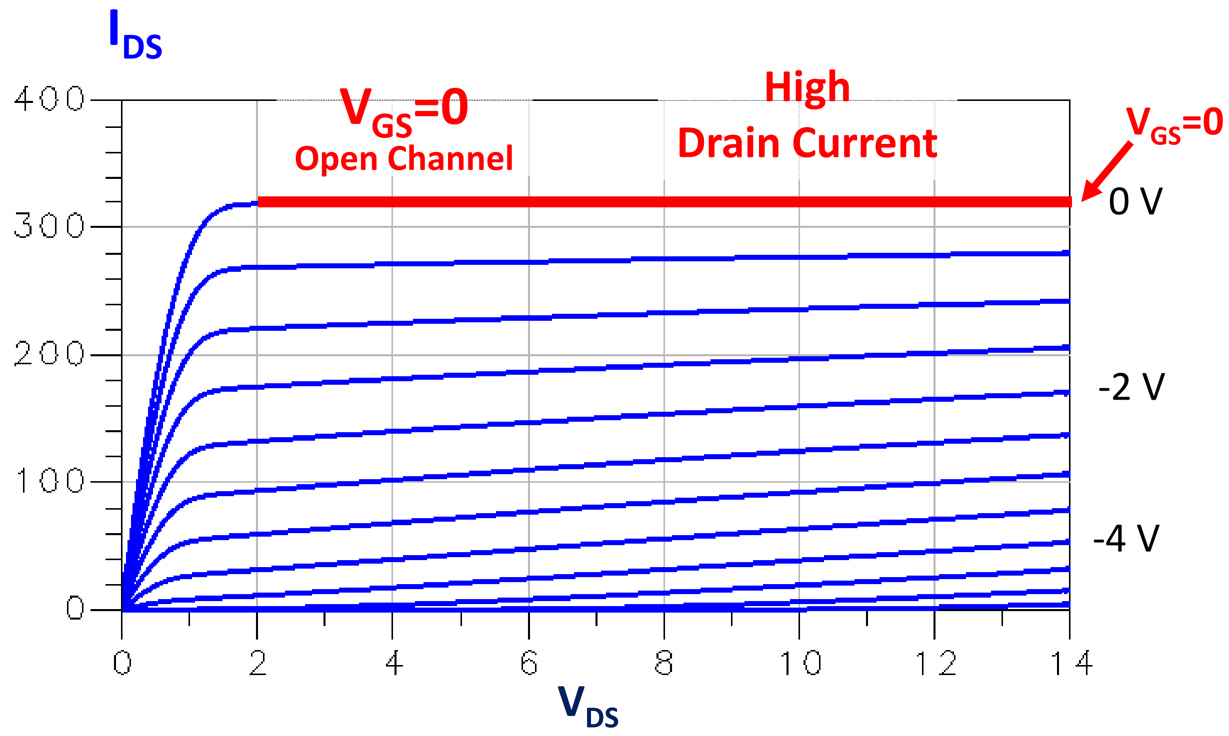
# I – Basics of MESFET operation

**FET** → Gate voltage controls the flow of drain current by modifying the available section W of the doped channel (Impureties, Ionized scattering → Low mobility)

→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)



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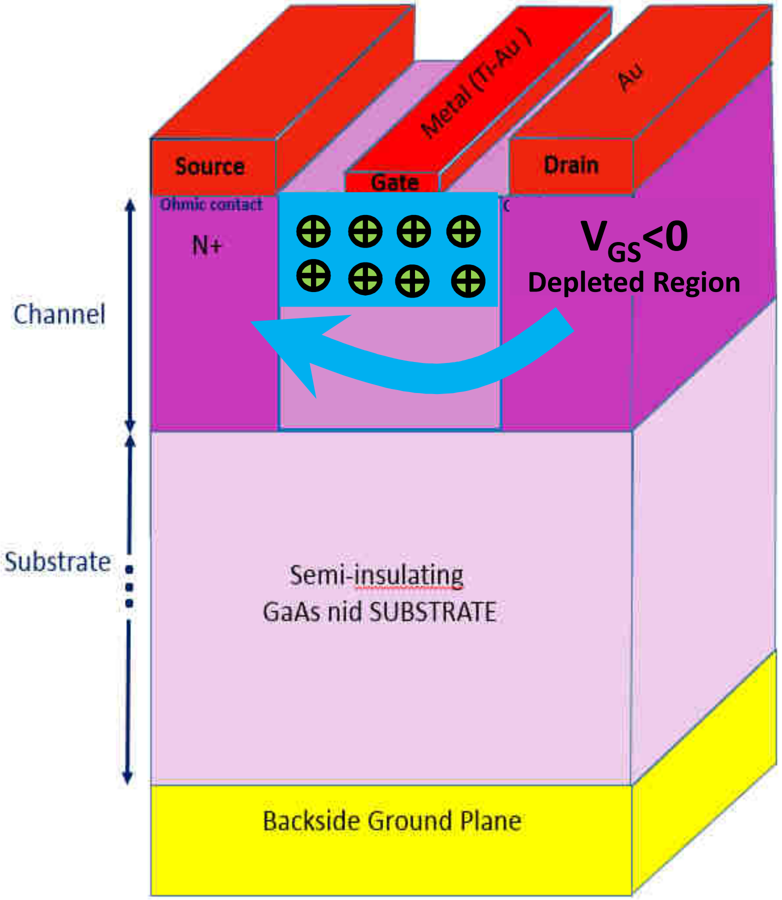


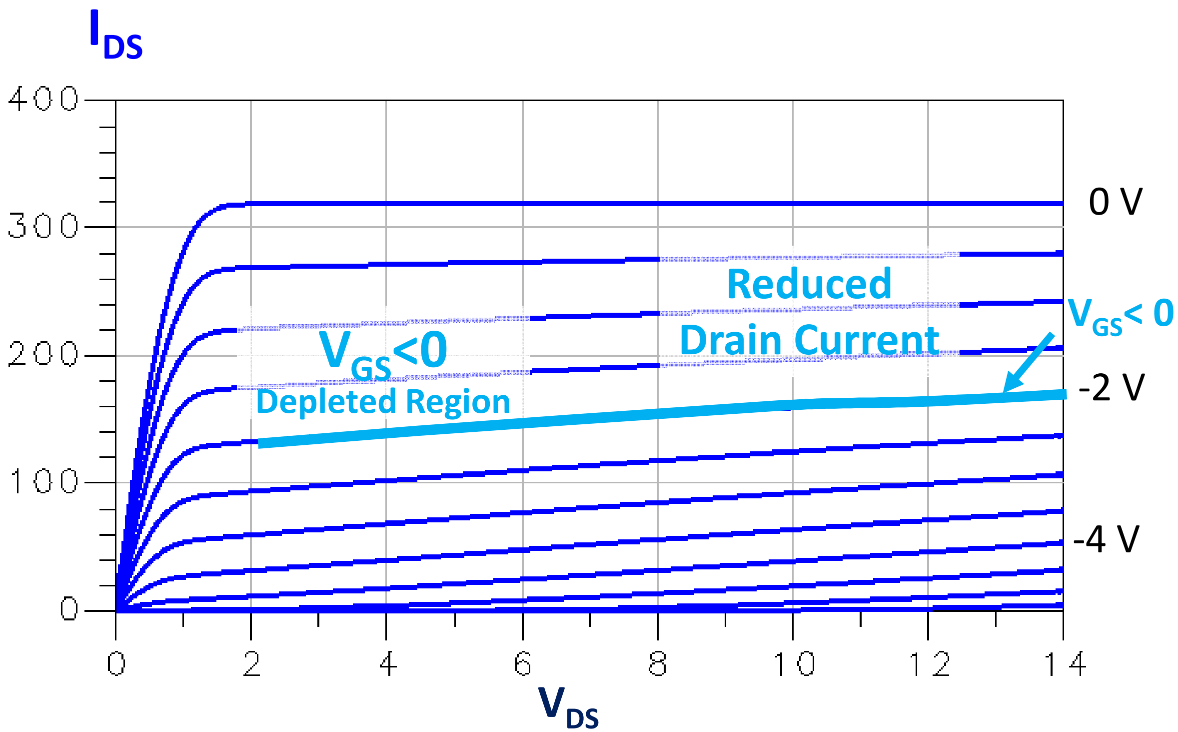

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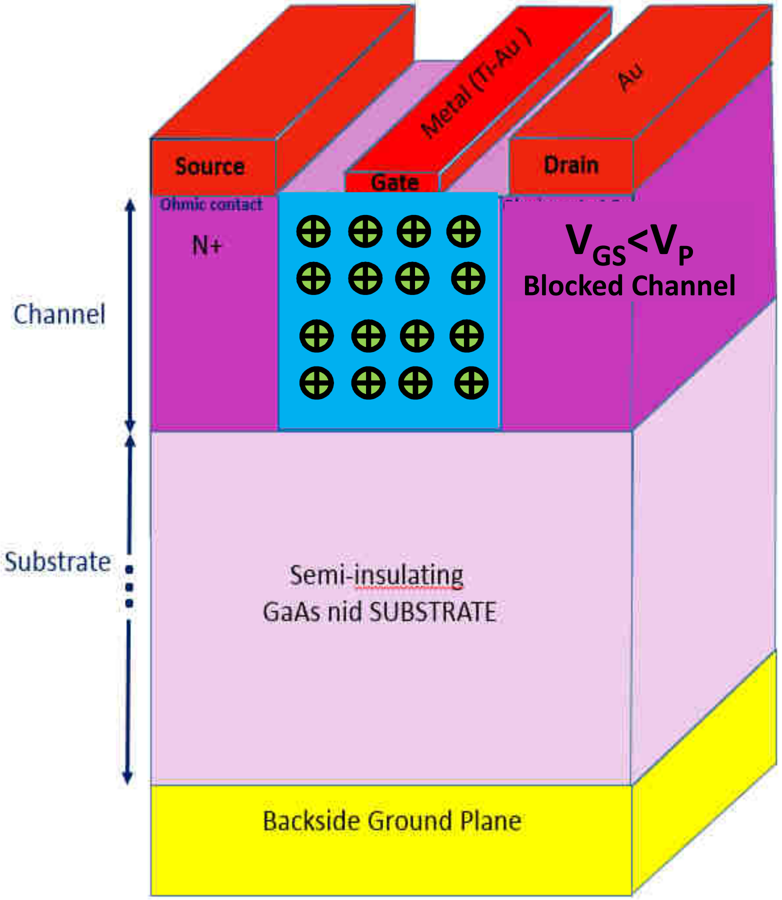


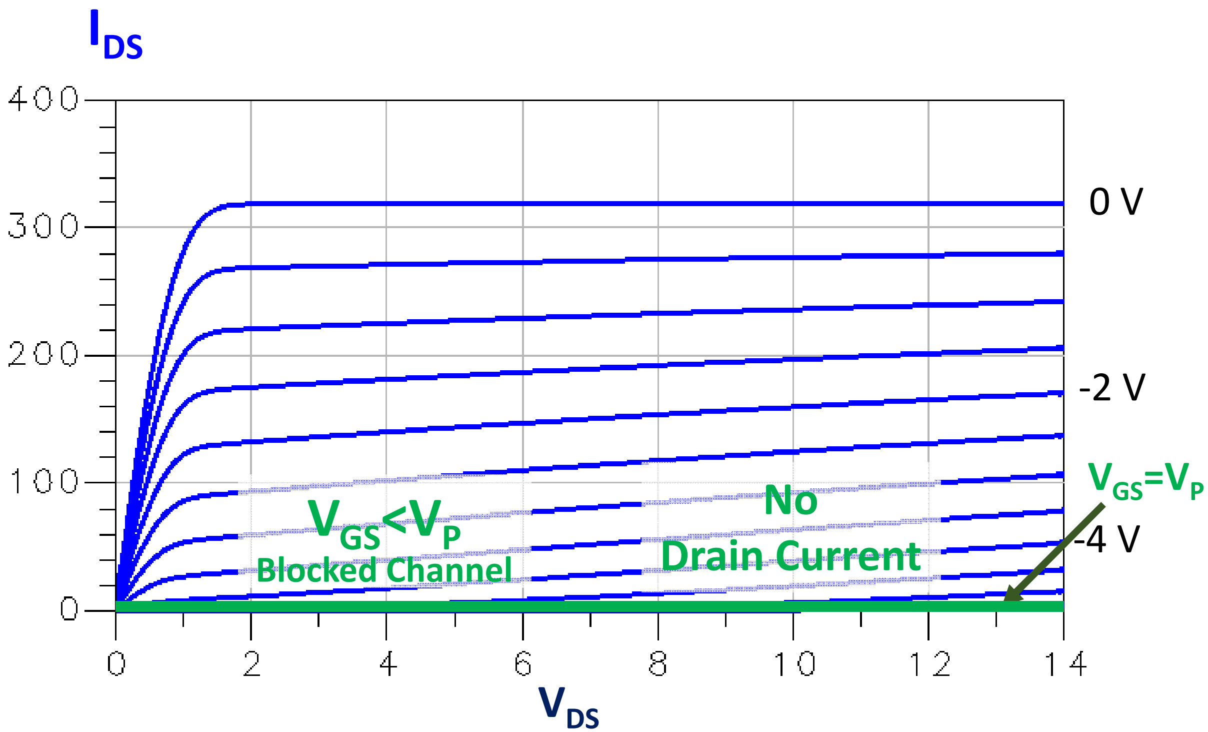

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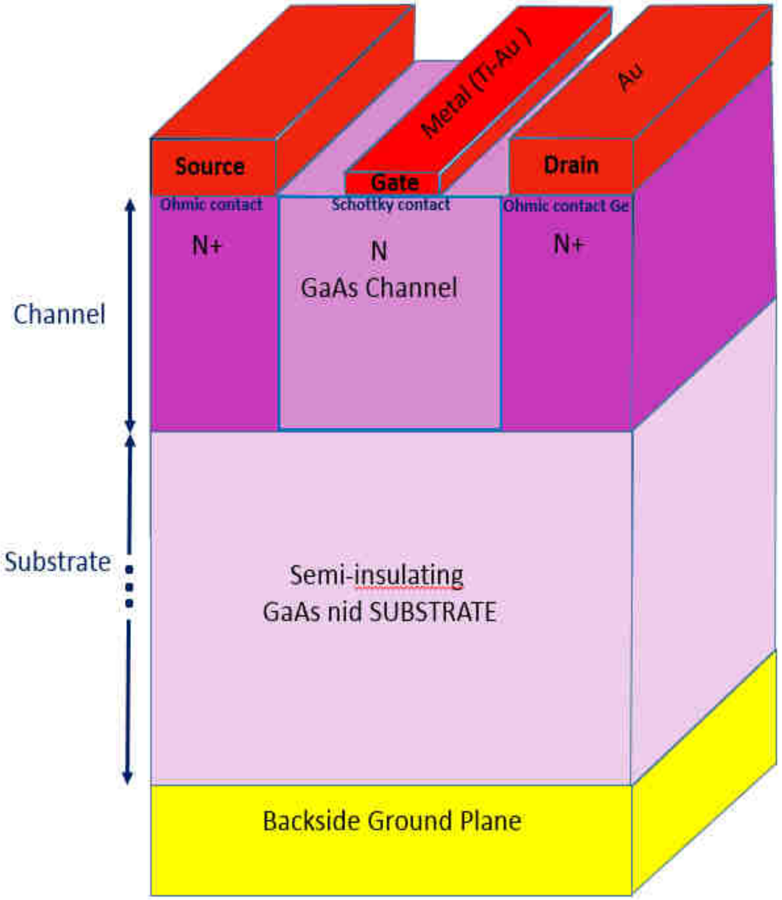
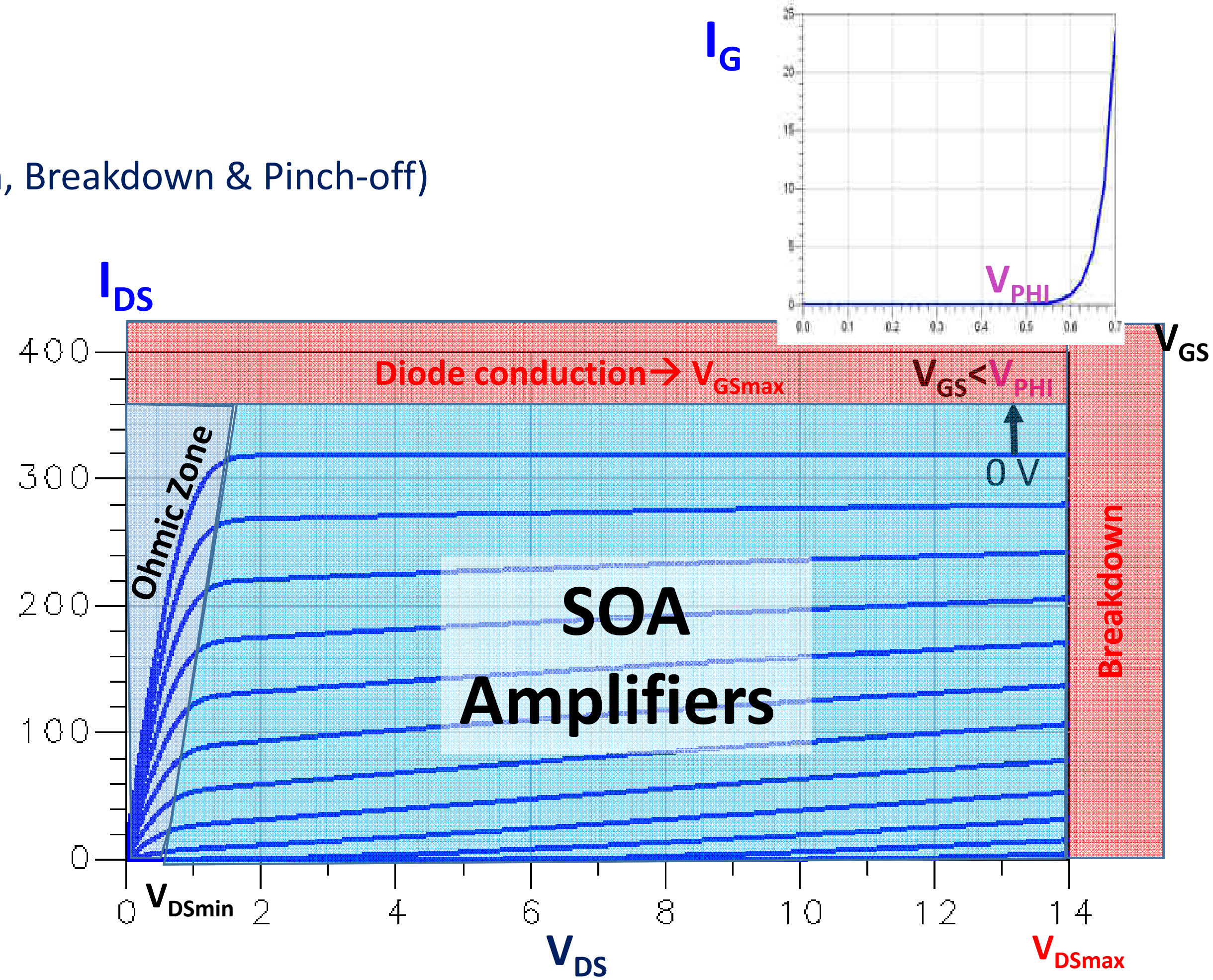
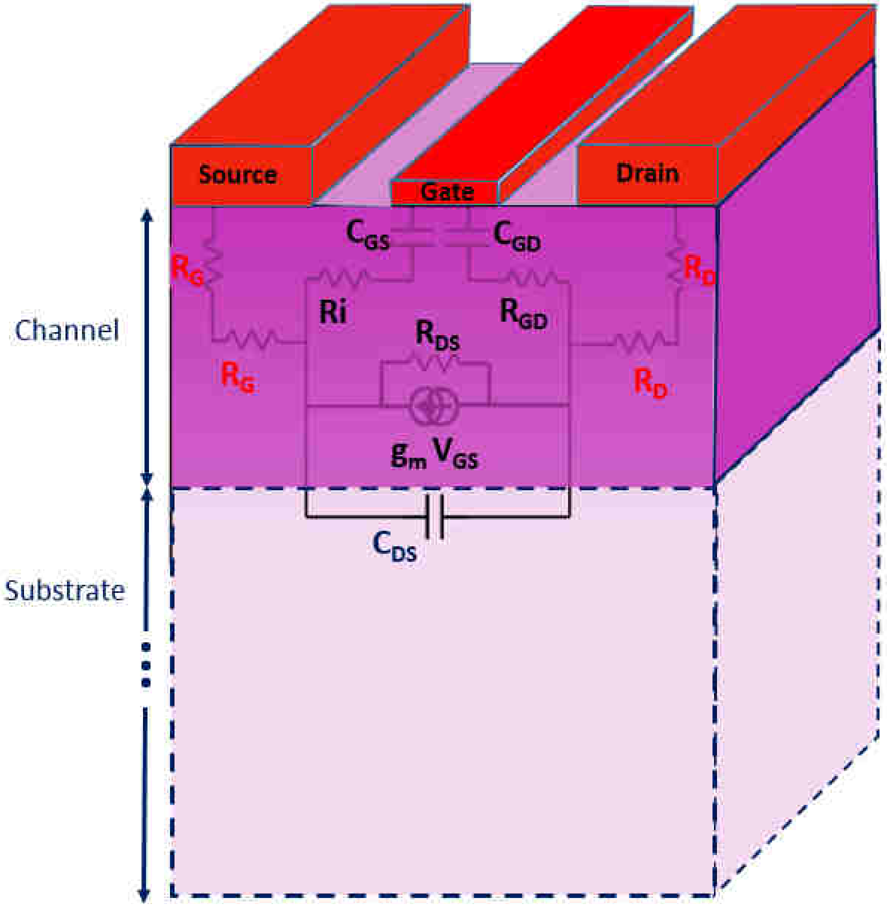
→ I-V regions (Ohmic, Saturated, Diode conduction, Breakdown & Pinch-off)



# I – Basics of MESFET operation

→ Simplified planar representation of FETs (localization of electrical lumped elements)



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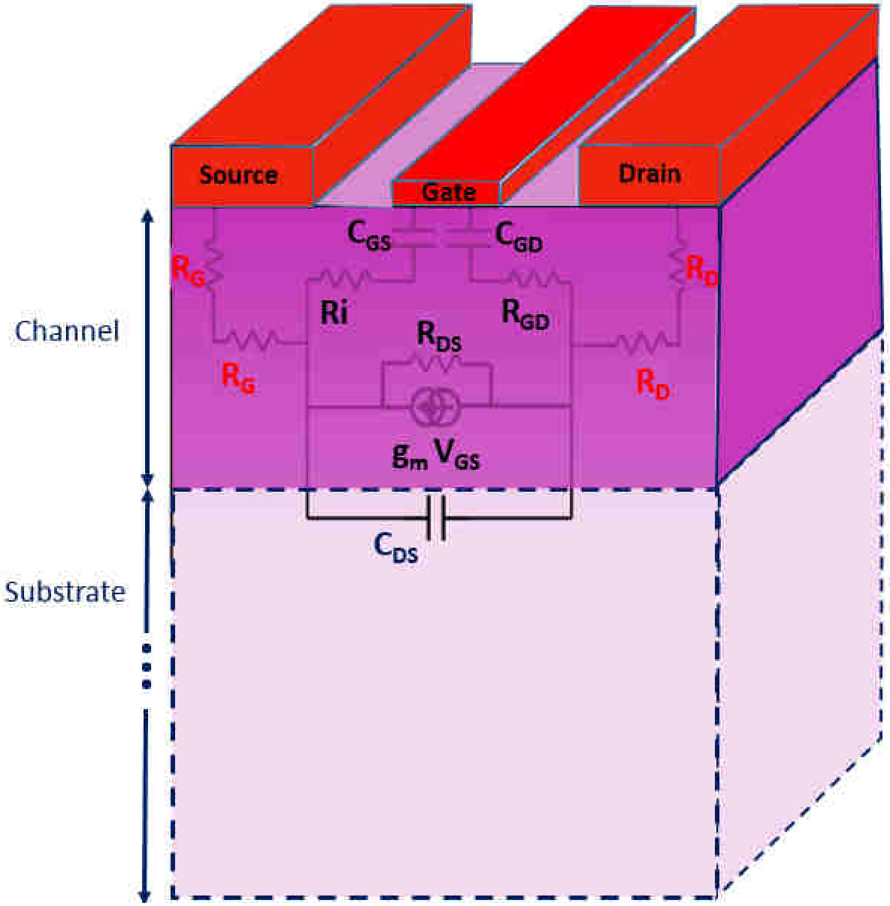


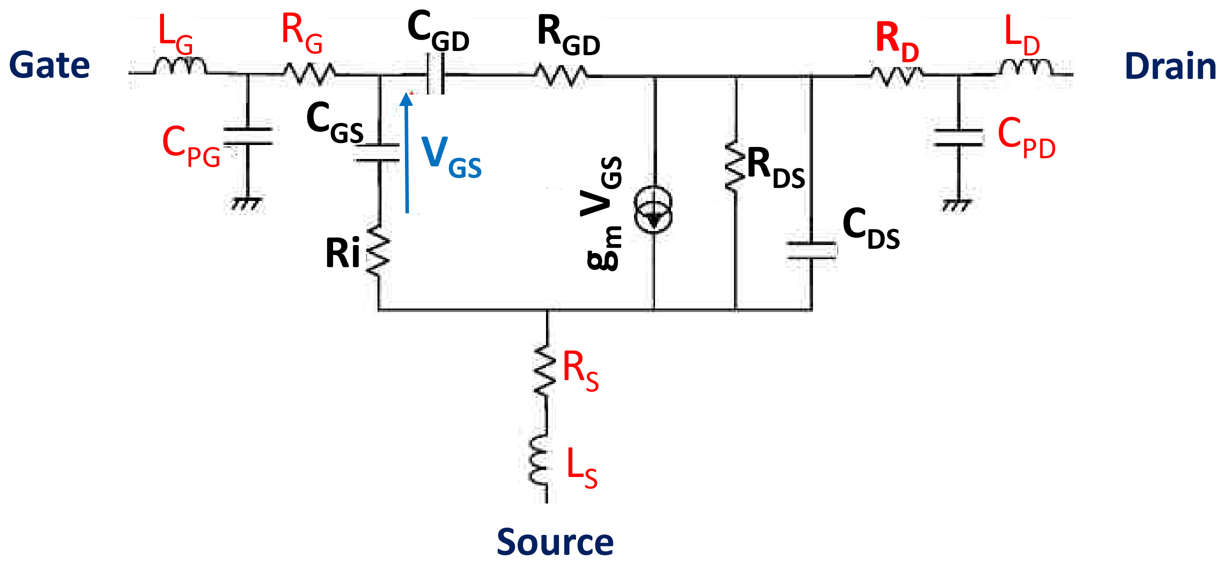

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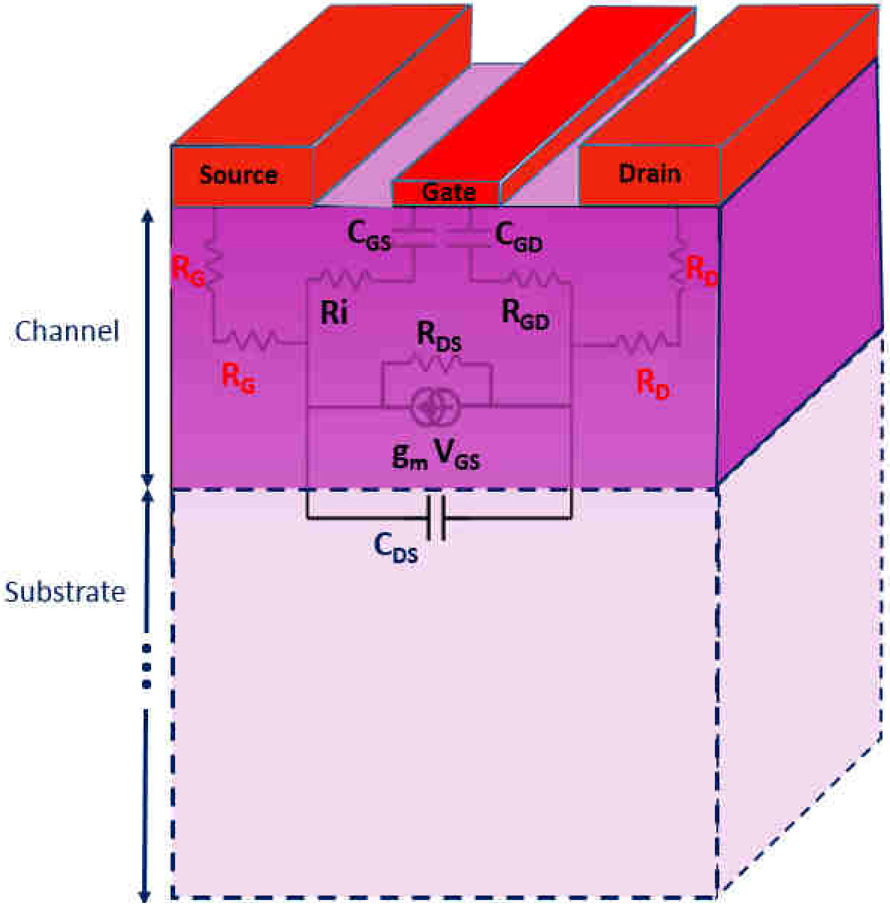


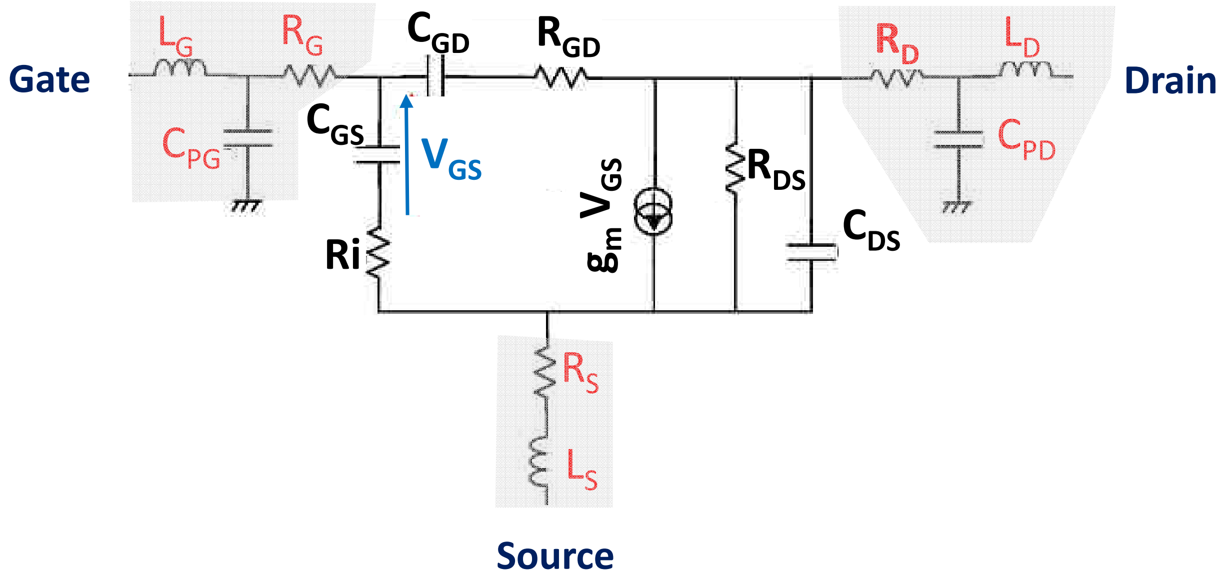


Extrinsic elements are the first ones that can be neglected when compared to other elements

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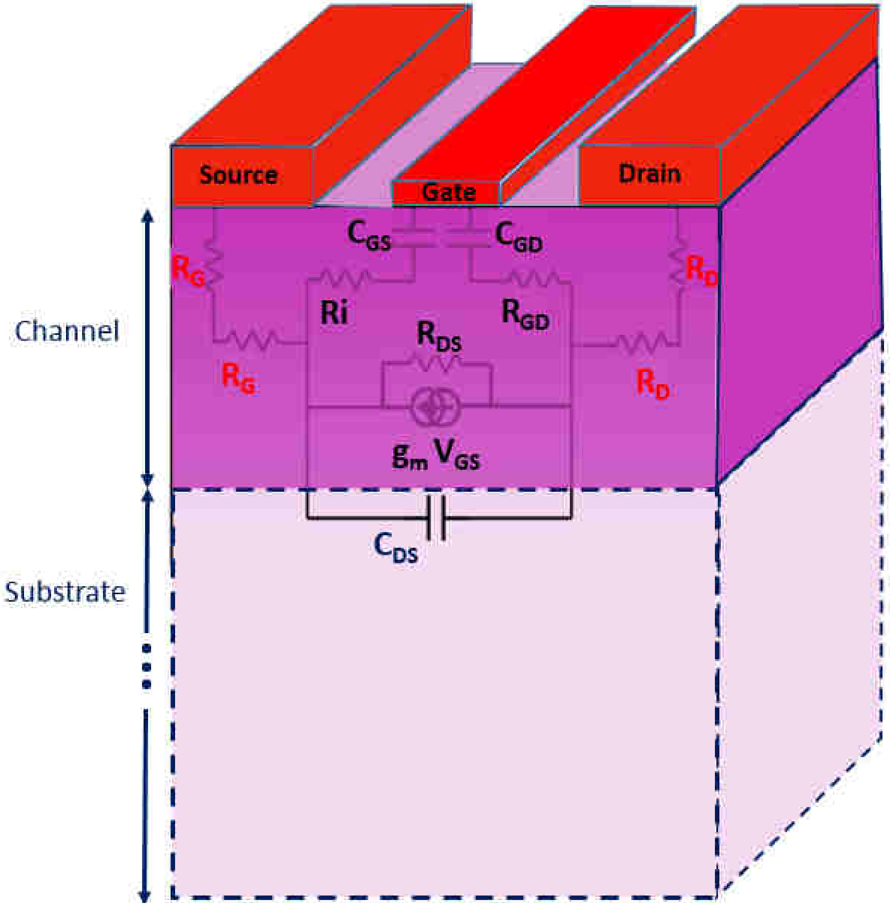


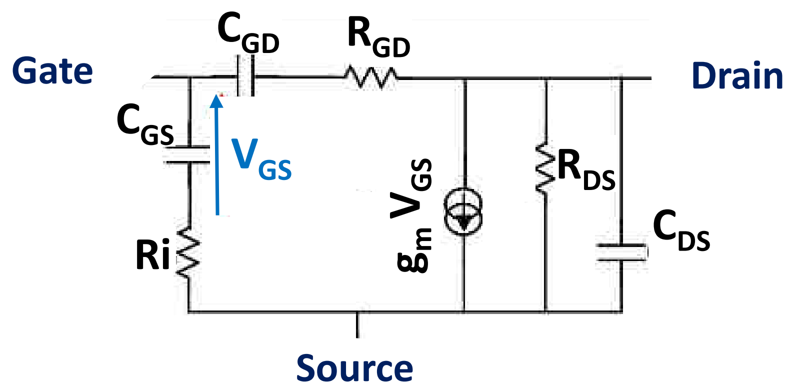


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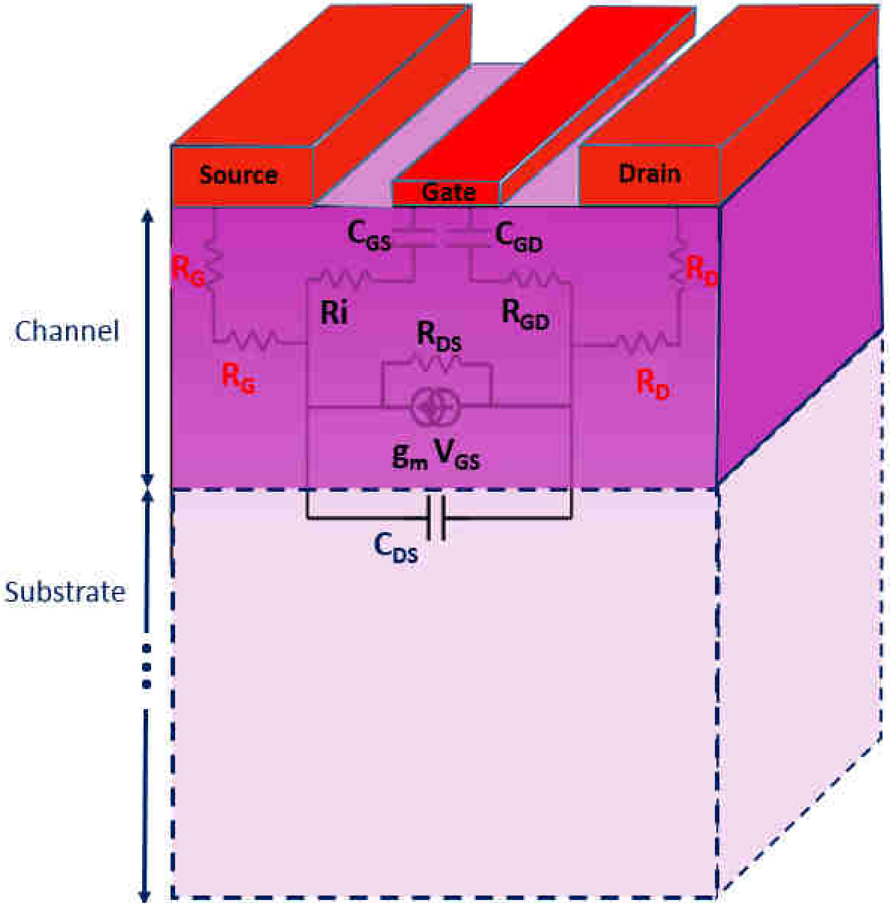


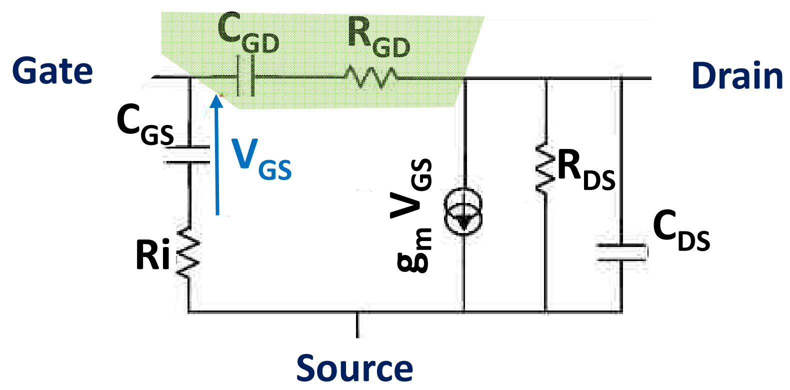


Feedback elements Gate-to-Drain can also be neglected.

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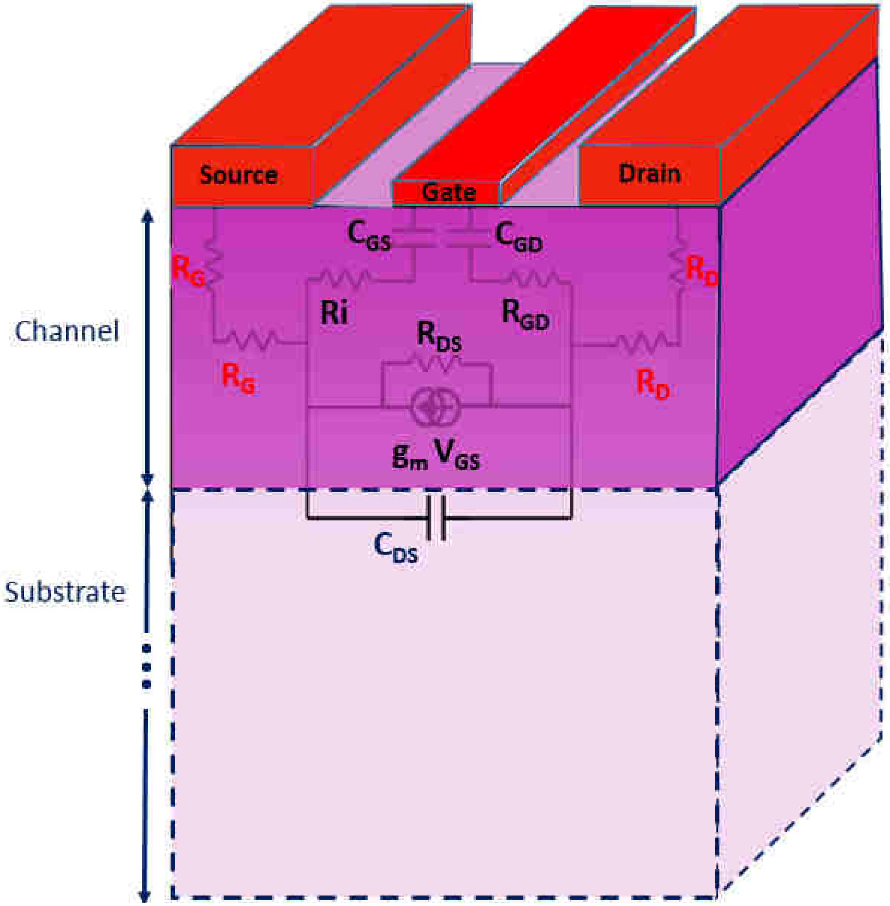
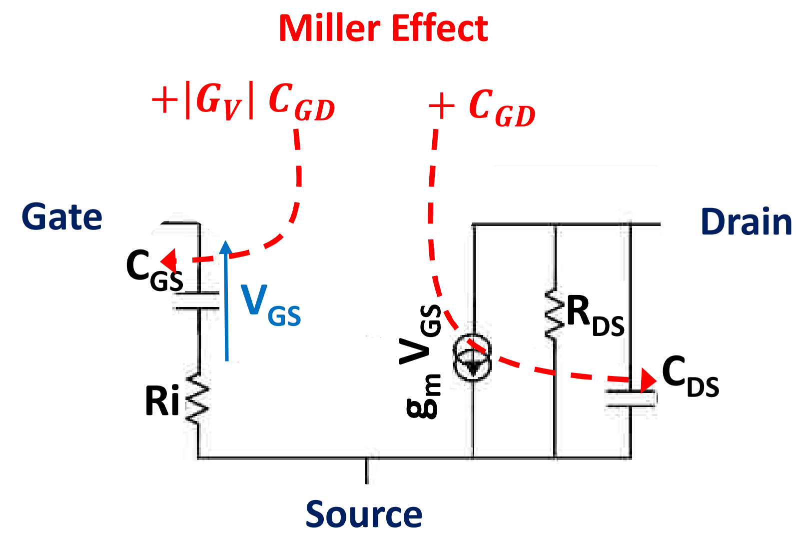


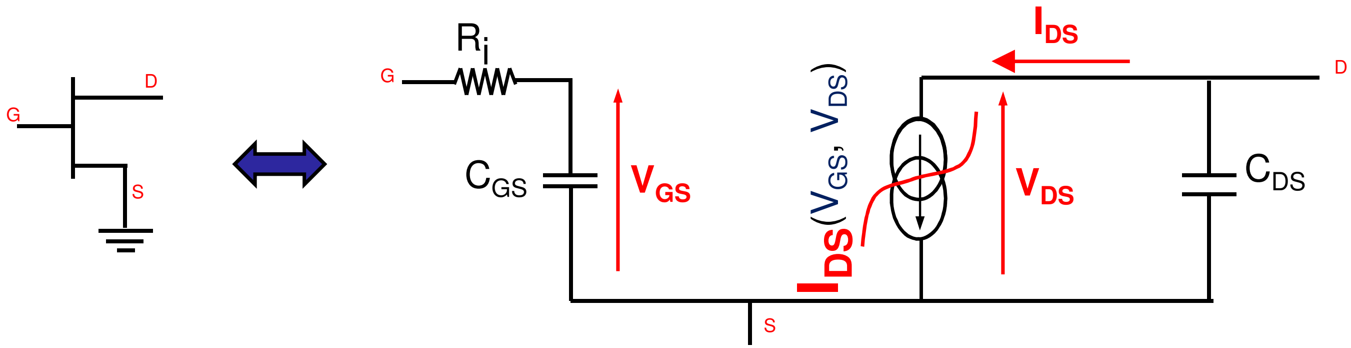




Feedback elements Gate-to-Drain can also be neglected.

However, the capacitive feedback is taken into account by **Miller Effect**

# I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point



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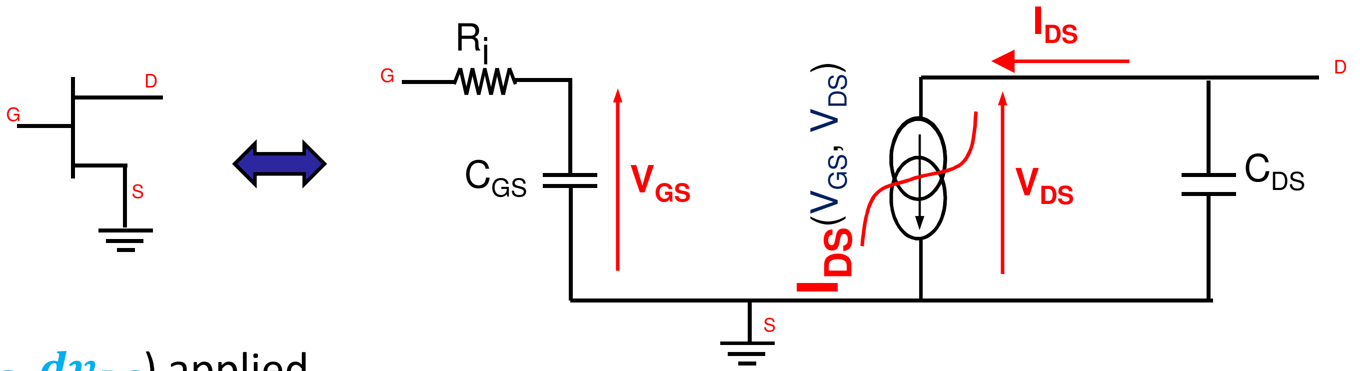
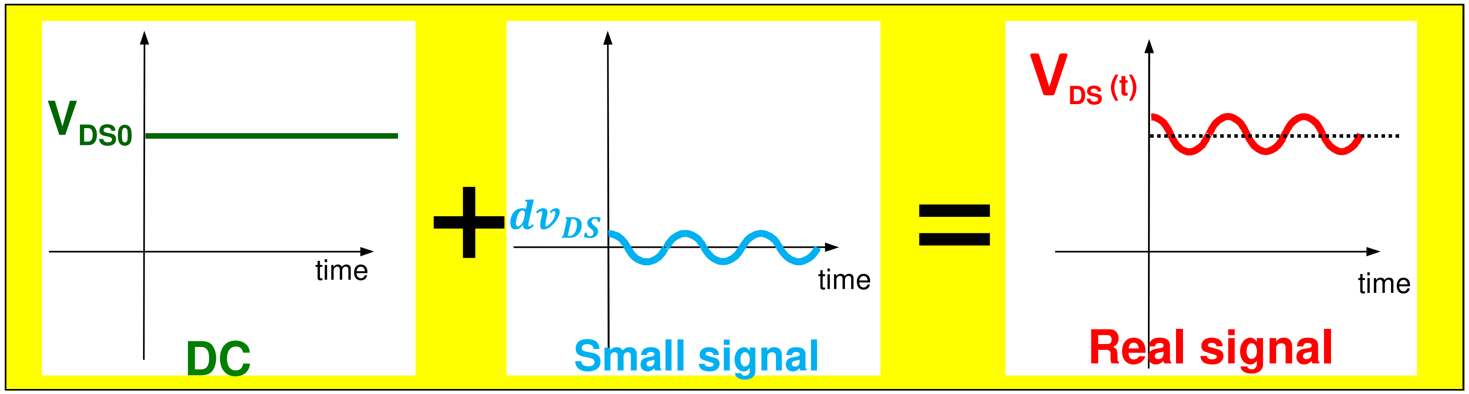



Small signals ($dv_{GS}$, $dv_{DS}$) applied around the bias point ($V_{GS0}$, $V_{DS0}$) give:



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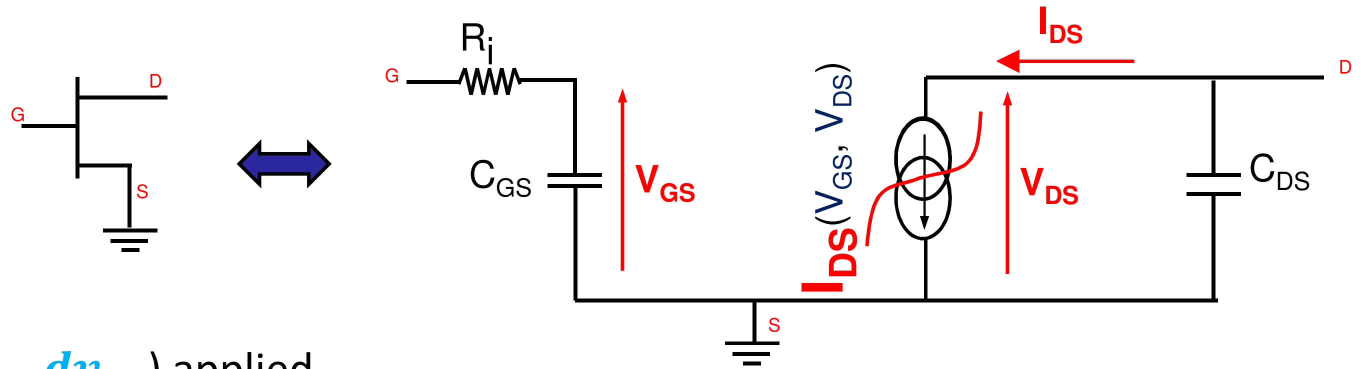


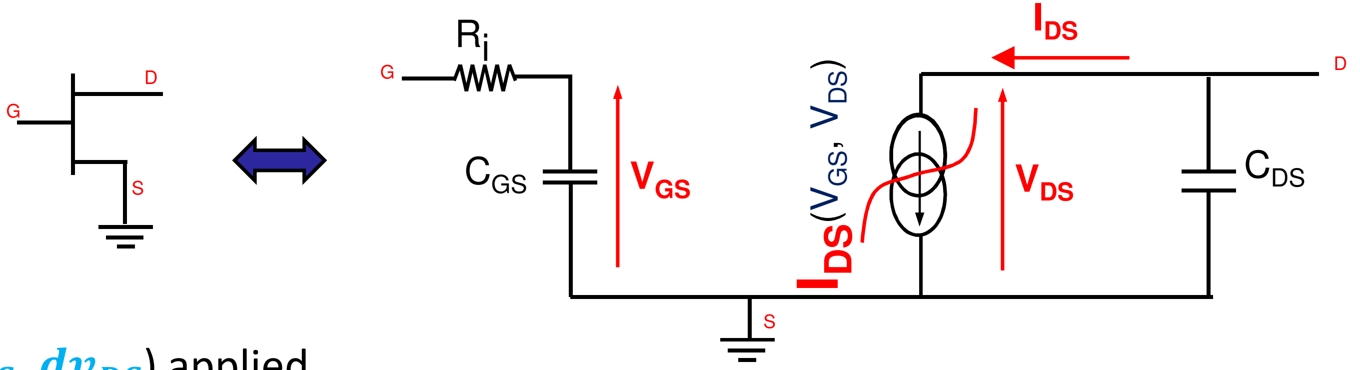

Small signals ($dv_{GS}$, $dv_{DS}$) applied around the bias point ($V_{GS0}$, $V_{DS0}$) give:

$$V_{GS}(t) = V_{GS0} + dv_{GS}(t)$$

$$V_{DS}(t) = V_{DS0} + dv_{DS}(t)$$

# I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point

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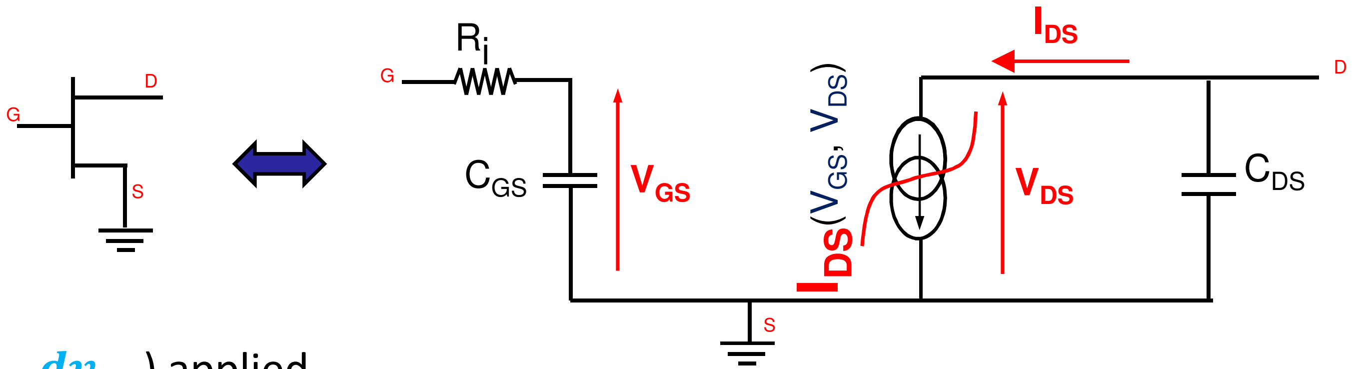
$$V_{GS}(t) = V_{GS0} + dv_{GS}(t)$$
$$V_{DS}(t) = V_{DS0} + dv_{DS}(t)$$

$$I_{DS}(t) = F_{NL}(V_{GS}, V_{DS}) = F_{NL}(V_{GS0}, V_{DS0}) + dF_{NL}$$
$$= I_{DS0} + dF_{NL}$$
$$I_{DS}(t) = I_{DS0} + di_{DS}$$

Taylor expansion

# I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point

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$$V_{DS}(t) = V_{DS0} + dv_{DS}(t)$$

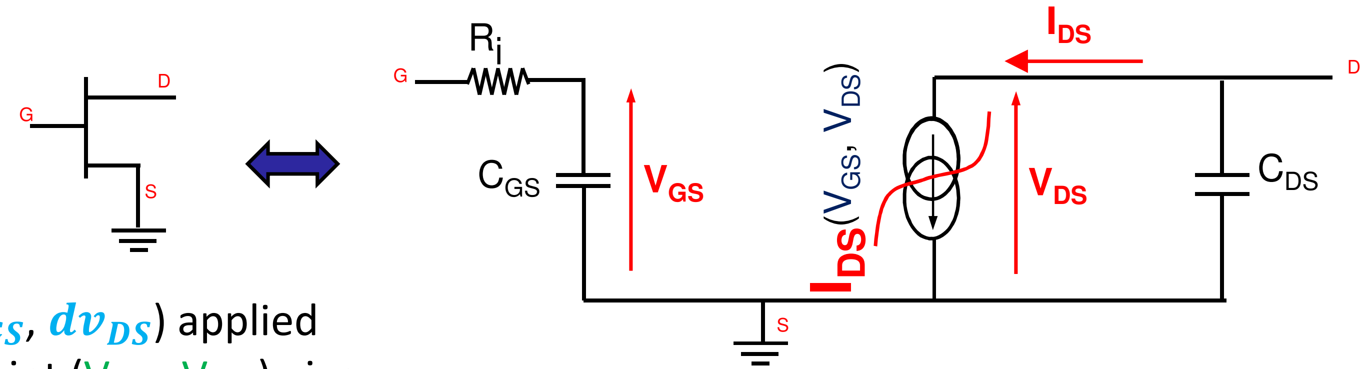
$$I_{DS}(t) = I_{DS0} + di_{DS}$$

Taylor expansion

$$di_{DS} = dF_{NL} = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\Bigg|_{(V_{GS0},\, V_{DS0})} .\ dv_{GS} + \left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\Bigg|_{(V_{GS0},\, V_{DS0})} .\ dv_{DS}$$

# I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point




Small signals ($dv_{GS}$, $dv_{DS}$) applied around the bias point ($V_{GS0}$, $V_{DS0}$) give:

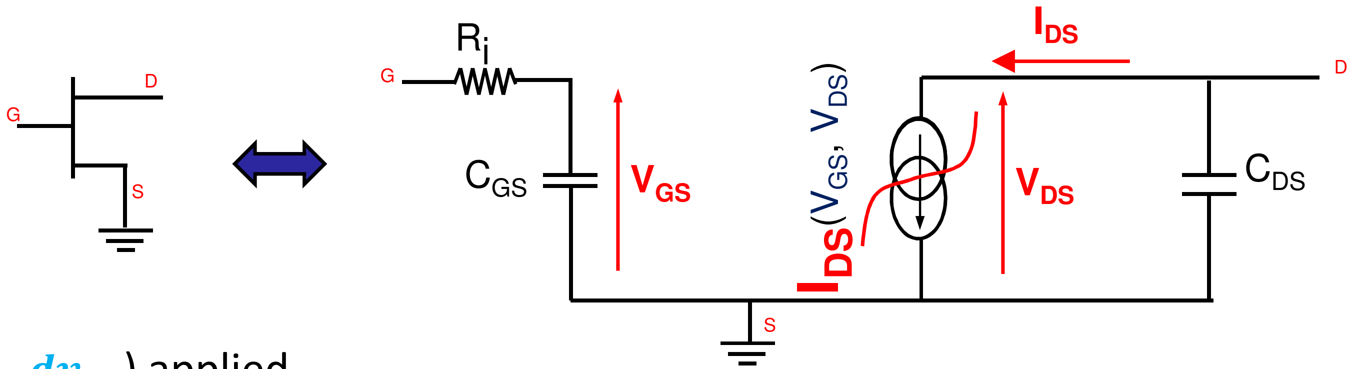
$dv_{GS}$(t)
$dv_{DS}$(t)

$$\Rightarrow \quad I_{DS}(t) = I_{DS0} + di_{DS}$$

$$di_{DS} = dF_{NL} = \left.\left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\right|_{(V_{GS0},\, V_{DS0})} .\, dv_{GS} + \left.\left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\right|_{(V_{GS0},\, V_{DS0})} .\, dv_{DS} = g_m\, .dv_{GS} + g_{DS}.\, dv_{DS}$$

# I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point




Small signals ($dv_{GS}$, $dv_{DS}$) applied around the bias point ($V_{GS0}$, $V_{DS0}$) give:

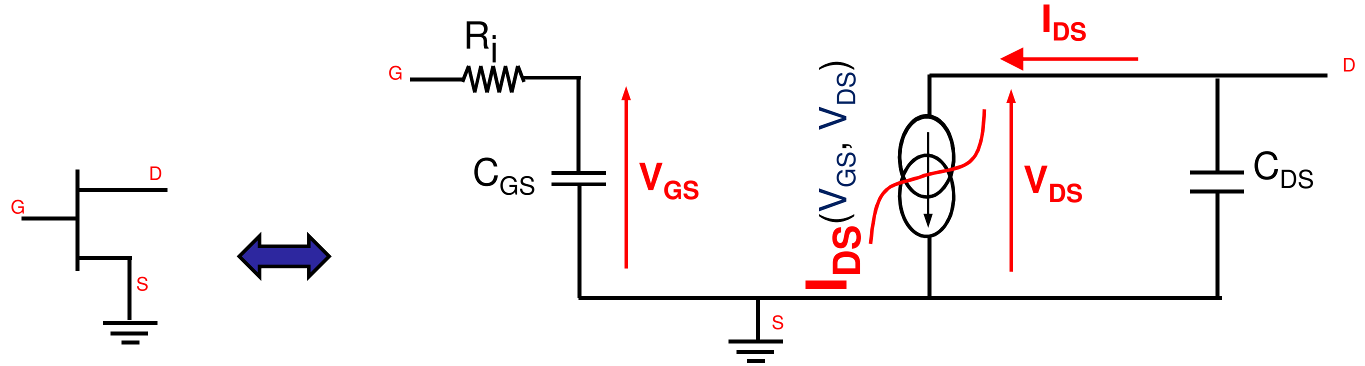
$dv_{GS}(t)$

$dv_{DS}(t)$

$$di_{DS} = g_m \cdot dv_{GS} + g_{DS} \cdot dv_{DS}$$

$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\Bigg|_{(V_{GS0},\, V_{DS0})} \qquad g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\Bigg|_{(V_{GS0},\, V_{DS0})}$$

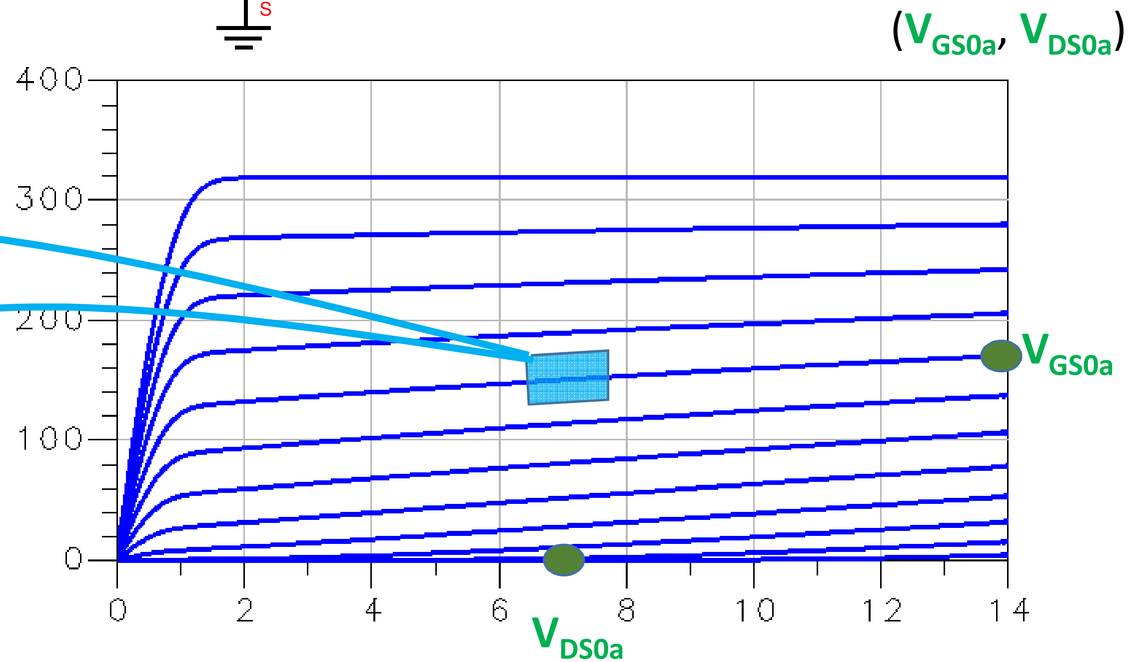
# I – Basics of FET operation



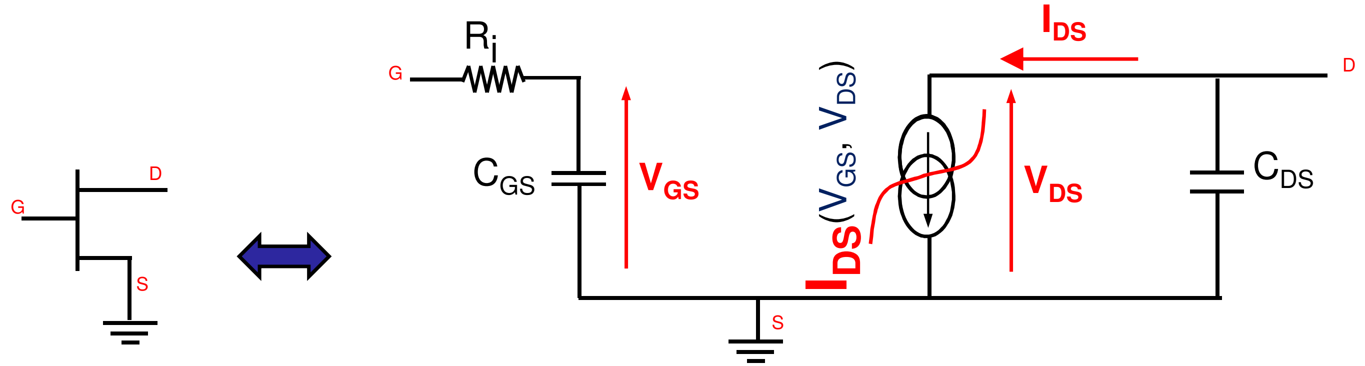

Small signals ($dv_{GS}$, $dv_{DS}$) applied around the bias point ($V_{GS0}$, $V_{DS0}$) give:

$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\Bigg|_{(V_{GS0},\ V_{DS0})}$$

$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\Bigg|_{(V_{GS0},\ V_{DS0})}$$



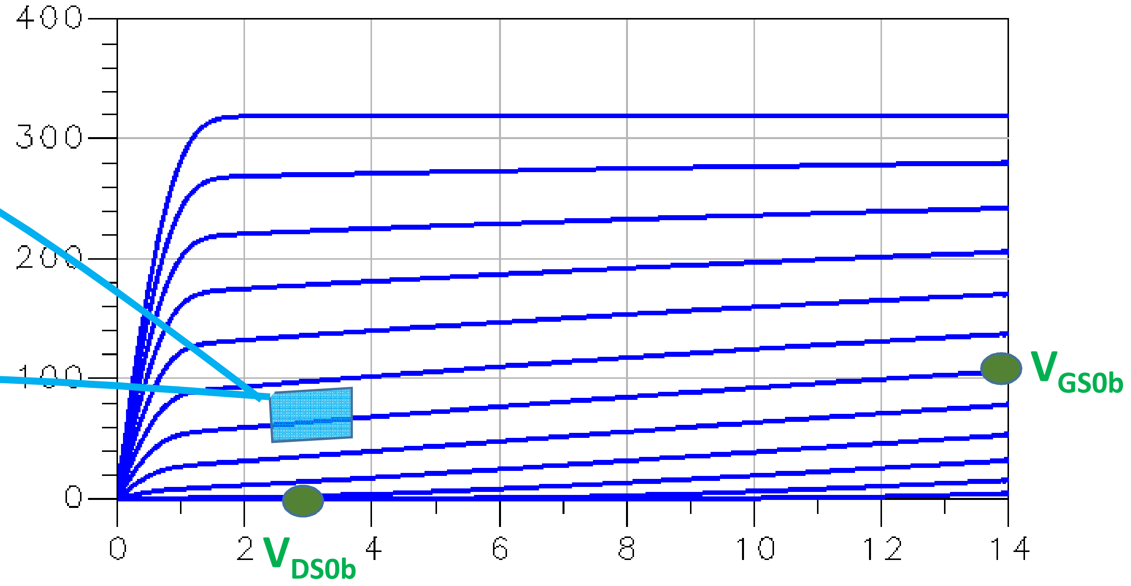
# I – Basics of FET operation



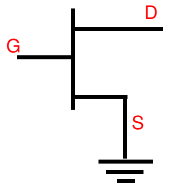

**Small signals** ($dv_{GS}$, $dv_{DS}$) applied around the bias point ($V_{GS0}$, $V_{DS0}$) give:

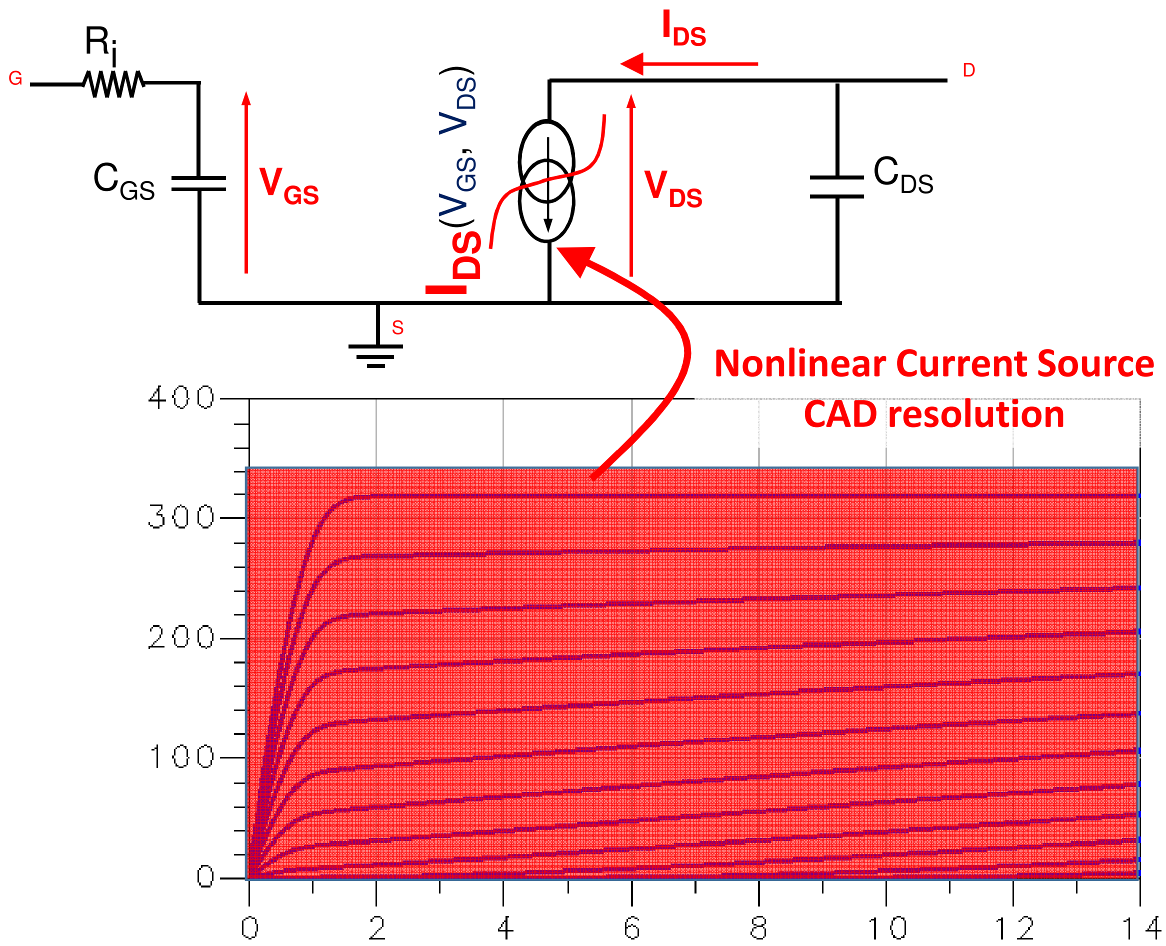
$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\Bigg|_{(V_{GS0},\,V_{DS0})}$$

$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\Bigg|_{(V_{GS0},\,V_{DS0})}$$



# I – Basics of FET operation



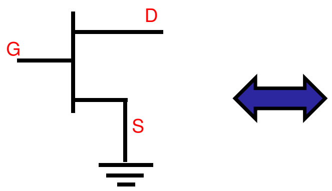

**Large signals** ($\Delta V_{GS}$, $\Delta V_{DS}$) applied around the bias point ($V_{GS0}$, $V_{DS0}$) give:

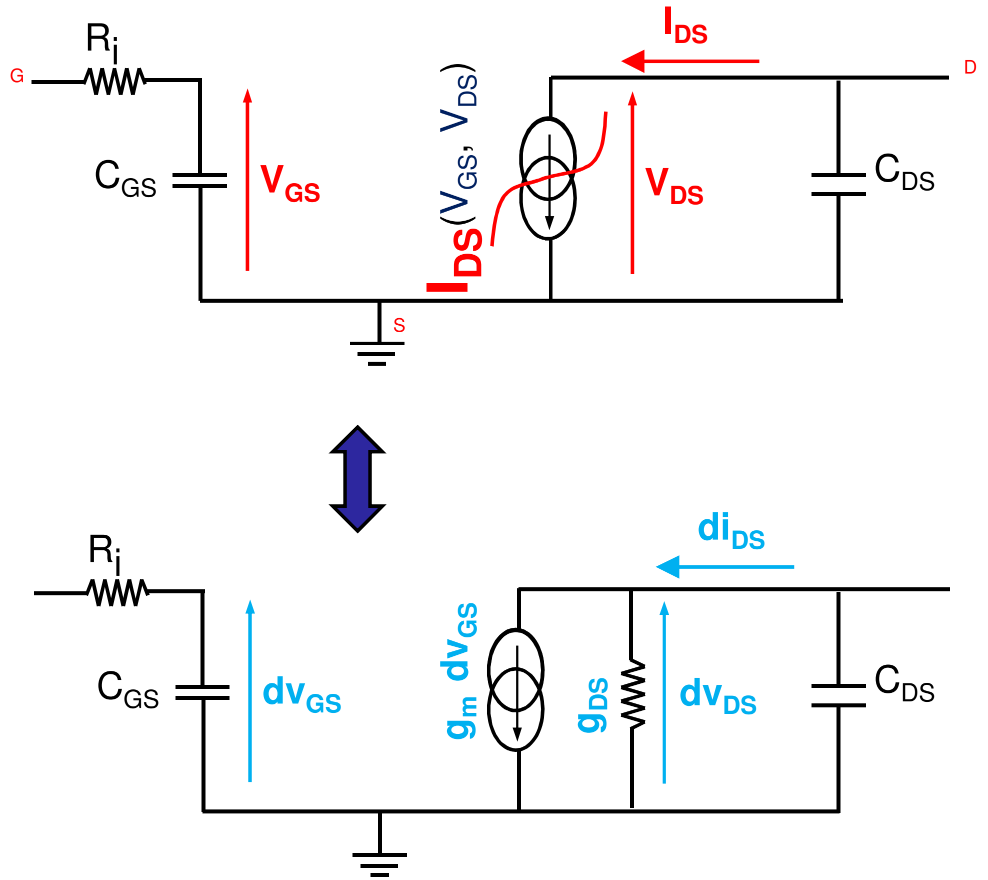
$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\bigg|_{(V_{GS0},\, V_{DS0})}$$

$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\bigg|_{(V_{GS0},\, V_{DS0})}$$

# I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point



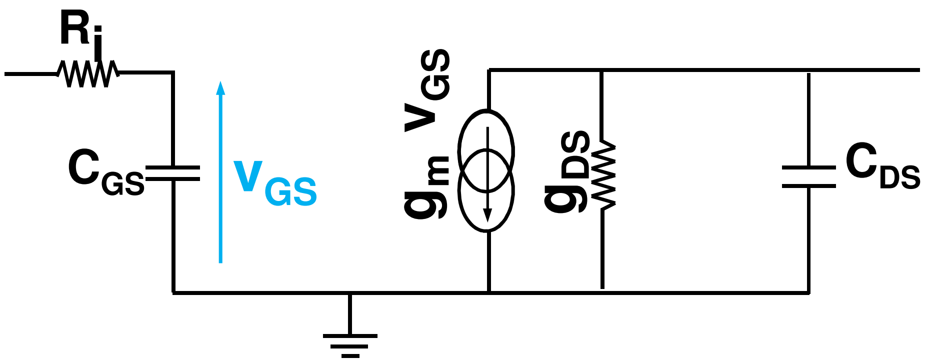




**<u>Small signals</u>** ($dv_{GS}$, $dv_{DS}$) applied around the bias point ($V_{GS0}$, $V_{DS0}$) give:

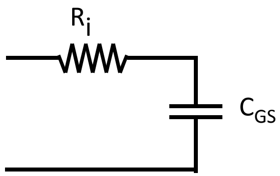
$V_{GS} = V_{GS0} + dv_{GS}$
$V_{DS} = V_{DS0} + dv_{DS}$

# I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point



# II – Intrinsic figures of merit for FETs




1) Low-Pass Frequency (Low-Pass Input RC circuit)

$$\boxed{f_{LP} = \frac{1}{2\pi R_i C_{GS}}}$$

The FET is efficiently used at frequencies $f \ll f_{LP}$ → $\boxed{R_i C_{GS} \omega \ll 1}$

2) Cutoff frequency of gain current

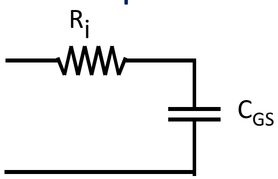
Current Gain in Short-Circuit

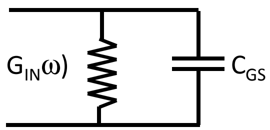
$$Gi_{SC} = \frac{I_{OUT_{SC}}}{I_{IN}} = \frac{g_m V_{GS}}{j\, C_{GS}\, \omega\, V_{GS}} = \frac{g_m}{j\, C_{GS} \omega} \Rightarrow |Gi_{SC}(f_C)| \overset{\text{def}}{=} 1 \iff \frac{g_m}{C_{GS}\omega_C} = 1 \iff \omega_C = \frac{g_m}{C_{GS}}$$

$$\boxed{f_C = \frac{g_m}{2\pi C_{GS}}}$$

$f_C$ is widely used to compare FETs with each other

→ Narrowband equivalence between (series RC) and (parallel RC) circuit at the FET input

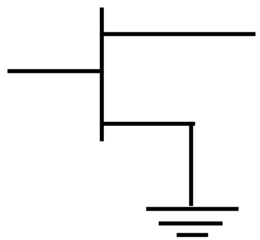


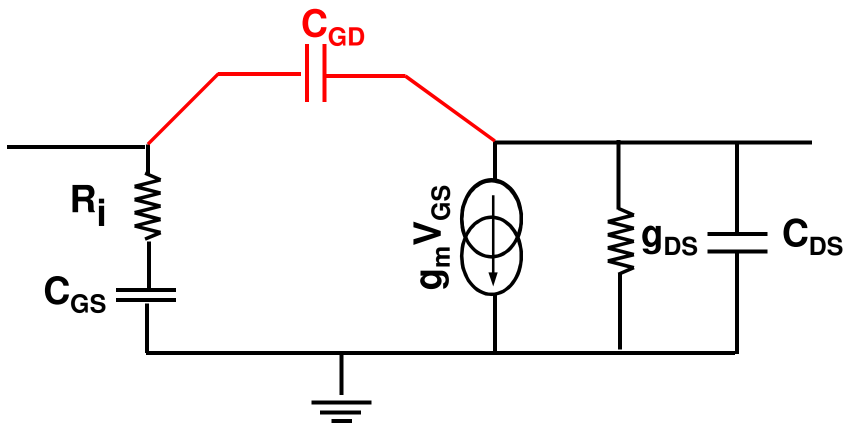




$$\boxed{G_{IN}(\omega) = R_i\, C_{GS}^2\, \omega^2}$$

# II – Intrinsic figures of merit for FETs

**3) Miller Effect** (Feedback admittance $Y_R$ and conductance load $G_L$)



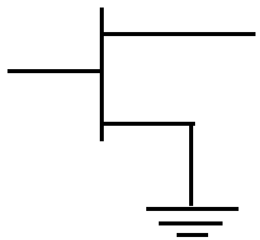


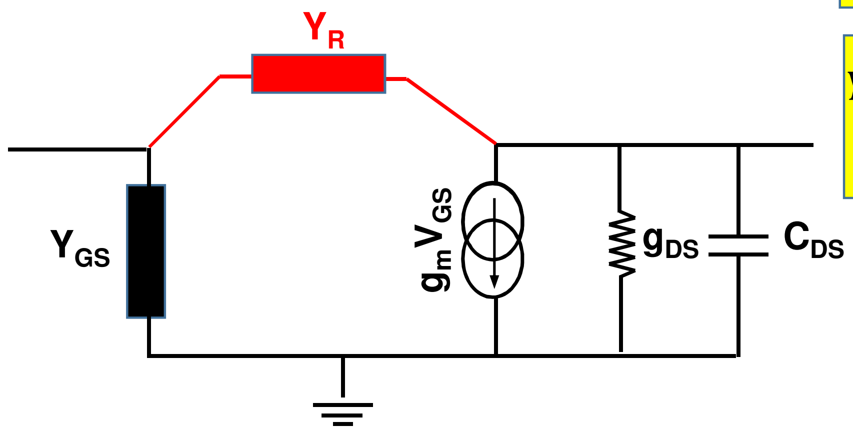
# II – Intrinsic figures of merit for FETs

**3) Miller Effect** (Feedback admittance $Y_R$ and conductance load $G_L$)

$$Y_R = j\, C_{GD}\omega$$

$$Y_{GS} = \frac{1}{R_i + \frac{1}{jC_{GS}\omega}}$$





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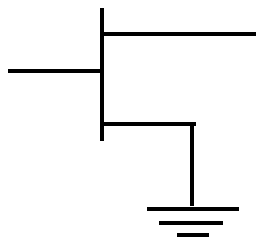
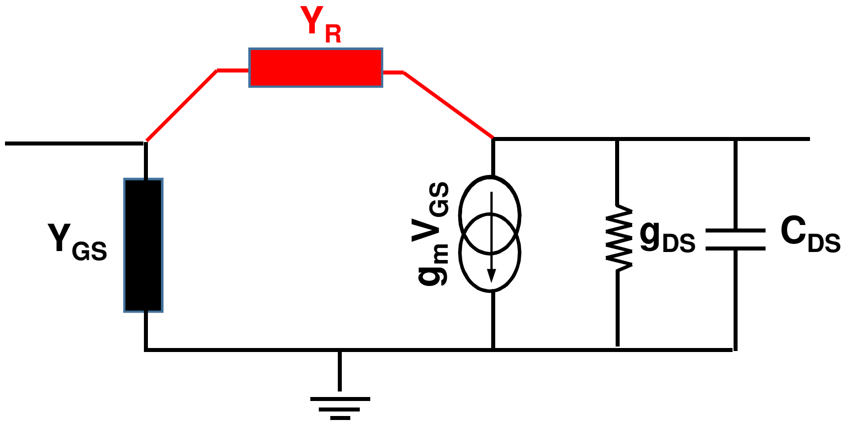
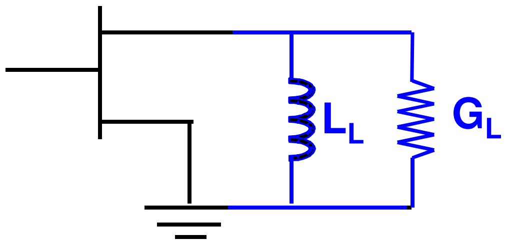
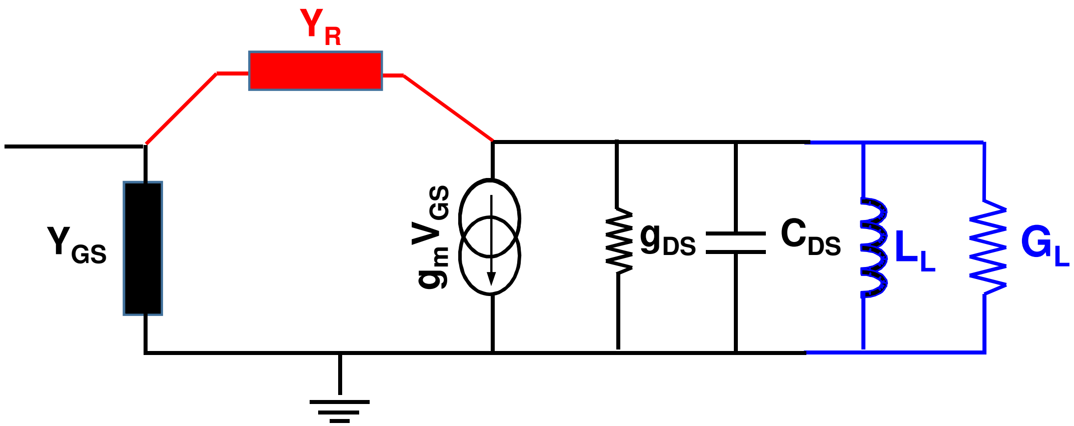




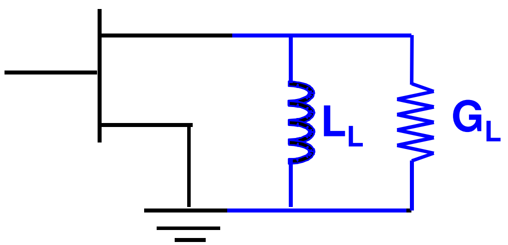



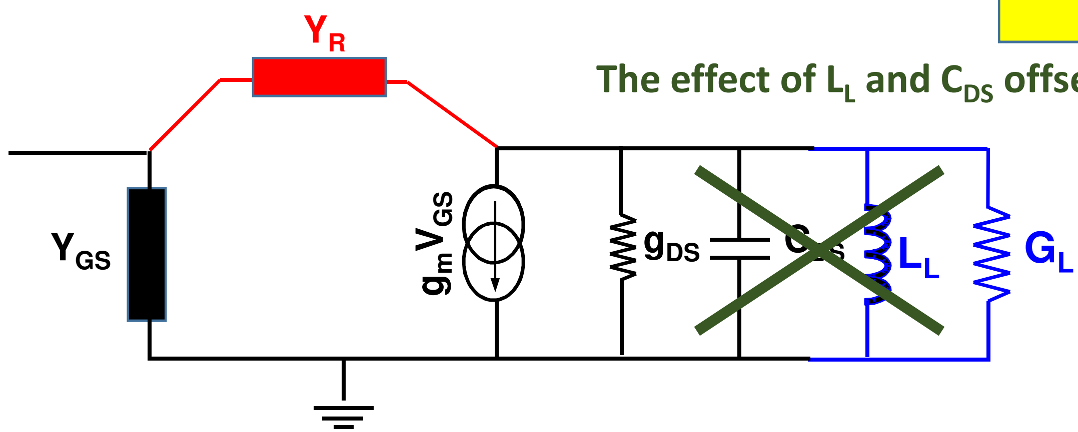
# II – Intrinsic figures of merit for FETs

**3) Miller Effect** (Feedback admittance $Y_R$ and conductance load $G_L$)

$$L_L\, C_{DS}\, \omega_o^2 = 1 \;\rightarrow\; \boxed{L_L = \frac{1}{C_{DS}\omega_o^2}}$$

The effect of $L_L$ and $C_{DS}$ offset each other



# II – Intrinsic figures of merit for FETs

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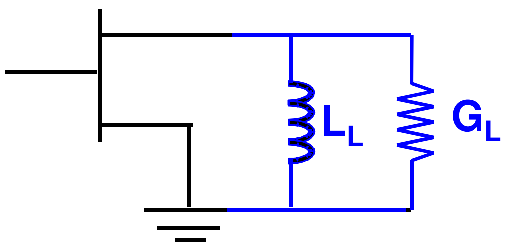


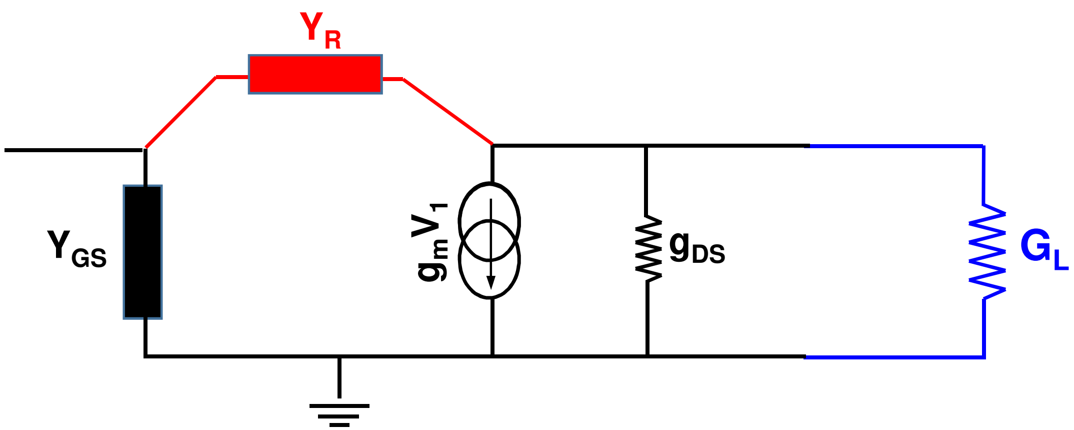

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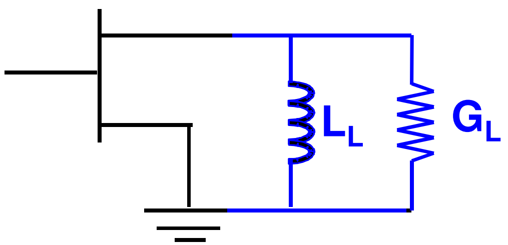
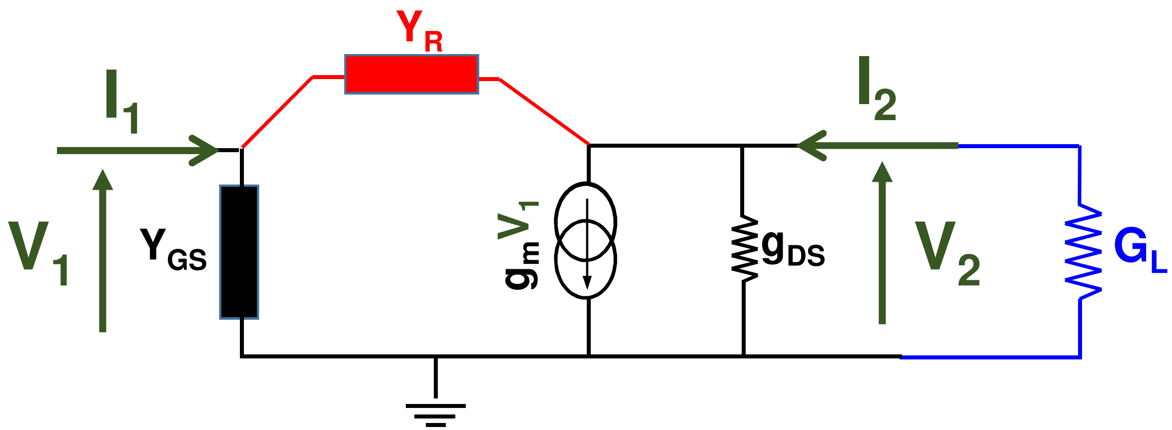
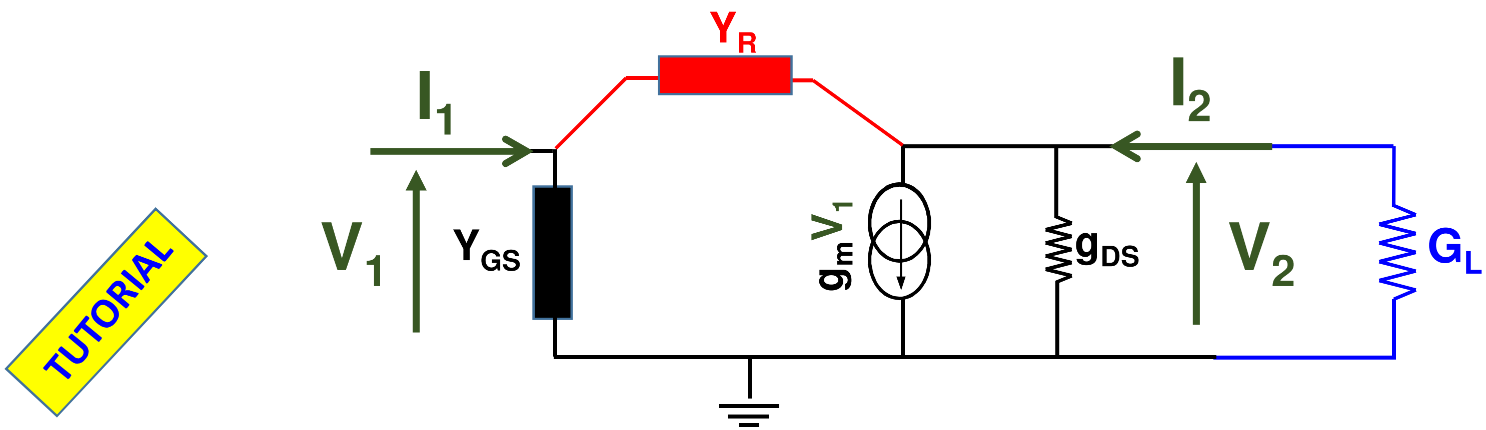


# II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance $Y_R$ and conductance load $G_L$)
   a) Voltage gain $G_V$

$$G_V = \frac{V_2}{V_1} = -\frac{g_m - Y_R}{g_{DS} + G_L + Y_R} \rightarrow -\frac{g_m}{g_{DS} + G_L} \rightarrow -\frac{g_m}{2g_{DS}}$$



# II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance $Y_R$ and conductance load $G_L$)

b) Input admittance $Y_{IN}$

$$Y_{IN} = \frac{I_1}{V_1} = Y_{GS} + Y_R[1 - G_V]$$

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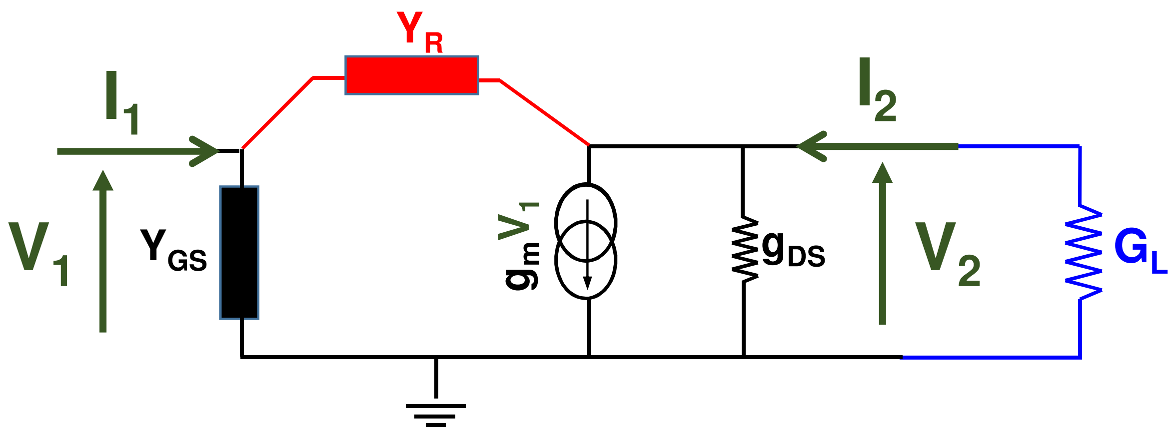
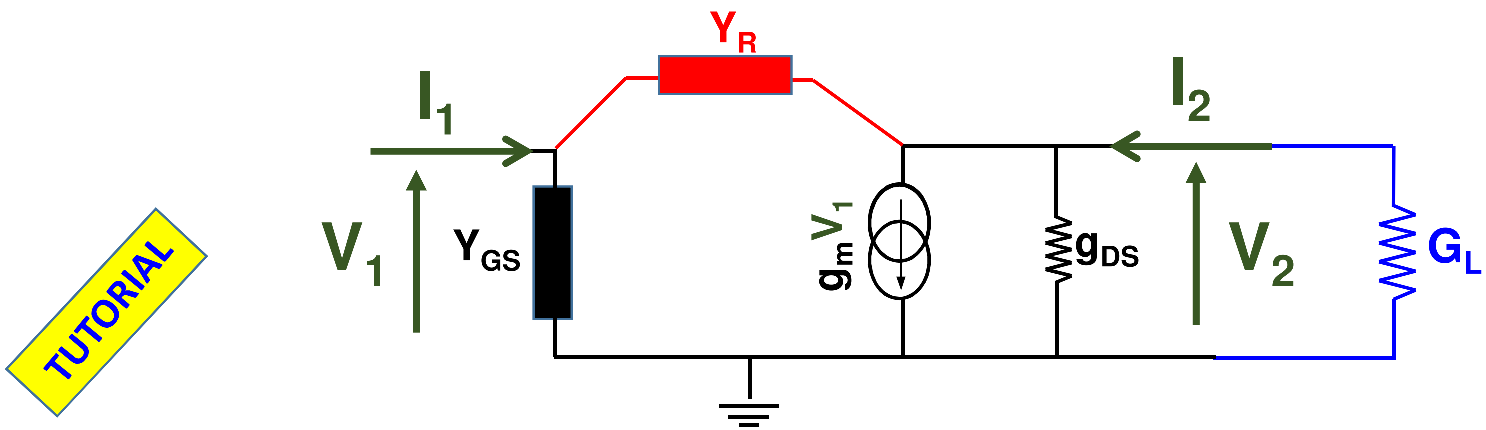


# II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance $Y_R$ and conductance load $G_L$)

c) Output admittance seen by the drain current source $Y_{OUT}$

$$Y_{OUT} = \frac{-g_m V_1}{V_2} = g_{DS} + G_L + Y_R\left[1 - \frac{1}{G_V}\right]$$



# II – Intrinsic figures of merit for FETs

$G_V<0$ and $|G_V|>>1$

3) Miller Effect (Feedback admittance $Y_R$ and conductance load $G_L$)

b) Input admittance $Y_{IN}$

$$Y_{IN} = Y_{GS} + Y_R[1 - G_V] \rightarrow \boxed{Y_{GS} + Y_R|G_V|}$$

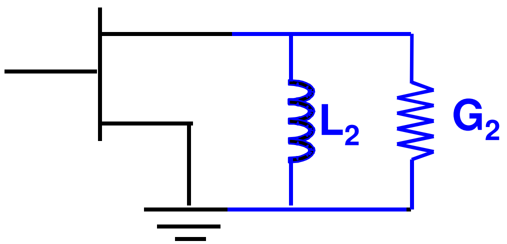
c) Output admittance seen by the drain current source $Y_{OUT}$

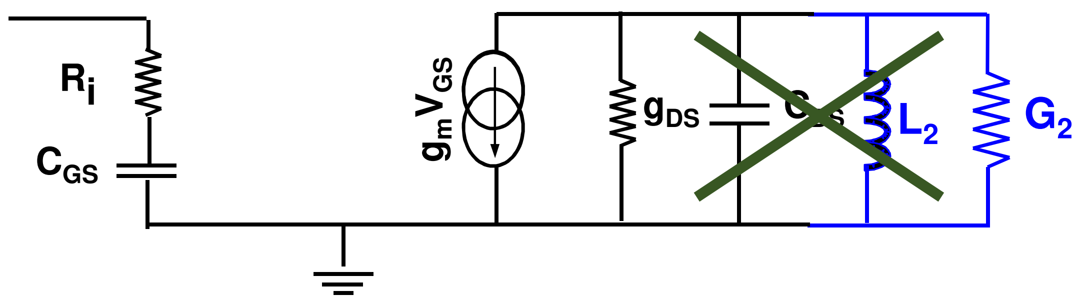
$$Y_{OUT} = g_{DS} + G_L + Y_R\left[1 - \frac{1}{G_V}\right] \rightarrow \boxed{g_{DS} + G_L + Y_R}$$

# II – Intrinsic figures of merit for FETs

3) Maximum Power Gain $\mathbf{G_{MAX}}$ → Simplified Electrical Small-Signal FET Model

$$L_2\, C_{DS}\, \omega^2 = 1 \quad \rightarrow \quad \boxed{L_2 = \frac{1}{C_{DS}\omega^2}}$$



# II – Intrinsic figures of merit for FETs

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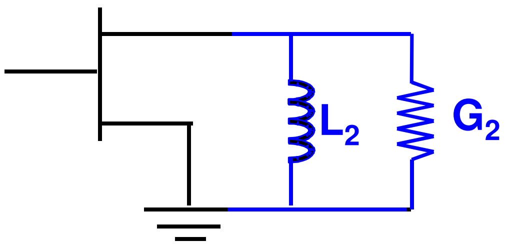
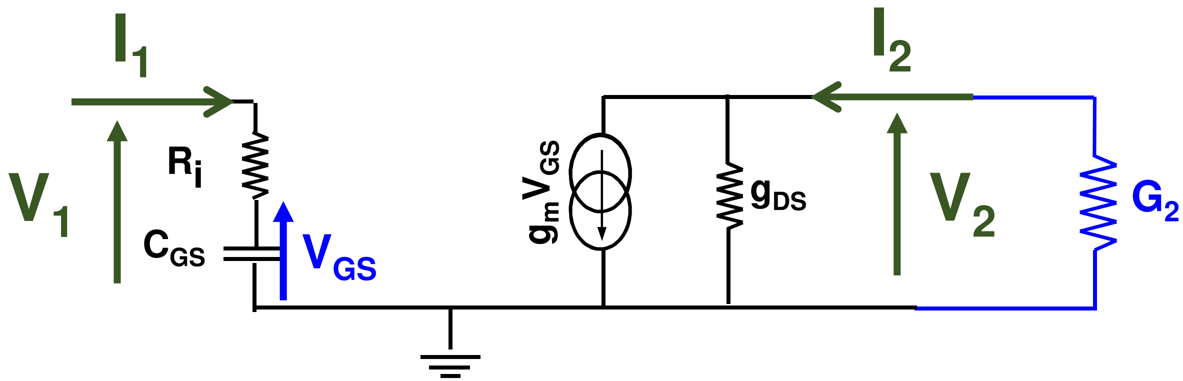
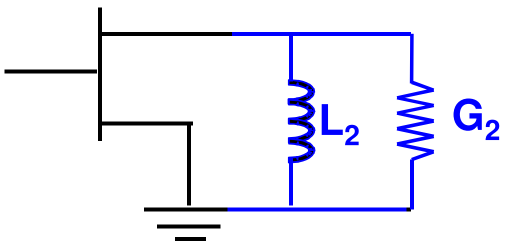
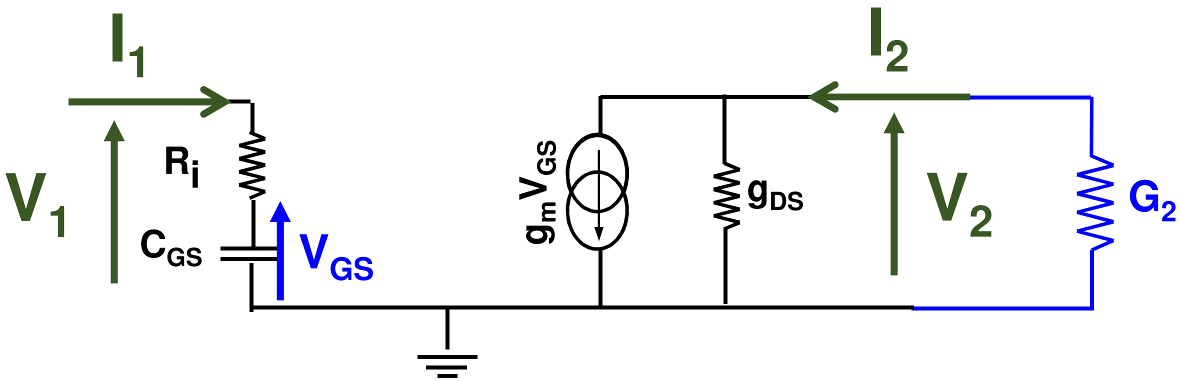


# II – Intrinsic figures of merit for FETs

3) Maximum Power Gain $\mathbf{G_{MAX}}$ → Simplified Electrical Small-Signal FET Model

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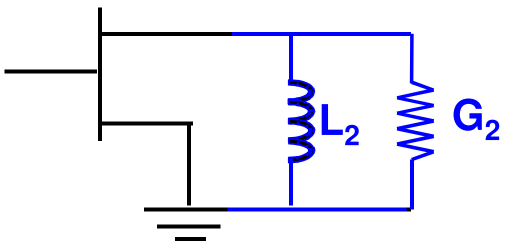
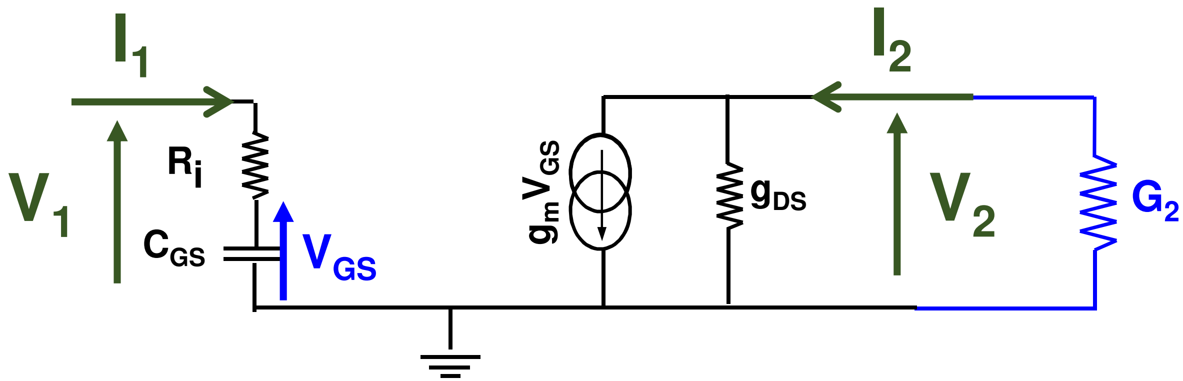
**<u>General case</u>** $(G_2 \neq g_{DS})$ → Not maximum Power Gain $\mathbf{G_P}$

$$G_P = \frac{\dfrac{G_2}{[G_2 + g_{DS}]^2}\ g_m^2}{R_i\ C_{GS}^2\ \omega^2}$$

# II – Intrinsic figures of merit for FETs

3) Maximum Power Gain $G_{MAX}$ → Simplified Electrical Small-Signal FET Model

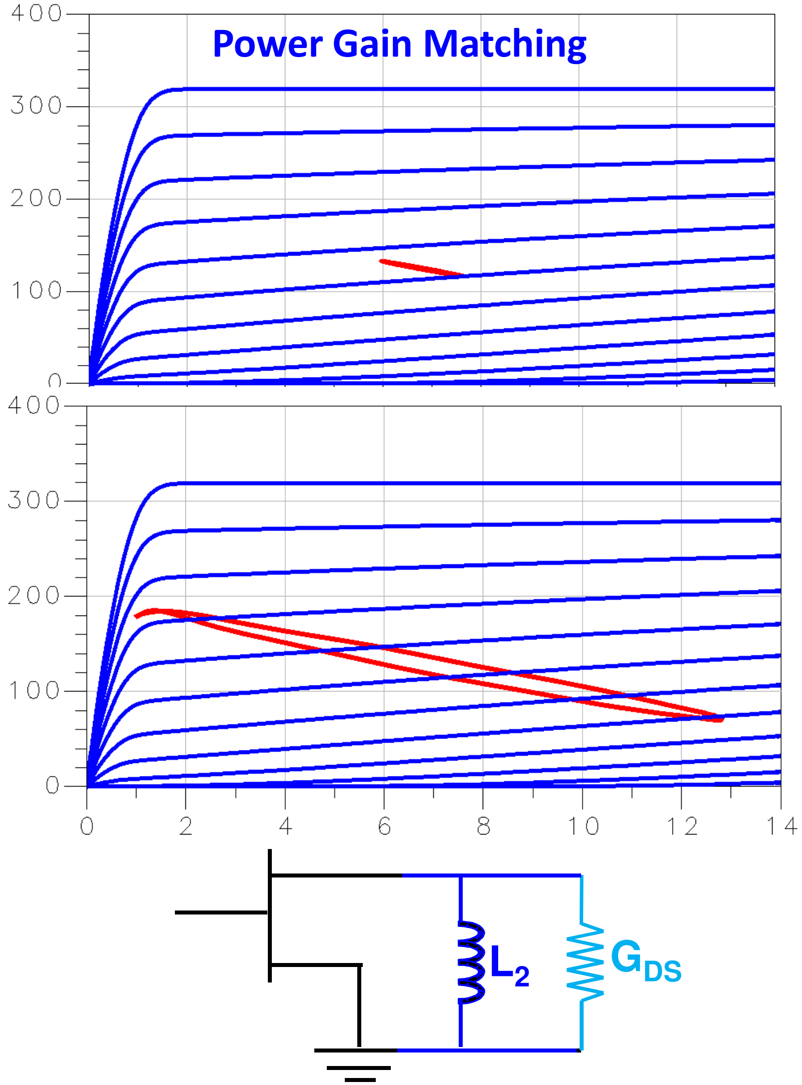


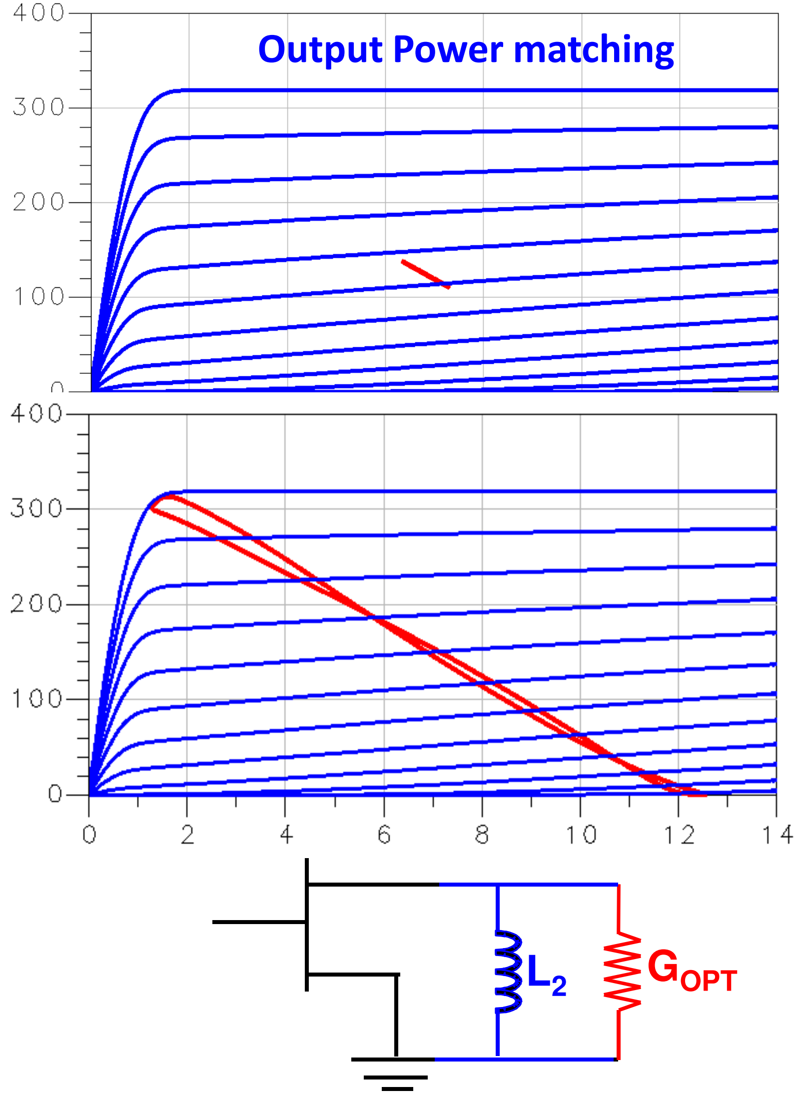



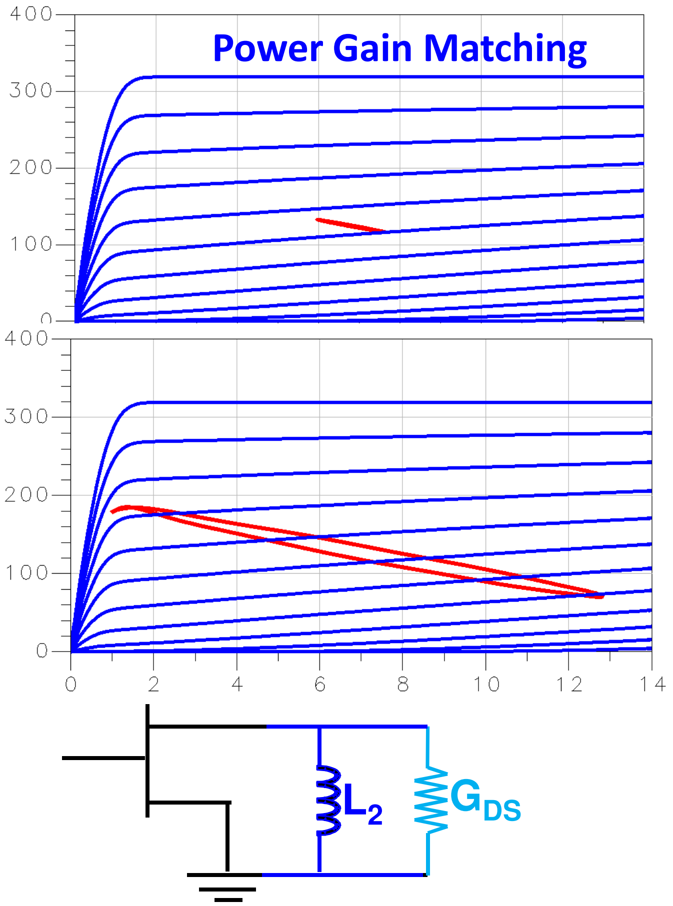

TUTORIAL

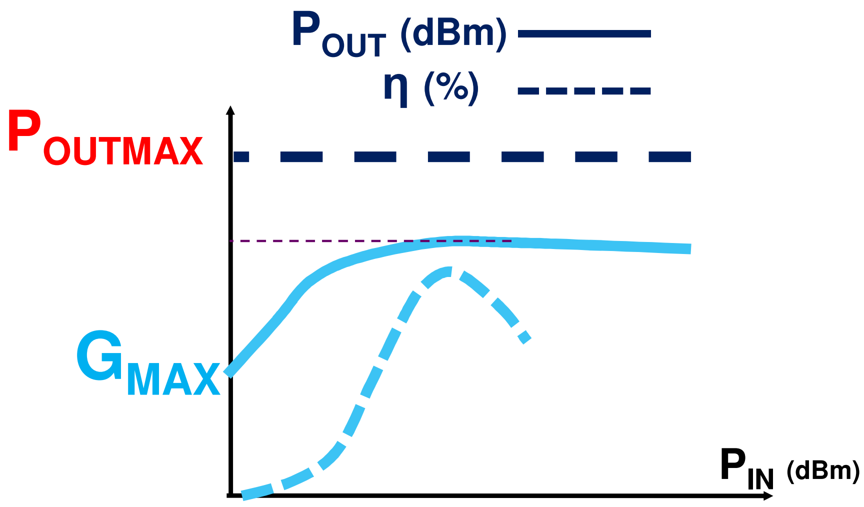
**Optimum case** $(G_2 = g_{DS})$ → Not maximum Power Gain $G_{max}$

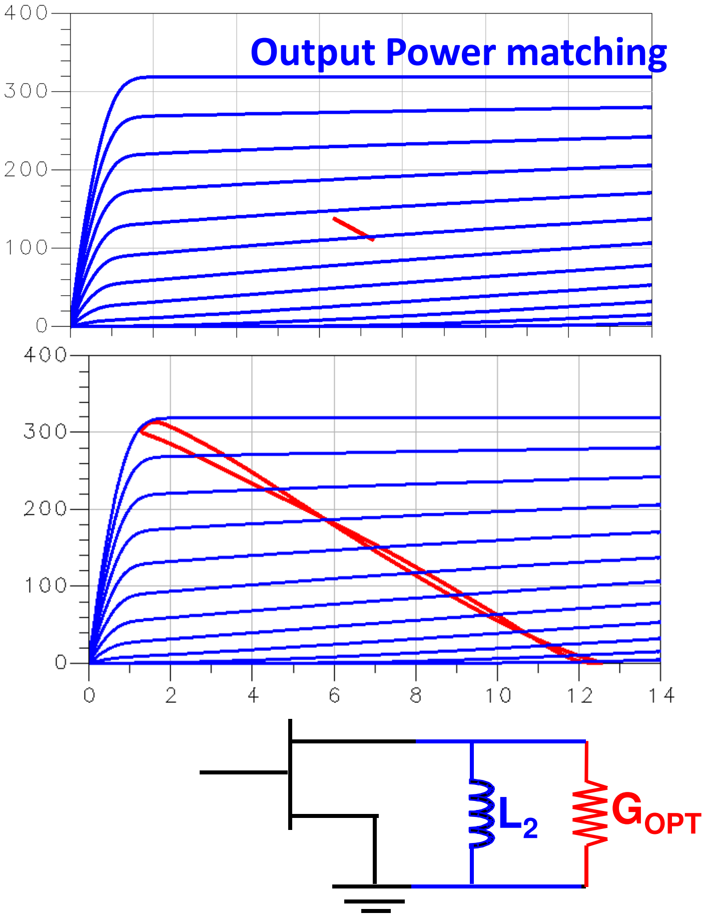
$$G_{max} = \frac{g_m^2}{4\, g_{DS}\, R_i\, C_{GS}^2\, \omega^2}$$

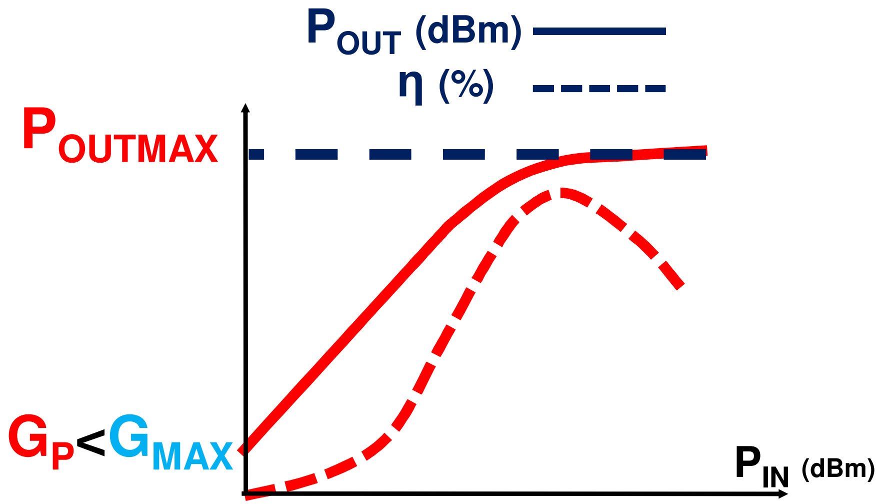

Power Gain Matching
400
300
200
100
0
0
2
4
6
8
10
12
14
L2
GDS


Output Power matching
400
300
200
100
0
0
2
4
6
8
10
12
14
L2
GOPT


Power Gain Matching
400
300
200
100
0
400
300
200
100
0
0
2
4
6
8
10
12
14
L2
GDS

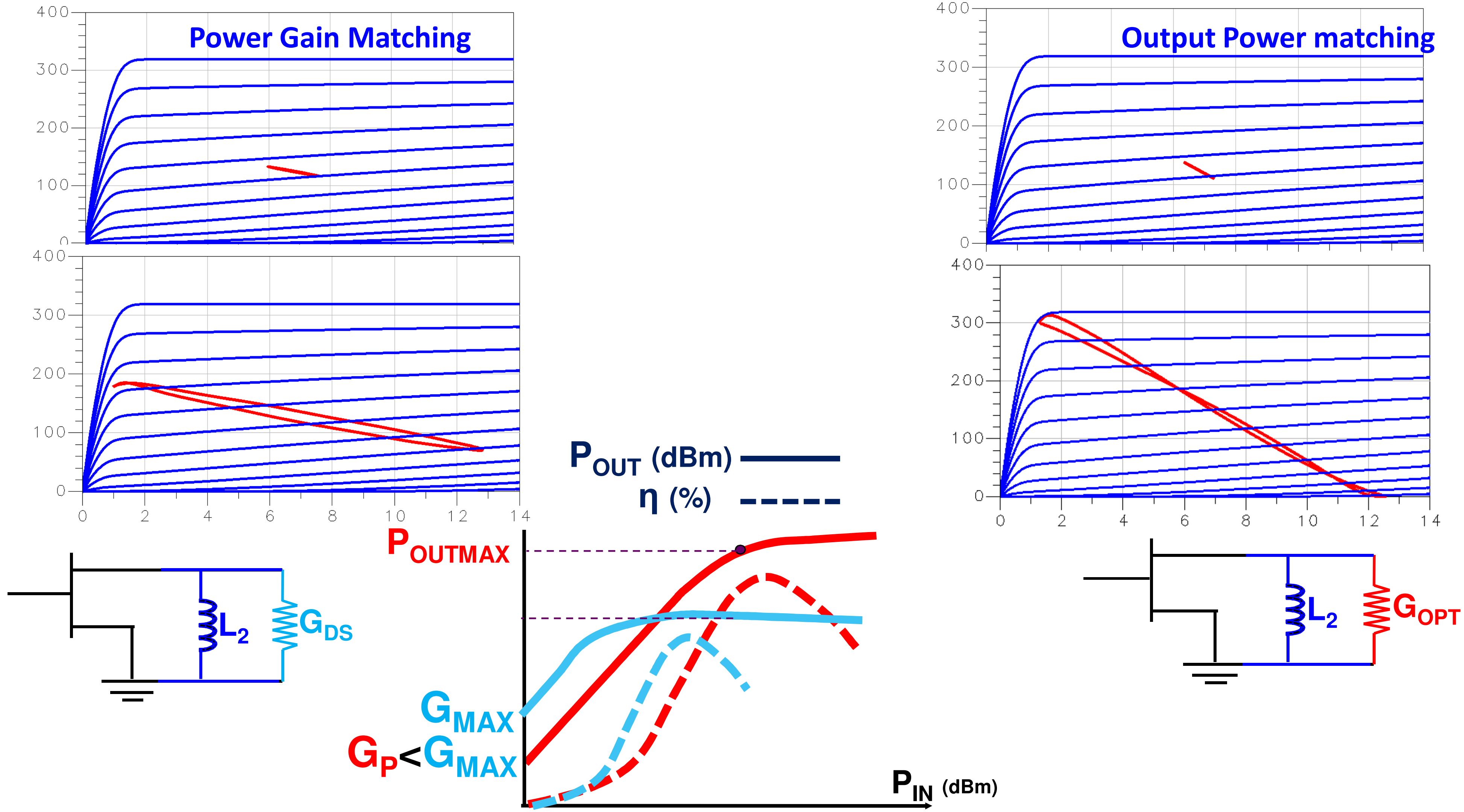

POUT (dBm)
η (%)
POUTMAX
GMAX
PIN (dBm)


Output Power matching
400
300
200
100
0
400
300
200
100
0
0
2
4
6
8
10
12
14
L2
GOPT


POUT (dBm)
η (%)
POUTMAX
GP<GMAX
PIN (dBm)

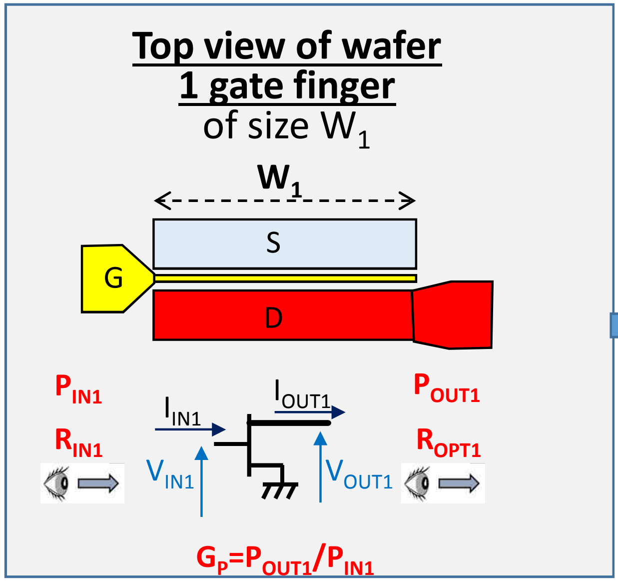
# EMIMEO

# E(rasmus) Mundus on Innovative Microwave Electronics and Optics



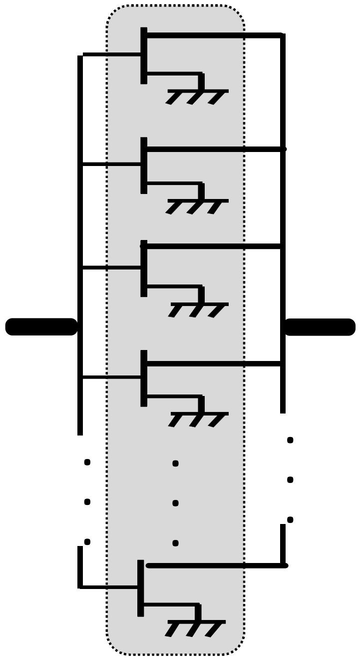
# Power combination (Power Bars) and power matching

## Illustration of critical issues in power matching

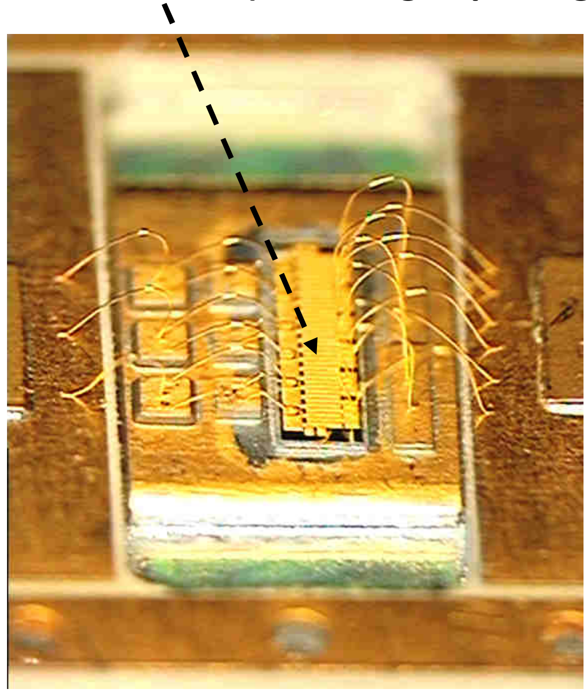



Increase device size to increase power

Power bar (n // devices)

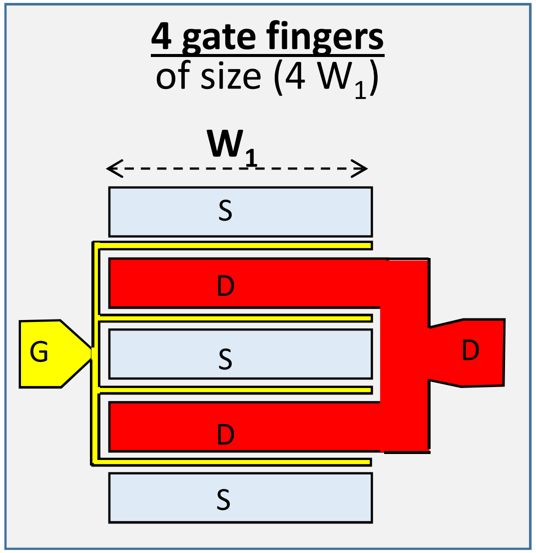


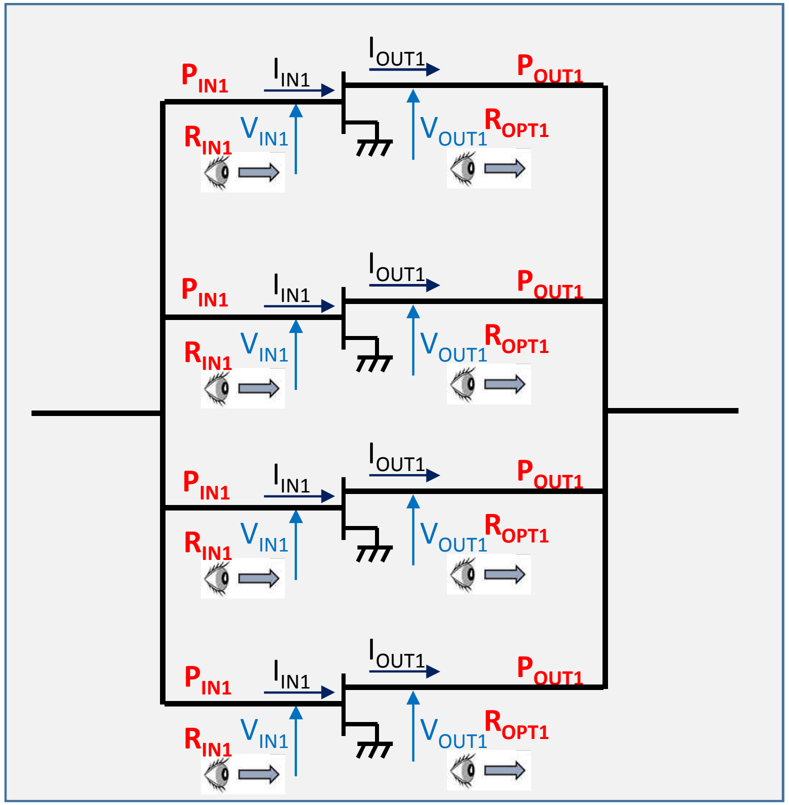
Power bar (matching in package)



# Power combination (Power Bars) and power matching

- Illustration of critical issues in power matching

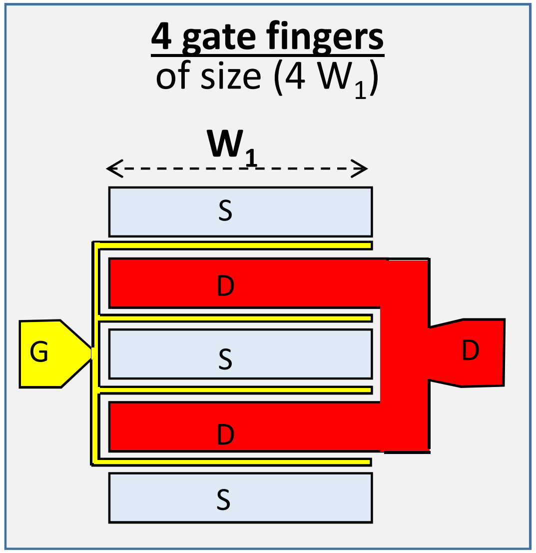


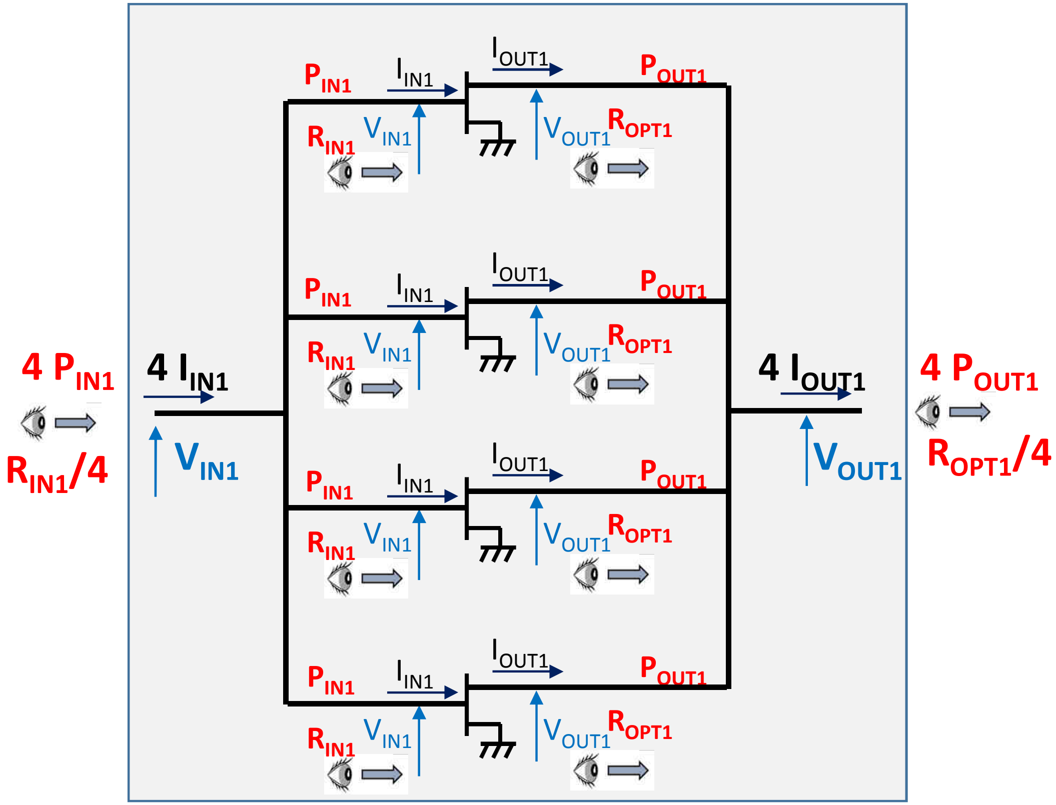




**Device size** = Total gate width = (N° of // gates) $\times$ (gate width) = **4** $\times$ $\mathbf{W_1}$

# Power combination (Power Bars) and power matching

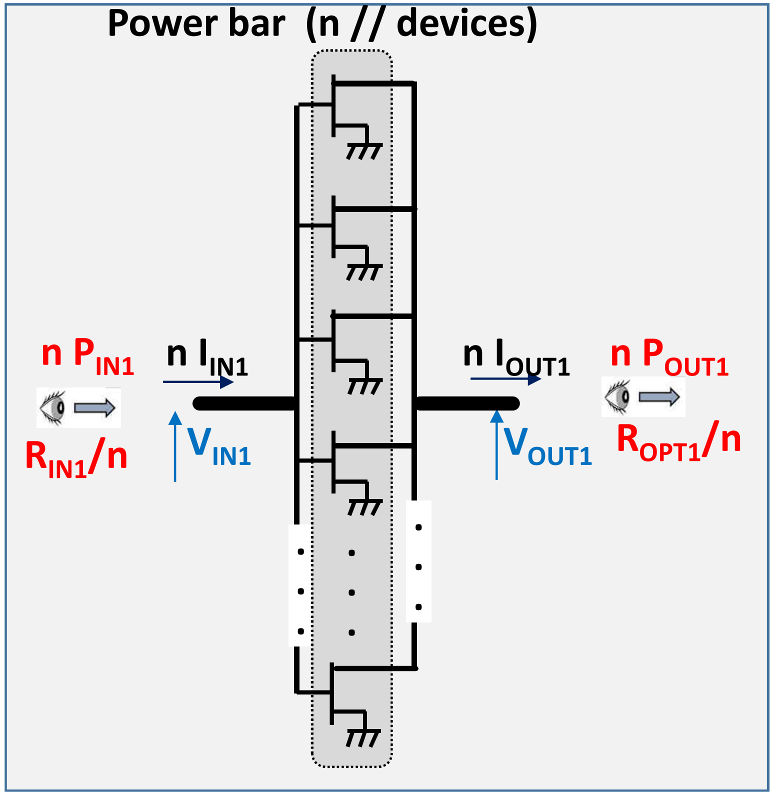
- Illustration of critical issues in power matching



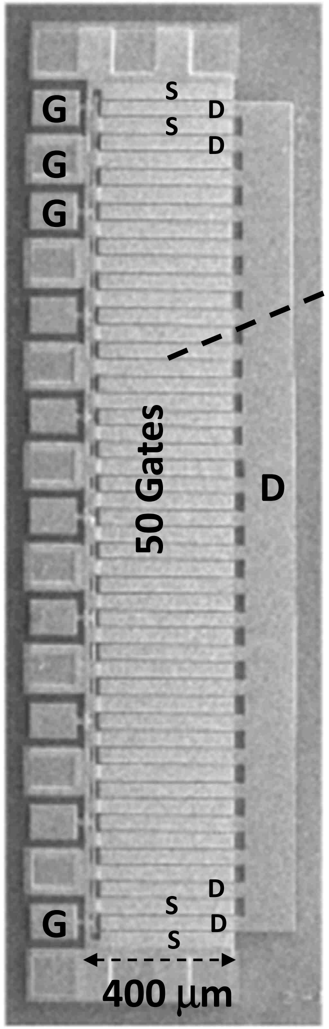



# Power combination (Power Bars) and power matching

- Illustration of critical issues in power matching




20 mm GaN HEMT die




**Device Size**
=
Total Gate Width
=
(N° of // gates) x (Gate width)
=
50 x 400 µm = **20 mm**

**Scaling Rules:**

- **Drain Current**
  $I_{DS}$ (mA/mm)
- **Voltages**
  $V_{GS}$ and $V_{DS}$ (V)
- **Output Power**
  $P_{OUT}$ (W/mm)
- **Optimum Output Load**
  $R_{OPT}$ (Ω . mm)

# Main transmission lines and Passive elements used in MMIC designs

## MMIC (Monolithic Microwave and Millimeterwave Integrated Technology)

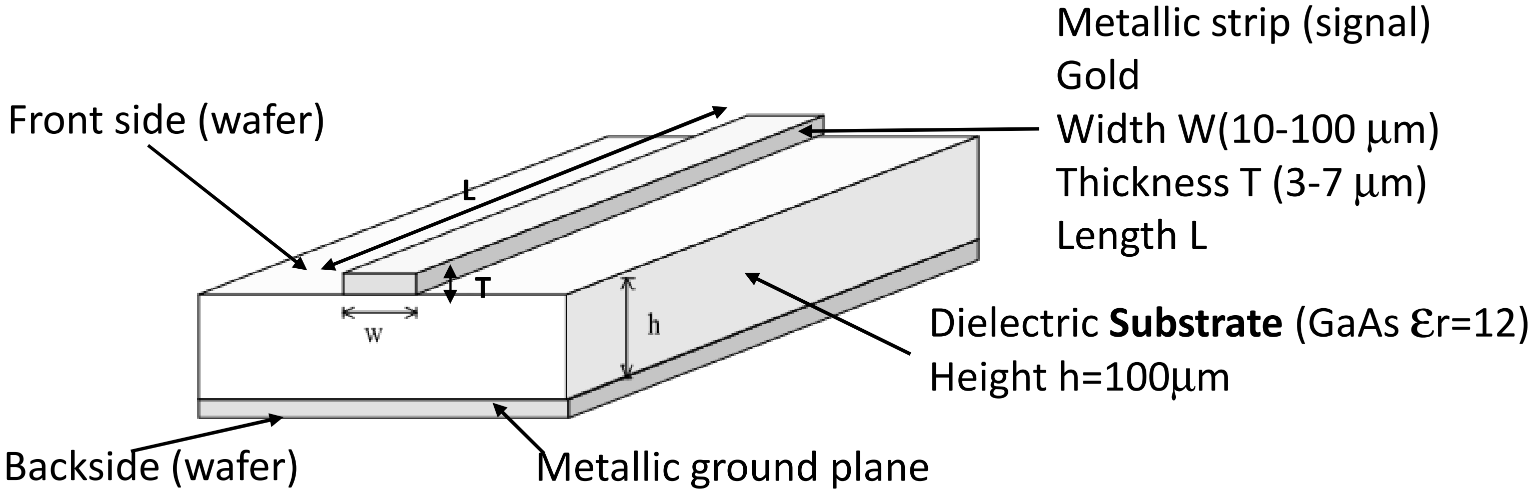
- Recall on Transmission lines

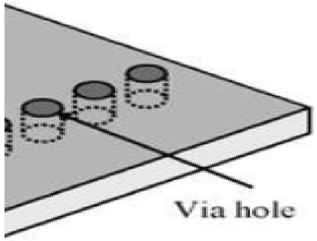
- Microstrip inductors/capacitors/resistors

- Harmonic loading and bias using $\lambda/4$ lines

- Matrix chain of a line and impedance transformation

# Microstrip lines



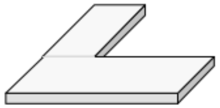




- Requirement of **metallized via holes** through the substrate to connect electrical elements from the front side to the metallic ground plane
  → expensive backside process after the front side process ☹
  → easier design of the signal paths on the front side when compared to coplanar
  → the most effective integrated technology at high frequencies ☺

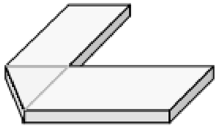
# Microstrip lines

In order to drive the signal, these are some of the main shapes of line connections

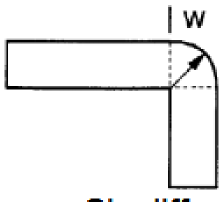
CORNER



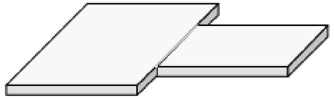
BEND



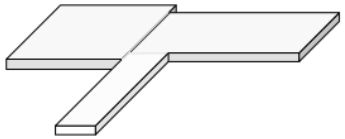
ROUND



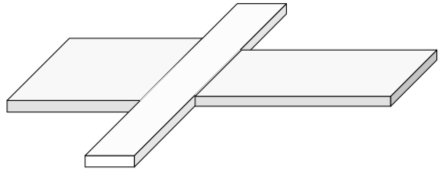

STEP (change of Zc)



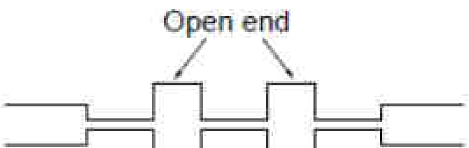
TEE junction (3 lines)



CROSS junction (4 lines)

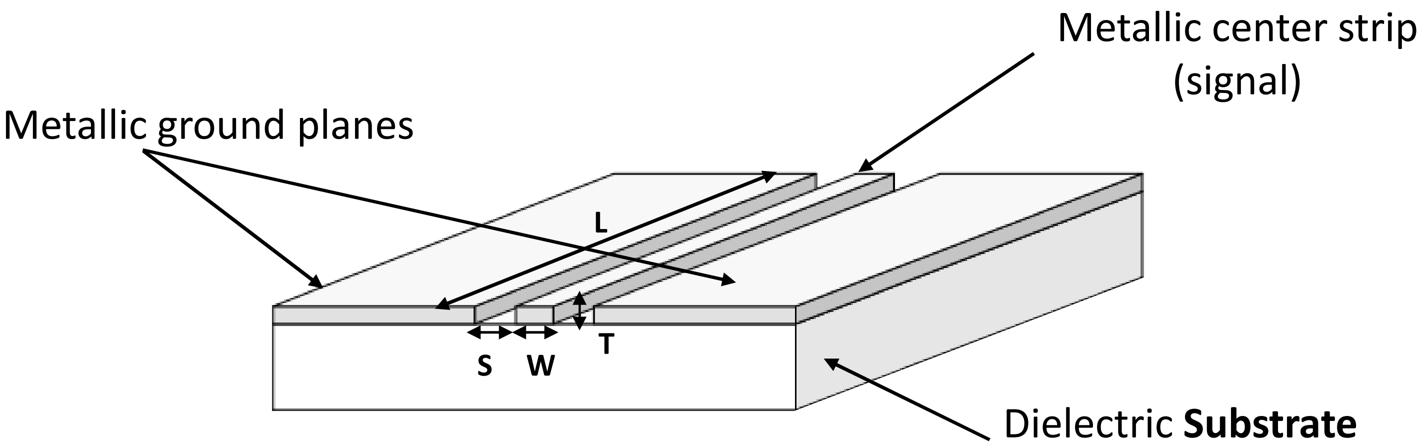


In order to design passive circuits→ Narrow Lines (Inductive) Wide Lines (Capacitive)




Microstrip Low Pass Filter

# Coplanar lines



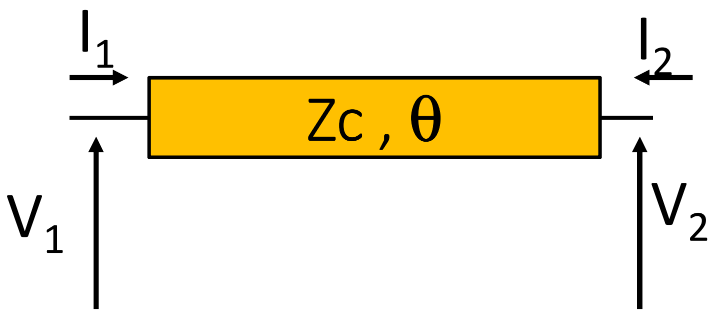

- No requirement of metallized via holes through the substrate to connect electrical elements from the front side to the metallic ground plane
  - → no expensive backside process after the front side process
  - → complex design of the signal paths on the front side
  - → lower performances than microstrip designs

# Line = Matrix chain

Propagation constant $\Gamma = \alpha + j\,\beta$ → Attenuation constant $\alpha$ and Phase constant $\beta$

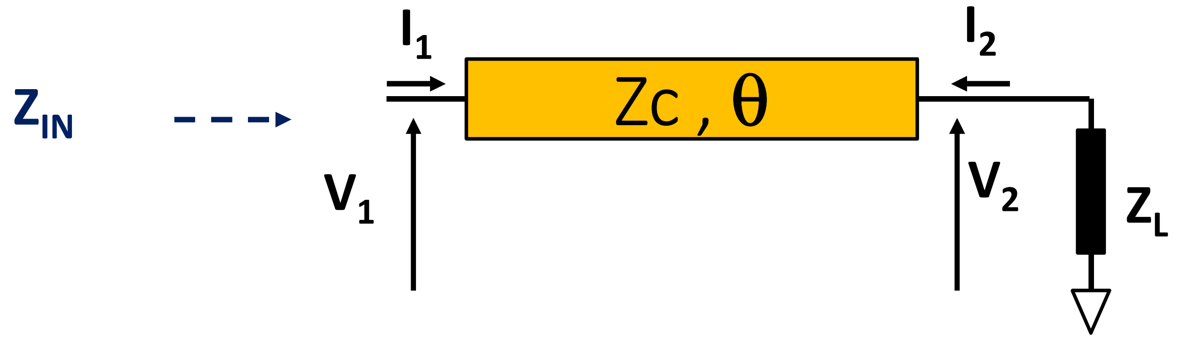
$\beta = 2\pi/\lambda$

$\theta = \beta\, L$




$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} cos(\theta) & jZ_C sin(\theta) \\ jsin(\theta)/Z_C & cos(\theta) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

# Equivalent input impedance of a loaded line



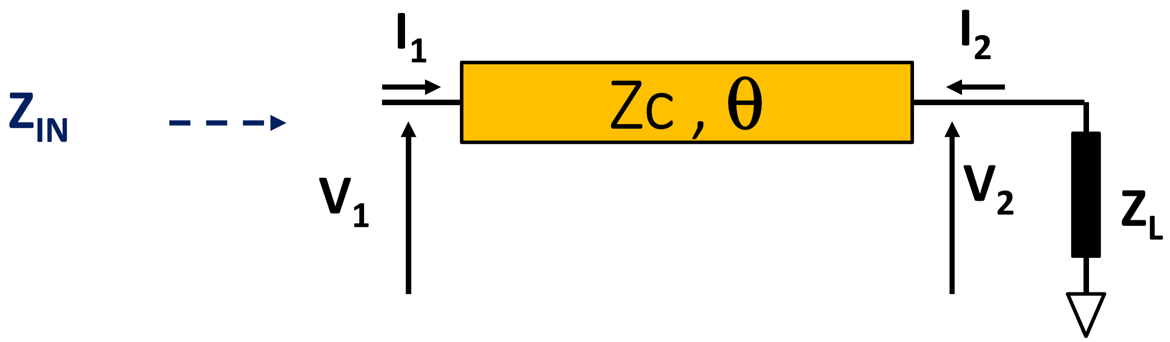

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_C\sin(\theta) \\ j\sin(\theta)/Z_C & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

$$V_2 = -Z_L I_2$$

$$\mathbf{Z_{IN}} = \frac{V_1}{I_1} = \frac{\cos(\theta)\,V_2 - jZ_C\sin(\theta)I_2}{\left(\frac{j\sin(\theta)}{Z_C}\right)V_2 - \cos(\theta)\,I_2} = \frac{\cos(\theta)\,(-Z_L I_2) - jZ_C\sin(\theta)I_2}{\left(\frac{j\sin(\theta)}{Z_C}\right)(-Z_L I_2) - \cos(\theta)\,I_2}$$

$$\mathbf{Z_{IN}} = \frac{\cos(\theta)\,(Z_L) + jZ_C\sin(\theta)}{\left(\frac{j\sin(\theta)}{Z_C}\right)(Z_L) + \cos(\theta)} = \mathbf{Z_C}\,\frac{\mathbf{Z_L\cos(\theta) + jZ_C\sin(\theta)}}{\mathbf{jZ_L\sin(\theta) + Z_C\cos(\theta)}}$$

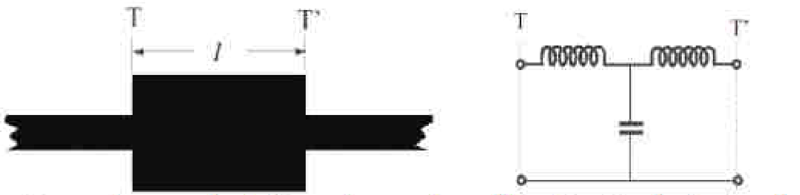
# Equivalent input impedance of λ/4 and λ/2 loaded lines




$$\boldsymbol{Z_{IN}} = \mathrm{Z_C}\,\frac{\mathrm{Z_L}\cos(\theta) + j\mathrm{Z_C}\sin(\theta)}{j\mathrm{Z_L}\sin(\theta) + \mathrm{Z_C}\cos(\theta)}\begin{cases} if\ \boxed{\boldsymbol{L} = \dfrac{\lambda}{\boldsymbol{4}}} \rightarrow \boldsymbol{\theta} = \dfrac{2\pi L}{\lambda} = \dfrac{\pi}{\boldsymbol{2}} \rightarrow \boxed{\boldsymbol{Z_{IN}} = \dfrac{\boldsymbol{Z_C^2}}{\boldsymbol{Z_L}}} \text{ Impedance inverter} \\ if\ \boxed{\boldsymbol{L} = \dfrac{\lambda}{\boldsymbol{2}}} \rightarrow \boldsymbol{\theta} = \dfrac{2\pi L}{\lambda} = \pi \rightarrow \boxed{\boldsymbol{Z_{IN}} = \boldsymbol{Z_L}} \end{cases}$$

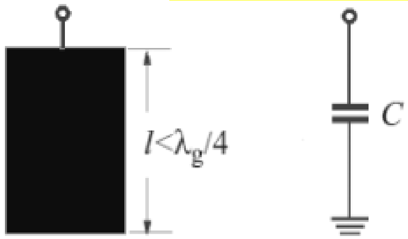
# High- and Low-impedance short lines (Inductive or capacitive)


High-impedance short-line element and the Equivalent circuit

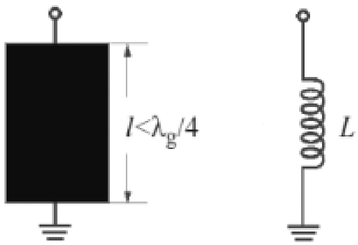



Low-impedance short-line element and the Equivalent circuit

# Open and short-circuited stubs

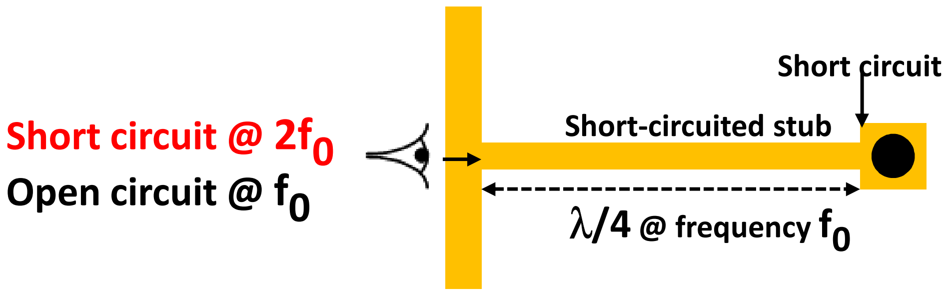


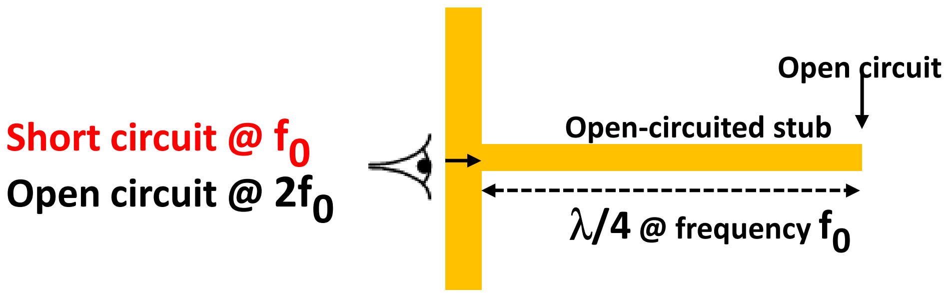

Open-Circuited Stub



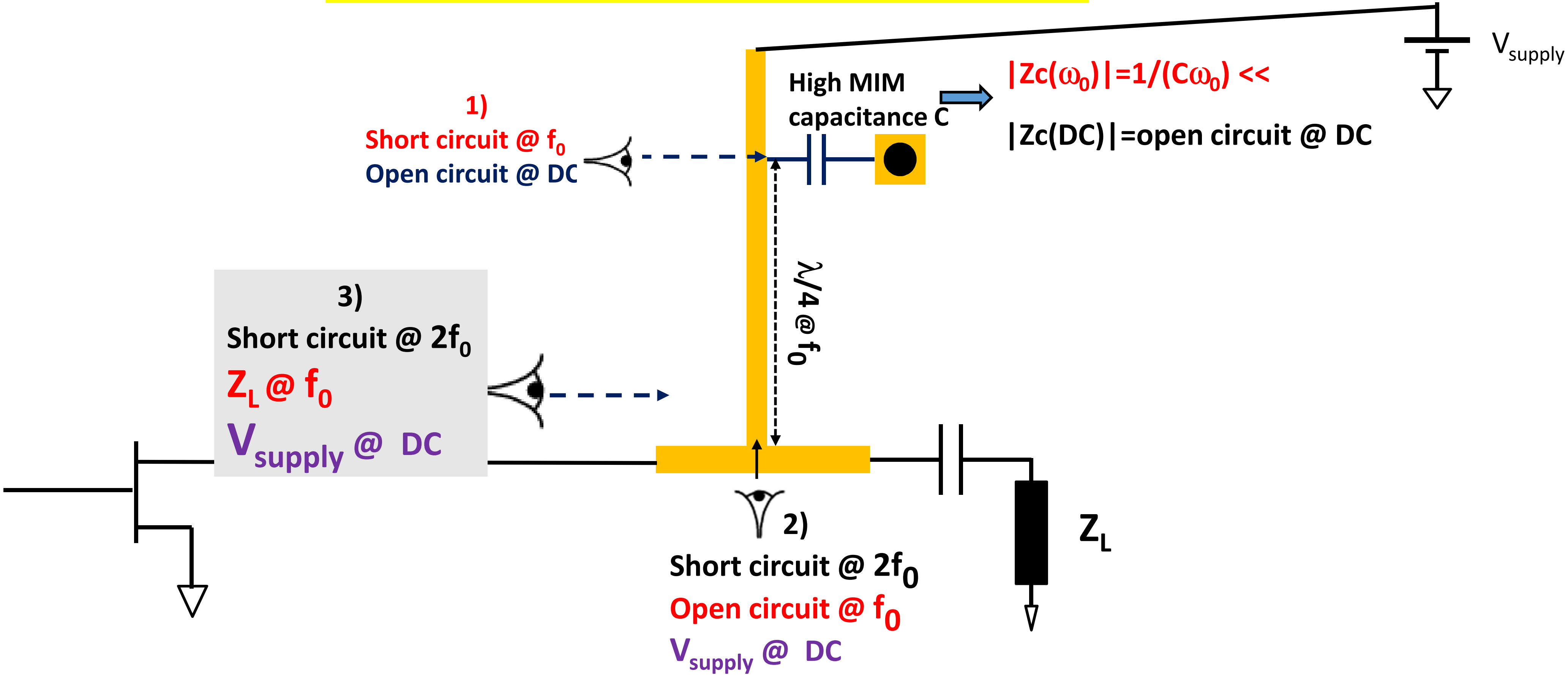

Short-Circuited Stub

# Narrowband Harmonic loading using quarter wavelength line ($\lambda/4$)



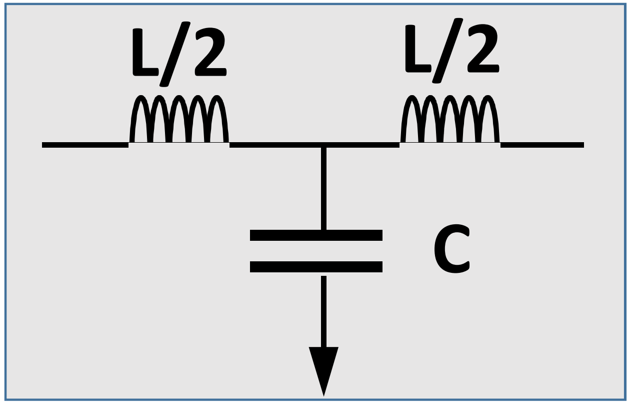
# Bias network decoupling using quarter wavelength line ($\lambda/4$)



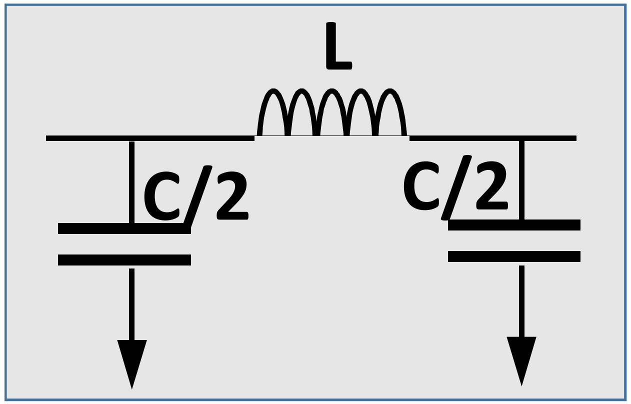
# Reminder = Electrical lumped equivalent (RLC) of transmission lines

# Electrical lumped equivalent (LC) of a lossless line (Zc, θ)


T cell




π cell

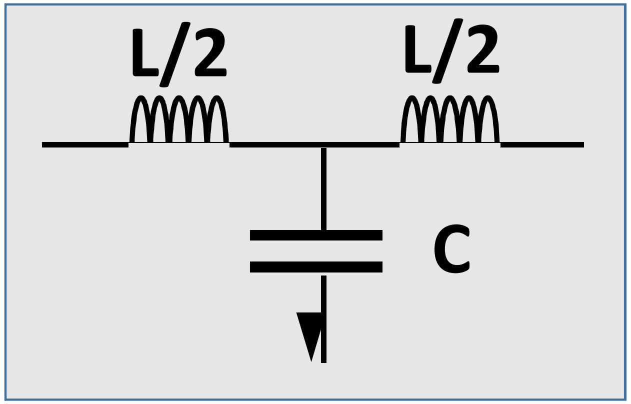


# Electrical lumped equivalent (LC) of a lossless line (Zc, θ)

**Cut-off frequency**

$$f_C = \frac{1}{\pi\sqrt{LC}}$$

**T cell**




**Characteristic Impedance**

$$Z_C = \sqrt{\frac{L}{C}}\sqrt{1-\left[\frac{f}{f_C}\right]^2}$$

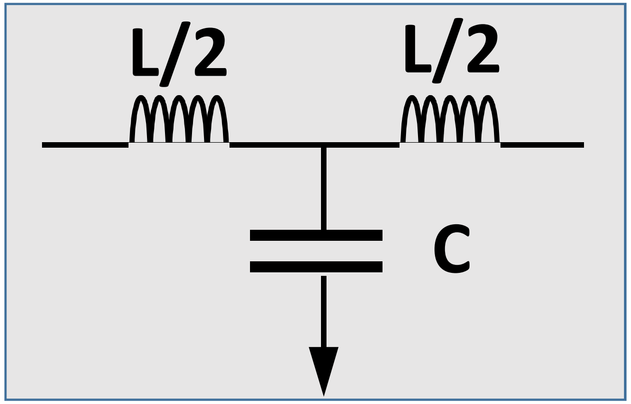
**Phase Shift**

$$\theta = \omega\sqrt{LC}\sqrt{1-\left[\frac{f}{f_C}\right]^2}$$

$$\sqrt{1-\left[\frac{f}{f_C}\right]^2} > 0.9 \iff f < 0.44\, f_C$$

# Electrical lumped equivalent (LC) of a lossless line (Zc, θ)


T cell




## Cut-off frequency

$$f_C = \frac{1}{\pi\sqrt{LC}}$$

## Characteristic Impedance

If f<<$f_C$ → $$Z_C \approx \sqrt{\frac{L}{C}}$$

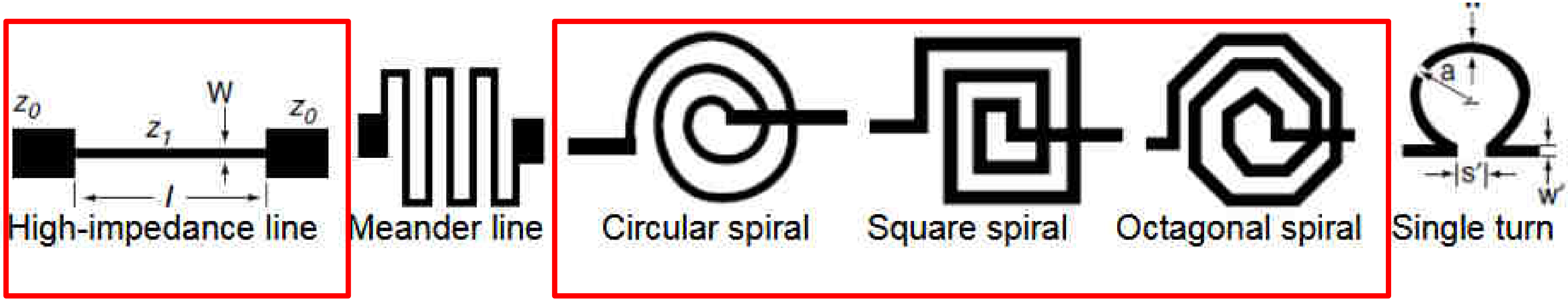
$f < 0.44\, f_C$

## Phase Shift

If f<<$f_C$ → $$\theta \approx \omega\sqrt{LC}$$

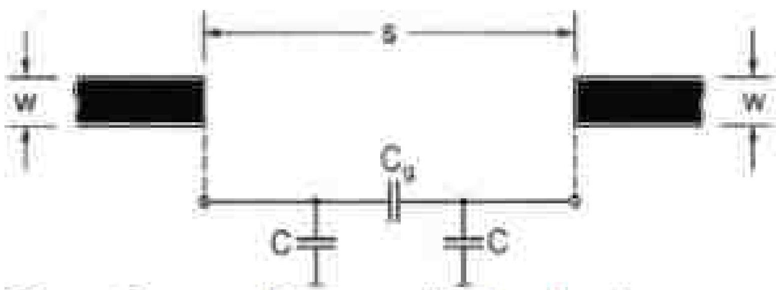
# Microstrip passive inductors, capacitors and resistors

# Microstrip Inductors

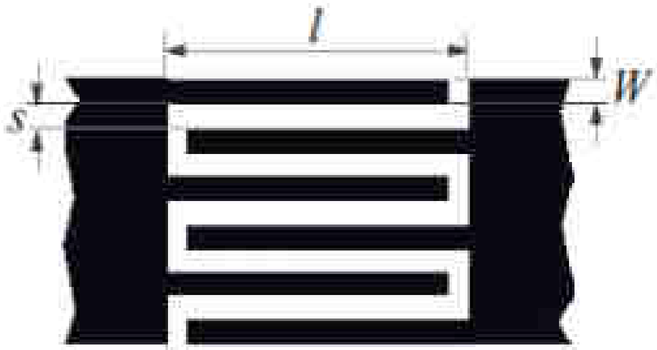



**Only used at lower frequencies up to 3-4GHz because of very high losses**
**Achievable values up to few nH**

# Microstrip Capacitors (MIM : Metal Insulator Metal)

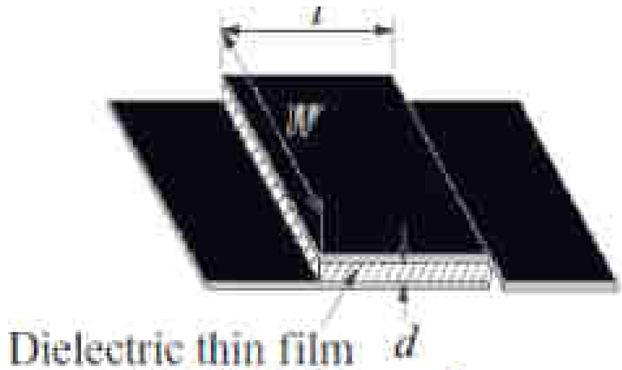



Gap Capacitor and Equivalency




Interdigital Capacitor

$SiO_2$




MIM Capacitor

$$C = \varepsilon \frac{S}{d} = \varepsilon \frac{l \times W}{d}$$

$$C = \frac{\varepsilon}{d}(l \times W)$$

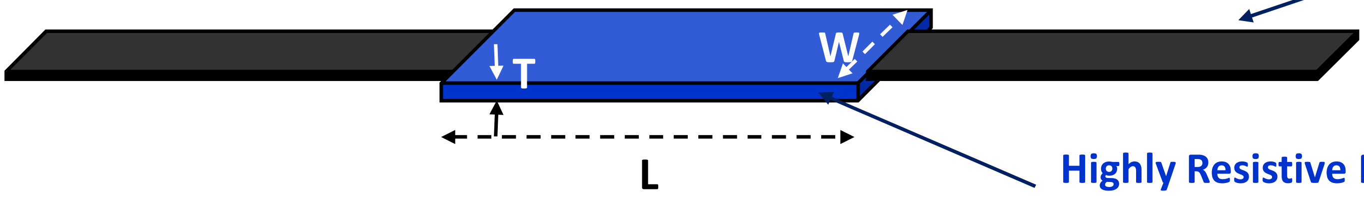
$$C = CD \times S$$

$$CD = \frac{\varepsilon}{d}$$

Capacitance density (F/m²)

Ex : 300 pF/mm²→ Achievable values 0.2pF→20pF

# Microstrip Resistors (TaN)




$$R = \rho_{TaN}\frac{L}{S} = \rho_{TaN}\frac{L}{T \times W}$$

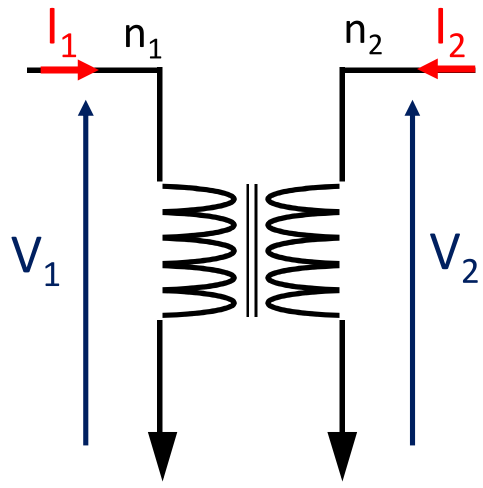
$$R = \frac{\rho_{TaN}}{T}\frac{L}{W} = R_S\frac{L}{W}$$

$$\boxed{R_S = \frac{\rho_{TaN}}{T}}$$

**Sheet resistance $R_S$ (Ω/sq)**
**(Ω/ )**

$$\boxed{R = R_S\frac{L}{W}}$$

# Reminder = Ideal Electrical transformers
# How are they realized at high frequencies ?



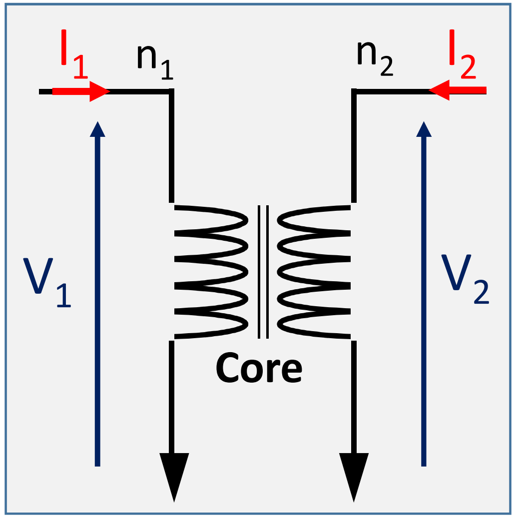
# Reminder = Ideal Electrical transformer

$$\boxed{\frac{V_2}{V_1} = \frac{n_2}{n_1}}$$

$$\boxed{\frac{I_2}{I_1} = -\frac{n_1}{n_2}}$$

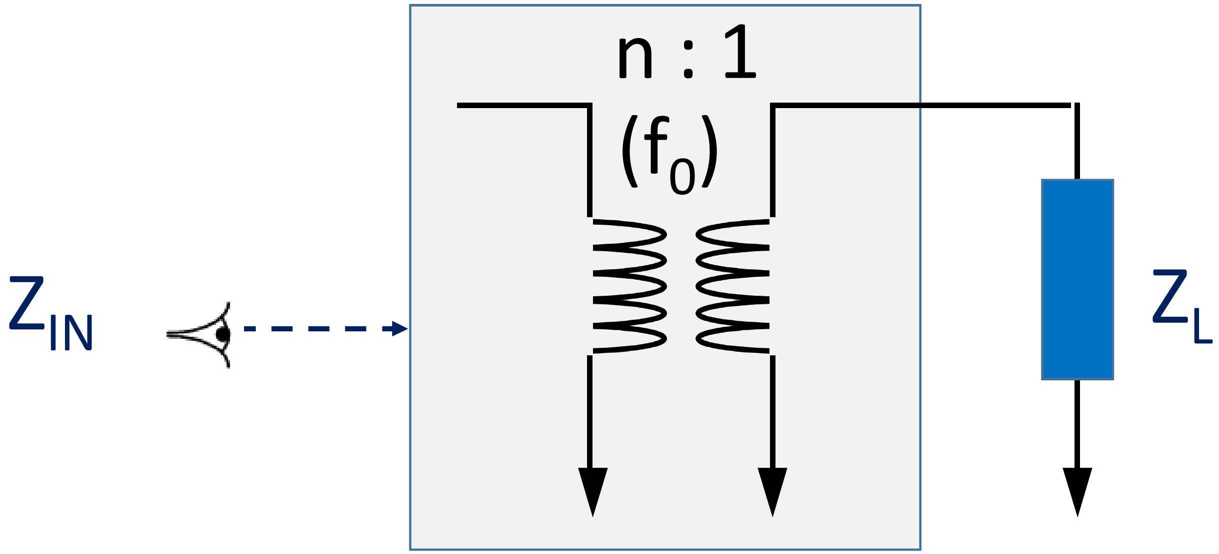
Conservation of energy

**Primary Winding (n1 turns)**




**Secondary Winding (n2 turns)**

# Reminder = Impedance transformation




Criterion

- Transformation ratio
- Bandwidth
- Technology

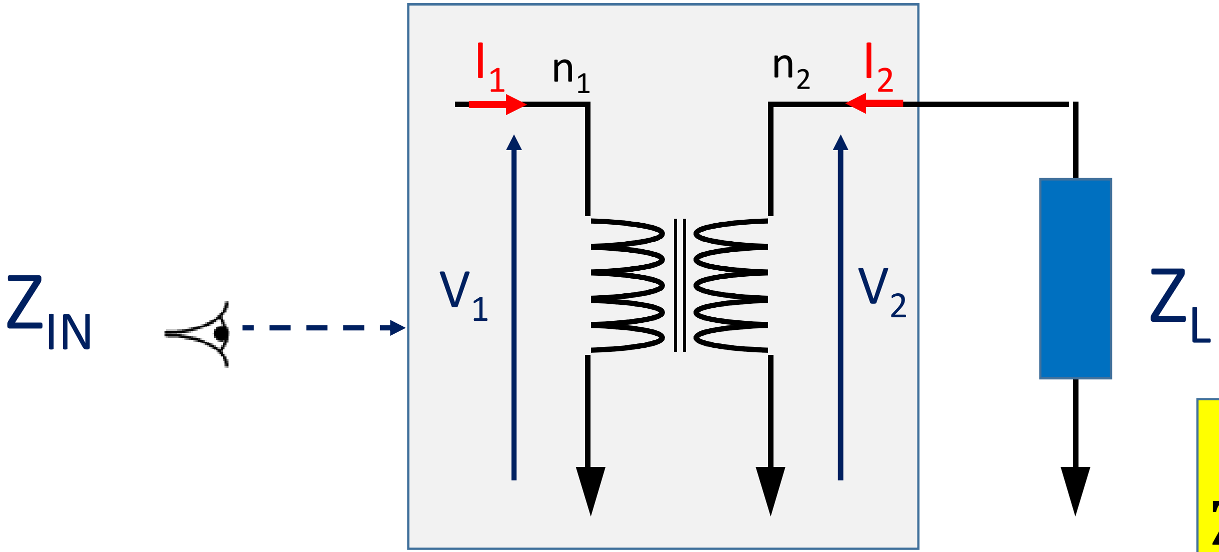
$$Z_{IN} = n^2 Z_L$$

$$n = \sqrt{\frac{Z_{IN}}{Z_L}}$$

## Reminder = Impedance transformation

$$\frac{V_2}{V_1} = \frac{n_2}{n_1}$$

$$\frac{I_2}{I_1} = -\frac{n_1}{n_2}$$




**Load**

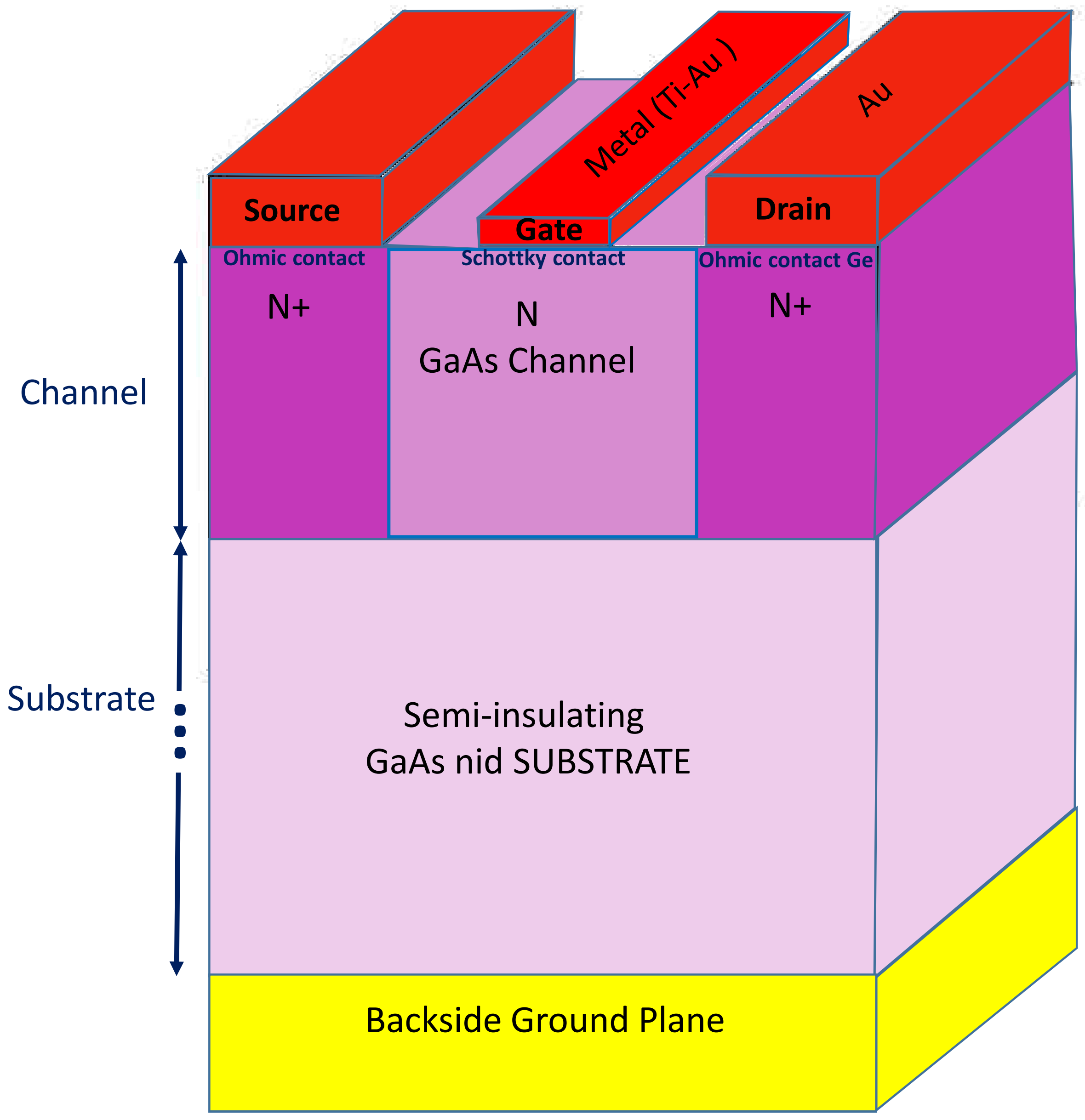
$$V_2 = -Z_L\, I_2$$

$$Z_{IN} = \frac{V_1}{I_1} = \frac{V_1}{V_2}\,\frac{V_2}{I_2}\,\frac{I_2}{I_1} = \frac{n_1}{n_2}\,(-Z_L)\,\frac{-n_1}{n_2} = \left[\frac{n_1}{n_2}\right]^2 Z_L$$

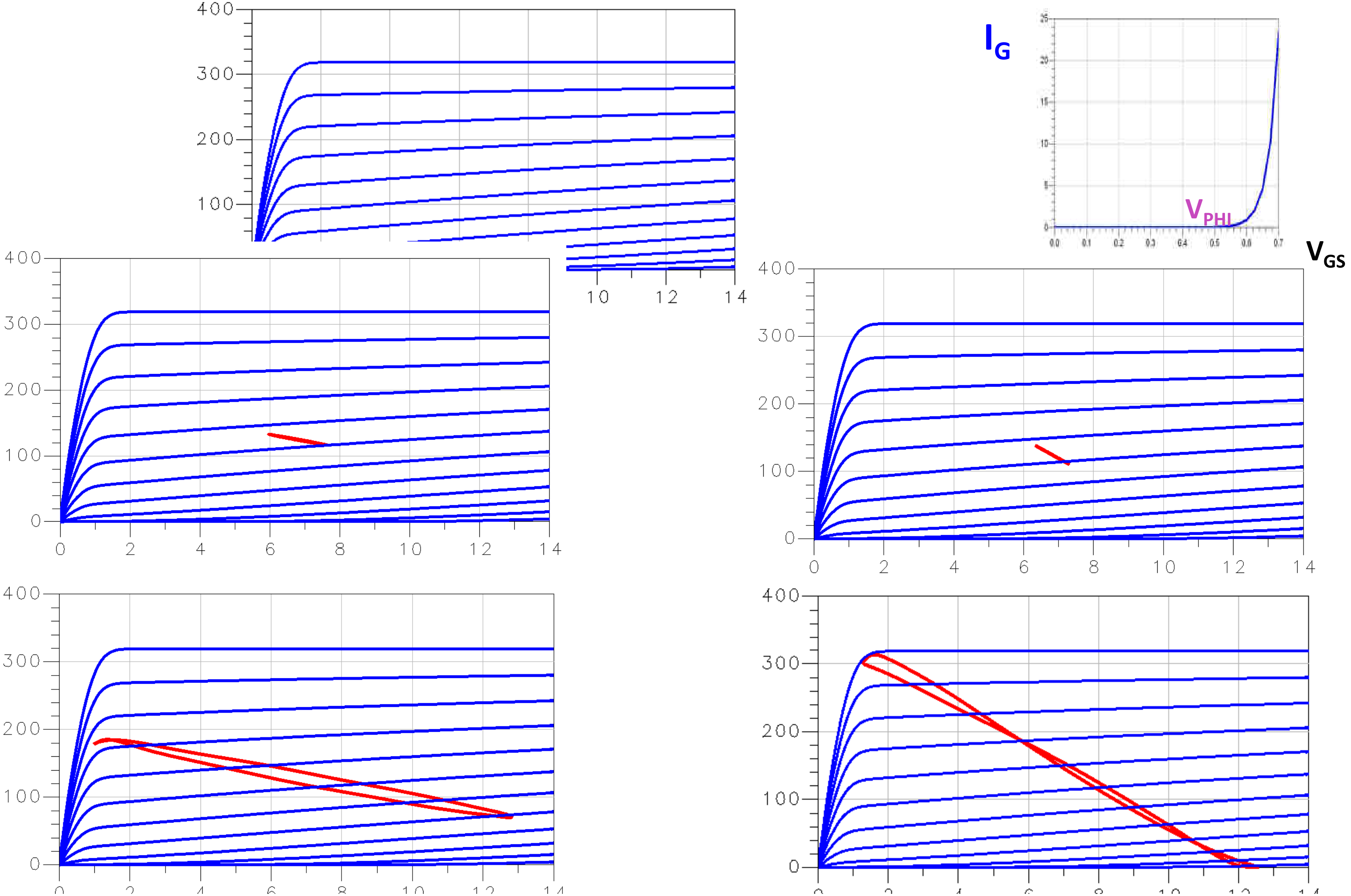
$$Z_{IN} = \left[\frac{n_1}{n_2}\right]^2 Z_L$$

$$n = \left[\frac{n_1}{n_2}\right] = \sqrt{\frac{Z_{IN}}{Z_L}}$$

# Additional Slides



Metal (Ti-Au )
Au
Source
Gate
Drain
Ohmic contact
Schottky contact
Ohmic contact Ge
N+
N
GaAs Channel
N+
Channel
Substrate
Semi-insulating
GaAs nid SUBSTRATE
Backside Ground Plane



$I_G$
$V_{PHI}$
$V_{GS}$

# I – Basics of HEMT operation → Same Electrical Circuit Model