Semester S1

Basics of Active and Non-Linear Electronics

PRACTICAL WORK

PW6:

TEST AND MEASUREMENT OF YOUR DESIGNED LINEAR AMPLIFIER @ 2GHZ

OUTLINE

TEST AND MEASUREMENT OF YOUR DESIGNED LINEAR AMPLIFIER @ 2GHZ

I OBJECTIVE

The goal of the PW is to test the designed linear power amplifier realized during the PW n ° 5 and optimized under small signal conditions to obtain the maximum gain. These tests will be made with the measuring tools that you have used during the first sessions of PW. You will measure:

1. The S parameters of the amplifier thanks to the calibrated vector network analyzer,
2. The power and performance characteristics with the calibrated the scalar network analyzer and finally,
3. Linearity characteristics using 3rd order intermodulation characterization measured with a spectrum analyzer.

II MEASUREMENTS OF THE [S] PARAMETERS OF THE OPTIMIZED GAIN LINEAR POWER AMPLIFIER.

II.1 VNA CALIBRATION

You are going to perform a full calibration of the network analyzer in the 1 to 3 GHz band..

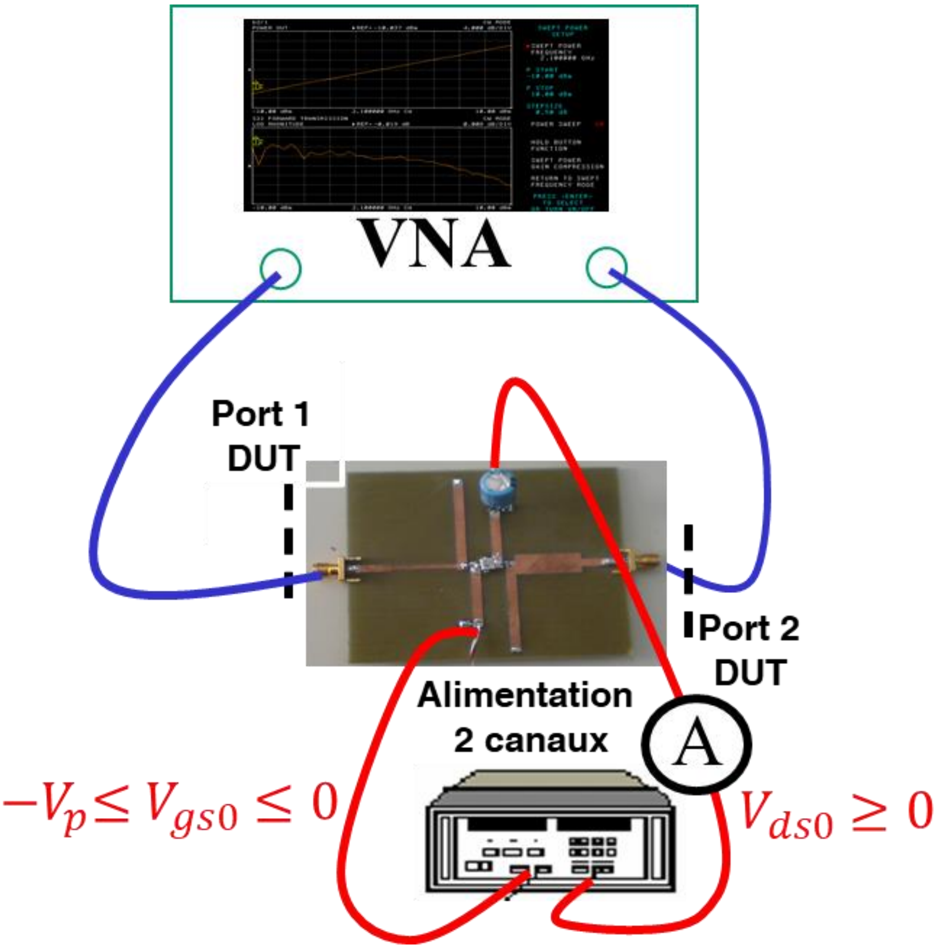
1. Reset the VNA.
2. Configure the analyser to display the 4 S parameters.
3. Perform a full (TOSM) calibration of the network analyser in the 1 to 3 GHz band.
4. Check this calibration from a direct connection between the 2 reference ports
5. Take many screenshots of the analyser with the 4 S parameters in the adequate formats (with 3 coupled markers at 1GHz, 2GHz and 3 GHz.

II.1.1 Amplifier biasing process.

A classic scheme of Biasing configuration of the amplifier is as described in the next figure.

The decoupling capacitances (DC block) and shock inductances (DC Feed) are integrated into the power amplifier PCB circuit.

It is FUNDAMENTAL to bias the power amplifier correctly according to a methodology described in PW 1, 2 and 3.



The following tasks should be performed in the process:

1. Switch off the two channels of the power supply with the power amplifier disconnected from the power supply
2. Check the polarity of the power supplies: $V_{gs0} < 0$ and $V_{ds0} > 0$

   Common Ground to
   both power supplies.
3. Adjust the power supply voltages before connecting them to the TEC at the values:

$$V_{gs0} = 0\text{V and } V_{ds0} = 0\text{ V}$$

4. Adjust the short circuit current for the gate
5. Adjust the short circuit current for the drain

6. Connect the gate power supply to the FET.
7. Connect the drain supply to the FET.
8. Switch on the channel of the power supply dedicated to the gate voltage.
9. Increase the gate voltage V_{gs0} first to the selected value, depending on the transistor and the polarization class
10. Switch on the channel of the power supply dedicated to the drain voltage.
11. - Increase the drain voltage V_{ds0} secondly to the desired I_{ds0} value.

MANDATORY !!!: Do not increase V_{DSO} when V_{GSO}=0V. The avalanche on the static characteristic at V_{GSO} =0V is unexpected and irreversible.

To depolarize the transistor, perform the following tasks in order:

1. Decrease V_{ds0} to 0 V and then Switch off the channel of the power supply dedicated to the drain voltage.
2. Decrease V_{gs0} to 0V and then Switch off the channel of the power supply dedicated to the gate voltage.
3. Disconnect the drain and gate ports respectively
4. Switch off the power supplies.

MANDATORY: Turn off the power supplies before disconnecting the FET...

In all cases, ask first the teacher to define and justify the limits of the potential source power variations without risk of damage of the power amplifier.

II.1.2 S Parameter Measurements of the power amplifier

1. Perform the measurement of the Power amplifier.
2. Choose the biasing conditions to compare your results with the performances given in the simulation performed during the PW5. Use a lower V_{DS0} voltage (3 V) to avoid thermal issues.
3. Take many screenshots of the analyser with the 4 S parameters in different formats (polar format (linear magnitude and phase, dB magnitude and phase),

Smith Chart, Real and Imaginary Part) with 3 coupled markers at 1GHz, 2GHz and 3 GHz.

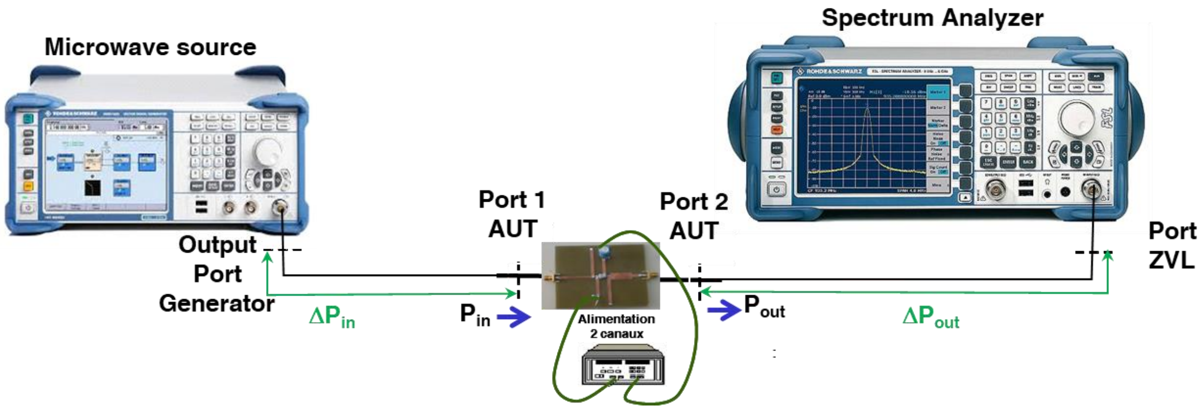
4. Compare to the values obtained with the simulation.
5. Comments.
6. Perform the depolarization of the transistor

III MEASUREMENT OF THE POWER CHARACTERISTICS OF THE LINEAR POWER AMPLIFIER

III.1.1 Objective and Reminders

You will measure the amplifier matched at the input and the output. So, you need to measure only the incident power and the transmitted power.

This measurement is made using the following test bench:



Implement the measurement and plotting of the following characteristics of the power amplifier with the biasing conditions used during the design with ADS (PW5).:

$P_{out}=f(P_{in})$ in mW

$P_{add}=f(P_{in})$ in mW

$PAE=f(P_{in})$ in %

It is recalled that: The following characteristic parameters are also defined at the frequency f_0 of the input generator:

- Input Power at f_0 :

$$\overline{P_{in}(f_0)} = \overline{P_{inc}(f_0)} + \overline{P_{ref}(f_0)} = \frac{1}{2}|\tilde{a}_1(f_0)|^2 - \frac{1}{2}\left|\tilde{b}_1(f_0)\right|^2$$

$$\overline{P_{in}(f_0)} = \frac{1}{2}|\tilde{a}_1(f_0)|^2\left(1 - \frac{\left|\tilde{b}_1(f_0)\right|^2}{|\tilde{a}_1(f_0)|^2}\right)$$

$$\overline{P_{in}(f_0)} = \frac{1}{2}|\tilde{a}_1(f_0)|^2\left(1 - \left|\tilde{S}_{11}(f_0)\right|^2\right)$$

Soit $\boxed{\overline{P_{in}(f_0)} = \frac{1}{2}|\tilde{a}_1(f_0)|^2}$ if matched input $|\tilde{S}_{11}(f_0)| = 0$

↳ Output Power at f_0 :

$$\overline{P_{out}(f_0)} = \overline{P_{transmitted}(f_0)} + \overline{P_{reflected}(f_0)} = \frac{1}{2}\left|\tilde{b}_2(f_0)\right|^2 - \frac{1}{2}|\tilde{a}_2(f_0)|^2$$

$$\overline{P_{out}(f_0)} = \frac{1}{2}\left|\tilde{b}_2(f_0)\right|^2\left(1 - \frac{|\tilde{a}_2(f_0)|^2}{\left|\tilde{b}_2(f_0)\right|^2}\right)$$

$\boxed{\overline{P_{out}(f_0)} = \frac{1}{2}\left|\tilde{b}_2(f_0)\right|^2}$ if matched load $|\tilde{\Gamma}_{ch}(f_0)| = 0$

↳ Added Power at f_0 :

$$\overline{P_{add}(f_0)}_{(mW)} = \overline{P_{out}(f_0)}_{(mW)} - \overline{P_{in}(f_0)}_{(mW)}$$

↳ DC Power consumption :

$$\overline{P_{DC}}_{(mW)} = \left|V_{GS0_{(V)}} I_{GS0_{(A)}}\right| + \left|V_{DS0_{(V)}} I_{DS0_{(A)}}\right|$$

↳ Power Gain at f_0 :

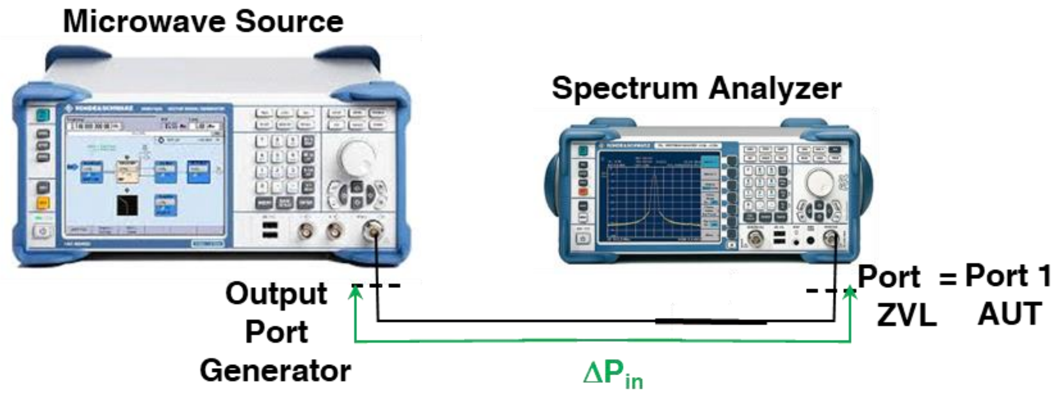
$$G_p(f_0) = \frac{\overline{P_{out}(f_0)}_{(mW)}}{\overline{P_{in}(f_0)}_{(mW)}}$$

↳ Power Added Efficiency at f_0 :

$$PAE_{(\%)} = 100\frac{\overline{P_{add}(f_0)}_{(mW)}}{\overline{P_{DC}}_{(mW)}}$$

III.1.1 Input Calibration

You must first measure the power losses $\Delta P_{in\ (dB)}$ between the output plane of the SMBV (Output Port Generator) and the input plane of the amplifier under test (Port 1 AUT). To do this: make the following test-bench configuration:



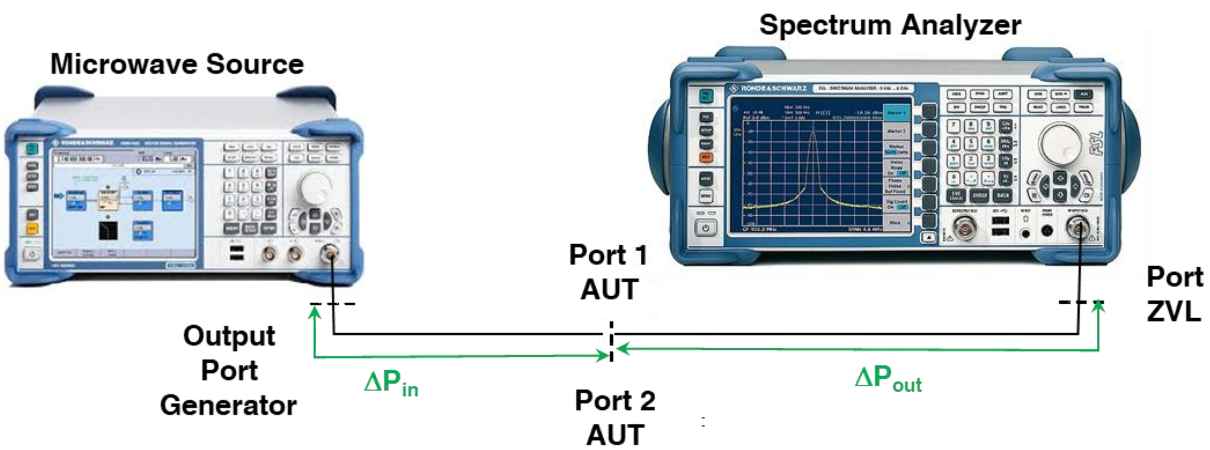
Fill the sheet “1.Delta Pin” of the excel file given in your platform :

Caracterisation of the losses between the generator and the input of the amplifier : Determination of ΔP_{in}

Freq Gene	$P_{output\_port\_gene}$	$P_{port1AUT}=P_{ZVLport}$	$\Delta P_{in}=P_{output\_port\_gene}-P_{ZVLport}$
GHz	dBm	dBm	dB

III.1.1 Output Calibration

You must then measure the power losses ΔP_{out} (dB) between the output plane of the amplifier under test (Port 2 AUT) and the input plane of the ZVL (Port ZVL). To do this, you will make a direct connection between the input plans (Port 1 AUT) and output (Port 2 AUT) of the amplifier under test by carrying out the following test-bench configuration:



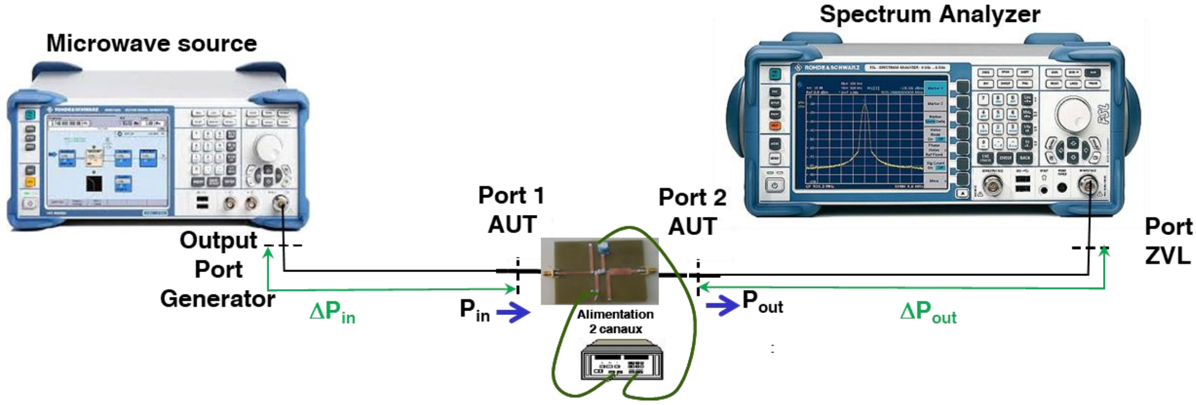
Fill the sheet “2.Delta Pout” of the excel file given in your platform :

Caracterisation of the losses between the onput of the amplifier and the input port of the ZVL : Determination of ΔP_{out}

Freq Gene	$P_{output\_port\_gene}$	$\lvert\Delta Pin\rvert$	$P_{in}=P_{output\_port\_gene}-\lvert\Delta pin\rvert$	$P_{port1AUT}=P_{port2AUT}$	$P_{ZVL}port$	$\Delta P_{out}=P_{output\_port\_gene}-P_{ZVLport}$
GHz	dBm	dB	dBm	dBm	dBm	dB

III.1.1 Power measurement of the biased amplifier.

Connect the power amplifier to the test bench to obtain the following configuration of the test bench:



The following tasks should be performed in the process:

12. Switch off the two channels of the power supply with the power amplifier disconnected from the power supply
13. Check the polarity of the power supplies: $V_{gs0} < 0$ and $V_{ds0} > 0$
    Common Ground to both power supplies.
14. Adjust the power supply voltages before connecting them to the TEC at the values:

$$V_{gs0} = 0V \text{ and } V_{ds0} = 0\text{ V}$$

15. Adjust the short circuit current for the gate
16. Adjust the short circuit current for the drain
17. Connect the gate power supply to the FET.
18. Connect the drain supply to the FET.
19. Switch on the channel of the power supply dedicated to the gate voltage.

20. Increase the gate voltage V_{gs0} first to the selected value, depending on the transistor and the polarization class
21. Switch on the channel of the power supply dedicated to the drain voltage.
22. - Increase the drain voltage V_{ds0} secondly to the desired I_{ds0} value.

MANDATORY !!!: Do not increase V_{DSO} when V_{GSO}=0V. The avalanche on the static characteristic at V_{GSO} =0V is unexpected and irreversible.

To depolarize the transistor, perform the following tasks in order:

5. Decrease V_{ds0} to 0 V and then Switch off the channel of the power supply dedicated to the drain voltage.
6. Decrease V_{gs0} to 0V and then Switch off the channel of the power supply dedicated to the gate voltage.
7. Disconnect the drain and gate ports respectively
8. Switch off the power supplies.

MANDATORY: Turn off the power supplies before disconnecting the FET...

In all cases, ask first the teacher to define and justify the limits of the potential source power variations without risk of damage of the power amplifier.

Fill the sheet "3.CW AUT PowerMeas" of the excel file given in your platform :

Power charcateristics of the Power Amplifier

Freq Gene	$P_{output\_port\_gene}$	$\|\Delta Pin\|$	$P_{in}=P_{output\_port\_gene}-\|\Delta pin\|$	P_{in_mW} =10^(P_{in}/10)	$P_{ZVL}port$	$\|\Delta Pout\|$	$P_{out}=P_{ZVLport}+\|\Delta Pout\|$	P_{out_mW} =10^(P_{out}/10)	|Gp|= P_{out_mW}/P_{in_mW}	$\|Gp\|_{dB}$= 10*$\log_{10}$(|Gp|)	Vds0	Ids0	Pdc= Vds0*Ids0	PAE= (P_{out_mW}-P_{in_mW})/Pdc*100
GHz	dBm	dB	dBm	mW	dBm	dB	dBm	mW		dB	V	mA	mW	%

IV MEASUREMENT OF LINEARITY CHARACTERISTICS OF THE LINEAR POWER AMPLIFIER (THIRD ORDER INTERMODULATION).

IV.1 INTERMODULATION CHARACTERISTICS (TWO-TONE)

For even finer validation of the non-linear performances of the Power Amplifier (PA), it is necessary to know them in terms of linearity.

Extraction by measurement or simulation of the intermodulation characteristics is performed using a particular test signal.

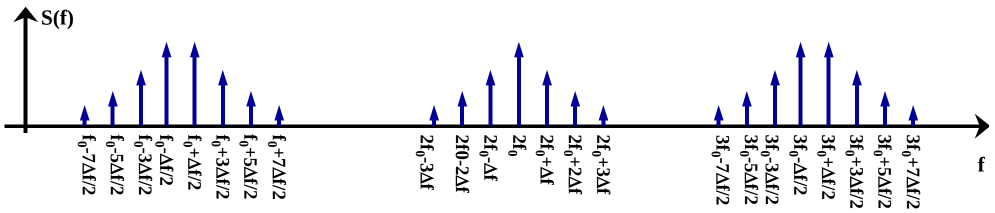
In this case, the incident power wave driving the PA under test is then the sum of two power waves of equal amplitude and of different frequencies coming from two sources synchronized by a unique reference clock (in general, a reference signal equal to 10MHz) or from a microwave source modulated around a carrier frequency. The modulation used is then a double side -band suppressed carrier- (DSB SC) modulation.

If we note Δf the frequency difference between the two sources around f_0, the excitation frequencies of the two synthesizers are therefore equal to:

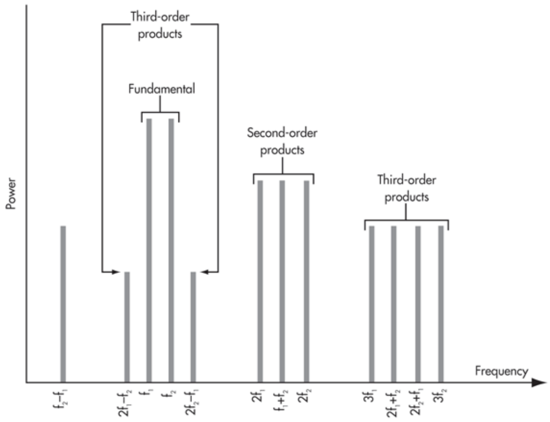
$$f_1 = f_0 - \frac{\Delta f}{2}$$

$$f_2 = f_0 + \frac{\Delta f}{2}$$

The frequency spectrum of the signals at the ports of the PA is therefore defined on the following figure:



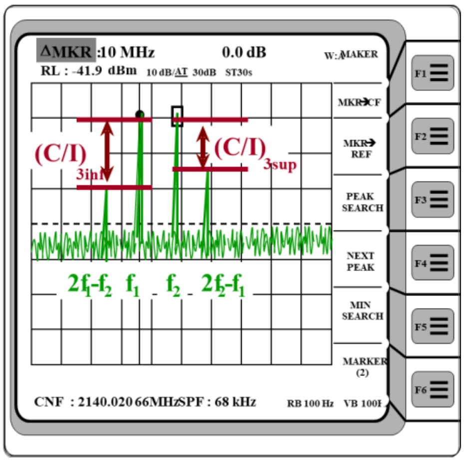
The intermodulation products are defined as follows from the spectral line measurements of the spectrum analyzer:



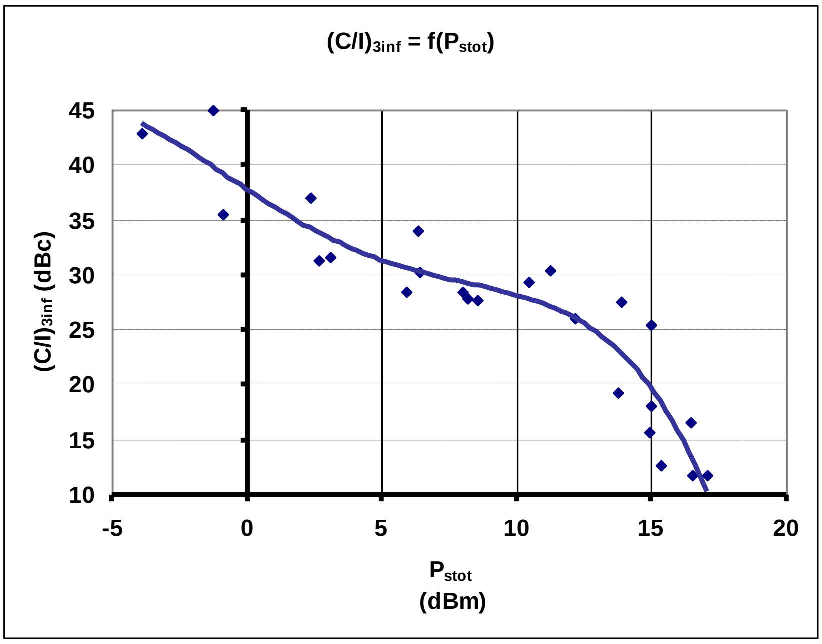
$$(C/I)_{3inf(dBc)} = P_{out}(f_1)_{(dBm)} - P_{out}(2f_1 - f_2)_{(dBm)}$$

$$(C/I)_{3sup(dBc)} = P_{out}(f_2)_{(dBm)} - P_{out}(2f_2 - f_1)_{(dBm)}$$

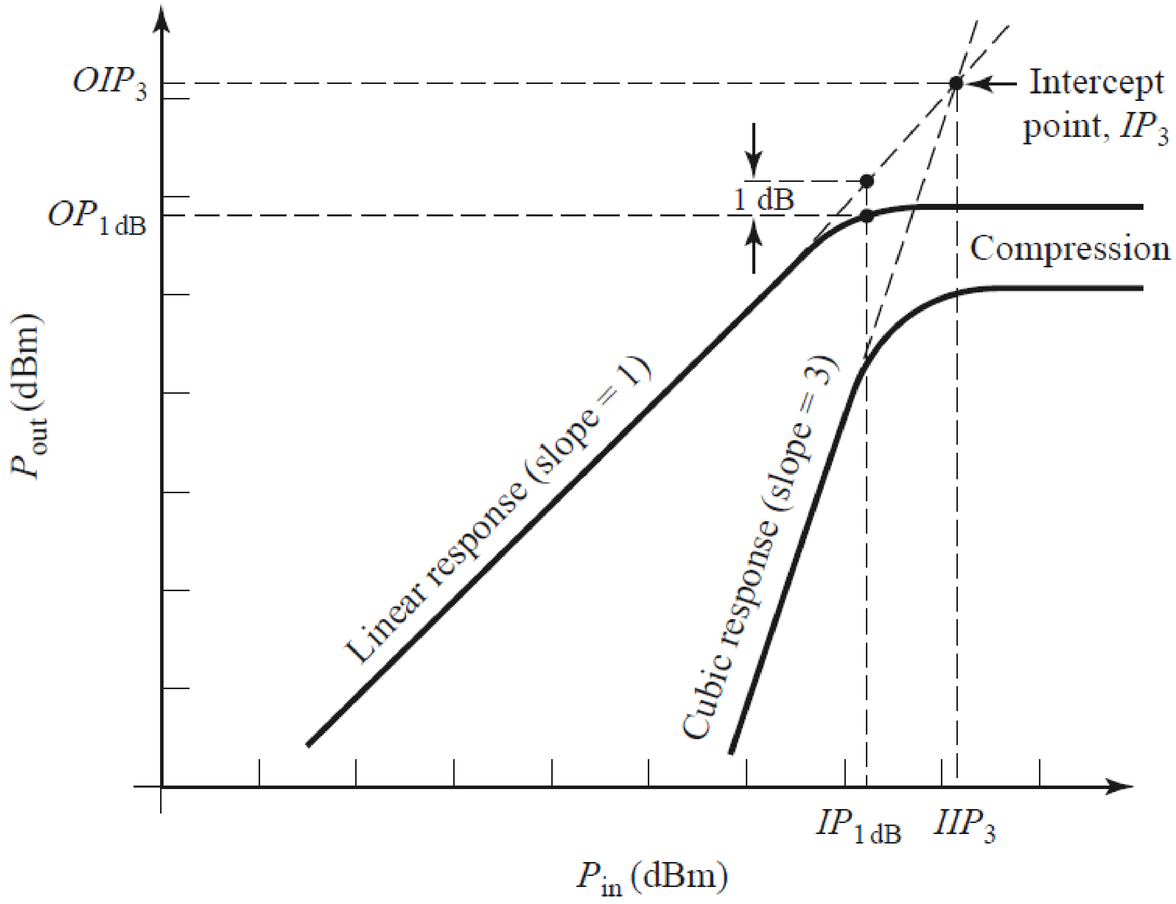
$$(C/I)_{3tot(dBc)} = 10 * log_{10}\left[\frac{P_{out}(f_1)_{(mW)} + P_{out}(f_2)_{(mW)}}{P_{out}(2f_1 - f_2)_{(mW)} + P_{out}(2f_2 - f_1)_{(mW)}}\right]$$



When the power at the input of the transistor is varied and the various values of the 3rd order intermodulation products are recorded for all power levels, the following curve is obtained:



Most of the amplifiers are defined for the criteria of linearity with respect to the 3rd order intercept point whose definition is as follows:



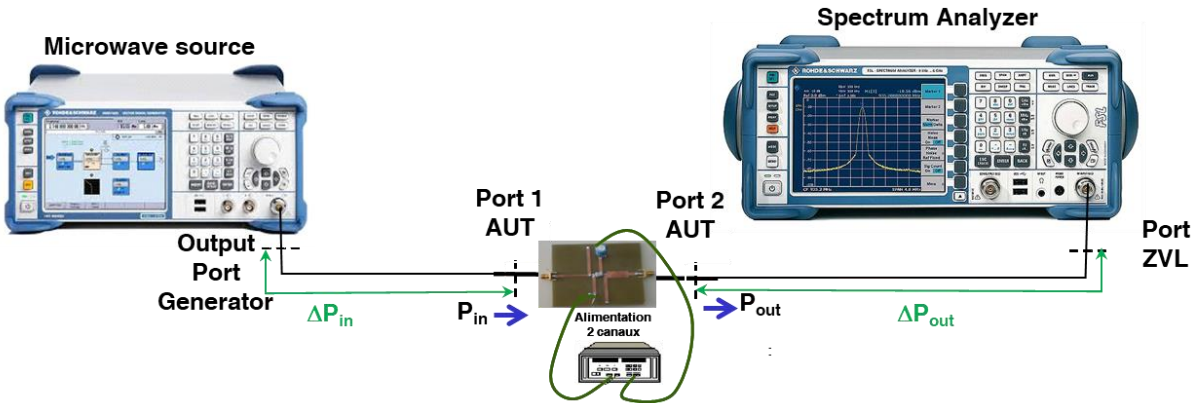
Third order intercept point is an hypothetical point where the power of third order components will reach to the same level of fundamental component's power.

If one draws the power input versus power output, they will observe the different frequency components having different slopes (cf. previous figure).

So, Third order intercept point is an ideal point as once the device reaches to 1 dB compression point the two curves will become parallel to each other and they will never cut. Which shows that the power for fundamental and third order component will not be same. but this parameter is very important in terms of characterizing a device.

IV.1.1 3rd intermodulation Test-bench.

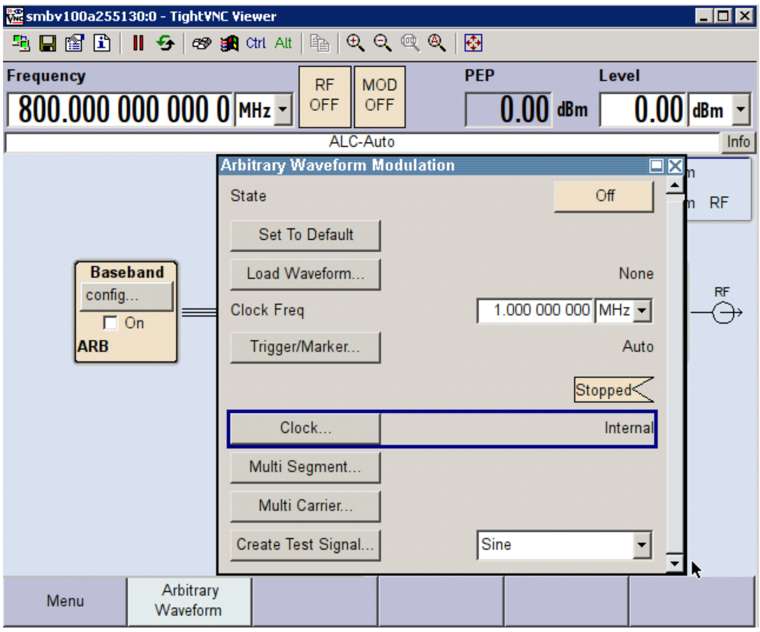
The measuring bench is in the following configuration:



Measurements will be made around the central operating frequency of the amplifier for varying source powers. You will use multicarrier type signals with two frequencies whose spacing will be equal to 100kHz then 1 MHz.

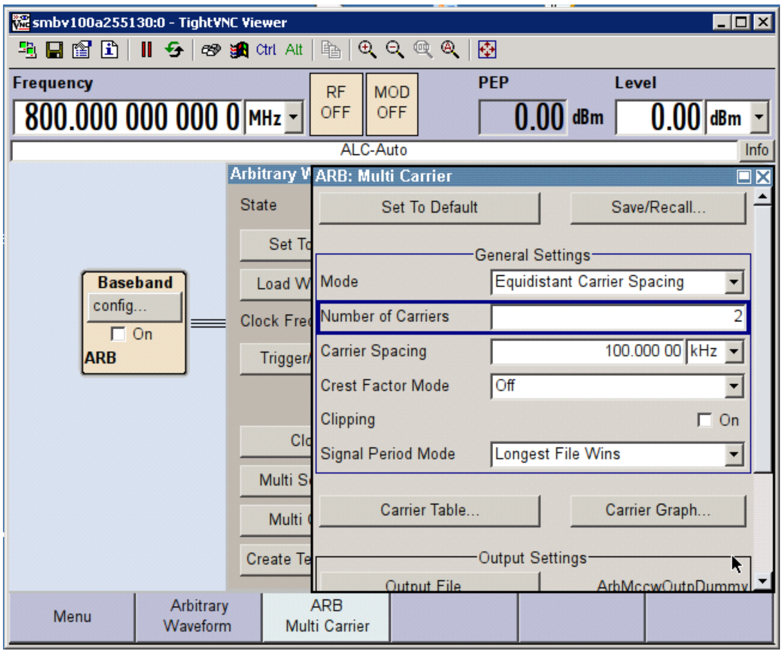
Open the Config menu of the Baseband button.

Choose Multicarrier.

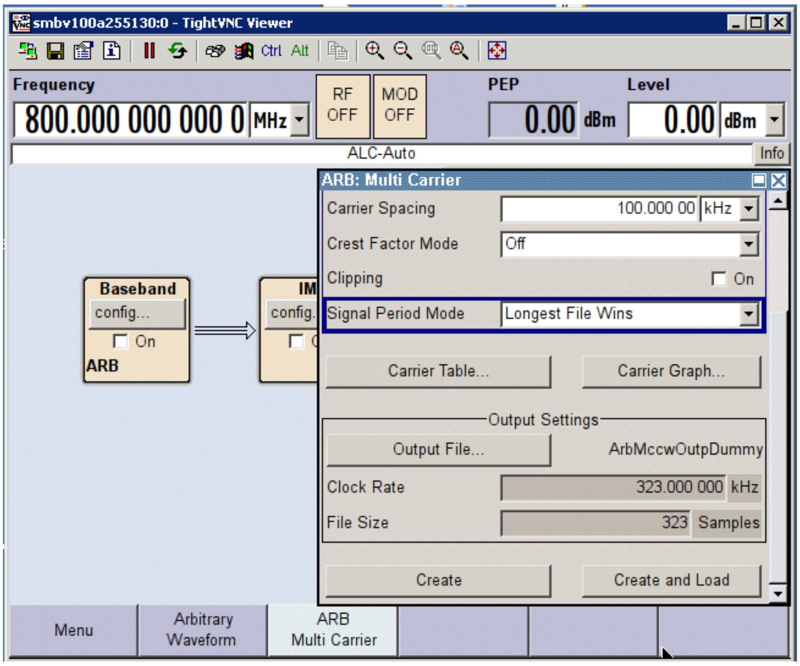


Choose Number of carriers 2

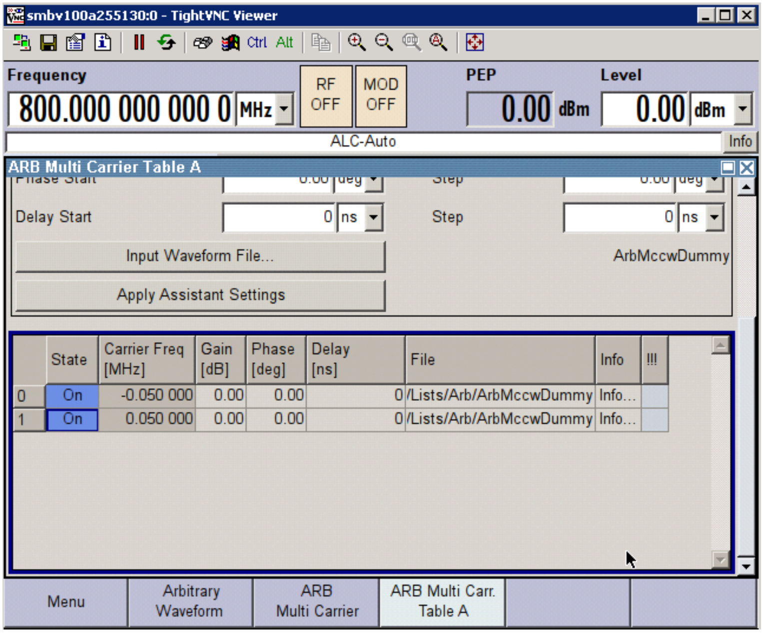
Enter the value of the Carrier Spacing



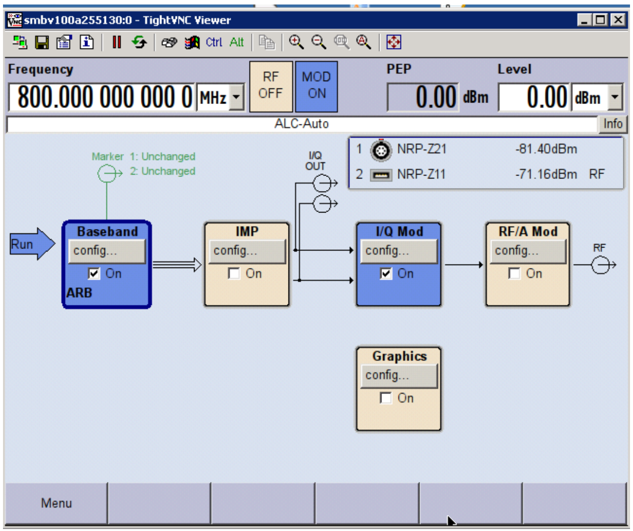
Click then on Create and load



Open the Carrier Table menu and switch ON state of the two frequencies.



Click on « ON » of the Baseband menu to activate the modulation.



Fill the sheet "4.2-tone AUT PowerMeas" of the excel file given in your platform:

3rd order Intermodulation product charcateristics of the Power Amplifier

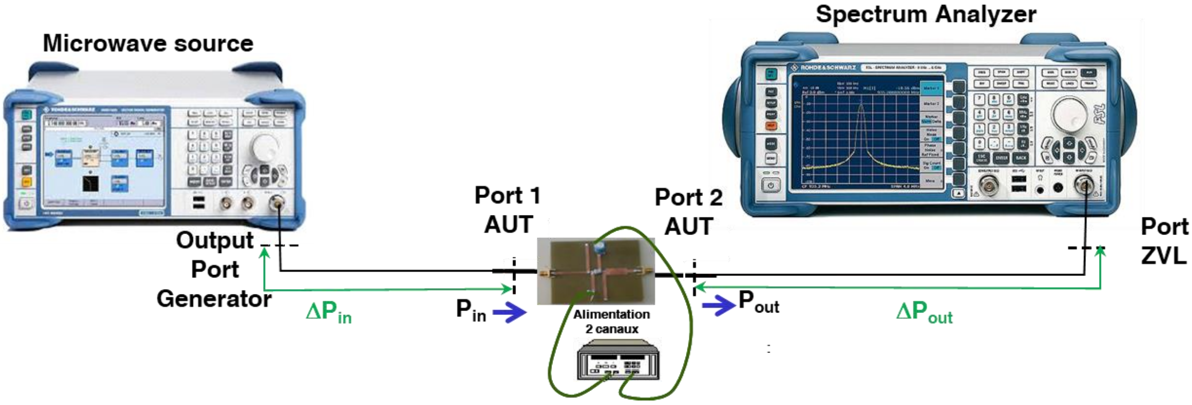
$f_{carrier}=f_0$	$\lvert\Delta f\rvert$	$P_{output\_port\_gene}$	$\lvert\Delta Pin\rvert$	$P_{in}=P_{output\_port\_gene}-\lvert\Delta pin\rvert$ @f1	$P_{in\_mW}=10^\wedge(P_{in}/10)$ @f1	$P_{in}=P_{output\_port\_gene}-\lvert\Delta pin\rvert$ @f2	$P_{in\_mW}=10^\wedge(P_{in}/10)$ @f2	P_{ZVL} port @2f1-f2	P_{ZVL} port @f1	P_{ZVL} port @f2	P_{ZVL} port @2f2-f1	$\lvert\Delta Pout\rvert$	$P_{out}=P_{ZVLport}+\lvert\Delta Pout\rvert$ @2f1-f2	$P_{out\_mW}=10^\wedge(P_{out}/10)$ @2f1-f2	$P_{out}=P_{ZVLport}+\lvert\Delta Pout\rvert$ @f1	$P_{out\_mW}=10^\wedge(P_{out}/10)$ @f1	$P_{out}=P_{ZVLport}+\lvert\Delta Pout\rvert$ @f2	$P_{out\_mW}=10^\wedge(P_{out}/10)$ @f2	$P_{out}=P_{ZVLport}+\lvert\Delta Pout\rvert$ @2f2-f1	$P_{out\_mW}=10^\wedge(P_{out}/10)$ @2f2-f1	Vds0	Ids0	Pdc= Vds0*Ids0	(C/I)3inf	(C/I)3sup	(C/I)3tot
GHz		dBm	dB	dBm	mW	dBm	mW	dBm	dBm	dBm	dBm	dB	dBm	mW	dBm	mW	dBm	mW	dBm	mW	V	mA	mW	dBc	dBc	dBc

Plot the associated curves of $(C/I)_3$ versus the total output power. Deduce the value of the 3rd order interception point.

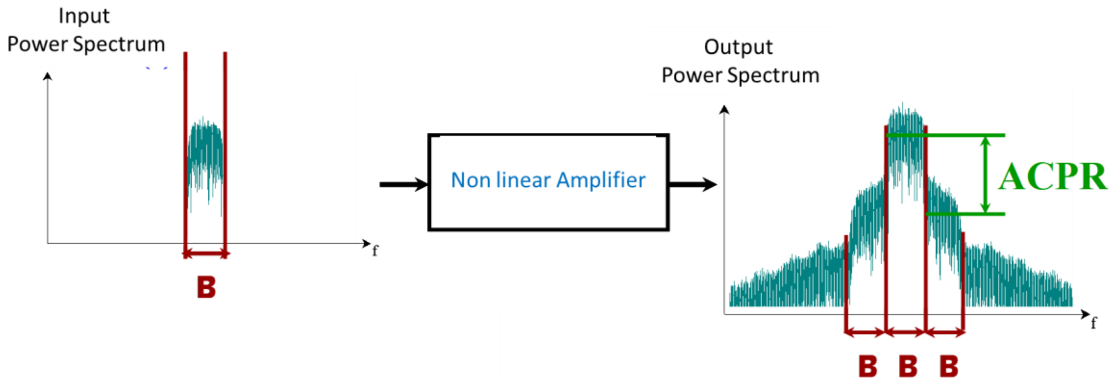
IV.2 LINEARITY CHARCATERISTICS WHEN THE PA IS DRIVEN WITH COMPLEX MODULATED SIGNALS.

For the characterization of the amplifier when driven by a 16QAM real modulated signal, it is possible to use the modulated signal source in the same configuration as before. The performance criterion tested is different.

The measuring bench is in the following configuration:



The most frequently used performance criteria are the adjacent channel power ratio:



ACPR stands for Adjacent Channel Power Ratio, is an important performance metric used to characterize spectral regrowth of transmitter frontend component or entire chain. One of the main source of spectral regrowth is power amplifier nonlinearity. Therefore this metric is used even to quantify the nonlinearity of a power amplifier. It is also called as Adjacent Channel Leakage Ratio (ACLR).

At times (at max power levels) PAs are forced to operate much beyond their linear range of operation to improve overall efficiency of transmitter. Due to nonlinear behavior of PA, along with power amplification in main channel some power leaks into adjacent channel (mainly due to intermodulation distortion). This spectral leakage is quantified through ACPR.

ACPR is defined as the ratio of power in the adjacent channels of main channel to the rms power of the transmitted signal in the main channel.

The spectral powers in main and adjacent channels are compared in relative sense, and specified in dBc.

Example :

In WCDMA the channels are spaced 5MHz apart with a carrier bandwidth of 3.84MHz. To estimate ACPR of outermost channel, the total carrier power in 3.84MHz bandwidth in main channel is compared to total power in 3.84MHz BW centered around 5MHz offset from main channel.

IV.2.1 Configuration of the test bench to use complex modulated signals for the ACPR characterization.

Measurements will be made around the central operating frequency of the amplifier for varying source powers. You will use the 16QAM type signals to be set in the Baseband menu.

Fill the sheet “5.ACPR AUT PowerMeas” of the excel file given in your platform:

ACPR charcateristics of the Power Amplifier

$f_{carrier}=f_0$	$\|\Delta f\|$	$P_{output\_port\_gene}$	$\|\Delta Pin\|$	$P_{in}=P_{output\_port\_gene}-\|\Delta pin\|$	P_{in_mW} =10^(P_{in}/10)	P_{ZVL} port @left adjacent Channel	P_{ZVL} port @Useful signal Channel	P_{ZVL} port @right adjacent Channel	$\|\Delta Pout\|$	$P_{out}=P_{ZVLport}+\|\Delta Pout\|$ @left adjacent Channel	P_{out_mW} =10^(P_{out}/10) @left adjacent Channel	$P_{out}=P_{ZVLport}+\|\Delta Pout\|$ @Useful signal Channel	P_{out_mW} =10^(P_{out}/10) @Useful signal Channel	$P_{out}=P_{ZVLport}+\|\Delta Pout\|$ @right adjacent Channel	P_{out_mW} =10^(P_{out}/10) @right adjacent Channel	Vds0	Ids0	Pdc= Vds0*Ids0	Left ACPR	Right ACPR
GHz		dBm	dB	dBm	mW	dBm	dBm	dBm	dB	dBm	dBm	dBm	mW	mW	mW	V	mA	mW	dBc	dBc

You will then plot the evolution of the ACPR (left and right) according to the output power level.