M1 EMIMEO

Tutorial N°6

Let us consider a transistor having the following I/V characteristics (Figure 1)

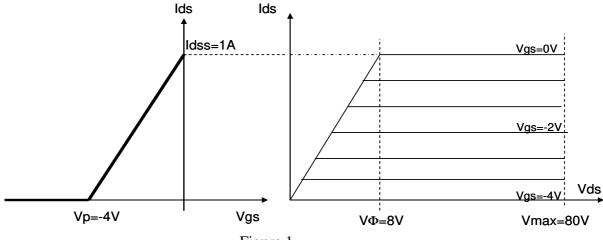


Figure 1

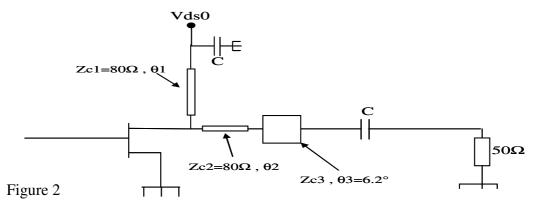
We consider also the following parameters:

$$Rg = 4\Omega$$
 , $Cgs=5pF$, $Fo=3.6 Ghz$, $Cds = 0.76 pF$

The gate source bias voltage Vgs0 is chosen in order to have an aperture angle ϕ = 110° when Vgs1 is at its maximum value . (Vgs(t)_{max} = 0V)

I] In this first part we want to obtain the maximum output RF power

- 1) Determine the values of Vgs0 and Vds0
- 2) Determine the corresponding optimal load impedance (Real part and Imaginary part)
- 3) Calculate the output power and the power added efficiency
- 4) We want to design the output RF matching Network with distributed elements as represented in Figure 2



Determine the values of the electrical lengths $\theta 1$ and $\theta 2$ and the value of the characteristic impedance Zc3

- II] In this second part we keep the same values for the load impedance, Vgs0 and Vds0 than the ones obtained in Part I but Vgs1 is decreased. Vgs1 is now equal to +2V.
 - 1) What are the corresponding values of the output RF power and the PAE.
- III] In this third part we keep the same values of the load impedance and Vgs0. We keep also Vgs1 equal to +2V but we decrease the value of Vds0.
 - 1) What is the minimal value of Vds0 for which we reach the saturation regime of the transistor
 - 2) What are the corresponding values of the output power and the PAE
- IV] In this last part we take again the values of Vgs0 and Vds0 determined in part I We keep Vgs1=+2V but we modify the value of the load impedance in order to have the maximum possible output RF power for Vgs1 = +2V.
 - 1) Determine the required value of the load resistance as well as the corresponding values of the output RF power and the PAE.

the output RF power and the PAE.

I)
$$V650 = V650 = V650$$

4)
$$\theta_1 = 90^{\circ}$$
 (corresponding to a 1/4 line)

For the output RF matching we wonk to have. the equivalence retwork

 $680 L$
 $100 L$
 1

