Faculté des Sciences & Techniques — Université de Limoges — EMIMEO Erasmus Mundus

1st session – January 7, 2022

Master 1 EMIMEO - Exam of "Basics of active and nonlinear electronics" (M. Campovecchio)

A- Narrow-band power amplifier (2 stages)

Specifications: Output Power $P_{OUT} > 2$ W ; Center frequency $f_0 = 10$ GHz ;
Source resistor $R_G = 10\ \Omega$ and Load resistors $R_L = 50\ \Omega$

MMIC technology (0.25 µm GaAs HEMT**) :** Selected transistor **8x75 µm** (size **T1 of 0.6mm**) @ 10GHz
Power density $PD(R_{OPT}) = 1$ W/mm ; Measured maximum gain @ 10 GHz $G_{MAX(@10GHz)} = 20$ dB ≈ 100 ;
Maximum drain current I_{DSmax} = 800 mA/mm; Limits of V_{DS} voltage (V_{DSmin}=1 V and V_{DSmax}=11 V)
Optimum power resistance: R_{OPT} = 12,5 Ω.mm
Linear electrical model : C_{GS} = 2 pF/mm ; R_i = 2 Ω.mm ; R_{DS} = 75 Ω.mm ; C_{DS} = 1 pF/mm

In the problem (C_{GS1} ; C_{DS1} ; Ri_1 ; R_{IN1} ; R_{DS1} ; R_{OPT1}) stand for the values of transistor **T1** = 8x75µm = **0.6 mm**

- In this problem, **the last stage B has to be matched to its optimum power load** R_{OPT_B}
  while the first stage A has to be matched to its optimum gain load R_{DS_A}

1) Using scaling rules, calculate the numerical values (C_{GS1} ; C_{DS1} ; Ri_1 ; R_{DS1} ; R_{OPT1}; R_{IN1}) of T1 @10GHz.
   The following equation gives the equivalent parallel input resistor : $R_{IN} = \frac{1}{R_i C_{GS}^2 \omega^2}$
2) Power gain and power density :

- $G_P(R_{OPT})$ is the power gain of a transistor T when it is loaded by its optimum power load (L_{OPT}//R_{OPT}).
- $G_{MAX} = G_P(R_{DS})$ is the maximum power gain of T when it is loaded by its optimum gain load (L_{OPT}//R_{DS}).

It can be demonstrated that the power gain $G_P(R_{OPT})$ can be expressed as a function of G_{MAX} by:
$G_P(R_{OPT}) = 4\,R_{OPT}\frac{R_{DS}}{[R_{DS}+R_{OPT}]^2}\,G_{MAX}$ *(not to be demonstrated)*

   a) Using the preceding equation, determine the numerical value of $G_P(R_{OPT})$ @ 10GHz when the transistor T1 is matched to its optimum power load.

   b) In the case of maximum gain matching, express the power density $PD(R_{DS})$ as a function of $PD(R_{OPT})$. Calculate its numerical value in W/mm.

3) Amplifier sizing:
   a) Last stage B optimized for maximum power: Using the specifications of output power, determine the number n_B of transistors T1 / its optimum load resistance R_{L_B} as a function of R_{OPT1} / its output power P_{OUT}=P_{OUT_B} / its gain G_{P_B} and the inter-stage power P_{IN_B}=P_{OUT_A}).

   b) First stage A optimized for maximum gain: Determine the number n_A of transistors T1 / its optimum load resistance R_{L_A} as a function of R_{DS1} / its gain G_{P_A} and the input power P_{IN}=P_{IN_A}).

4) On the amplifier schematic (Fig 1), indicate the numerical values of each stage when the amplifier operates at the maximum output power of the last stage.

5) Input and inter-stage matching using scaling rules
   a) Using questions 1 and 3, calculate the equivalent series input resistances R_{i_A} and R_{i_B} of each stage.
   b) Using questions 1 and 3, calculate the parallel resistances R_{IN_A} and R_{IN_B} of each stage at 10GHz.

6) On Fig. 2, draw the electrical matching circuits (inductors and transformers) of the two-stage amplifier when matched to R_S=10Ω and R_L=50Ω and write the expression of matching elements **without calculating numerical values**. For the sake of simplicity, you can use the notations:
$$L_1 = 1/(C_{GS1}\,\omega_0^2) \text{ and } L_2 = 1/(C_{DS1}\,\omega_0^2)$$

7) If both stages operate in class-A, calculate the maximum PAE of the amplifier? Why is-it less than 50%?

Name:

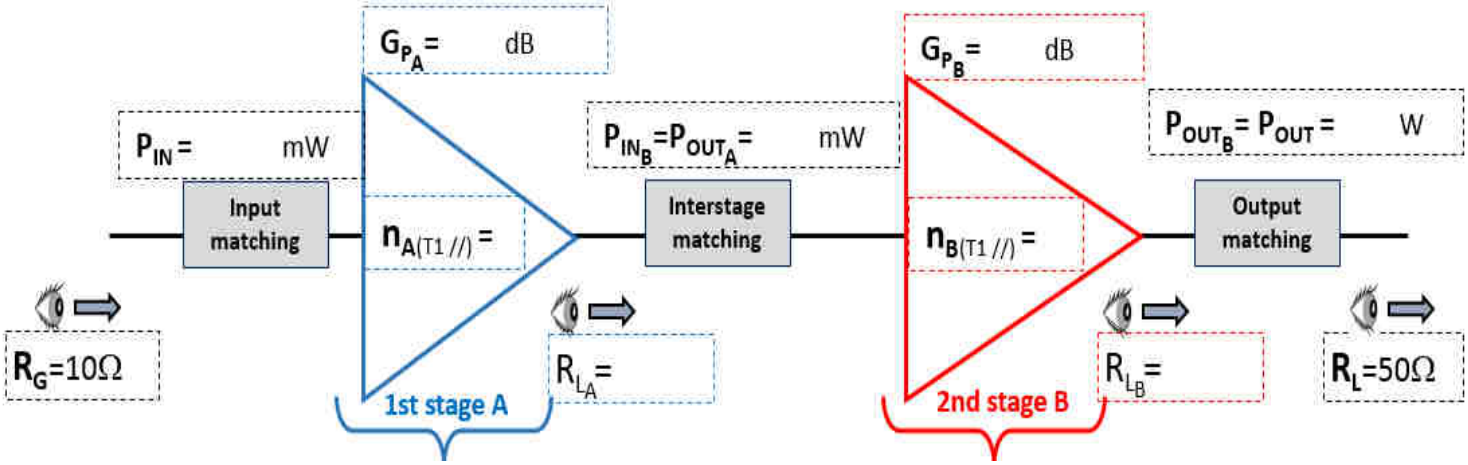

Figure 1: Sizing values for the power amplifier

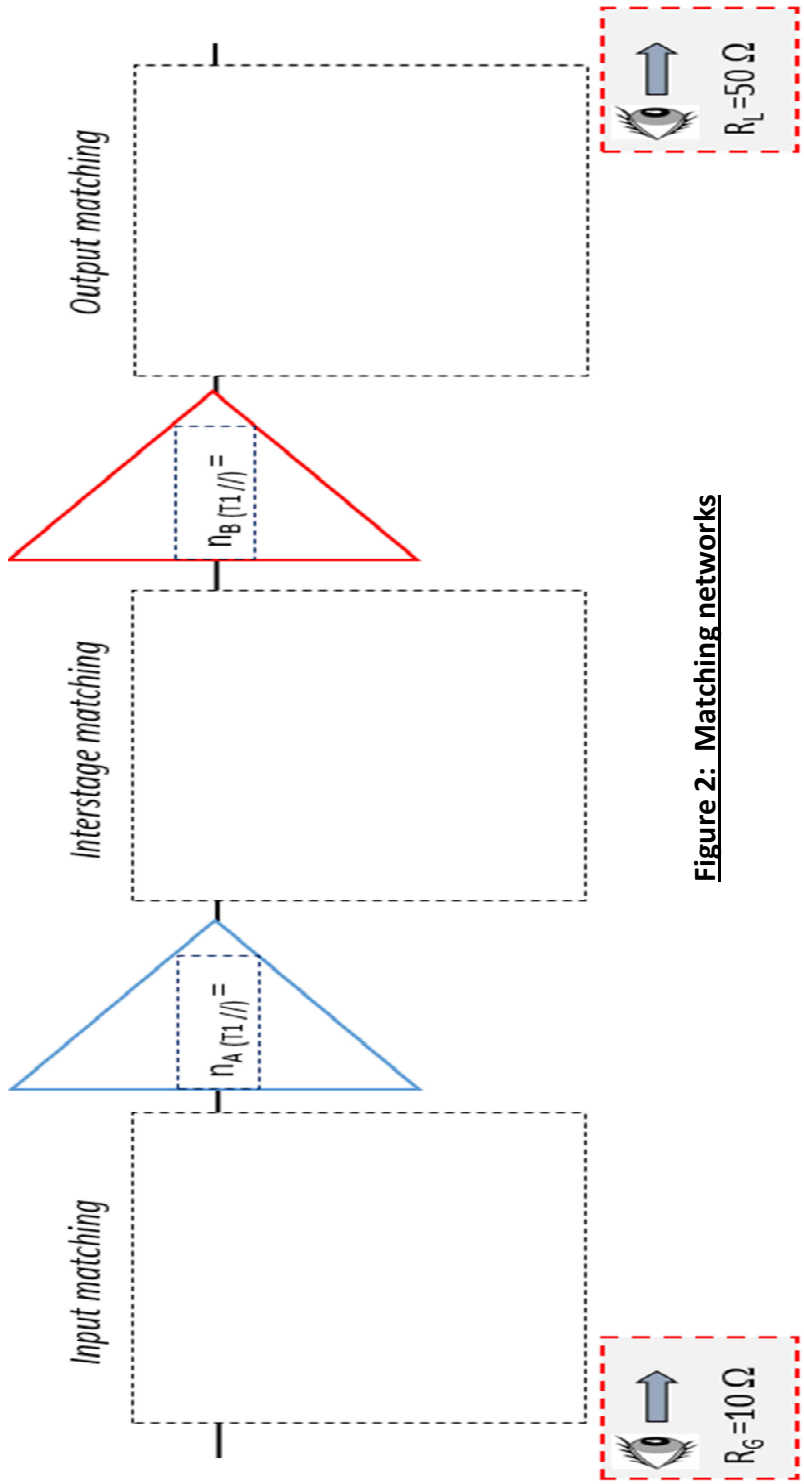

Figure 2: Matching networks