Class Integrated Passives – M. BLONDY

1. Silicon integrated RF passives

A bit of history

RF Silicon integrated circuits have grown considerably over the past twenty years. They represent today the vast majority of RF and microwave circuits. This growth is all the more spectacular considering that for many years, the conductivity of this substrate has been considered a major roadblock for the successful integration of microwave circuits. For example, a simple micro-strip transmission line fabricated on doped silicon substrate has very significant losses, and therefore most microwave integrated circuits have initially been realized on substrates in Gallium Arsenide (GaAs), since this substrate has low loss and allows the fabrication of low loss passives.

This semiconductor material has very low losses at microwave frequencies, in addition to excellent charge mobility. Thus, it is possible to realize active microwave integrated circuits (amplifiers, mixers, oscillators ...) on these substrates, with excellent performance. These circuits are called MMICs (Monolithic Microwave Integrated Circuits), they were the first high frequency integrated circuits.

In a simplified manner, these circuits make it possible to integrate fast transistors, with the most common elements of the microwave circuits (stubs, microstrip lines), in the form of a chip that performs one or more functions of a subsystem.

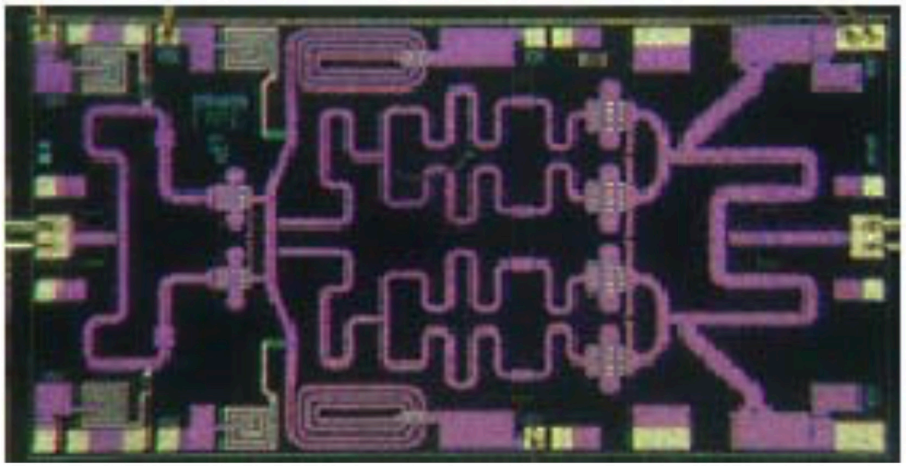

Figure 1- A GaAs Monolithic Microwave Integrated Circuit Amplifier.

With the arrival of mobile telephony in the late nineties, strong industrial demand has emerged to push the integration of digital circuits (Silicon) closer to RF circuits.

Industry has therefore developed new silicon manufacturing processes by adding layers above the transistor layers to make low-loss passive circuits. At the same time, a new generation of bipolar transistors based on silicon and germanium (SiGe) compounds appeared, with speeds comparable to those obtained on GaAs substrate, with lower manufacturing costs.

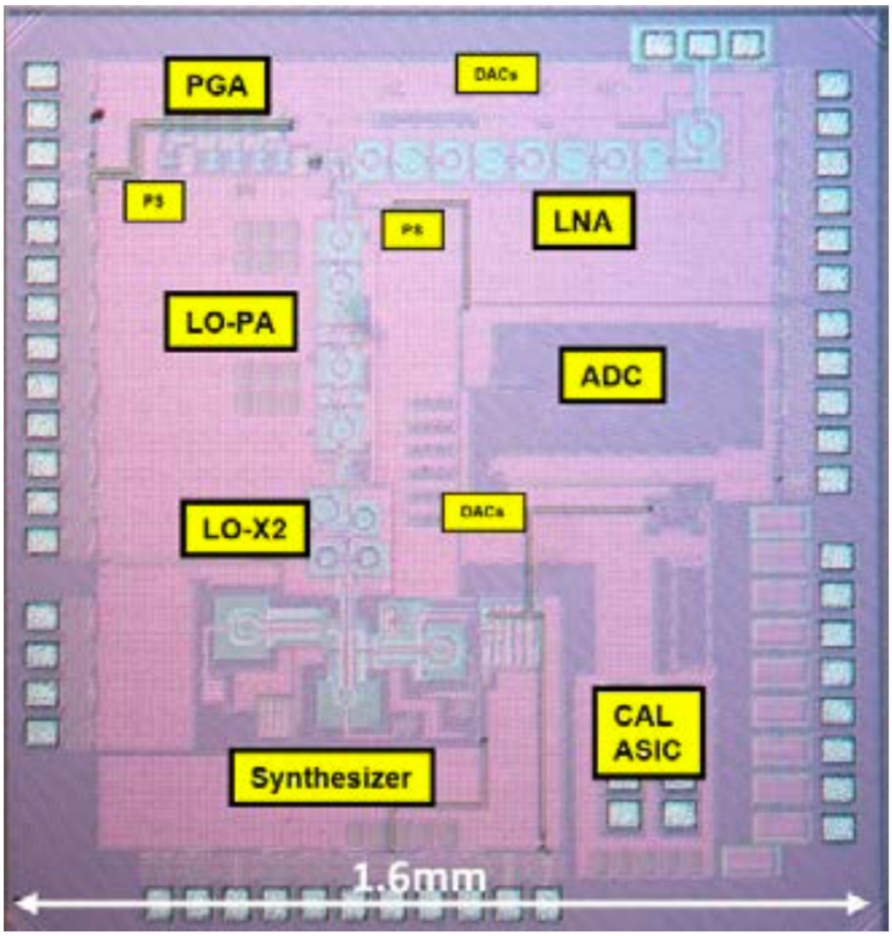

Figure 2 – An RFIC circuit. The circuit comprises several local oscillators (LO-xx), a low-noise amplifier (LNA), and a Power Amplifier (PA) and digital Circuits (DACs-ADC) and a calibration ASIC. All these functions, digital and analog, are integrated on a single chip.

The combination of these new generation transistors and the addition of several metallization layers above the silicon substrate (see below) made it possible to realize passive matching circuits completely isolated from the lossy silicon substrate.

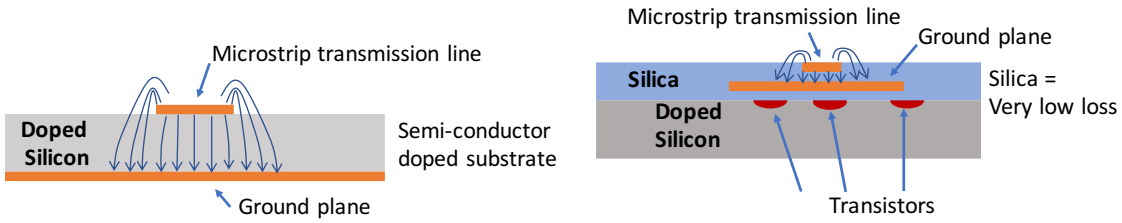

Figure 3 – Cross-sectional view of a microstrip line on a doped silicon substrate, and on a modern RFIC circuit. On the RFIC circuit, the microstrip line is compact, and isolated by the ground plane of the substrate.

Processes for manufacturing so-called "BiCMOS" circuits for "Bipolar CMOS" suited to Radio Frequency (RF) circuits of mobile phones have thus been developed. New microwave integrated circuits, Radio Frequency Integrated Circuits (RFICs) have appeared. A large number of RF functions such as mixers, oscillators or low-level amplifiers can be realized at low cost with this technology, on very small surfaces.

Mobile telephony has experienced a considerable development, and RFIC technology has followed the same path, and it is now possible to make a large number of circuits on silicon. The cost of this technology has greatly decreased because of the high demand for these circuits, but also by intrinsic qualities of silicon, which is a material easier to handle than GaAs.

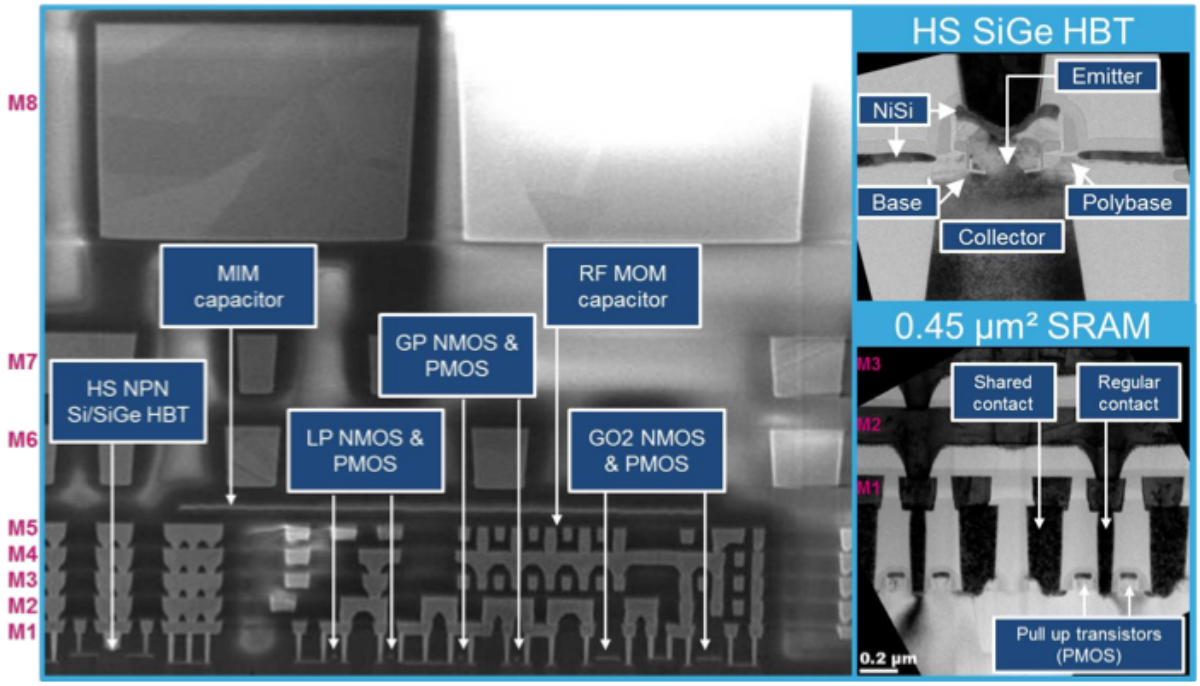

Figure 4 – Cross-sectional view of the layers of a silicon manufacturing process (BiCMOS 55nm ST Microelectronics)

Several types of passive circuits can be integrated on these substrates, which will be briefly reviewed below:

Resistors

For a metal film whose thickness is less than the skin depth, it can be considered that the current is distributed uniformly over the conductor section of thickness t, width w, and conductivity. The conductivity is in Siemens/m, t and w are in meters.

The surface S of the section is:

$$S = w.t$$

The resistance of a length l of this conductor is given by the following formula:

$$R = \frac{\rho l}{S} = \frac{l}{\sigma . w . t}$$

A square pattern of this conductor has a length-to-width ratio $\frac{l}{w} = 1$. R can be re-computed in this configuration and one may consider a resistance per square $R_{\square}$:

$$R_{\blacksquare} = \frac{1}{\sigma t}$$

To determine the resistance of a pattern drawn on a circuit layout, simply count the squares of the pattern, and add the corresponding square resistances.

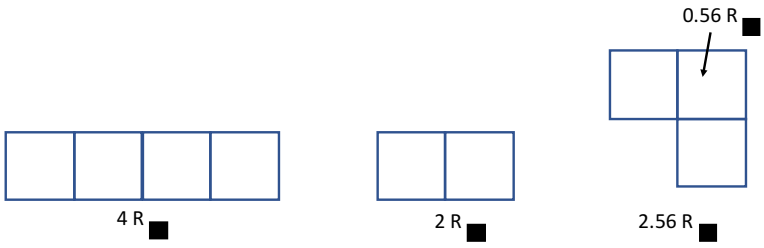

Figure 5 - Exemples de calculs de valeurs de résistances carrées de différents layouts

In the case of meanders, which are often used for reasons of compactness of the circuit and in this case, illustrated in Figure 4, the square is about 0.5 squares or 0.56, when using little more rigorous calculations.

It is possible to make resistors from CMOS transistors, using the polysilicon of the gate of the transistor as a resistive material, or other layers integrated in the manufacturing process.

Integrated passives

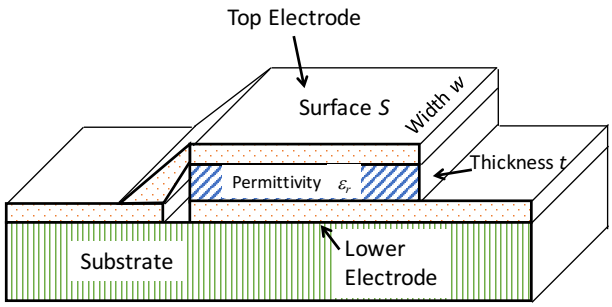

Figure 6 - Metal-Insulator-Metal (MIM) capacitor

The capacitance is given by the following expression:

$$C = \frac{\varepsilon_0 \varepsilon_r S}{t} \; Farads$$

$$\text{avec } \varepsilon_0 = 8.82\ 10^{-12} F/m$$
$$\text{et } S = w.l$$

Its equivalent scheme is:

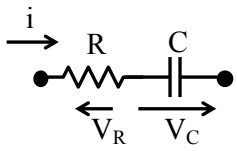

Figure 7 – Simplified equivalent scheme of an integrated capacitor

The capacity of the equivalent scheme is deduced from the layout, and the resistance can be determined by measuring the overvoltage coefficient of the circuit.
The Q- factor ("overvoltage coefficient" literally in French) of the circuit in Figure 7 is given by the following equation:

$$Q = \frac{V_C}{V_R} = \frac{\left(\frac{1}{C\omega}\right) i}{R.i} = \frac{1}{RC\omega}$$

We can also retrieve this expression as follows, starting from a more general expression of the Q-factor:

$$Q = \omega \frac{Stored\ energy}{Average\ Dissipated\ Power} = \omega \frac{\frac{1}{2} C V_C^2}{\frac{1}{2} R i^2} = \omega \frac{\frac{1}{2} C V_C^2}{\frac{1}{2} R V_C^2 C^2 \omega^2} = \frac{1}{RC\omega}$$

Figure 8 – General outlook of the Q-factor of a capacitor in series with a resistor

Planar spiral inductors

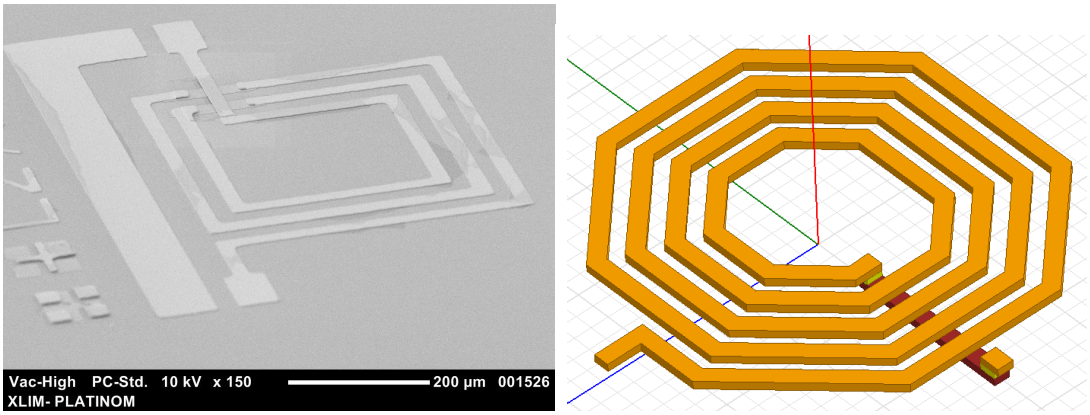

Figure 9 – Exemple d'inductances planaires intégrées

Inductors are integrated in microelectronics in the form of planar metal spirals, which realize a mutual inductance by the proximity of the currents on the different windings of the inductor. These components are relatively compact (<150 µm) and are highly optimized by silicon foundries.

Modeling of these components remains complex, and powerful electromagnetic simulation software still have difficulties to determine accurately the characteristics of these spirals. The effects of accumulation of currents on the sides of the conductors are difficult to model and the presence of the conductive substrate close to the self generates eddy currents (Foucault's currents in French) which must be modeled finely.

There are many approximate formulas for calculating choke values from their geometry that are incorporated in most commercial circuit simulation software.

These formulas are mostly empirical, and will not be given back in these notes. On the other hand, the modeling of inductances modeling will make it possible to grasp the approach followed to build an equivalent electric model of the inductor.

1.1.1. Equivalent scheme

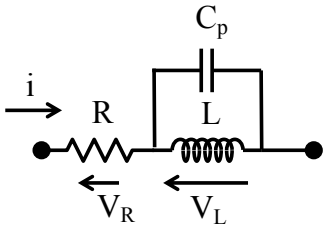

Figure 10 – Equivalent scheme of an integrated inductor

The equivalent scheme consists of a series with a resistor. Resistance models the losses of the spirals, but also the modification of the current distribution on the turns. We note the presence

of a capacity in parallel with, which allows to model the phenomenon of resonance of the spiral. The impedance of the circuit is shown in Figure 10.

$$Z = R + jL\omega \,//\, \frac{1}{C_P\omega}$$

The resonant frequency of the self ω_0 is given by the following equation :

$$\omega_0 = \frac{1}{\sqrt{LC_P}}$$

If ω is small versus ω_0, then Z becomes:

$$Z \approx R + jL\omega$$

In this frequency range, the Q-factor of the inductor can be defined as follows:

$$Q = \frac{V_L}{V_R} = \frac{L\omega i}{Ri} = \frac{L\omega}{R}$$

In the same way, we can retrieve this formula from the energy stored in the inductor:

$$Q = \omega \frac{Stored\ Energy}{Average\ Dissipated\ Power} = \omega \frac{\frac{1}{2}Li^2}{\frac{1}{2}Ri^2} = \frac{L\omega}{R}$$

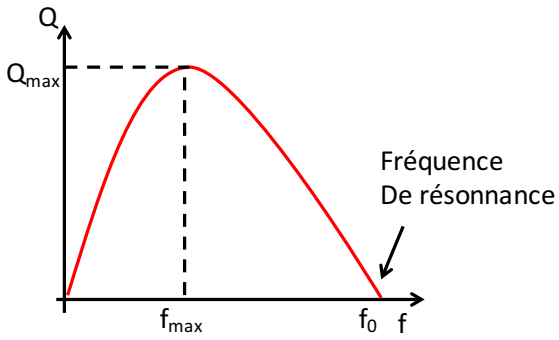

Figure 11 - Allure du coefficient de surtension de la self en fonction de la fréquence, en intégrant la capacité inter-spires

The Q factor of the inductor increases linearly with the frequency, following $\frac{L\omega}{R}$ in the first part of the curve, then the parasitic capacitance C_P just decreases this coefficient, up to its resonance frequency, f_0, up to which it is no longer possible to use the inductor (it's a *parallel* resonant circuit).
In practice, there is a max frequency $f_{\max}$ up to which the Q factor reaches a maximum value $Q_{\max}$. The inductor is generally optimized to be used around this frequency.