Semester S1

Basics of Active and Non-Linear Electronics

PRACTICAL WORK

PW4:

SIMULATION OF A LINEAR AMPLIFIER @ 2GHZ USING KEYSIGHT ADS AND BASED ON LUMPED COMPONENTS

OUTLINE

I OBJECTIVE 3

II TRANSISTOR MATCHING – THEORETICAL REMINDERS 3

II.1 GENERALITIES ABOUT AMPLIFIER DESIGN 3

II.2 REMINDER ABOUT TRANSFORMERS 5

II.2.1 Open circuit voltage output : 5

II.2.2 Perfect transformer 6

II.2.3 impedance reflected back to the primary of a perfect transformer 7

III MANIPULATION : POWER TRANSISTOR MATCHING (IN CLASS A) 8

III.1 OUTPUT MATCHING 8

III.1.1 Cancellation of the imaginary part of the transistor output impedance 8

III.1.2 Matching of the real part of the transistor output impedance 10

III.1.3 Simulation of the output matched transistor 12

III.2 INPUT MATCHING 13

III.2.1 Cancellation of the imaginary part of the transistor input impedance 13

III.2.2 Matching of the real part of the transistor input impedance 13

III.2.3 Simulation of the matched transistor (input and output) 13

IV MANIPULATION: LOW-LEVEL SIMULATION OF THE TRANSISTOR IN CLASS A. 16

V MANIPULATION : HIGH-LEVEL SIMULATION OF THE TRANSISTOR IN CLASS AB 16

SIMULATION OF A LINEAR AMPLIFIER @ 2GHZ USING KEYSIGHT ADS AND BASED ON LUMPED COMPONENTS

I OBJECTIVE

The goal of this practical work (PW) is to use Keysight's ADS (Advanced Design System) simulation software for the narrow-band design of a power amplifier from a field-effect transistor (FET). Particularly, we want to match (in terms of power) the FET transistor you have already used in the previous experimental PWs in a narrowband around the frequency of 2 GHz:

- to a generator having a purely real internal impedance R_0 equal to 50 Ω connected at the input of the FET;
- To a purely real load of 50Ω connected at the output of the FET.

You will use again the ADS project you have already use in PW3. This project is normally located in your personal dedicated space in the application server. Start by opening this project. In addition, you have at the end of this document a small booklet detailing all the simulation files contained in the project, as well as the corresponding results.

II TRANSISTOR MATCHING – THEORETICAL REMINDERS

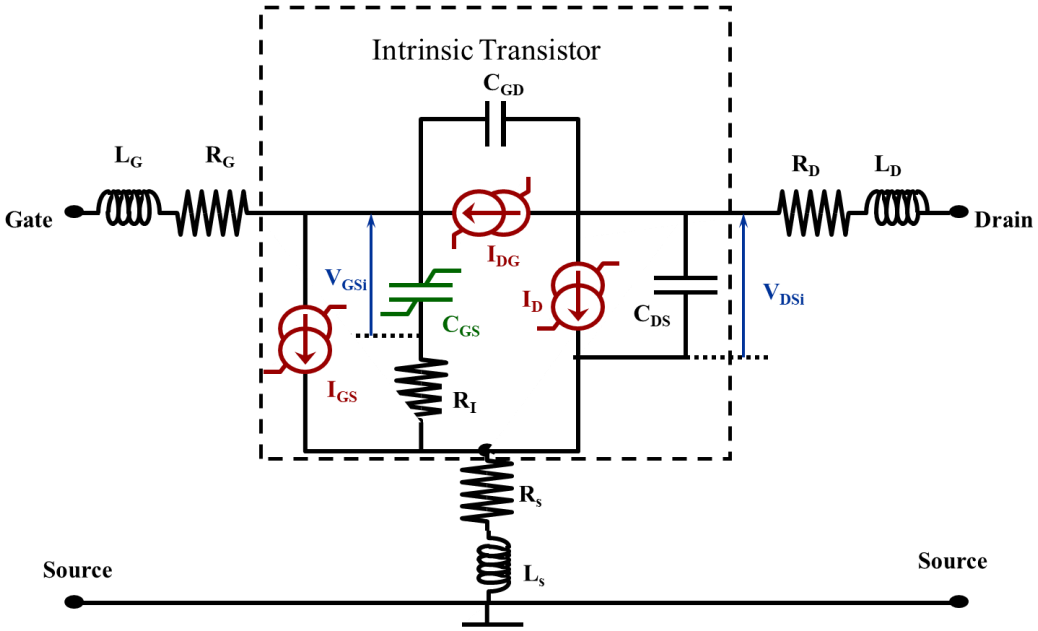
II.1 GENERALITIES ABOUT AMPLIFIER DESIGN

In a power amplifier design, the predominant element is the numerical model of the transistor. Indeed, it must be as close as possible to the behavior of the real transistor from the point of view of the power performance but also efficiency or linearity.

As described in the first PW using ADS in this PW serie (i.e., PW3), measurements carried out with the pulse bench I/V and S-parameters make possible to characterize the static and dynamic behavior of the component over a wide range of frequencies.

A conventional structure including a controlled current source is chosen to model the transistor, as shown in the following figure:

NON LINEAR ELECTRONIC MODEL of a DISCRETE MESFET



Intrinsic and extrinsic elements of the transistor model are extracted and adjusted following an optimization made using S-parameter measurements for different DC bias point over a well-defined frequency band. Typically, non-linear capacitances extracted from the measurements vary according to the control voltages V_{GS} and V_{DS}. Capacitance values are also obtained by extraction, from the measured S-parameters and at different bias value of Vgs for the nonlinear capacitance Cgs. Thus, the model build following this procedure combines a faithful functioning of the transistor with respect to a real one as well as a reduced computation time.

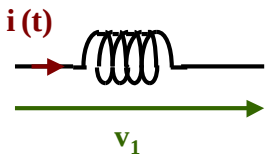
The convective non-linear model used for the transistor is valid for a positive drain bias voltage up to the avalanche region and a gate bias voltage from the pinched-off state (from Threshold voltage) of the transistor to the gate conduction region of the transistor.

The electrical modeling of the transistor is obtained by adjusting the elements (R_s, R_g and R_d resistances, I_{DS} current source, avalanche generator, input diode) so that the simulated I/V network matches satisfyingly with the measured one. The two gate-source and gate-drain input diodes drives the positive gate current measured for high V_{GS} voltage values and low V_{DS} values. The avalanche generator characterizes the beginning of the phenomenon, often destructive for the transistor.

If the chosen convective model is well adjusted, only the parasitic elements have to be optimized. These parasitic phenomena correspond to the inductive and capacitive effects of the transistor: L_g, L_d, L_s and C_{GS} which is non-linear.

II.2 REMINDER ABOUT TRANSFORMERS

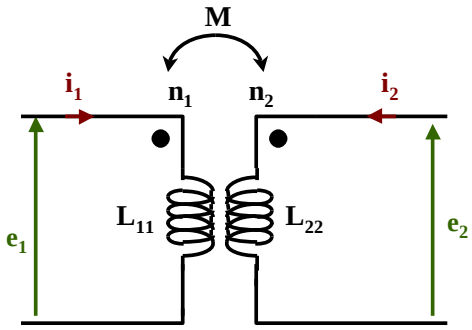
A self-inductance associated to the following representation (on the left) can be defined by the equations written below (on the right):



$$v_1(t) = L_1 \frac{di_1(t)}{dt}$$

$$V_1 = jL\omega I_1$$

A mutual inductance is defined as the association of two self-inductances (L_{11} and L_{22} being the self-inductances of windings 1 and 2) whose effects can be described as follows:



$$L_{11}\frac{di_1(t)}{dt} + L_{12}\frac{di_2(t)}{dt} = e_1$$

$$L_{21}\frac{di_1(t)}{dt} + L_{22}\frac{di_2(t)}{dt} = e_2$$

The degree of coupling is driven by L_{21} and L_{12}. Ideally, these elements are reciprocal and therefore $L_{12} = L_{21} = M$.

II.2.1 Open circuit voltage output :

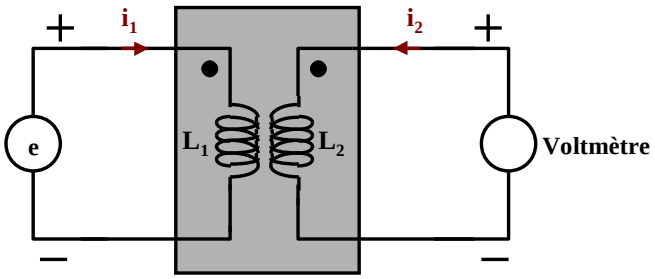
A voltage e_{10} applied on L_{11} when L_{22} is in open circuit (i.e. i_2=0) gives:

$$e_{10} = L_{11}\frac{di_1(t)}{dt}$$

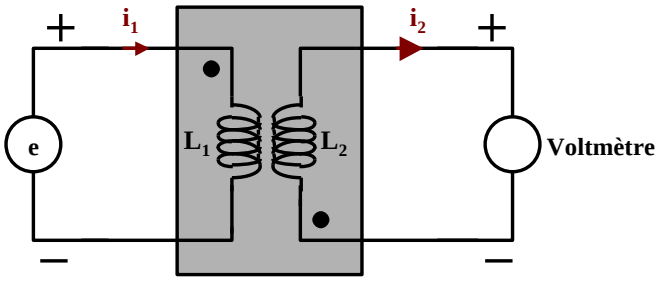
$$e_{20} = L_{21}\frac{di_1(t)}{dt} \quad \text{(induced at secondary)} \quad \text{donc :} \quad \frac{e_{20}}{e_{10}} = \frac{L_{21}}{L_{11}}$$

Coupling coefficient

If currents i_1 and i_2 flow in opposite directions as in the following diagram, fluxes add up and $L_{12} = L_{21} > 0$:



If currents i_1 and i_2 flow in the same direction as in the following diagram, fluxes are subtracted and $L_{12} = L_{21} < 0$:



In both cases, the coupling coefficient *k* is defined as follows

$$k = \left|\frac{L_{12}}{\sqrt{L_{11}L_{22}}}\right| = \left|\frac{M}{\sqrt{L_{11}L_{22}}}\right| \Rightarrow \frac{e_{20}}{e_{10}} = \frac{L_{21}}{L_{11}} = \pm k\sqrt{\frac{L_{22}}{L_{11}}}$$

It is possible to demonstrate that $0 \le k \le 1$ and consequently $|L_{12}| \le \left|\sqrt{L_{11}L_{22}}\right|$

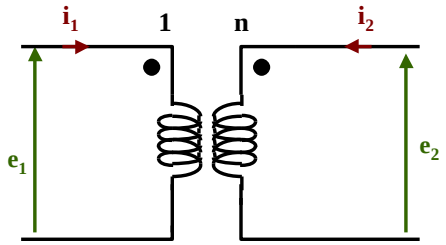
II.2.2 Perfect transformer

If *k*=1, both inductances are said to be perfectly coupled and the transformer is considered as a perfect transformer. Writtening the following equation:

$$\frac{L_{22}}{L_{11}} = \left(\frac{n_2}{n_1}\right)^2 = n^2 \Rightarrow \frac{e_{20}}{e_{10}} = \pm n$$

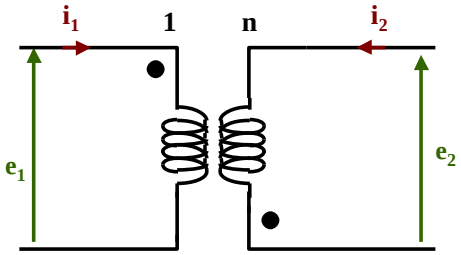
n_1 and n_2 are respectively the number of windings at the primary and the secondary of the transformer.

A perfect transformer can be represented either by



$$\frac{e_1}{e_2} = \frac{n_1}{n_2} = \frac{1}{n}$$
$$\frac{i_1}{i_2} = -\frac{n_2}{n_1} = -n$$

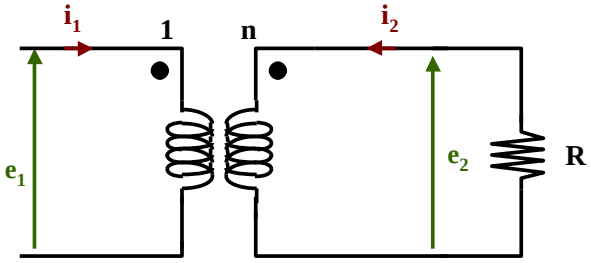
or by



$$\frac{e_1}{e_2} = \frac{n_1}{n_2} = -\frac{1}{n}$$
$$\frac{i_1}{i_2} = n$$

NB : the signs given in the previous relationships can be different if the conventional direction of the voltages v_1 and v_2 and the currents i_1 and i_2 are defined differently.

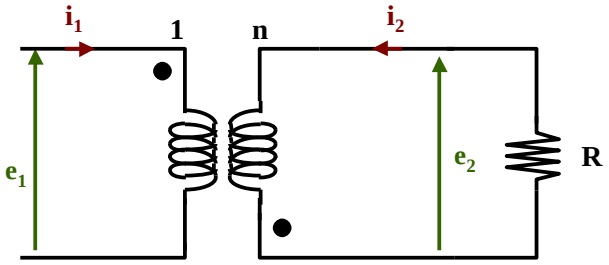
II.2.3 impedance reflected back to the primary of a perfect transformer



$$e_1 = \frac{e_2}{n}$$
$$i_1 = -n i_2$$
$$\Downarrow$$
$$\frac{e_1}{i_1} = -\frac{e_2}{i_2}\frac{1}{n^2}$$

Consequently, the impedance at the primary of a perfect transformer corresponding to the previous diagram writes as follows

$$\frac{\boldsymbol{e_1}}{\boldsymbol{i_1}} = \boldsymbol{R}\frac{\boldsymbol{1}}{\boldsymbol{n^2}} \Leftrightarrow \boldsymbol{Z_e} = \frac{\boldsymbol{Z_s}}{\boldsymbol{n^2}}$$



$$e_1 = -\frac{e_2}{n}$$
$$i_1 = n i_2$$
$$\Downarrow$$
$$\frac{e_1}{i_1} = -\frac{e_2}{i_2}\frac{1}{n^2}$$

Consequently, the impedance at the primary of a perfect transformer corresponding to the previous diagram writes as follows

$$\frac{e_1}{i_1} = -R\frac{1}{n^2} \Leftrightarrow Z_e = -\frac{Z_s}{n^2}$$

III MANIPULATION : POWER TRANSISTOR MATCHING (IN CLASS A)

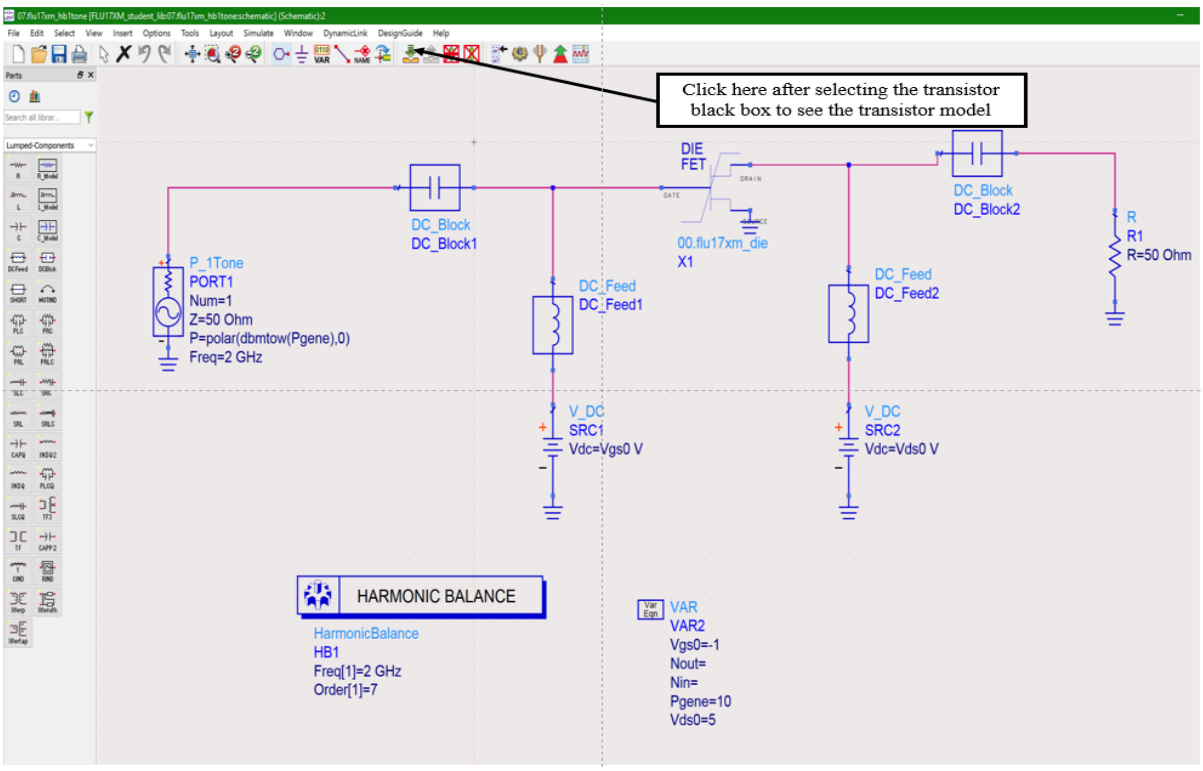
III.1 OUTPUT MATCHING

In this part, the aim is to match (**in terms of power**) the field effect transistor used in the previous experimental PWs in a narrowband around the frequency of 2 GHz to a purely resistive load of value R_0=50Ω connected at the output of the transistor.

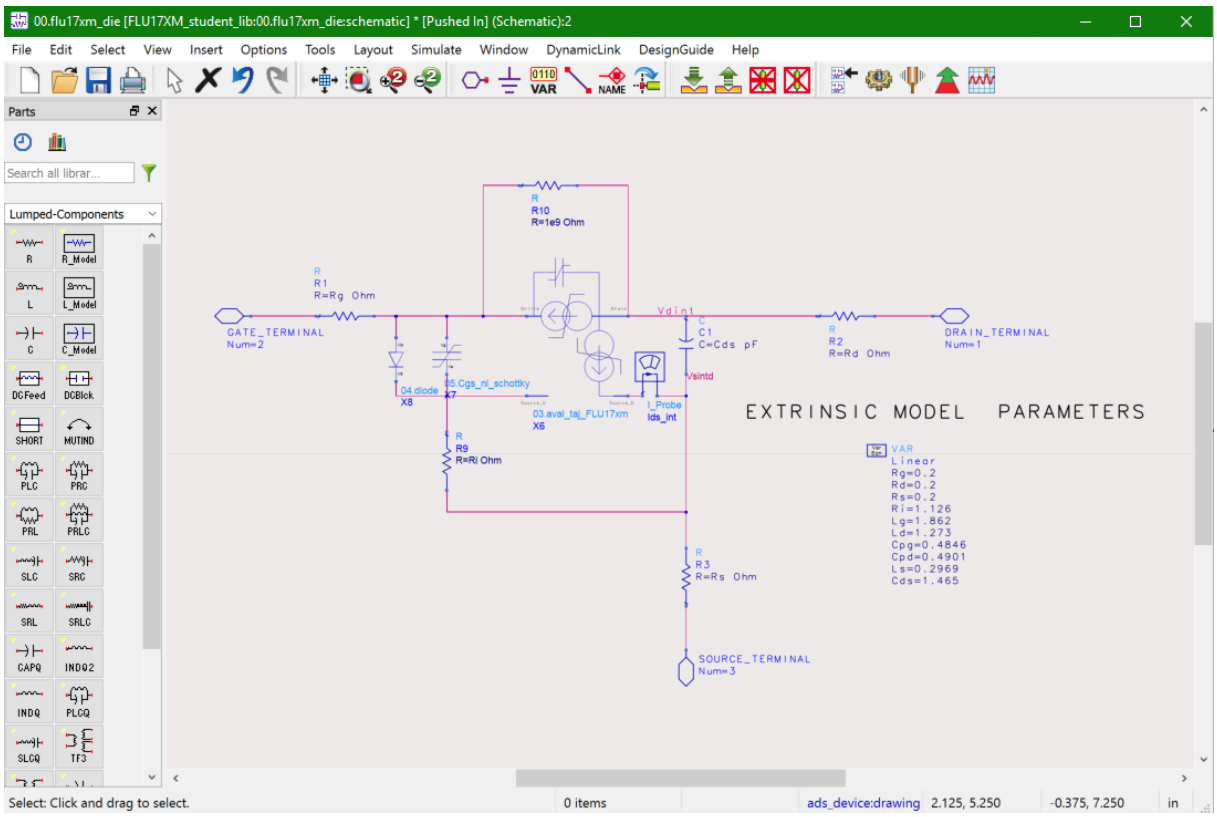
III.1.1 Cancellation of the imaginary part of the transistor output impedance

Question : What elements can we connect at the transistor output in order to cancel the imaginary part of the output impedance at the frequency of 2 GHz? What kind of resonant circuit can we use here? Then give the good matching relations at the output. Give the results of the numerical applications.

To help you answer this question, open the file *07.flu17xm_hb1tone.dsn*. The symbol of the extrinsic nonlinear model (**Die Model**) of the transistor and the two bias tee are then shown. Help: the non-linear model of the extrinsic transistor is described in the file *00.flu17xm_die.dsn*, you can edit this file by selecting the symbol of the transistor and clicking on it



and this will open the file *00.flu17xm_die.dsn*

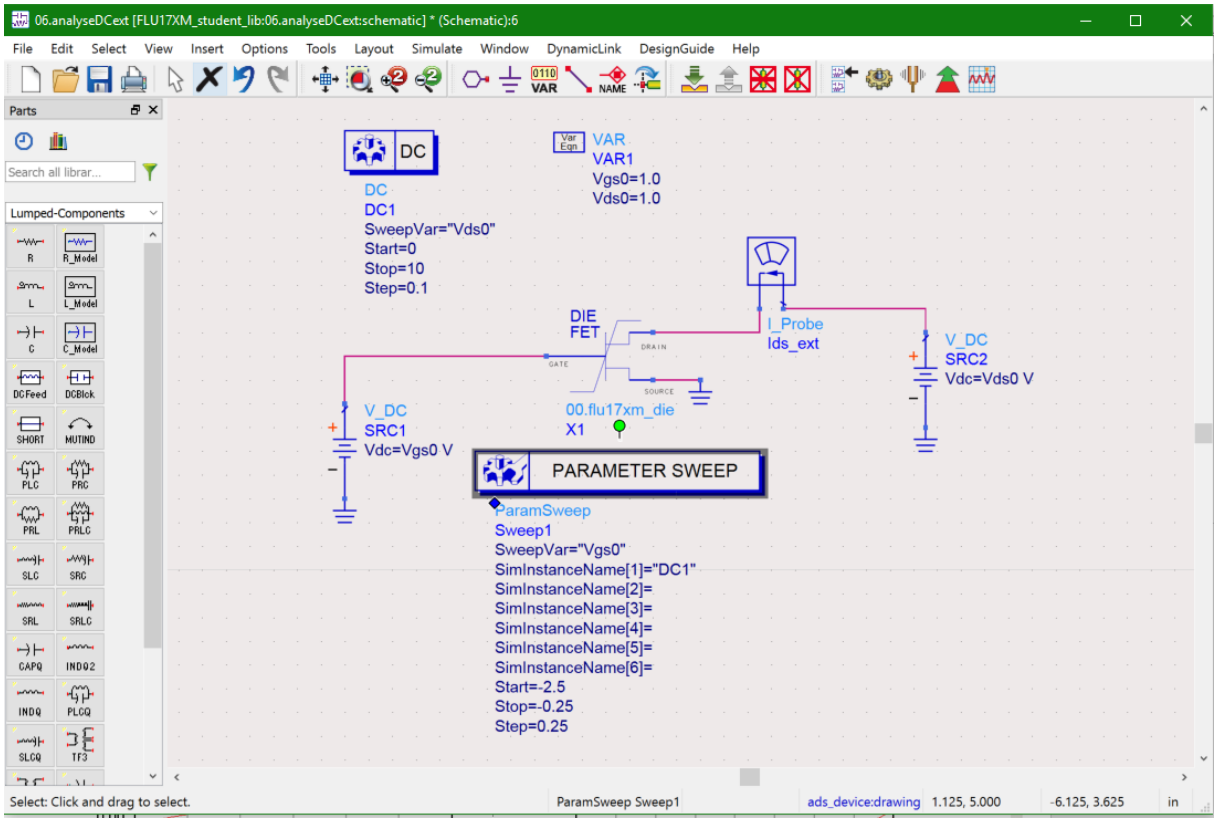


III.1.2 Matching of the real part of the transistor output impedance

Question : Give the transistor diagram when the imaginary part has been canceled.

What elements can we connect at the transistor output in order to match the real part of the output impedance at the frequency of 2 GHz?

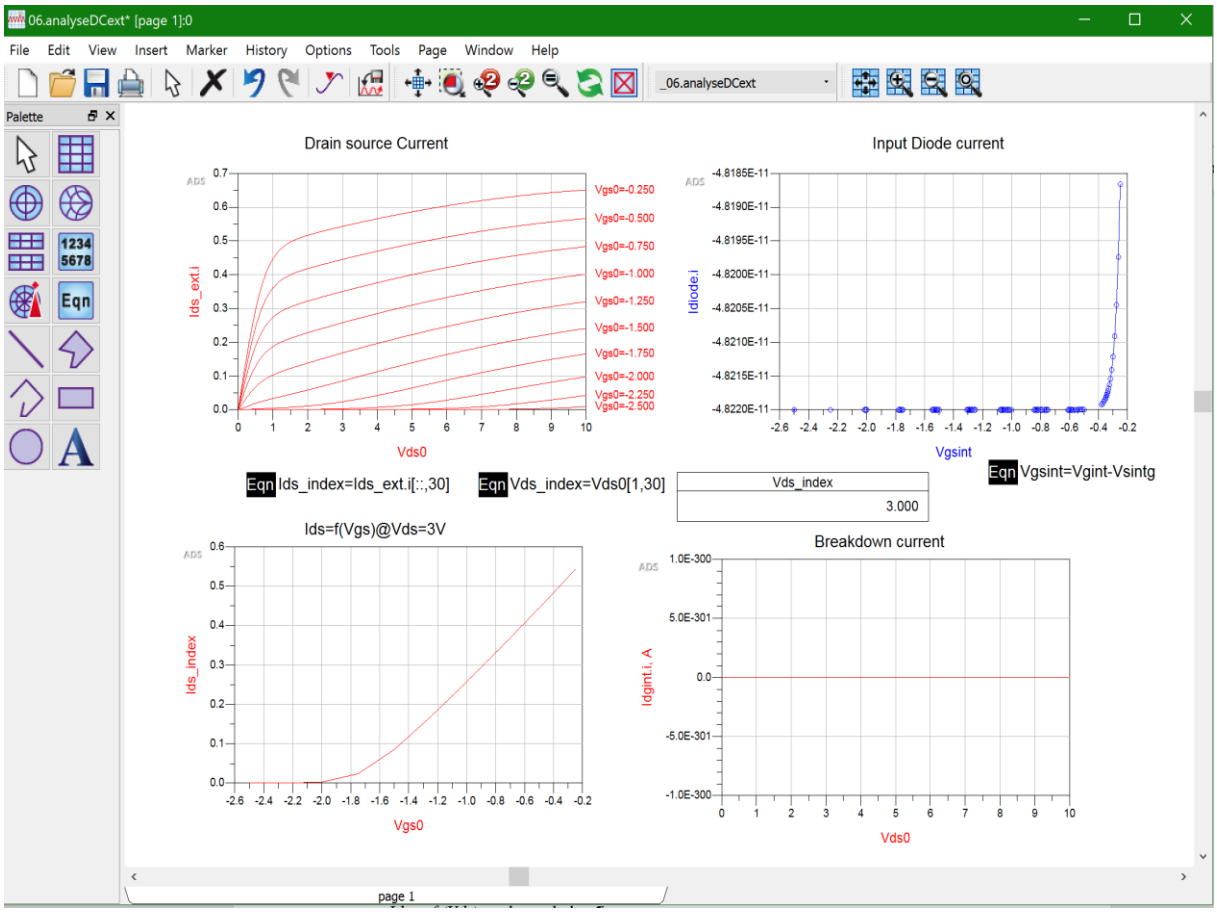
To help you answer this question, open the file *06.analyseDCext.dsn* you have done in the previous PW.



Start the simulation to plot the static I/V curves of the extrinsic transistor for the following ranges of V_{DS} and V_{GS}:

- V_{GS} : from -2.5V to -0.25V with a 0.25V step,
- V_{DS} : from 0V to 10V with a 0.1V step.

From the "data display" window called "*06.analyseDCext*", you will zoom on the network of curves *Ids = f (Vds)* as shown below



You will obtain the following display

From this graph, you will give the value of

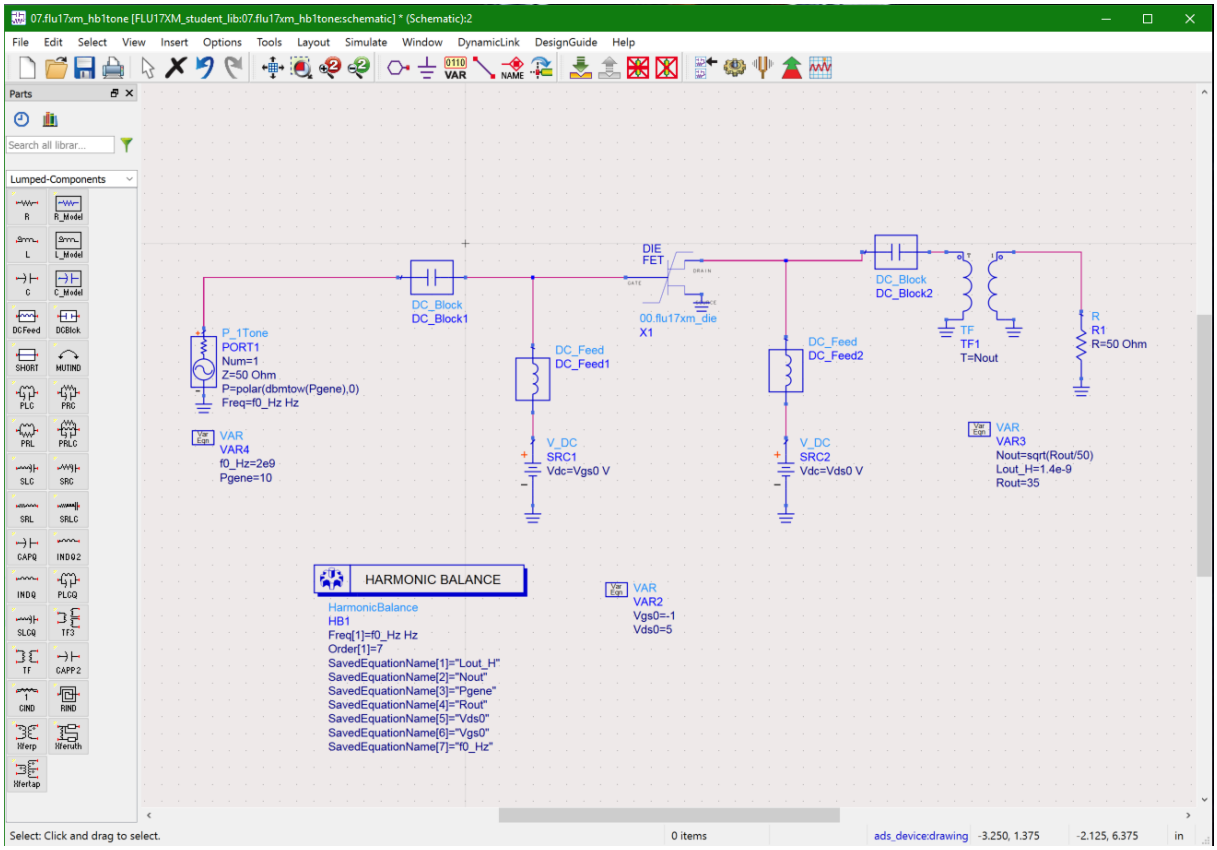
- the maximum voltage excursion around V_{ds} = 5 V (DC bias point in class A) in order to maximize the output power,
- the maximum current excursion around $I_{ds} = I_{dss}/2$ (DC bias point in class A) in order to maximize the output power

Then, you will deduce

- the maximum power available at the transistor output once adapted,
- the value of the resistance R_{out} to insert at the transistor output,
- the value of the transformer turns ratio N_{out}.

III.1.3 Simulation of the output matched transistor

The following schematic will help you to realize as a first step the output transistor matching (i.e. delete all the input matching elements at this stage):



- Modify the frequency: we want to match the FET at the frequency of 2 GHz
- Enter the number of harmonics of the ‘’Harmonic Balance’’ simulation to take into account
- Set the power of the generator to 10 dBm. You have to match the FET at a high level (to define with the teacher). This initial power must therefore be modified according to the simulation results obtained to achieve the high level matching.
- Enter the values of L_{out} and N_{out} find previously. They are the initial values required to start the first simulation.
- Modify the value of L_{out} in order to obtain a correct load line in class A and to optimize the power at the output of the FET. Give the definition of a correct load cycle.
- Write some additional equations to define the extrinsic input impedance of the FET. Compare with the intrinsic input impedance. Conclude.

III.2 INPUT MATCHING

In this part, the aim is to match (**in terms of power**) the field effect transistor used in the previous experimental PWs in a narrowband around the frequency of 2 GHz to a generator having a purely resistive internal load of value R_0=50Ω connected at the input of the transistor.

III.2.1 Cancellation of the imaginary part of the transistor input impedance

Question : What elements can we connect at the transistor input in order to cancel the imaginary part of the input impedance at the frequency of 2 GHz? What kind of resonant circuit can we use here? Then give the good matching relationships at the input. Give the results of the numerical applications.

Using the value of the input impedance find during the transistor output matching, compute again the previous results. Conclude.

You have to add in the schematic : the correct element cancelling the imaginary part of the input impedance of the transistor.

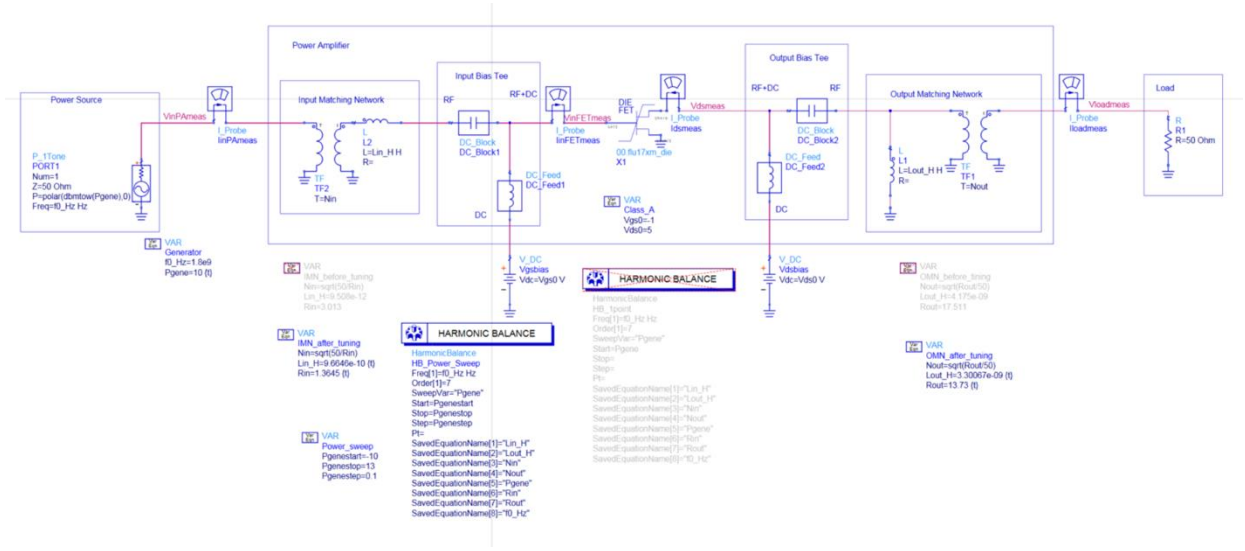
III.2.2 Matching of the real part of the transistor input impedance

Question : Give the transistor diagram when the imaginary part has been canceled. What elements can we insert at the input of the transistor to match the real part of the input impedance of the transistor to a 50 Ω load (the internal impedance of the generator) at the frequency of 2 GHz?

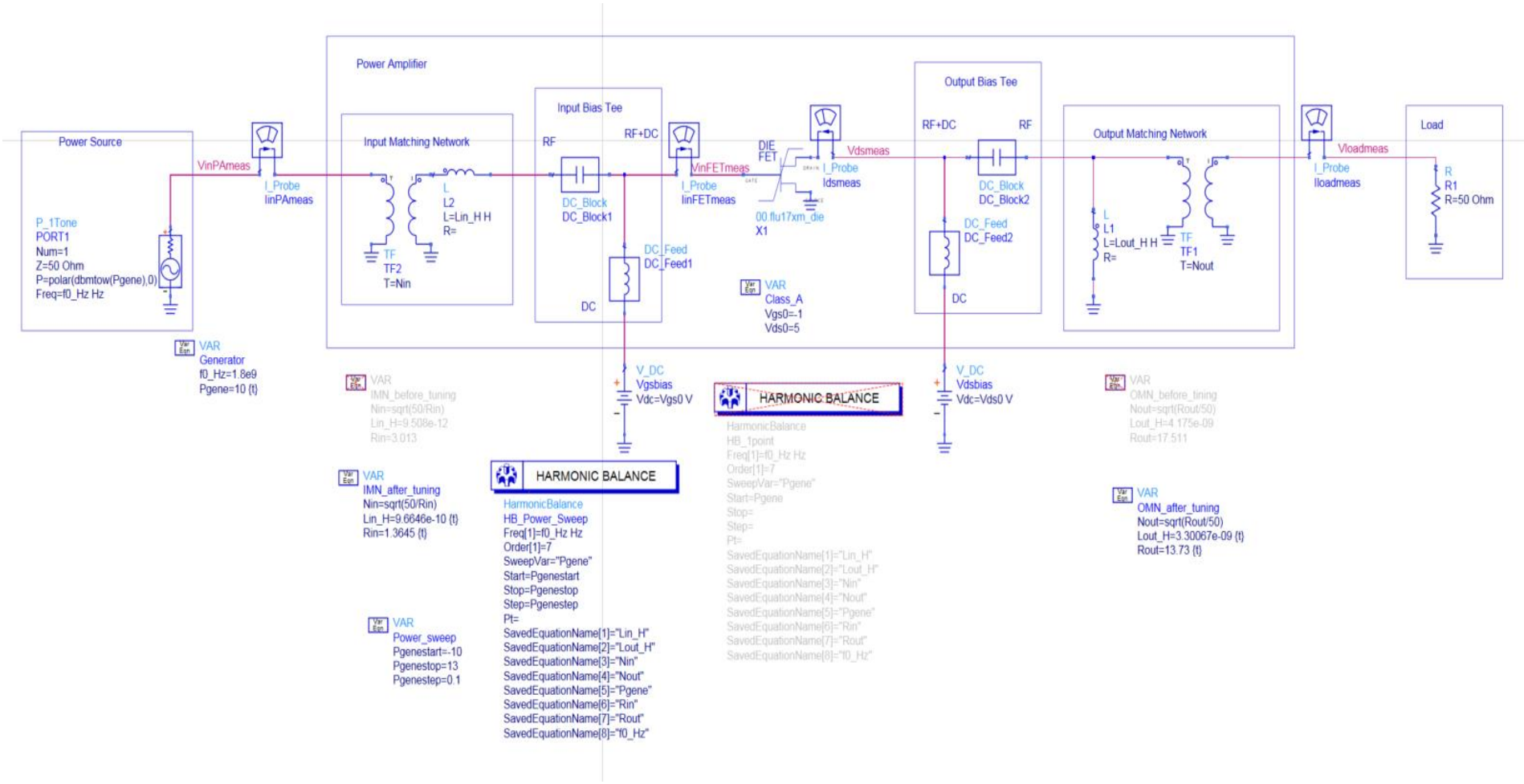
You have to add in the schematic : the correct element matching the real part of the input impedance of the transistor.

III.2.3 Simulation of the matched transistor (input and output)

The following schematic you have to reproduce will help you to realize the input matching of the transistor



- On the data display window, add a Smith chart in order to observe the input impedance of the transistor. Enter the equation related to the input reflection coefficient Γ_{in}.
- Use the same optimal power of the generator used during the high level output impedance matching of the transistor.
- Enter the values of L_{in} and N_{in} find previously. They are the initial values required to start the first simulation.
- Modify L_{in} and N_{in} in order to optimize the input impedance of the FET. Verify simultaneously the results obtained in terms of power, matching and efficiency.
- Plot the following characteristics : Ps=f(Pe) ; Gp= f(Ps) ; PAE= f(Ps).



IV MANIPULATION: LOW-LEVEL SIMULATION OF THE TRANSISTOR IN CLASS A.

This matching is performed at a low level. Select a generator power of 0 dBm. The DC bias point does not change:

- V_{DS} = 5 Volts (unchanged)
- Choose V_{GS} to work with a DC bias current of Idss/2.

Start again the entire matching procedure in these new conditions. To do so, perform as before the matching of the transistor output and input in order to optimize the load cycle and the input matching. Conclude.

Plot the following characteristics: Ps=f(Pe) ; Gp= f(Pe) ; η_{aj}= f(Pe). Conclude.

V MANIPULATION : HIGH-LEVEL SIMULATION OF THE TRANSISTOR IN CLASS AB

This matching is performed at a high level. Modify the generator power accordingly.

Modify the DC bias point of the transistor to work in (deep) AB class:

- V_{DS} = 5 Volts (unchanged)
- Choose V_{GS} to work with a DC bias current of Idss/10.

Start again the entire matching procedure in these new conditions. To do so, perform as before the matching of the transistor output and input in order to optimize the load cycle and the input matching. Conclude.

Plot the following characteristics : Ps=f(Pe) ; Gp= f(Ps) ; PAE= f(Ps).Conclude.