Semester S1

Basics of active and non linear electronics

RF Power amplifiers (JM Nebus)

COURSE N° 5

Chapter V : Load modulated Power amplifier
(Doherty power amplifier : DPA)

I] Motivations

We want to design a power amplifier having an efficiency which remains at a high value even if the input RF power decreases from the maximum input power at saturation ($Vgs=Vgs_{max}$) to a lower input power ($Vgs=Vgs_{max}/2$) .

Doing so we can have a high average efficiency for useful input modulated signal having a varying instantaneous envelope power as mentioned in chapter I .

Let us consider class B operation of a transistor.

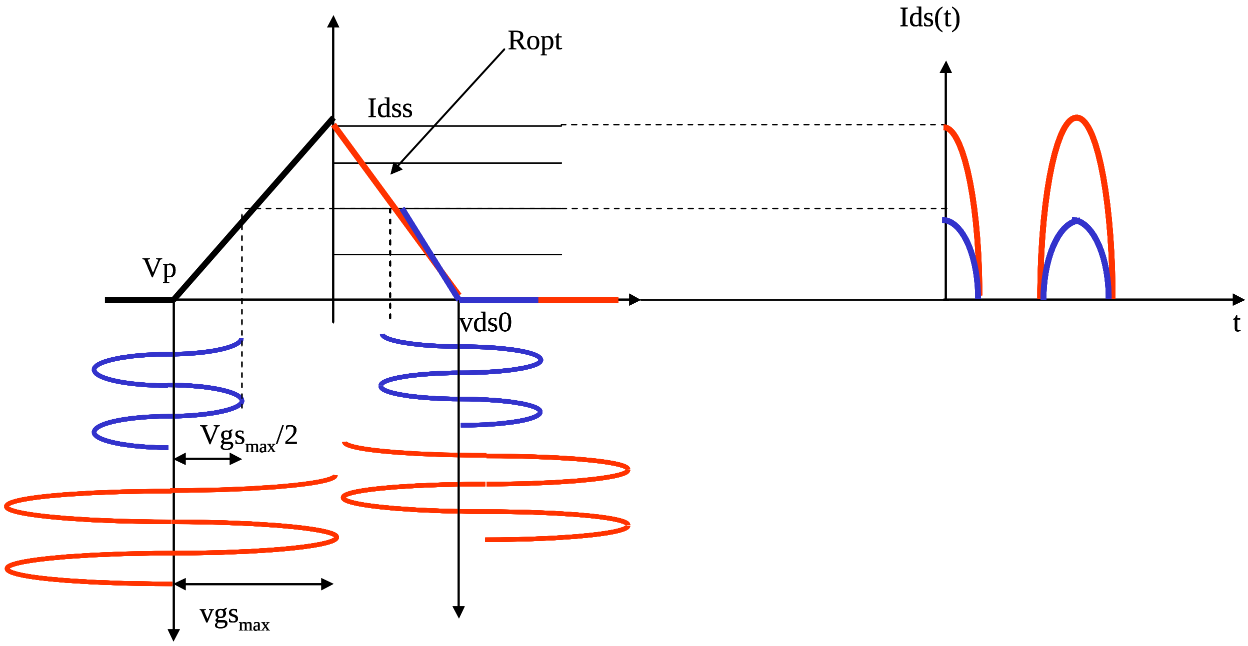


Figure 1

If the load resistance remains constant and at its optimal value (Ropt) for maximum output power , we can see that the RF drain voltage swing decreases if the input gate source voltage decreases as represented in Figure 1 .

If we take for example, Vds0=30V , Vk=Vdsmin= 5V and Idss=1A

- **For Vgs1= Vgsmax= -Vp (high input power level)**

Ropt = 50Ω , Pout = 6.25W and ηd=65.5 % , Vds1 = 25V and Ids1= 0.5 A

- **For Vgs1= Vgsmax / 2 (medium input power level)**

Vds1 = Ropt . Idss/4 =12.5 V and Ids1 = 0.25 A

Pout= 3.125W and ηd=33%

The drain efficiency decreases drastically because Vds1 is reduced

We can plot the representative RF power and efficiency characteristics as shown in figure 2

When Vgs is divided by 2 , the input RF power is divided by 4

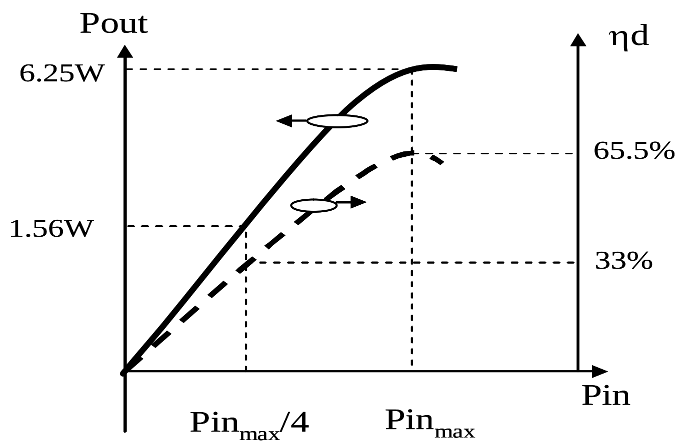
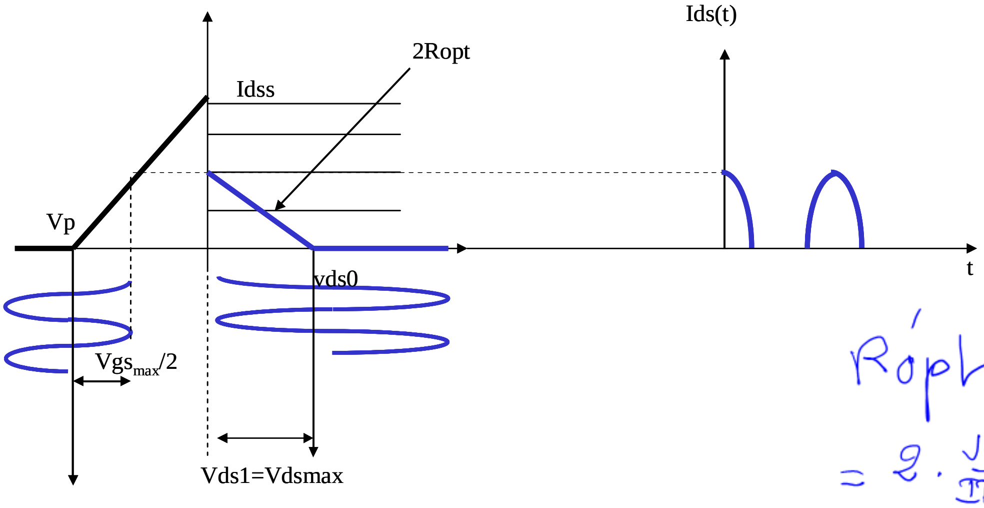


Figure 2

In order to maintain a high efficiency value when the input power decreases we can modify the optimal load resistance (R’opt) to have a higher drain voltage swing Vds1 .

The maximum achievable value of Vds1 is equal to 25V

So we need to have R’opt = 2Ropt as depicted in, figure 3



$$R'opt = \frac{V_{DS1}}{\frac{I_{DSS}/2}{2}} = 2 \cdot \frac{V_{DS1}}{I_{DSS}/2} = 2\,Ropt$$

Figure 3

In this case we obtained the power characteristics plotted in figure 4 .

Calculations give: R’opt = 100Ω , P’out max = 3.125W and η’d=65.5 %

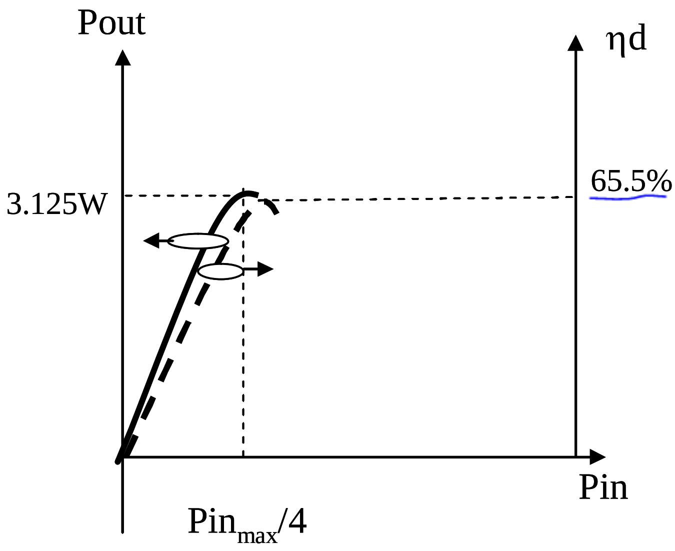


Figure 4

Consequently the aim of load modulation is to target a drain efficiency curve having the shape shown in figure 5 . For this purpose the load resistance needs to be varied from 2Ropt to Ropt when the input gate voltage Vgs varies from Vgsmax/2 up to Vgsmax as shown in figure 6 .

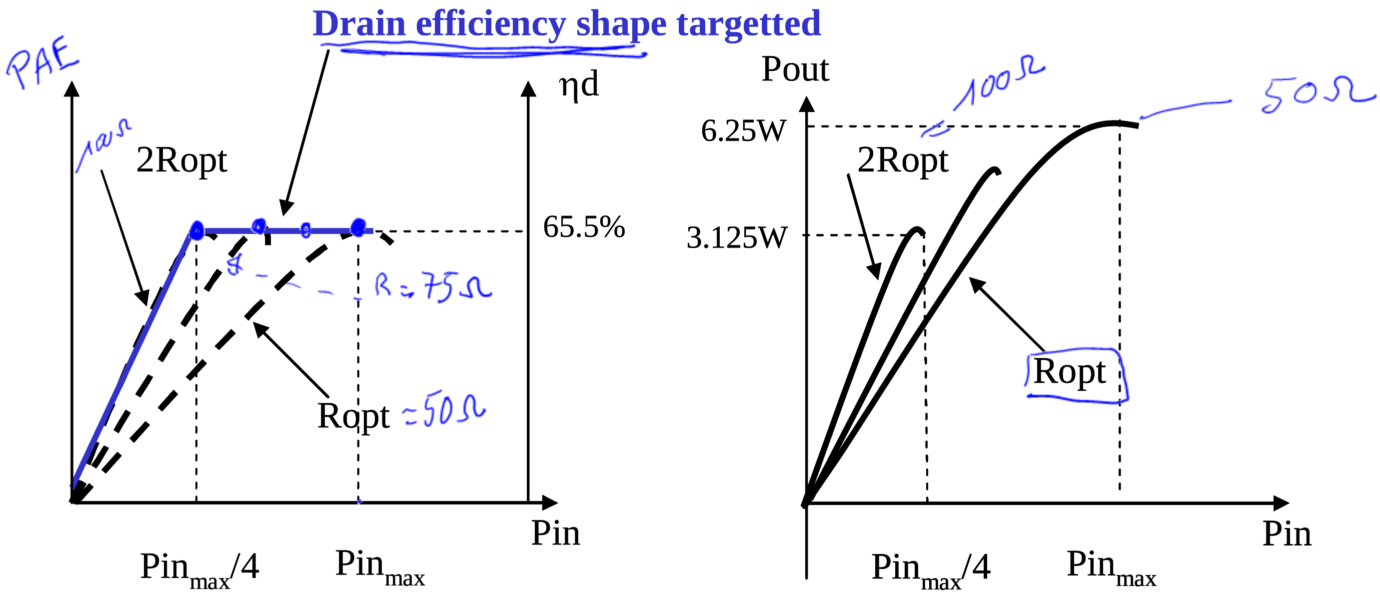


Figure 5

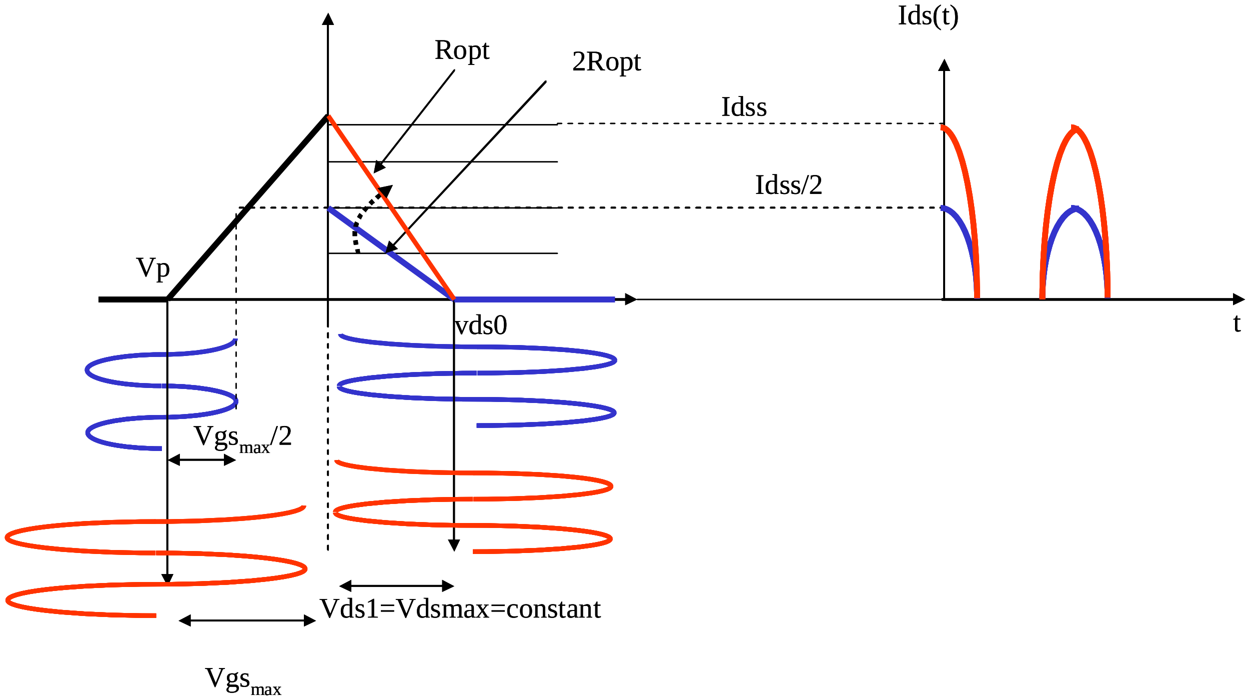


Figure 6

For Vgs lower than Vgsmax/2 , the load resistance is kept at a fixed value of 2 Ropt

II] Load modulation circuit principle (figure 7)

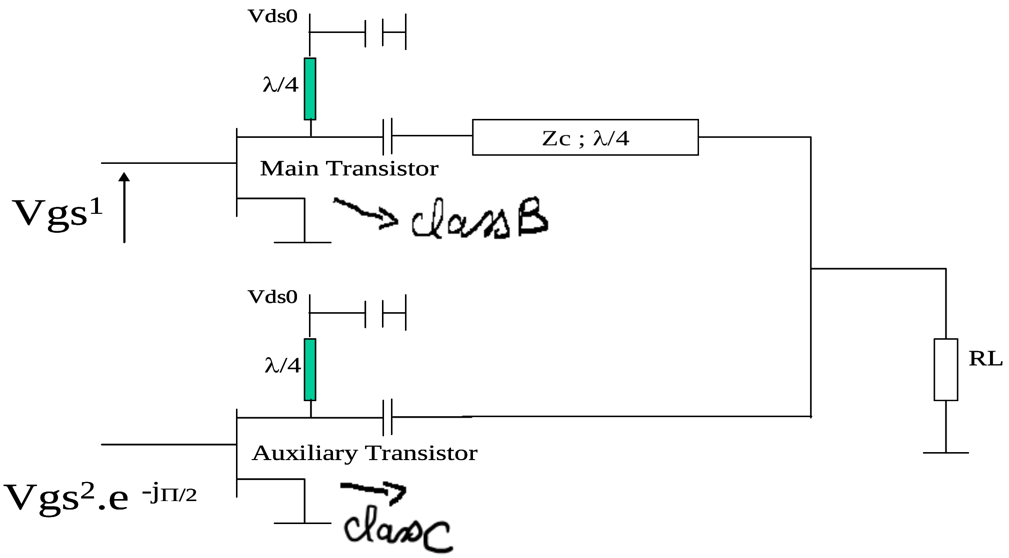


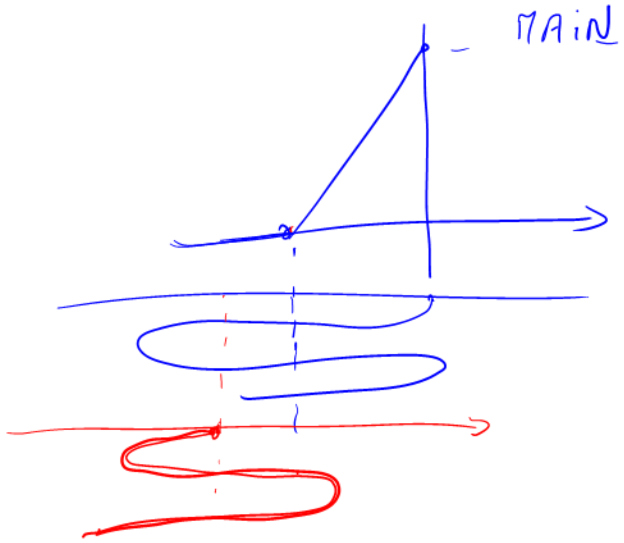
Figure 7

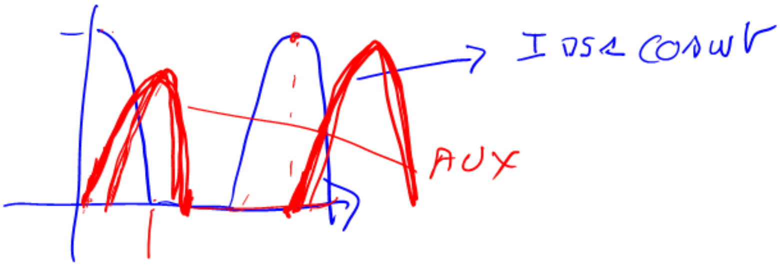
Using quaterwave line for the drain bias circuit , second harmonic of the drain currents are terminated into a short circuit .

We consider also that higher harmonics are small and not taken into account in the following.

The gate source voltage that drives the auxiliary transistor is applied when the gate source voltage of the main transistor is higher than Vg_{smax} /2 . Below this value the auxiliary transistor is considered to be turned off .

This could be realised by using a Class C auxiliary transistor while the main transistor is operating in class B .

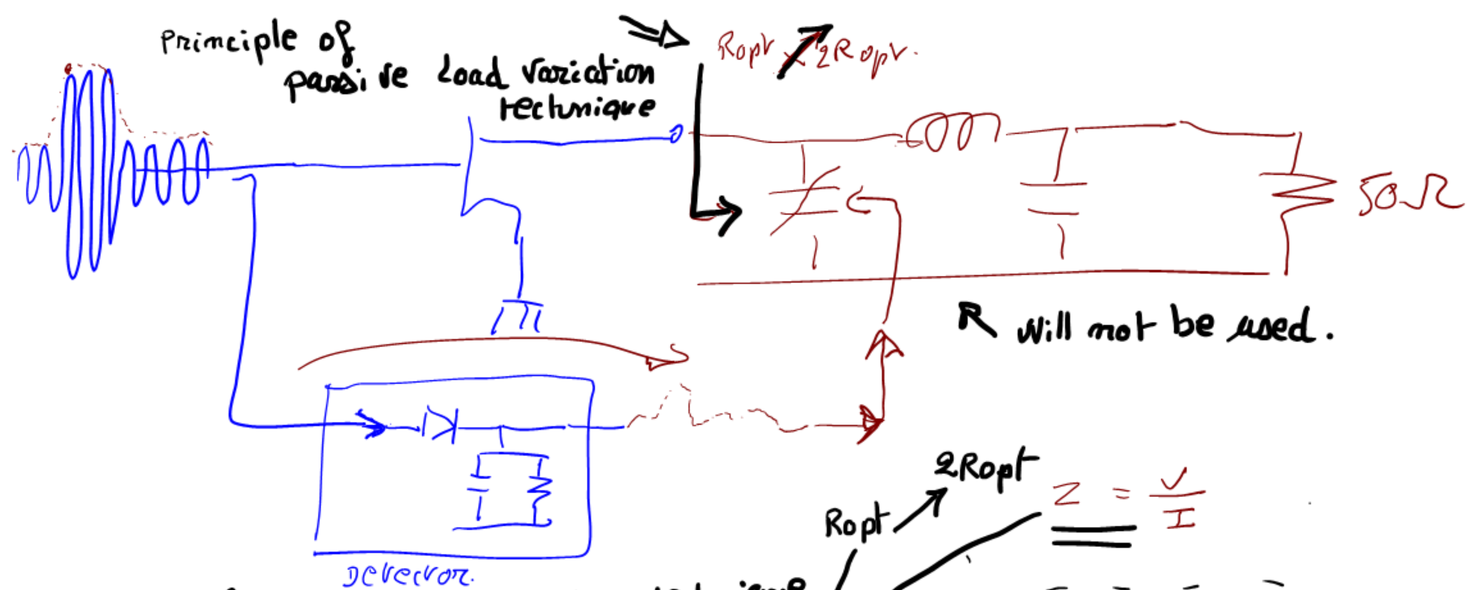




$$\cos \omega\left(t - \frac{T}{4}\right) \longrightarrow$$

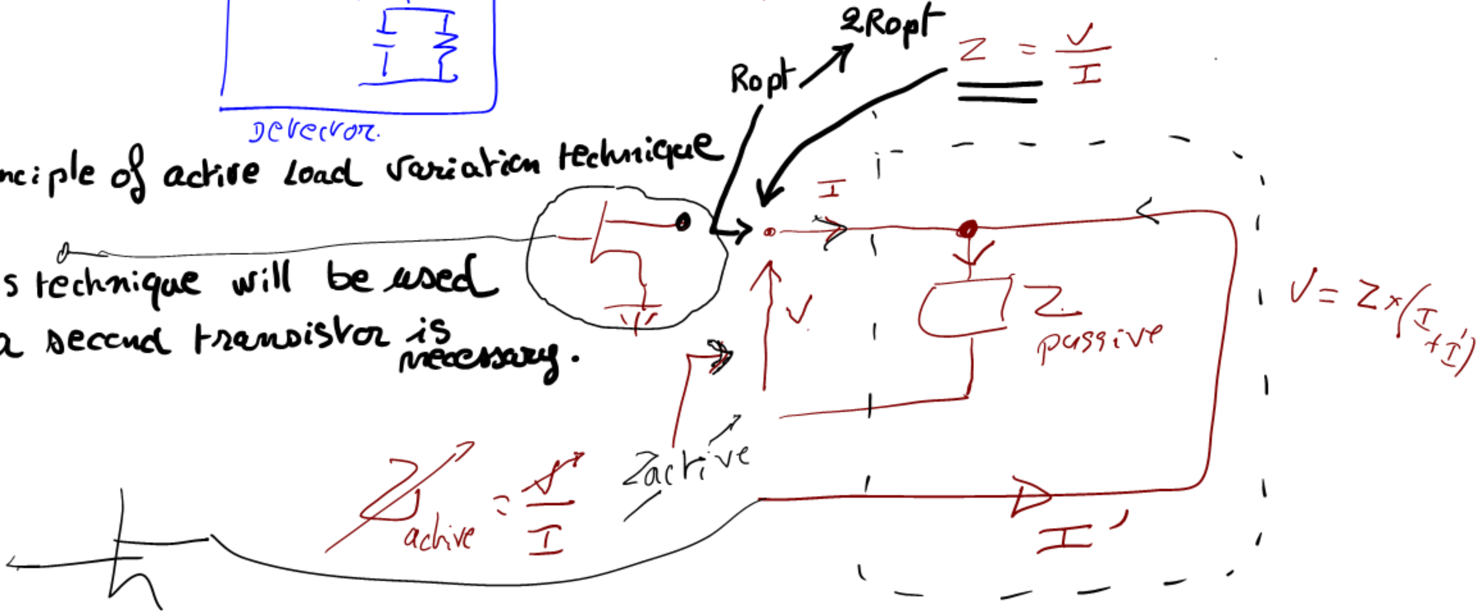
$$\cos\left(\omega t - \frac{2\pi}{T}\frac{T}{4}\right) = \cos\left(\omega t - \frac{\pi}{2}\right)$$

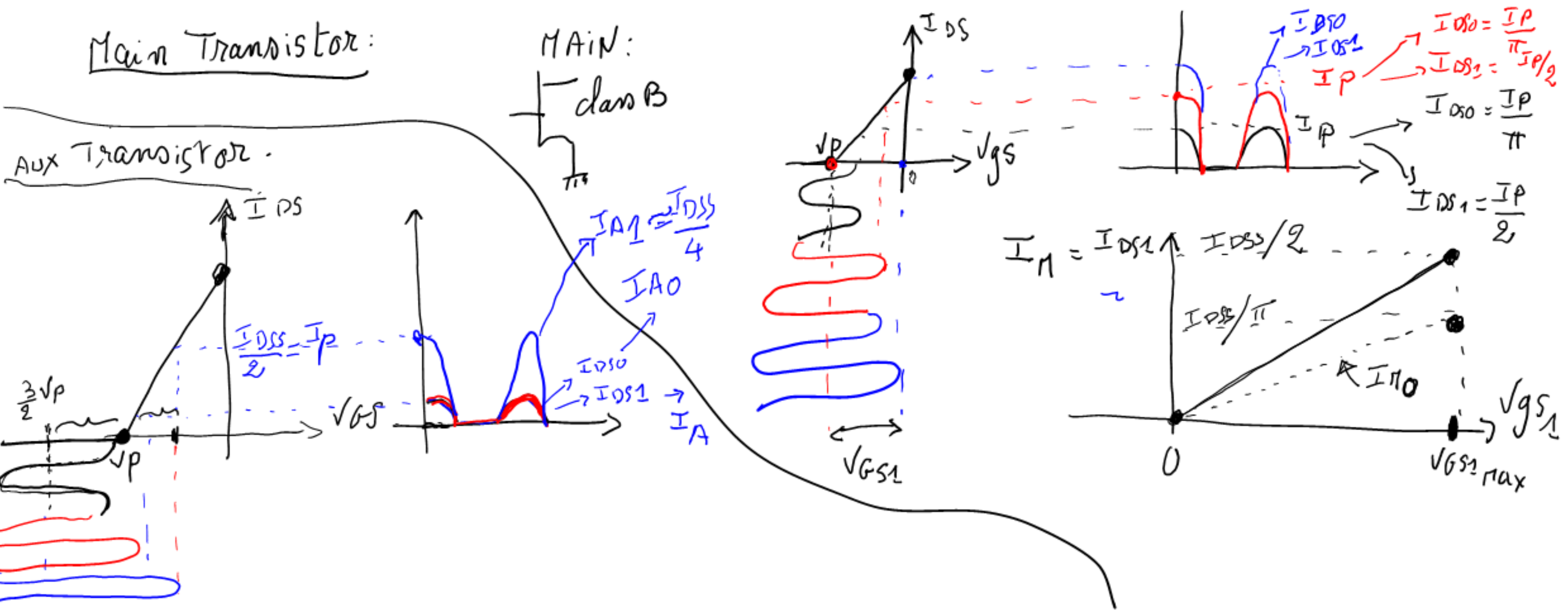
Principle of passive load variation technique



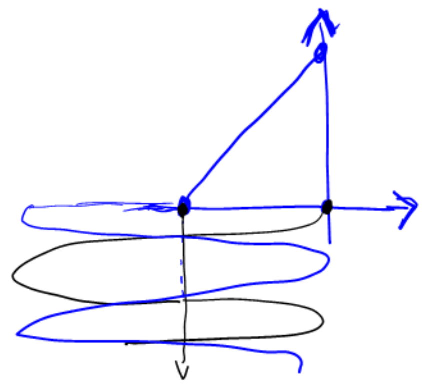
Principle of active load variation technique

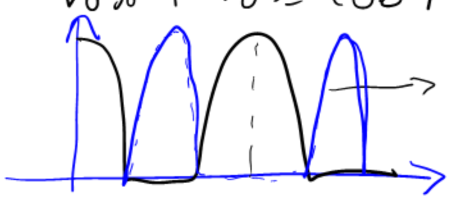
This technique will be used
a second transistor is necessary.





$V_{GS0} + V_{GS1}\cos\varphi = V_p$.





$\to I_{DS0} + I_{DS1}\cos\omega t + I_{DS2}\cos(2\omega t)$

$I_{DS}(t) = I_{DS}\left(t - \frac{T}{2}\right)$

$I_{DS}(t) = I_{DS0} + I_{DS1}\cos\omega\left(t - \frac{T}{2}\right) + I_{DS2}\cos\left(2\omega\left(t-\frac{T}{2}\right)\right)$

$I_{DS}(t) = I_{DS0} - I_{DS1}\cos\omega t + I_{DS2}\cos(2\omega t)$

The equivalent circuit at the fundamental operating frequency is given in figure 8

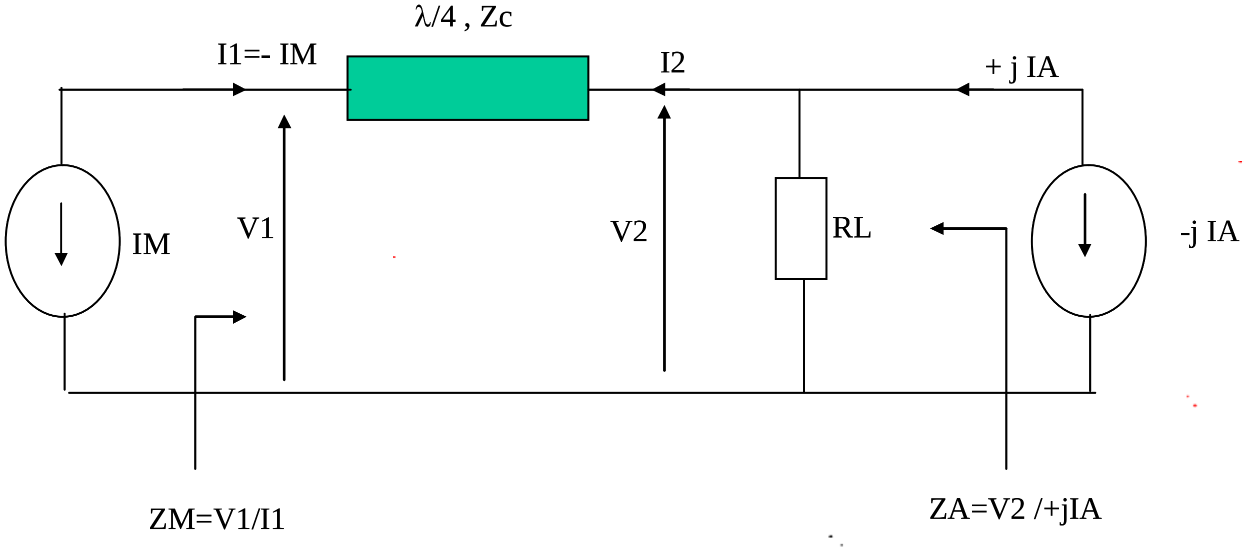


Figure 8

$$\begin{pmatrix} V1 \\ I1 \end{pmatrix} = \begin{pmatrix} 0 & jZc \\ \frac{j}{Zc} & 0 \end{pmatrix} \cdot \begin{pmatrix} V2 \\ -I2 \end{pmatrix}$$

$$V_1 = -jZ_c I_2 \qquad I_2 = jI_A - \frac{V_2}{R_L} \qquad Z_M = \frac{V_1}{I_1} = \frac{-jZ_c(jI_A - \frac{V_2}{R_L})}{-I_M} = \frac{Z_c^2}{R_L} - Z_c\frac{I_A}{I_M}$$

$$I_1 = \frac{jV_2}{Z_c} \qquad V_2 = -jZ_c I_1 = +jZ_c I_M \qquad Z_A = Z_c\frac{I_M}{I_A}$$

When I_A=0 (auxiliary off) we want to have Ropt

$$Z_M = \frac{Z_c^2}{R_L} = 2Ropt$$

$$\frac{Ropt^2}{R_L} = 2Ropt \longrightarrow R_L = \frac{Ropt}{2}$$

At maximum output power of both transistors ($I_M = I_A$) we want to have

$$Z_M = Z_A = Ropt$$

This leads to

$$Z_C = Ropt \qquad R_L = \frac{Ropt}{2}$$

The variations of the currents I_M and I_A versus Vgs are given in figure 9 :

(linear variations of both the fundamental and DC value for class B operation)

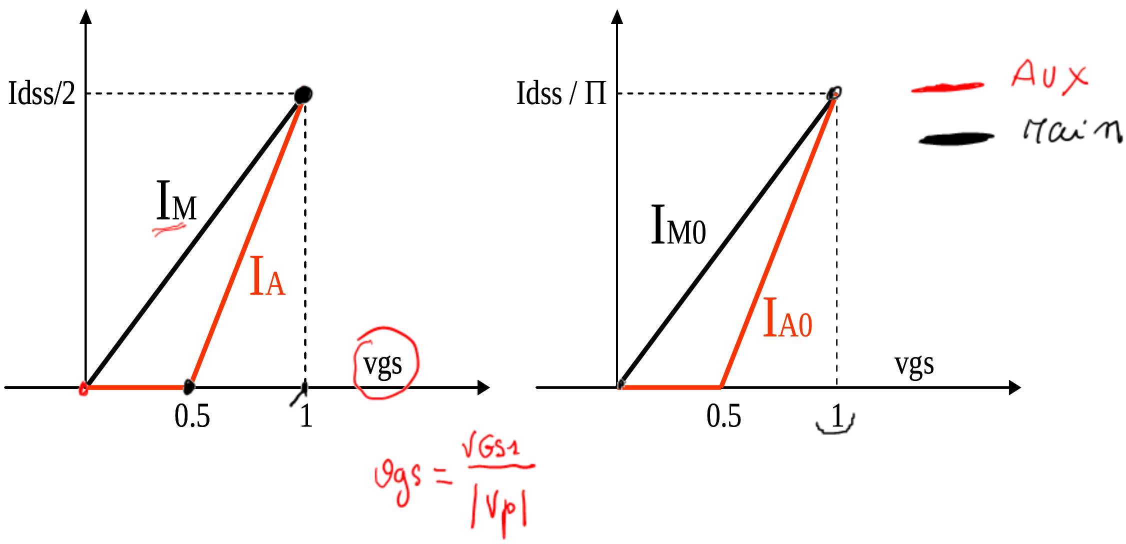


Figure 9

I_M and I_A are fundamental frequency components of currents while I_{M0} and I_{A0} are DC components of currents .

vgs is here normalized to - Vp . It varies between 0 and 1

- Equations of current components are :

$$I_M = \frac{Idss}{2}\cdot vgs \qquad I_{M0} = \frac{Idss}{\pi}\cdot vgs \longrightarrow \underbrace{\text{For } 0<vgs<1}$$

$$I_A = Idss\cdot vgs - \frac{Idss}{2} \qquad I_{A0} = (Idss\cdot vgs - \frac{Idss}{2})\cdot\frac{2}{\pi} \longrightarrow \underbrace{\text{For } 0.5<vgs<1}$$

- Equations of load impedances are :

$$\underbrace{Z_M = \frac{Z_C{}^2}{R_L}} \qquad Z_A = \infty \qquad \text{For } 0<vgs<0.5$$

IM ≠ 0
IA = 0

IA ≠ 0 IM ≠ 0

$$\underbrace{\underbrace{Z_M} = \frac{Z_C{}^2}{R_L} - Z_C(2-\frac{1}{vgs})} \qquad \underbrace{Z_A = Z_C\cdot\left(\frac{1}{2-\frac{1}{vgs}}\right)} \qquad \text{For } 0.5<vgs<1$$

Zc = Ropt :
RL = Ropt/2 → vgs = 0.5 → $Z_M = \frac{Z_C{}^2}{R_L} = \frac{(Ropt)^2}{Ropt/2} = 2Ropt$

vgs = 1 → $Z_M = \frac{Z_C{}^2}{R_L} - Z_C = \frac{Ropt^2}{\frac{Ropt}{2}} - Ropt = Ropt$

Load impedance variations versus vgs are plotted in figure 10

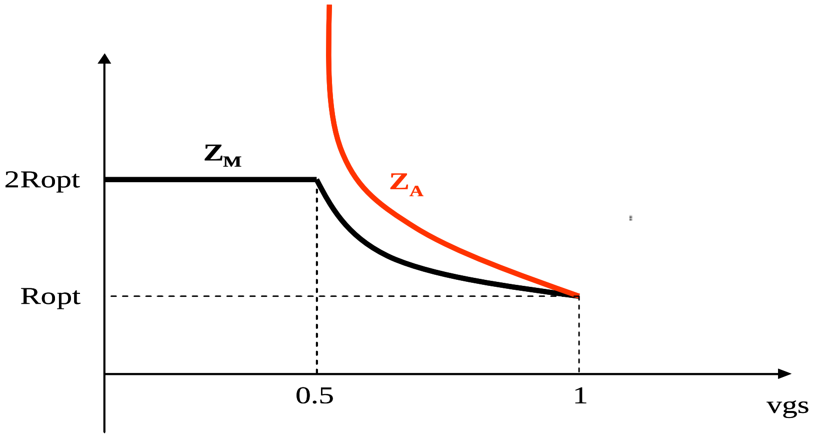


Figure 10

- **Equations of Voltages are** :

$$= |V2|$$

$$V1 = V_M = Z_M \cdot I_M = \frac{Z_C^{\,2} \cdot Idss}{2R_L} \cdot vgs \qquad |V_A| = Z_C \cdot I_M = \frac{Ropt \cdot Idss}{2} \cdot vgs$$

For 0<vgs<0.5

? VA = V2 (initial chain matrix of λ/4)

$$V_M = Z_M I_M$$

$$V_M = \frac{Ropt \cdot Idss}{2} \qquad |V_A| = Z_C \cdot I_M = \frac{Ropt \cdot Idss}{2} \cdot vgs$$

For 0.5<vgs<1

Note that as Zc= Ropt we have the following relationship

$$\frac{Ropt\cdot Idss}{2} = \underbrace{Vds1_{max}}_{V_M} = Vds0$$

$|V_A|$

If we consider Vdsmin= Vk = 0

Plots of voltages are given in figure 11

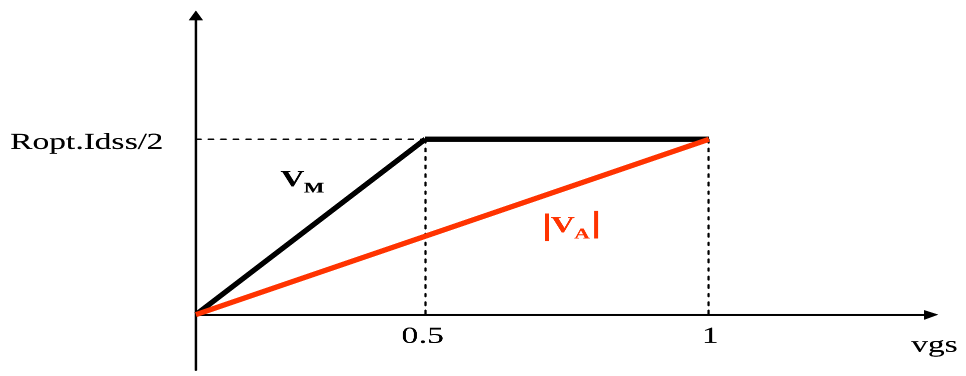


Figure 11

- **Equations of RF powers are :**

ONLY the Main is ON

For 0<vgs<0.5

$$\boxed{P_M} = \frac{1}{2}\mathrm{Re}al(\underbrace{Z_M I_1}_{V_1 \; V_M} I_1^*) = \underbrace{Ropt\frac{Idss^2}{4}\cdot vgs^2}$$

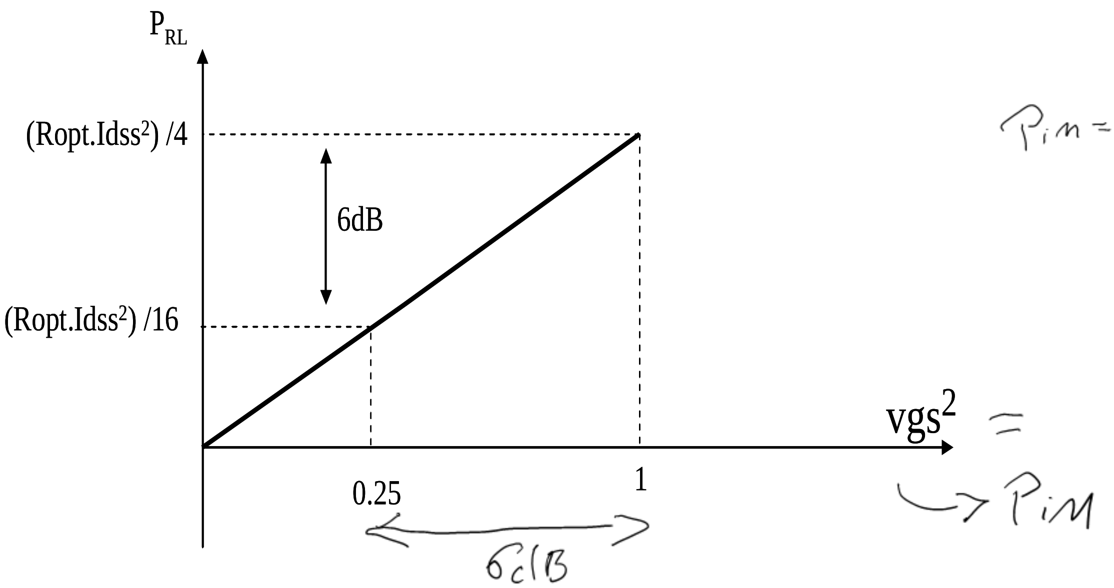
$$P_A = 0$$

$P_{our\ Amplifier} = P_M + P_A$:

For 0.5<vgs<1

$$\underbrace{P_M = Ropt\frac{Idss^2}{8}\cdot vgs} \qquad P_A = \frac{1}{2}\mathrm{Re}al\left(V_A\cdot\left(jI_A\right)^*\right) = \underbrace{\frac{1}{8}Ropt\cdot Idss^2\cdot(2vgs^2 - vgs)}$$

And $P_{RL} = P_M + P_A$



$P_{in} = \frac{1}{2} R_g C_{gs}^2 \omega^2 (V_{gs})^2$

Figure 12

- **Equations of Drain efficiency are** :

$\eta_D = \frac{P_{out}}{V_{M0} I_{M0} + V_{A0} + I_{A0}}$

V_{DS0} V_{DS0}

$$\eta_d = \frac{\pi}{4}\cdot\left(\frac{Ropt.Idss}{Vds0}\right).vgs$$

For 0<vgs<0.5

$$\eta_d = \frac{\pi}{2}\cdot\left(\frac{vgs^2}{3vgs-1}\right)$$

For 0.5<vgs<1

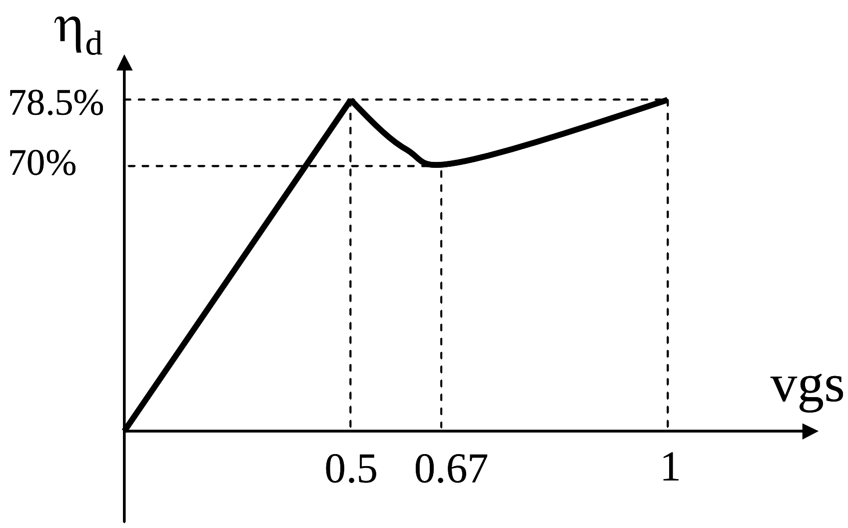


Figure 13