



Basics of Active and Nonlinear High-Frequency Electronics



UNIVERSITÀ
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Module Title

Date

- 1 -

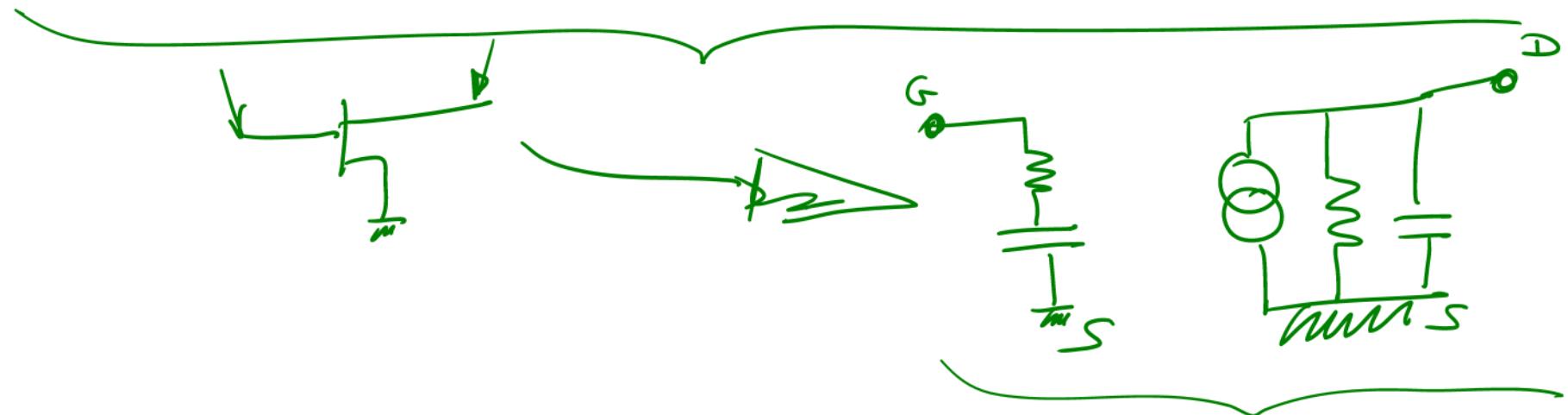
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Basics of Active and Nonlinear High-Frequency Electronics

- ❑ Chapter I : Introduction to active high-frequency circuits in communication systems
- ❑ Chapter II : Introduction to the Non-linear Electrical Modeling of microwave transistors
- ❑ Chapter III : Design method of narrow-band power amplifiers
- ❑ Chapter IV : Architectures of high-frequency mixers
- ❑ Chapter V : Architectures of wideband resistive and distributed power amplifiers
- ❑ Chapter VI : Architectures of non-linear active circuits controlled by cold HEMTs

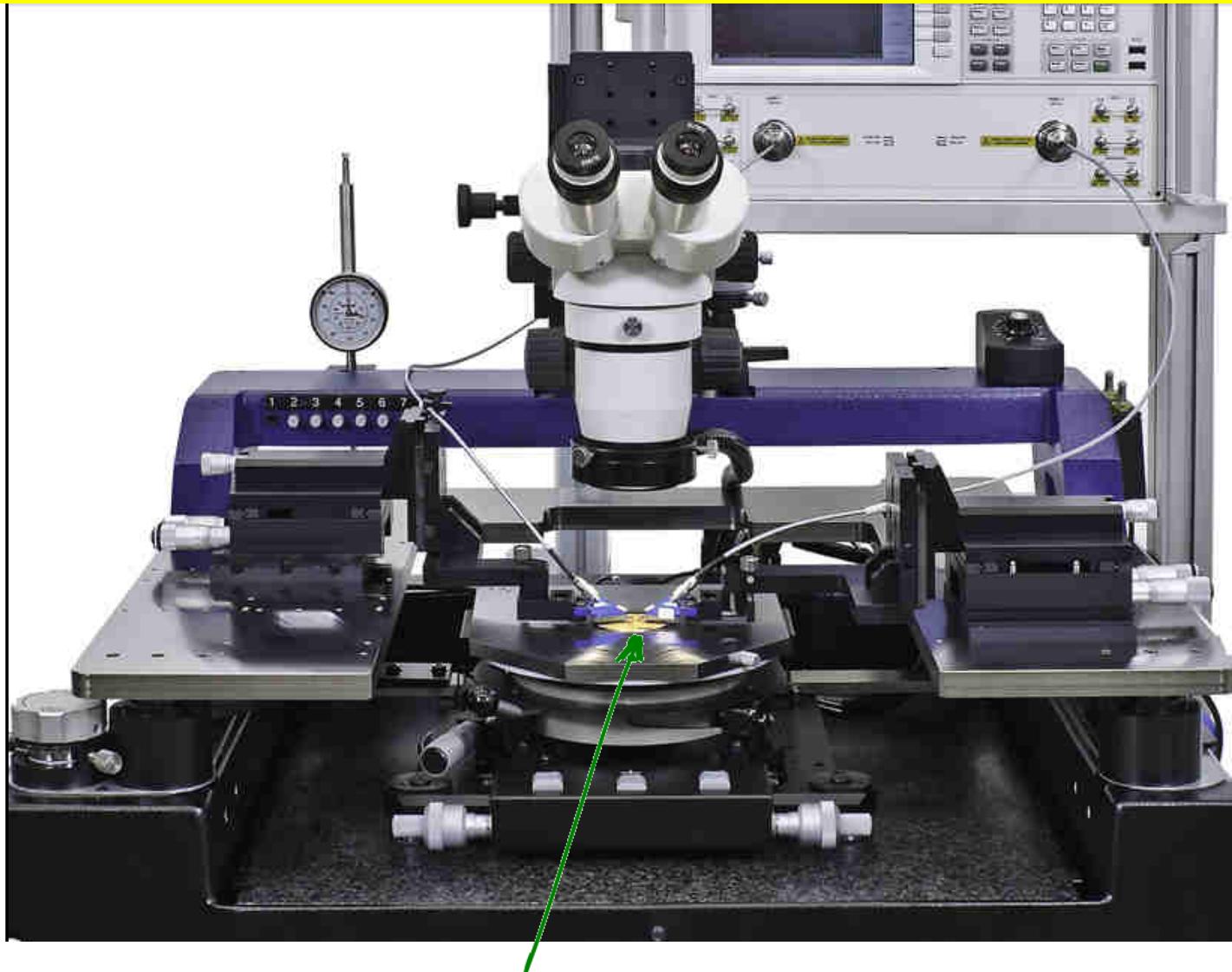
Chapter II :

Introduction to the Non-linear Electrical Modeling of microwave transistors



High-frequency Pulsed Measurement Systems

{ On-wafer Probing Stations
for RF/Microwave circuits

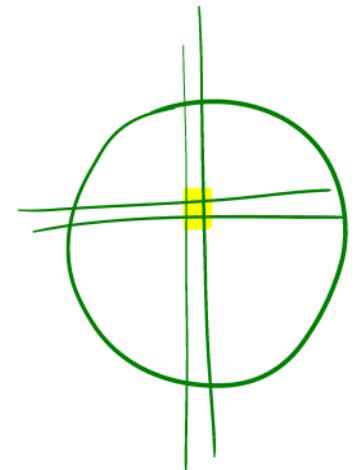
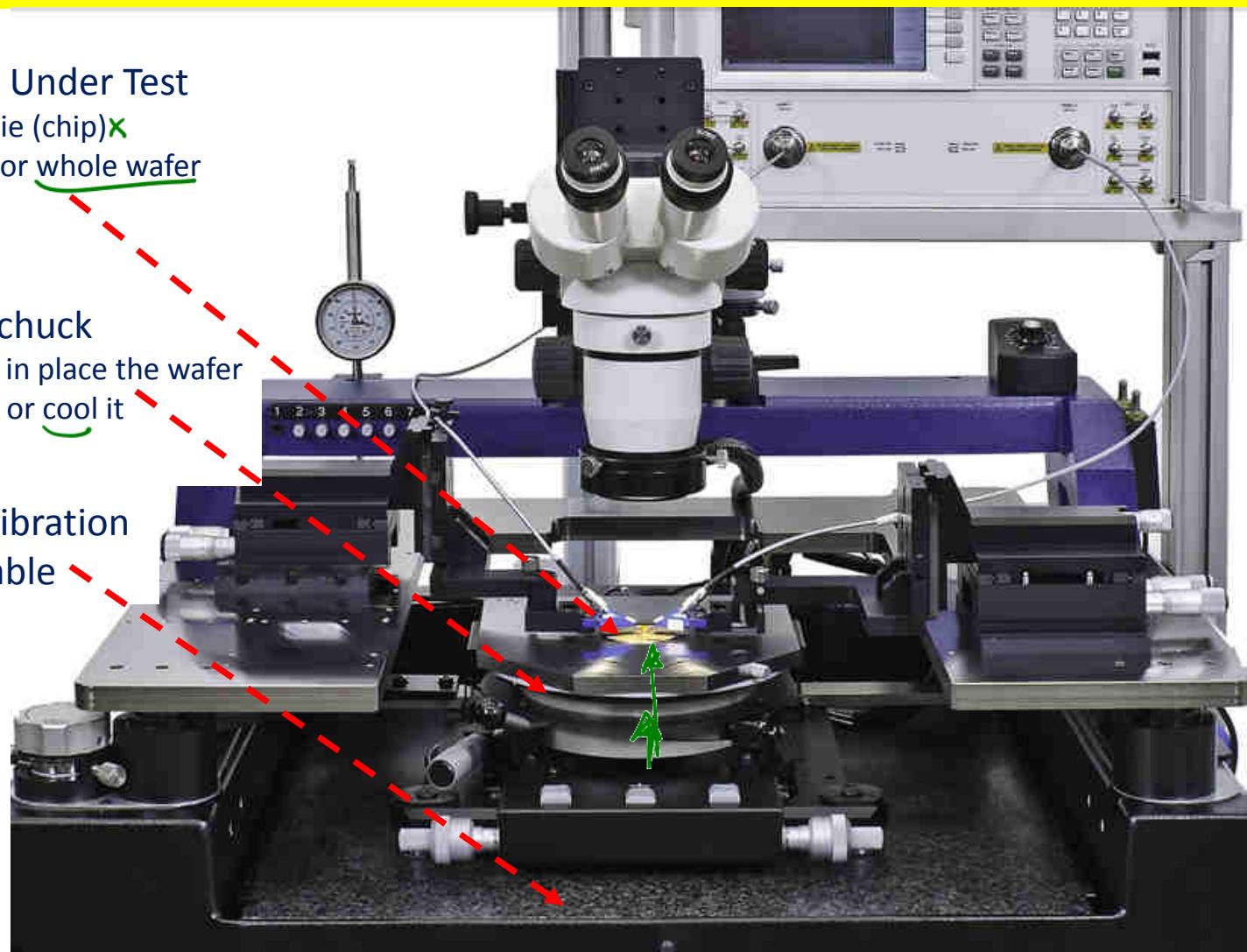


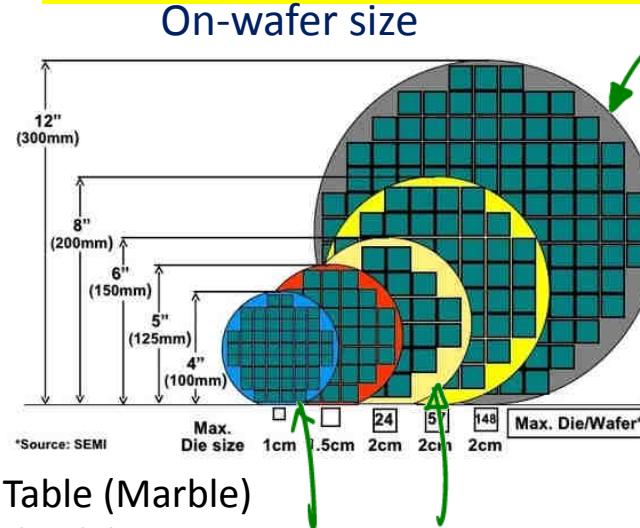
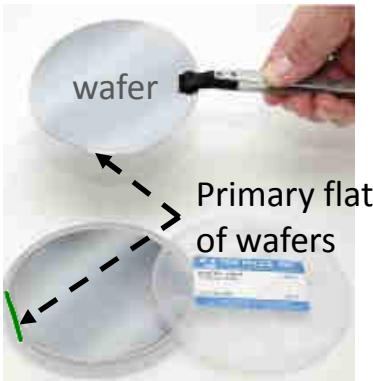
DUT

Device Under Test
- small die (chip)
- partial or whole wafer

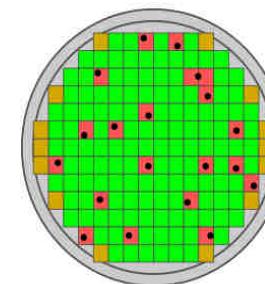
Wafer chuck
- to hold in place the wafer
- to heat or cool it

Anti- Vibration
Table

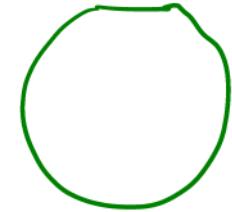




On-wafer test and sorting

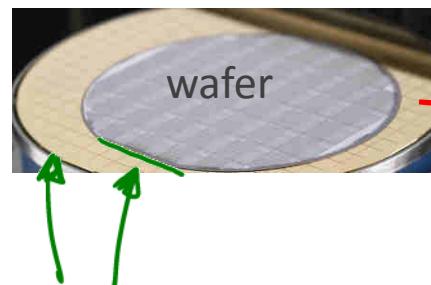
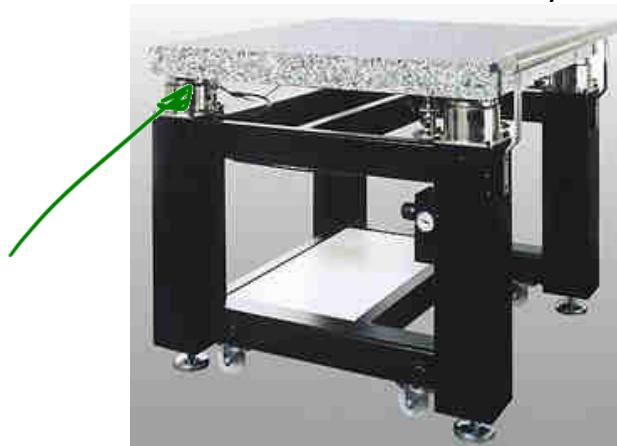


- - defect
- - defective die
- - good die
- - partial edge die



Vibration Isolation Table (Marble)

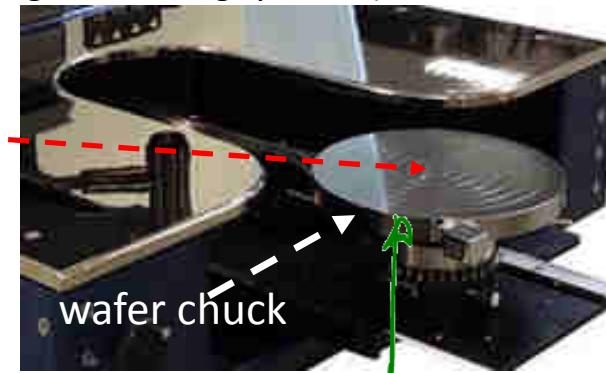
- keep high mechanical stability
- reliable sub-micron stability

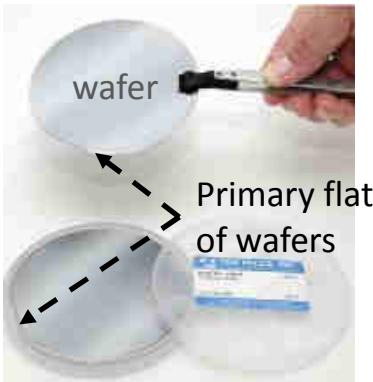


Wafer Chuck → Thermal chuck (-60°C → 300°C)

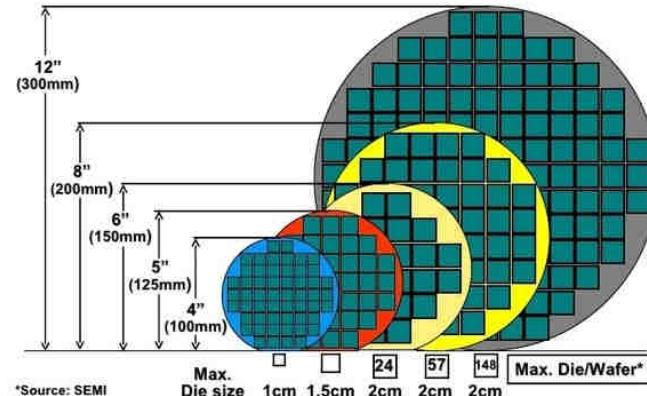
Thermal enclosure

- hold wafers in place while they are being probed
- apply a small amount of vacuum to the wafer backside
- can hold small die and partial or whole wafer
- cooling and heating systems (air flow conditioning)

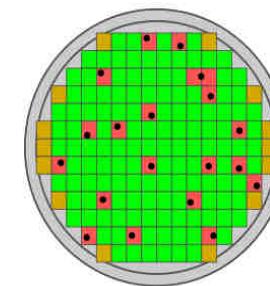




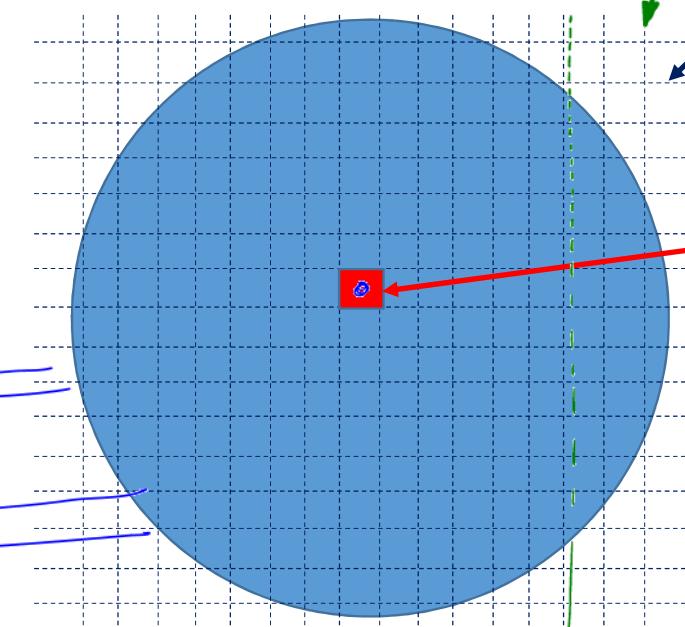
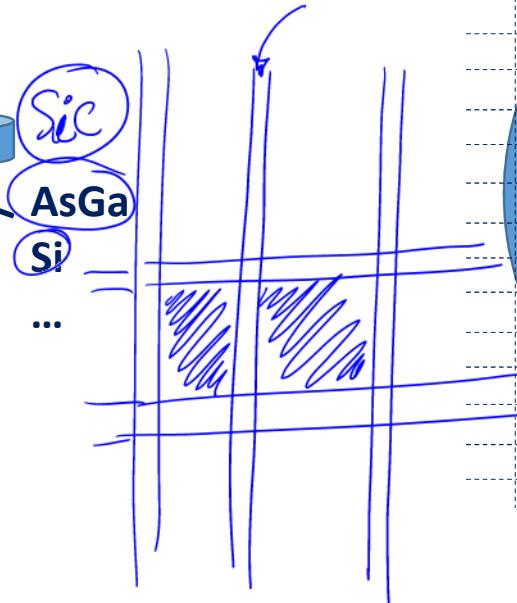
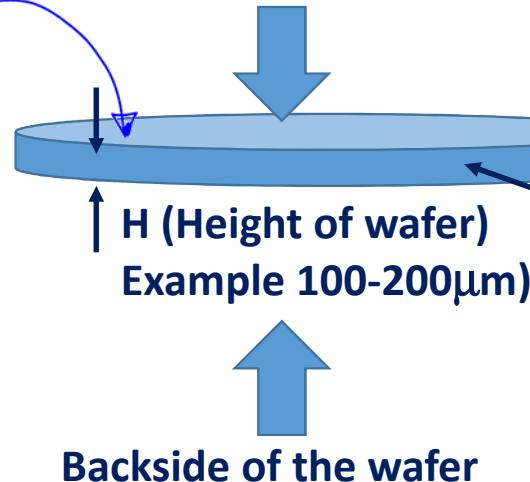
On-wafer size



On-wafer test and sorting



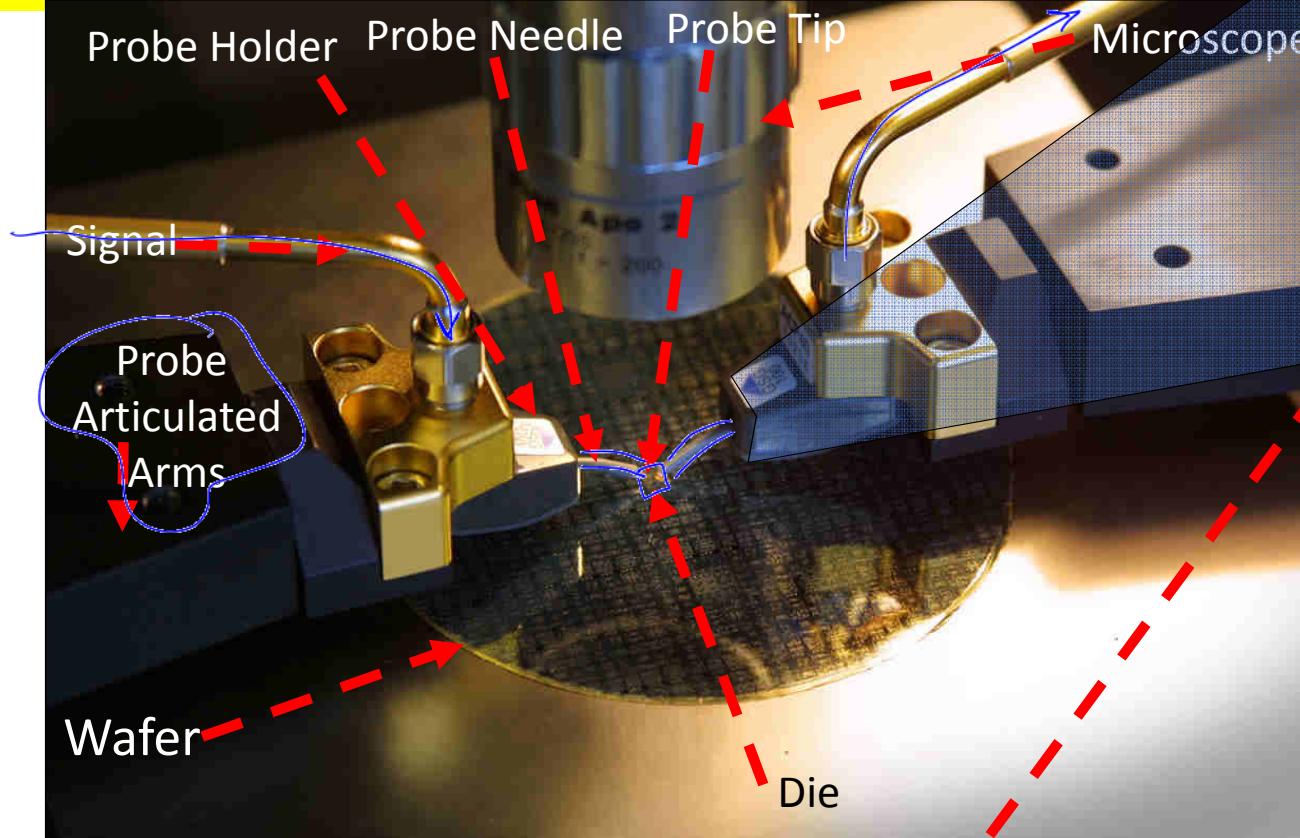
Front side of the wafer



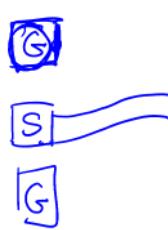
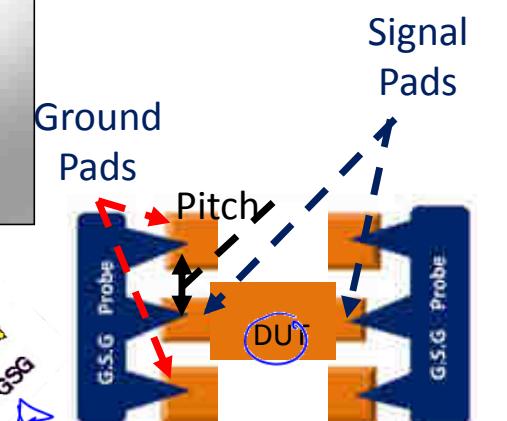
Dicing streets

Chip (die)

On-Wafer Probing

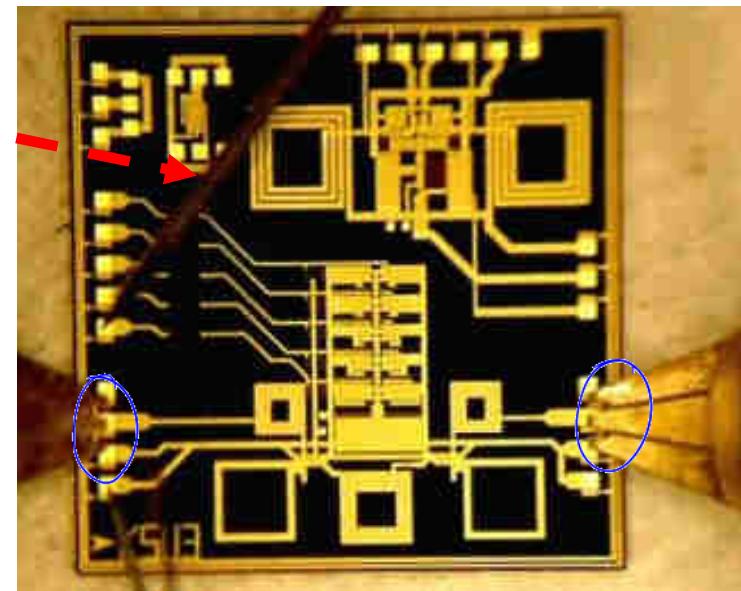
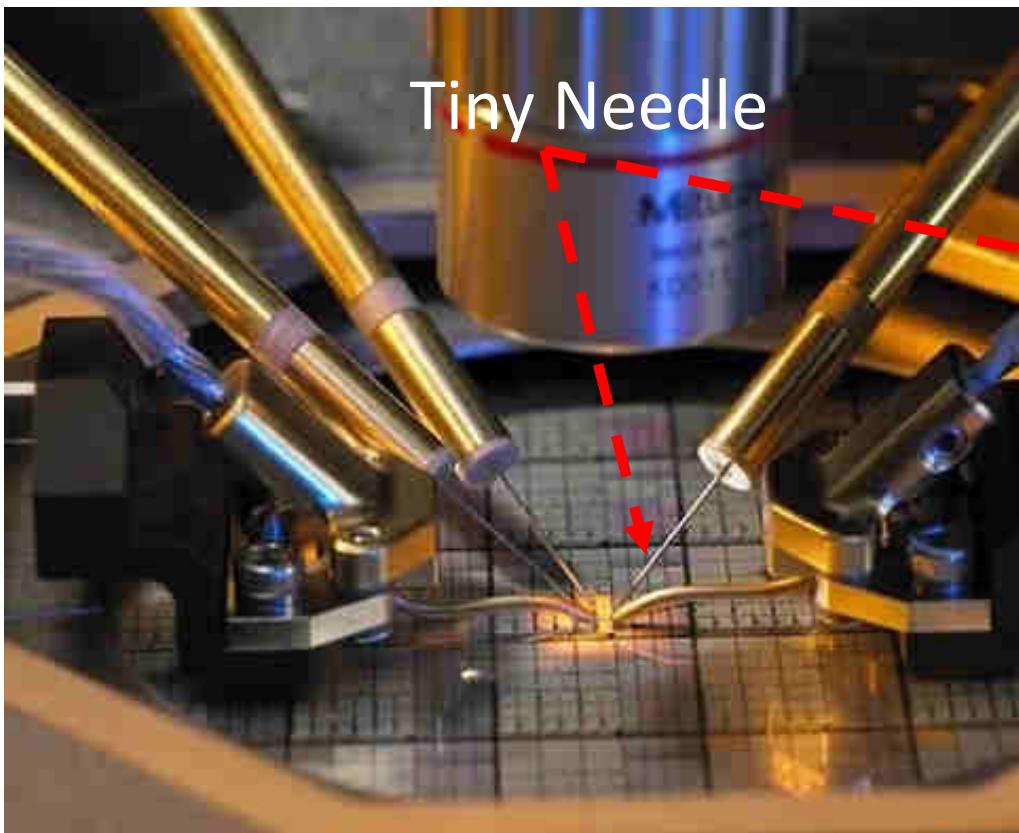


GSG is the most common type of RF probe.
Many standard pitches



GSG probes

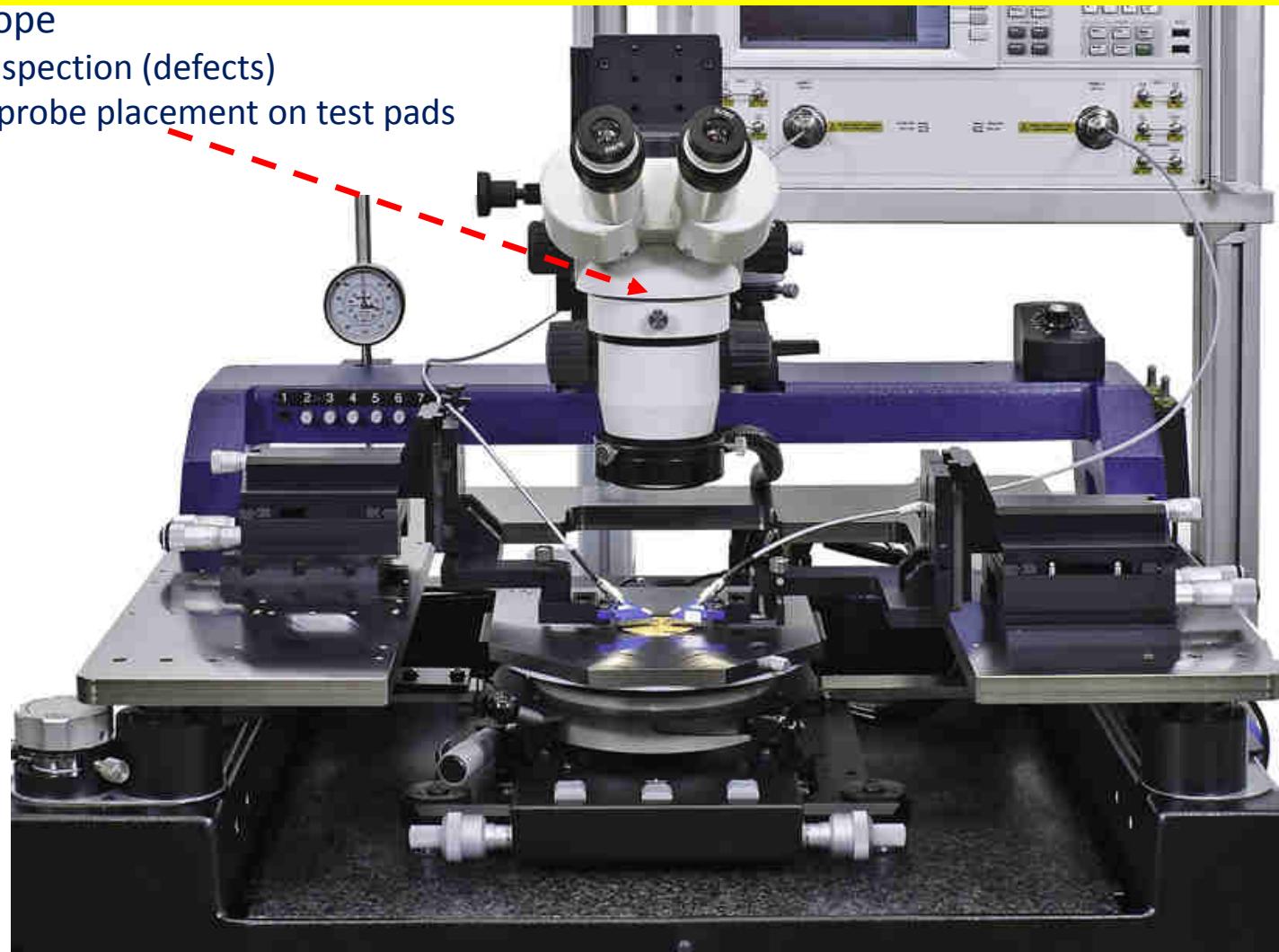
On-Wafer Probing



HF probe stations On-wafer Probing System

Microscope

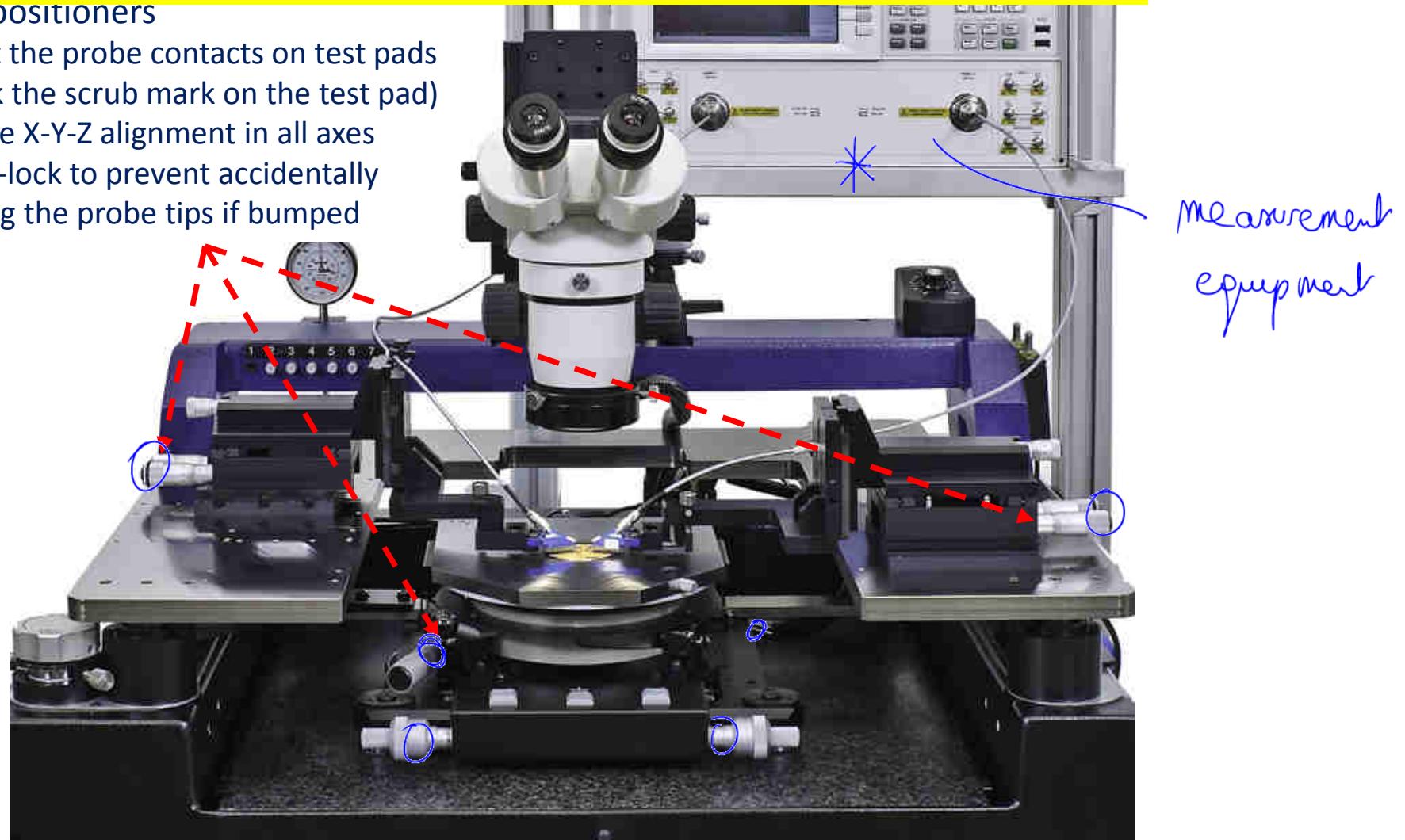
- ➊ wafer inspection (defects)
- ➋ precise probe placement on test pads



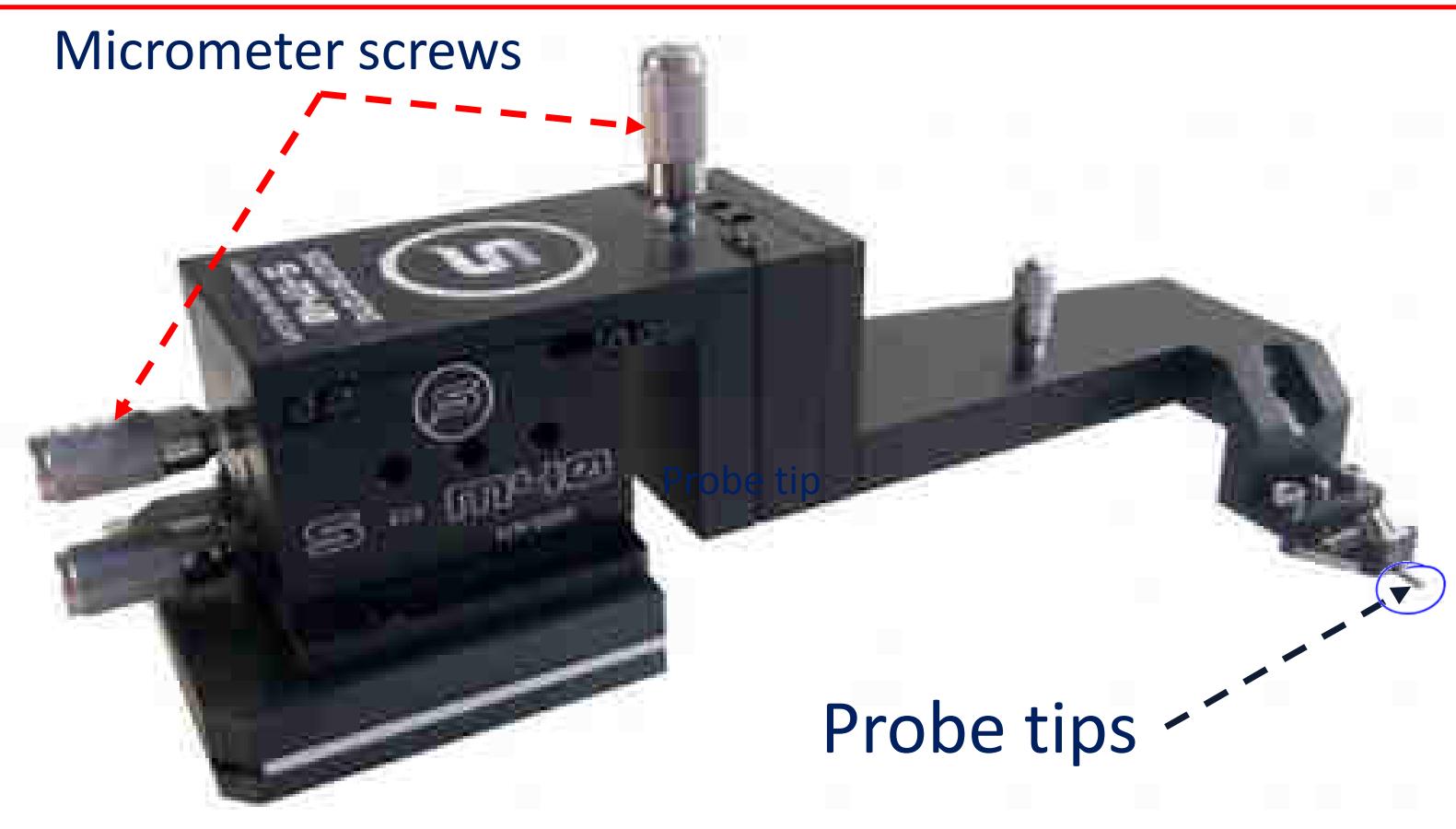
HF probe stations On-wafer Probing System

Micropositioners

- adjust the probe contacts on test pads
(check the scrub mark on the test pad)
- precise X-Y-Z alignment in all axes
- screw-lock to prevent accidentally moving the probe tips if bumped



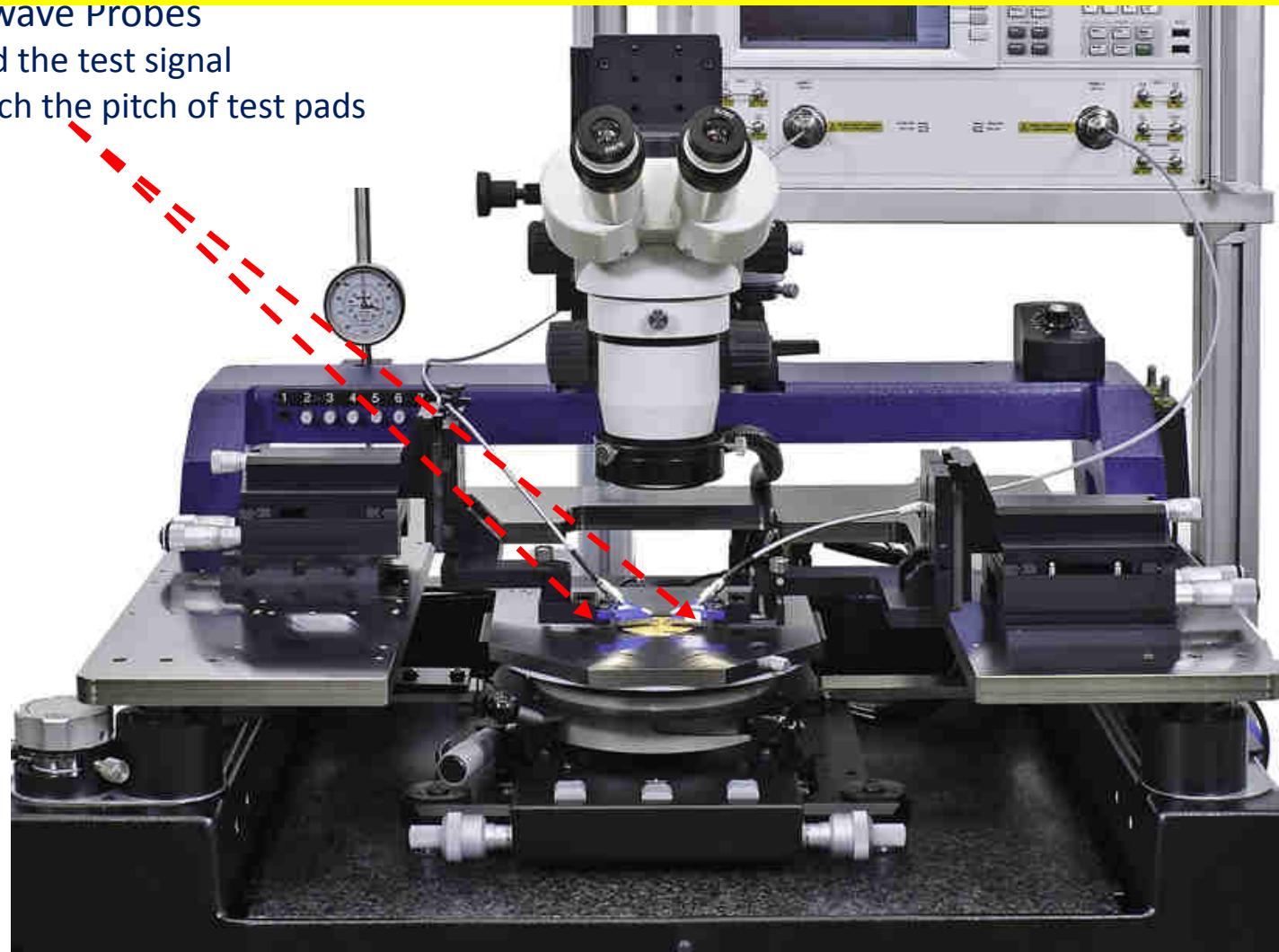
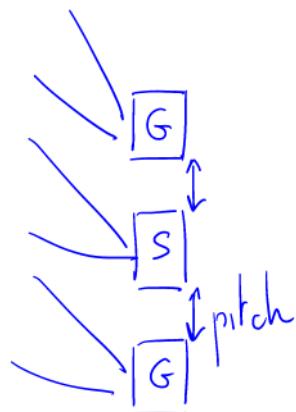
Micropositioner of probe tips



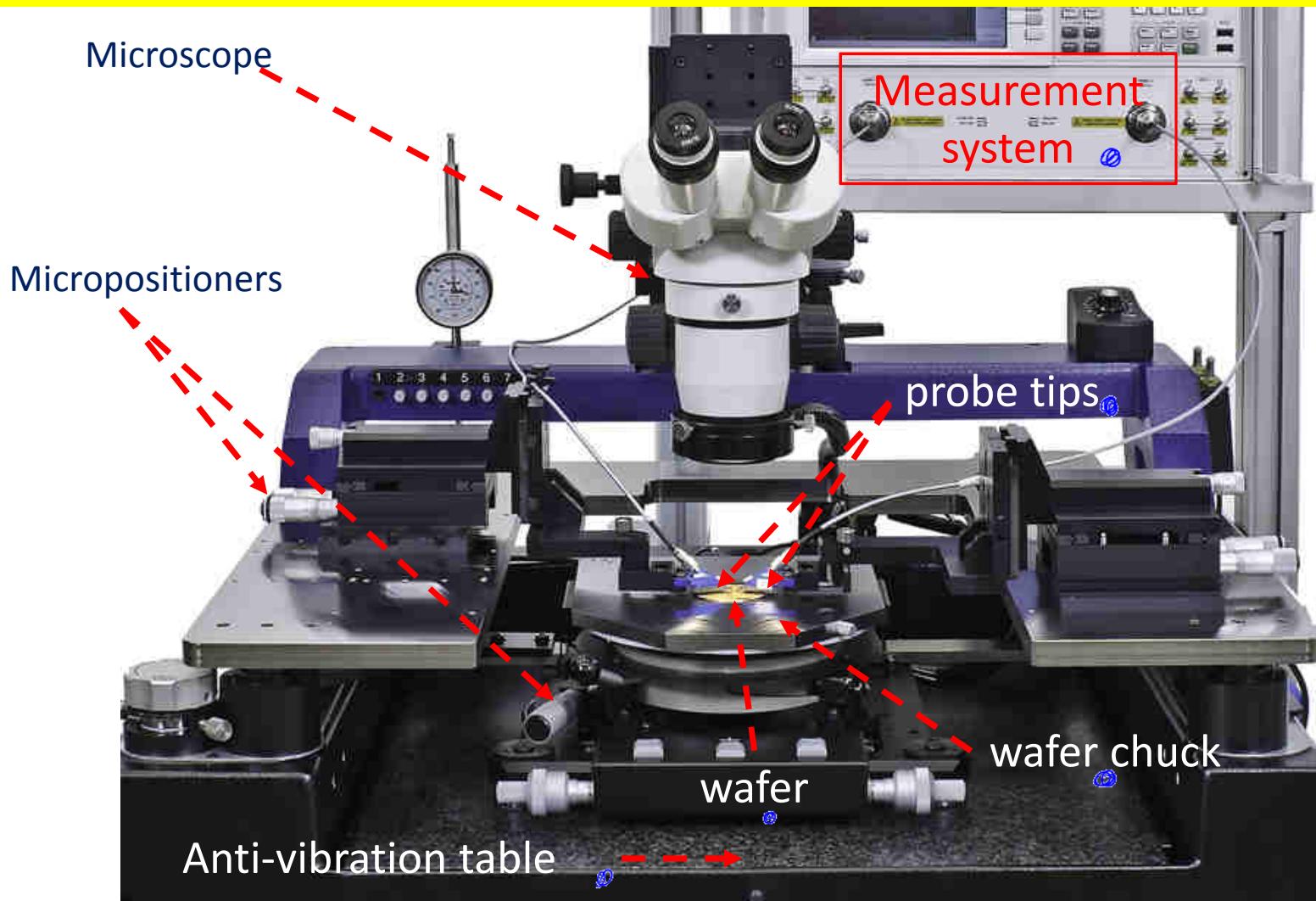
HF probe stations On-wafer Probing System

Microwave Probes

- Feed the test signal
- Match the pitch of test pads



HF probe stations On-wafer Probing System



I – Basics of MESFET operation

$\text{HEMT} \Rightarrow$ Same model topology

* Low-Frequency Bipolar transistors are based on the well-known PN Junction (P-type-SC / N-type-SC)

* High-Frequency MESFET (MEtal Semiconductor Field Effect Transistor) based on Schottky Junction (Metal / N-type-SC)

HEMT

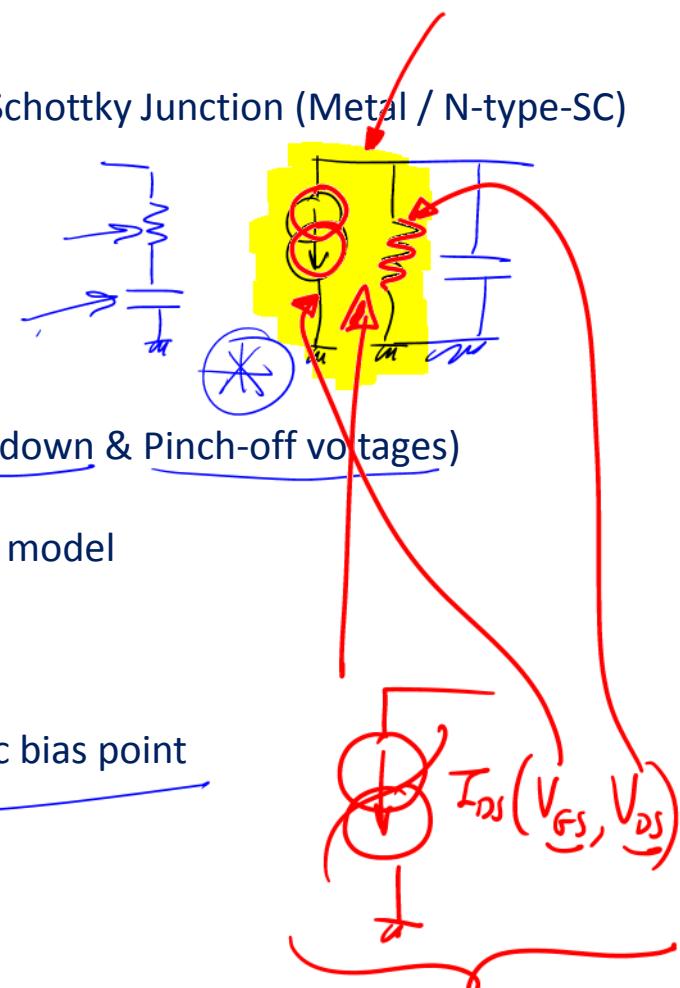
→ Simplified planar representation of FETs

→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)

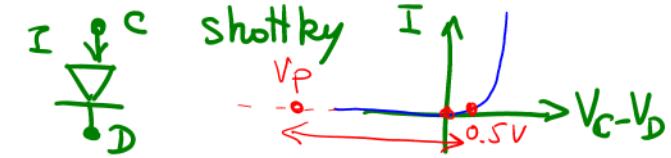
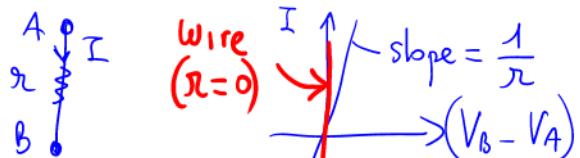
→ Localization of electrical equivalent elements that gives the nonlinear electrical model

→ Successive simplification to derive the simplified linear electrical FET model *

→ Small-signal equivalent of the nonlinear drain current (g_m , g_d) around a specific bias point



ohmic contact

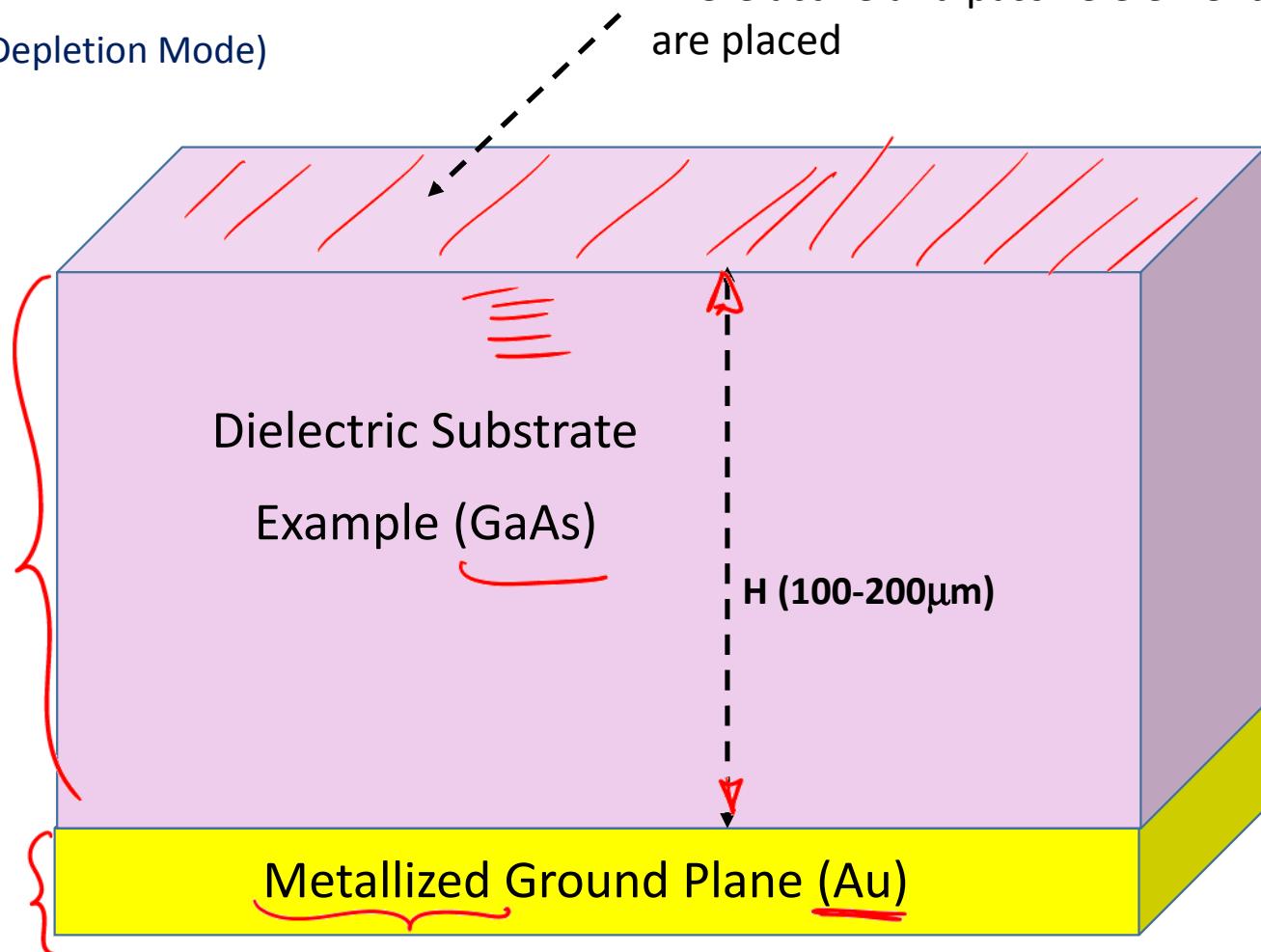
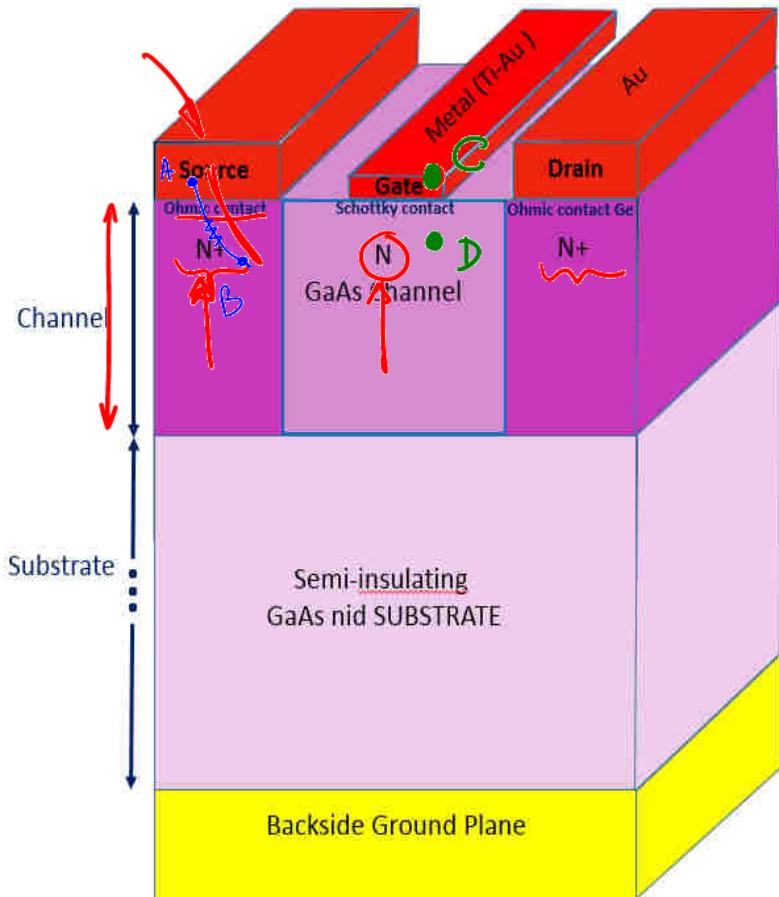


EMI MEO

E(rasmus) Mundus on Innovative Microwave Electronics and Optics

I – Basics of MESFET operation

→ Simplified planar representation of FETs (Depletion Mode)



Operating principles (FET / HEMT)

■ **FET** → Gate voltage controls the flow of drain current by modifying the available section W of the doped channel (Impurities, Ionized scattering → Low mobility)

→ Schottky Junction (Metal / SC_N channel) in reverse mode



■ **HEMT** → Gate voltage controls the flow of drain Current by modifying the carrier density n_s of a 2DEG in the undoped channel (no impurities → Very high mobility)

The (two-dimensional Electron Gas) **2DEG** is located at the **heterojunction** between a **wide bandgap semi-conductor (AlGaN)** and a **narrow bandgap semi-conductor (GaN)**.

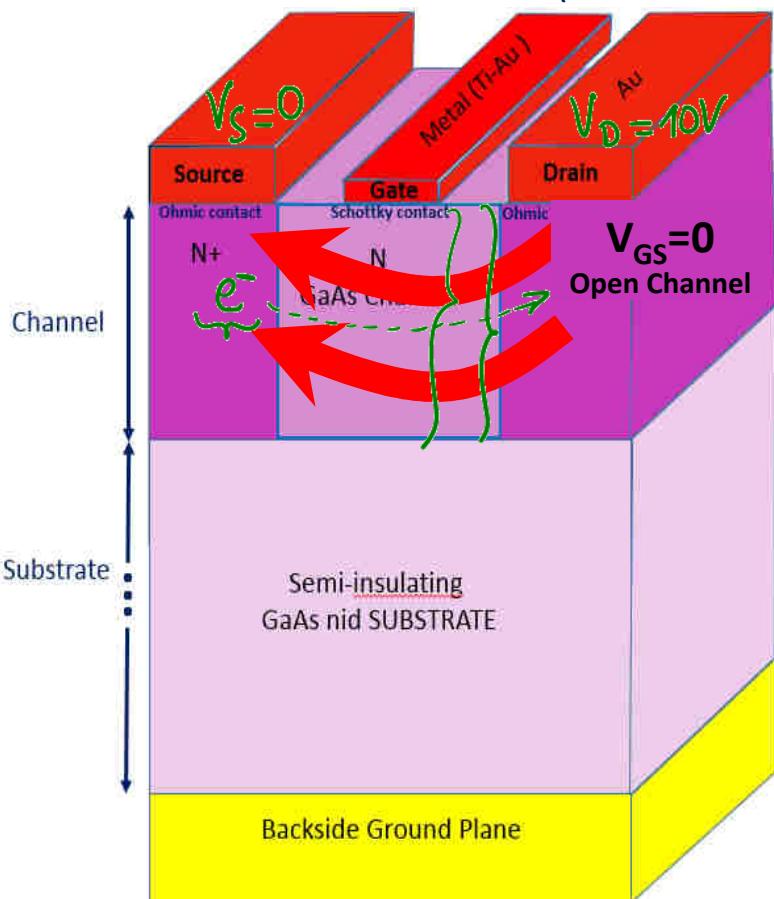
The electrons of the 2 DEG are free to move in a two-dimensional plane (x,z)
but tightly confined in the 3rd dimension (y)

because they are trapped in a potential well created at the heterojunction surface

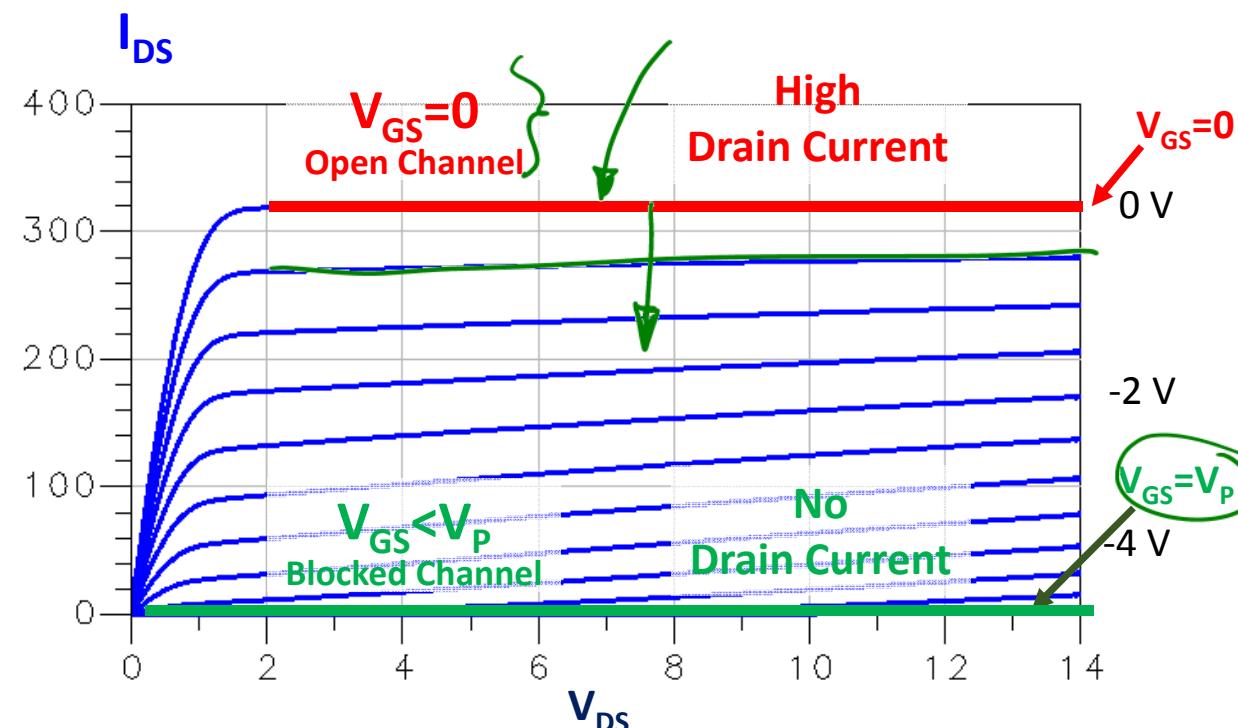
→ heterostructure (Wide bandgap SC / Narrow bandgap SC) 

I – Basics of MESFET operation

→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)



FET → Gate voltage controls the flow of drain current by modifying the available section W of the doped channel (Impurities, Ionized scattering → Low mobility)



Operating principles (FET / HEMT)

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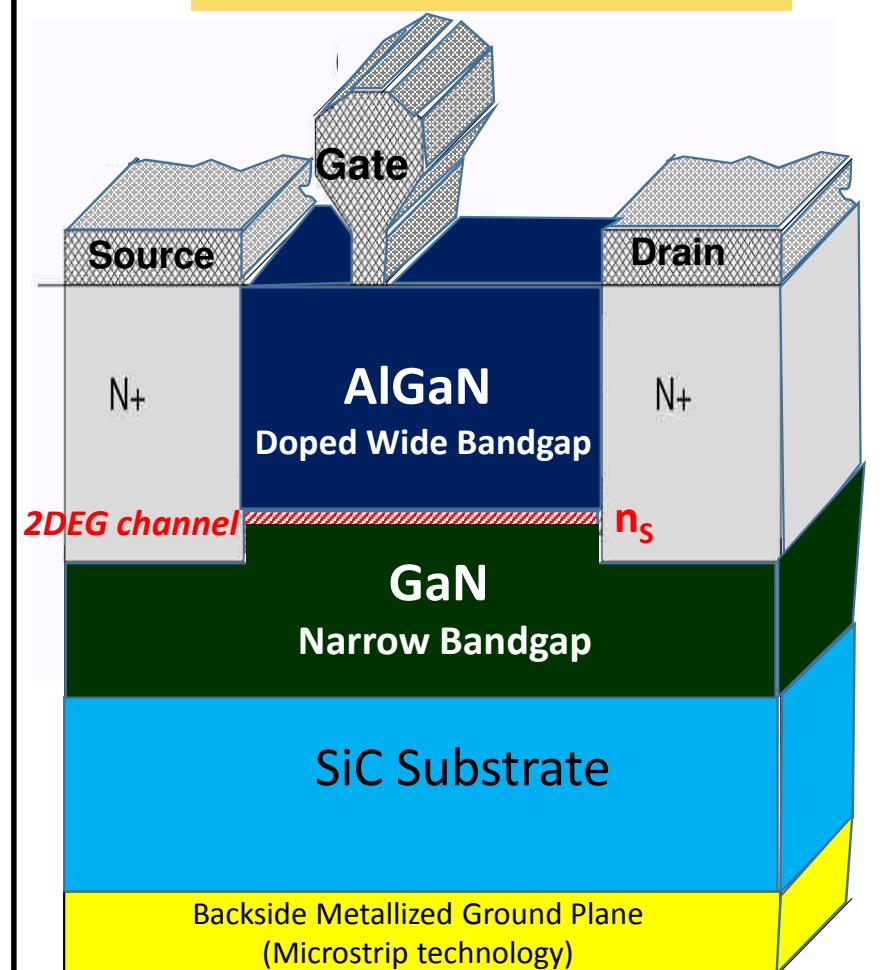
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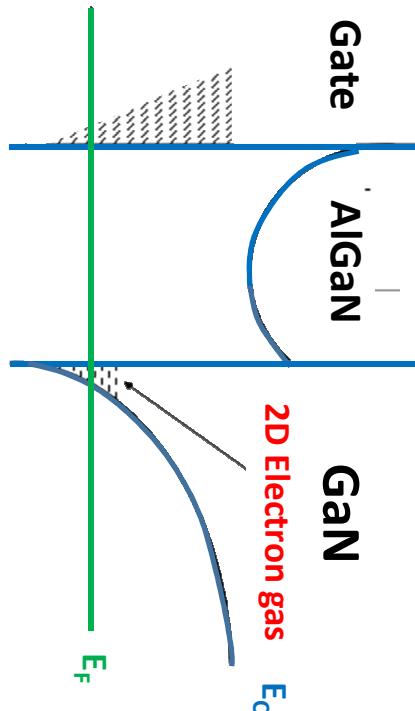
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I – Basics of HEMT operation → Same Electrical Circuit Model than FET

AlGaN/GaN HEMT on SiC



HEMT → Gate voltage controls the flow of drain current by modifying the carrier density n_s of a 2DEG in the undoped channel (no impurities → Very high mobility)

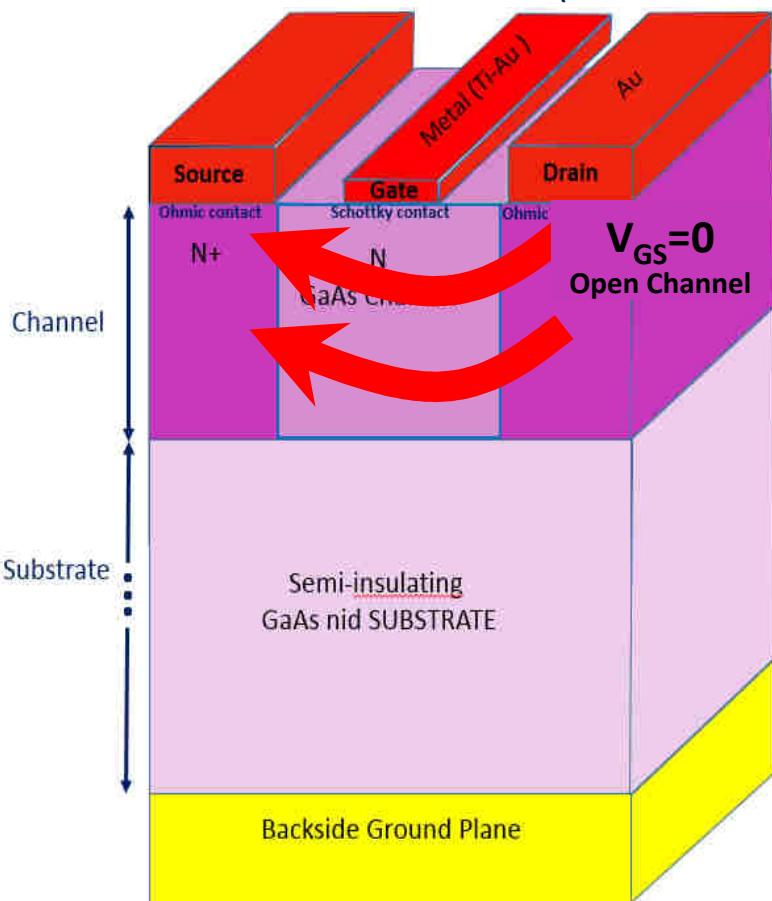


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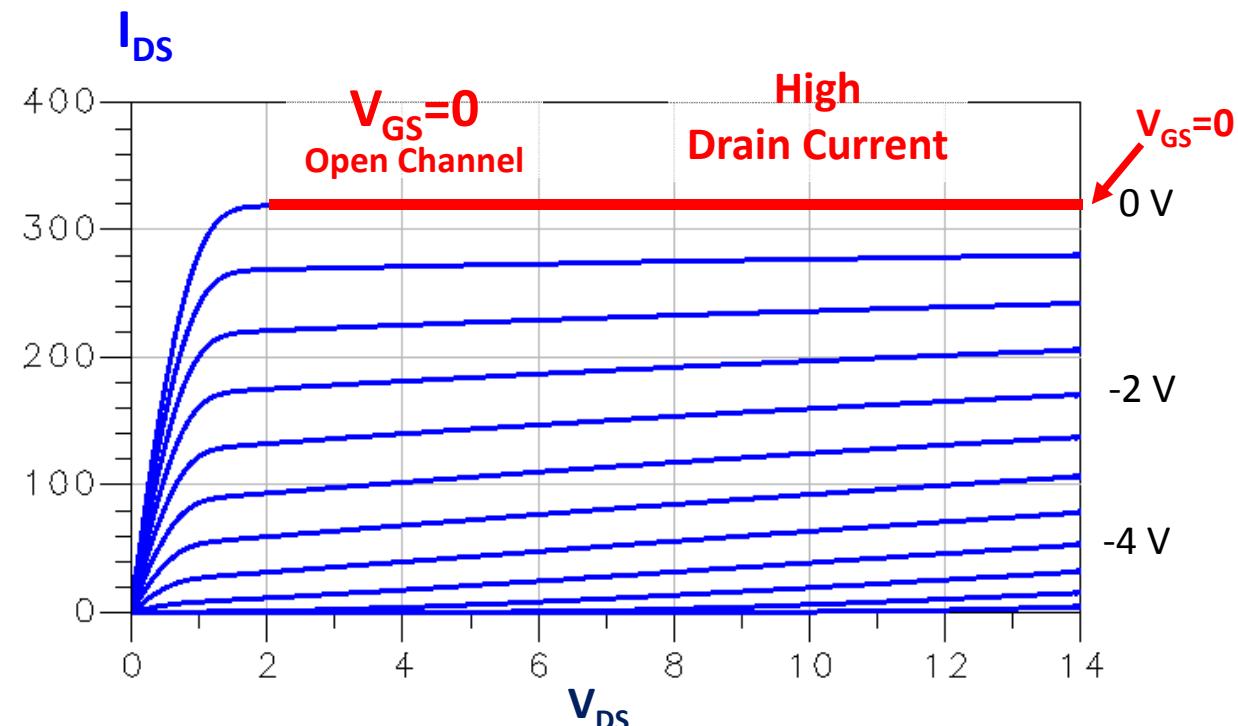
The electrons of the 2 DEG are free to move in a two-dimensional plane (x,z) but tightly confined in the 3rd dimension (y) because they are trapped in a potential well created at the heterojunction surface

I – Basics of MESFET operation

→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)

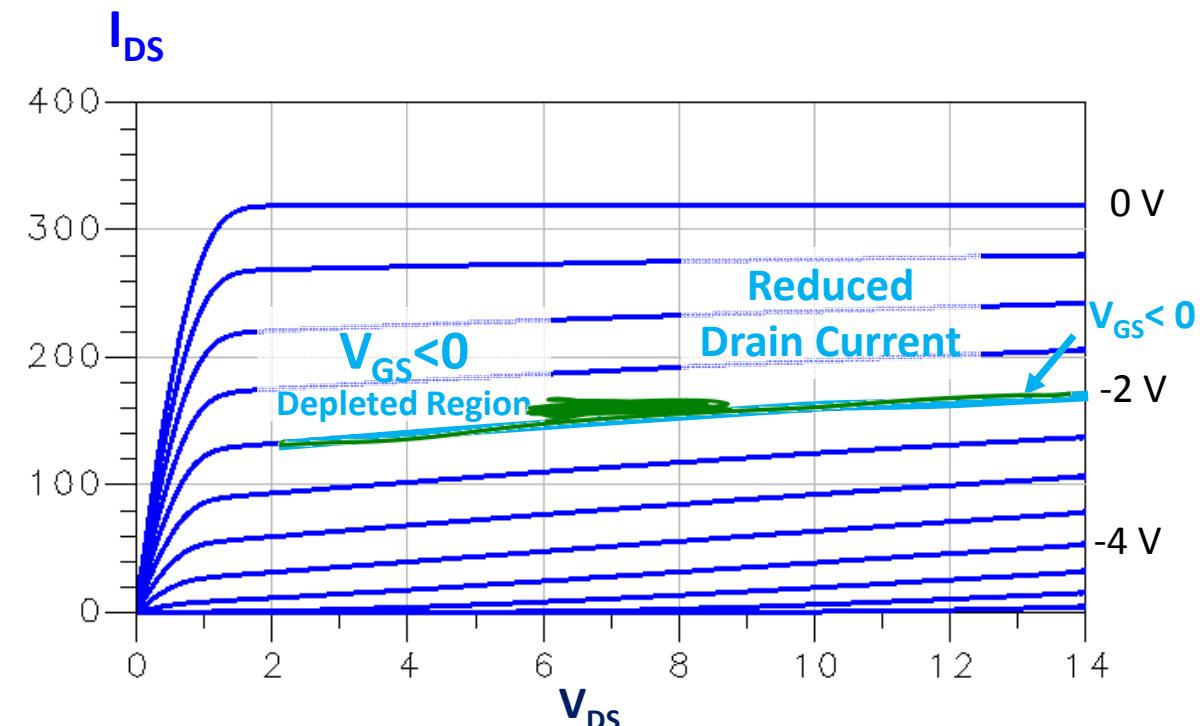
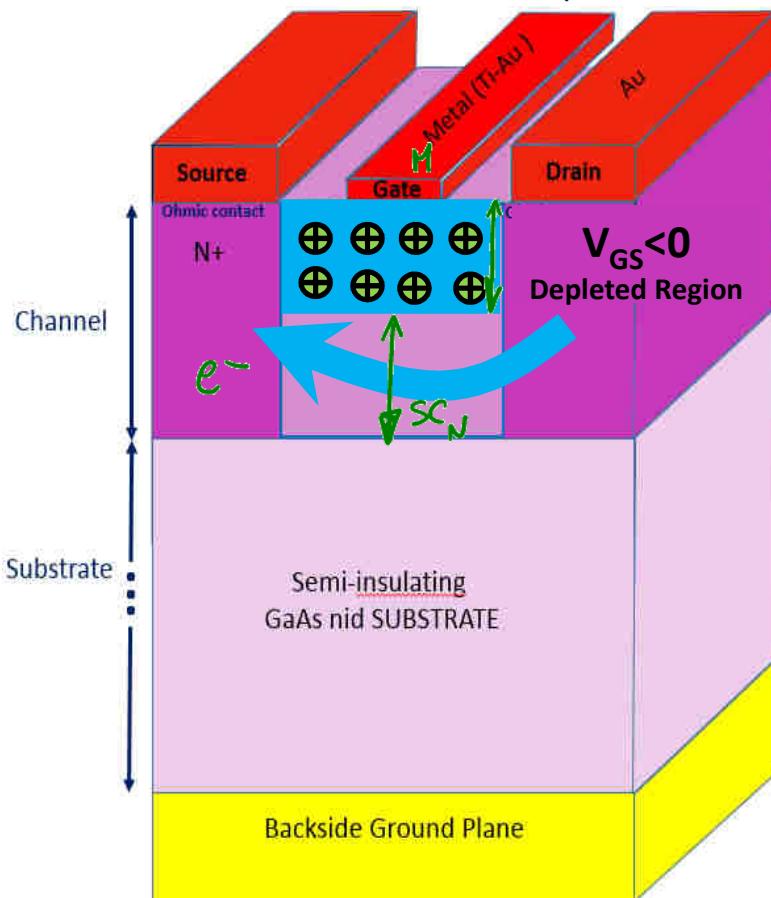


FET → Gate voltage controls the flow of drain current by modifying the available section W of the doped channel
(Impurities, Ionized scattering → Low mobility)



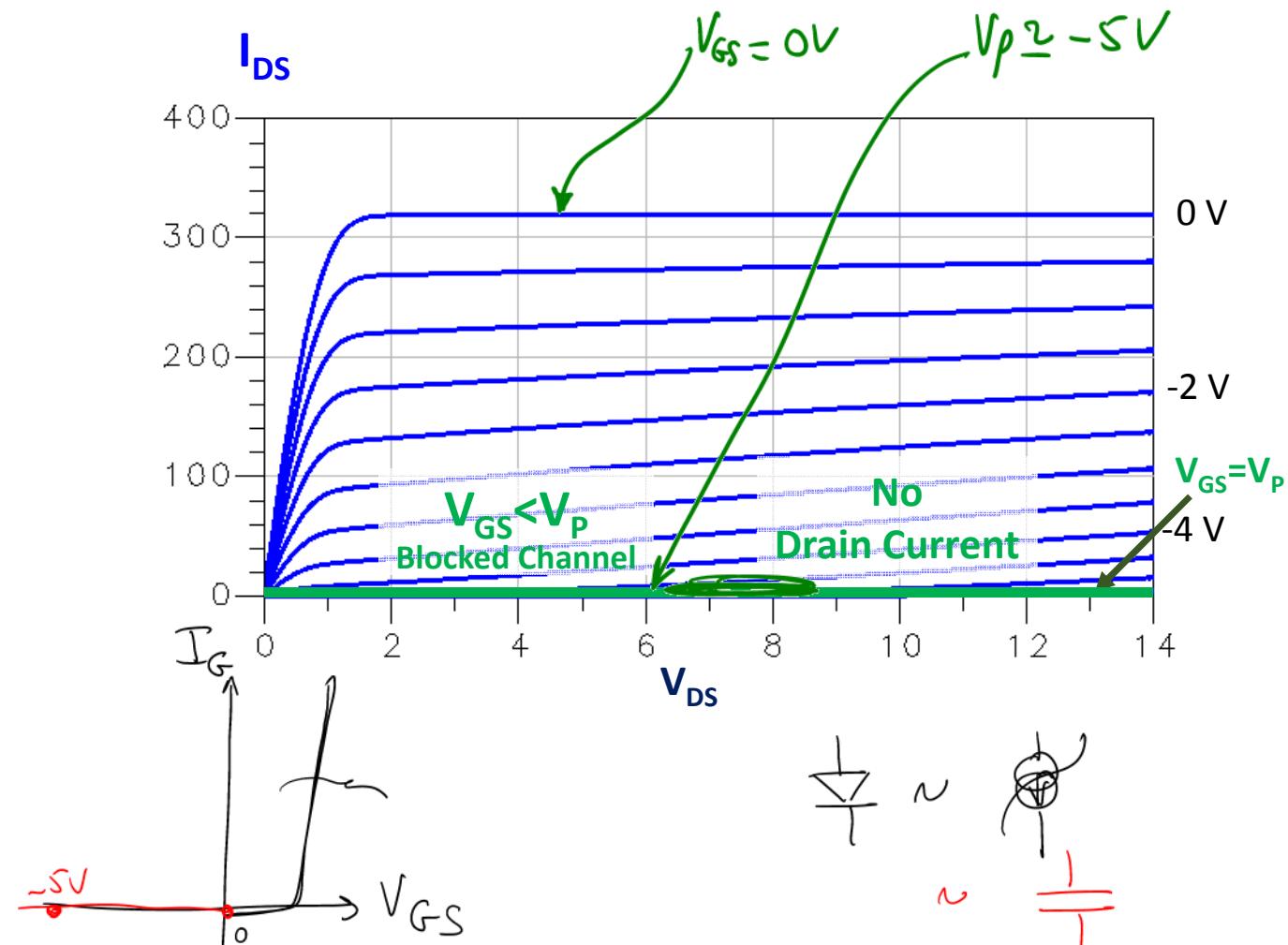
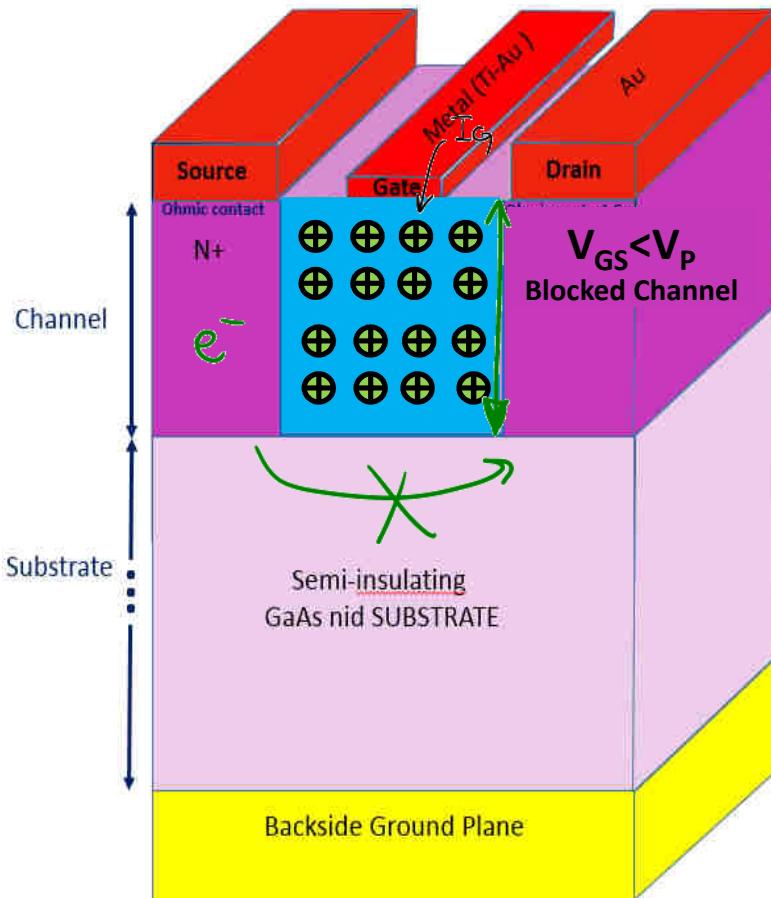
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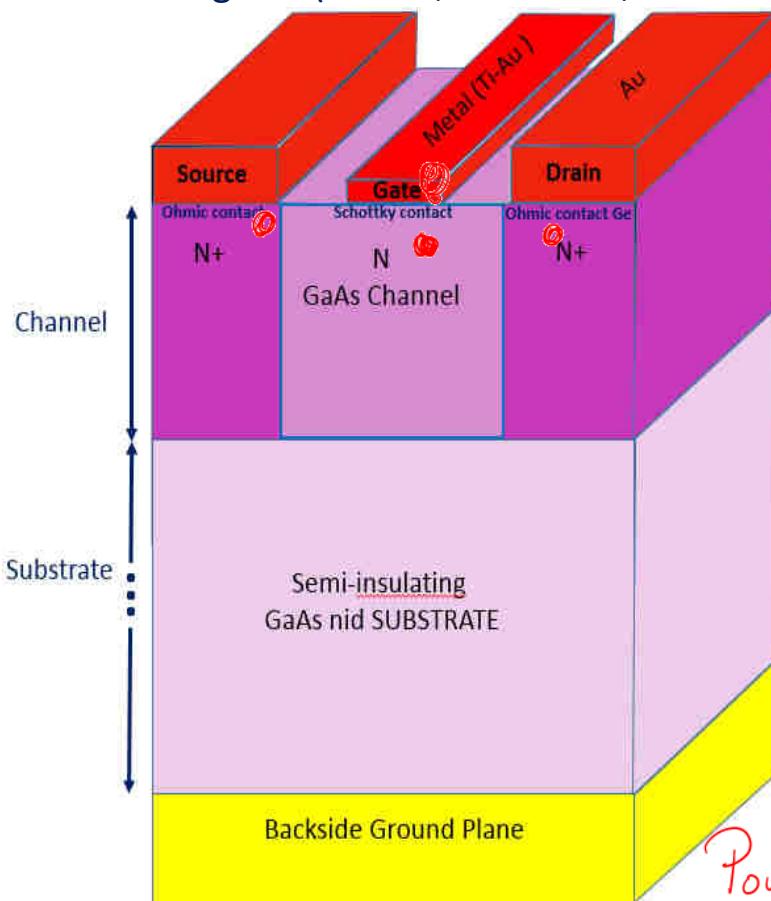
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→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)

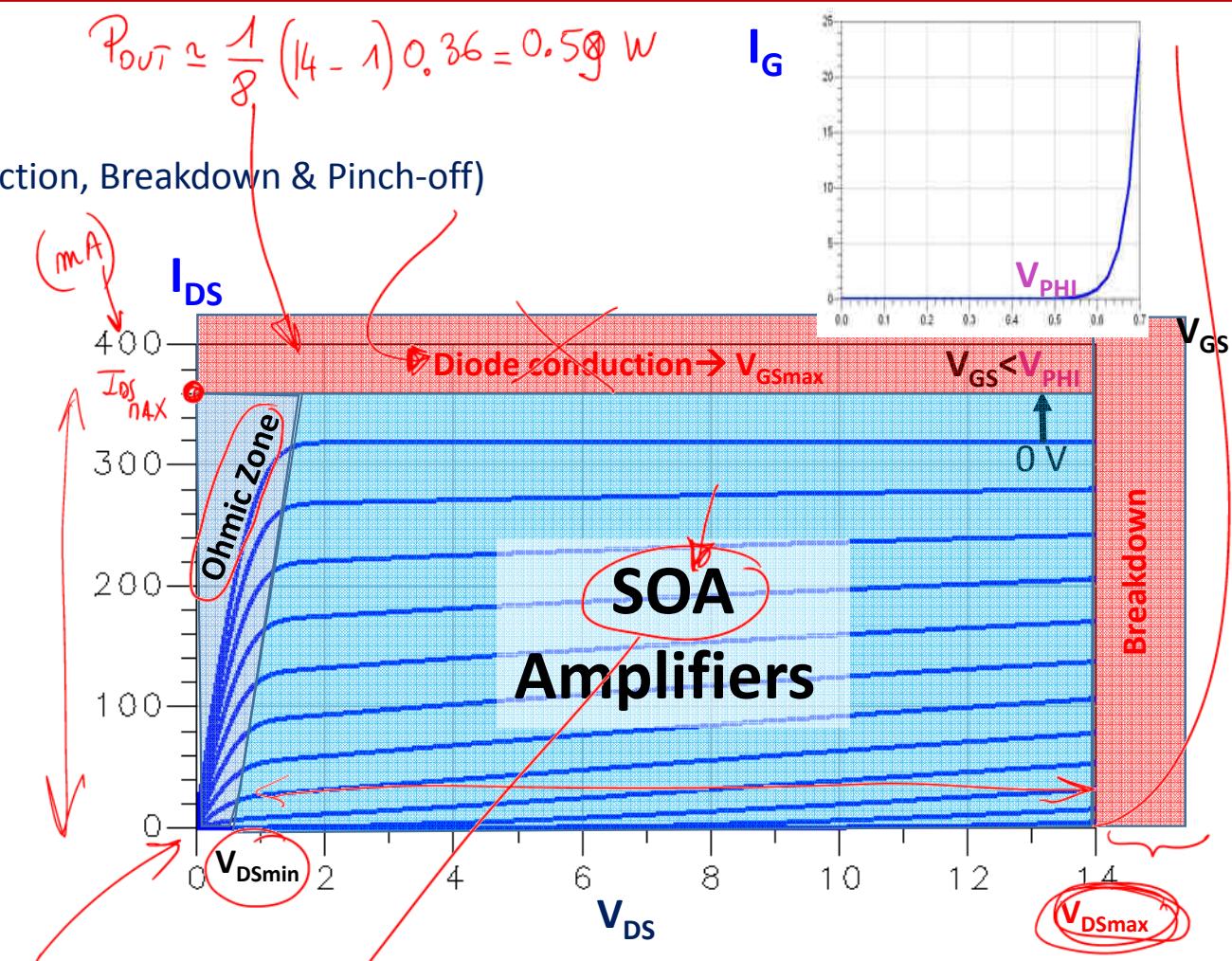


I – Basics of MESFET operation

→ I-V regions (Ohmic, Saturated, Diode conduction, Breakdown & Pinch-off)



$$\approx \frac{1}{2} \times \frac{V_{DSMAX} - V_{DSMIN}}{2} \times \frac{I_{DSMAX}}{2}$$

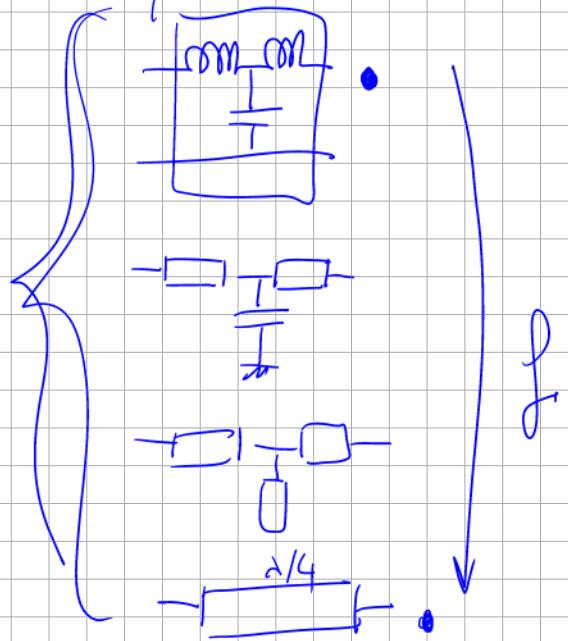
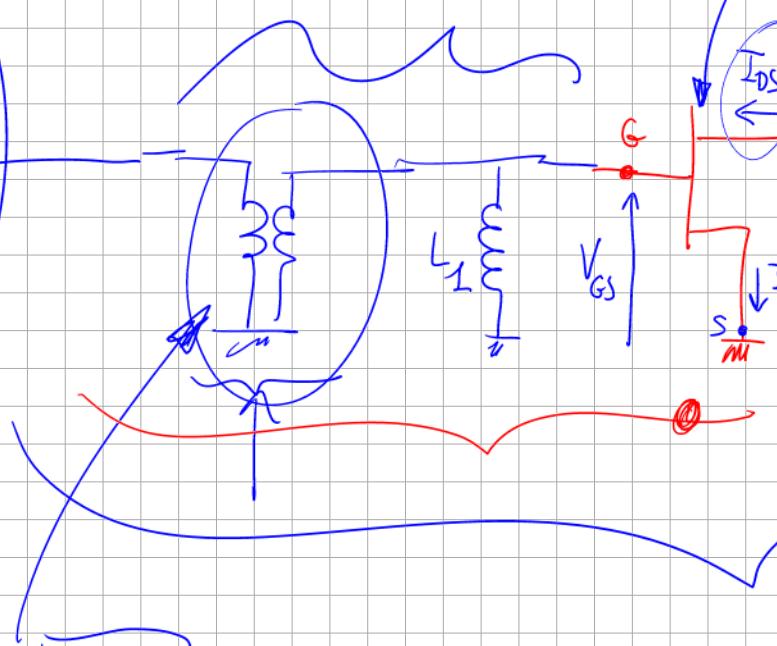


Safe Operating Area

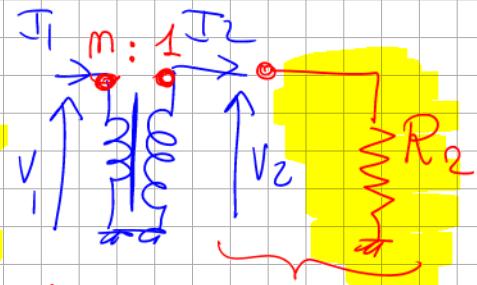
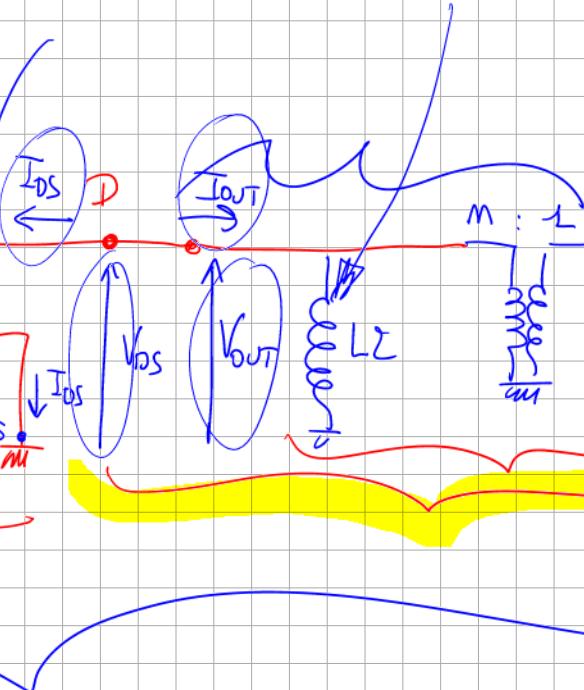
FET → $V_{DSMAX} \approx 80 V$
 HEMT → $V_{DSMAX} \approx 100 V$



IMC
Input Matching Circuit



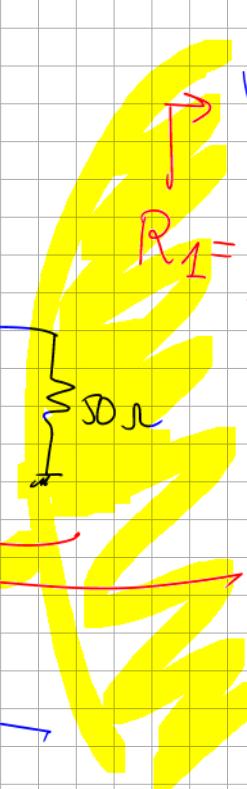
OMC



$$R_1 = \frac{V_1}{I_1}$$

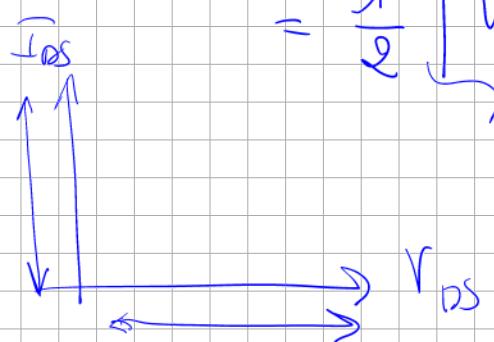
$$M = \frac{M_2}{M_1}$$

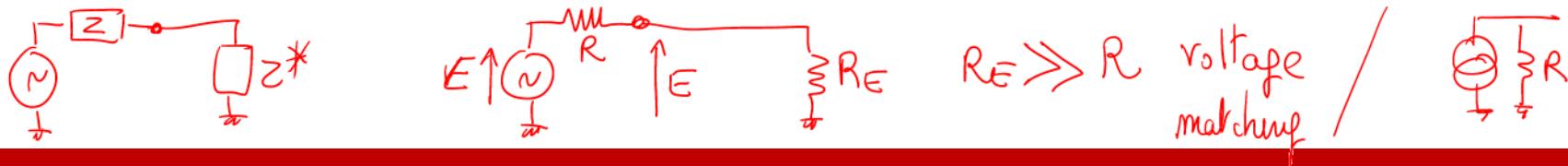
$$M = \sqrt{\frac{R_2}{R_1}}$$



$$P_{\text{out}} = \frac{1}{2} \rho_e (V_{\text{out}} \times I_{\text{out}}^*)$$

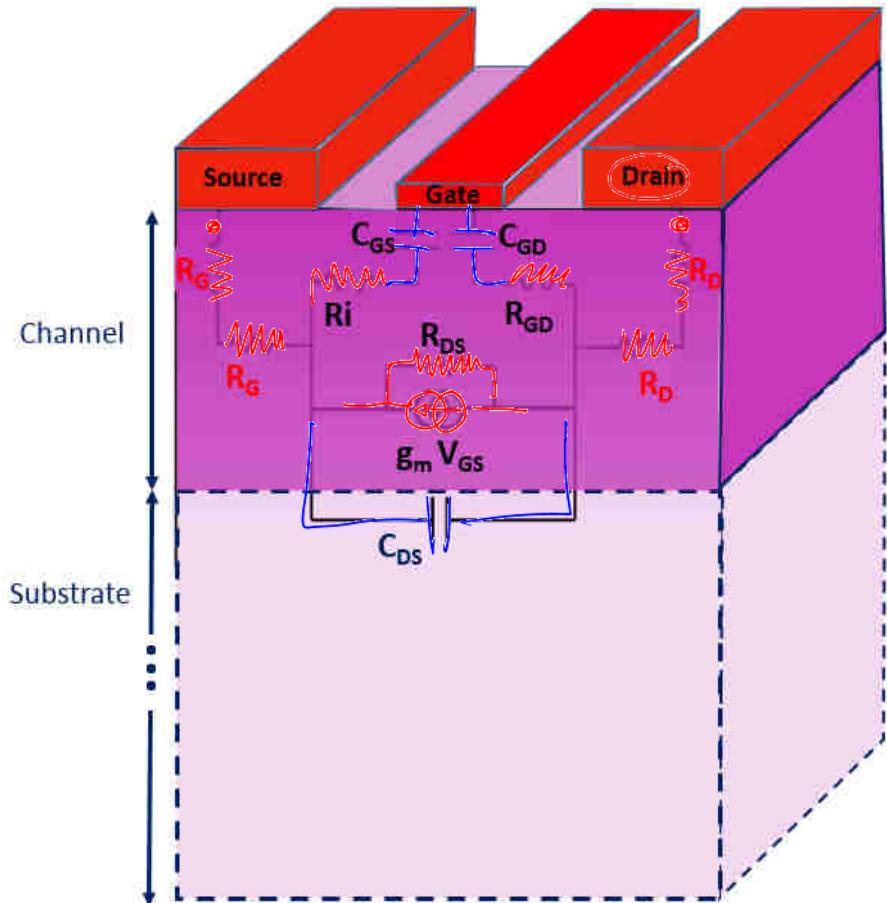
$$= \frac{1}{2} |V_{\text{out}}| |I_{\text{out}}| \cos(\phi_{V_{\text{out}}} - \phi_{I_{\text{out}}})$$





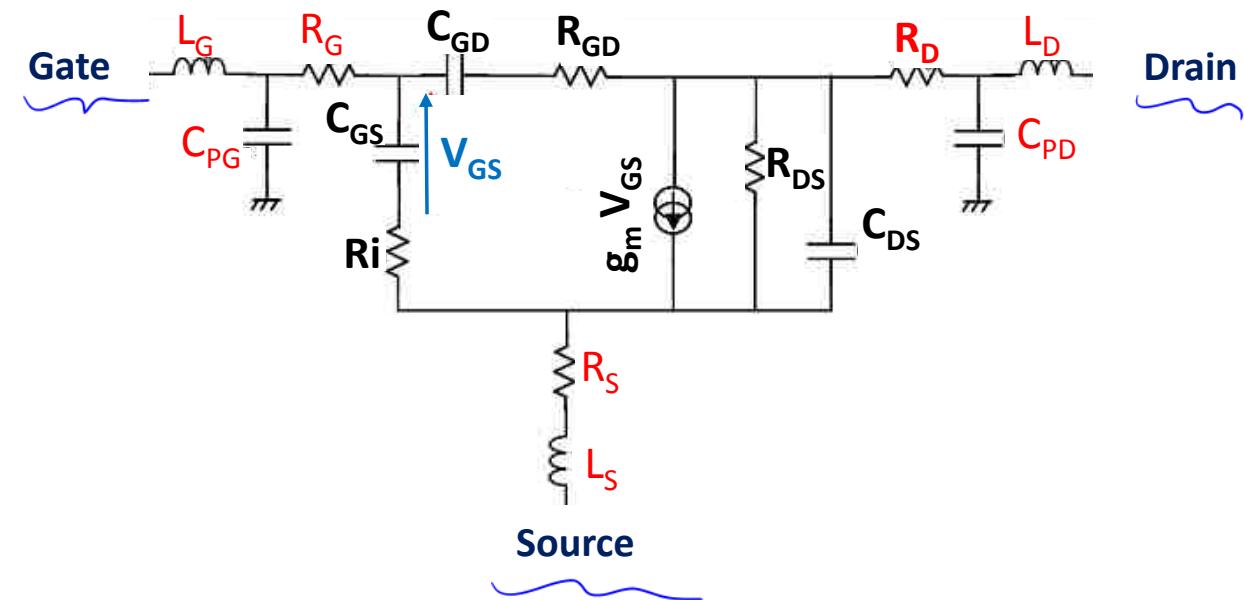
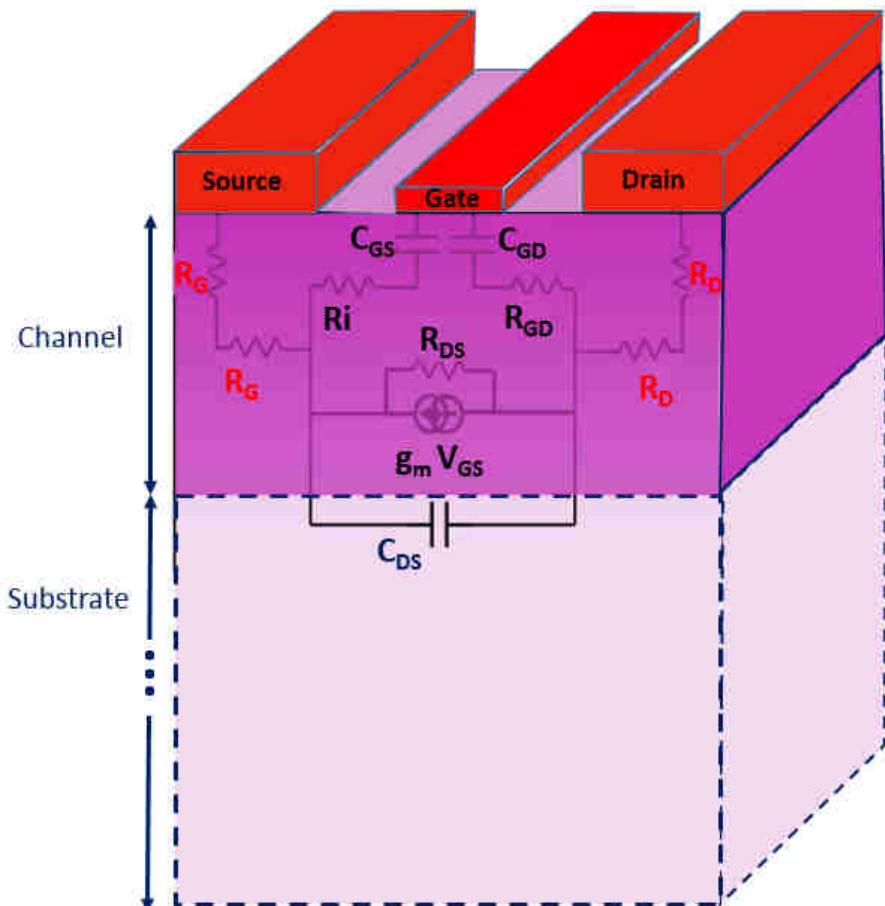
I – Basics of MESFET operation

→ Simplified planar representation of FETs (localization of electrical lumped elements)



I – Basics of MESFET operation

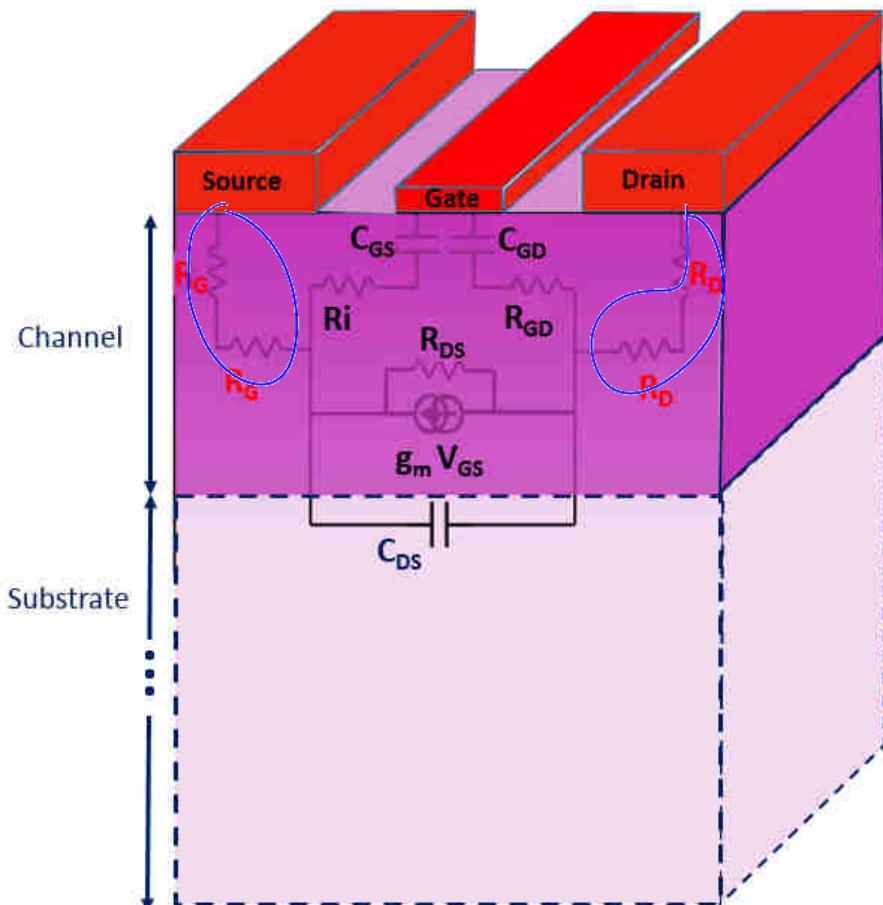
→ Simplified planar representation of FETs (localization of electrical lumped elements)



$$G = \underline{14 \text{ dB}} \quad \begin{matrix} 15 \\ 13 \end{matrix}$$

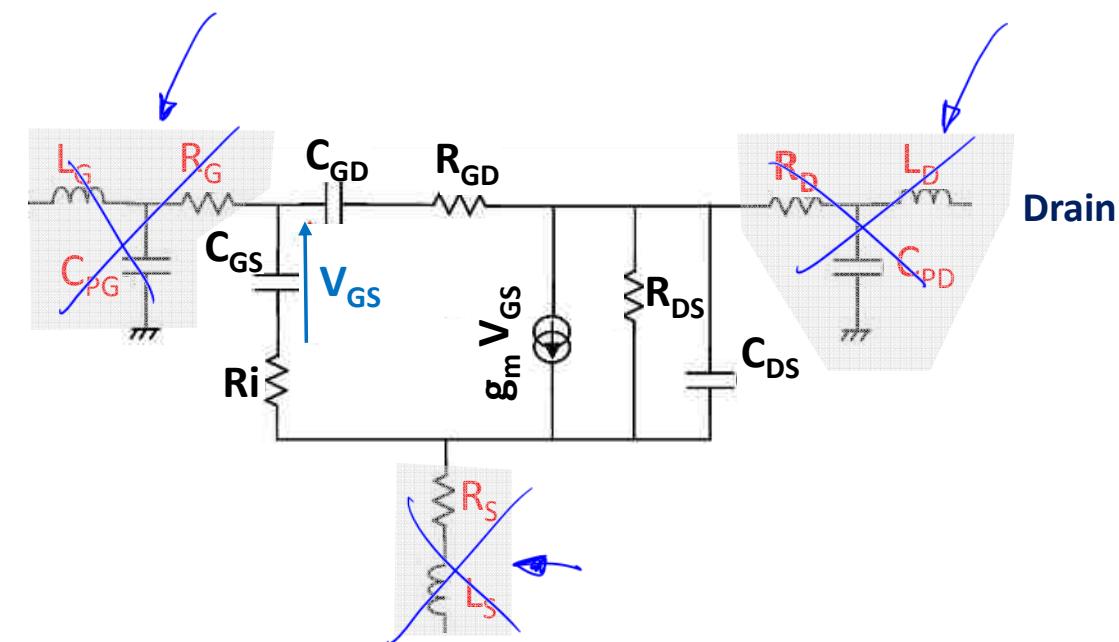
I – Basics of MESFET operation

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Gate

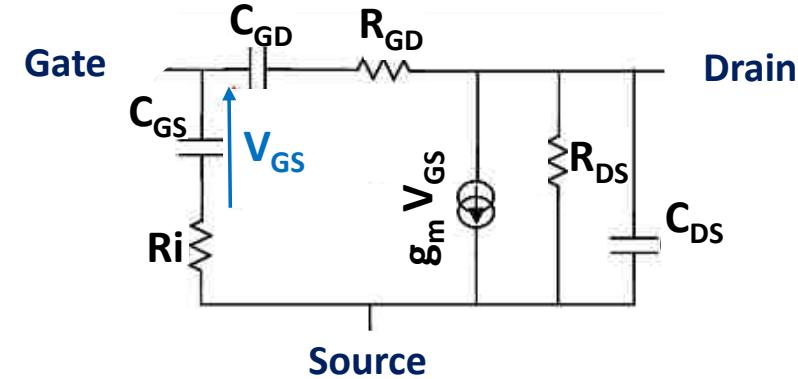
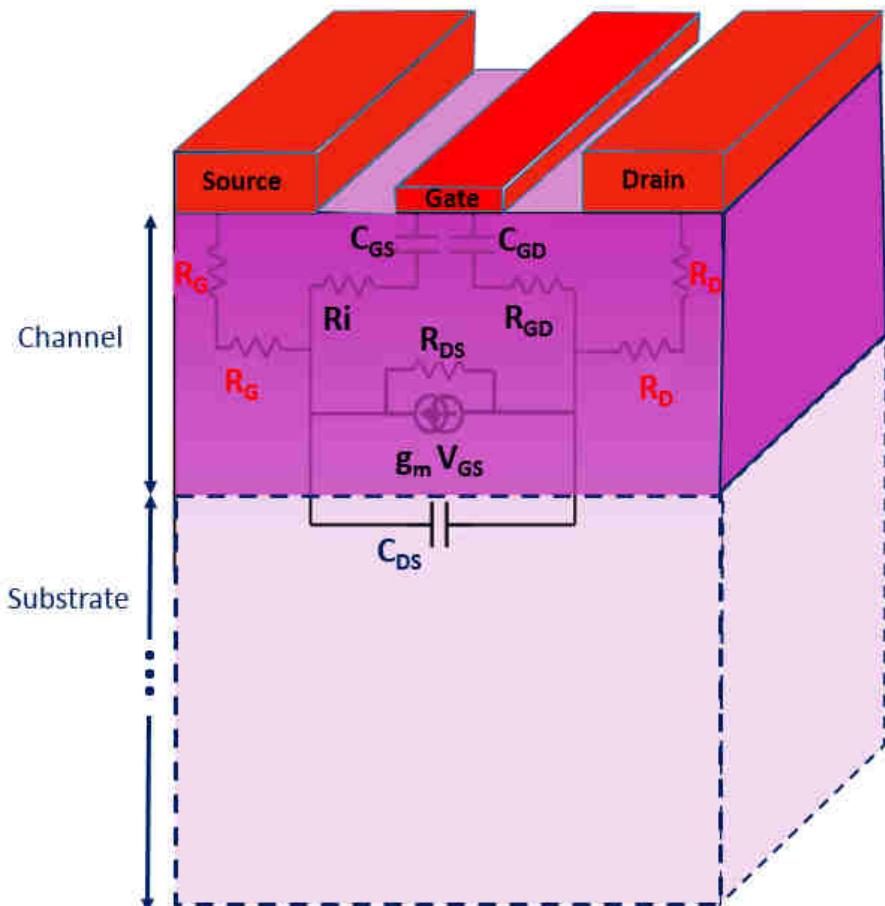
Source



Extrinsic elements are the first ones that can be neglected when compared to other elements

I – Basics of MESFET operation

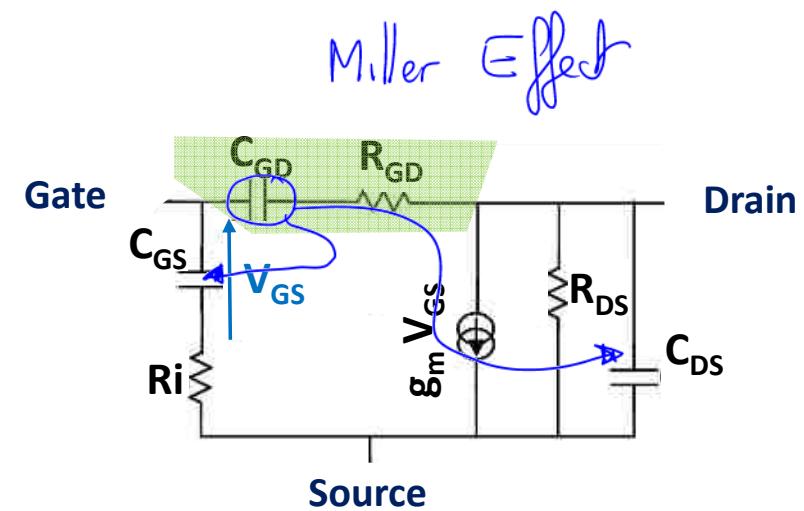
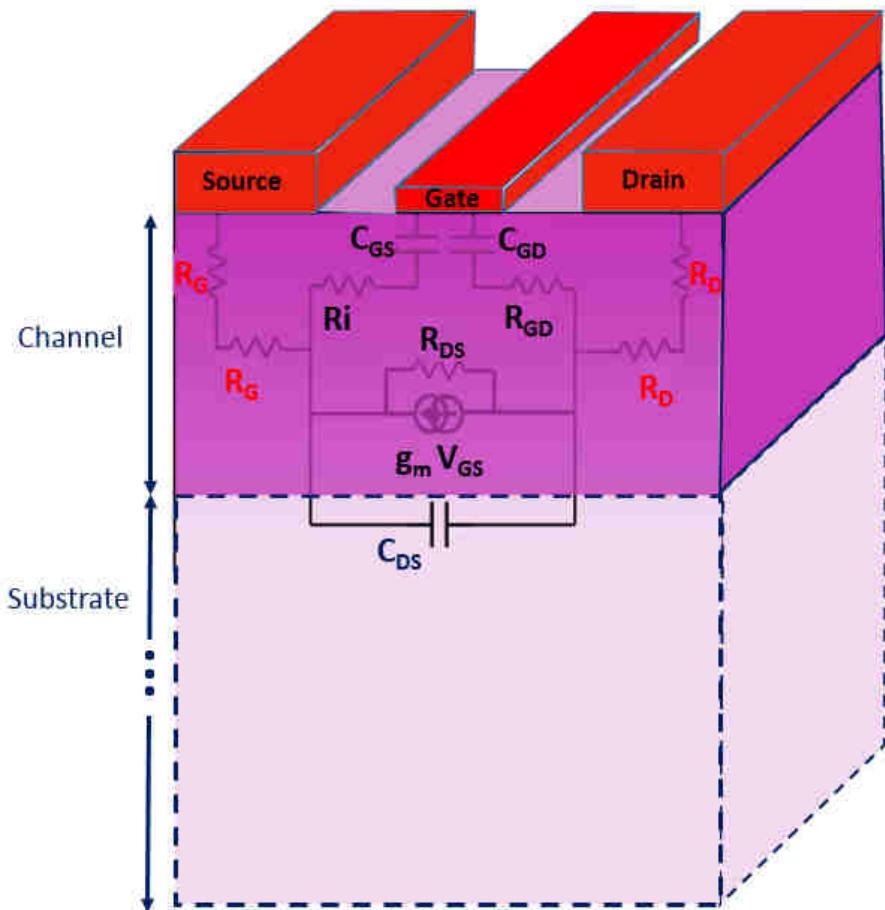
→ Simplified planar representation of FETs (localization of electrical lumped elements)



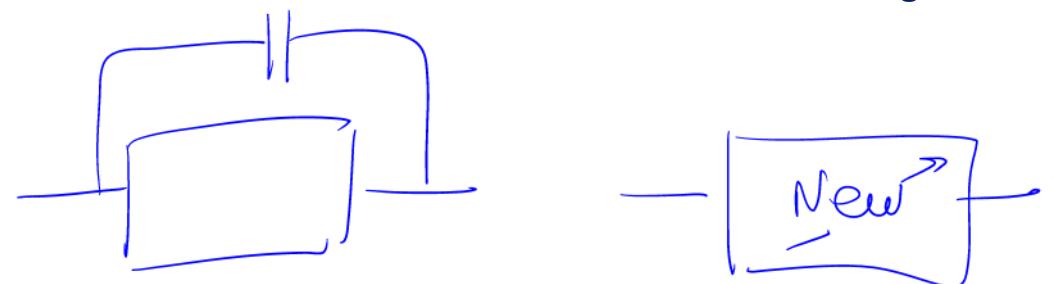
Extrinsic elements are the first ones that can be neglected when compared to other elements

I – Basics of MESFET operation

→ Simplified planar representation of FETs (localization of electrical lumped elements)

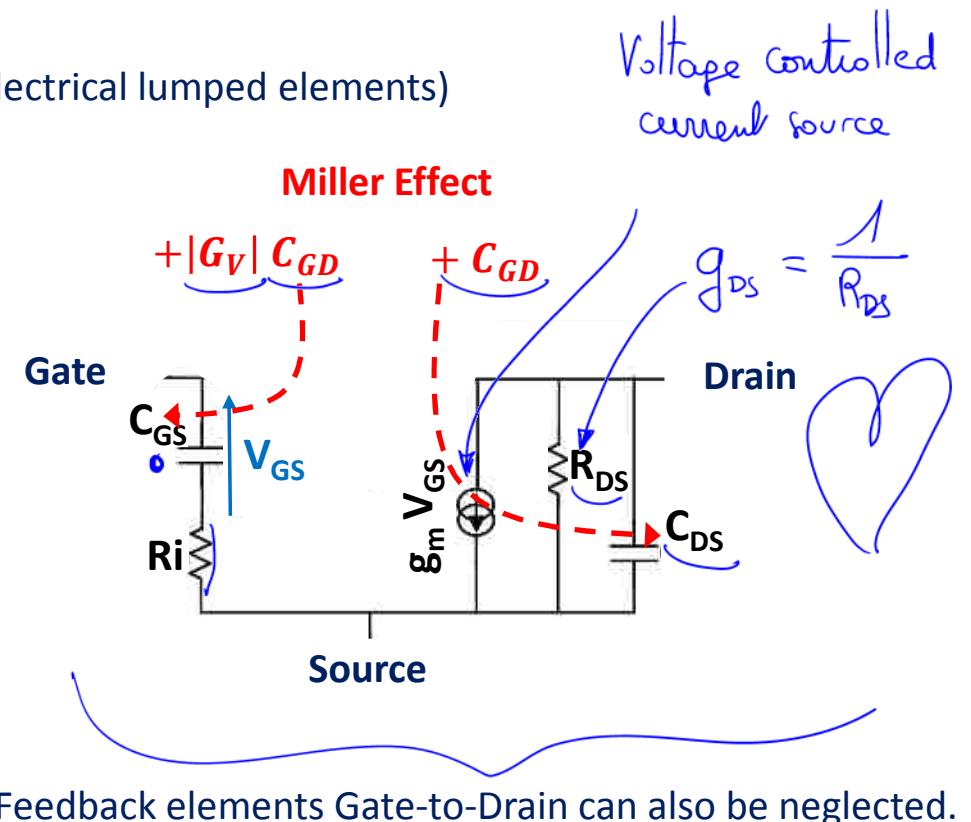
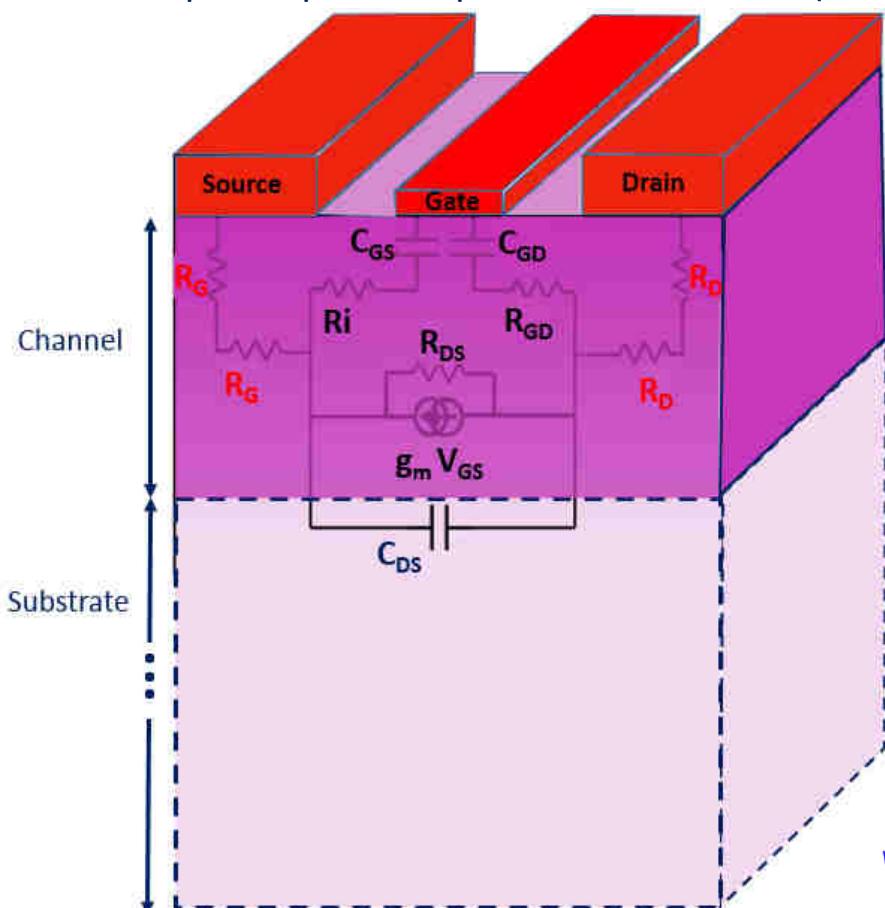


Feedback elements Gate-to-Drain can also be neglected.



I – Basics of MESFET operation

→ Simplified planar representation of FETs (localization of electrical lumped elements)

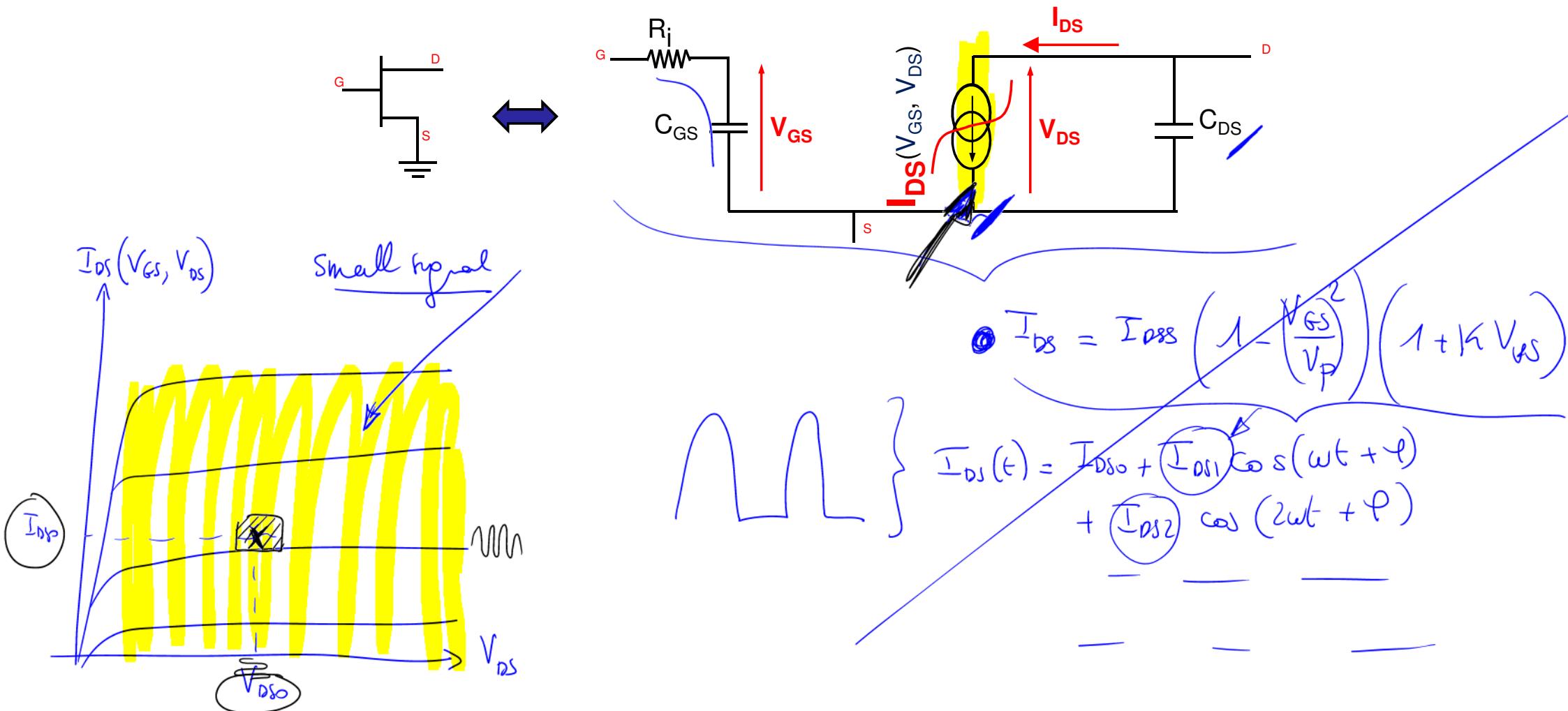


Feedback elements Gate-to-Drain can also be neglected.
However, the capacitive feedback is taken into account
by **Miller Effect**

$$I = GV \quad \text{with } G = 1/R$$

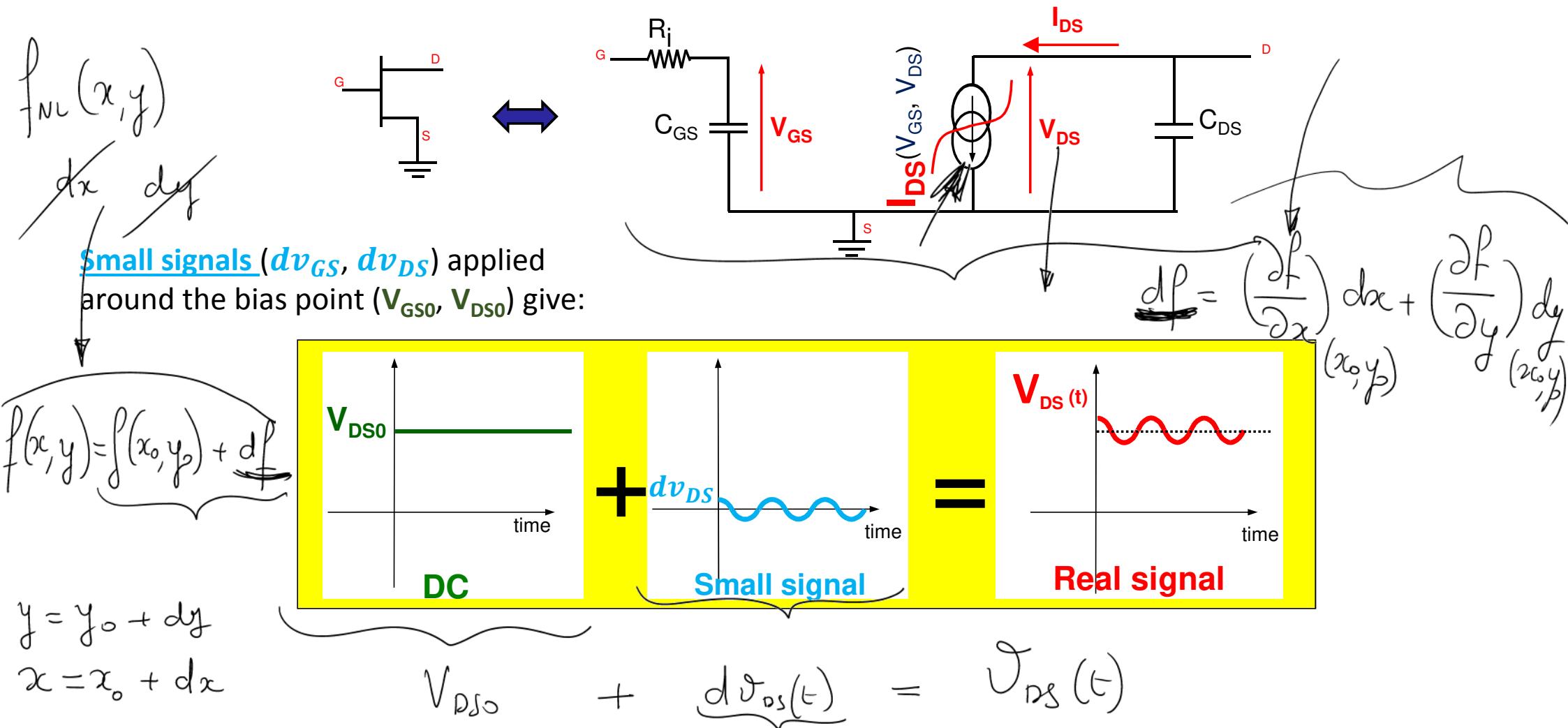
I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm , gd) around a specific bias point



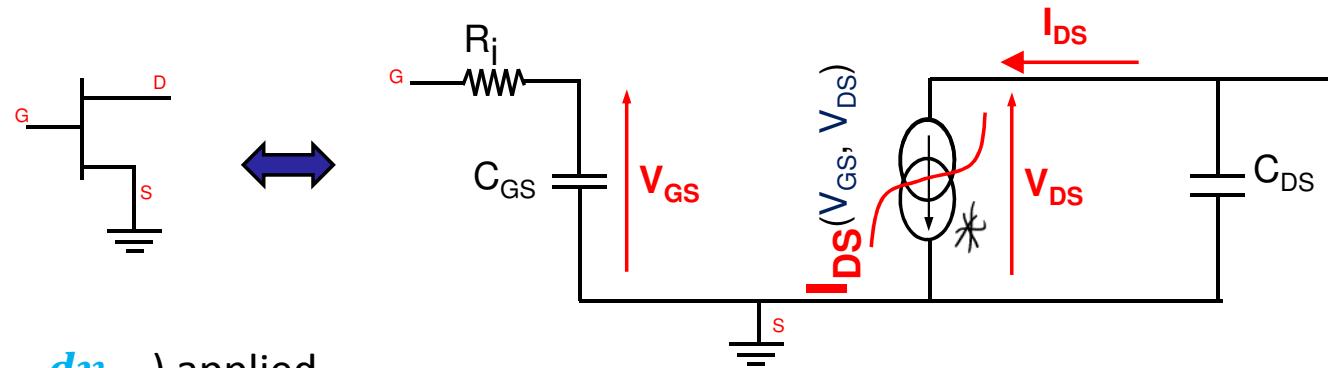
I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm , gd) around a specific bias point



I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm , gd) around a specific bias point

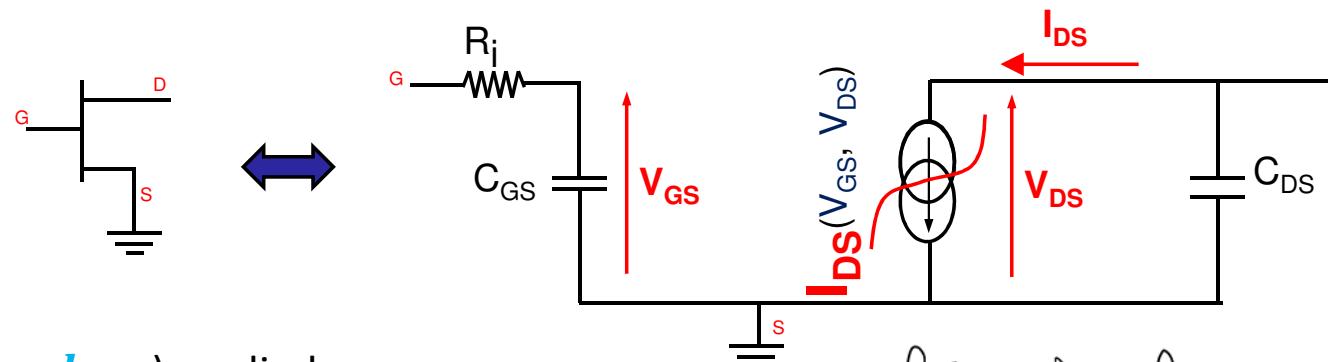


Small signals (dV_{GS} , dV_{DS}) applied
around the bias point (V_{GS0} , V_{DS0}) give:

$$\begin{cases} \widetilde{V_{GS}(t)} = \widetilde{V_{GS0}} + \widetilde{dV_{GS}(t)} \\ \widetilde{V_{DS}(t)} = \widetilde{V_{DS0}} + \widetilde{dV_{DS}(t)} \end{cases}$$

I – Basics of FET operation

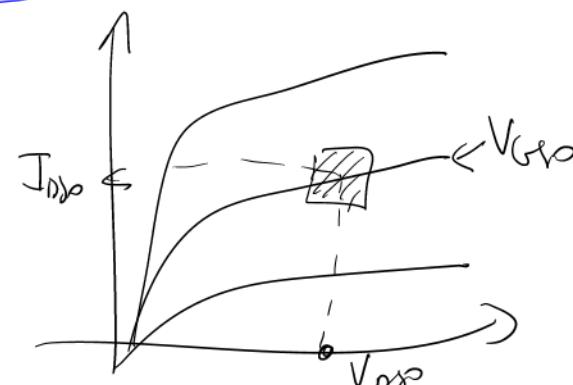
→ Simplified Small-signal equivalent of the nonlinear drain current (gm , gd) around a specific bias point



Small signals (dv_{GS} , dv_{DS}) applied around the bias point (V_{GS0} , V_{DS0}) give:

$$f(x, y) = f(x_0, y_0) + \frac{\partial f}{\partial x}(x_0, y_0)(x - x_0) + \frac{\partial f}{\partial y}(x_0, y_0)(y - y_0)$$

$$\begin{aligned} V_{GS}(t) &= V_{GS0} + \underbrace{dv_{GS}(t)}_{*} \\ V_{DS}(t) &= V_{DS0} + \underbrace{dv_{DS}(t)}_{*} \end{aligned} \quad \rightarrow \quad \begin{aligned} \overbrace{I_{DS}(t)} &= \overbrace{F_{NL}(V_{GS}, V_{DS})} = \overbrace{F_{NL}(V_{GS0}, V_{DS0})} + \underbrace{dF_{NL}}_{=} \\ &= \overbrace{I_{DS0}} + \underbrace{dI_{DS}}_{=} \end{aligned}$$

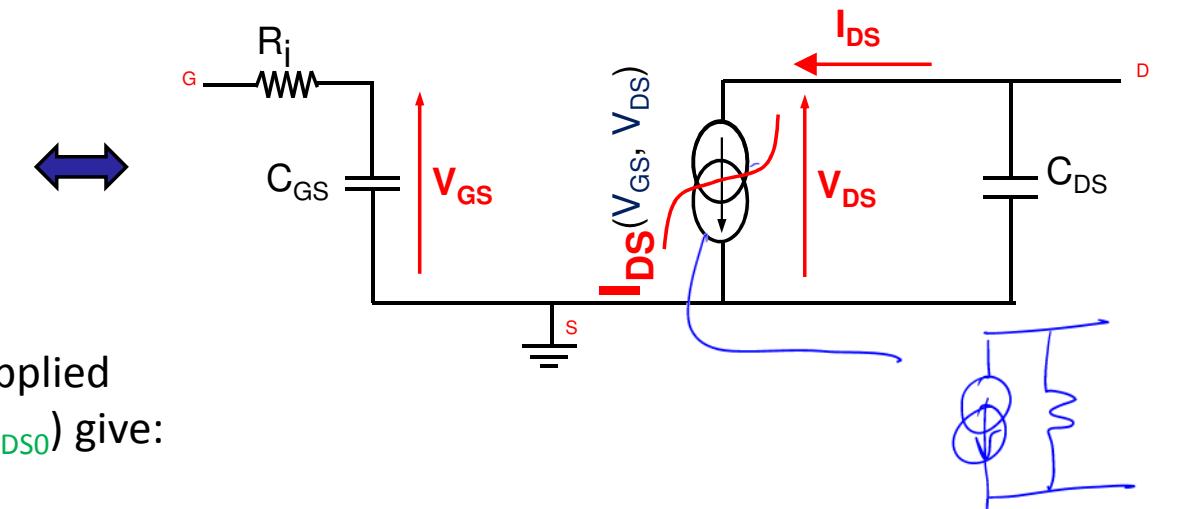


$$\begin{aligned} I_{DS}(t) &= \overbrace{I_{DS0}} + \underbrace{dI_{DS}}_{=} \\ &\quad + \text{Taylor expansion} \end{aligned}$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm , gd) around a specific bias point

$$f(x,y) \quad d\int = (\quad) dx + (\quad) dy =$$



Small signals (dv_{GS} , dv_{DS}) applied
around the bias point (V_{GS0} , V_{DS0}) give:

$$V_{GS}(t) = V_{GS0} + dv_{GS}(t) \quad \rightarrow \quad I_{DS}(t) = I_{DS0} + di_{DS}$$

$$V_{DS}(t) = V_{DS0} + dv_{DS}(t)$$

Taylor expansion

$$di_{DS} = dF_{NL} = \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right)_{(V_{GS0}, V_{DS0})} \cdot dv_{GS} + \left(\frac{\delta I_{DS}}{\delta V_{DS}} \right)_{(V_{GS0}, V_{DS0})} \cdot dv_{DS}$$

gm

$gd = 1/R_{DS}$

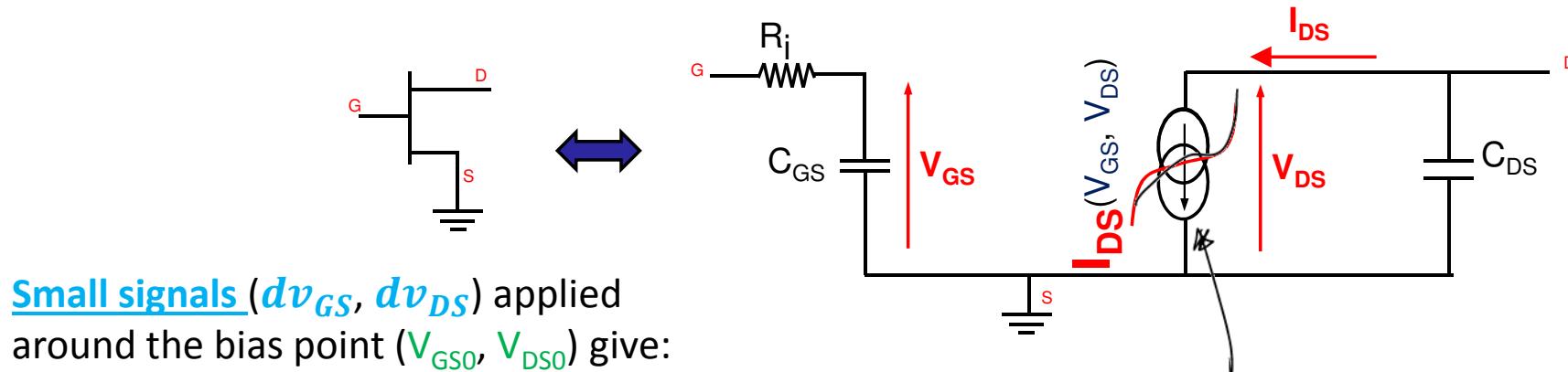
$$g_m = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{(V_{GSO}, V_{DSO})} = \underline{\text{FET transconductance}} = S = \Omega^{-1}$$

$$g_D \approx g_{DS} = \left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{(V_{GSO}, V_{DSO})} = \underline{\text{Drain-Source conductance}} = \Omega^{-1}$$

$$R_{DS} = \frac{1}{g_{DS}}$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm , gd) around a specific bias point

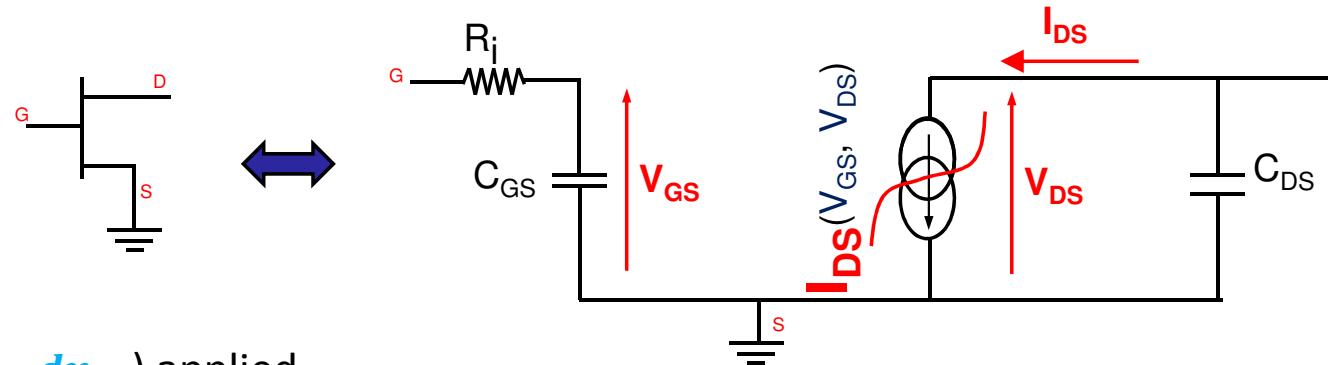


$$\frac{dV_{GS}(t)}{dV_{DS}(t)} \longrightarrow I_{DS}(t) = I_{DS0} + di_{DS}$$

$$di_{DS} = dF_{NL} = \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right)_{(V_{GSO}, V_{DSO})} \cdot dV_{GS} + \left(\frac{\delta I_{DS}}{\delta V_{DS}} \right)_{(V_{GSO}, V_{DSO})} \cdot dV_{DS} = g_m \cdot dV_{GS} + g_{DS} \cdot dV_{DS}$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (g_m , g_d) around a specific bias point



Small signals (dV_{GS} , dV_{DS}) applied
around the bias point (V_{GSO} , V_{DSO}) give:

$$\frac{dV_{GS}(t)}{dV_{DS}(t)} \rightarrow \cancel{di_{DS}} = g_m \cdot \cancel{dv_{GS}} + g_{DS} \cdot \cancel{dv_{DS}}$$

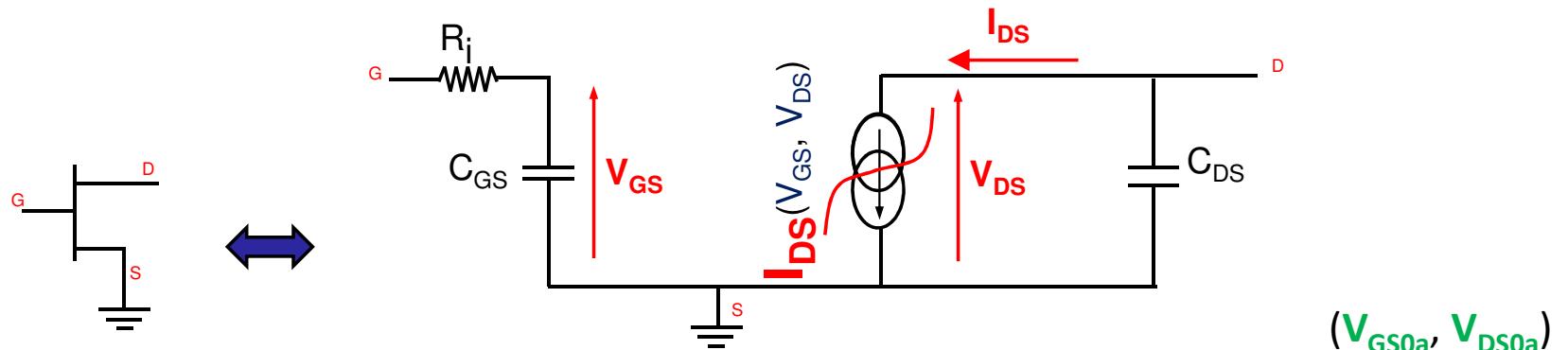
$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right) \Big|_{(V_{GSO}, V_{DSO})}$$

$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}} \right) \Big|_{(V_{GSO}, V_{DSO})}$$

$$I_{DS} = g_m \cdot V_{GS} + g_{DS} \cdot V_{DS}$$

$$V_{DS} = V_{DSO} + \Delta V_{DS}$$

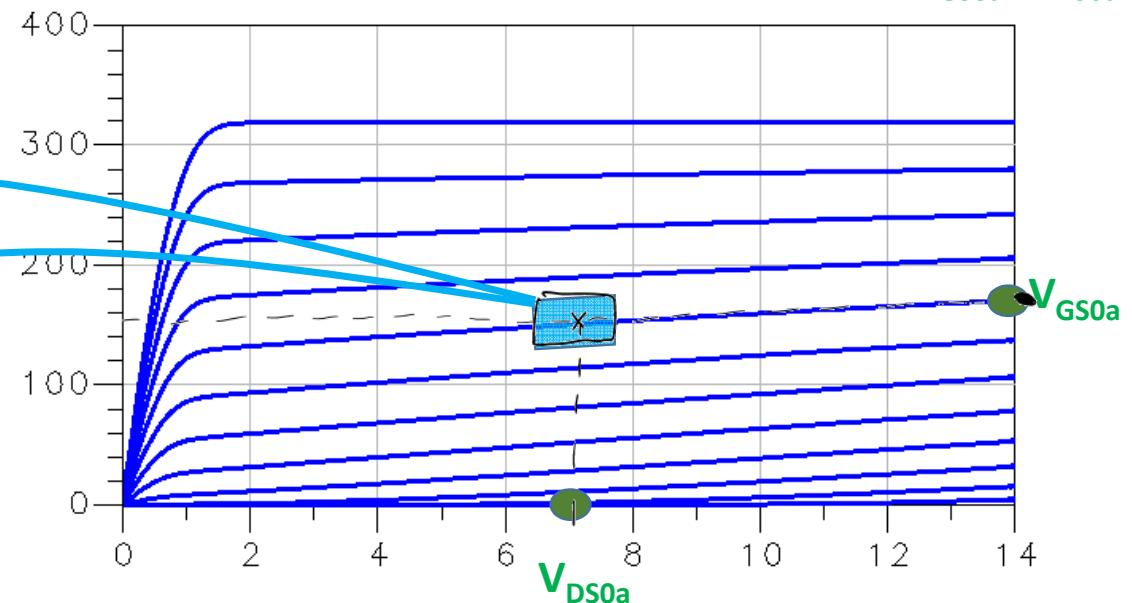
I – Basics of FET operation



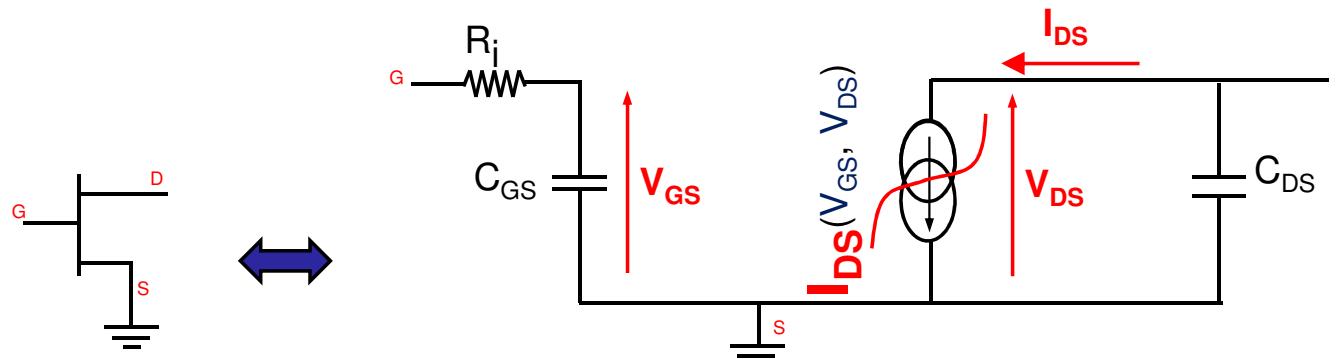
Small signals (dV_{GS} , dV_{DS}) applied around the bias point (V_{GS0} , V_{DS0}) give:

$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right) \Big|_{(V_{GS0}, V_{DS0})}$$

$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}} \right) \Big|_{(V_{GS0}, V_{DS0})}$$



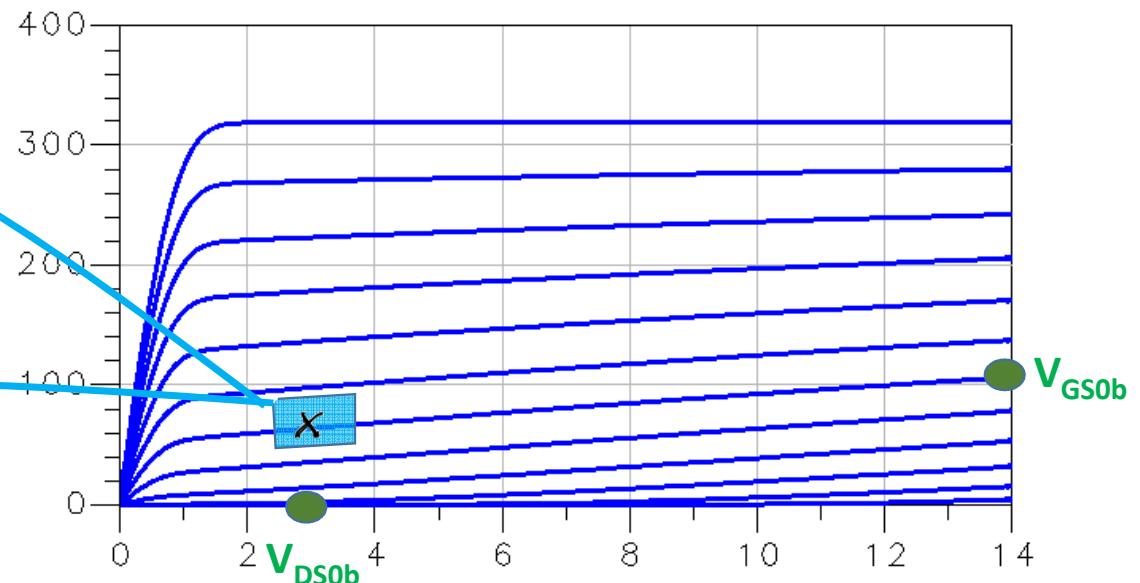
I – Basics of FET operation



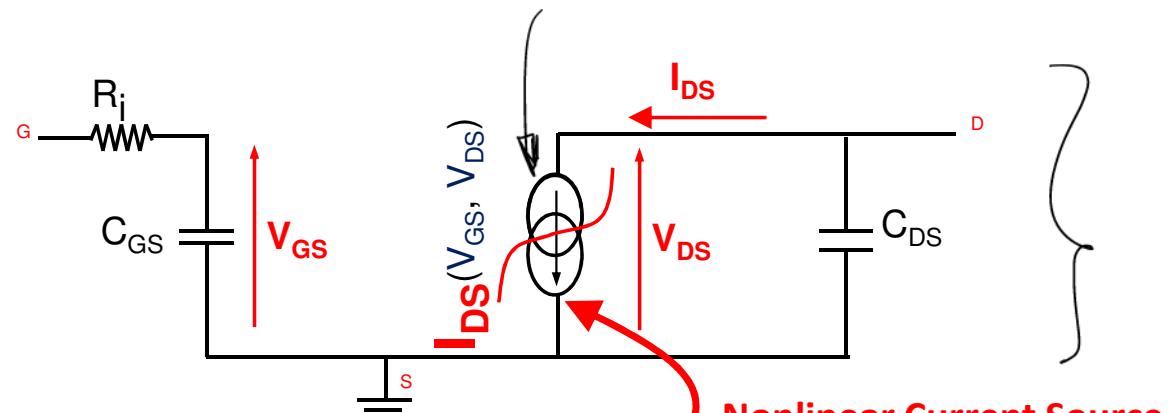
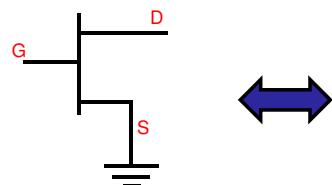
Small signals (δV_{GS} , δV_{DS}) applied around the bias point (V_{GS0} , V_{DS0}) give:

$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right)_{(V_{GS0}, V_{DS0})}$$

$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}} \right)_{(V_{GS0}, V_{DS0})}$$



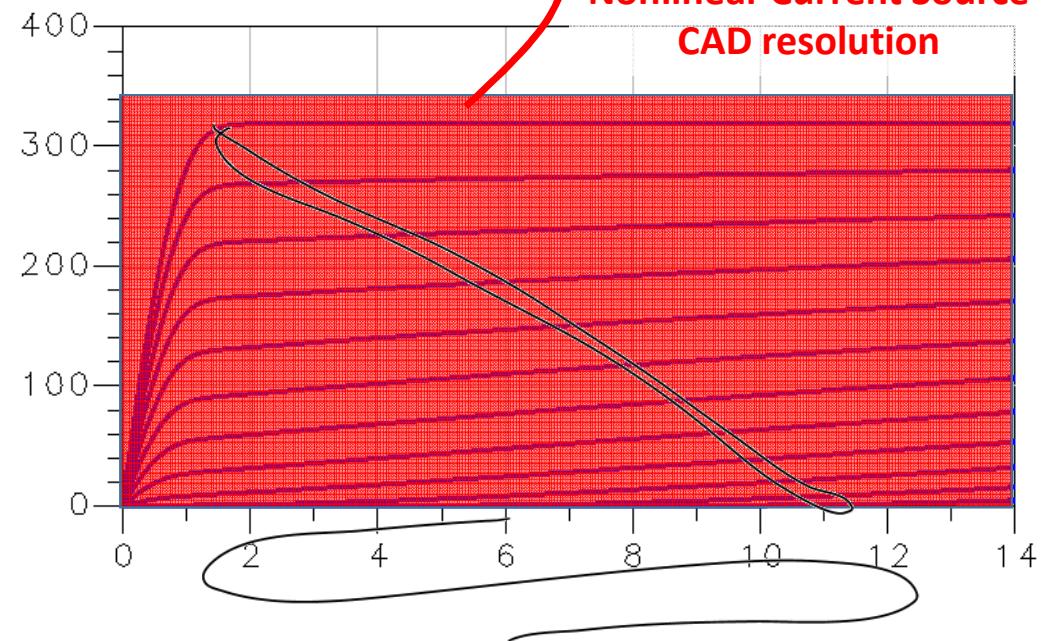
I – Basics of FET operation



Large signals (ΔV_{GS} , ΔV_{DS}) applied around the bias point (V_{GSO} , V_{DSO}) give:

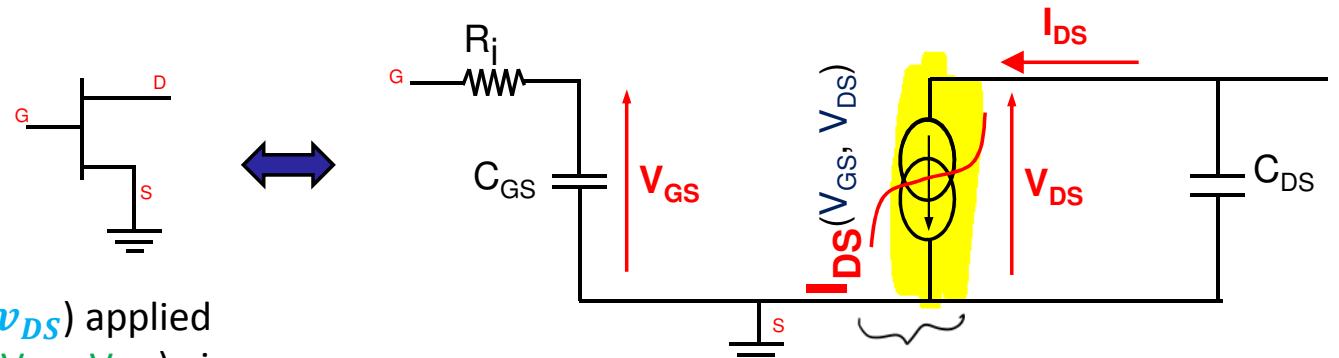
~~$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right) \Big|_{(V_{GSO}, V_{DSO})}$$~~

~~$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}} \right) \Big|_{(V_{GSO}, V_{DSO})}$$~~



I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (g_m , g_d) around a specific bias point

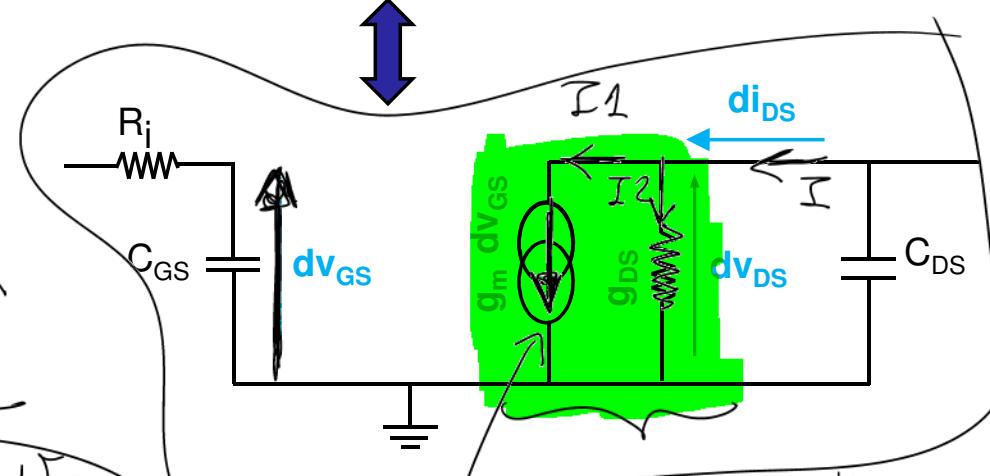


Small signals (dv_{GS} , dv_{DS}) applied around the bias point (V_{GSO} , V_{DSO}) give:

$$\begin{aligned} V_{GS} &= V_{GSO} + dv_{GS} \\ V_{DS} &= V_{DSO} + dv_{DS} \end{aligned} \quad \left\{ \right.$$

$$di_{DS} = g_m \times dv_{GS} + g_d \times dv_{DS}$$

$$I = I_1 + I_2 = \frac{dv_{DS}}{R_{DS}}$$

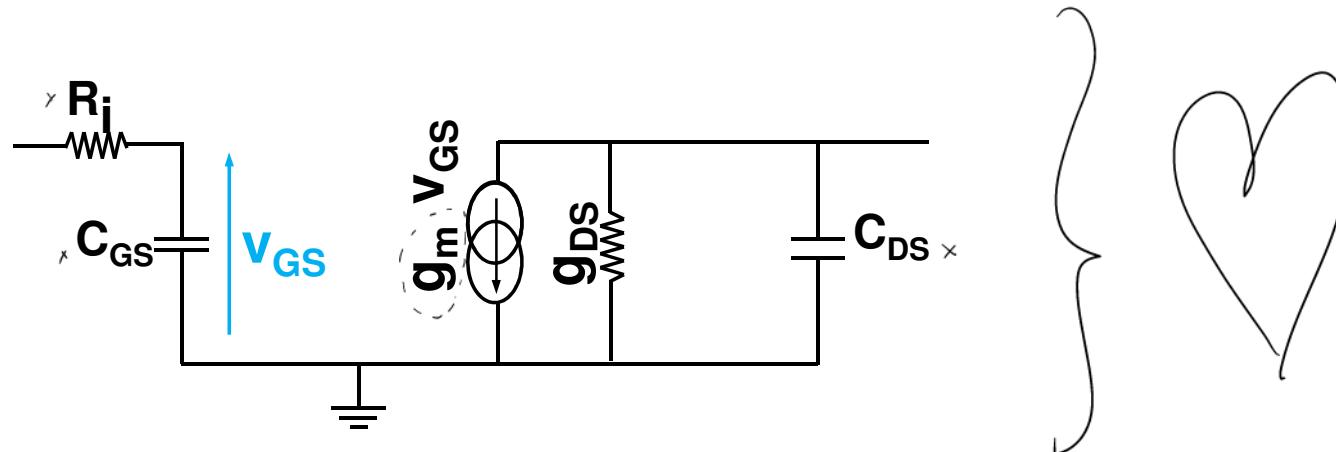


$$\begin{aligned} I &\downarrow \\ R &\quad \uparrow \\ V &= RI \\ I &= \frac{V}{R} \end{aligned}$$

Ohm's Law

I – Basics of FET operation

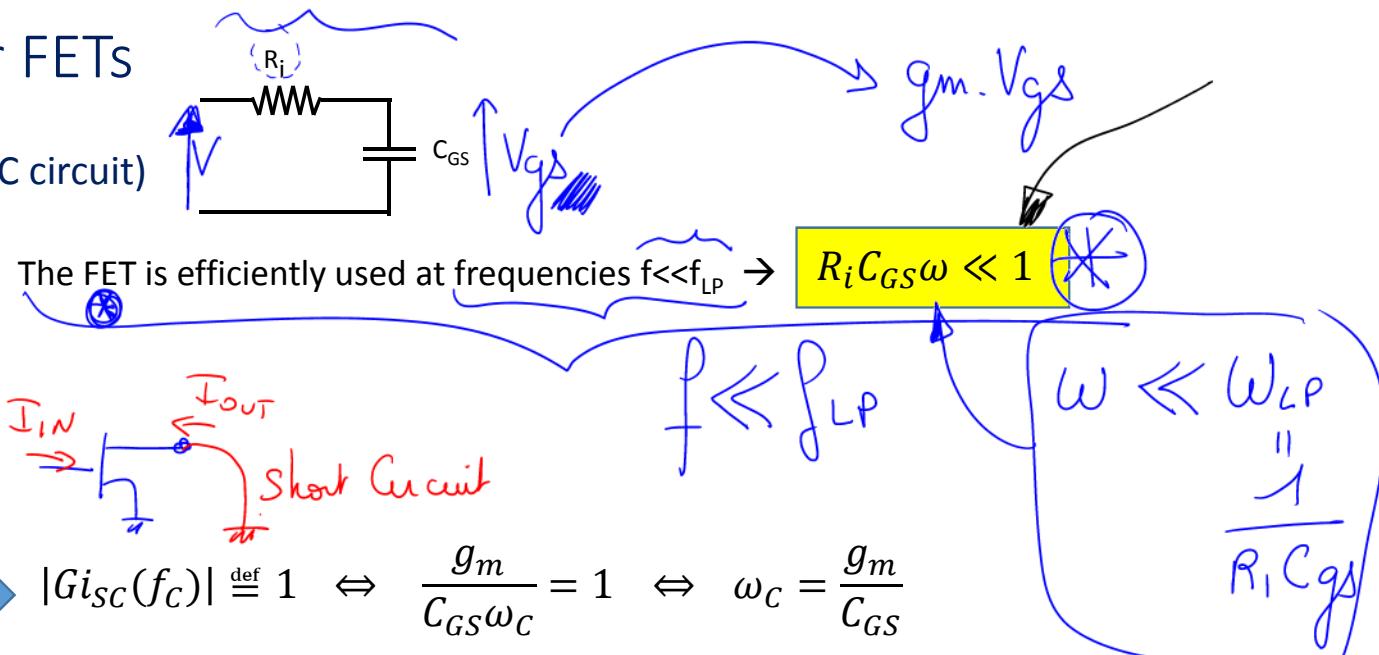
→ Simplified Small-signal equivalent of the nonlinear drain current (g_m , g_d) around a specific bias point



II – Intrinsic figures of merit for FETs

1) Low-Pass Frequency (Low-Pass Input RC circuit)

$$f_{LP} = \frac{1}{2\pi R_i C_{GS}}$$



2) Cutoff frequency of gain current

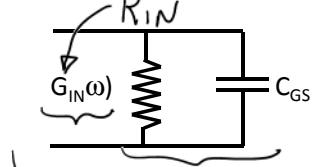
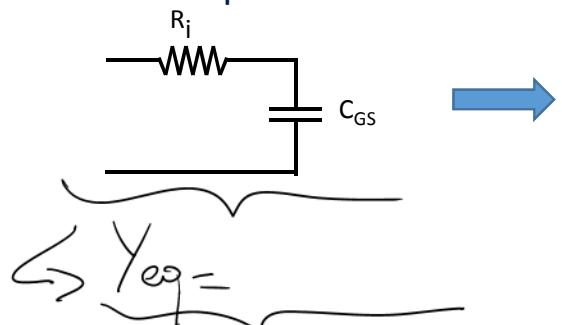
Current Gain in Short-Circuit

$$G_{ISC} = \frac{I_{OUTSC}}{I_{IN}} = \frac{g_m V_{GS}}{j C_{GS} \omega V_{GS}} = \frac{g_m}{j C_{GS} \omega} \rightarrow |G_{ISC}(f_c)| \stackrel{\text{def}}{=} 1 \Leftrightarrow \frac{g_m}{C_{GS} \omega_c} = 1 \Leftrightarrow \omega_c = \frac{g_m}{C_{GS}}$$

$$f_c = \frac{g_m}{2\pi C_{GS}}$$

f_c is widely used to compare FETs with each other

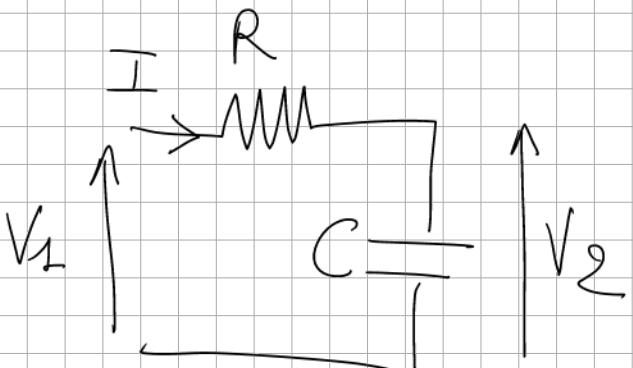
→ Narrowband equivalence between (series RC) and (parallel RC) circuit at the FET input



$$G_{IN}(\omega) = R_i C_{GS}^2 \omega^2$$

$$R_{IN} = \frac{1}{G_{IN}}$$

$$Y_{eq} = \left(\frac{1}{R_{IN}} \right) + j (C_{GS} \omega)$$



$$\begin{cases} V_2 = Z_C \times I \\ V_1 = (R + Z_C) I \end{cases}$$

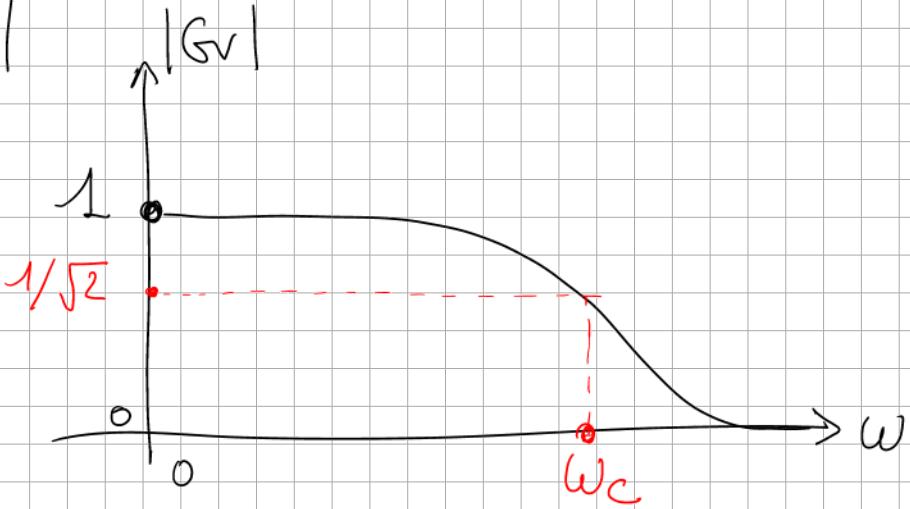
$$Z_C = \frac{1}{j C \omega}$$

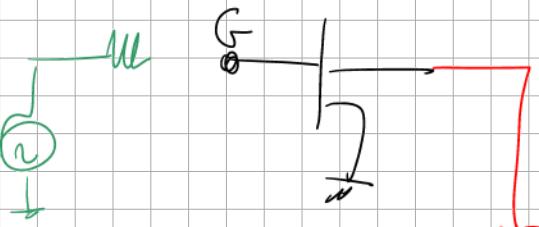
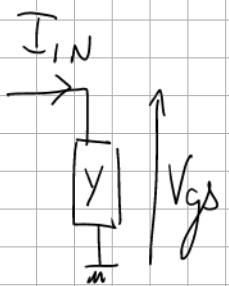
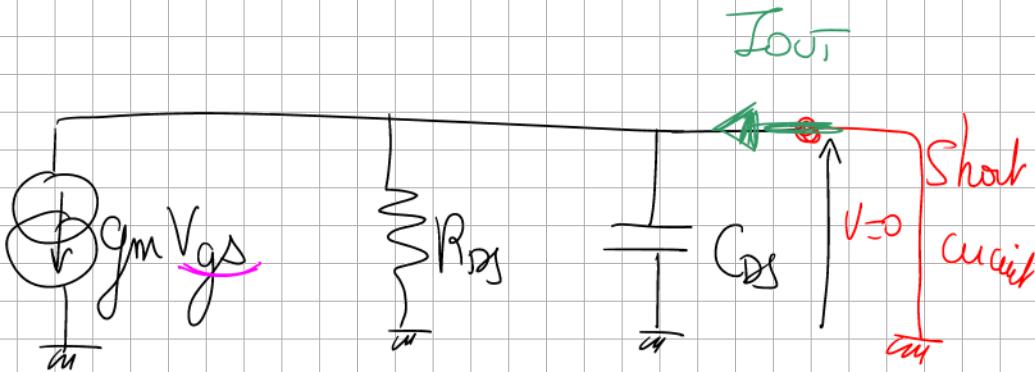
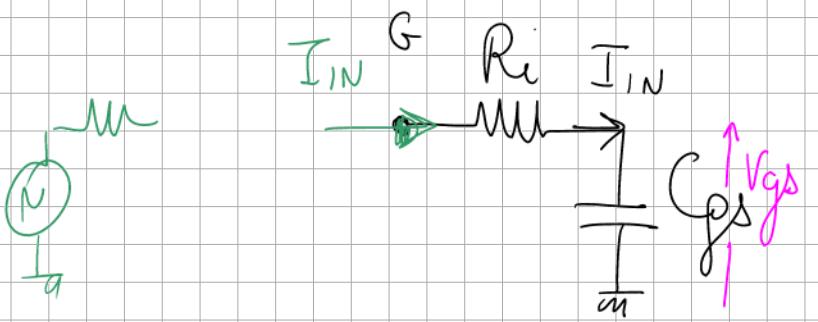
$$\frac{V_2}{V_1} = \frac{Z_C}{R + Z_C} = \frac{1}{1 + \frac{R}{Z_C}}$$

$$\frac{V_2}{V_1} = \frac{1}{1 + j RC\omega}$$

$$\rightarrow \left| \frac{V_2}{V_1} \right| = \frac{1}{\sqrt{1 + (RC\omega)^2}} = |G_V|$$

$$\omega_C = \frac{1}{RC} \rightarrow f_C = \frac{1}{2\pi RC}$$





$$V = Z I$$

$$Z = \frac{V}{I} = Y \times V$$

$$I_{IN} = Y_{GS} \times V_{GS}$$

$$\boxed{I_{IN} = (j C_{GS} \omega) V_{GS}}$$

$$\boxed{I_{OUT} = g_m \cdot V_{GS}}$$

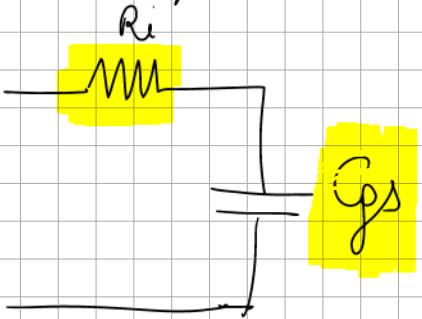
$$\left| G_{I_{SC}}(f_c) \right| = 1$$

$$\frac{g_m}{C_{GS} \omega_c} \stackrel{\triangle}{=} 1$$

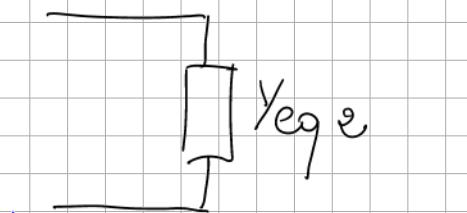
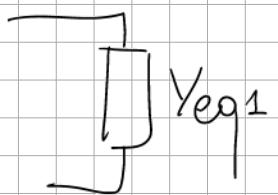
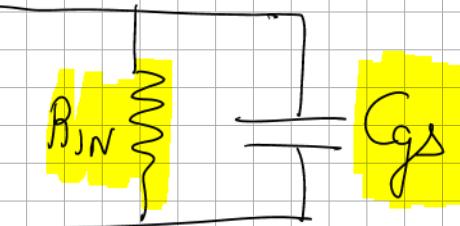
$$G_{I_{SC}} = \frac{f_{OUT}}{I_{IN}} = \frac{g_m \cdot V_{GS}}{(j C_{GS} \omega) V_{GS}} = \frac{g_m}{j C_{GS} \omega}$$

$$\frac{g_m}{j C_{GS} \omega}$$

Equivalent parallel circuit at the output



\equiv



$$Z_{eq1} = R_i + \frac{1}{j G_s \omega} = \frac{1 + j R_i G_s \omega}{j G_s \omega}$$

$$Y_{eq1} = \frac{j G_s \omega}{1 + j R_i G_s \omega}$$

$$= \frac{j G_s \omega (1 - j R_i G_s \omega)}{1 + (R_i G_s \omega)^2}$$

$f \ll f_{LP}$

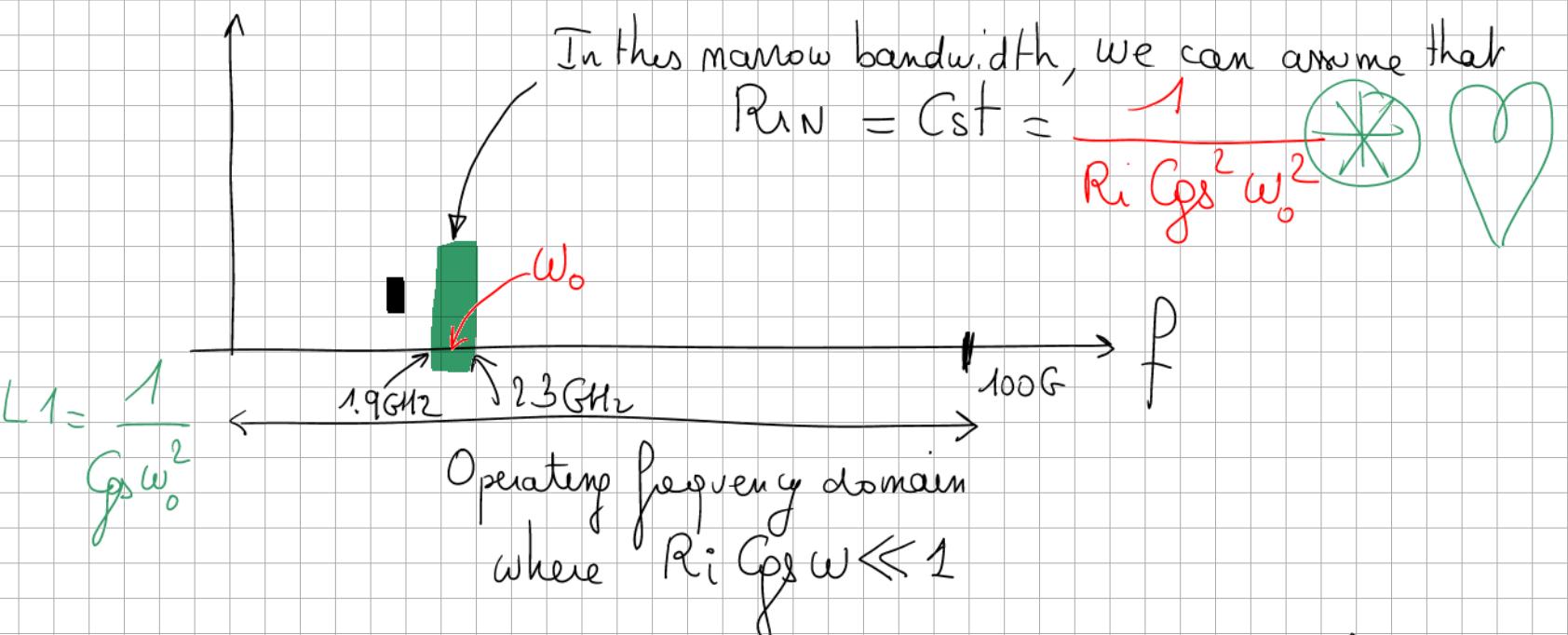
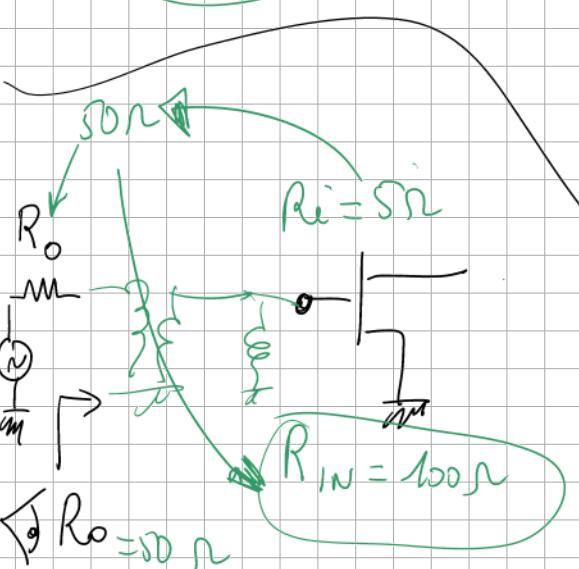
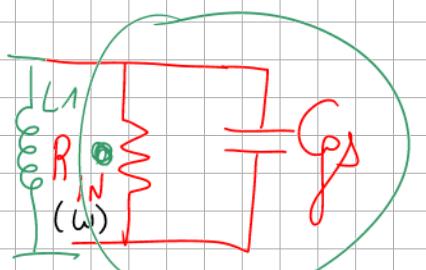
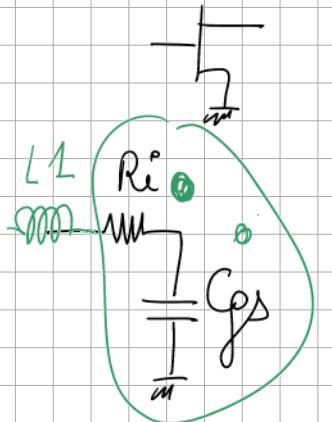
$$|R_i G_s \omega| \ll 1$$

$$Y_{eq2} = \frac{1}{R_{IN}} + j G_s \omega$$

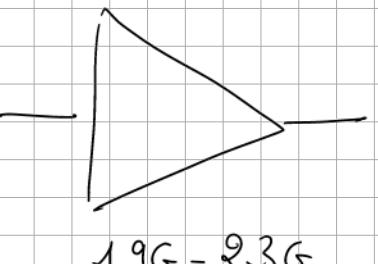
$$(R_i G_s \omega)^2$$

$$j G_s \omega$$

$$R_{IN} = \frac{1}{R_i G_s^2 \omega^2} = R_{IN}(\omega)$$



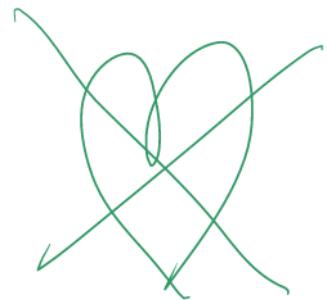
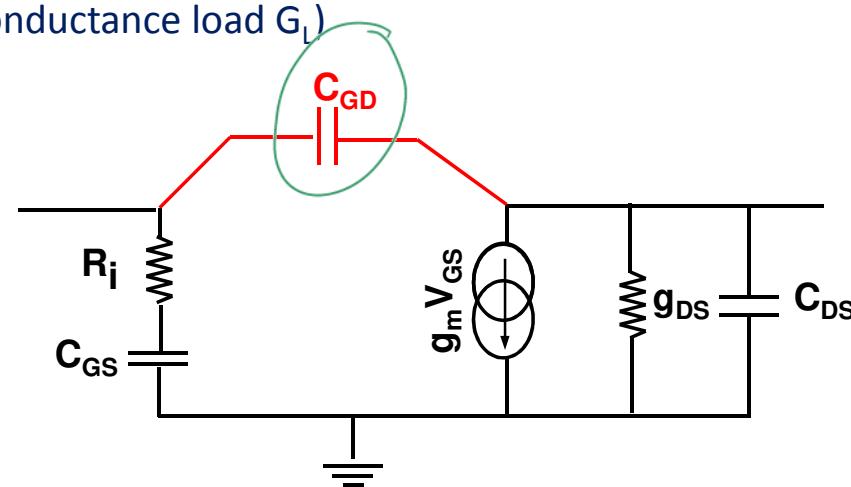
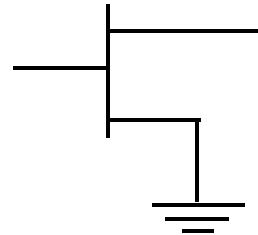
e.g.: $R_i = 4 \Omega$
 $C_{gs} = 2 \text{ pF}$



$R_{IN} = 10$

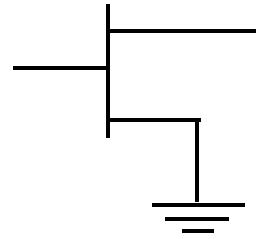
$R_o \propto R_{IN}$

II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

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3) Miller Effect (Feedback admittance Y_R and conductance load G_L)



$$Y_R = j C_{GD} \omega$$

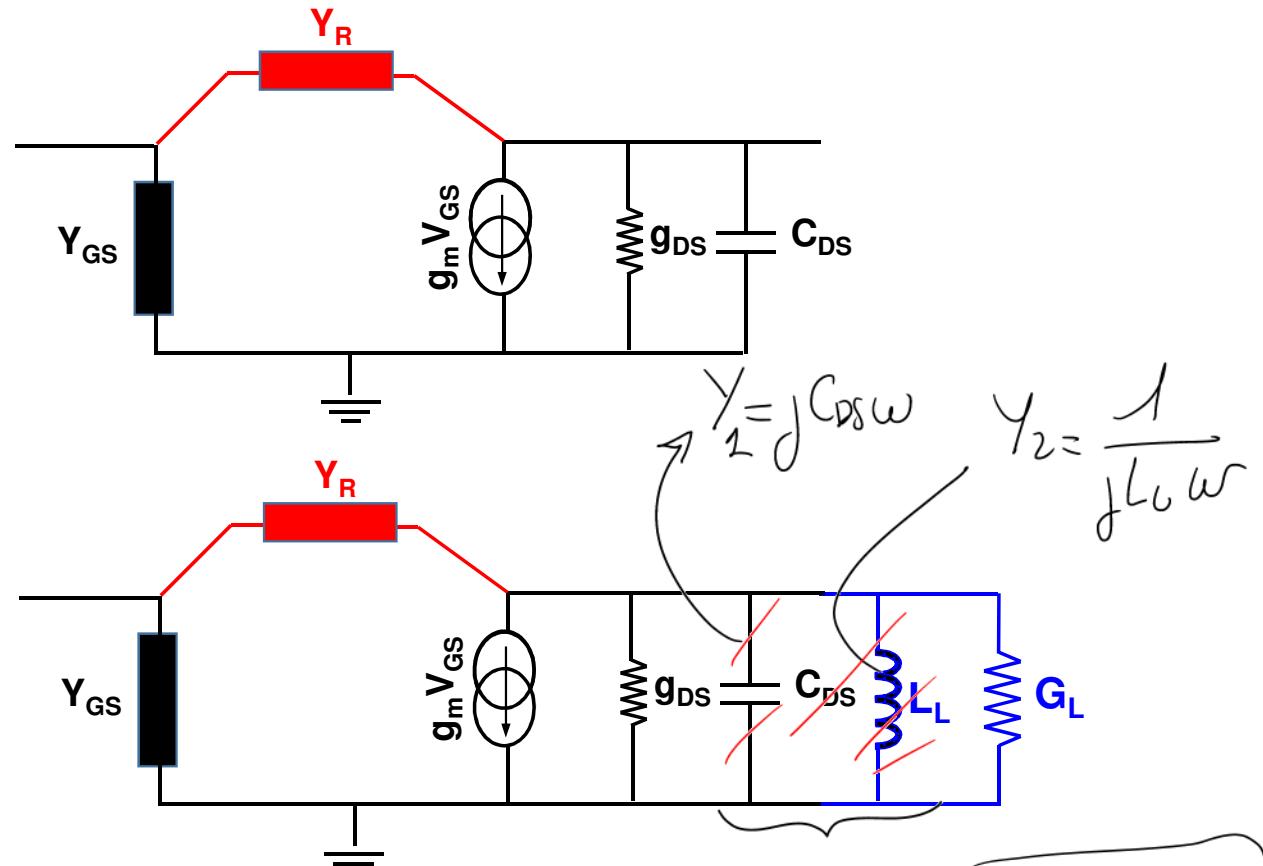
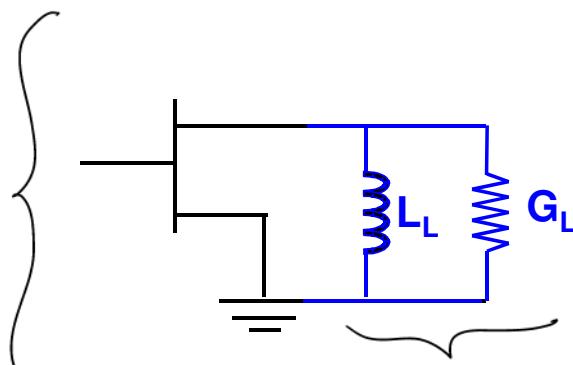
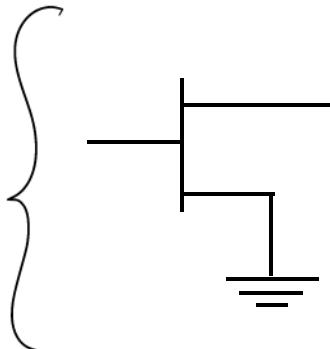
$$Y_R = j C_{GD} \omega$$

$$Y_{GS} = \frac{1}{R_i + \frac{1}{j C_{GS} \omega}}$$

$$Y_{GS} = \frac{1}{R_{IN}} + j G_S \omega$$

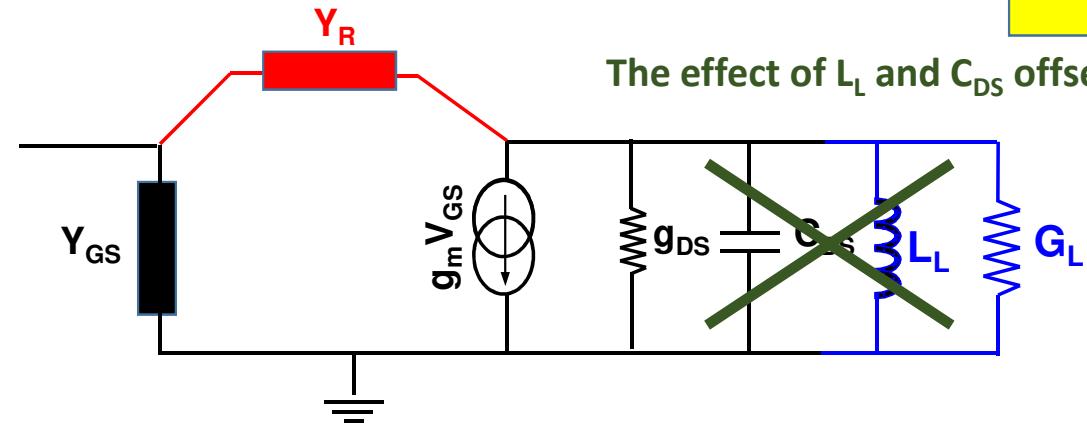
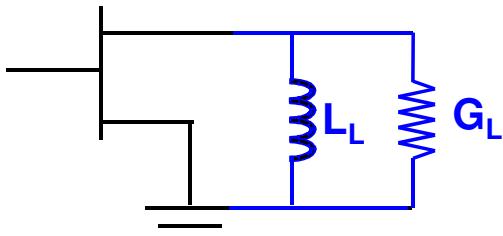
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3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

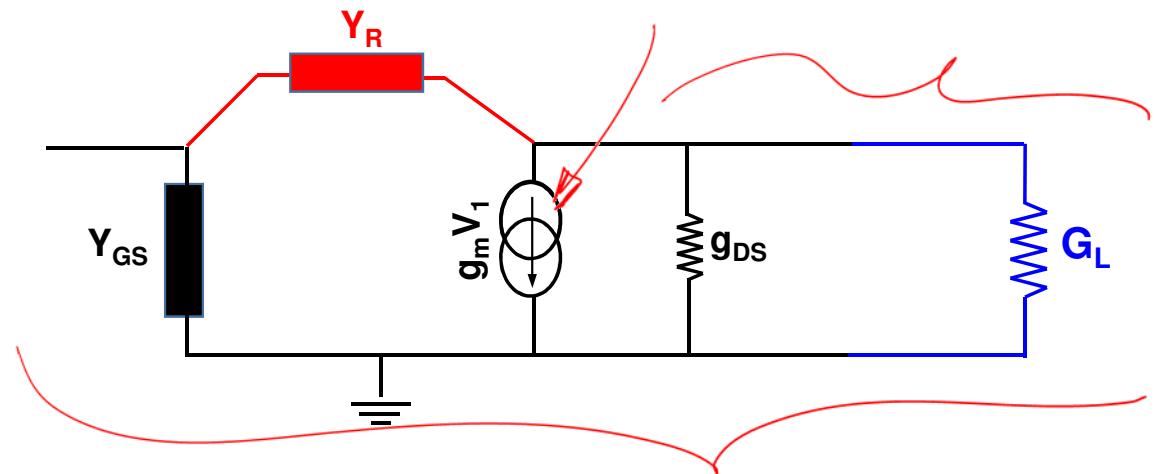
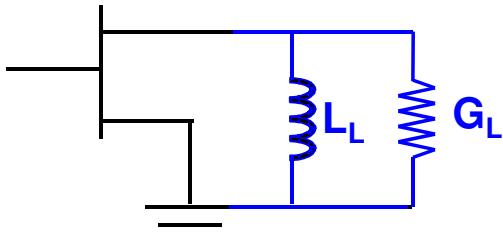


$$Y_1 + Y_2 = 0 \rightarrow \Leftrightarrow j C_{DS} \omega = \frac{-1}{j L_L \omega} \Rightarrow \boxed{L_L C_{DS} \omega^2 = 1}$$

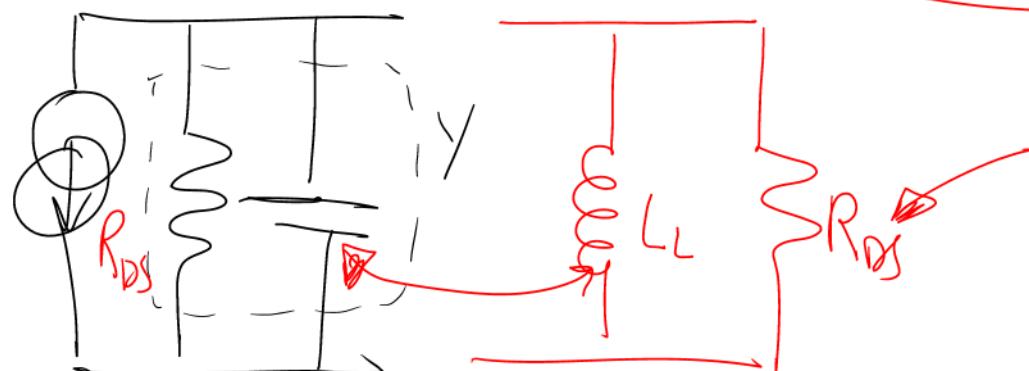
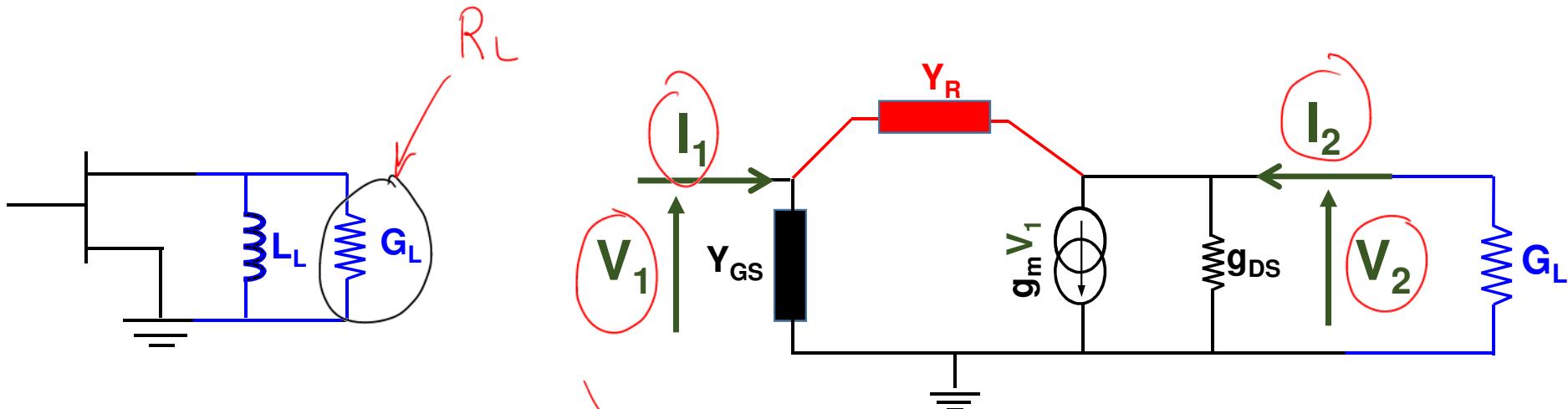
II – Intrinsic figures of merit for FETs

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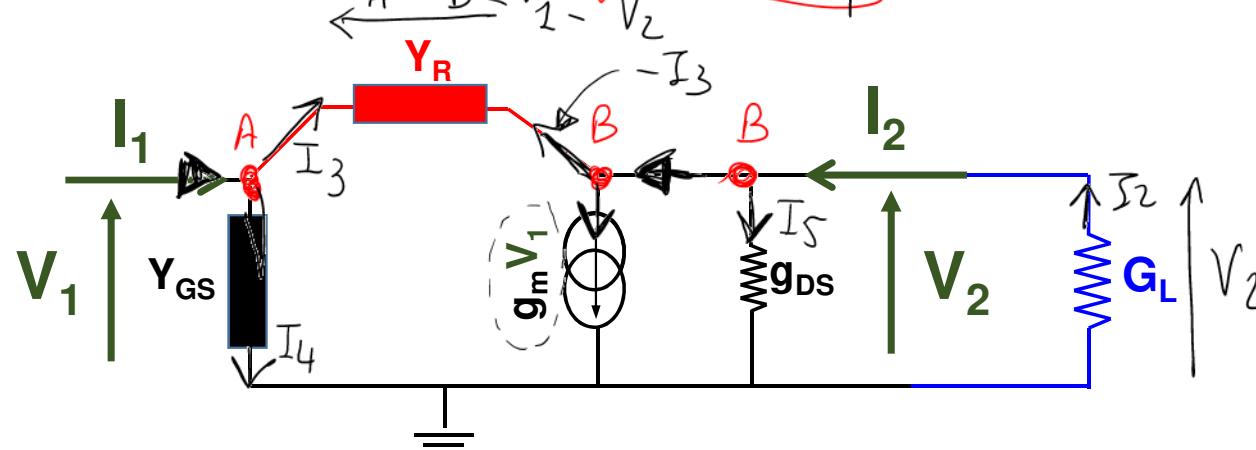
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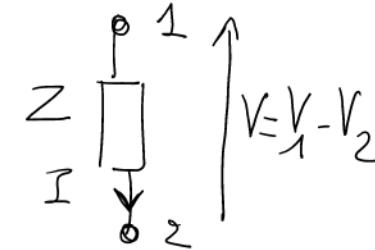
a) Voltage gain G_V



$$G_V = \frac{V_2}{V_1} = -\frac{g_m - Y_R}{g_{DS} + G_L + Y_R}$$

$$\frac{V_A - V_B}{V_1 - V_2} \approx \frac{V_A - V_B}{V_1 - V_2}$$

$$-\frac{g_m}{g_{DS} + G_L} \rightarrow -\frac{g_m}{2g_{DS}}$$



$$V = Z I$$

$$I = Y V$$

$$\textcircled{1} \quad I_1 = I_3 + I_4 = Y_R (V_1 - V_2) + Y_{GS} V_1$$

$$\textcircled{2} \quad I_2 = I_5 + g_m V_1 - I_3 = g_{DS} V_2 + g_m V_1 - Y_R (V_1 - V_2) = -G_L V_2$$

$$Q \rightarrow V_2 \left[g_{DS} + Y_R + G_L \right] = \left(-g_m + Y_R \right) V_1$$

· ↴

$$\frac{V_2}{V_1} = \frac{-g_m + Y_R}{g_{DS} + G_L + Y_R} = -\frac{(g_m - Y_R)}{g_{DS} + G_L + Y_R}$$

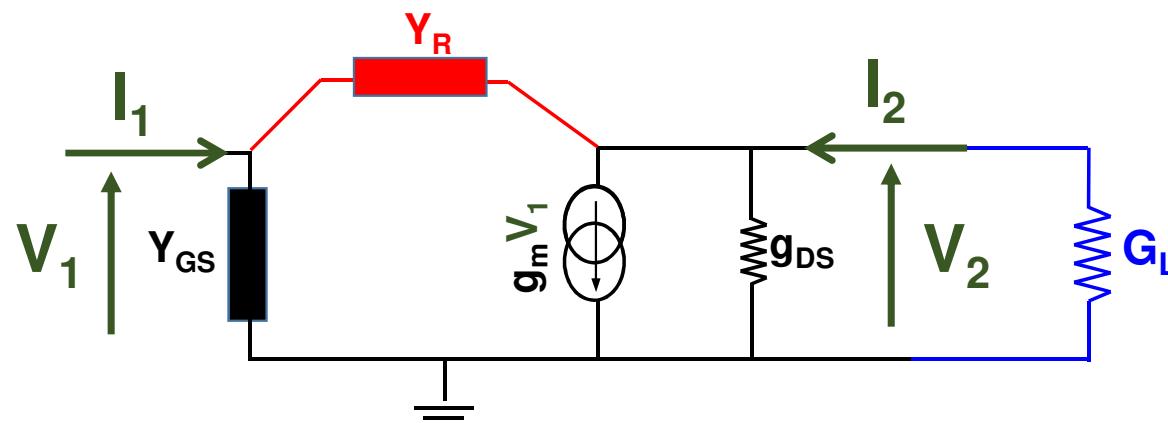
$$Y_{IN} = \frac{I_1}{V_1}$$

II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

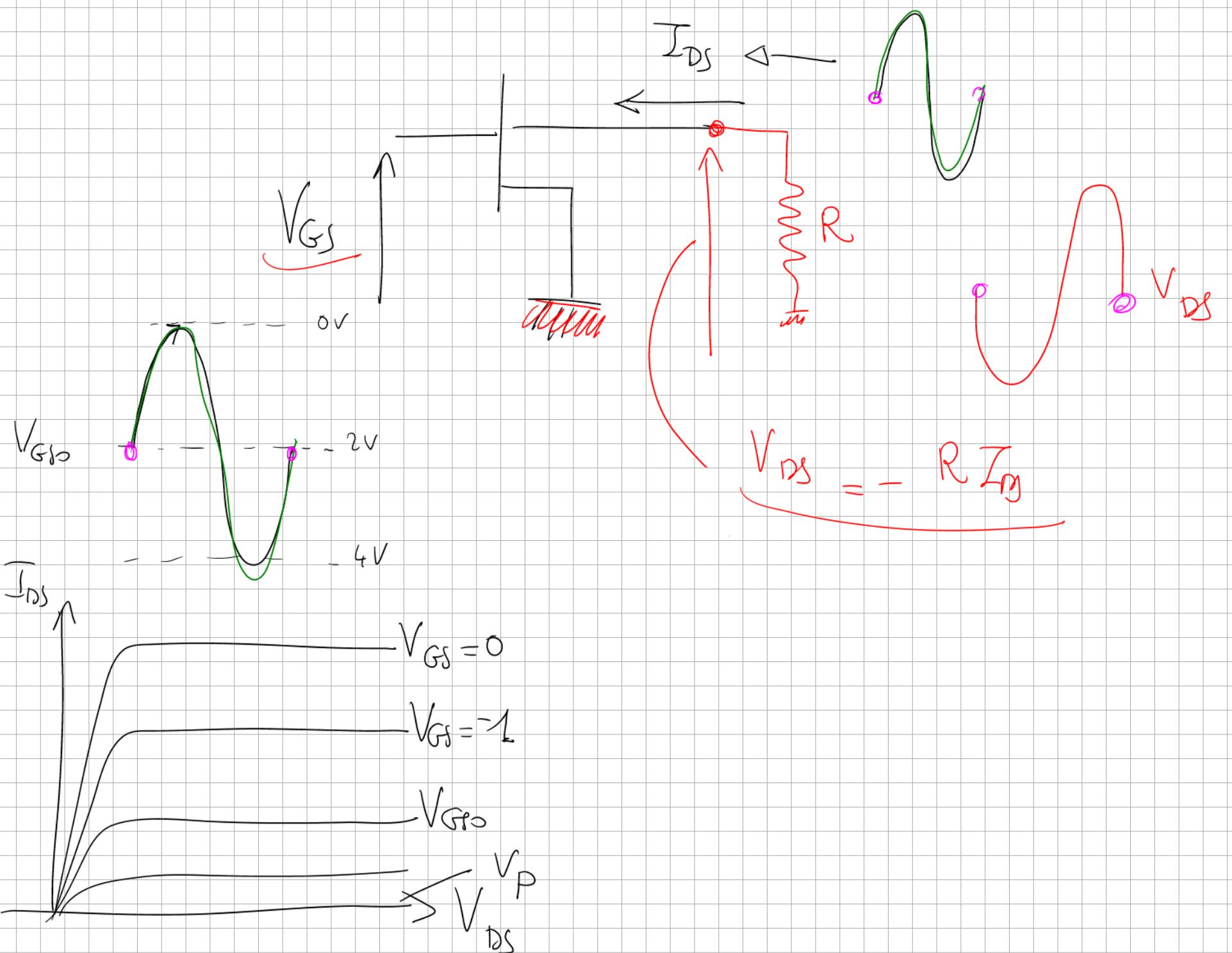
b) Input admittance Y_{IN}

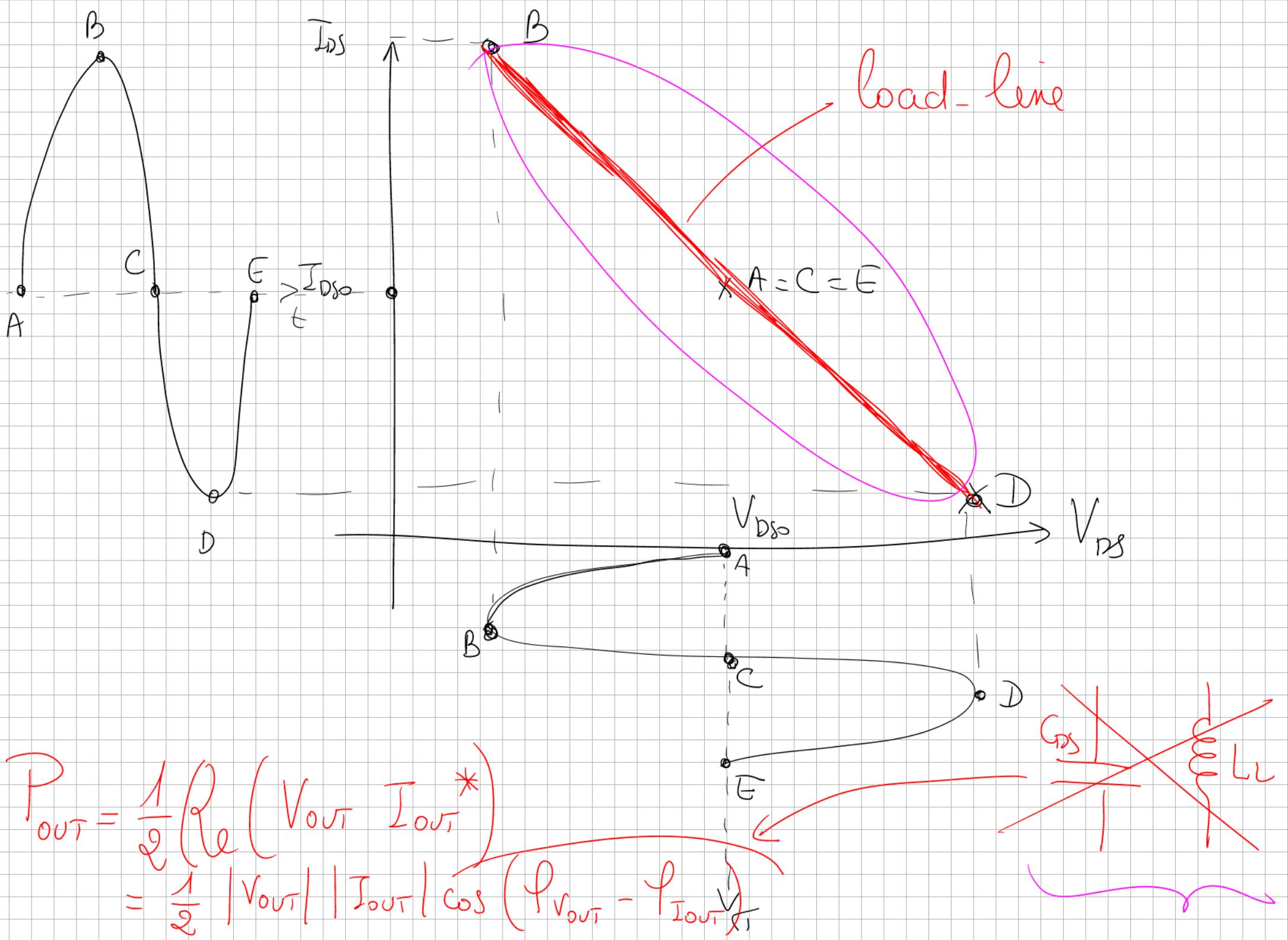
$$Y_{IN} = \frac{I_1}{V_1} = Y_{GS} + Y_R[1 - G_V]$$



$$\textcircled{1} \quad I_1 = Y_{GS} V_1 + Y_R (V_1 - V_2) \rightarrow Y_{IN} = \frac{I_1}{V_1} = Y_{GS} + Y_R (1 - G_V)$$

In the case of FETs, $|G_V| \gg 1$



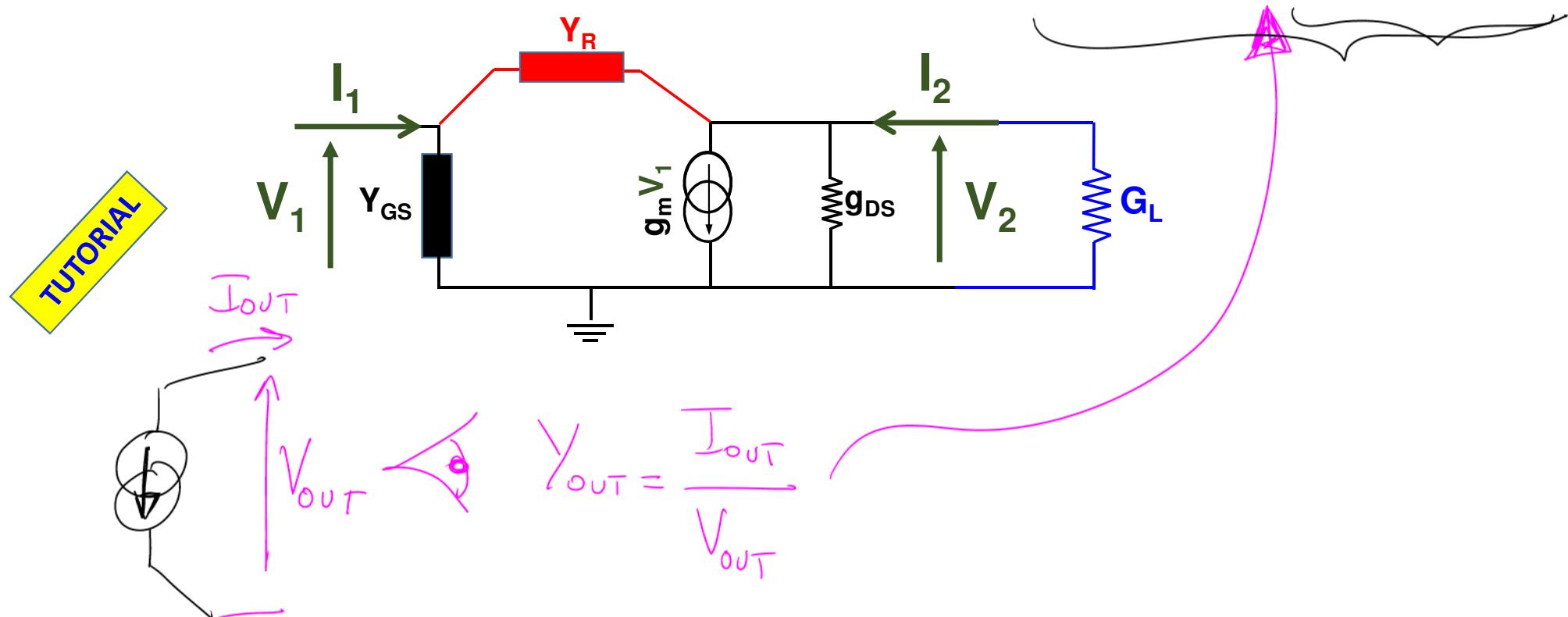


II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

c) Output admittance seen by the drain current source Y_{OUT}

$$Y_{OUT} = \frac{-g_m V_1}{V_2} = g_{DS} + G_L + Y_R \left[1 - \frac{1}{G_V} \right]$$



$$① I_1 = Y_{GS} V_1 + Y_R (V_1 - V_2)$$

$$② I_2 = g_{DS} V_2 + \underbrace{g_m V_1}_{+} + Y_R (V_2 - V_1) = -G_L V_2$$

$$Y_{OUT} = \frac{I_{OUT}}{V_{OUT}} = \frac{-g_m V_1}{V_2} = \frac{-g_m}{G_V} = \frac{-g_m}{\cancel{g_m - Y_R}}$$

$$\Rightarrow g_m V_1 = -g_{DS} V_2 - Y_R (V_2 - V_1) - G_L V_2$$

$$\Rightarrow Y_{OUT} = \frac{-g_m V_1}{V_2} = g_{DS} + Y_R \left(1 - \frac{V_1}{V_2} \right) + G_L$$

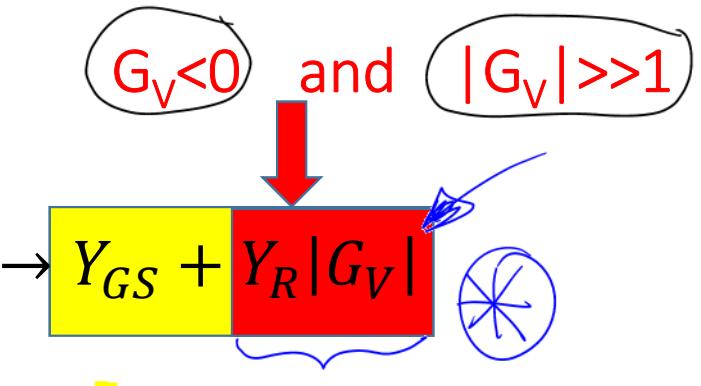
$$Y_{OUT} = g_{DS} + G_L + \left(Y_R \left(1 - \frac{1}{G_V} \right) \right)$$

II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

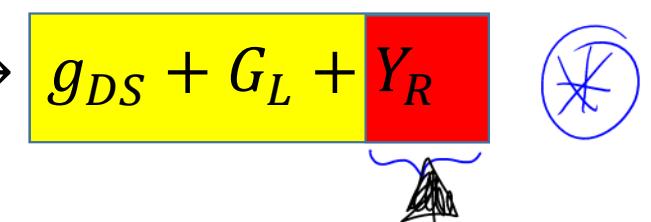
b) Input admittance Y_{IN}

$$Y_{IN} = Y_{GS} + Y_R [1 - G_V]$$



c) Output admittance seen by the drain current source Y_{OUT}

$$Y_{OUT} = g_{DS} + G_L + Y_R \left[1 - \frac{1}{G_V} \right]$$



$$1 - \frac{1}{G_V} = 1 + \frac{1}{|G_V|}$$

$$1 - G_V = 1 + |G_V| \rightarrow |G_V|$$

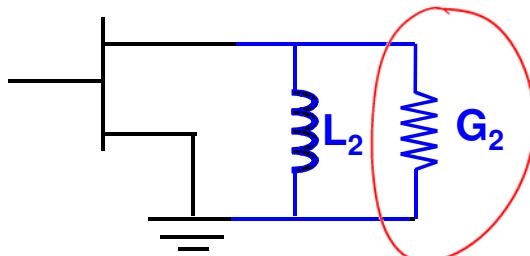
because $G_V < 0$

$$|G_V| \gg 1$$

$$j C_{GD} \omega$$

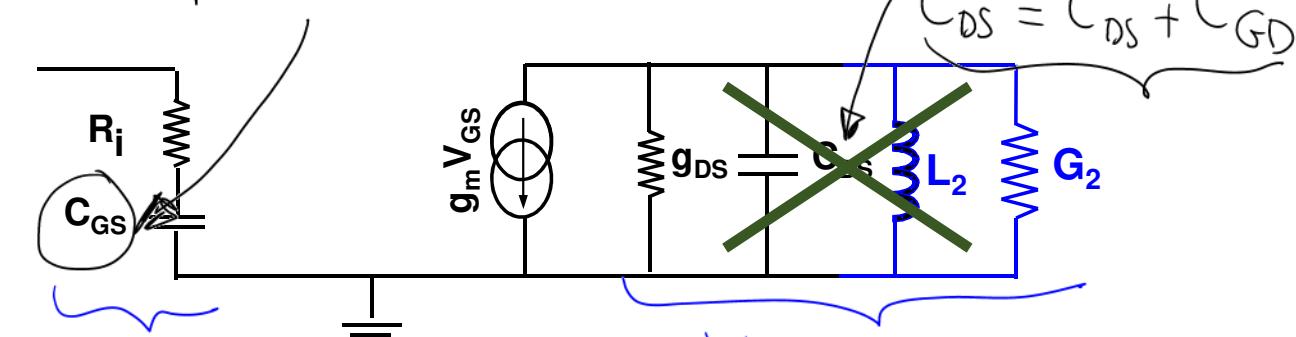
II – Intrinsic figures of merit for FETs

3) Maximum Power Gain G_{MAX} → Simplified Electrical Small-Signal FET Model



$$C_{GS} = C_{GS} + |G_V| G_d$$

$$L_2 C_{DS} \omega^2 = 1 \rightarrow L_2 = \frac{1}{C_{DS} \omega^2}$$



$$Y_R = j C_{GD} \omega$$

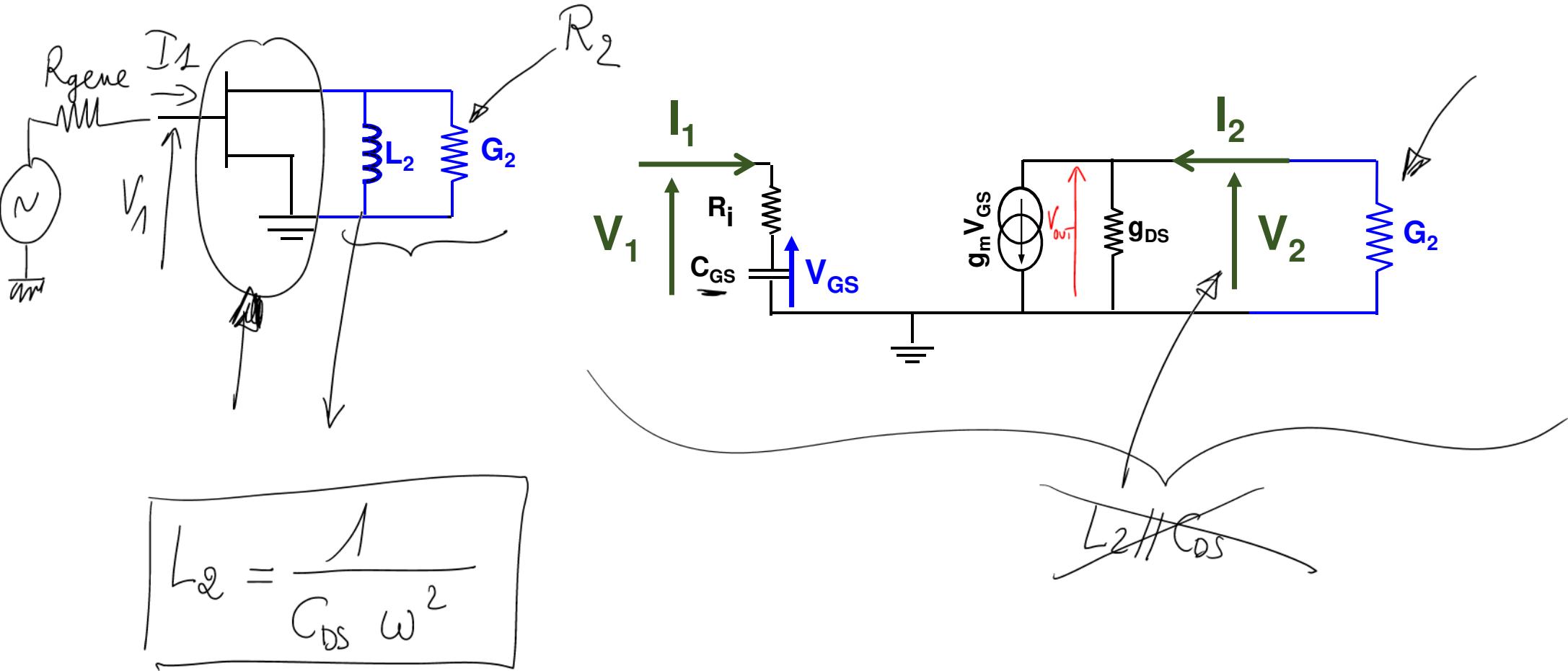
$$Y_{IN} = Y_{GS}$$

$$Y_{IN} = \frac{1}{R_{IN}} + j C_{GS} \omega + j |G_V| C_{GD} \omega$$

$$j C_{eq} \omega \text{ where } C_{eq} = C_{GS} + |G_V| C_{GD}$$

II – Intrinsic figures of merit for FETs

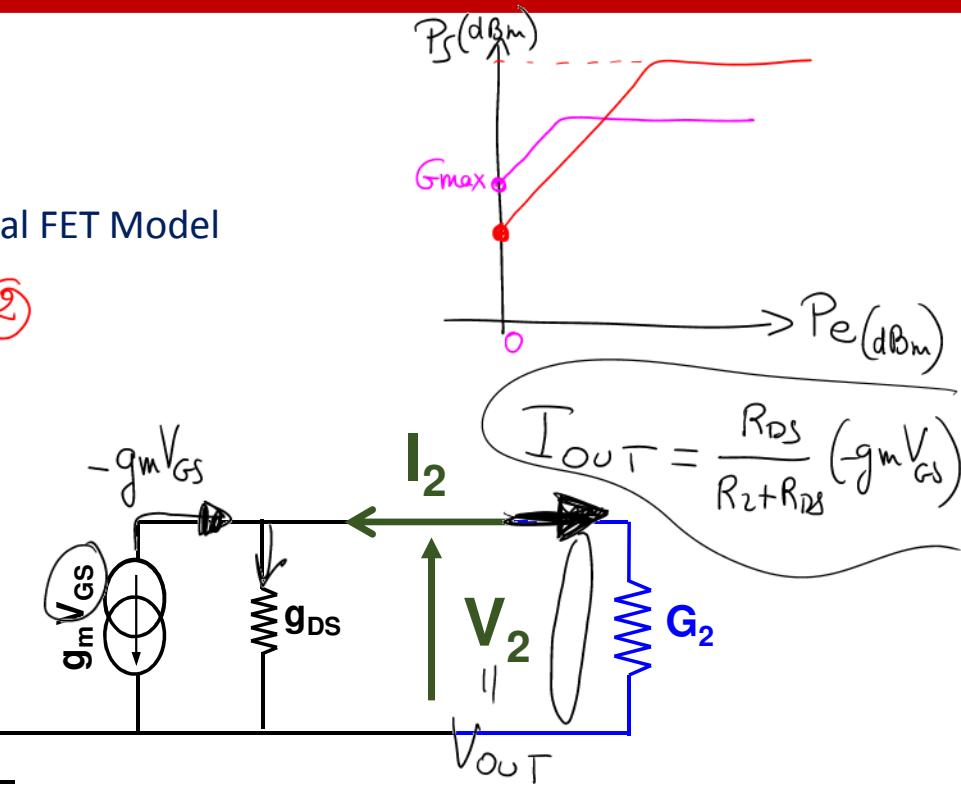
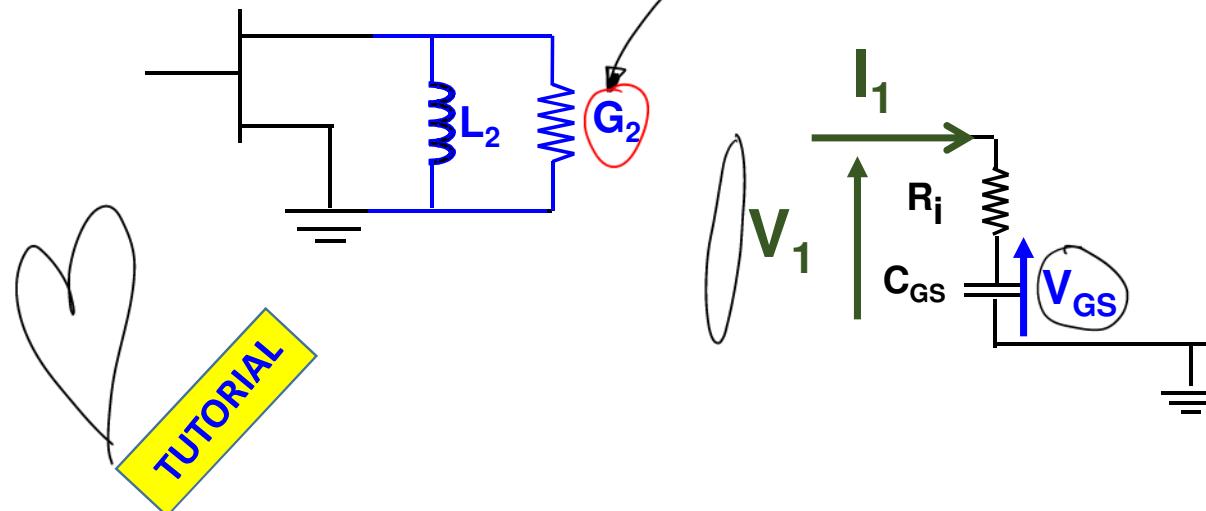
3) Maximum Power Gain G_{MAX} → Simplified Electrical Small-Signal FET Model



II – Intrinsic figures of merit for FETs

3) Maximum Power Gain G_{MAX} → Simplified Electrical Small-Signal FET Model

$$\textcircled{1} R_2 = R_{DS} \quad \text{or} \quad R_2 = R_{out} \textcircled{2}$$



General case ($G_2 \neq g_{DS}$) → Not maximum Power Gain G_P

$$P_{IN} = \frac{1}{2} \operatorname{Re} (V_1 I_1^*)$$

$$P_{OUT} = \frac{1}{2} \operatorname{Re} (V_{out-T} I_{out-T}^*)$$

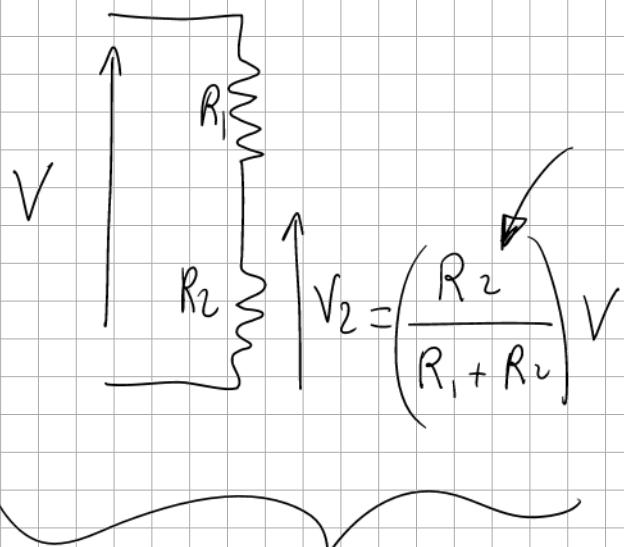
$$G_P = \frac{G_2}{[G_2 + g_{DS}]^2} \frac{g_m^2}{R_i C_{GS}^2 \omega^2}$$

Calculation of Input Power

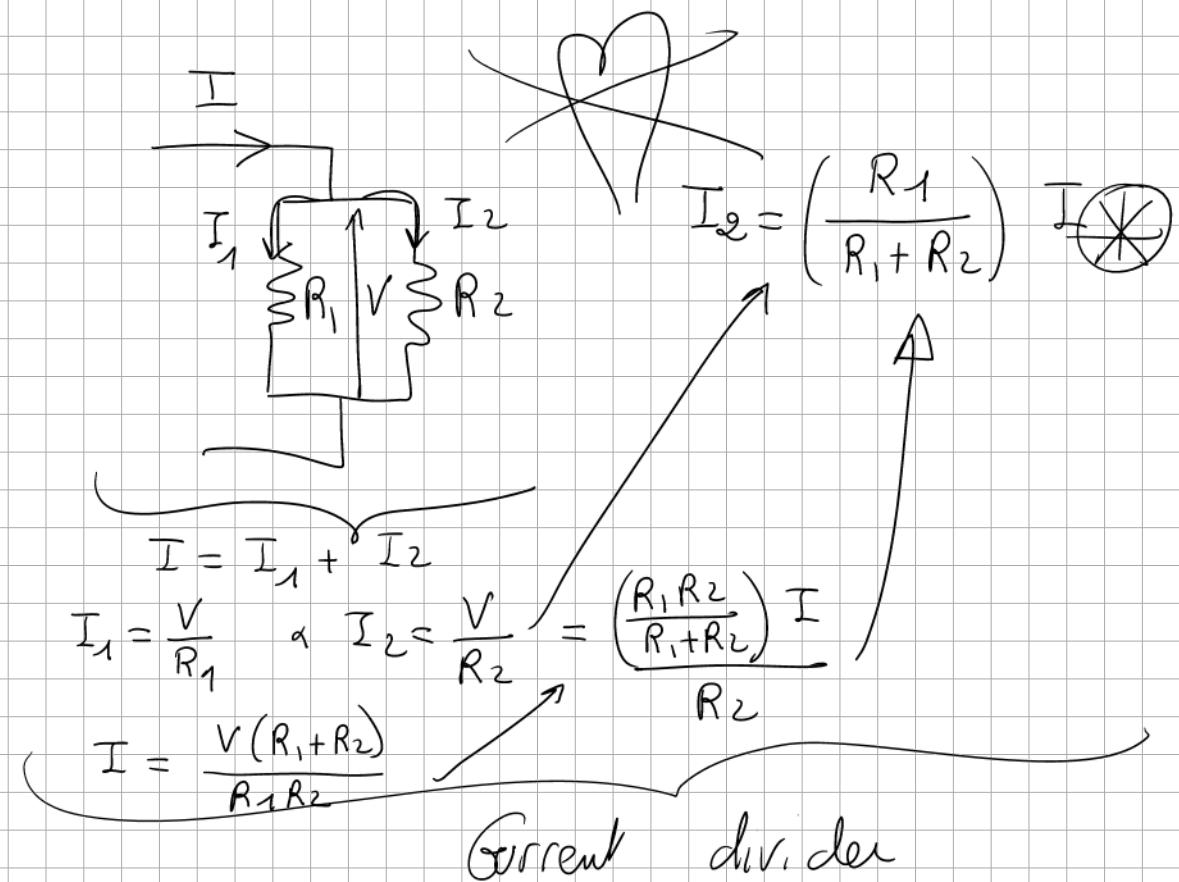
$$I_1 = j G_s \omega \times V_{GS}$$

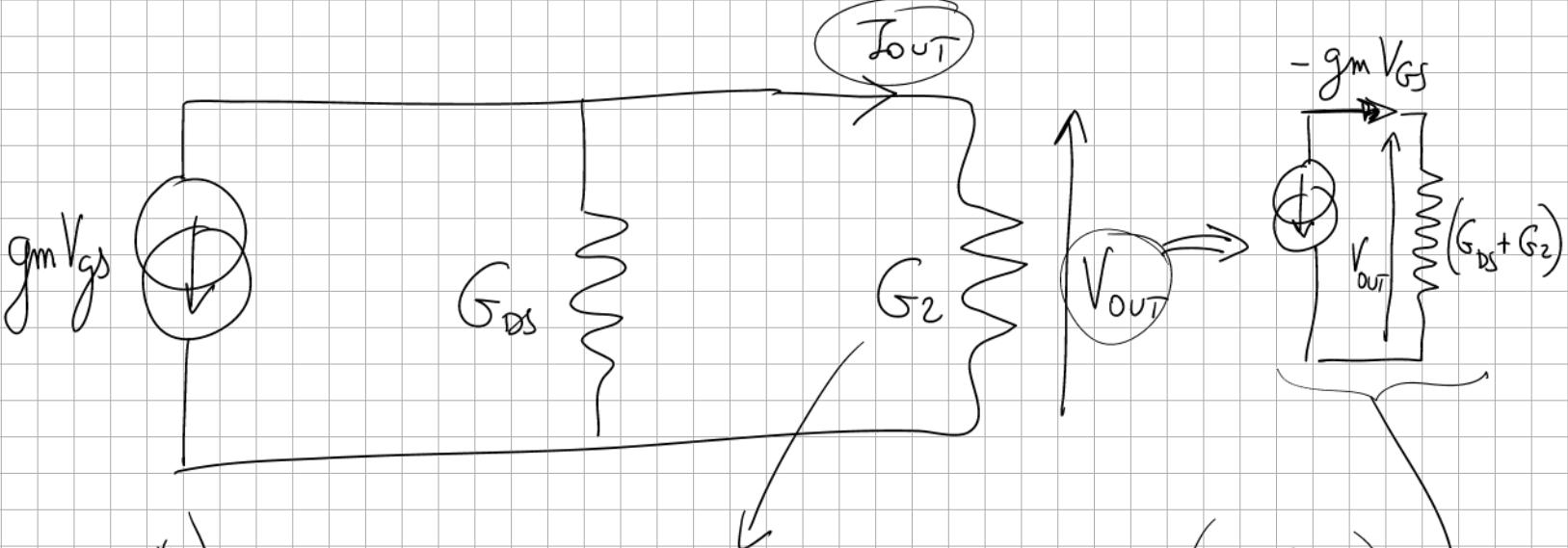
$$V_1 = \left(R_i + \frac{1}{j G_s \omega} \right) I_1$$

$$\begin{aligned} \operatorname{Re}(V_1 I_1^*) &= \operatorname{Re} \left[\left(R_i + \frac{1}{j G_s \omega} \right) \underbrace{I_1 I_1^*}_{|I_1|^2} \right] = |I_1|^2 \operatorname{Re} \left(R_i + \frac{1}{j G_s \omega} \right) \\ P_{IN} &= \frac{1}{2} R_i G_s^2 \omega^2 |V_{GS}|^2 \end{aligned}$$



Voltage Div. der





$$P_{\text{out}} = \frac{1}{2} \operatorname{Re} (V_{\text{out}} I_{\text{out}}^*)$$

$$I_{\text{out}} = G_2 V_{\text{out}}$$

$$V_{\text{out}} = (V_{\text{gs}})$$

$$= \frac{1}{2} \operatorname{Re} (V_{\text{out}} (G_2 V_{\text{out}})^*)$$

$$= \frac{1}{2} \operatorname{Re} \left(V_{\text{out}} V_{\text{out}}^* \underbrace{|V_{\text{out}}|^2}_{G_2} \right)$$

$$V_{\text{out}} = \frac{-g_m V_{\text{gs}}}{G_2 + G_{\text{DS}}}$$

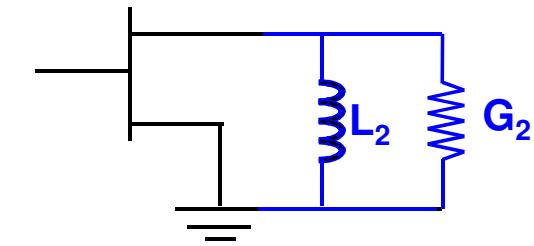
$$P_{\text{out}}$$

$$= \frac{1}{2} G_2 |V_{\text{out}}|^2 = \frac{1}{2} G_2$$

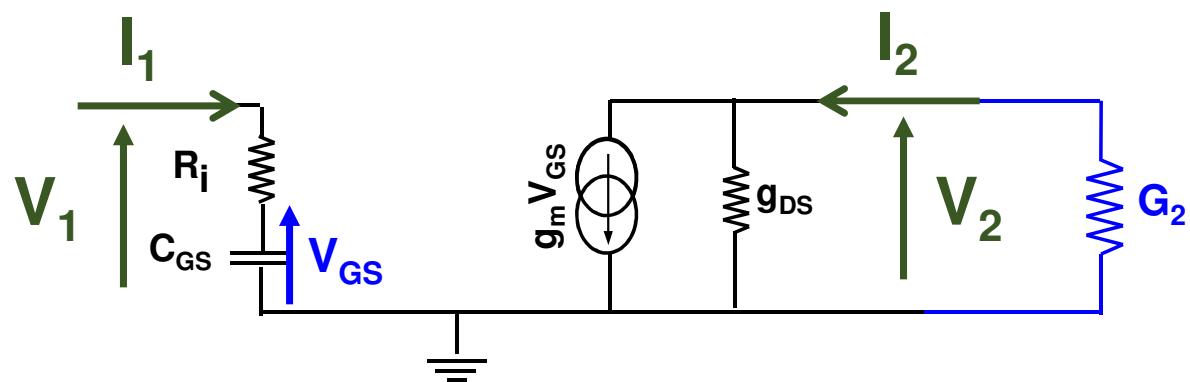
$$\left| \frac{-g_m V_{\text{gs}}}{G_2 + G_{\text{DS}}} \right|^2 = \frac{1}{2} \frac{G_2}{(G_2 + G_{\text{DS}})^2} g_m^2 |V_{\text{gs}}|^2$$

II – Intrinsic figures of merit for FETs

3) Maximum Power Gain G_{MAX} → Simplified Electrical Small-Signal FET Model

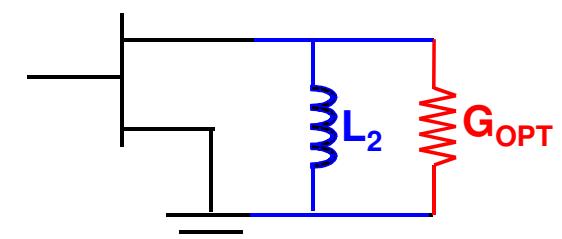
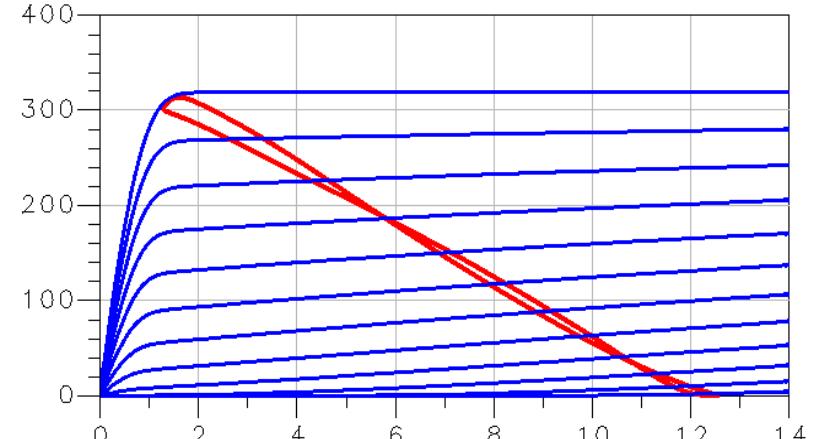
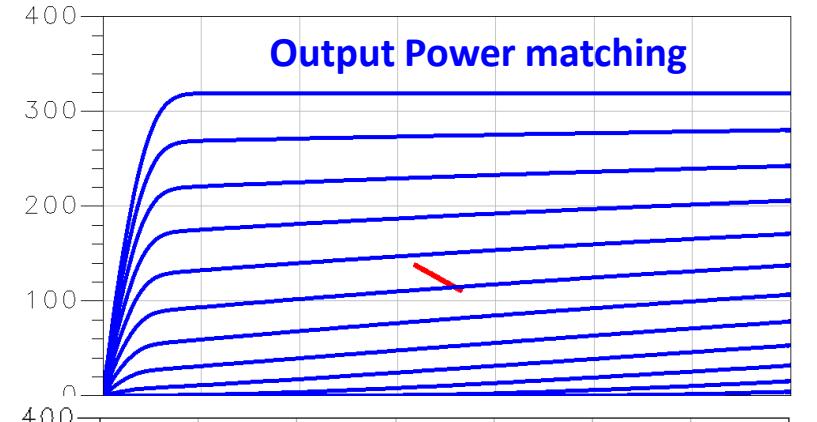
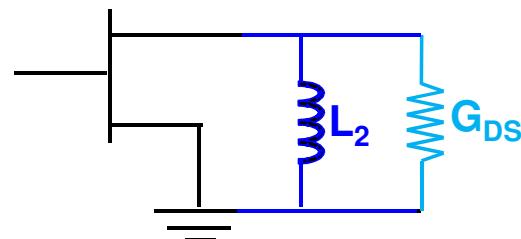
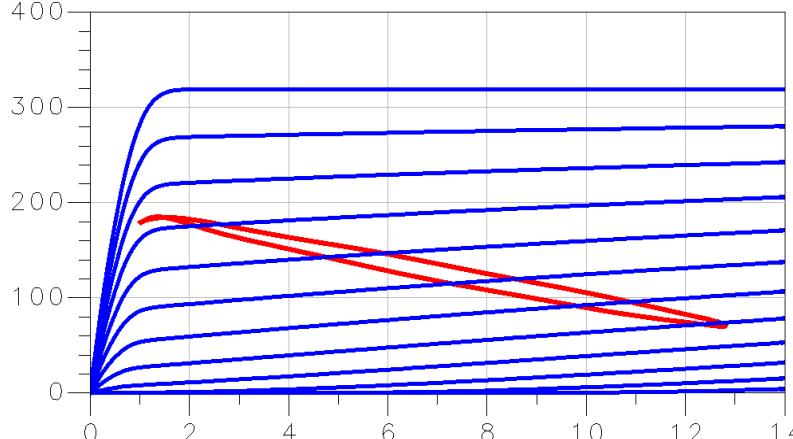
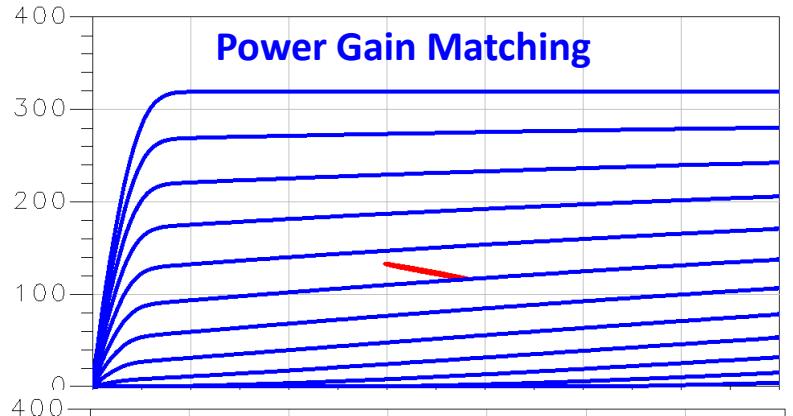


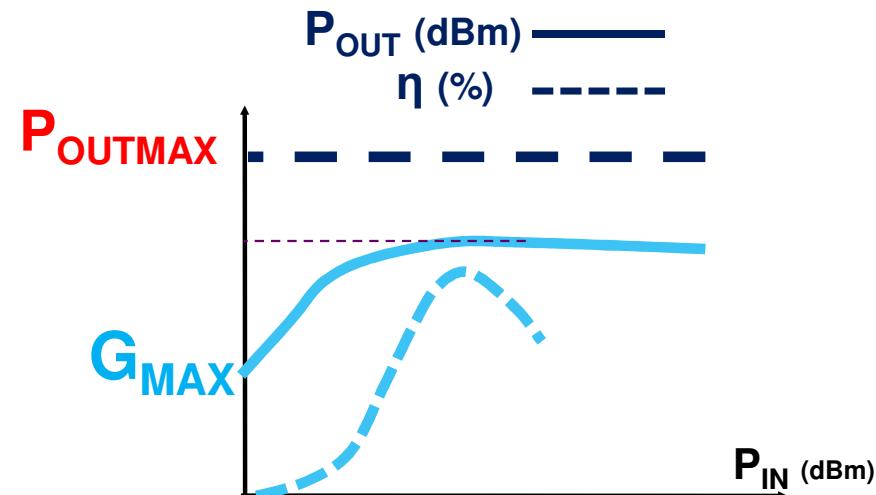
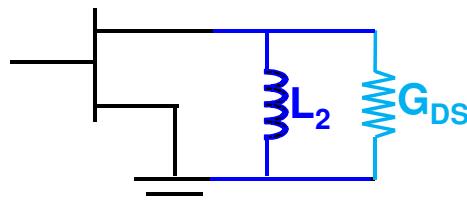
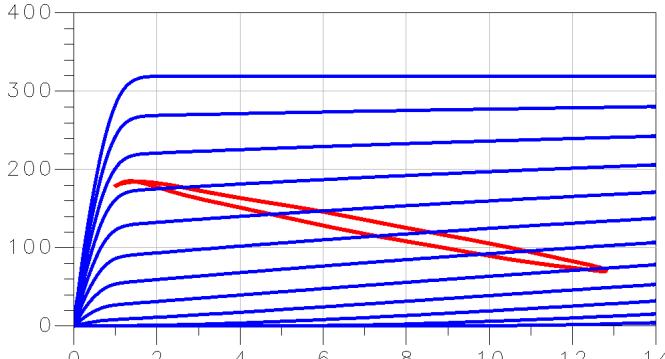
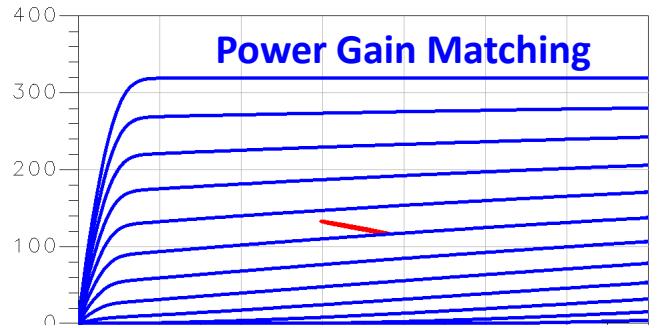
TUTORIAL

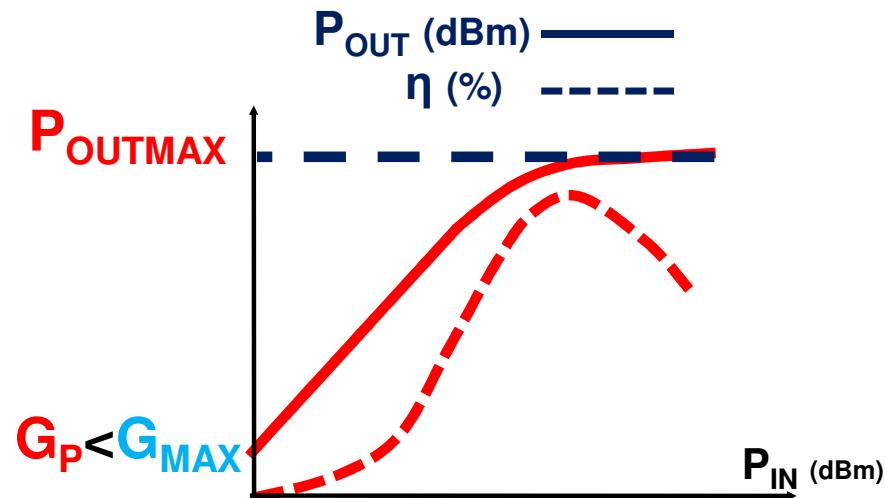
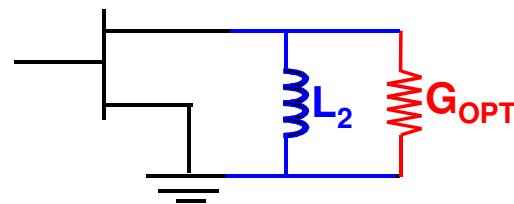
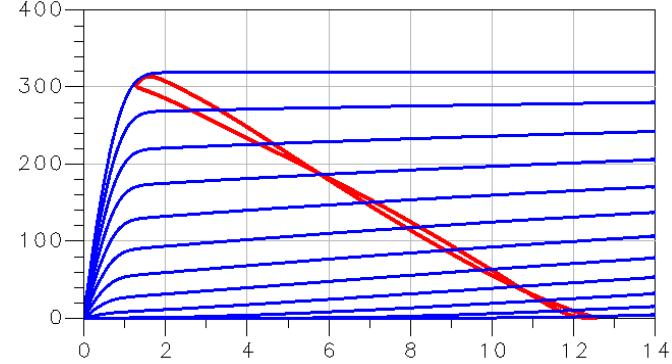
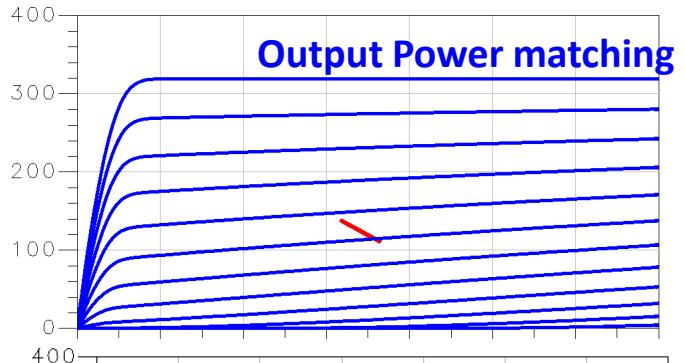


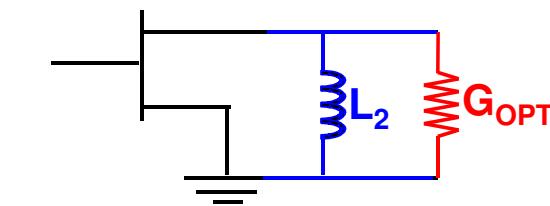
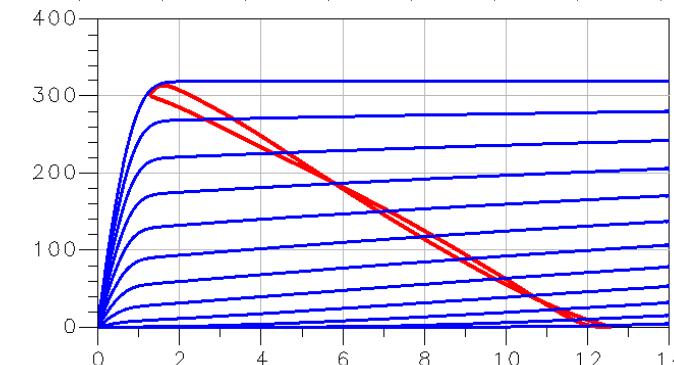
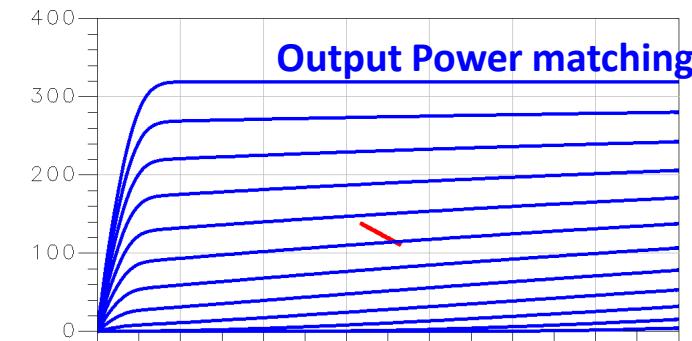
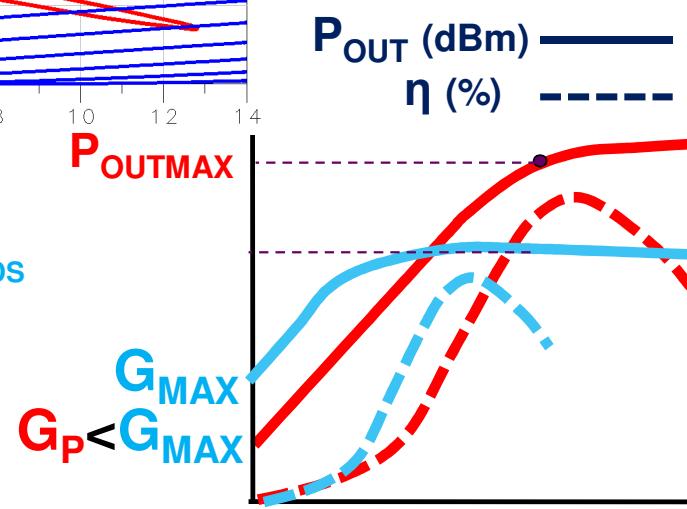
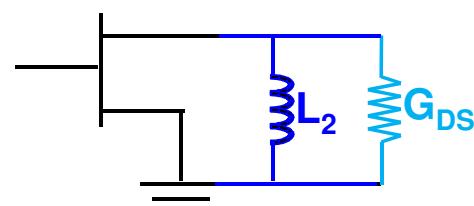
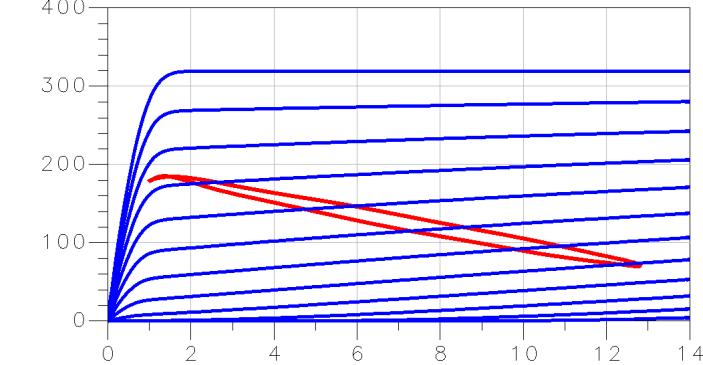
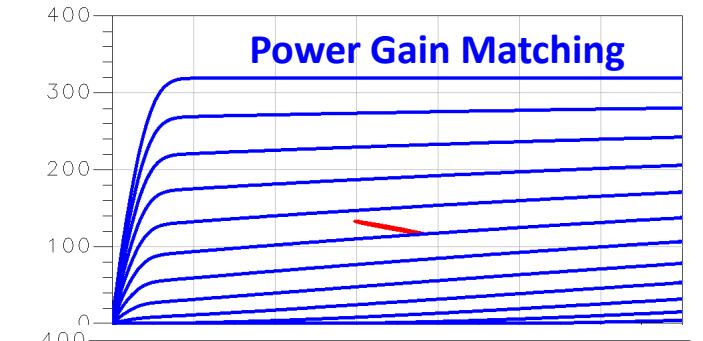
Optimum case ($G_2 = g_{DS}$) → Not maximum Power Gain G_{max}

$$G_{max} = \frac{g_m^2}{4 g_{DS} R_i C_{GS}^2 \omega^2}$$



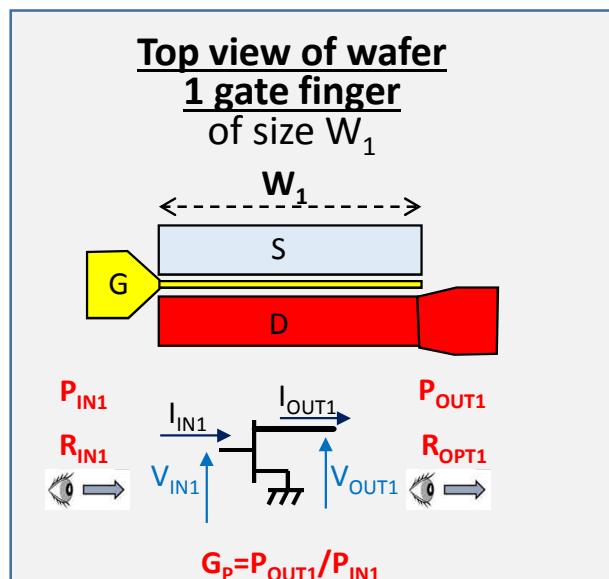






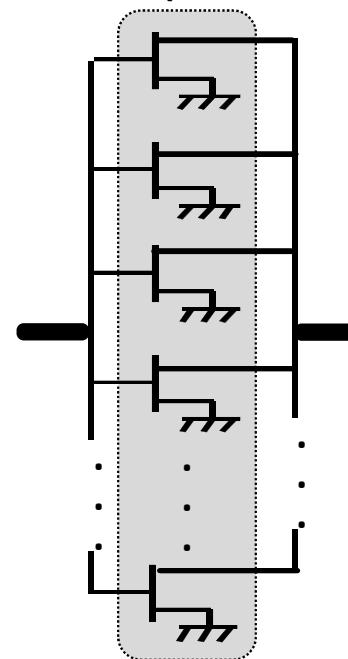
Power combination (Power Bars) and power matching

■ Illustration of critical issues in power matching

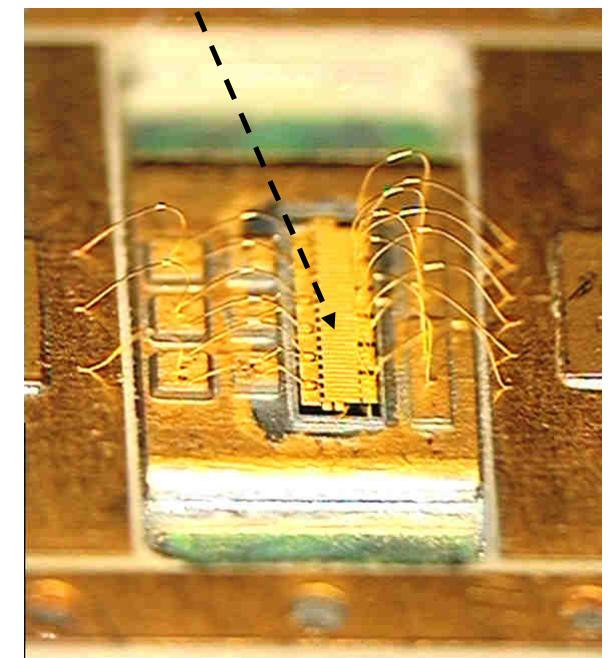


Increase device size to increase power

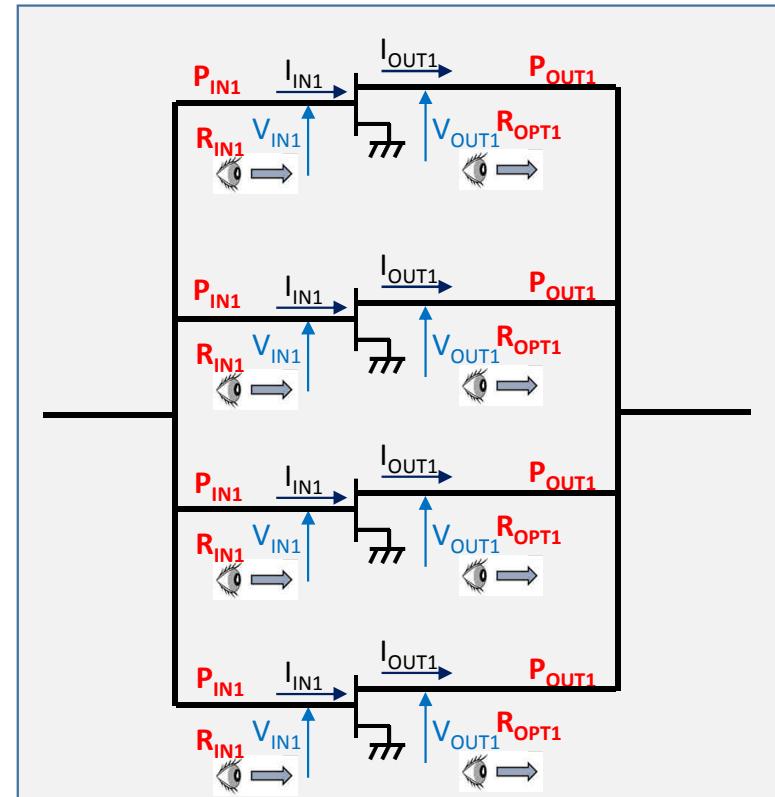
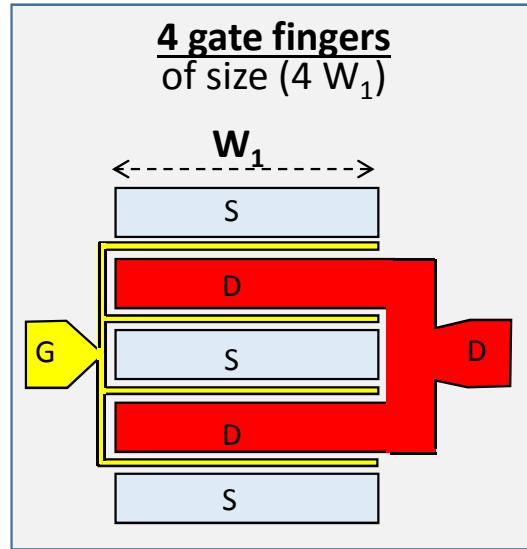
Power bar ($n //$ devices)



Power bar (matching in package)



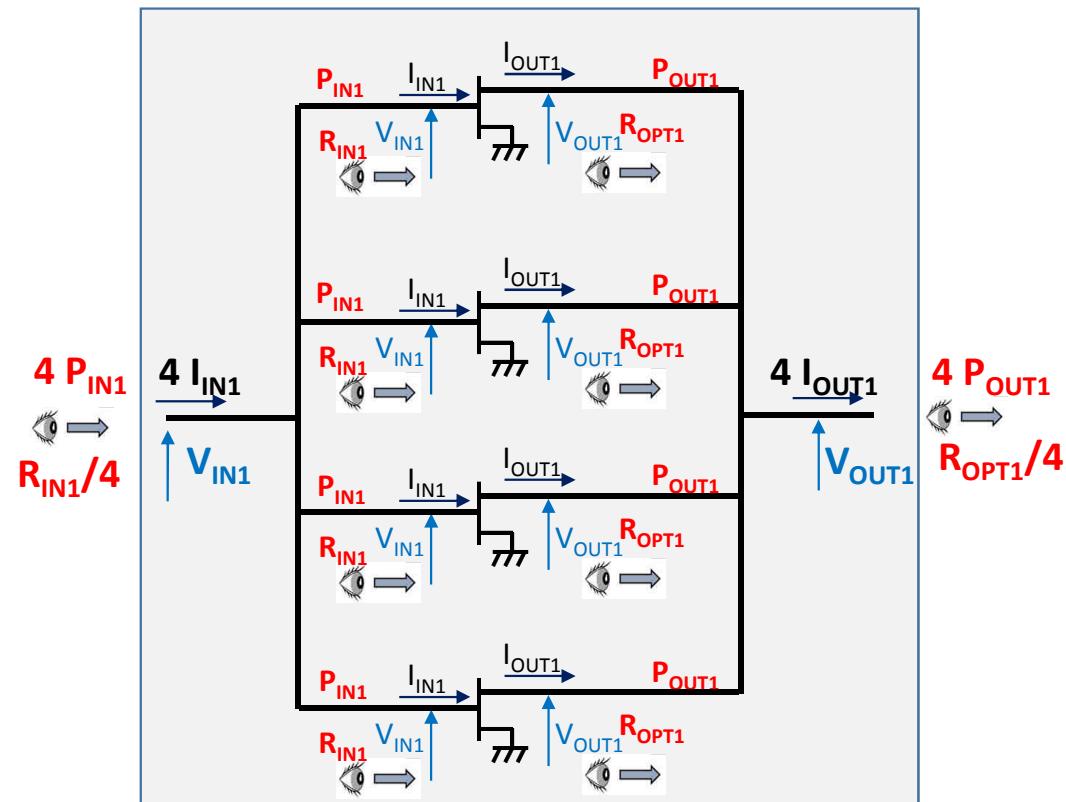
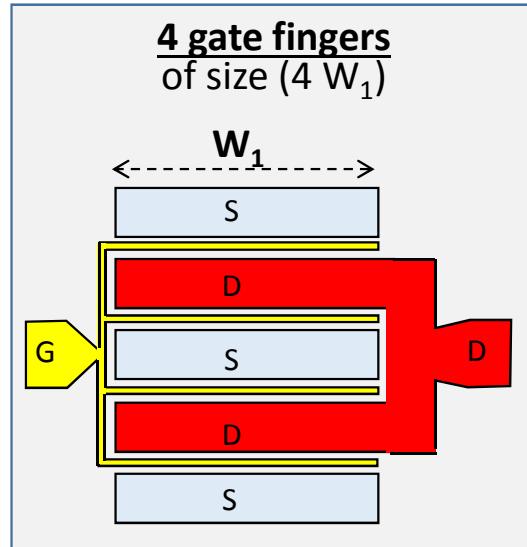
Power combination (Power Bars) and power matching

■ Illustration of critical issues in power matching

Device size = Total gate width = (N^o of // gates) \times (gate width) = $4 \times W_1$

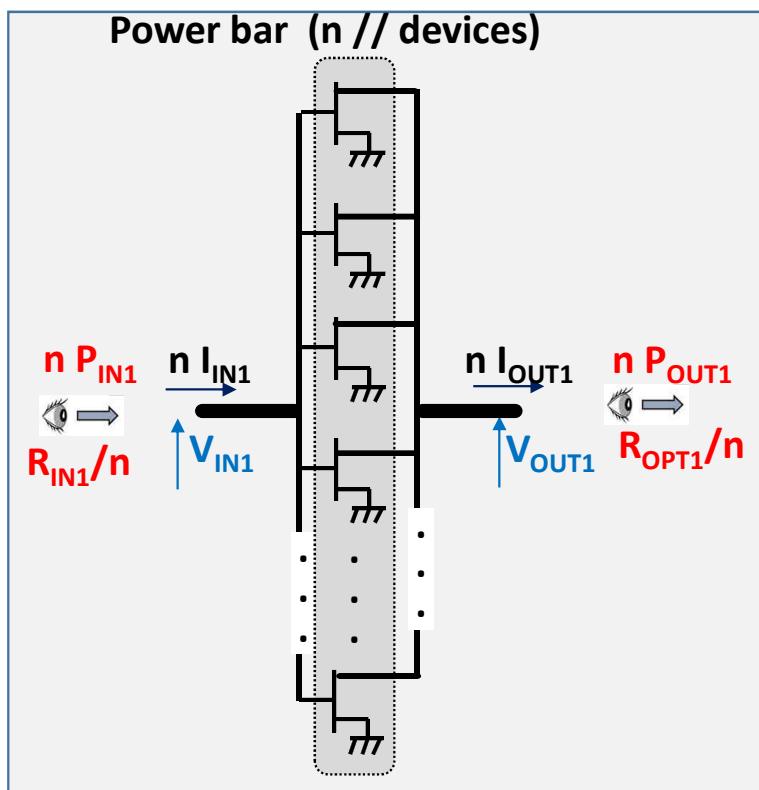
Power combination (Power Bars) and power matching

■ Illustration of critical issues in power matching

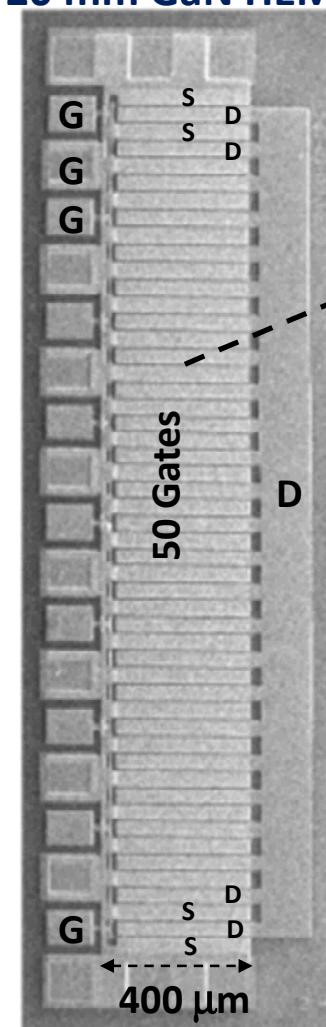


Power combination (Power Bars) and power matching

- Illustration of critical issues in power matching



20 mm GaN HEMT die



Device Size
 = Total Gate Width
 = (N^o of // gates) x (Gate width)
 = $50 \times 400 \mu\text{m} = 20 \text{ mm}$

Scaling Rules:

- Drain Current** I_{DS} (mA/mm)
- Voltages** V_{GS} and V_{DS} (V)
- Output Power** P_{OUT} (W/mm)
- Optimum Output Load** R_{OPT} ($\Omega \cdot \text{mm}$)

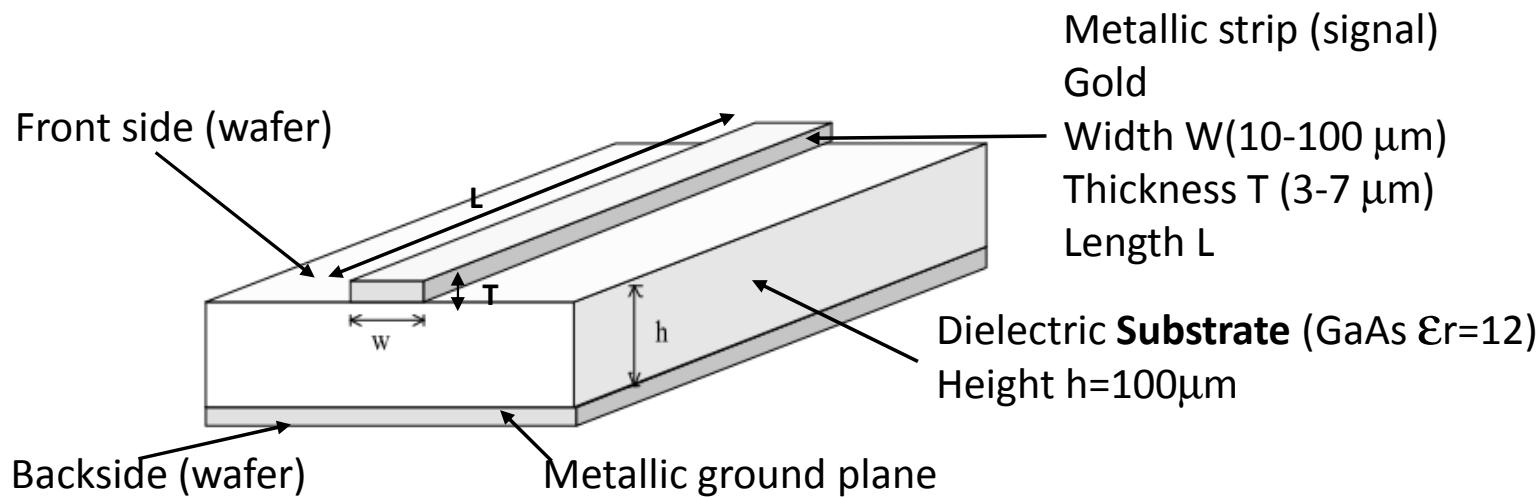


Main transmission lines and Passive elements used in MMIC designs

MMIC (Monolithic Microwave and Millimeterwave Integrated Technology)

- Recall on Transmission lines
- Microstrip inductors/capacitors/resistors
- Harmonic loading and bias using $\lambda/4$ lines
- Matrix chain of a line and impedance transformation

Microstrip lines



Metallic strip (signal)

Gold

Width $W(10-100 \mu\text{m})$

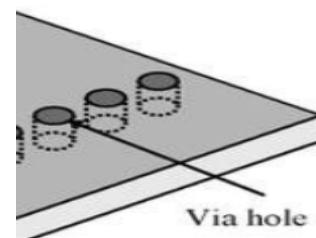
Thickness $T (3-7 \mu\text{m})$

Length L

Dielectric Substrate (GaAs $\epsilon_r=12$)

Height $h=100\mu\text{m}$

- Requirement of **metallized via holes** through the substrate to connect electrical elements from the front side to the metallic ground plane
 - expensive backside process after the front side process 😞
 - easier design of the signal paths on the front side when compared to coplanar
 - the most effective integrated technology at high frequencies 😊



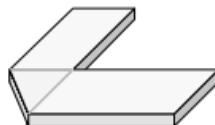
Microstrip lines

In order to drive the signal, these are some of the main shapes of line connections

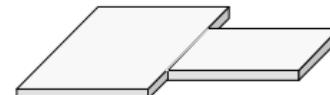
CORNER



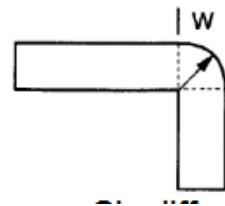
BEND



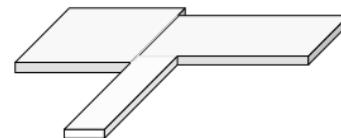
STEP (change of Z_c)



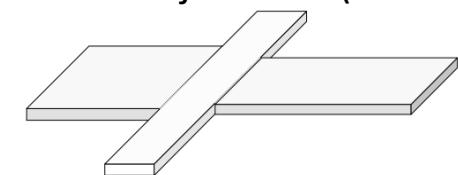
ROUND



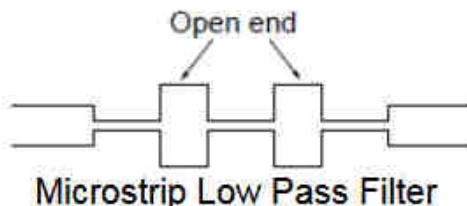
TEE junction (3 lines)



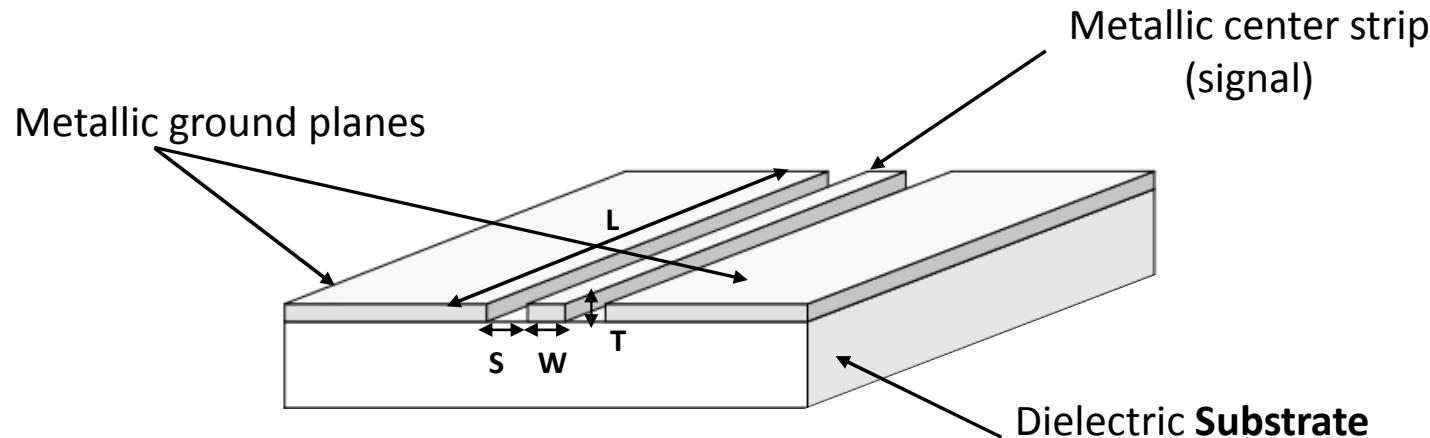
CROSS junction (4 lines)



In order to design passive circuits → Narrow Lines (Inductive) Wide Lines (Capacitive)



Coplanar lines



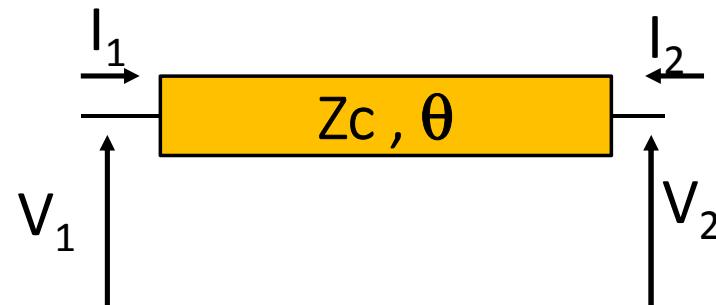
- No requirement of metallized via holes through the substrate to connect electrical elements from the front side to the metallic ground plane
 - no expensive backside process after the front side process 
 - complex design of the signal paths on the front side 
 - lower performances than microstrip designs 

Line = Matrix chain

Propagation constant $\Gamma = \alpha + j \beta \rightarrow$ Attenuation constant α and Phase constant β

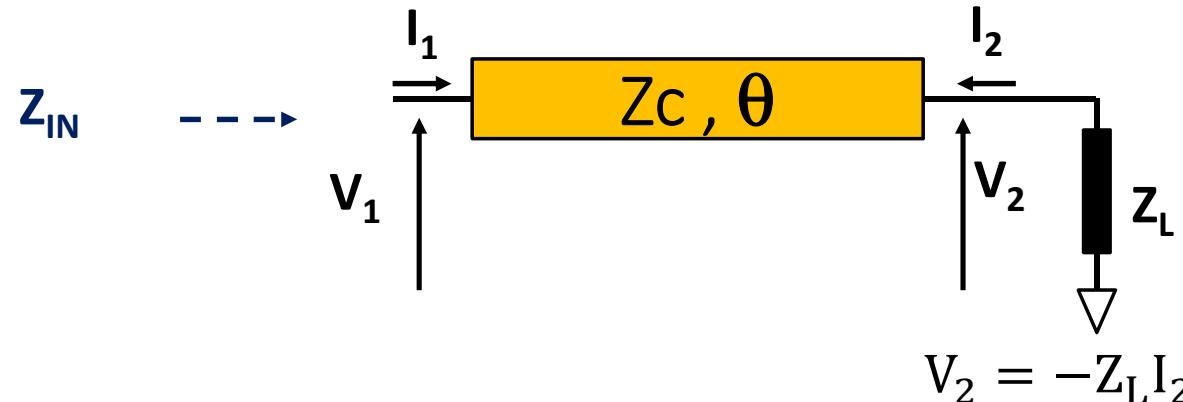
$$\beta = 2\pi/\lambda$$

$$\theta = \beta L$$



$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_C \sin(\theta) \\ j \sin(\theta)/Z_C & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

Equivalent input impedance of a loaded line



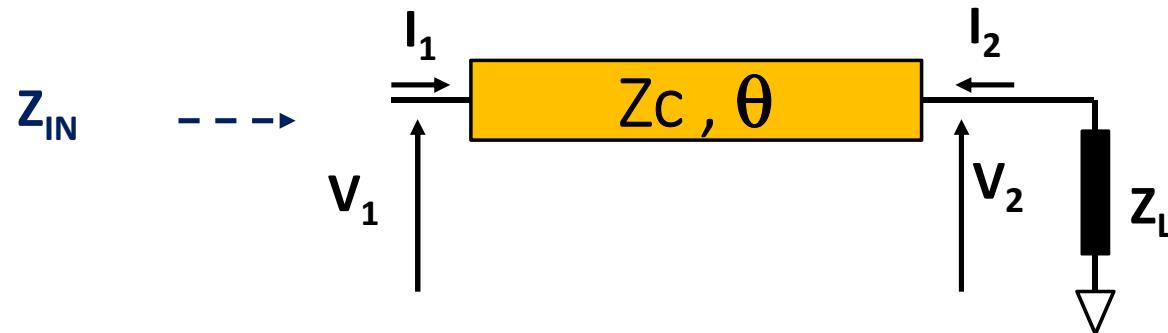
$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_C \sin(\theta) \\ j\sin(\theta)/Z_C & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

$$Z_{IN} = \frac{V_1}{I_1} = \frac{\cos(\theta) V_2 - jZ_C \sin(\theta) I_2}{\left(\frac{j\sin(\theta)}{Z_C}\right) V_2 - \cos(\theta) I_2} = \frac{\cos(\theta) (-Z_L I_2) - jZ_C \sin(\theta) I_2}{\left(\frac{j\sin(\theta)}{Z_C}\right) (-Z_L I_2) - \cos(\theta) I_2}$$

$$Z_{IN} = \frac{\cos(\theta) (Z_L) + jZ_C \sin(\theta)}{\left(\frac{j\sin(\theta)}{Z_C}\right) (Z_L) + \cos(\theta)} = Z_C \frac{Z_L \cos(\theta) + jZ_C \sin(\theta)}{jZ_L \sin(\theta) + Z_C \cos(\theta)}$$



Equivalent input impedance of $\lambda/4$ and $\lambda/2$ loaded lines



$$Z_{IN} = Z_C \frac{Z_L \cos(\theta) + j Z_C \sin(\theta)}{j Z_L \sin(\theta) + Z_C \cos(\theta)}$$

if $L = \frac{\lambda}{4}$ $\rightarrow \theta = \frac{2\pi L}{\lambda} = \frac{\pi}{2} \rightarrow Z_{IN} = \frac{Z_C^2}{Z_L}$ Impedance inverter
 if $L = \frac{\lambda}{2}$ $\rightarrow \theta = \frac{2\pi L}{\lambda} = \pi \rightarrow Z_{IN} = Z_L$

High- and Low-impedance short lines (Inductive or capacitive)

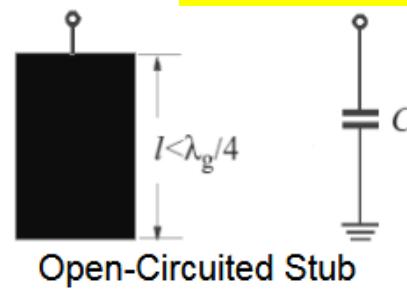


High-impedance short-line element and the Equivalent circuit

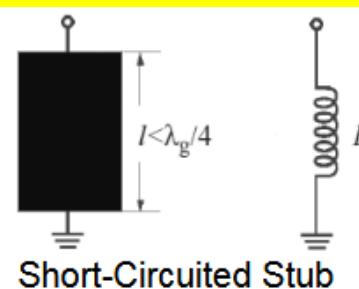


Low-impedance short-line element and the Equivalent circuit

Open and short-circuited stubs

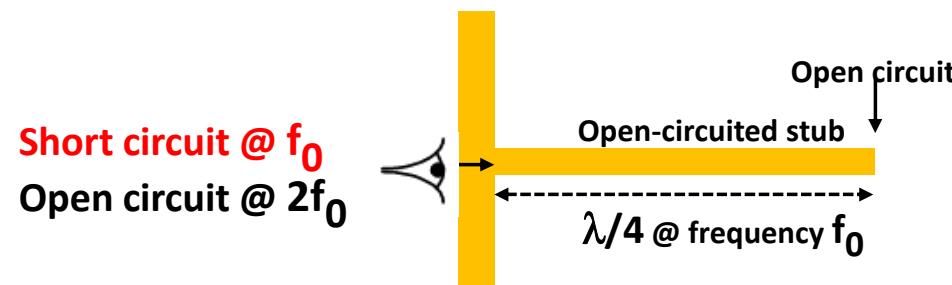
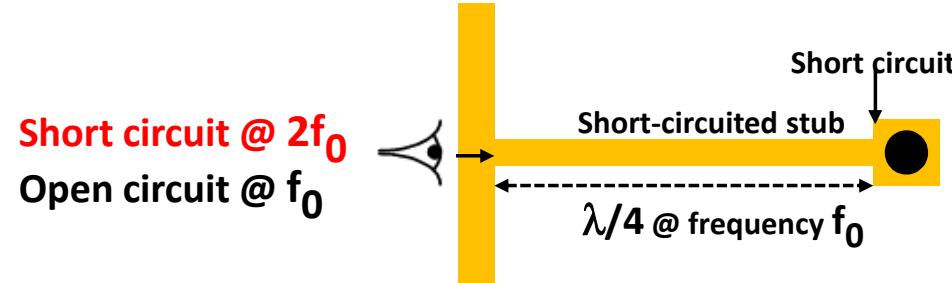


Open-Circuited Stub

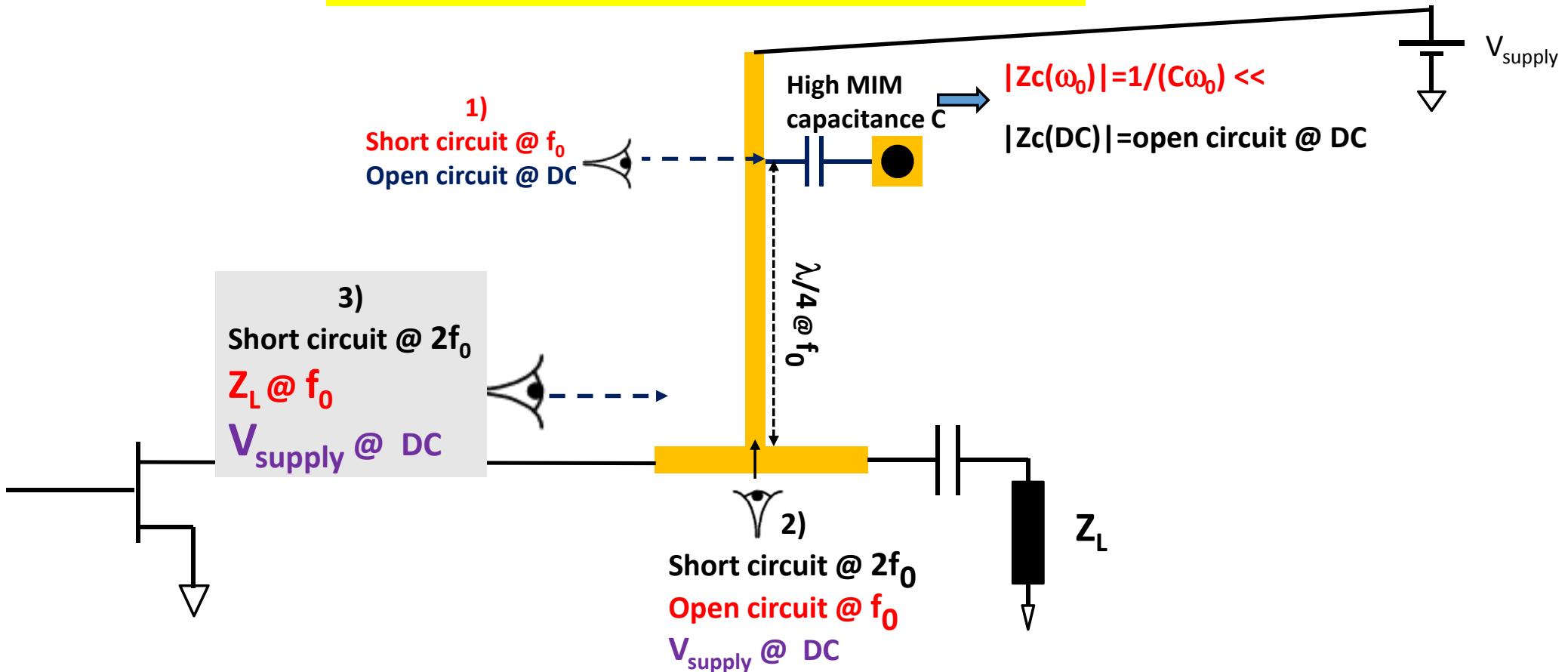


Short-Circuited Stub

Narrowband Harmonic loading using quarter wavelength line ($\lambda/4$)



Bias network decoupling using quarter wavelength line ($\lambda/4$)

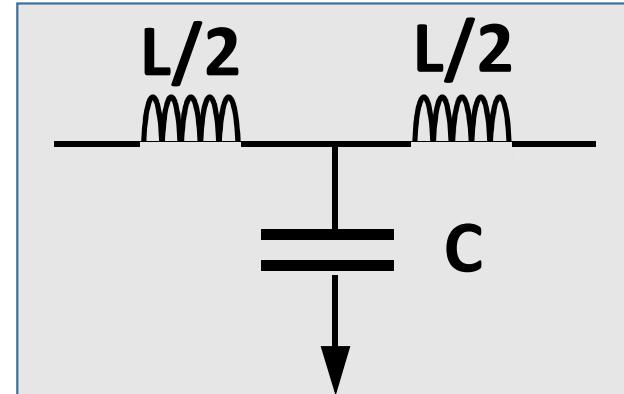


**Reminder = Electrical lumped equivalent (RLC)
of transmission lines**

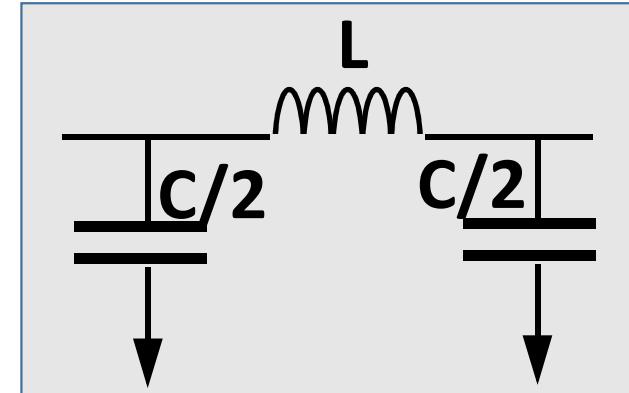
Electrical lumped equivalent (LC) of a lossless line (Z_c, θ)



T cell



π cell

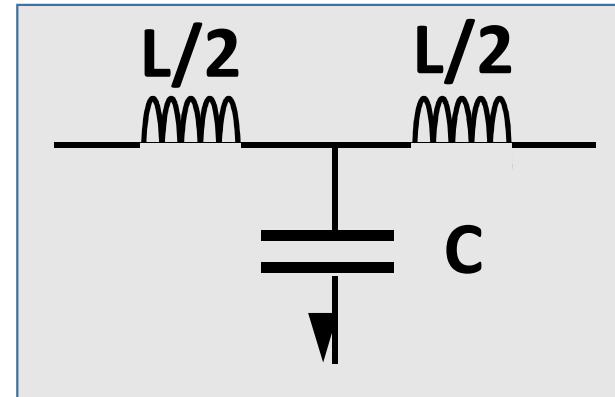


Electrical lumped equivalent (LC) of a lossless line (Z_c, θ)

Cut-off frequency

$$f_c = \frac{1}{\pi\sqrt{LC}}$$

T cell



Characteristic Impedance

$$Z_c = \sqrt{\frac{L}{C}} \sqrt{1 - \left[\frac{f}{f_c}\right]^2}$$

$$\sqrt{1 - \left[\frac{f}{f_c}\right]^2} > 0.9 \Leftrightarrow f < 0.44 f_c$$

Phase Shift

$$\theta = \omega\sqrt{LC} \sqrt{1 - \left[\frac{f}{f_c}\right]^2}$$

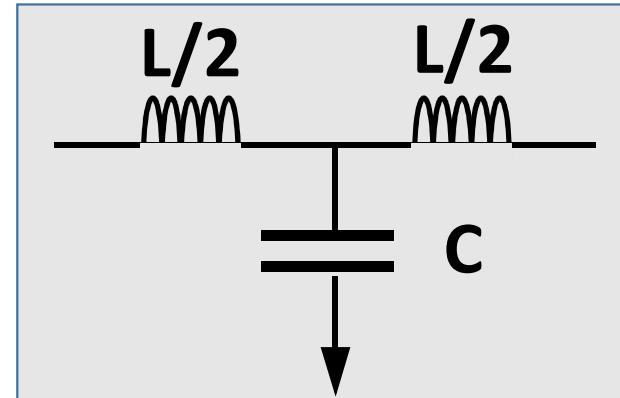
Electrical lumped equivalent (LC) of a lossless line (Z_c, θ)



Cut-off frequency

$$f_c = \frac{1}{\pi\sqrt{LC}}$$

T cell



Characteristic Impedance

If $f \ll f_c \rightarrow f < 0.44 f_c$

$$Z_c \approx \sqrt{\frac{L}{C}}$$

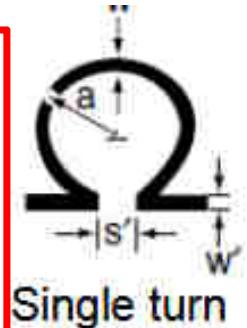
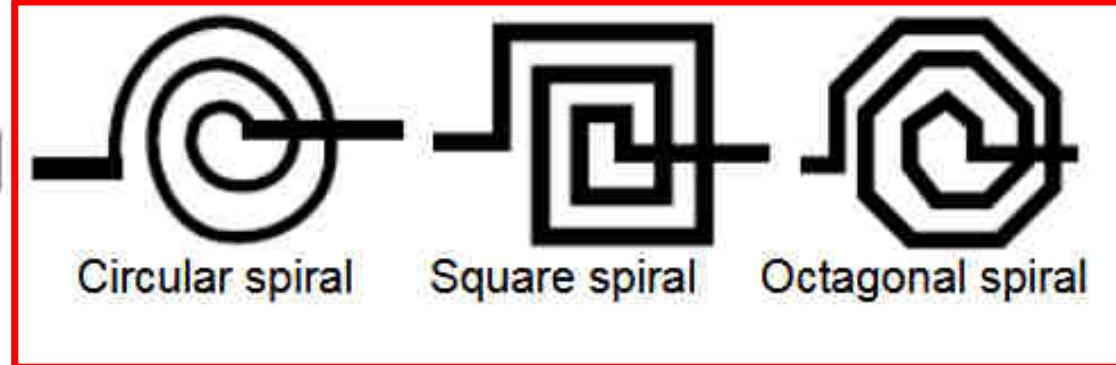
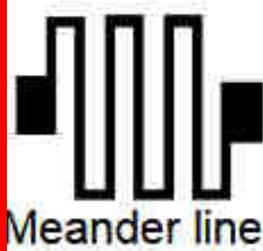
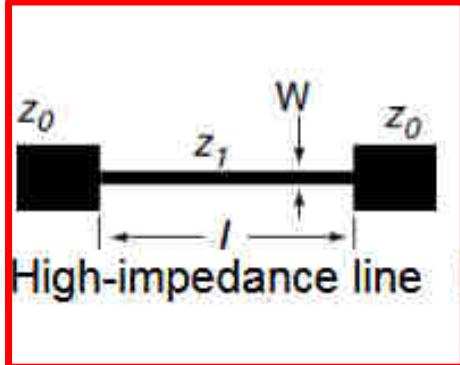
Phase Shift

$$\text{If } f \ll f_c \rightarrow \theta \approx \omega\sqrt{LC}$$



Microstrip passive inductors, capacitors and resistors

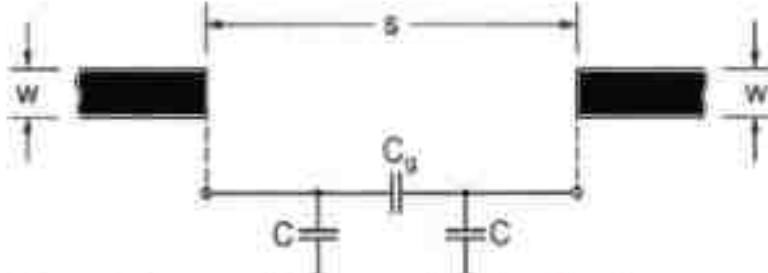
Microstrip Inductors



Only used at lower frequencies up to 3-4GHz because of very high losses
Achievable values up to few nH



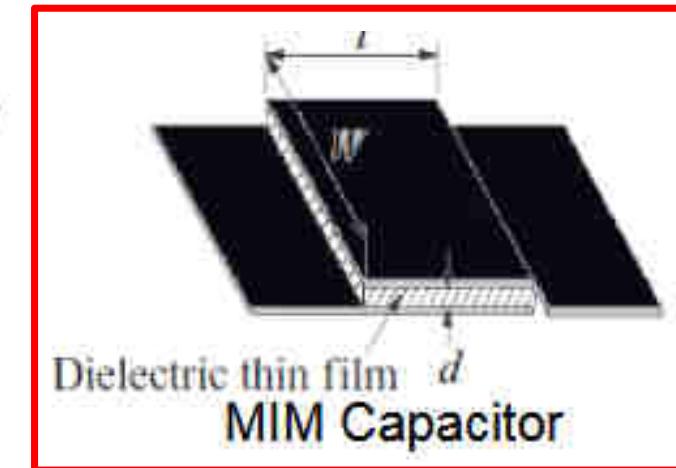
Microstrip Capacitors (MIM : Metal Insulator Metal)



Gap Capacitor and Equivalency



Interdigital Capacitor SiO_2



Dielectric thin film d
MIM Capacitor

$$CD = \frac{\epsilon}{d}$$

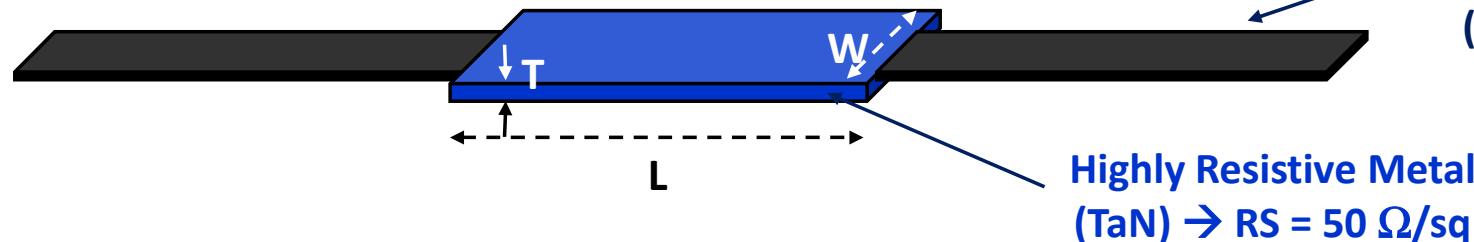
Capacitance density (F/m^2)
 Ex : $300 \text{ pF/mm}^2 \rightarrow$ Achievable values $0.2\text{pF} \rightarrow 20\text{pF}$

$$C = \epsilon \frac{S}{d} = \epsilon \frac{l \times W}{d}$$

$$C = \frac{\epsilon}{d} (l \times W)$$

$$C = CD \times S$$

Microstrip Resistors (TaN)



$$R = \rho_{\text{TaN}} \frac{L}{S} = \rho_{\text{TaN}} \frac{L}{T \times W}$$

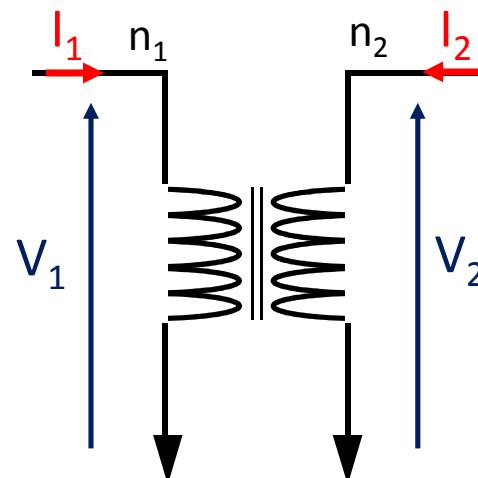
$$R = \frac{\rho_{\text{TaN}}}{T} \frac{L}{W} = R_S \frac{L}{W}$$

$$R_S = \frac{\rho_{\text{TaN}}}{T}$$

$$R = R_S \frac{L}{W}$$

Sheet resistance $R_S (\Omega/\text{sq})$
 $(\Omega/\text{ })$

Reminder = Ideal Electrical transformers How are they realized at high frequencies ?



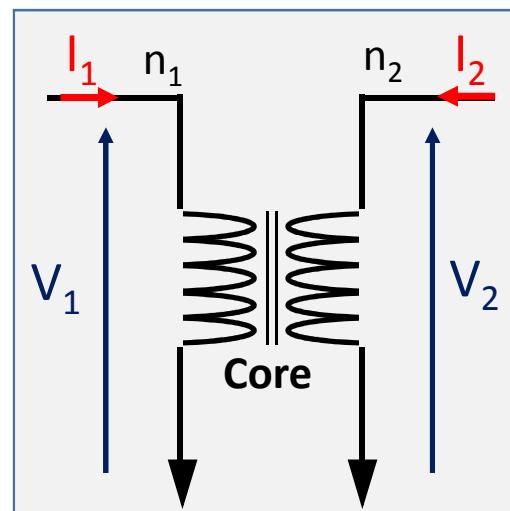
Reminder = Ideal Electrical transformer

$$\frac{V_2}{V_1} = \frac{n_2}{n_1}$$

$$\frac{I_2}{I_1} = -\frac{n_1}{n_2}$$

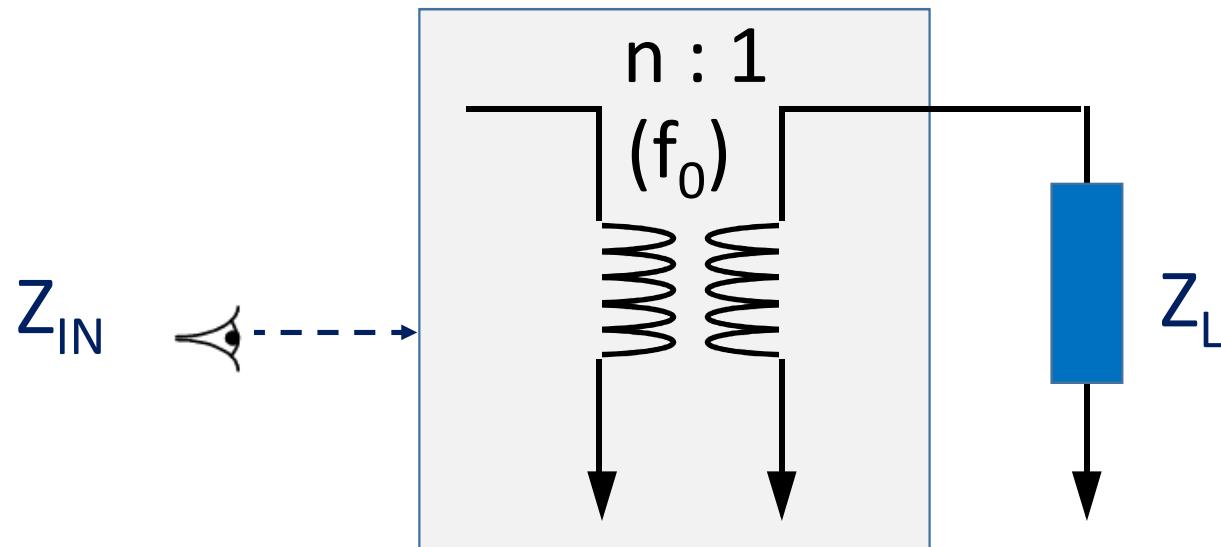
Conservation of energy

Primary Winding
(n_1 turns)



Secondary Winding
(n_2 turns)

Reminder = Impedance transformation



- Criterion
- Transformation ratio
 - Bandwidth
 - Technology

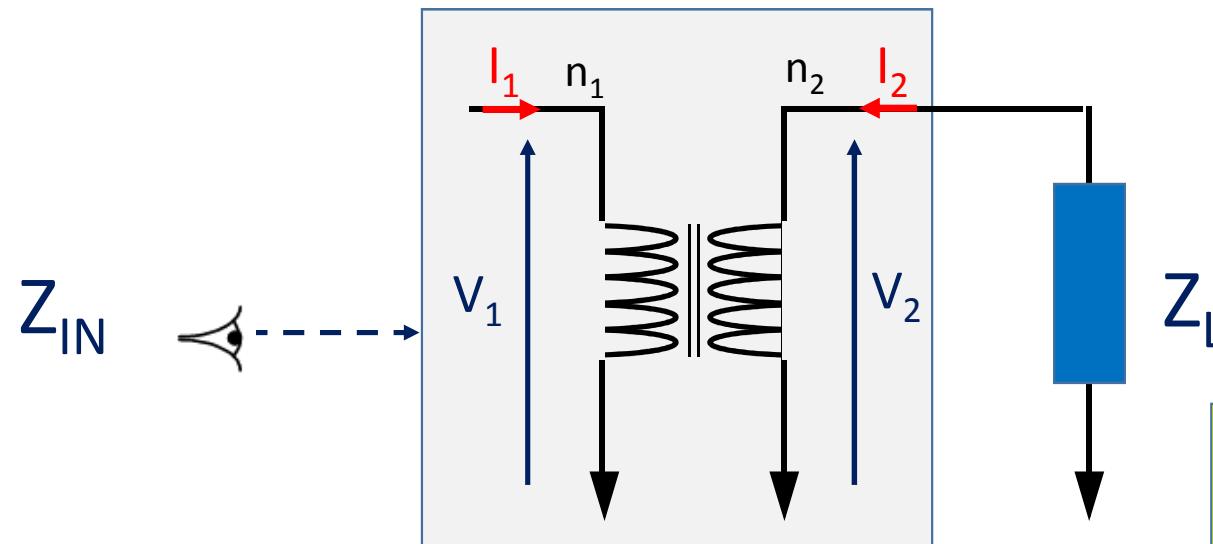
$$Z_{IN} = n^2 Z_L$$

$$n = \sqrt{\frac{Z_{IN}}{Z_L}}$$

Reminder = Impedance transformation

$$\frac{V_2}{V_1} = \frac{n_2}{n_1}$$

$$\frac{I_2}{I_1} = -\frac{n_1}{n_2}$$



$$Z_{IN} = \frac{V_1}{I_1} = \frac{V_1}{V_2} \frac{V_2}{I_2} \frac{I_2}{I_1} = \frac{n_1}{n_2} (-Z_L) \frac{-n_1}{n_2} = \left[\frac{n_1}{n_2} \right]^2 Z_L$$

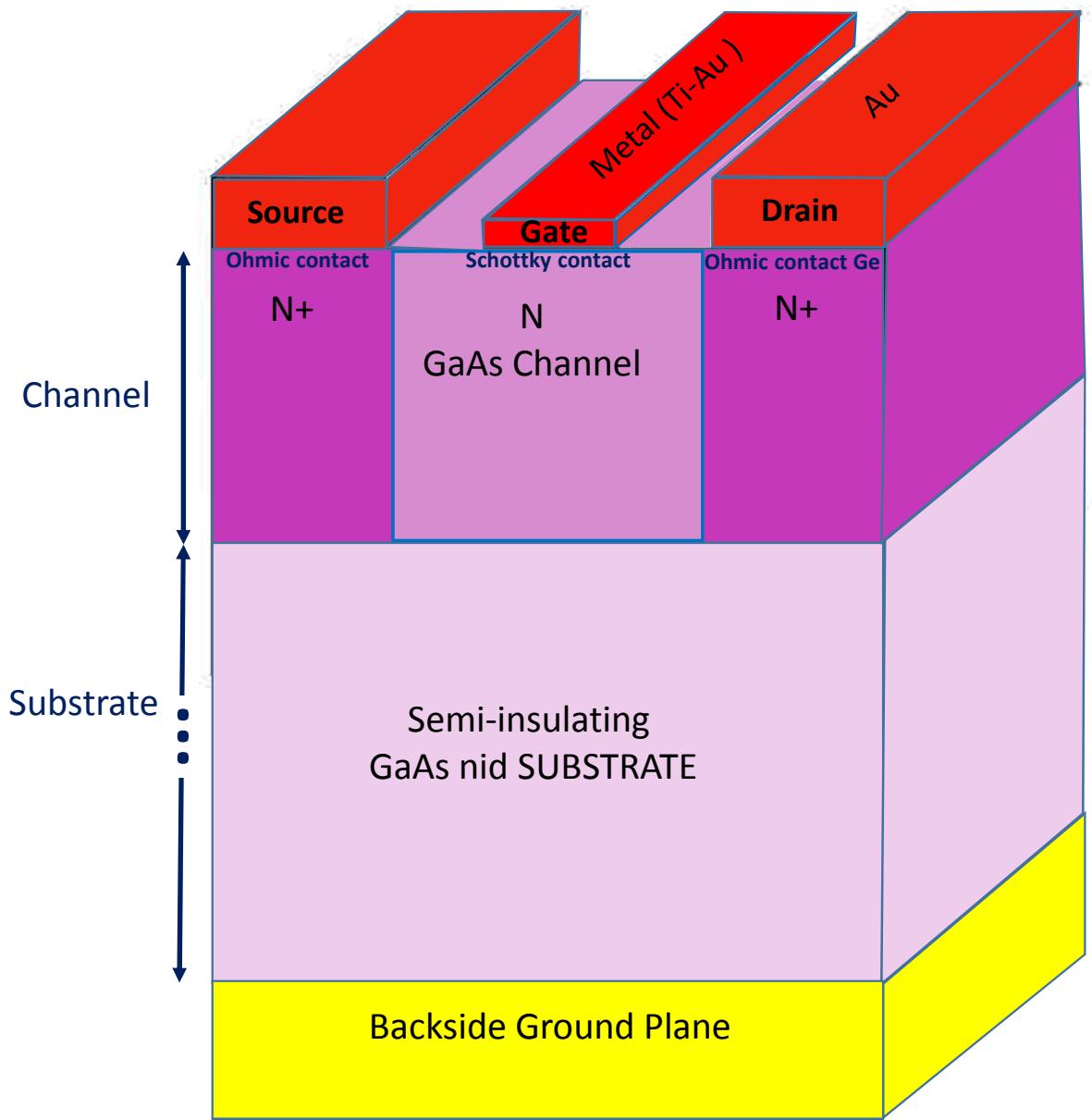
Load

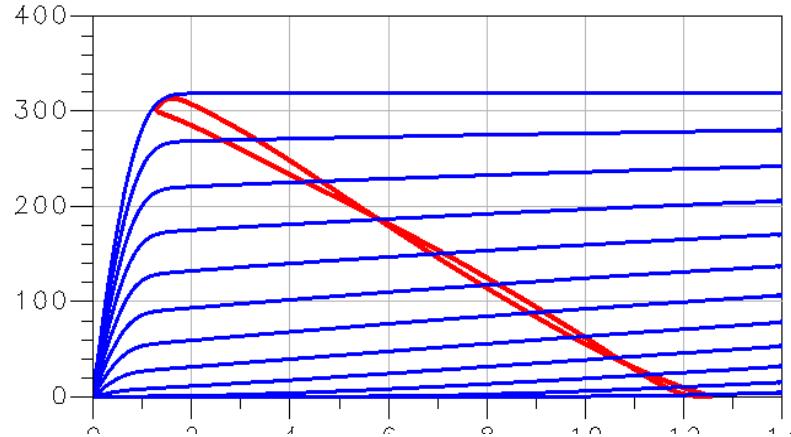
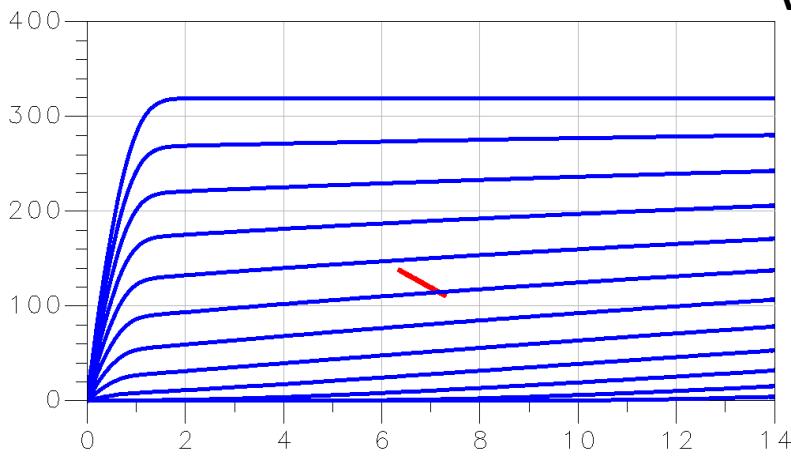
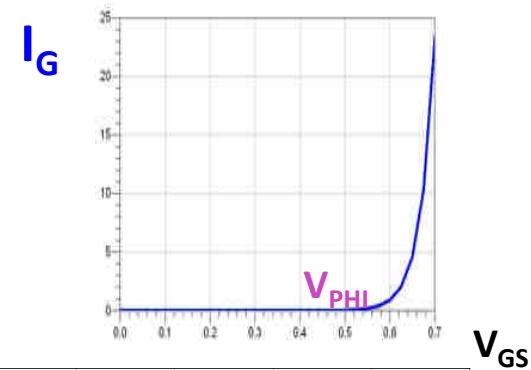
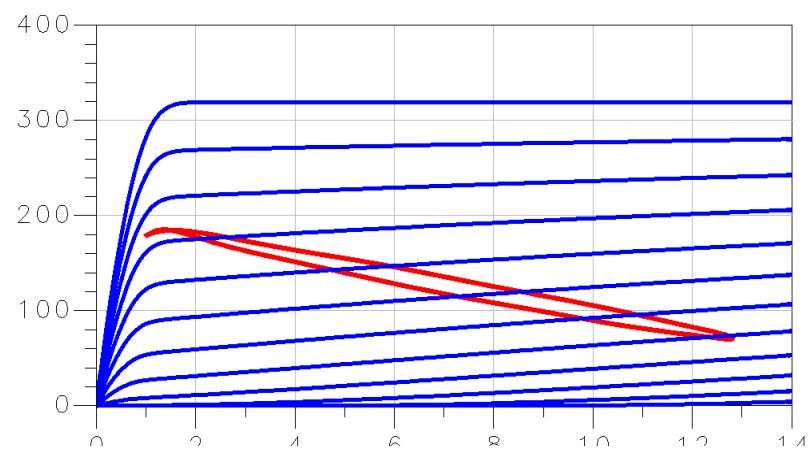
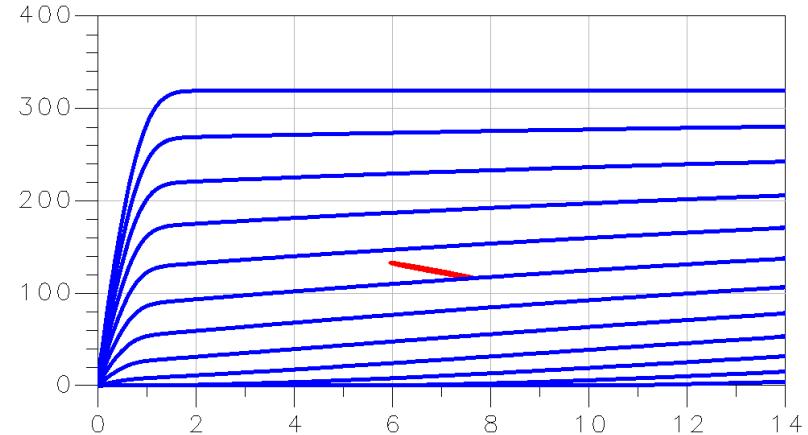
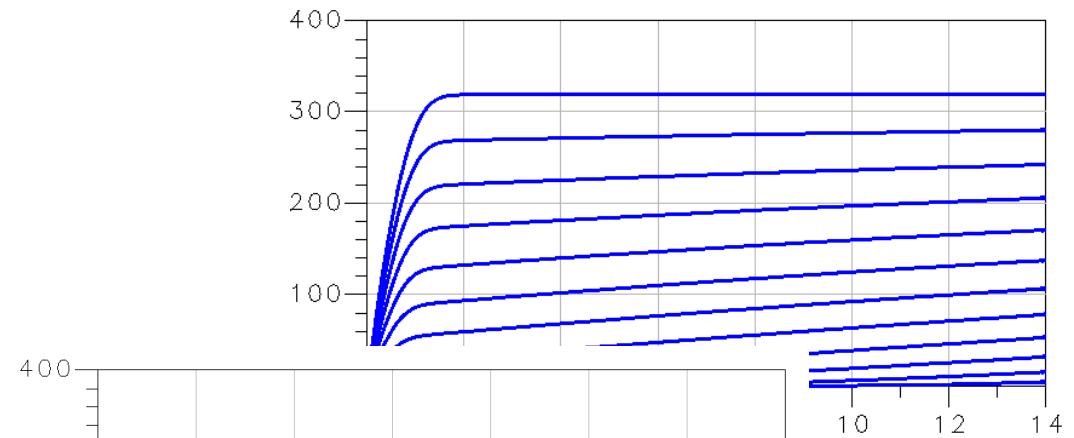
$$V_2 = -Z_L I_2$$

$$Z_{IN} = \left[\frac{n_1}{n_2} \right]^2 Z_L$$

$$n = \left[\frac{n_1}{n_2} \right] = \sqrt{\frac{Z_{IN}}{Z_L}}$$

Additional Slides





I – Basics of HEMT operation → Same Electrical Circuit Model

