

Semester S1

Basics of Active and Non-Linear Electronics

PRACTICAL WORK

PW3:

**LINEAR ADS ANALYSIS AND LINEAR
MEASUREMENTS OF A FET**

OUTLINE

I OBJECTIVE	3
II GENERAL INFORMATION ON MODELING TRANSISTORS	3
II.1 EQUIVALENT SMALL SIGNAL MODEL.....	4
II.1 NON LINEAR MODEL.	5
II.1.1 Measurement of the convective characteristics of the transistor.....	7
II.1.2 Measurement of pulsed I/V characteristics.....	7
III EXPERIMENTAL OPERATIONS.	9
III.1 MEASUREMENTS OF STATIC CHARACTERISTICS OF A FET	9
III.1.1 Theoretical information: characteristic networks.....	9
III.1.2 Manual Biasing of transistors.....	11
III.1.3 Automatic biasing of the FET using a LabVIEW software	13
III.1.4 Measurement of Output I/V Characteristics.	17
III.1.1 Measurement of Input I/V Characteristics.....	19
III.2 STATIC SIMULATION OF THE FET	21
III.2.1 Static Simulation of the extrinsic model of the FET.	23
III.2.1 Static Simulation of the intrinsic model of the FET.	27
III.3 S PARAMETER SIMULATION OF THE FET.....	28



LINEAR ADS ANALYSIS AND LINEAR MEASUREMENTS OF A FET

I OBJECTIVE

The goal of this PW is to work with Keysight's ADS (Advanced Design System) simulation software for transistor modelling. In this first PW, the fundamental knowledge will be acquired to begin the design of power amplifiers. The 2 parts of this PW are the following:

- The first part is devoted to the measurement of the static I/V characteristics of the final power amplifier to compare with the same characteristics given in the data sheet of the studied field effect transistor. From these characteristics, the main parameters of the current sources are calculated as the first parameters to introduce in the non-linear model of the transistor.
- The second part of the PW consists in simulating:
 - the extrinsic and intrinsic I/V characteristics of the transistor,
 - the S parameters by comparing the results obtained from the non-linear model.

II GENERAL INFORMATION ON MODELING TRANSISTORS.

The modelling of the transistors leads to the development of several models whose domain of validity is always verified using comparison with actual experimental characterizations. A model cannot represent EXACTLY the reality. It is only a mathematical expression which validity is associated to specific conditions.

The approach of an electrical equivalent model is based on the choice of an equivalent circuit topology, of a layout and the nature of the components used to obtain a simplified view of the involved physical phenomena. This approach is the most appropriate in terms of time, simulation, ease of parameterization and implementation in the current CAD tools.

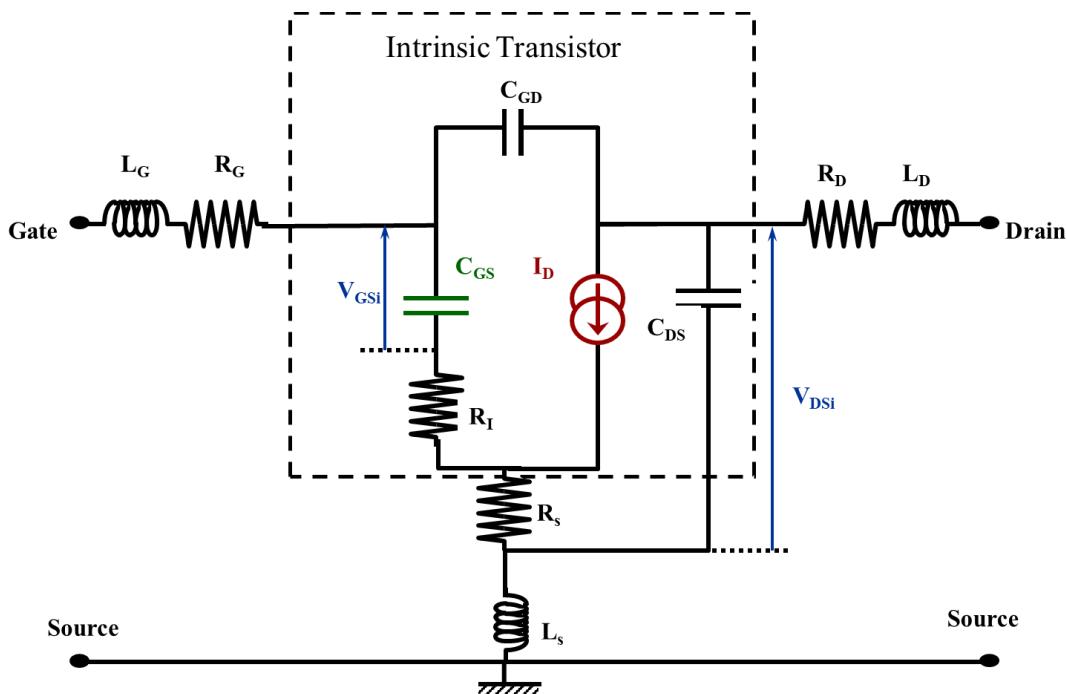
II.1 EQUIVALENT SMALL SIGNAL MODEL.

The method to extract the small signal equivalent model is based on a classic approach to implement a nonlinear transistor model into a simulator.

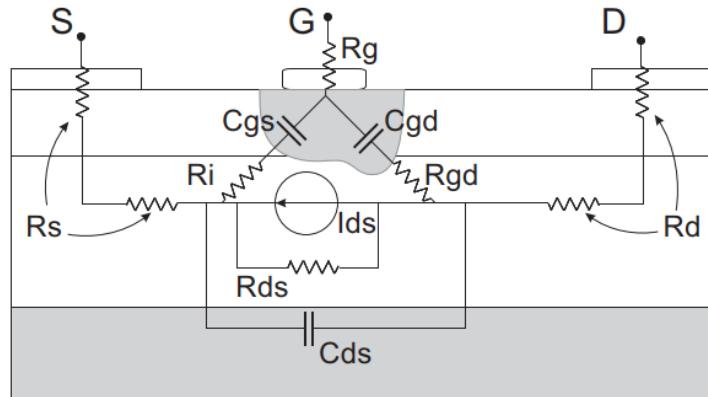
The intrinsic characteristics of transistors are of great interest to circuit designers. In addition, they must know the parasitic elements that actually exist around the transistors when they are integrated in a circuit. These elements are, for a FET, the metallization and access resistances to the channel and the gate as well as the inductance of the source

Despite the three-dimensional nature of distributed transistors, an equivalent circuit with localized differential elements (lumped components) can be proposed as a first approximation to simulate its behaviour. The values of the lumped components for a bias point are evaluated from the small signal microwave measurements made at and around this bias point. The advantages of this approach are as follows: the implementation of such a model is very easy in circuit simulators and designers are used to manipulate the transconductance, output conductance and capacitance values of these equivalent models. However, the validity of these small signal models has to be carefully verified because some elements of the circuit may lose their physical meaning. The extrapolations allowed by the different simulators must be carefully verified and known.

The conventional equivalent field effect transistor model of the following figure can be calculated from small microwave signal measurements:



This small signal differential model around a bias point contains 6 extrinsic elements (L_G , L_D , L_S , R_G , R_D , R_S) and 6 intrinsic elements (C_{GS} , C_{GD} , R_i , G_m , τ , C_{DS}). The following figure shows the origin of electrical components in the case of a representation of a MESFET [C. A. Leichti, “Microwave field effect transistors - 1976,” IEEE Transactions on Microwave Theory and Techniques, vol. 24, pp. 279–300, 1976]. The values of the different elements depend on the technological parameters and on the carrier profile in the component for a given bias point.



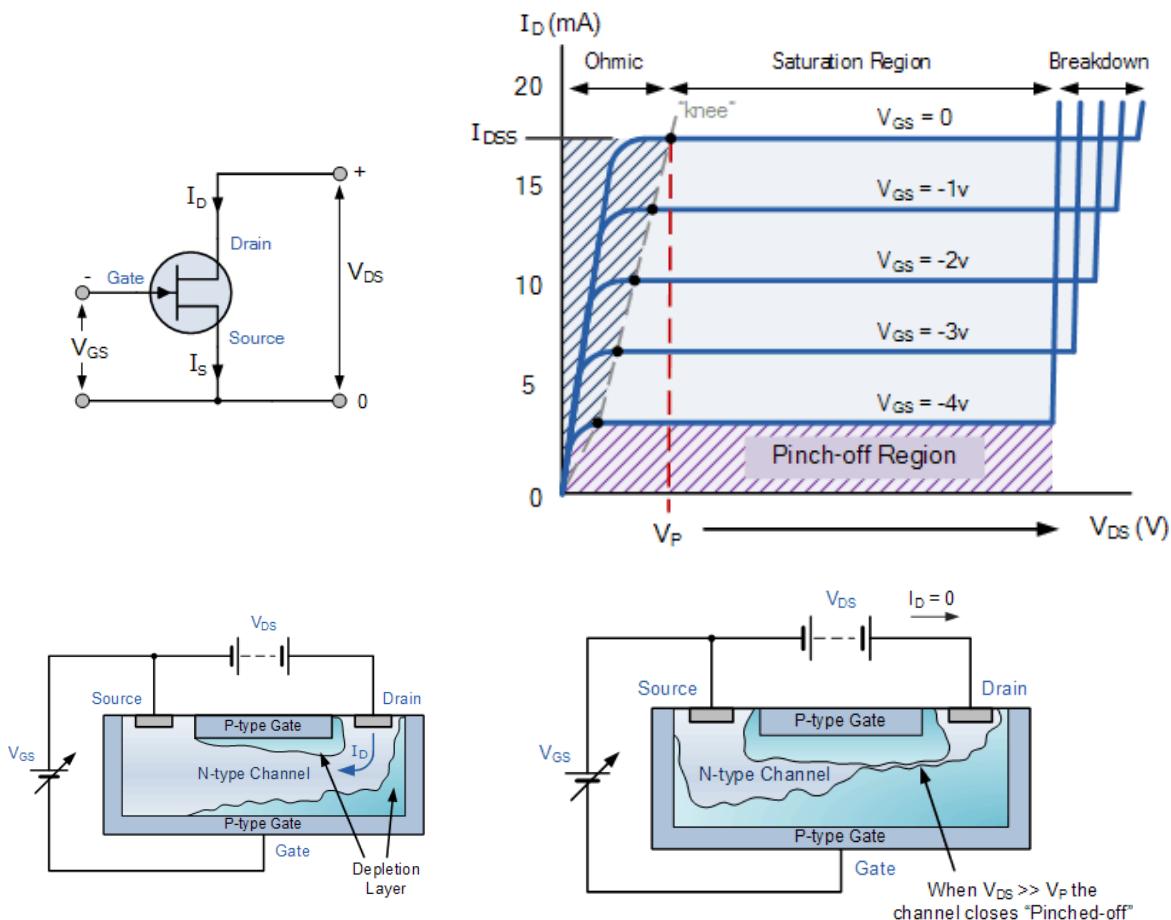
The voltage-controlled current source can then be expressed as:

$$I_D = f_{\text{linear}}[V_{gs}(t)] \Rightarrow I_D = g_m[V_{gs}(t - \tau)]$$

The small signal models obtained from the S parameters represent a linearization of the component for a bias point. Very good designs of microwave circuits have been made using such models for sufficient linear devices. Circuit simulators can efficiently process a transistor linear model, either from an extraction of its equivalent scheme, or from a small signal interpolation black box. For strongly non-linear circuit designs, it is necessary to characterize the intrinsic behaviour as a function of the applied voltage, and thus to integrate multi-bias measurements of S parameters.

II.1 NON LINEAR MODEL.

To obtain the most valid non linear model, it is necessary to characterize the transistor in the four regions defined in the following figure (ohmic, pinch-off or cut-off, saturation and breakdown zones):



The characteristics curves example shown above, shows the four different regions of operation for a FET and these are given as:

1. Ohmic Region – When $V_{GS} = 0$ the depletion layer of the channel is very small and the FET acts like a voltage-controlled resistor.
2. Cut-off Region – This is also known as the pinch-off region where the Gate voltage, V_{GS} is sufficient to cause the FET to act as an open circuit as the channel resistance is at maximum.
3. Saturation or Active Region – The FET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.
4. Breakdown Region – The voltage between the Drain and the Source, (V_{DS}) is high enough to cause the FET's resistive channel to break down and pass uncontrolled maximum current.

Two types of pulsed measurements enable reaching these four zones:

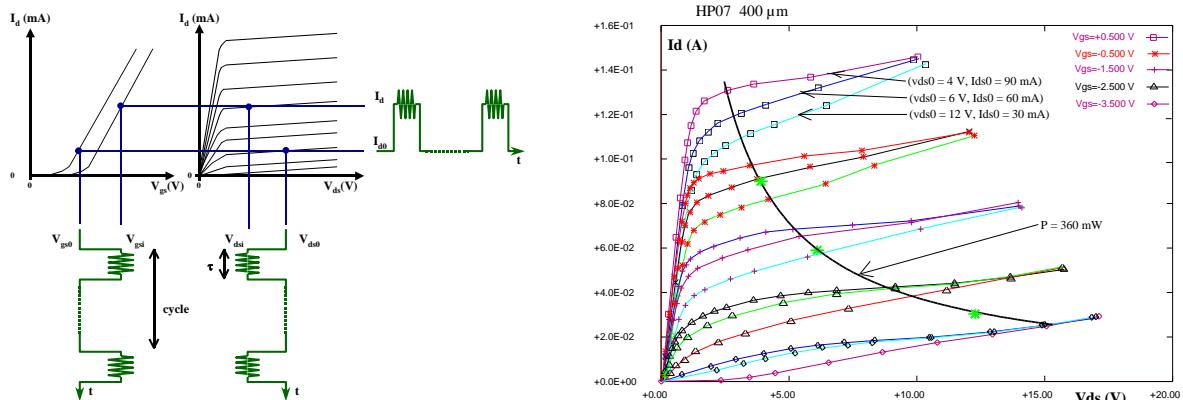
- pulsed measurements of static I/V networks for the extraction of the convective elements of the models as well as access resistances.
- measurements of [S] parameters necessary for the extraction of the linear and nonlinear reactive elements of the models

II.1.1 Measurement of the convective characteristics of the transistor.

The principle of the convective characterization consists in simultaneously applying to the input and the output of the component (transistor) short pulses around a given bias point. An example of characterization of a field effect transistor illustrates this principle in the following figure.

Convective measurements are then performed for constant thermal states (constant dissipated power), defined from different biasing points.

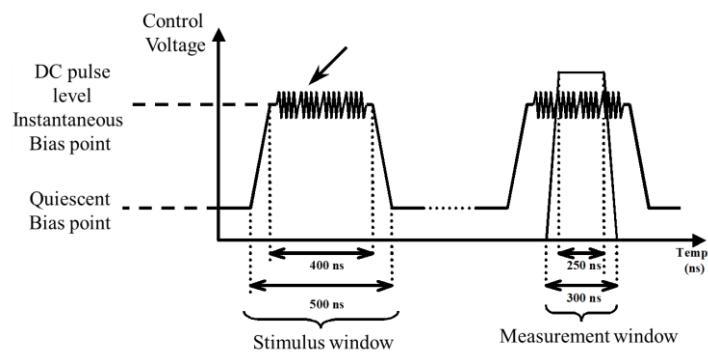
An example of static characteristic measurements is given in the following figure. This figure represents the measured I/V characteristics of a 4x100 μ m MESFET transistor.



II.1.2 Measurement of pulsed I/V characteristics.

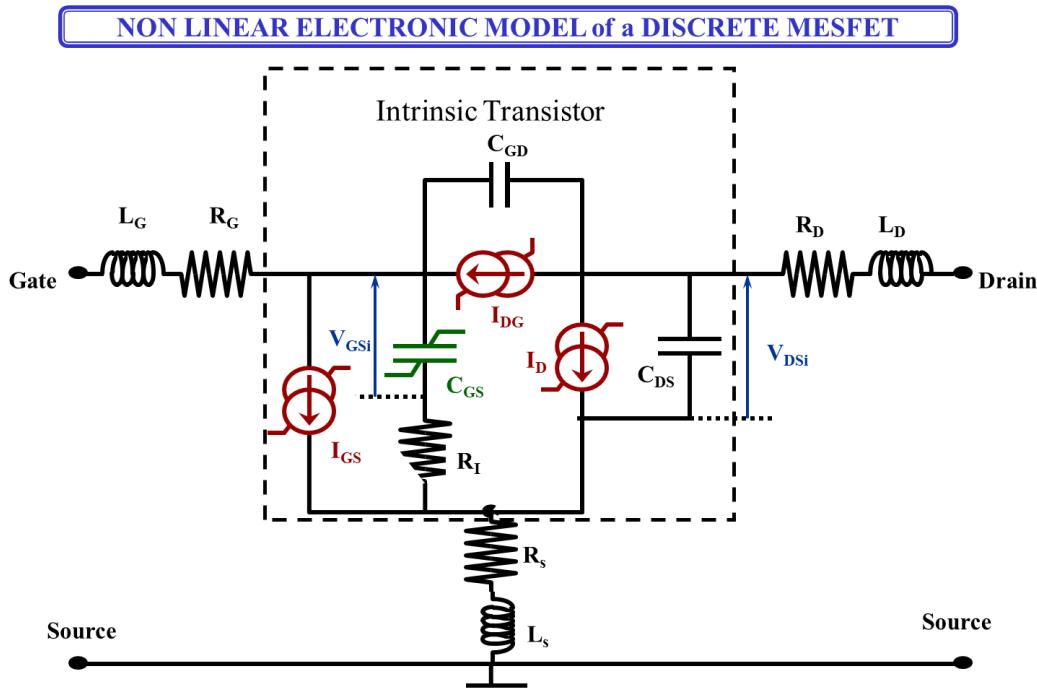
Small signal microwave characteristics obtained from [S] parameter measurements of the transistor are added to convective measurements to extract the complete model of the non-linear transistor.

The principle of measurement consists in superimposing a microwave excitation at the steady state of the short bias pulses. The measurement of the [S] parameters is carried out in a window called "profile", of duration less than or equal to the so called "stimulus" window of the microwave excitation signal:



At each measurement point of the I/V characteristic is associated a [S] parameter file over a wide frequency band. The measured [S] parameters are thus subsequently used to extract the linear and non-linear reactive elements from the models of the components.

In this PW, a classical structure including a controlled current source is chosen to model the transistor, as shown in the following figure:



This equivalent non-linear model is valid for several bias points and integrates 6 linear extrinsic elements (L_G , L_D , L_s , R_G , R_D , R_s) and 4 NON-LINEAR intrinsic elements (C_{GS} , I_{DG} , g_m , τ , I_{GS}).

The voltage-controlled current source can then be expressed as:

$$I_D = f_{Non-linear}[V_{gs0}, V_{ds0}, V_{gs}(t), V_{ds}(t)]$$

Similarly, the current I_{dg} can be expressed as:

$$I_{dg} = f_{Non-linear}[V_{gs0}, V_{gs}(t)]$$

Similarly, the C_{gs} capacitance can be expressed as:

$$Q_{gs} = f_{Non-linear}[V_{gs0}, V_{gs}(t)]$$

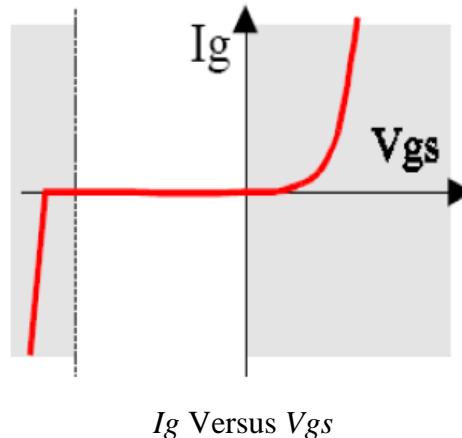
III EXPERIMENTAL OPERATIONS.

III.1 MEASUREMENTS OF STATIC CHARACTERISTICS OF A FET

III.1.1 Theoretical information: characteristic networks

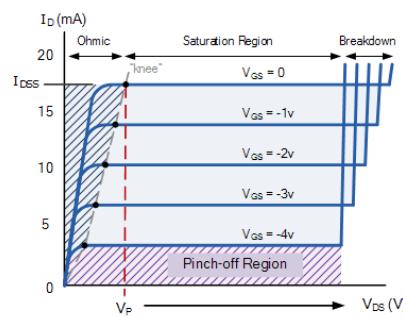
III.1.1.1 Input Network

FET transistors must only be used with negative V_{GS} voltages and below the reverse breakdown voltage. The input characteristics are the ones of a reverse biased diode. So, we always have: $I_G \approx 0$.



III.1.1.2 Output Network

The output network is the one with the $I_D = f(V_{DS})$ with $V_{GS} = \text{Constant}$ previously presented with the three useful regions: the ohmic region, the cut-off region and the saturation zone.



III.1.1.3 Transfer or Transconductance Network

The network corresponds to the curves $I_D=f(V_{GS})$ for $V_{DS} = \text{constant}$. The characteristics are straight lines for the ohmic part. In the saturation zone for the higher values of V_{DS} , the characteristics are parabolic, and one can write as a first approximation that:

$$I_D = I_{dss} \left(1 - \frac{V_{gs0}}{V_p} \right)^2$$

FETs are characterized by a wide dispersion of parameter values. For the same type of transistor, the maximum drain current I_{DS} and the V_{GS} pinch-off voltage V_p can vary by a factor of 4 to 5.

III.1.1.4 How to bias a FET ?

Because of this dispersion of the parameters, it is impossible to set the operating point by imposing the gate potential because I_D can vary too much for a given V_{GS} .

III.1.1.5 Small Signal Model

Examining the characteristics of a biased FET in the saturation zone shows that the equations governing the operation are:

- At the input: $I_G = 0$
- At the output: $I_D = g_m V_{GS} + g_d V_{DS}$

The slope or transconductance is defined, in first approximation, by:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{\partial I_D}{\partial V_{GS}} \Big|_{V_{DS}=\text{constant}}$$

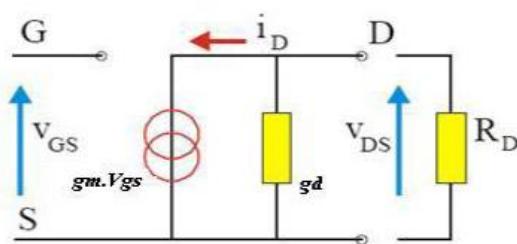
The internal resistance is defined by:

$$g_d = \frac{\Delta I_D}{\Delta V_{DS}} = \frac{\partial I_D}{\partial V_{DS}} \Big|_{V_{GS}=\text{constant}}$$

Using the relation

$I_D = I_{dss} \left(1 - \frac{V_{gs0}}{V_p} \right)^2$, the following expression for the value of the slope can be obtained:

$$g_m = -2I_{dss} \left(1 - \frac{V_{gs0}}{V_p} \right) \frac{1}{V_p}$$



Measurement scheme of static characteristics

At the input, a voltage V_{GS} is applied and the consumed current is equal to zero. At the output, the FET behaves like a current generator of intensity gmV_{GS} in parallel with a resistor. This simplified diagram allows interpreting the operation of the FETs working as an amplifier.

Since the transconductance characteristic is parabolic, FETs distort large amplitude signals.

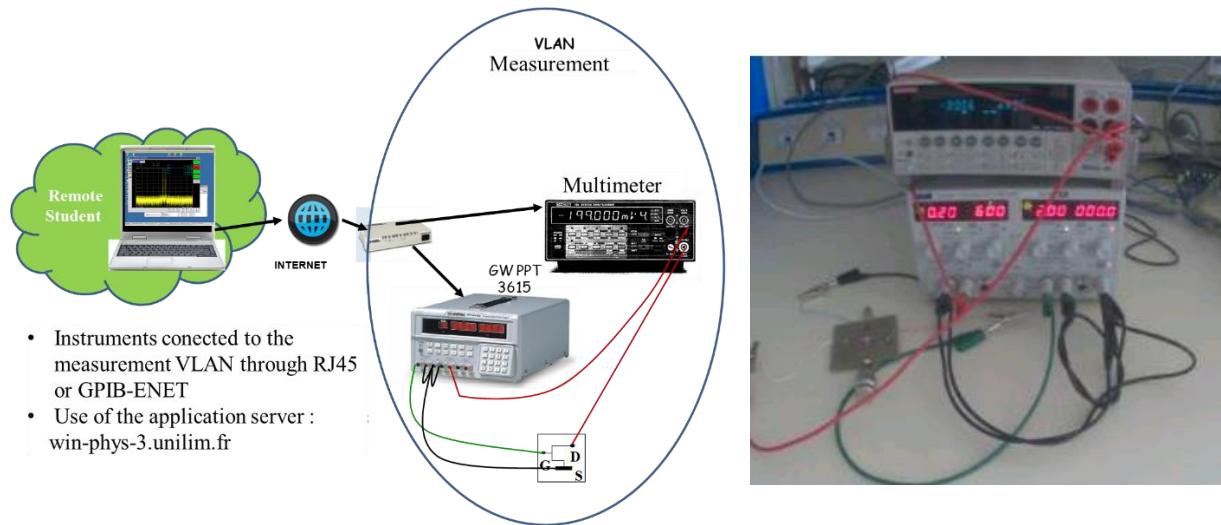
III.1.2 Manual Biasing of transistors.

The microwave transistors used in this PW are AsGa TEC. FLU17XM TEC Datasheet is given on the training platform.



[Datasheet FLU17XM FET](#)

You will then build a test bench of the following type (CH1 will be chosen for V_{gs} and CH2 will be chosen for V_{ds}):





- The power supplies you will use are all connected to the Measurement VLAN using GPIB adapters or directly using RJ45 wires.
- The multimeter allows visualizing the current consumed by the transistor, but it is not used in this PW for its measurement.
- Voltage and current measurements are made with the power supply.
- 50-ohm loads are connected at the microwave input/output ports of the transistor or amplifier.

You will first manually use the characterization test-bench to learn how to bias the transistor.

You will bias the transistor at the following point of polarization:

$V_{GS0} = -1V$ and $V_{DS0} = 3V$

In any case, ask the teacher to bias and unbiased the transistor for the first time without risk of damage of the TEC.

It is OF PRIME IMPORTANCE to bias the transistor correctly according to a methodology that will be described during the PW

The following tasks should be performed in the process:

1. Check the polarity of the power supplies: $V_{gs0} < 0$ and $V_{ds0} > 0$
Common Ground to
both power supplies.
2. Adjust the power supply voltages before connecting them to the TEC at the values:
 $V_{gs0} = 0V$ and $V_{ds0} = 0 V$
3. Adjust the short circuit current for the gate
4. Adjust the short circuit current for the drain
5. Connect the gate power supply to the FET.
6. Connect the drain supply to the FET.
7. Increase the gate voltage V_{gs0} first to the selected value, depending on the transistor and the polarization class
8. Compare this value with the one written in the data sheet.



9. - Increase the drain voltage V_{ds0} secondly to the desired I_{ds0} value.

MANDATORY !!!: Do not increase V_{DS0} when $V_{GSO}=0V$. The avalanche on the static characteristic at $V_{GSO} =0V$ is unexpected and irreversible.

To depolarize the transistor, perform the following tasks in order:

1. Decrease V_{ds0} to 0 V and then decrease V_{gs0} to 0V.
2. Disconnect the drain and gate ports respectively
3. Switch off the power supplies.

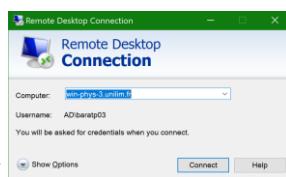
MANDATORY: Turn off the power supplies before disconnecting the FET...

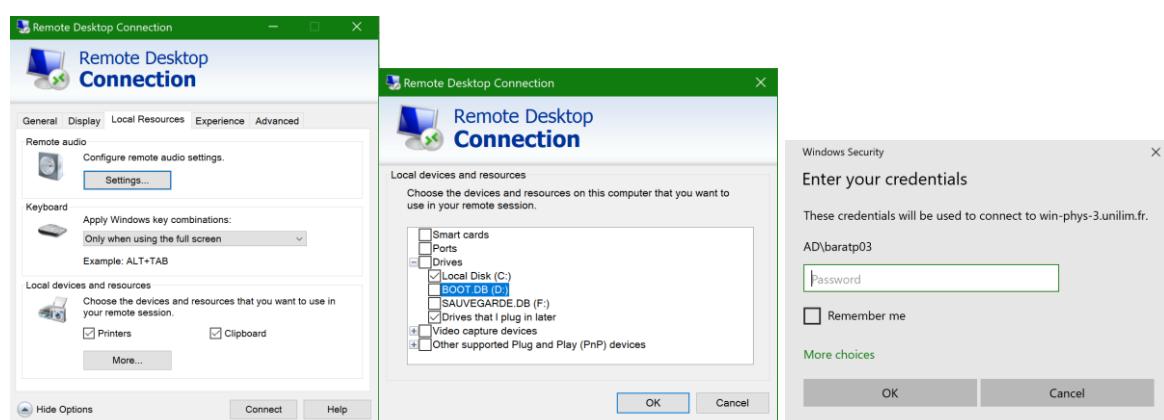
In all cases, ask first the teacher to define and justify the limits of the potential source power variations without risk of damage of the FET.

III.1.3 Automatic biasing of the FET using a LabVIEW software

The goal of this manipulation is to learn how to use the automatic static characterization program at your disposal.

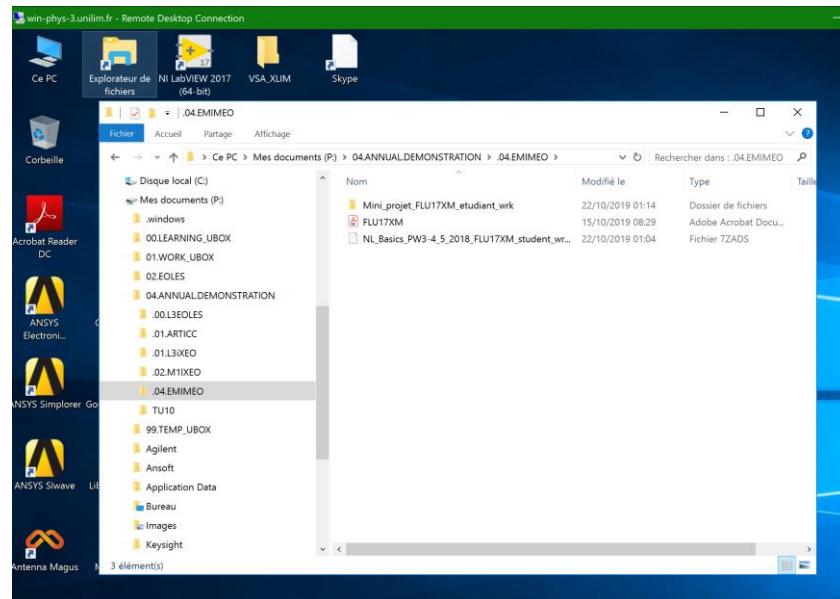
You must first download the programs that will allow you to trace these characteristics from the training platform on the application server **win-phys-3.unilim.fr**.

Login to the application server  with the following options:





If it is not already done, create a specific directory for your PW in your storage server “Mes document (P:)”.

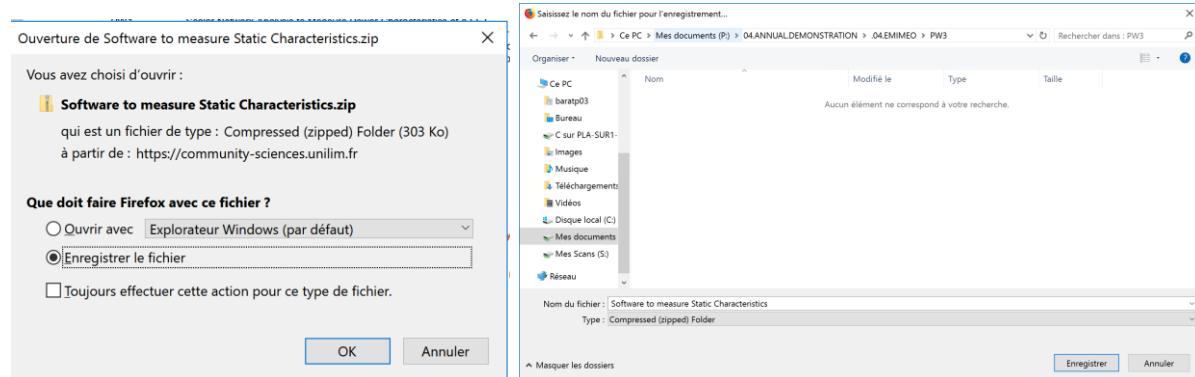


From the application server, login to the Moodle platform:

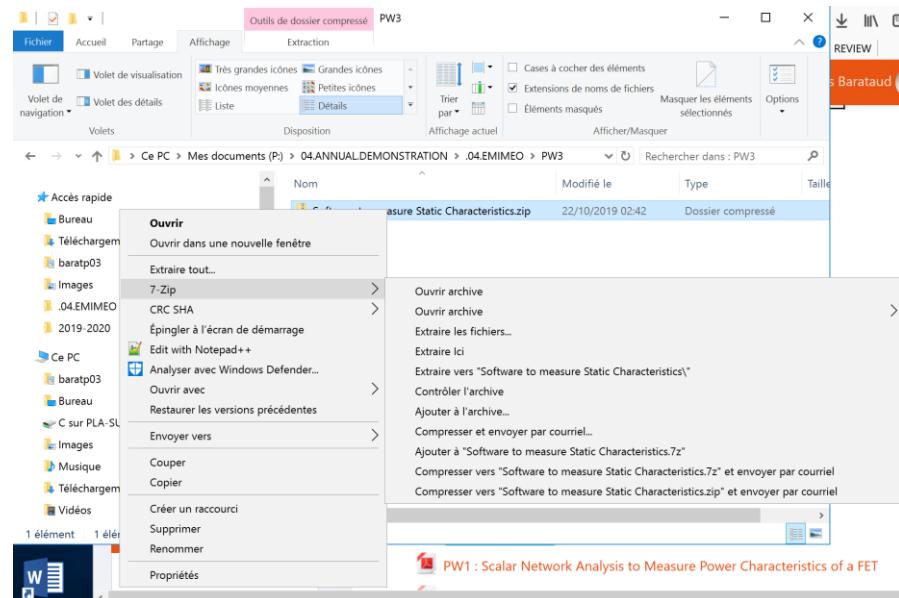
Download the zipped LabVIEW programs in the previous created directory:

PW3 : Software to measure Static Characteristics ($Id=f(Vds, Vgs)$)

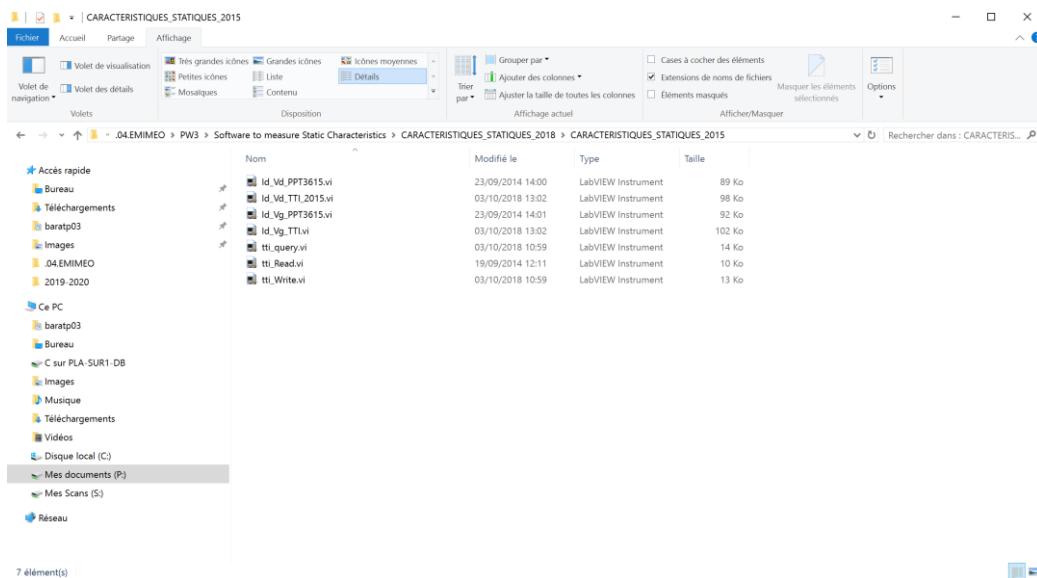
Use the following window to download it in the previous created directory:



In the directory where you downloaded the zip file, unzip it:

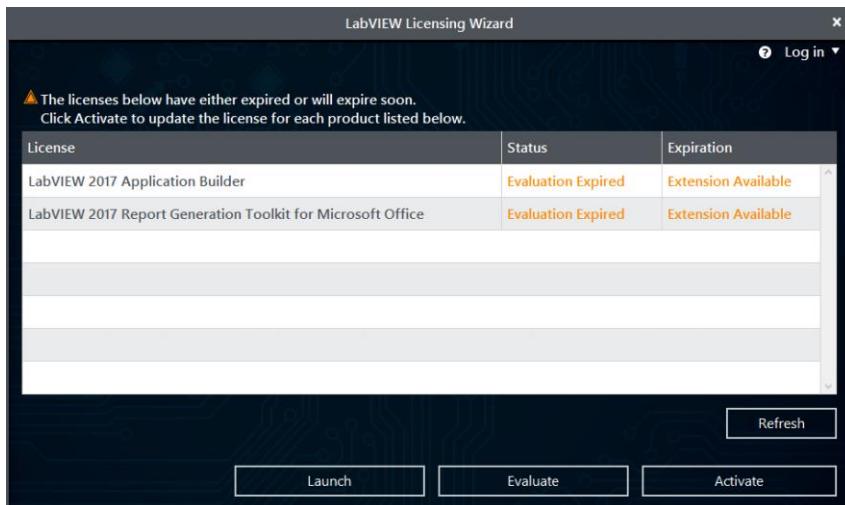


In the created directory many files appear:

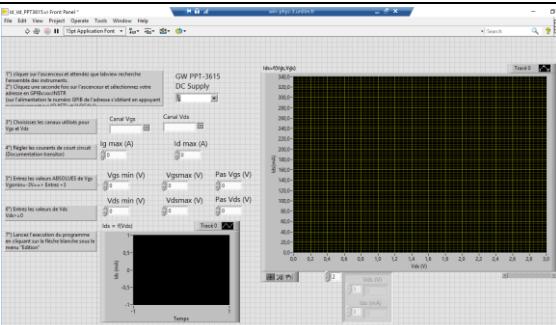
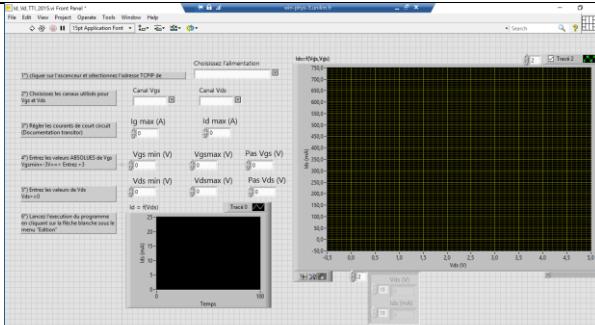


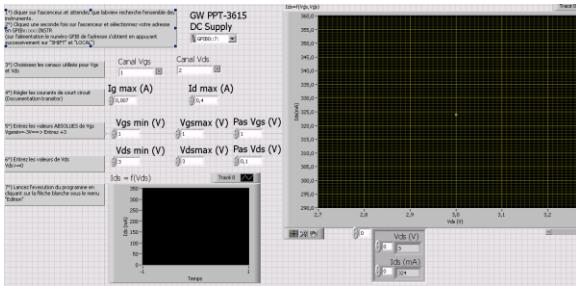
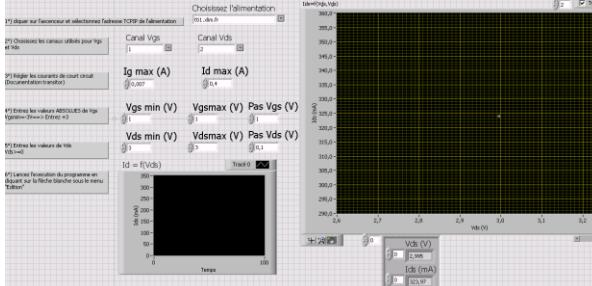


Click on the Id_Vd_PPT3615 program if your test bench is based on the use of a GW PPT 3615 power supply or Id_Vd_TTI if your test bench is based on the use of a TTI PL303 QMD power supply. If the next windows opens, click on the “Launch” button.



The following windows open then:

Use of a GW PPT 3615 power supply	Use of a TTI PL303 QMD power supply
 <p>1. click on the scroll bar and wait for labview to search for all the instruments. 2. Click a second time on the scroll bar and select your address in GPIBx :: xx :: INSTR (on the power supply the number GPIB of the address is obtained by pressing successively on "SHIFT" and "LOCAL") 3. Choose the channels used for Vgs (1,2 or 3) and Vds (1,2 or 3)</p>	 <p>1. Click on the scroll bar and select the TCPIP address of the power supply. 2. Choose the channels used for Vgs (1 or 2) and Vds (2 or 1)</p>

Use of a GW PPT 3615 power supply	Use of a TTI PL303 QMD power supply
<p>4. Set the values of the short-circuit currents (Transistor Documentation) Ig and Id</p> <p>5. Enter the ABSOLUTE values of Vgs (Vgsmin = -3V ==> Enter +3)</p> <p>6. Enter the values of Vds (Vds> = 0)</p> <p>7. Start the program execution by clicking on the white arrow under the "Edit" menu.</p>	<p>4. Enter the ABSOLUTE values of Vgs (Vgsmin = -3V ==> Enter +3)</p> <p>5. Enter the values of Vds (Vds> = 0)</p> <p>6. Start the program execution by clicking on the white arrow under the "Edit" menu.</p>
<p>Once the application is run, you should obtain the following window:</p> 	<p>Once the application is run, you should obtain the following window:</p> 

Whatever the power supply you use, check that the values given for this polarization correspond to the value obtained manually.

III.1.4 Measurement of Output I/V Characteristics.

III.1.4.1 Determination of g_d at constant V_{gs} .

Use the Id_Vd_PPT3615.vi program if your test-bench is based on the use of a GW PPT 3615 power supply or the Id_Vd_TTI.vi program if your test-bench is based on the use of a TTI PL303 QMD power supply.

You will now plot the output network characteristics $I_{ds} = f(V_{ds})$ for a given value of V_{gs0} of the transistor under test.

To do this you will choose the following values (to be checked ABSOLUTELY with the teacher):

- I_{gmax} (A) =
- I_{dmax} (A) =

- $V_{gs0min} (\text{V}) = V_{gs0}$
- $V_{gs0max} (\text{V}) = V_{gs0}$
- $V_{gs0step} (\text{V}) = 0.5$
- $V_{ds0min} (\text{V}) =$
- $V_{ds0max} (\text{V}) =$
- $V_{ds0step} (\text{V}) =$

Once you have drawn this characteristic, use the table viewer below the graph to calculate the value of g_d for this curve.

Compare this value to the one given by the manufacturer.

III.1.4.2 Determination of g_d for many V_{gs} .

You will now plot the output network characteristics $I_{ds} = f(V_{ds})$ for many values of V_{gs0} of the transistor under test to compare these curves to the ones given by the manufacturer.

To do this you will choose the following values (to be checked ABSOLUTELY with the teacher):

- $I_{gmax} (\text{A}) =$
- $I_{dmax} (\text{A}) =$
- $V_{gs0min} (\text{V}) =$
- $V_{gs0max} (\text{V}) =$
- $V_{gs0step} (\text{V}) =$
- $V_{ds0min} (\text{V}) =$
- $V_{ds0max} (\text{V}) =$
- $V_{ds0step} (\text{V}) =$

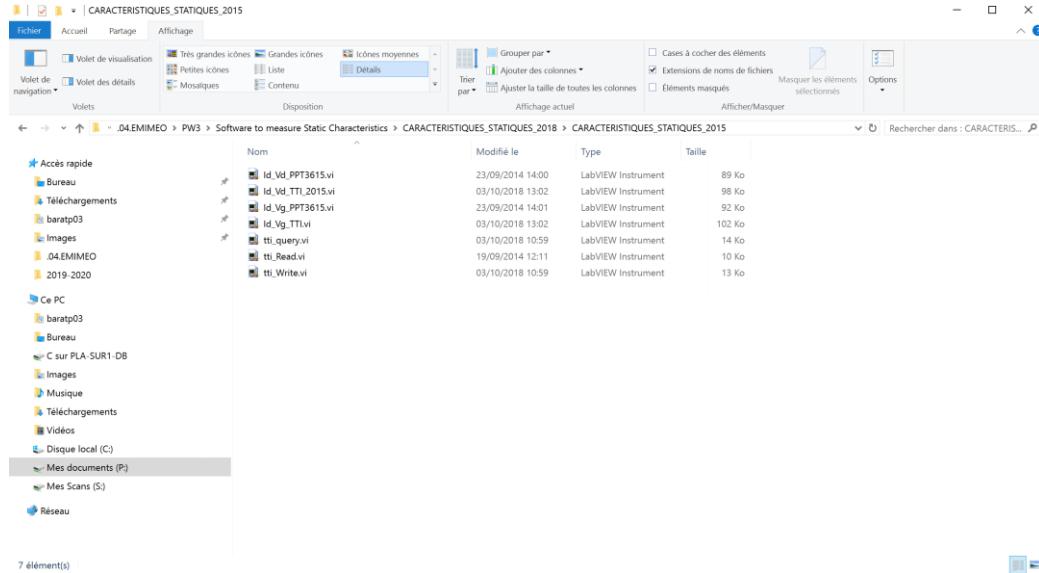
Once you have drawn these characteristics, use the table viewer below the graph to calculate the value of g_d for two values of $(V_{gs0}; V_{ds0})$.

Comment your results.



III.1.1 Measurement of Input I/V Characteristics.

In this part of the PW, you will use two other LabVIEW programs:



Use the Id_Vg_PPT3615.vi program if your test-bench is based on the use of a GW PPT 3615 power supply or the Id_Vg_TTI.vi program if your test-bench is based on the use of a TTI PL303 QMD power supply.

III.1.1.1 Determination of g_m at constant V_{ds} .

Use the Id_Vg_PPT3615.vi program if your test-bench is based on the use of a GW PPT 3615 power supply or the Id_Vg_TTI.vi program if your test-bench is based on the use of a TTI PL303 QMD power supply.

You will now plot the output network characteristics $I_{ds} = f(V_{gs})$ for a given value of V_{ds0} of the transistor under test.

To do this you will choose the following values (to be checked ABSOLUTELY with the teacher):

- I_{gmax} (A) =
- I_{dmax} (A) =
- V_{gs0min} (V) =
- V_{gs0max} (V) =
- $V_{gs0step}$ (V) =
- V_{ds0min} (V) = V_{ds0}

- V_{ds0max} (V) = V_{ds0}
- $V_{ds0step}$ (V) = 0.1

Once you have drawn this characteristic, use the table viewer below the graph to calculate the value of g_m for this curve.

Compare this value to the one given by the manufacturer.

What can you say about this characteristic? Which component has such a characteristic? What is the value of the pinch-off voltage?

III.1.1.2 Determination of g_m for many V_{ds} .

You will now plot the output network characteristics $I_{ds} = f(V_{gs})$ for many values of V_{ds0} of the transistor under test to compare these curves to the ones given by the manufacturer.

To do this you will choose the following values (to be checked ABSOLUTELY with the teacher):

- I_{gmax} (A) =
- I_{dmax} (A) =
- V_{gs0min} (V) =
- V_{gs0max} (V) =
- $V_{gs0step}$ (V) =
- V_{ds0min} (V) =
- V_{ds0max} (V) =
- $V_{ds0step}$ (V) =

Once you have drawn these characteristics, use the table viewer below the graph to calculate the value of g_m for two values of $(V_{gs0}; V_{ds0})$.

Comment your results.

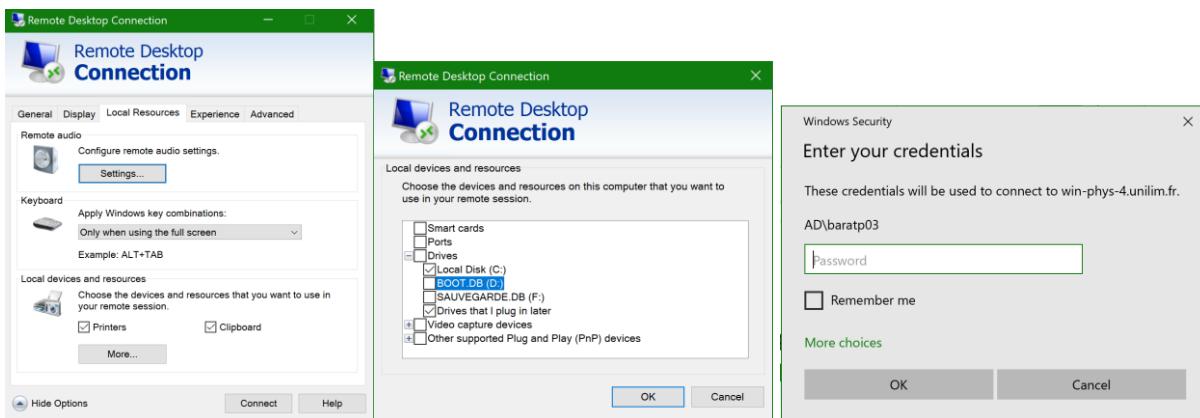


III.2 STATIC SIMULATION OF THE FET

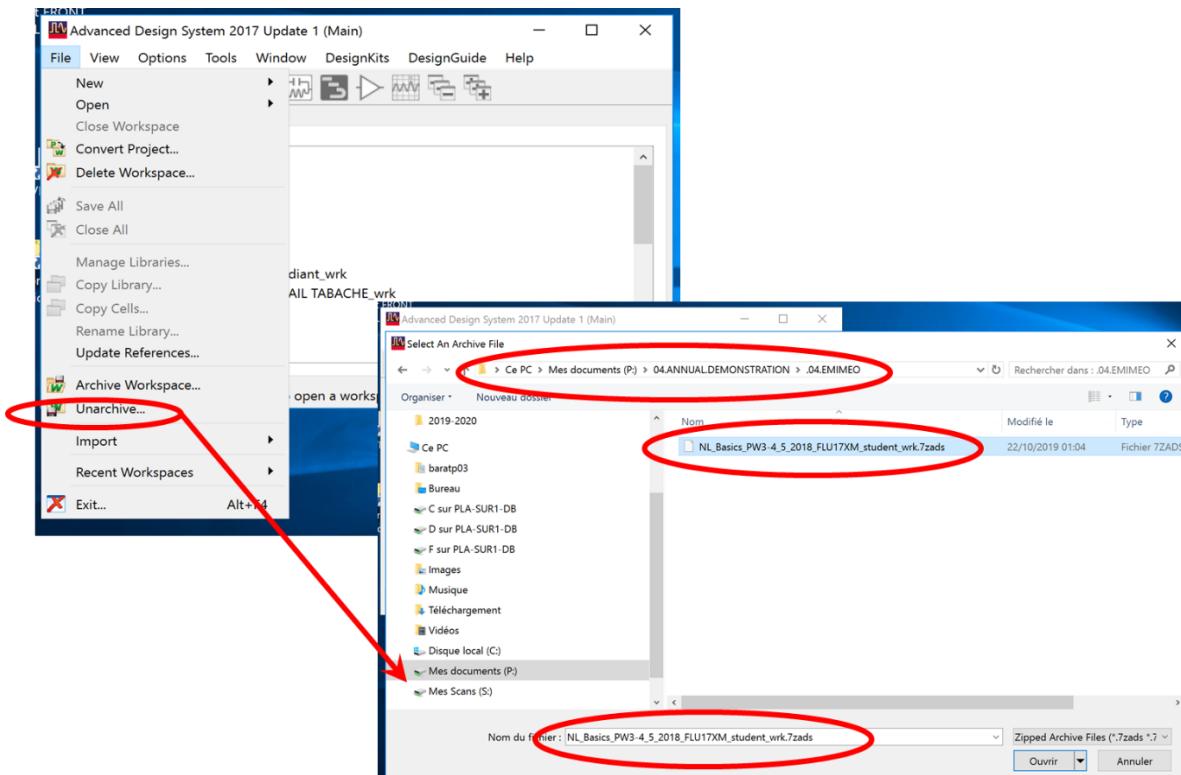
You must first download the programs that will allow you to trace these characteristics from the training platform on the application server **win-phys-4.unilim.fr**.

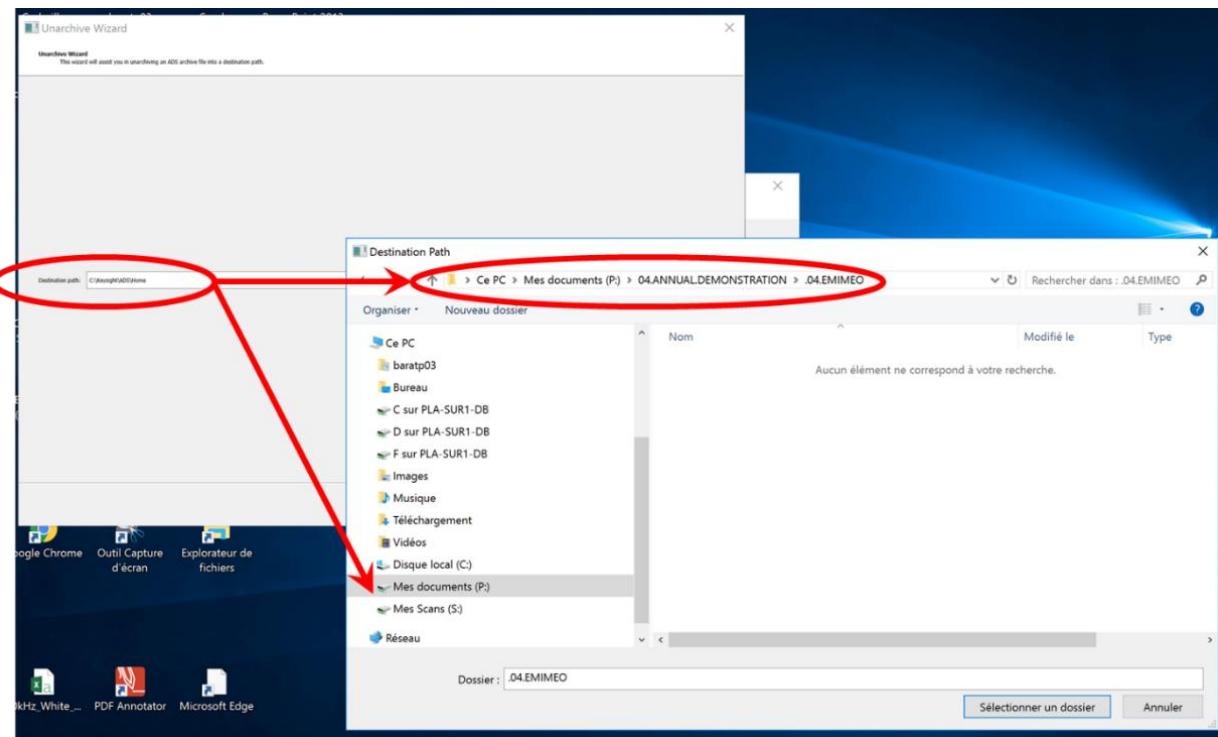
Login to the application server

with the following options:



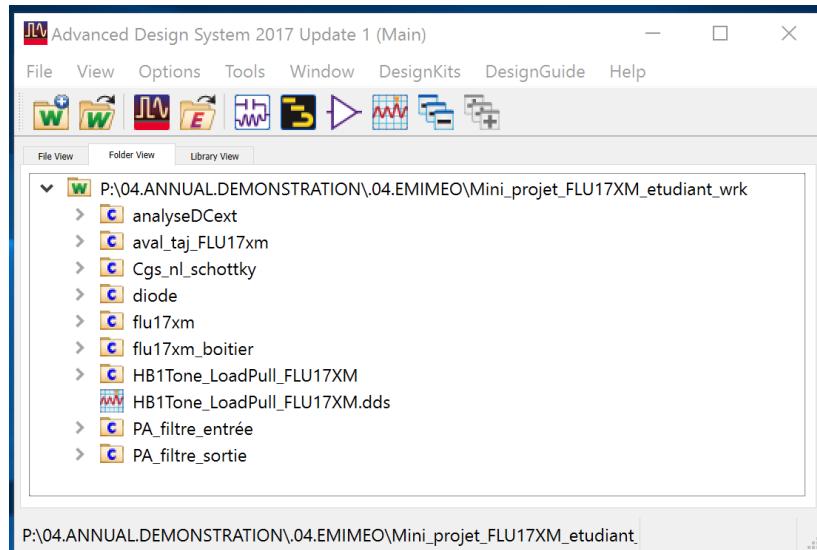
You will use the ADS archived workspace called ‘Initial Workspace for PW3, 4 and 5’ which you will download on the training platform. Download it and unarchive it in a specific directory you previously created in your storage server “Mes document (P:)”.





Click on the “selectionner un dossier” button and then “next button” many times to finish with the “Finish” button.

A window as the following one should then appear:



In addition, you have a small booklet detailing examples of all the simulation files you will need to create in the workspace, along with the corresponding result score sheets.



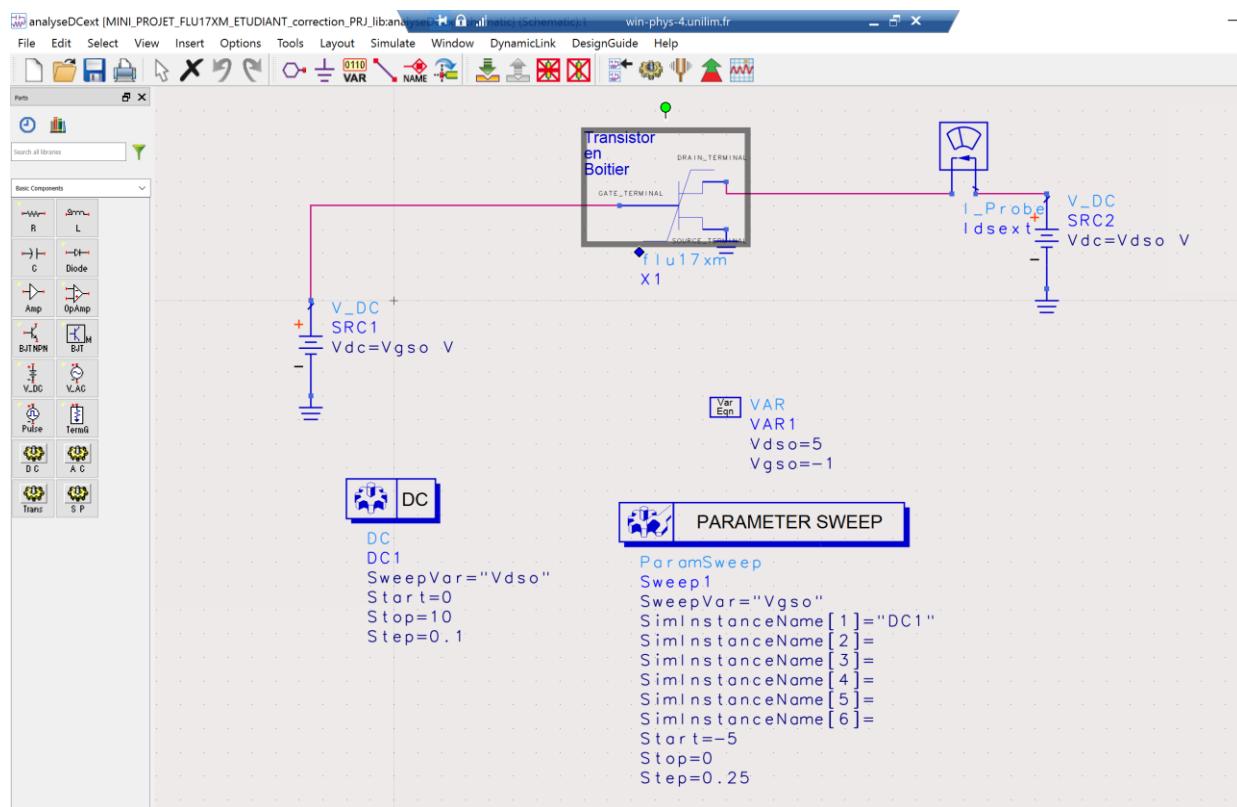
III.2.1 Static Simulation of the extrinsic model of the FET.

Open the *analyseDCext* schematic:

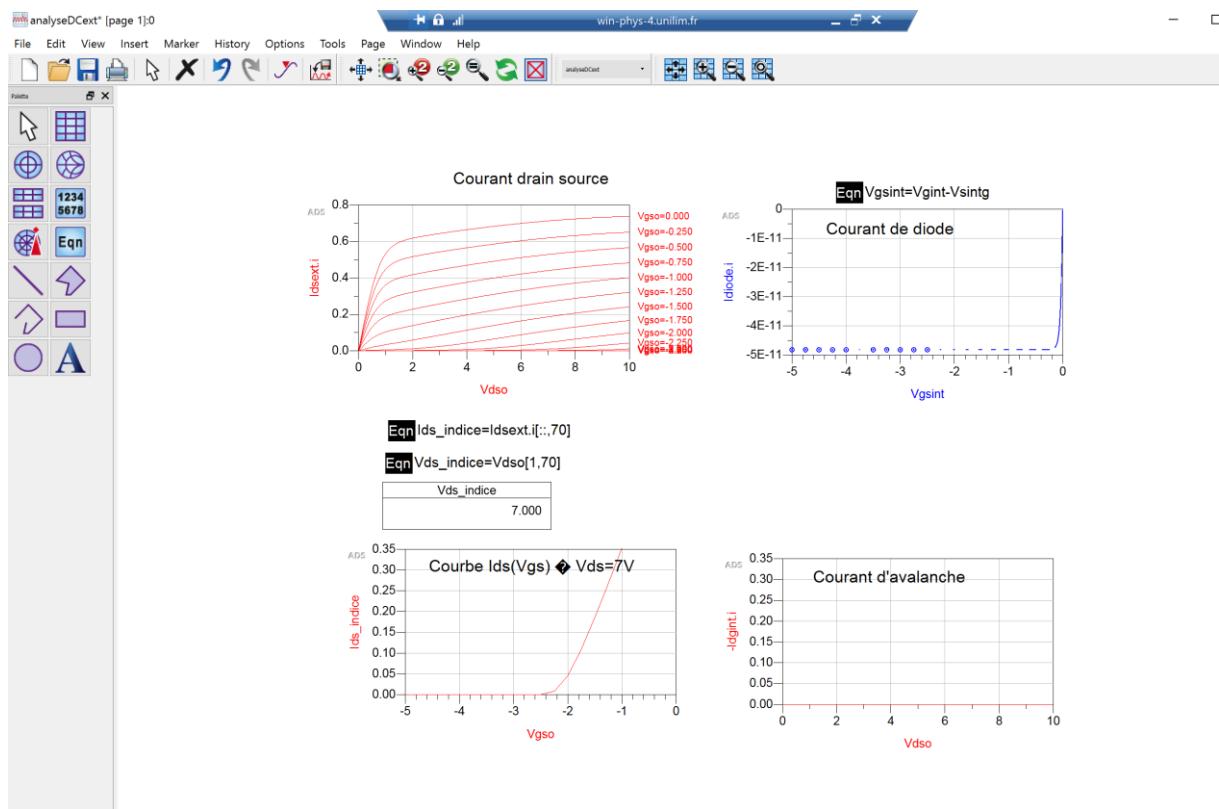
You must then complete this schematic so that you can plot the static curves of the extrinsic transistor, the ranges of V_{ds0} and V_{gs0} voltage variations are as follows:

- V_{gs0} : from -5V to 0.5V with a 0.5V step,
- V_{ds0} : from 0V to 20V with a 0.1V step.

The schematic should look like the following figure:

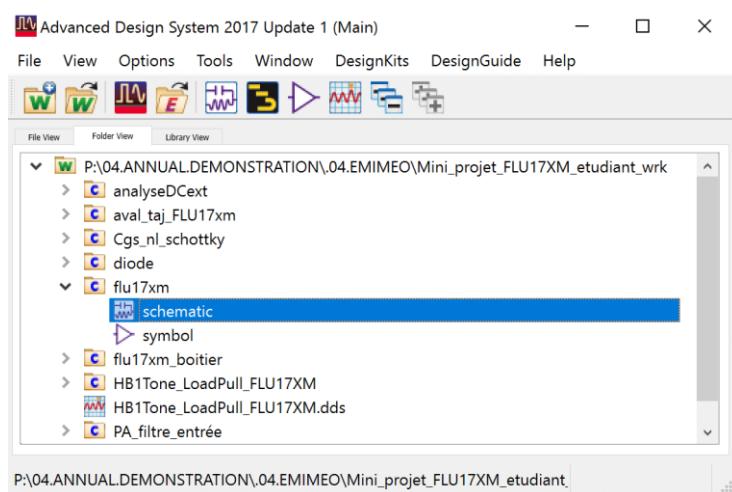


Save your file then start the simulation, an empty window "data display" appears; recreate the entire data display file as follows:

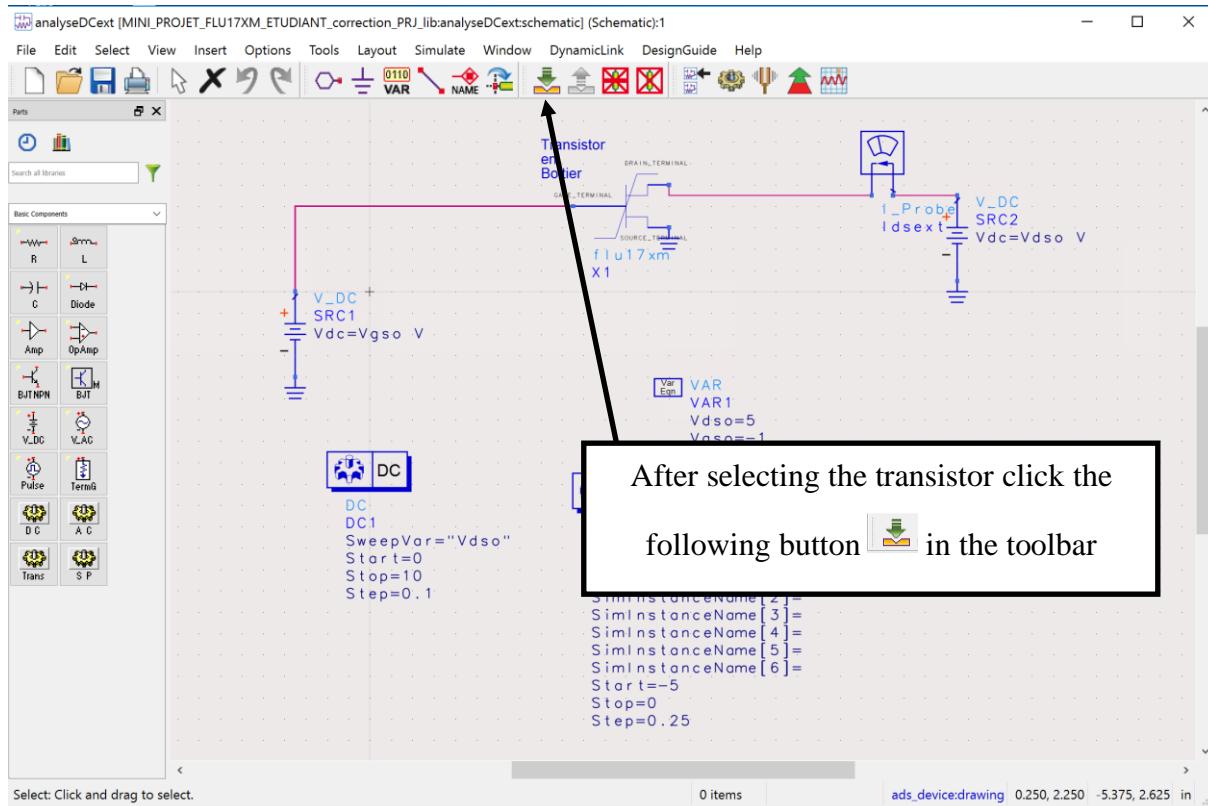


- Comment the results obtained and relate the simulated variables (currents and voltages) to their location in the internal circuit diagram of the transistor.

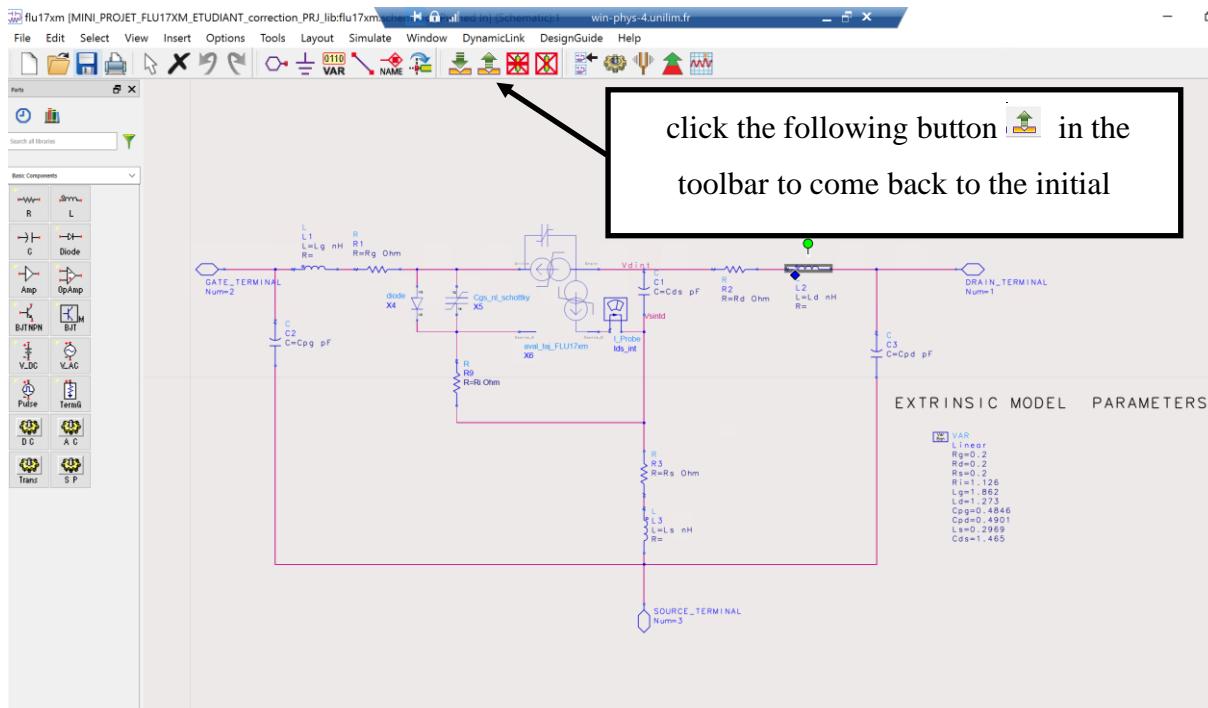
Help: the non-linear model of the extrinsic transistor is described by the cell or schematic flu17xm.



You can edit this file by opening the schematic of this cell or selecting the symbol of the transistor on the analyzeDCext schematic and clicking on:



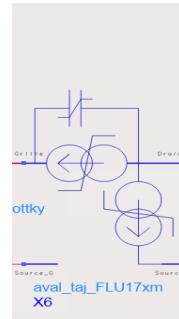
Then the flu17xm schematic opens:



Same process if you want to have more information concerning:

- the intrinsic nonlinear model

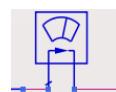
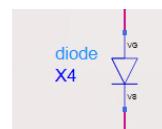
aval_taj_FLU17xm



- the capacitance CGS_nl_schottky



- the diode



The currents are measured by probes: **I_Probe** (in the Probe Component/Iprobe menu).

The voltages are defined by names associated with the connection wires where it is

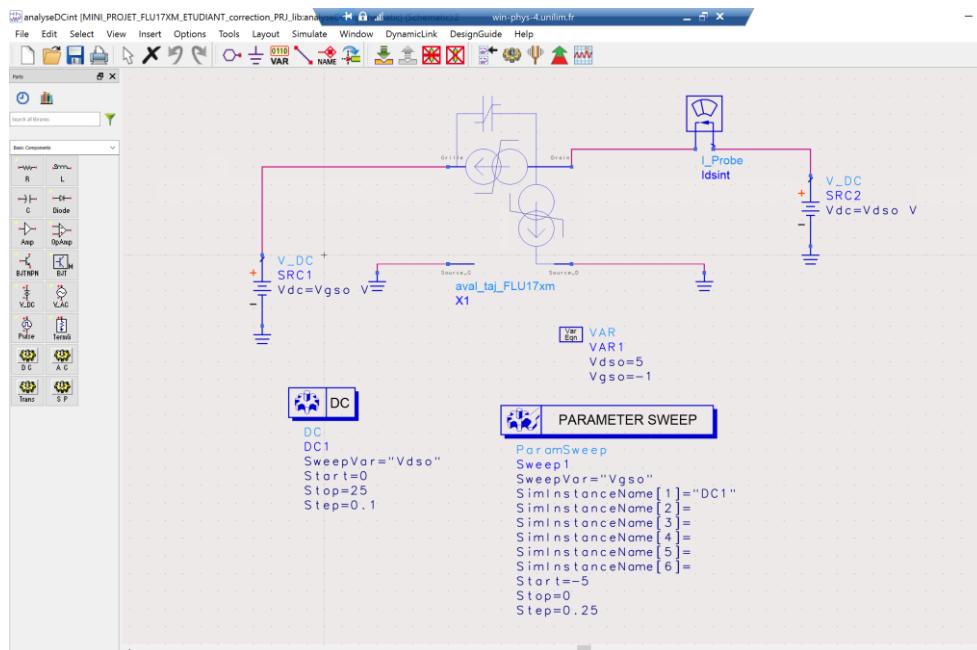


desired to measure the voltage:

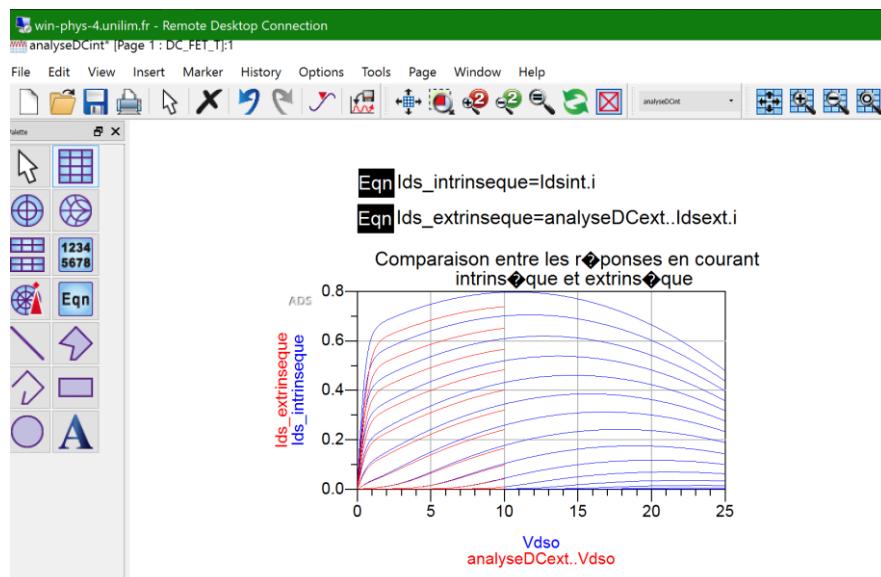
To set the name of a connection: Insert / Wire / Pin label.

III.2.1 Static Simulation of the intrinsic model of the FET.

You will now plot the static characteristics of the intrinsic transistor. For this, you will modify the *analysisDCext* schematic you previously implemented and save it as a new schematic file renamed *analysisDCint.dsn*.



Run the simulation, a "data display" window named *analysisDCint.dds* opens. Complete this window to compare the intrinsic and extrinsic results.



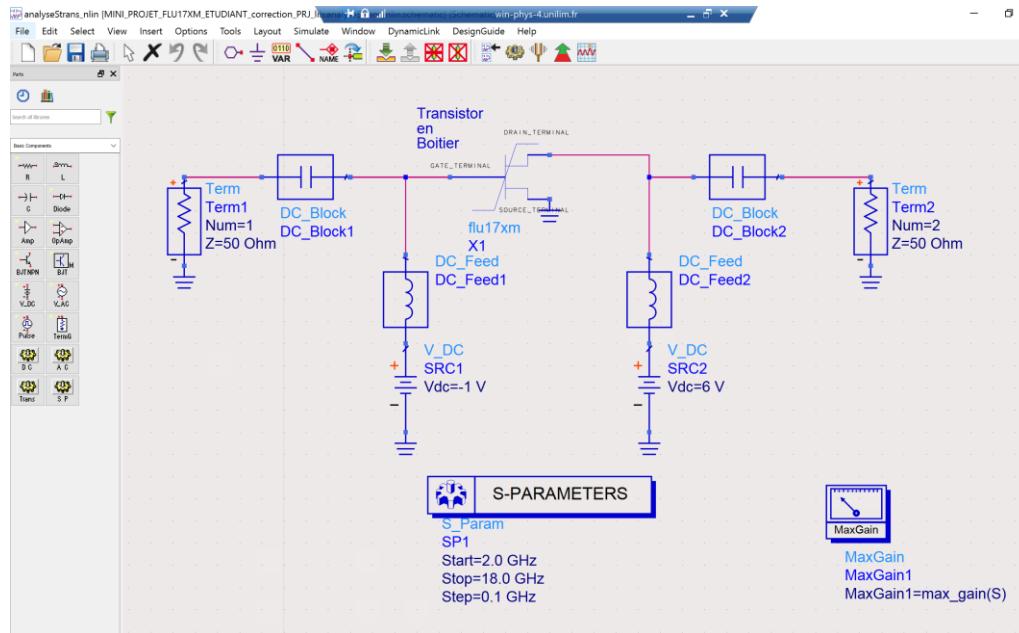
Comment the results



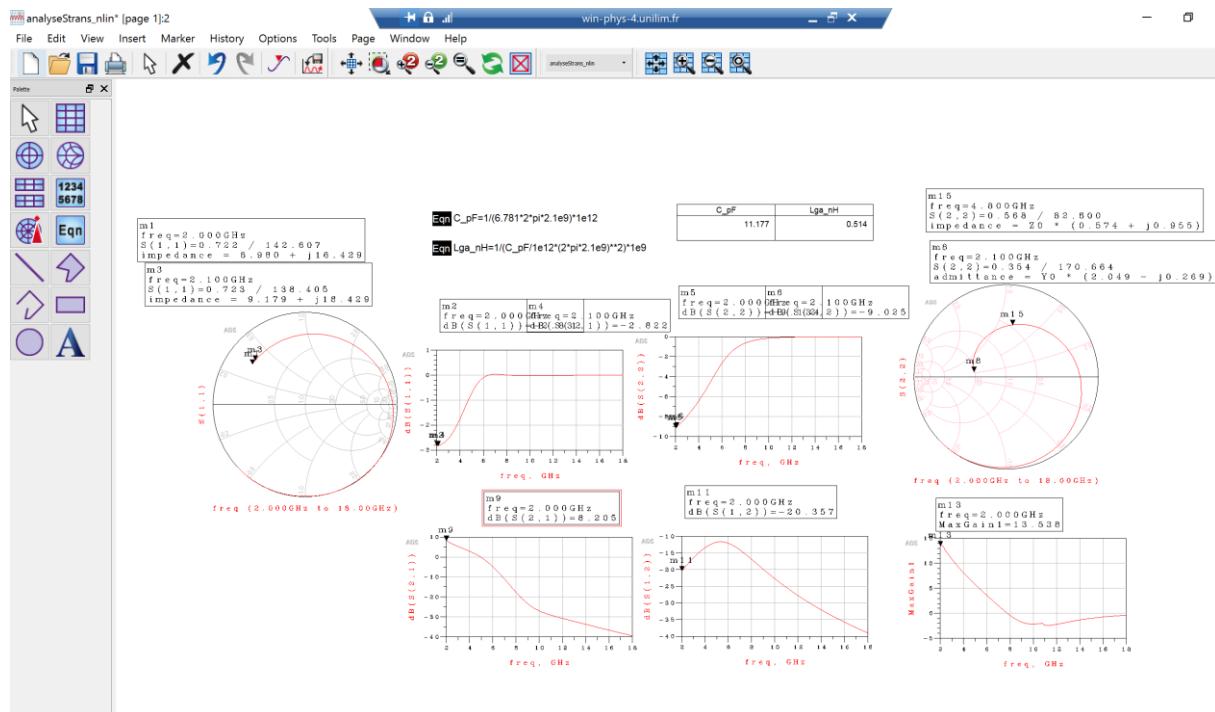
III.3 S PARAMETER SIMULATION OF THE FET.

The simulation of the S parameters between 500 MHz and 3 GHz of the transistor is obtained by using the nonlinear model (flu17xm file) around 2 polarization points ($I_{ds}/2$ and $I_{ds}/10$) and $V_{ds0} = 3V$.

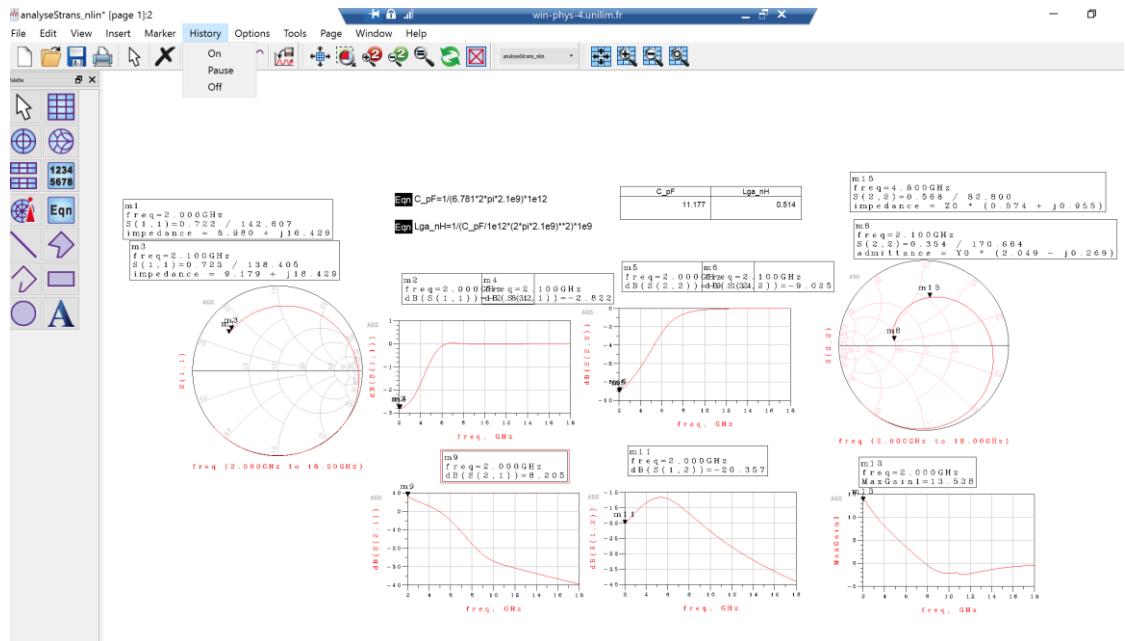
Create a schematic file: *analysisStran_nlin.dsn*, perform the simulation for the first bias point as follows:



Configure the "data display" window to view the four S parameters as follows.

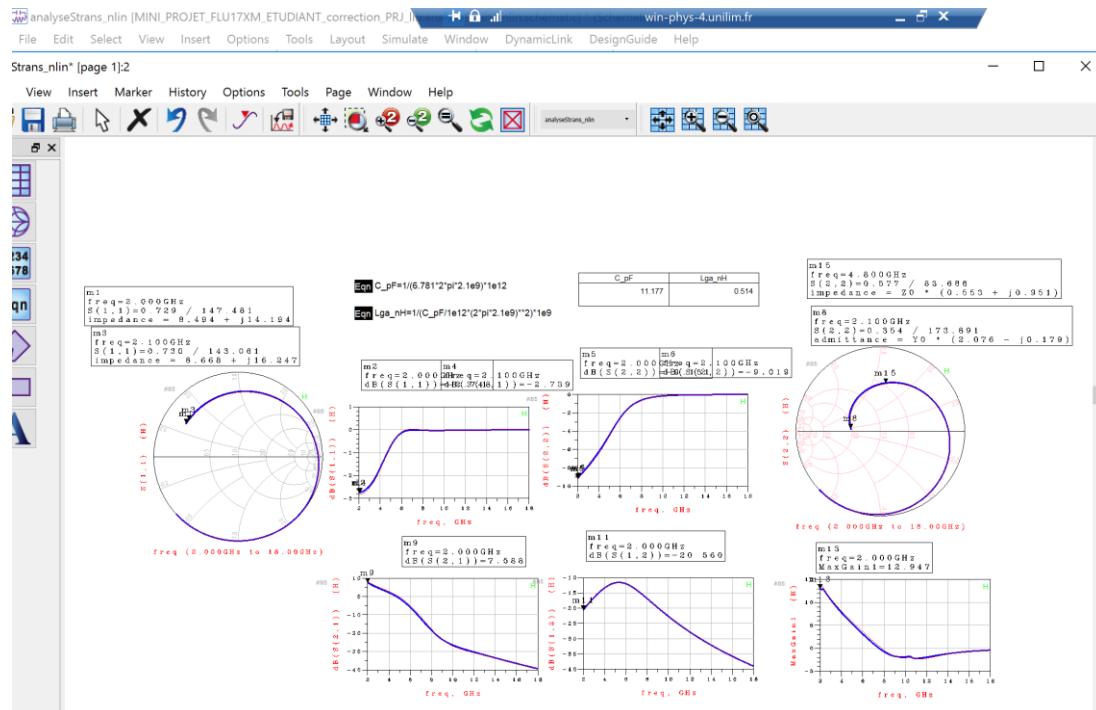


In the data display window click on the button « History On » :

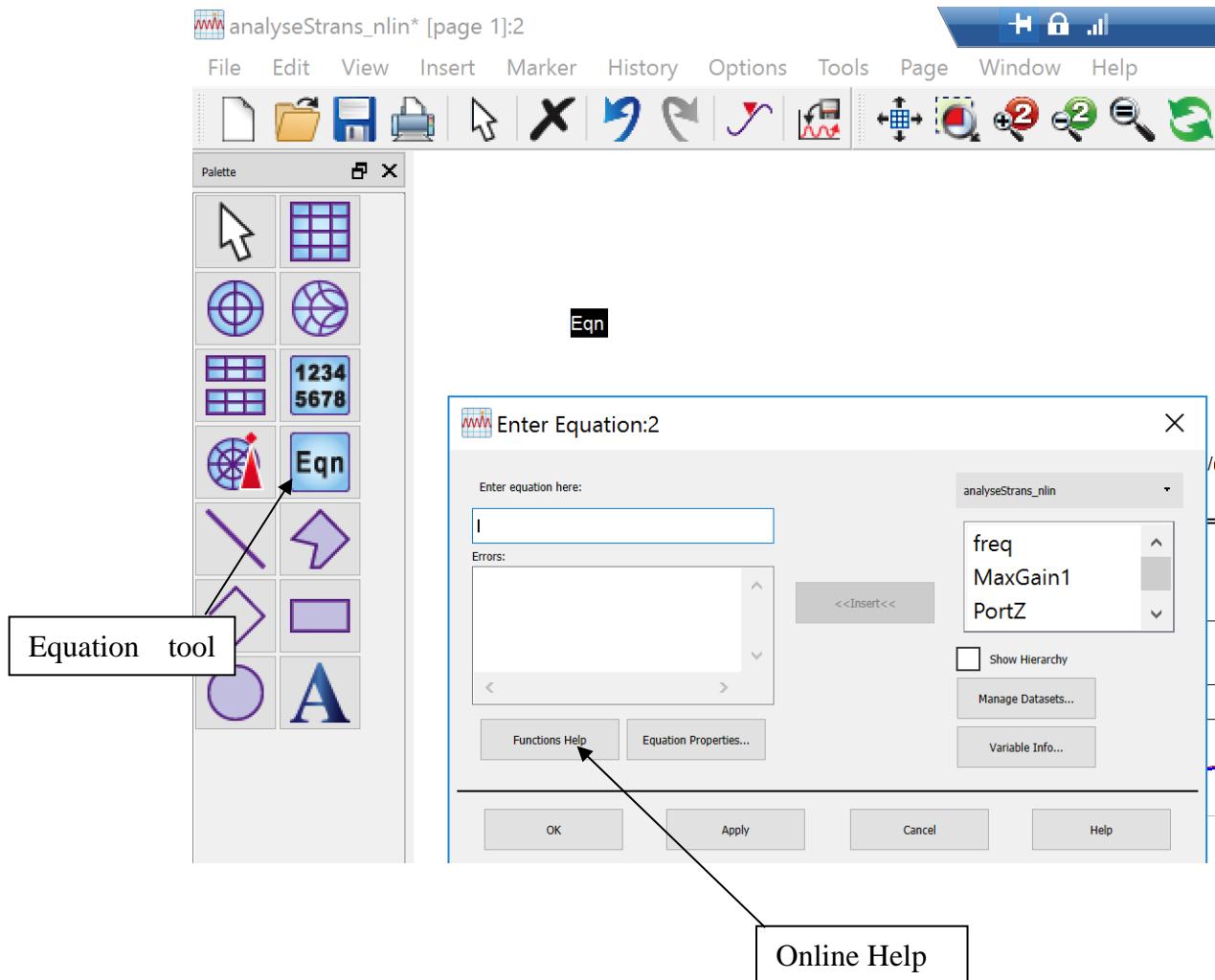


What should be added to the previous simulation file to ensure correct static operation of the transistor corresponding to the desired bias point?

Restart the simulation of the file *analyzeStran_nlin* with the second bias point. In the "data display" window, observe the results of the two simulations and compare the parameters [S] of the nonlinear models for these two bias points. Comment these results.



In this "data display" window, plot the phase of the parameters [S]. Recall the theoretical definition of the group delay. Then implement the determination of the group delay using an equation box as shown in the following figure:



You can use the function `diff()`

Plot the group delay according to the frequency. With a marker, give the value of a specific point of the TPG curve, then check the accuracy of the implemented equation using a quick calculation.

Conclusion.



In the workspace window change the packaged model of transistor with the model of the transistor die, run the simulation and plot the parameters [S] @ 2GHz that will allow you to design the power amplifier during the next lab session.

