

Semester S1

Basics of Active and Non-Linear Electronics

PRACTICAL WORK

PW5:

**DESIGN OF A LINEAR AMPLIFIER @ 2GHZ USING
KEYSIGHT ADS**

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DESIGN OF A LINEAR AMPLIFIER @ 2GHZ USING KEYSIGHT ADS

I OBJECTIVE

The aim of this PW5 is to use the Keysight ADS software to design and build at a low-level (i.e. from S-parameters) an optimized power amplifier [S] using an Eudyna FLU17XM Field Effect Transistor (FET). This PW will require to carry out ADS simulations in order to realize the input and output impedance matching of the FET using microstrip lines. The main difference with respect to PW4 is that this optimization process will be done in the linear mode (low-level signal) and not in the saturated mode (high-level signal) also with a nonlinear model of the FET. Once optimized, you will have to build the layout of the designed amplifier and to print this layout on a printed circuit board (PCB) using a T-Tech engraving machine and the ISOPRO control software.

In the last PW of this series (PW6), you will test the real amplifier by comparing the performance of the amplifier with respect to the simulated results. This will be done using the measurement devices used during the first 3 PWs of this series. So you will measure the S-parameters of the amplifier with a vector network analyzer, the power and efficiency characteristics with a scalar network analyzer and finally the linearity characteristics using 3rd order intermodulation characterization with a spectrum analyzer.

In this PW, we want to optimize the **low-level gain** (i.e. using S-parameter simulations) of the FET transistor you have already used in the previous experimental PWs in a narrowband around the frequency of 2 GHz:

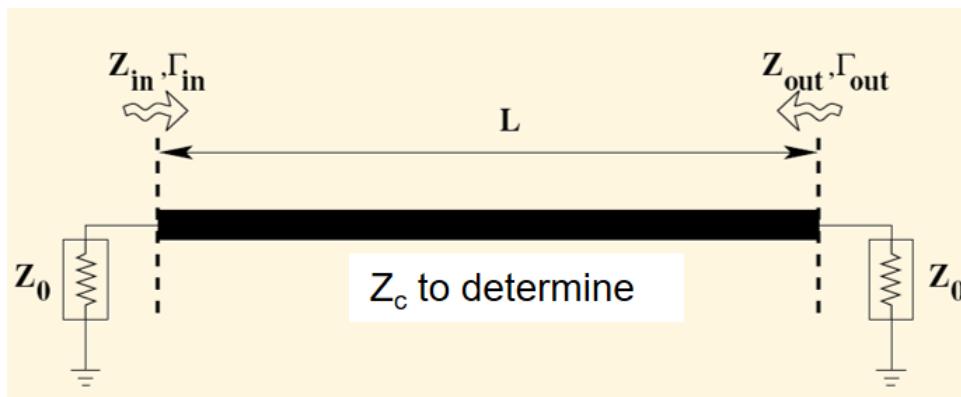
- to a generator having a purely real internal impedance R_0 of 50Ω connected at the input of the FET;
- to a purely real load of 50Ω connected at the output of the FET.

You have to work again with the ADS project you have work with in PW3 & 4.

II TRANSISTOR MATCHING USING STUBS – THEORETICAL REMINDERS

II.1 TRANSMISSION LINE

When designing linear or power amplifier, designers use microstrip transmission lines rather than lumped elements. At high frequency, the microstrip line does not behave like a simple wire of null resistance. This transmission line, according to its (constant) characteristic impedance and its length (chosen according to the desired effect) exhibits an input impedance different with respect to the load impedance connected at the other extremity. A microstrip transmission line can be represented as follows



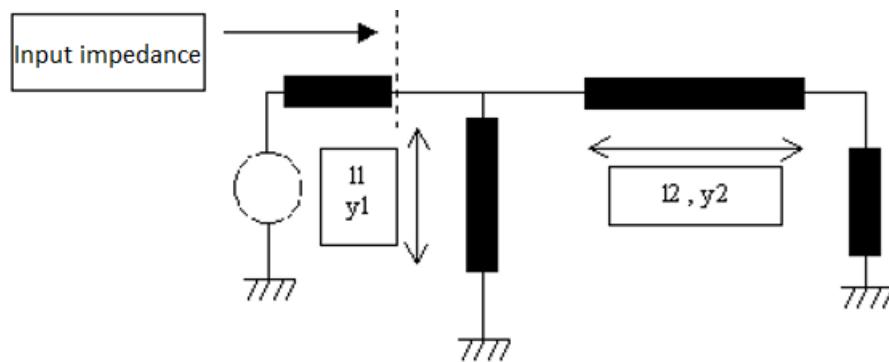
Its characteristic impedance is written Z_c . When inserted between two 50Ω impedance ports (for S-parameter measurement or simulation for instance), the input impedance and the reflection coefficient of the transmission line at its input writes respectively

$$Z_{in} = Z_c \frac{Z_{out} + jZ_c \tan(\beta l)}{Z_c + jZ_{out} \tan(\beta l)} \quad (1)$$

$$|\Gamma_{in}|^2 = \frac{P_r}{P_i} = \left| \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \right|^2 \quad (2)$$

II.1.1 Simple stub setup

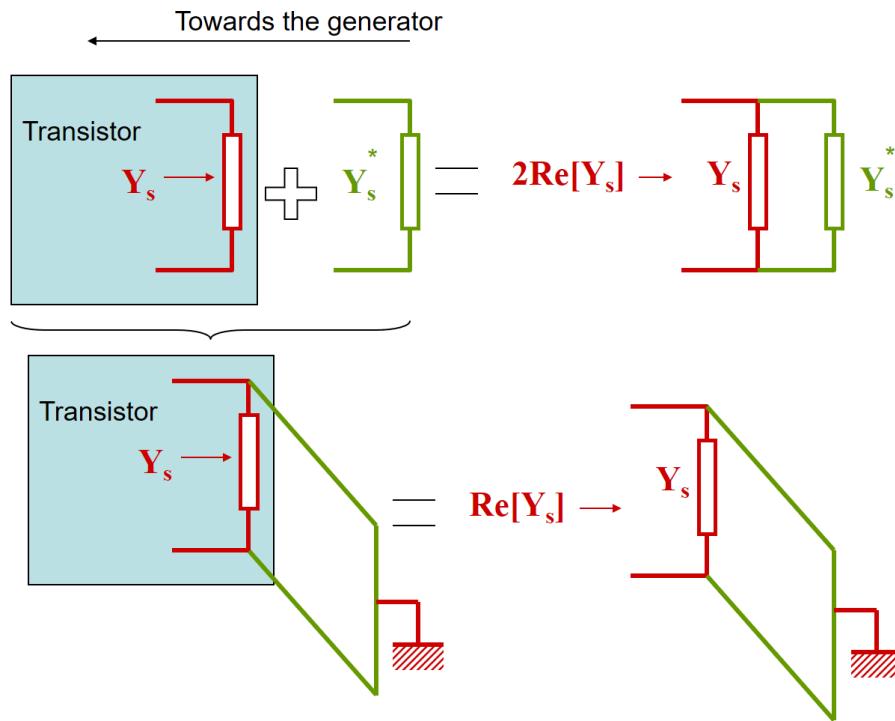
The "simple stub" assembly generally enables realizing the impedance matching in order to make sure that the generator (with a internal impedance) has a 50Ω load impedance at the input plane (Input Impedance) symbolized by the dotted line in the next figure, while the load at the end of the line may have a different impedance.



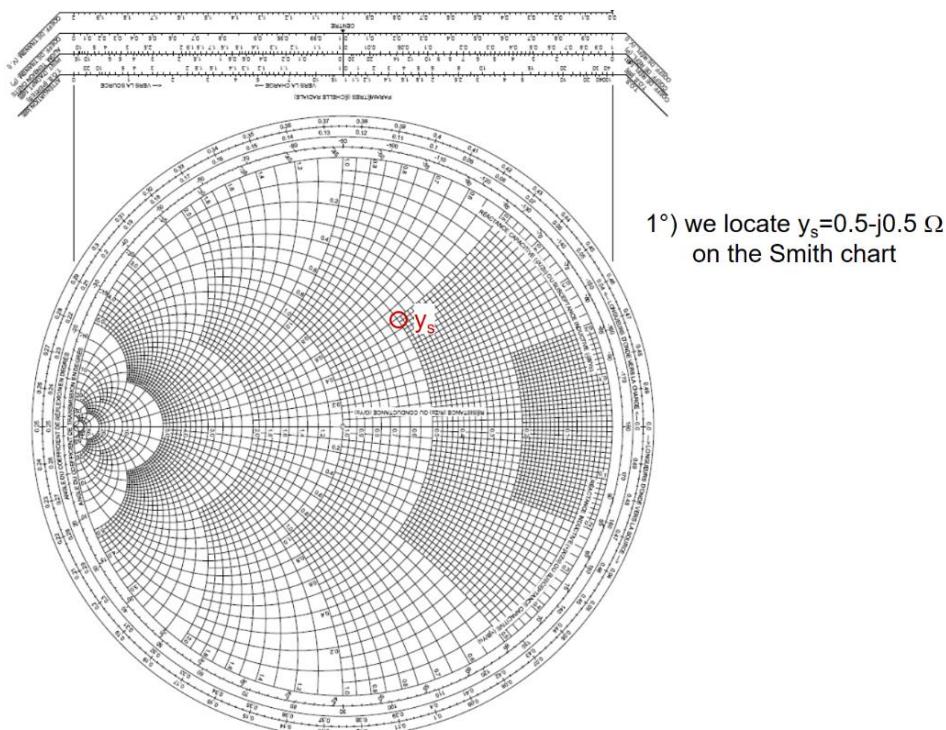
The lengths and widths of sections l_1 and l_2 are usually determined using a Smith chart working with normalized values (i.e. all impedances and admittances are divided by the characteristic impedance of the lines used, here 50Ω). In addition, in this configuration, admittances are used rather than impedances because the "simple stub" arrangement consists in associating two elements in parallel (and we know that the admittances of parallel elements are added).

In the context of this PW, it will be necessary, as seen in the previous PWs, to realize the input and output impedance matching of the transistor by first canceling the imaginary part of the impedances presented by the transistor and secondly, by matching the real part of these impedances to a 50Ω load.

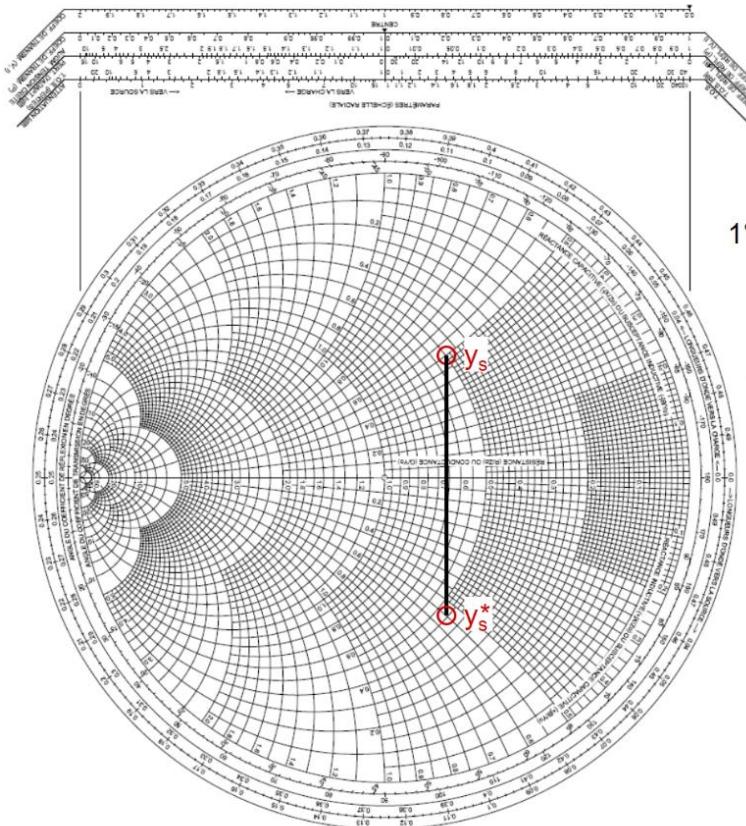
To cancel the imaginary part of the admittance, it is necessary to calculate the stub length that will be placed in parallel with the admittance (if the output of the packaged transistor presents an equivalent capacitive circuit : parallel resonant circuit) presented at the output of the transistor, in the case of the output impedance matching.



This stub makes possible to add to the output reactance of the transistor an imaginary part which cancels the total reactance. To calculate the stub length, we use the Smith chart in admittance on which we first localize the normalized admittance y_s . Do not forget that the Smith chart is inverted in this case with respect to the Smith chart with impedance format.



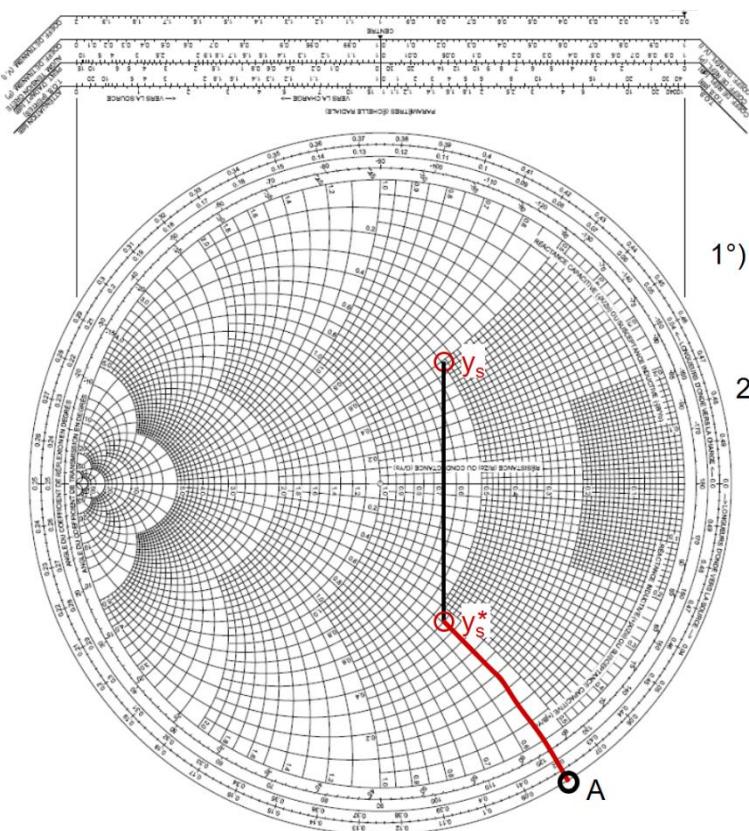
We then put the conjugate of y_s (i.e. y_s^*) on the Smith chart: it is the desired admittance of the stub we want to add.



1°) we locate $y_s=0.5-j0.5 \Omega$
on the Smith chart

2°) we locate $y_s^*=0.5+j0.5 \Omega$

The length of the stub (in terms of wavelength) is given on the outer edge of the Smith chart. Therefore, it is necessary to extend the arc of the imaginary part of y_s^* to the edge of the Smith chart (point A on the next figure).



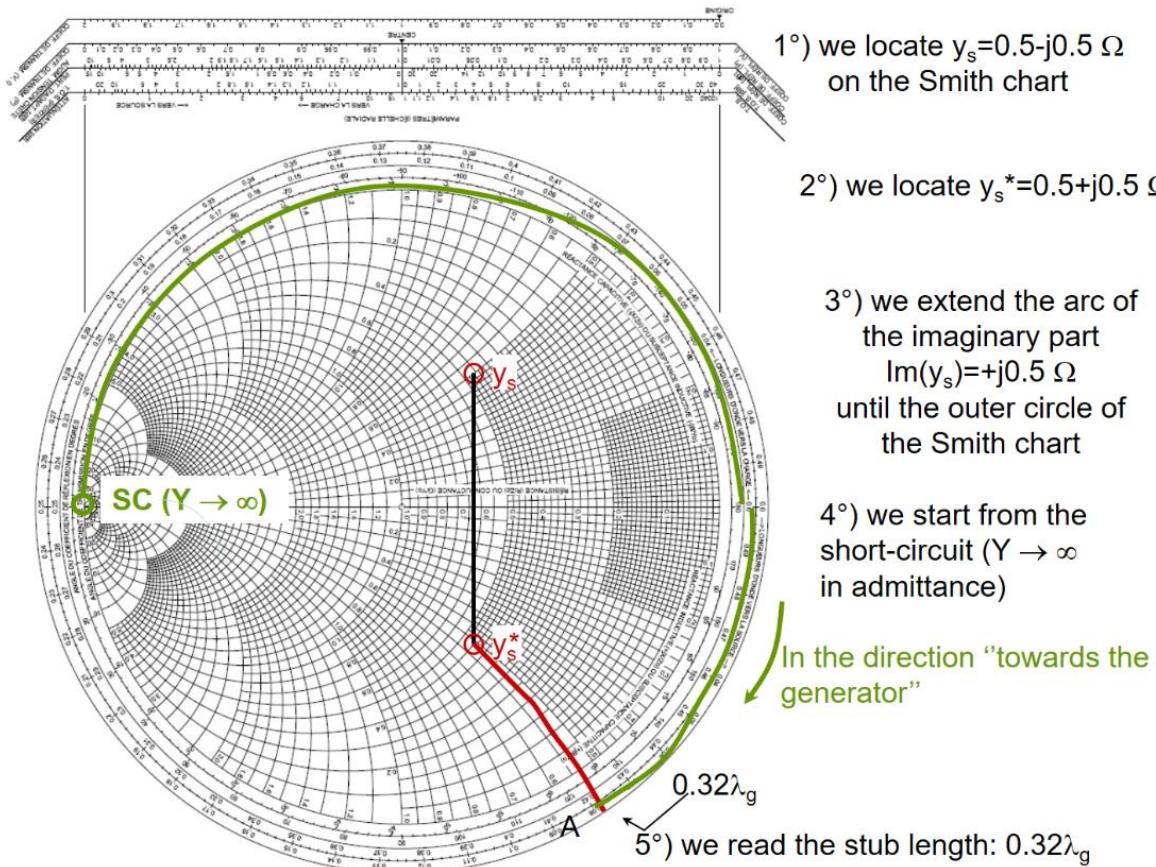
1°) we locate $y_s=0.5-j0.5 \Omega$
on the Smith chart

2°) we locate $y_s^*=0.5+j0.5 \Omega$

3°) we extend the arc of
the imaginary part
 $\text{Im}(y_s)=+j0.5 \Omega$
until the outer circle of
the Smith chart

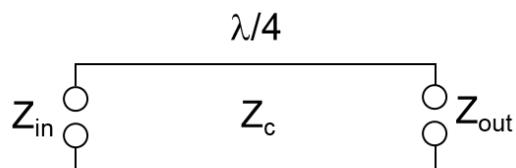
We can then use short-circuited or open-circuited stubs. At the frequency of 2 GHz, it is easier to create to short-circuited stub with a microstrip line by drilling the substrate to add a "via hole" connected to the rear face (in copper) of the PCB representing the circuit ground. The total imaginary part of the output admittance is therefore the one of the short-circuited stub added with the output reactance of the transistor itself.

Open-circuited stubs are also used but their values may have some imperfections in reason of the presence of a parasitic capacitance at the end of the stub instead of a perfect open circuit. To deduce the stub length, we start from the short circuit of the Smith chart and we rotate until reaching the A point "towards the generator". Be careful, the infinite admittance (i.e. corresponding to a short-circuit) is on the left of the admittance Smith chart (i.e. a Smith chart inverted with respect to the impedance Smith chart).



II.1.2 Impedance matching using a quarter wavelength transmission line

On a narrow band, a quarter-wave transmission line can play the role of an impedance transformer. This is what we use to transform the actual impedance toward a 50-ohm impedance.



The relationship between the output impedance Z_{out} , the characteristic impedance Z_c of the quarter-wave line and the input impedance Z_{in} is

$$Z_c = \sqrt{Z_{in} \times Z_{out}} \quad (3)$$

Indeed, if $l = \lambda / 4$, we have $\beta l = \frac{2\pi}{\lambda} \lambda / 4 = \frac{\pi}{2}$.

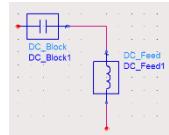
Inserting this in the general formula yields to:

$$Z_{in} = Z_c \frac{Z_{out} + jZ_c \tan\left(\frac{\pi}{2}\right)}{Z_c + jZ_{out} \tan\left(\frac{\pi}{2}\right)}$$

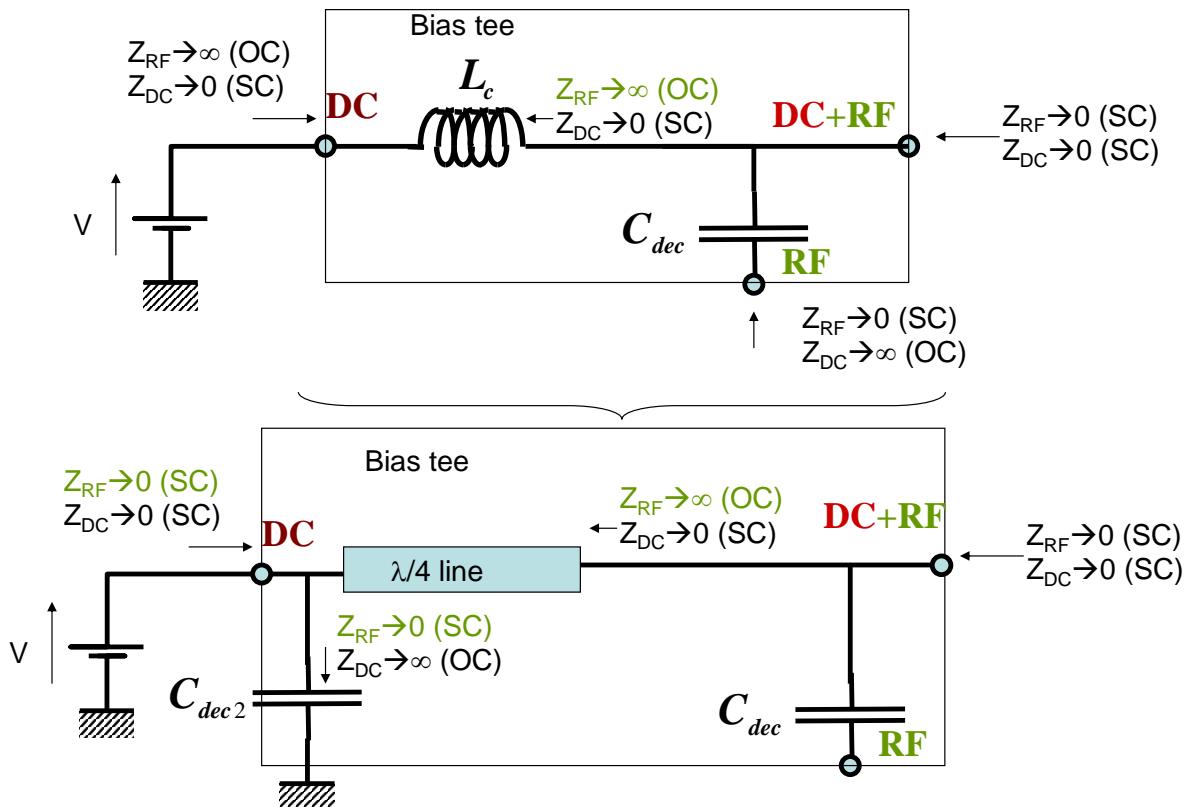
and we obtain $Z_{in} = Z_c \frac{Z_c}{Z_{out}}$ or $\mathbf{Z}_{in} = \frac{\mathbf{Z}_c^2}{\mathbf{Z}_{out}}$.

II.1.3 Use of a quarter-wave transmission line for Bias-Tees

During the design of the high-level amplifier (PW4), you have used ideal bias tees.



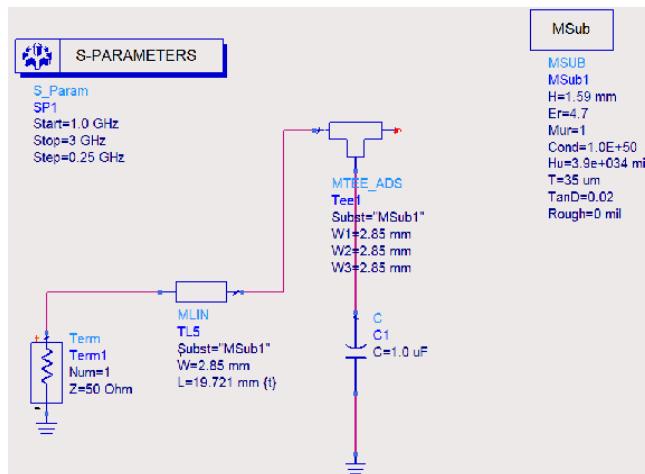
However, these tees are not feasible in practice. Quarter-wave lines are used to replace the "shock inductance" L_c according to the following scheme



The decoupling capacitance C_{dec} allows to short-circuit the RF signals transmitted by the quarter-wave line and also compensates the parasitic effects of the DC power supply. On the supply side, the quarter-wave line has no effect with respect to the DC signal but transforms the short-circuit related to the capacitance into a high impedance (i.e. open circuit) according to equation (3)

$$Z_{out} = \frac{Z_c^2}{Z_{in}} = \frac{50^2}{0} \rightarrow \infty \quad (4)$$

The following schematic shows the bias tee realized with the quarter-wave line and the localized capacitance of $1 \mu\text{F}$



During this PW, you will have to design this bias tee.

II.1.4 Technological structure

The circuit will be realized in microstrip technology with an FR4 glass epoxy (FR stands for flame retardant) substrate for practical reasons of availability and of cost (high-performance microwave substrates [glass-teflon, ceramic-teflon, alumina, etc ...] are indeed very expensive).

The main characteristics of the FR4 substrate you will use to print the designed amplifier are contained in the following table:

Relative permittivity (ϵ_r)	4.8
Substrate thickness (H)	1.59 mm
Copper thickness (T)	35 μm
Dielectric loss tangent (T_d)	0.025 @ 2GHz
Copper conductivity (Cond)	5.62^{e+07} Siemens/m
Copper surface roughness (Rough)	2.4 μm

During the simulations, it will therefore be necessary to define the FR4 substrate characteristics in the schematic page using the Msub component.

III MANIPULATION 1 : TRANSISTOR IMPEDANCE MATCHING (CLASS A)

III.1 SIMULATION AND ANALYSIS OF THE I/V CHARACTERISTICS OF THE TRANSISTOR

Using the schematic used in the previous PW “06.analysisDCext” that you will save as the 09.analyseDCext_packages_FET, plot the static I/V curves of the transistor. You must here delete the previously used transistor (“00.flu17xm_die”) and replace it with the “01.flu17xm_package” model in the library. The variation ranges for V_{DS} and V_{GS} voltages are chosen as follows:

- V_{GS} : from -3V to 0V with a step of 0.5V
- V_{DS} : from 0V to 10V with a step of 0.1V

Save your file and start the simulation. Examine the obtained results and give the value of the DC bias point to work in class A. Estimate then the maximum output power of the FET and the possible efficiency of the amplifier (in class A).

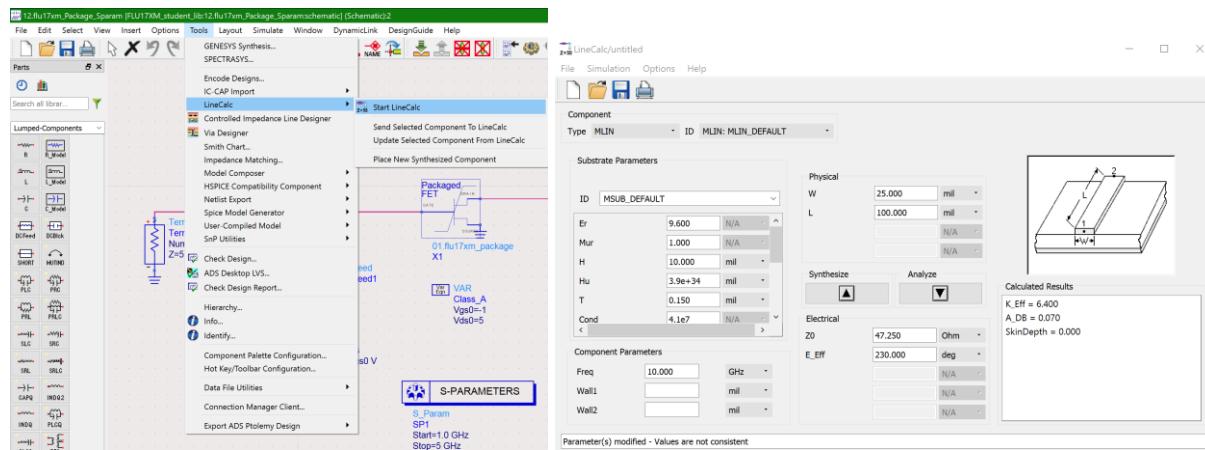
III.2 SIMULATION AND ANALYSIS OF THE S-PARAMETERS OF THE TRANSISTOR

Using the schematic you created in the previous PW to simulate the S parameters of the packaged transistor, plot the S-parameters of the “01.flu17xm_package” model using, at this point, the ideal bias tees (using “DC block” and “DC feed” elements).

Note the S-parameters (magnitude in dB and phase) of the FET at the frequency of 2GHz as well as the values of the impedances and admittances associated to the reflection parameters S_{11} and S_{22} .

III.3 COMPUTATION OF THE WIDTH OF A MICROSTRIP LINE OF 50Ω CHARACTERISTIC IMPEDANCE (FOR QUARTER-WAVE LINE AND STUB)

It is necessary to specify in the Msub component, the width of the microstrip lines that you will use to design a 50Ω characteristic impedance microstrip line. To do this, you will use the "Linecalc" tool of the Keysight ADS software.

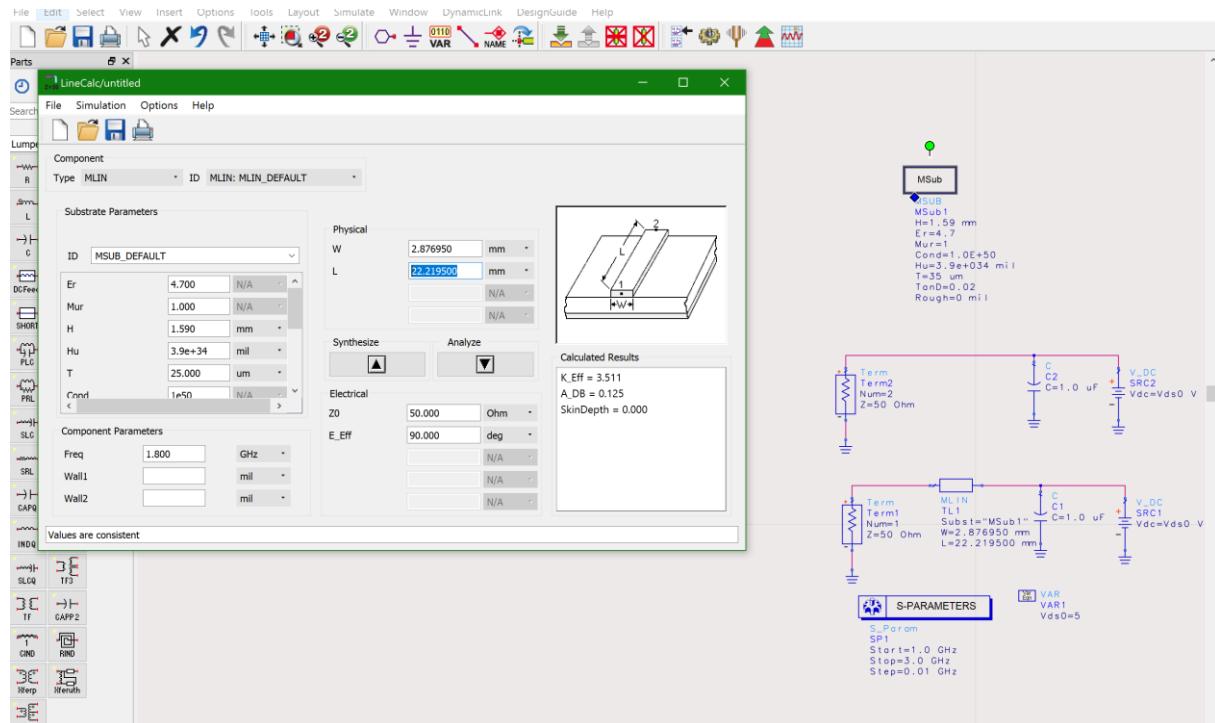


Using Linecalc, determine the width W of a 50-ohm quarter-wave line at 2 GHz. As we know that a line of length λ implies a phase shift “E_Eff” of 360° , what is the required length for a quarter-wave line?

III.4 REALISATION OF BIAS TEE IN MICROSTRIP TECHNOLOGY

III.4.1 Study of the bias tee alone.

You will use the previous calculations to visualize the behavior of a quarter-wavelength line used to achieve a bias tee at the frequency of 2 GHz. You have to reproduce the following schematic

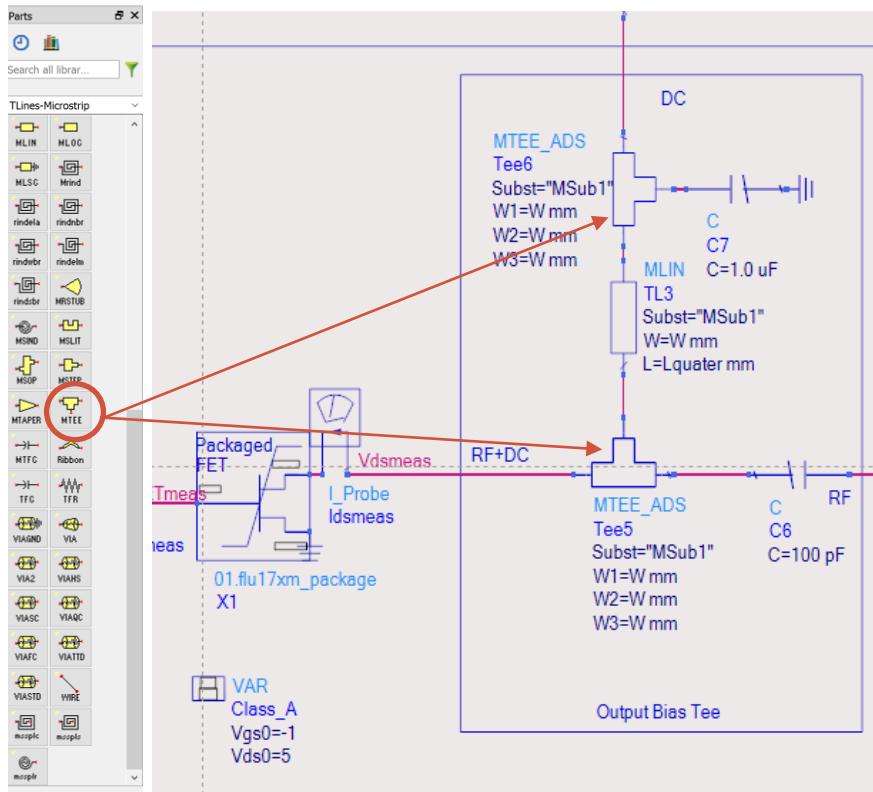


Start the "S-PARAMETER" simulation to compare the reflection coefficients of the $1\mu\text{F}$ decoupling capacitance with the configuration made of the same capacitance and of the quarter-wavelength transmission line with the width and the length previously found in section III.3.

Question : Is this schematic corresponding to the normal operation of a bias tee? What are the impedances at the RF frequency (i.e. 2 GHz) by the by capacitance alone and by the combination of the quarter-wave line and the capacitance?

It is worth noting that it will be necessary to add an additional section (TLines-Microstrip section, "MTEE_ADS" element) between the transistor, the bias tee and the output port of the bias tee (DC side) to design the layout. It will also be necessary to add this element on the DC access of the quarter-wave line in order to be able to connect the decoupling capacitance of the power supply (the capacitance required to compensate the parasitic effects of the power supply) as shown in the following figure for the drain. These junctions will be added to the grid and to the drain and can be found in the library "Tlines-Microstrip" shown in the following figure.

Finally, the internal decoupling capacity of the bias tee ("DC block" of the ideal tee under ADS), will be substituted by another capacitance must be added ("C4" in the following schematic).



To calculate the value of this capacitance, you will give the value of the desired impedance we want at the frequency of 2 GHz.

III.4.2 Study and simulation of the transistor using the microstrip bias tees

Start the "S-PARAMETER" simulation of the FLU17XM packaged transistor with two bias tees: one at the input (for V_{gs0}) and one at the output (for V_{ds0}) of the transistor. Be careful to insert them in opposite directions in order 1) to limit the parasitic couplings (not taken into account by ADS) between both quarter wavelength transmission lines when the final layout will be printed and 2) to make easier the soldering of the components. Set the DC bias point chosen previously.

Note the values of the admittances at the input and at the output of the setup including the transistor and both bias tees. Compare the results with the previous ones obtained with the ideal bias tees. Comments.

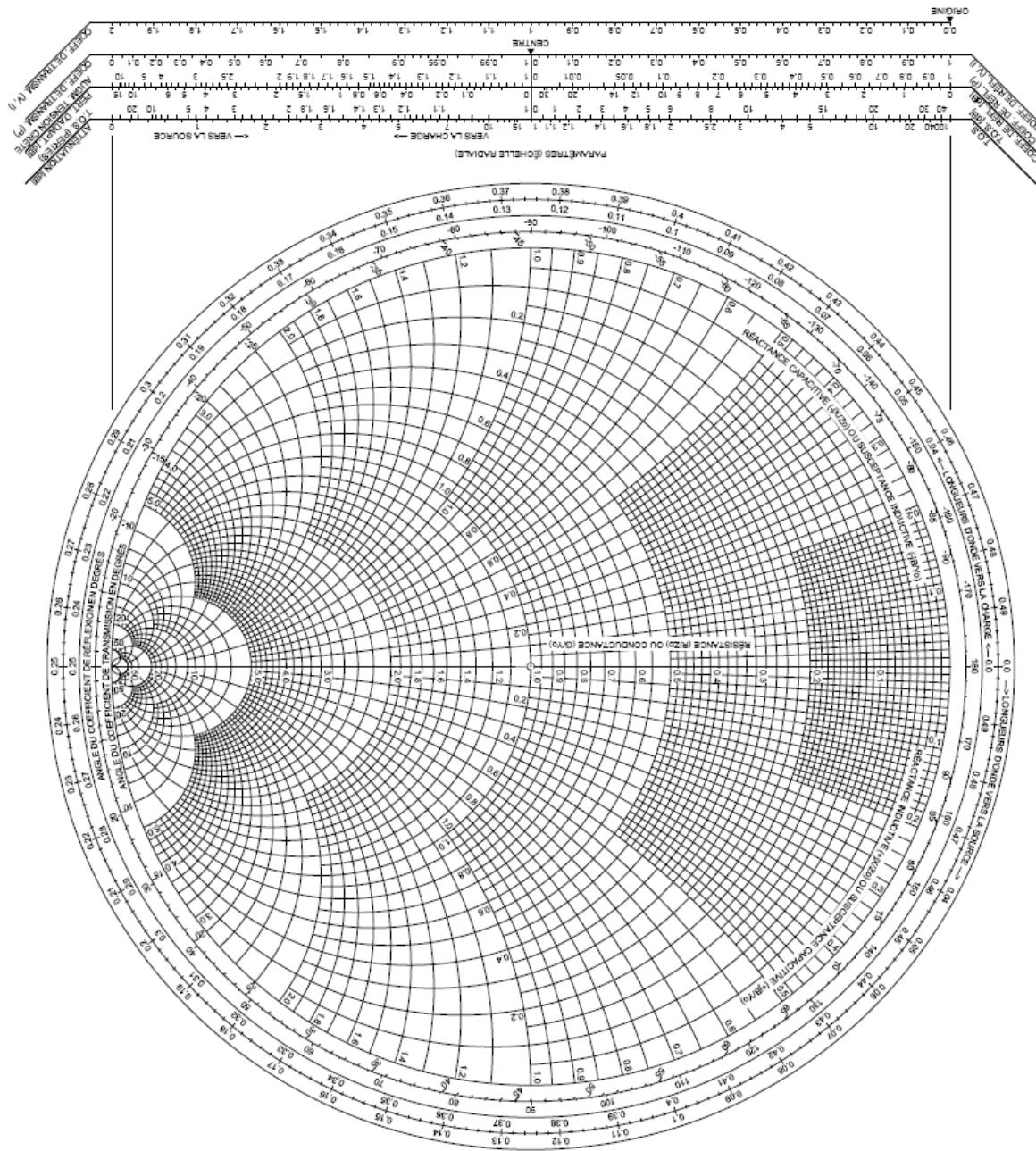
III.5 OUTPUT IMPEDANCE MATCHING

We want to match the output of the packaged FLU17XM field effect transistor to a purely real load $R_0 = 50 \Omega$. This impedance matching has to be achieved on a narrow band around the frequency of 2 GHz for a **low-level signal** (i.e. S-parameter simulations).

III.5.1 Cancellation of the imaginary part of the output admittance

Use the smith chart below to cancel the imaginary part of the admittance at the output of the circuit made of the transistor and the bias tees at the frequency of 2 GHz. To do this, you will use the admittance y_{out} or the impedance z_{out} found in the previous paragraph and you will follow the procedure described in paragraph II.1.1.

QUESTION : Give the length L_{out} of the stub used to cancel the imaginary part of the output admittance of the transistor. Insert this element in the ADS schematic and run the “S-parameter” simulation. Then use the tuning function to adjust this value in order to cancel as much as possible the imaginary part of the output admittance of the circuit. Note the updated value of the output admittance y_{out} and the corresponding output impedance z_{out} .



III.5.2 Matching of the real part of the output admittance

QUESTION : What element do we have to connect to match the real part of the output impedance to a 50Ω load? What should be the characteristic impedance and the length of the element found? You can help yourself with the theory presented in section II.1.2. Once these values calculated, you will use the "linecalc" tool to determine its width W_{out} . Insert this element in the ADS schematic and run the “S-parameter” simulation.



Use the tuning function to adjust the L_{out} and W_{out} values in order to have an output impedance of the circuit as close as possible to a 50Ω load. Note the updated value of the output admittance y_{out} and of the input admittance y_{in} or the input impedance z_{in} .

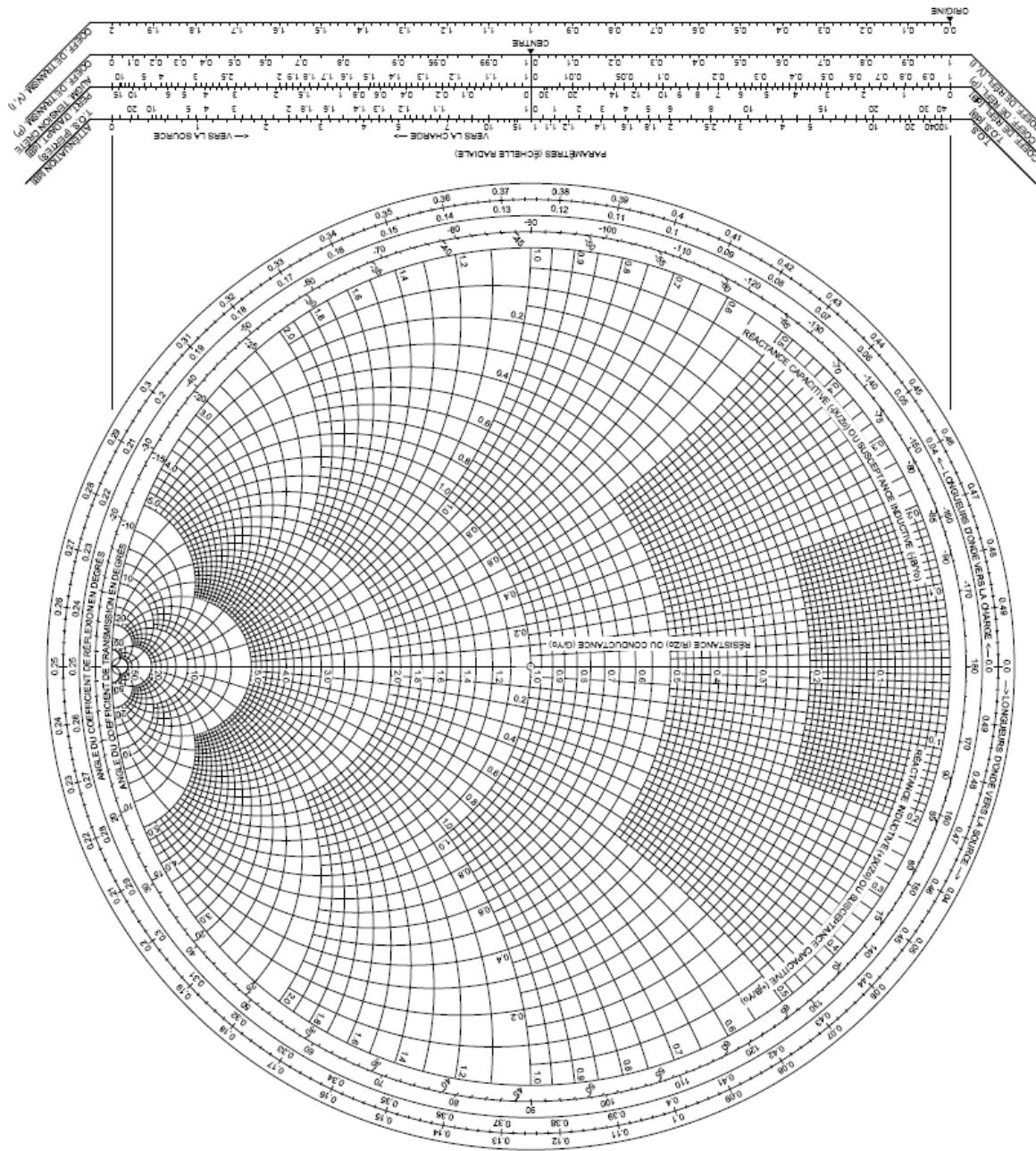
III.6 INPUT IMPEDANCE MATCHING

We want to match the input of the packaged FLU17XM field effect transistor (including both bias tees) to a generator having a purely real internal impedance $R_0 = 50 \Omega$. This has to be achieved on a narrow band around the frequency of 2 GHz for a **low-level signal** (i.e. S-parameter simulations).

III.6.1 Cancellation of the imaginary part of the input admittance

You have to use the Smith chart to cancel the imaginary part of the input admittance of the field effect transistor (including both bias tees) at the frequency of 2 GHz. To do so, you have to use the y_{in} admittance, or the input impedance z_{in} of the amplifier find at the previous paragraph and to follow the approach described in section II.1.1.

QUESTION : Give the length L_{in} of the stub used to cancel the imaginary part of the input admittance of the transistor. Insert this element in the ADS schematic and run the “S-parameter” simulation. Then use the tuning function (on L_{in} but also L_{out} and W_{out}) to adjust this value in order to cancel as much as possible the imaginary part of the input admittance of the circuit while keeping a satisfying output admittance. Note the updated value of the input admittance y_{in} and the corresponding input impedance z_{in} .



III.6.2 Matching of the real part of the input admittance

QUESTION : What element can we connect at the amplifier input in order to cancel the real part of its input admittance at the frequency of 2 GHz? What should be the characteristic impedance and the length of the element found? You can help yourself with the theory presented in section II.1.2. Once these values calculated, you will use the "linecalc" tool to determine its width W_{in} . Insert this element in the ADS schematic between the generator and the short-circuited stub and run the “S-parameter” simulation. Then use the tuning function (L_{in} ,

W_{in} , L_{out} and W_{out}) to obtain a satisfying input and output impedance matching of the created amplifier.

III.7 SIMULATION OF THE AMPLIFIER

In order to verify the performances of the simulated amplifier, you will launch a HARMONIC BALANCE simulation by inserting a P_1tone generator at the input of the amplifier. You will have to insert amperemeters at both the input and the output of the amplifier as well as voltage probes.

- Plot the following curves : $P_{out}=f(P_{in})$; $G_p=f(P_{in})$; $\eta_{aj}=f(P_{in})$. What efficiency do you obtain ? Comments.
- Plot the input and output impedances as a function of the frequency at the first three harmonic frequencies.
- Plot the load cycle of the transistor
- Plot the variation of the drain current of the transistor

These results will then be compared to the measurement results you will get in PW6 with your real amplifier once printed on the PCB.

IV MANIPULATION 2: LAYOUT CONCEPTION OF THE AMPLIFIER - REALISATION ON THE PCB PRINTER T-TECH

IV.1 PREPARATION OF THE AMPLIFIER LAYOUT

The components used to make this amplifier are CMS capacitances and a packaged transistor (see appendix). These components will be soldered on a FR4 substrate previously printed (only the microstrip lines will appear on one side). The rear face will serve as a ground, and SMA connectors will be placed at both access points of the amplifier.

You will now modify your schematic obtained during the final optimization of the amplifier circuit (i.e. the "schematic" used during the HARMONIC BALANCE simulation) in order to substitute the components to be soldered (capacitances and transistor) by "gaps" ("MGAP" element of the library "TLines-Microstrip"). They correspond in reality to spaces left to solder these components.

Concerning the CMS capacitances, you will measure their length to define the corresponding gap width. Concerning the transistor, you will look on the datasheet (see the appendix) the transistor dimensions to determine the gap width. Make sure here that the unit is in mm.



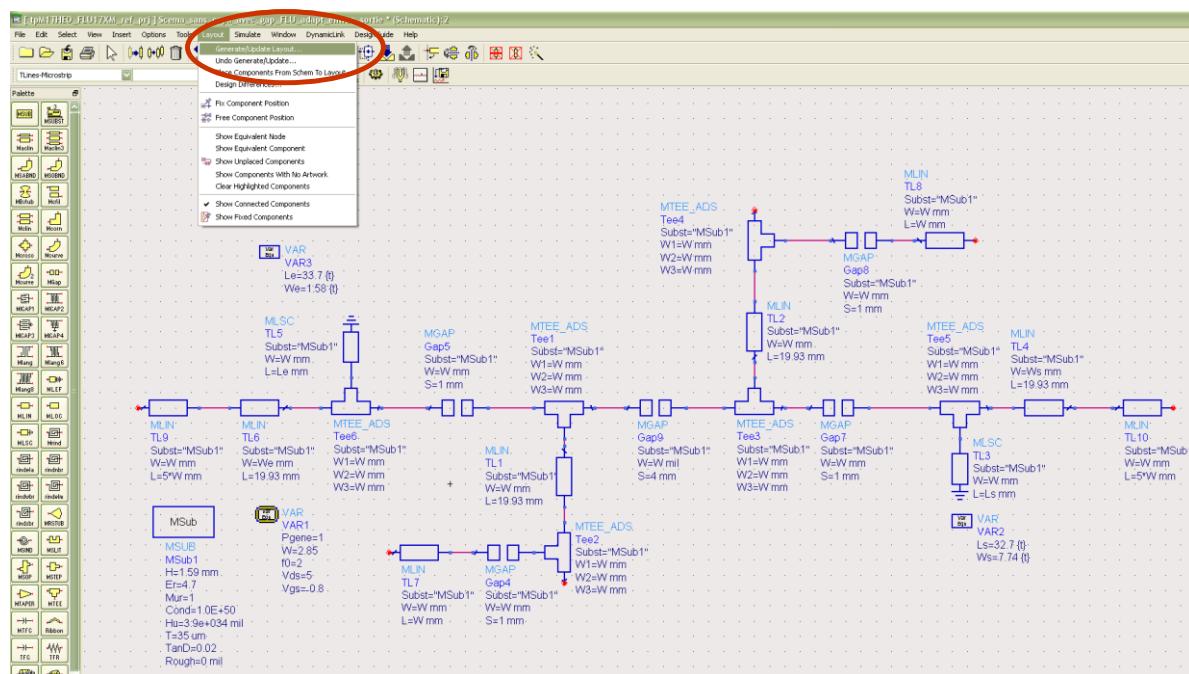
Concerning the short circuits of the stubs related to the bias tees, small additional line sections will be added ("MLIN" element of the "TLines-Microstrip" library), these lines having a length equal (at least) to the line width of $50\ \Omega$ characteristic impedance at 2 GHz. This will make easier the drilling of the plate and the short-circuit connections on the rear face of the PCB. In the via holes, you will insert small wires to make the connection between both metallized sides of the PCB (after soldering).

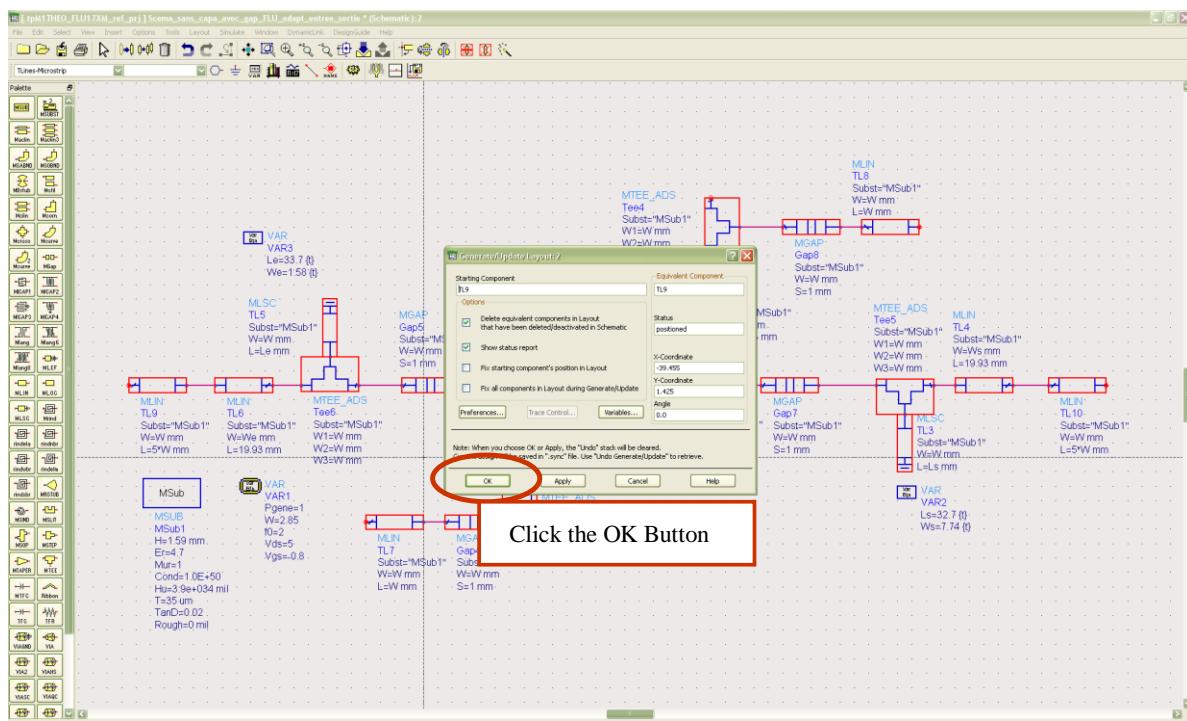
At the input and at the output of the amplifier, some small additional line sections (of $50\ \Omega$ characteristic impedance) will be added to facilitate the soldering of SMA connectors.

You can see on the booklet the final result of the layout you have to obtain.

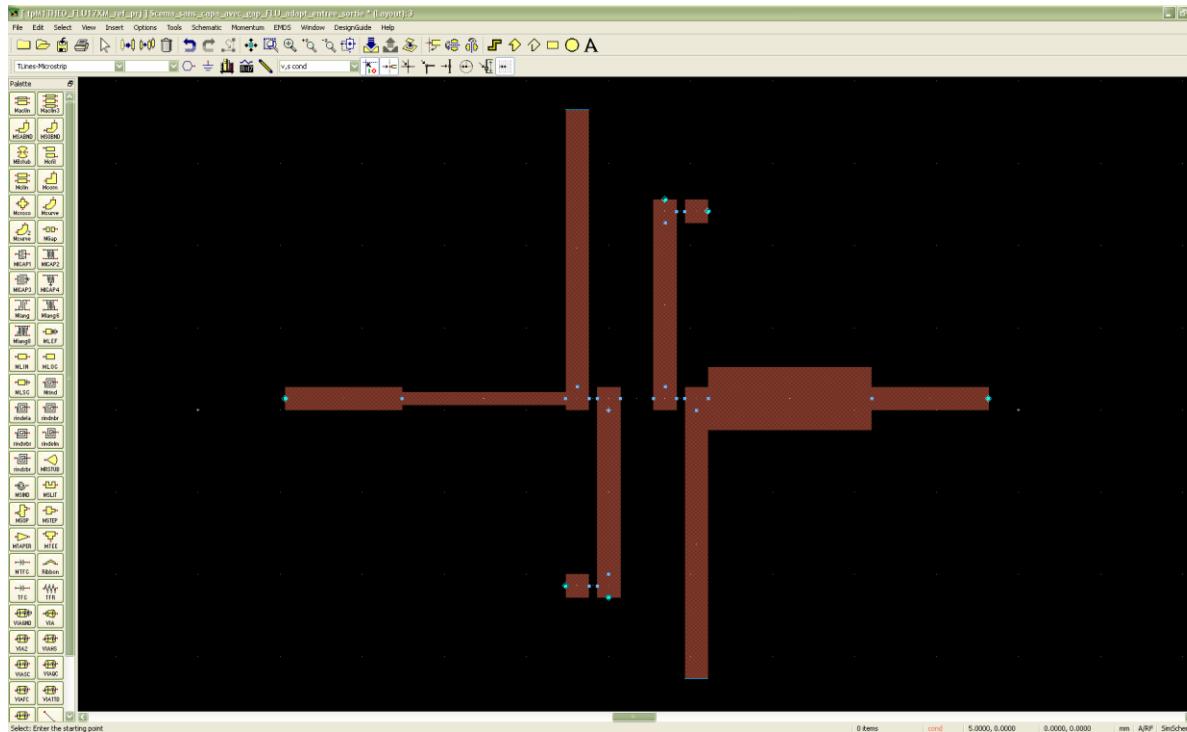
IV.2 CREATION OF THE AMPLIFIER LAYOUT

You will automatically create the layout of the amplifier as follows





You obtain the following window



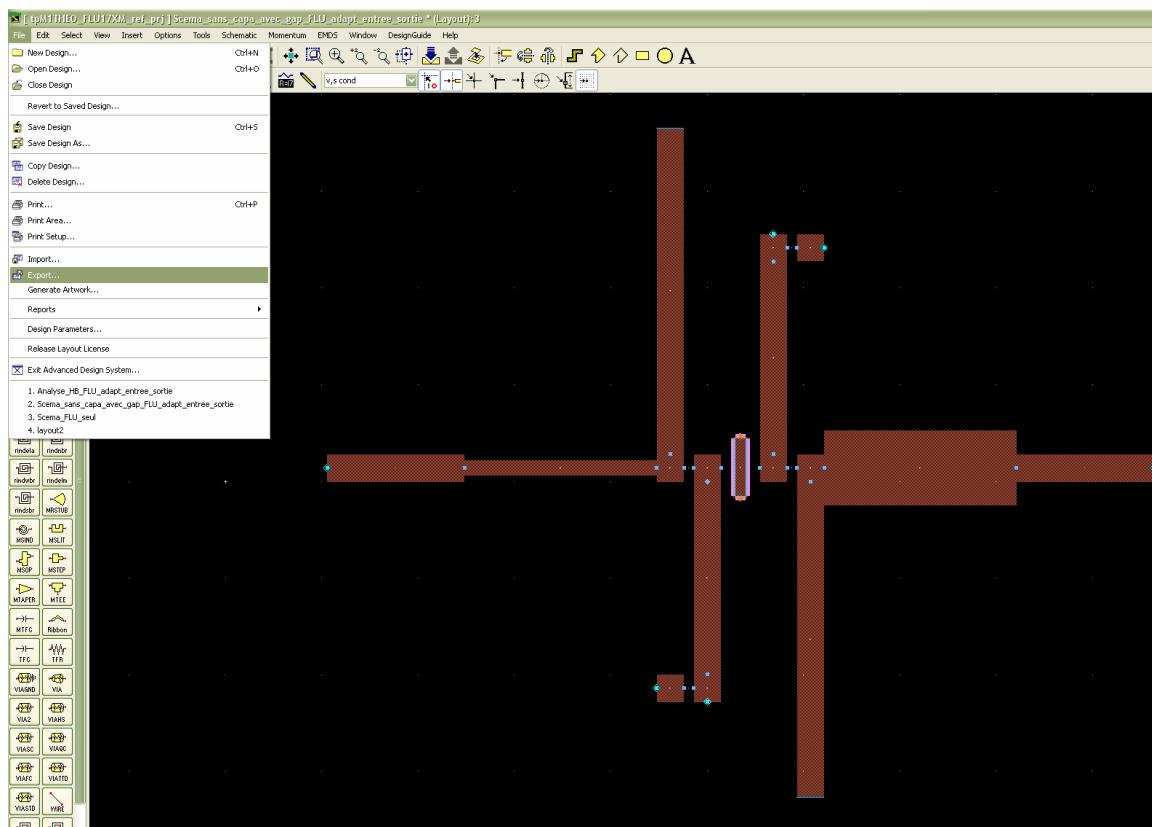
It is necessary to add a line section below the transistor to be able to connect the transistor source to the ground. On the documentation, these accesses are on both sides of the transistor. You will locate a line section of sufficient length to be able to solder it easily and to

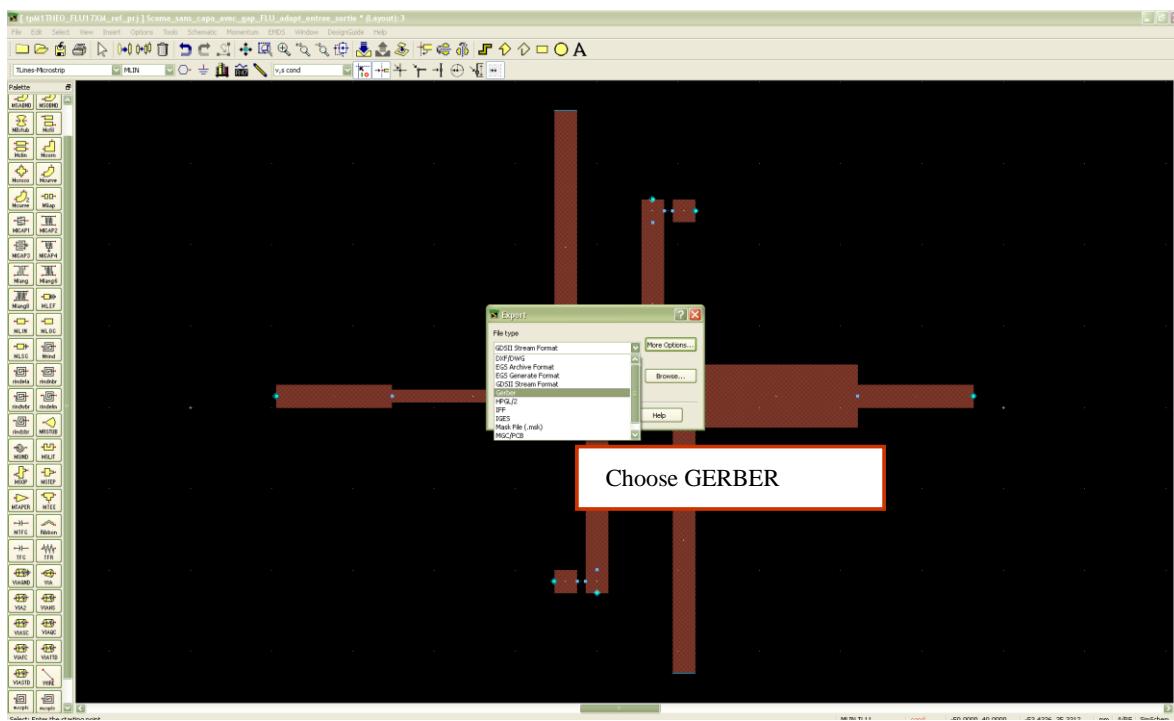


be able to drill the "via hole" easily. Do not do it too long to avoid an unwanted coupling with the stubs.

IV.3 CREATION OF THE GERBER FILE

Here, you will create a GERBER file that you will use on the ISOPRO software that allows you to control the PCB printer



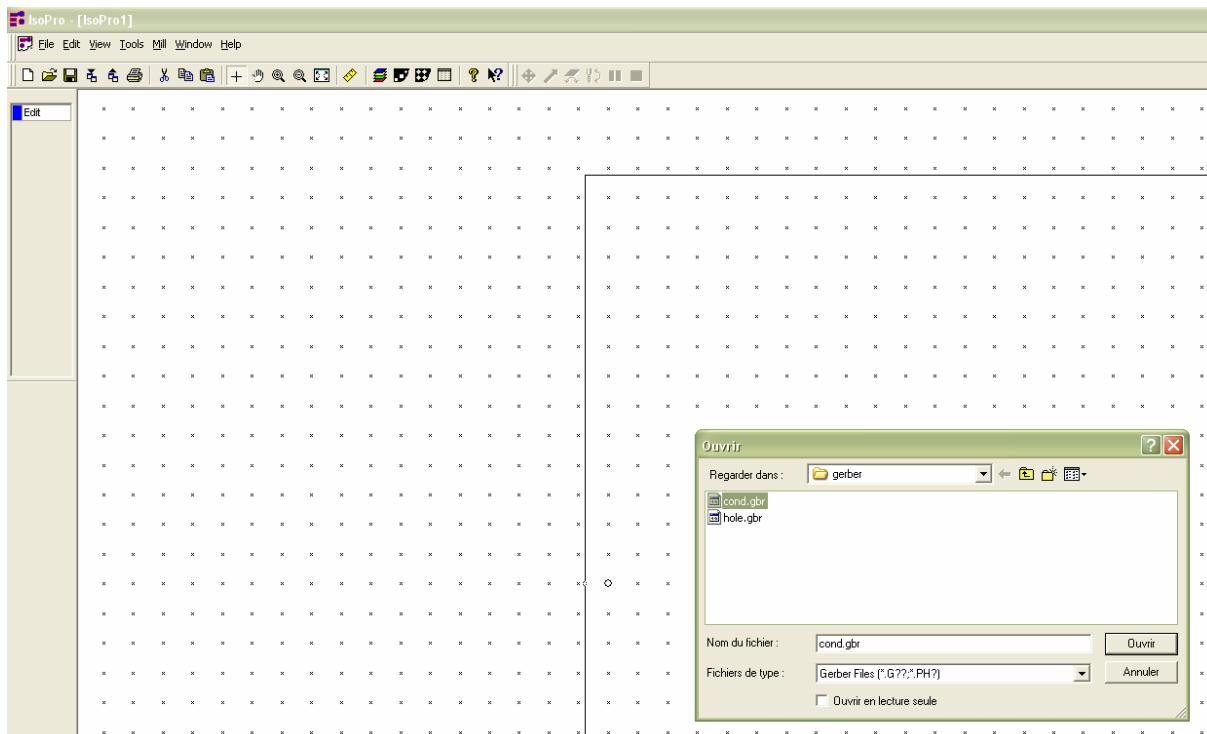
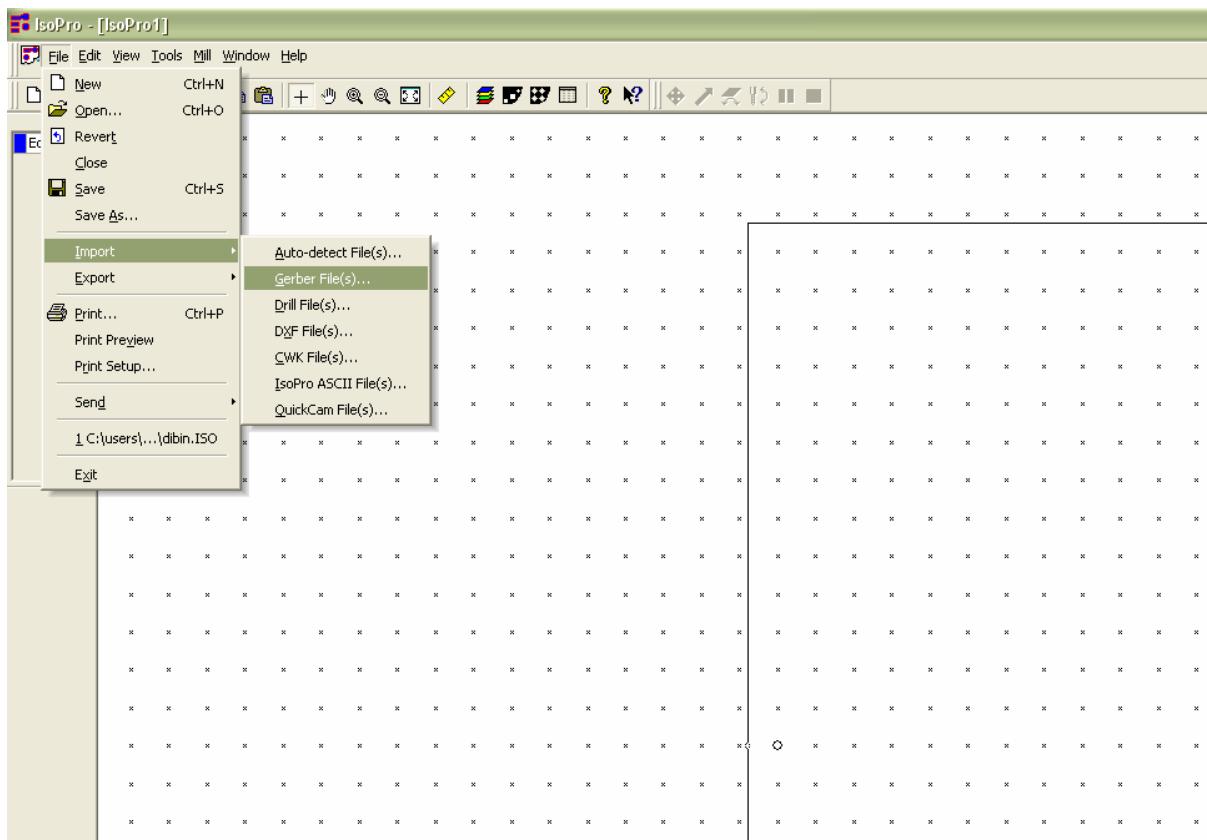


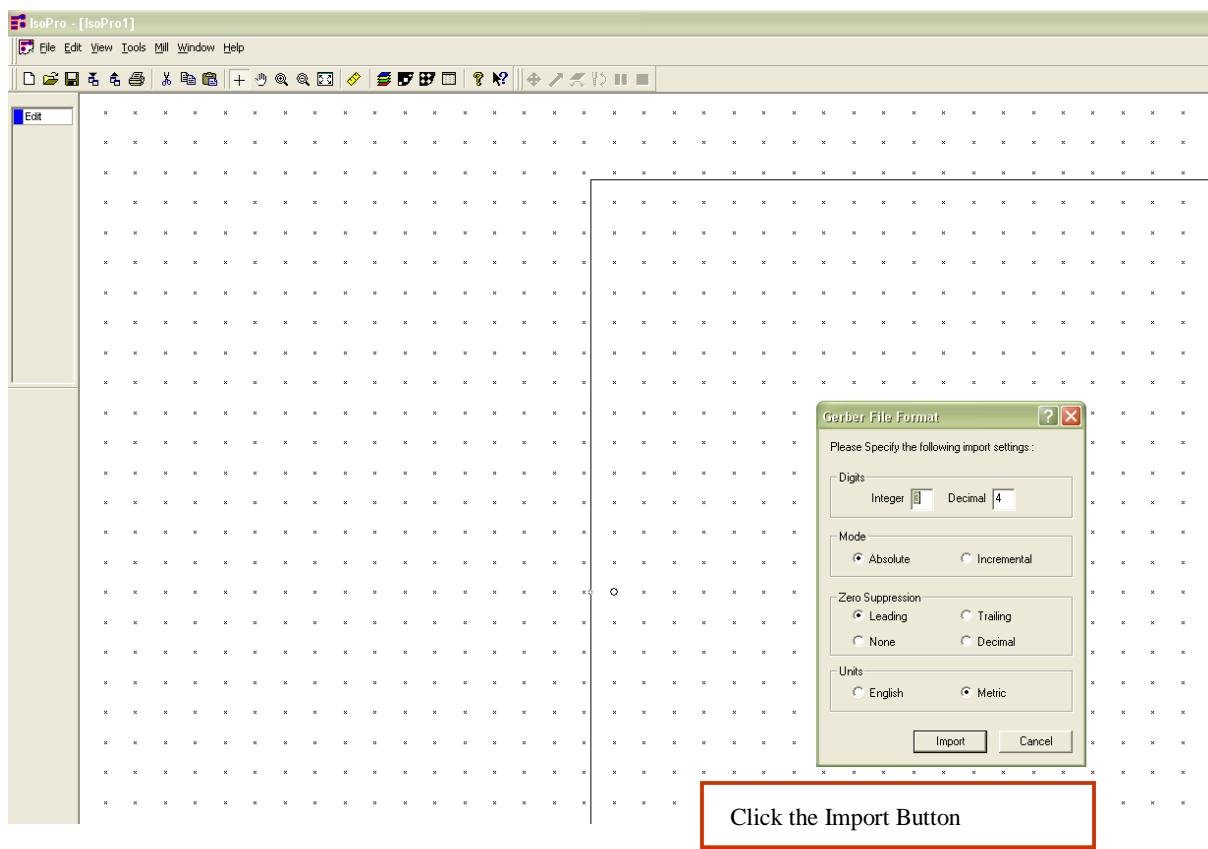
IV.4 USE OF THE ISOPRO SOFTWARE AND OF THE PCB PRINTER T-TECH.

After the creation of the layout with ADS, you will use the ISOPRO software which makes it possible to monitor the PCB printer.

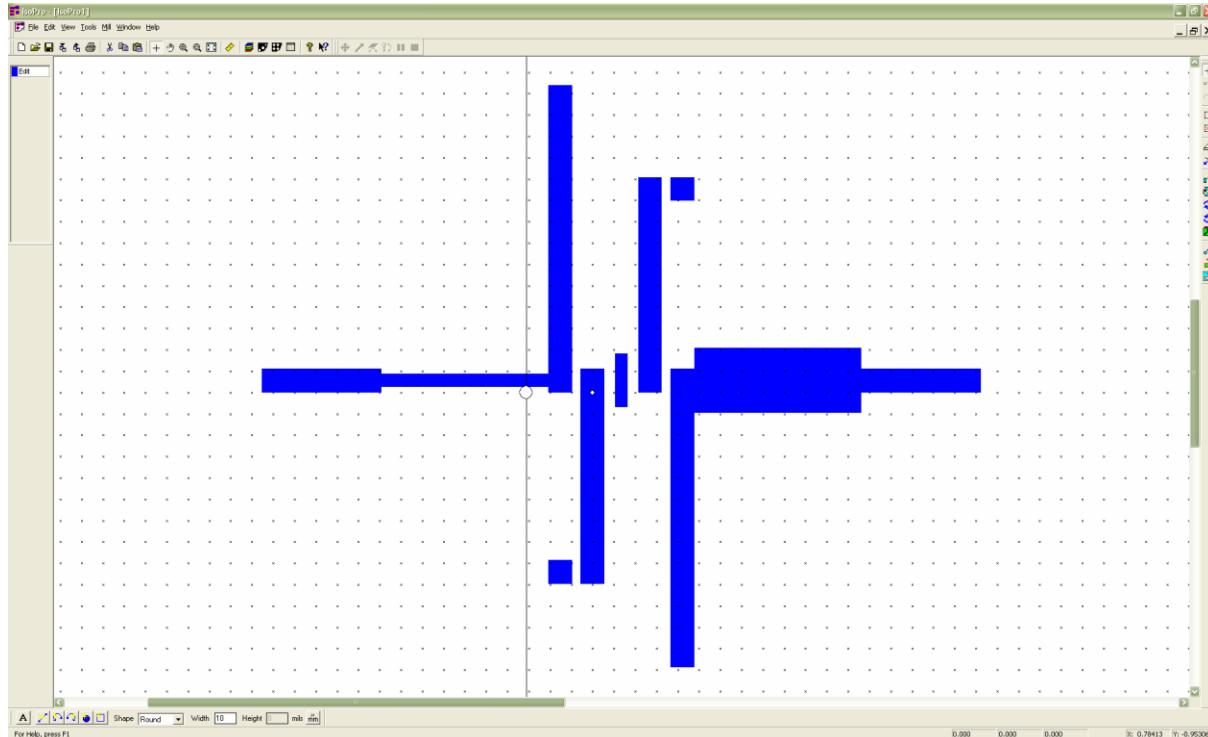
IV.4.1 Importation of the created files on ADS

Select the menu "File/Import/Gerber File(s)" to import the GERBER file. Select the file "cond.gbr" that you have placed in the working directory. After clicking on Open, a window appears where it is necessary to use again the configuration of ADS if required.



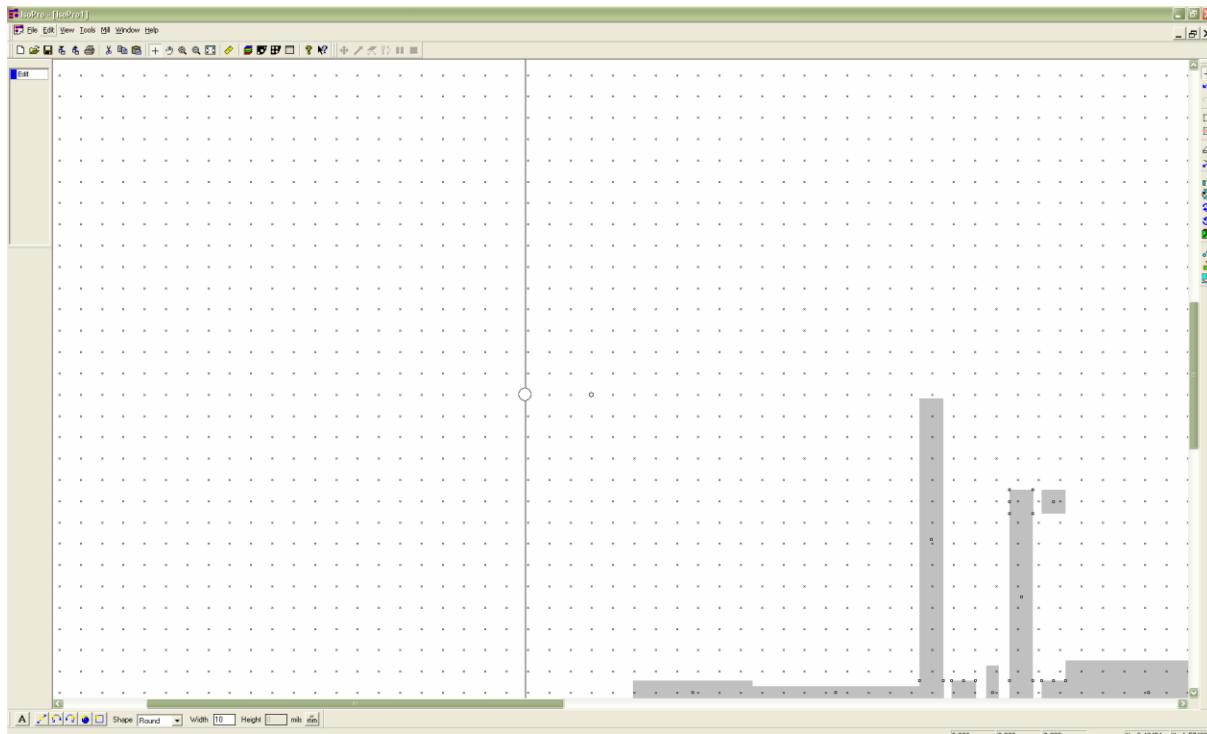


You find here the layout of your circuit

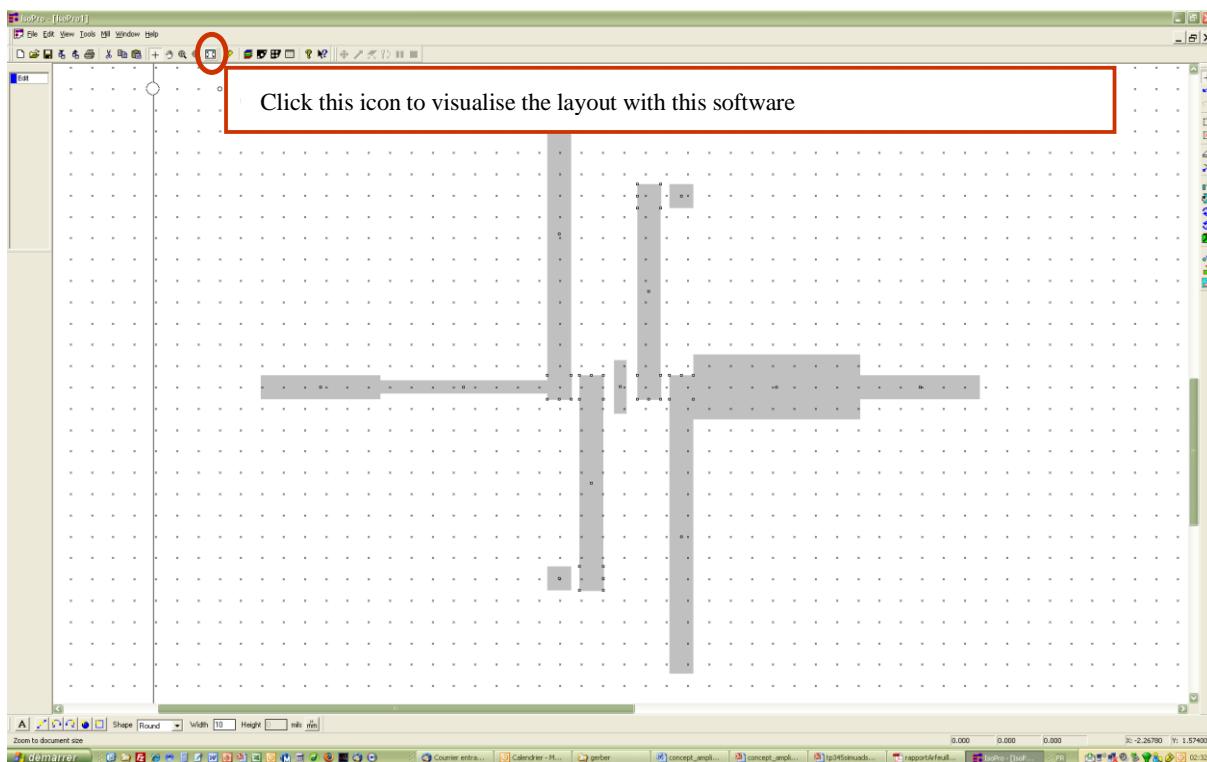




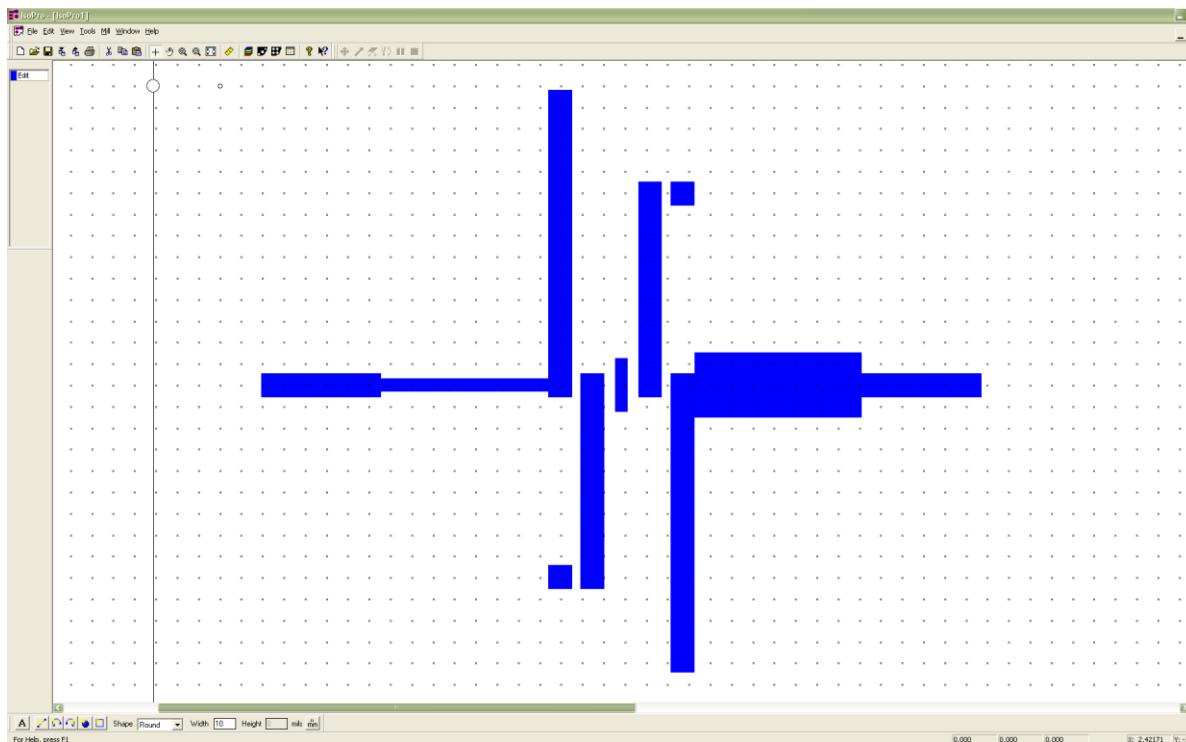
It is necessary to move this layout which is not centered with respect to the PCB printer system of axis. Select the entire mask and move it down to the right



Click on this icon  to see the entire layout



Press on ‘‘ESC’’ and the layout appears in blue color



At the top left, you can find the description and the operating mode of the conductor layer that the machine must leave on the plate. This layer can work in different modes (by clicking on the left button of the mouse on this menu): ‘‘Edit’’ mode, ‘‘View’’ mode or ‘‘Hide’’ mode.

IV.4.2 Layout realization

The procedure is given in the booklet available in the lab room and annexed to this text.

V ANNEX : TRANSISTOR DATASHEET

FLU17XM

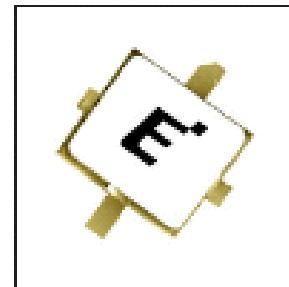
L-Band Medium & High Power GaAs FET

FEATURES

- High Output Power: $P_{1dB}=32.5\text{dBm}$ (Typ.)
- High Gain: $G_{1dB}=13.5\text{dB}$ (Typ.)
- High PAE: $\eta_{add}=48\%$ (Typ.)
- Hermetic Metal/Ceramic (SMT) Package
- Tape and Reel Available

DESCRIPTION

The FLU17XM is a GaAs FET designed for base station applications in the PON/PCS frequency range. This is a new product series that uses a surface mount package that has been optimized for high volume cost driven applications.



Eudyna stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature $T_a=25^\circ\text{C}$)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_T	$T_a = 25^\circ\text{C}$	7.5	W
Storage Temperature	T_{stg}		-65 to +175	°C
Channel Temperature	T_{ch}		+175	°C

Eudyna recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain - source operating voltage (V_{DS}) should not exceed 10 volts.
2. The forward and reverse gate currents should not exceed 0.6 and -1.0 mA respectively with gate resistance of 200Ω.
3. The operating channel temperature (T_{ch}) should not exceed +45°C.

ELECTRICAL CHARACTERISTICS (Ambient Temperature $T_a=25^\circ\text{C}$)

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Drain Current	I_{DS}	$V_{DS} = 5\text{V}$, $V_{GS}=0\text{V}$	-	600	900	mA
Transconductance	gm	$V_{DS} = 5\text{V}$, $I_{DS}=400\text{mA}$	-	300	-	mS
Pinch-Off Voltage	V_p	$V_{DS} = 5\text{V}$, $I_{DS}=30\text{mA}$	-1.0	-2.0	-3.5	V
Gate-Source Breakdown Voltage	V_{GSO}	$I_{GS} = 30\mu\text{A}$	-5	-	-	V
Output Power at 1 dB G.C.P.	P_{1dB}	$V_{DS} = 10\text{V}$	91.5	92.5	-	dBm
Power Gain at 1 dB G.C.P.	G_{1dB}	$f=2.0\text{ GHz}$ $I_{DS}=0.6\text{A}$	12.5	13.5	-	dB
Power Added Efficiency	η_{add}		-	46	-	%
Thermal Resistance	R_{th}	Channel to Case	-	15	20	°C/W

Case Style: XM

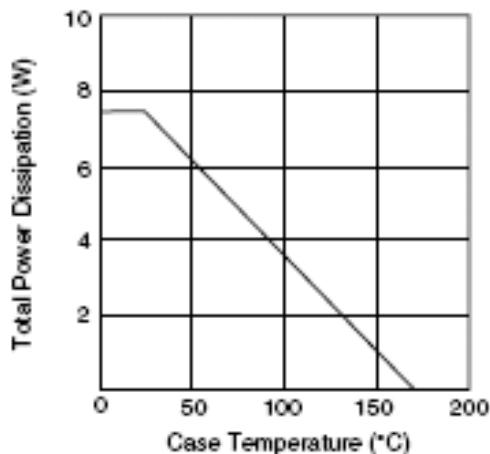
G.C.P.: Gain Compression Point

Note: The RF parameters are measured on a lot basis by sample testing
at an AQL = 0.1%, Level-II inspection. Any lot failure shall be 100% retested.

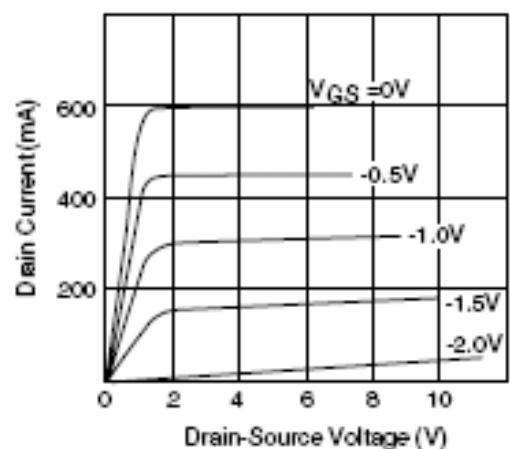
FLU17XM

L-Band Medium & High Power GaAs FET

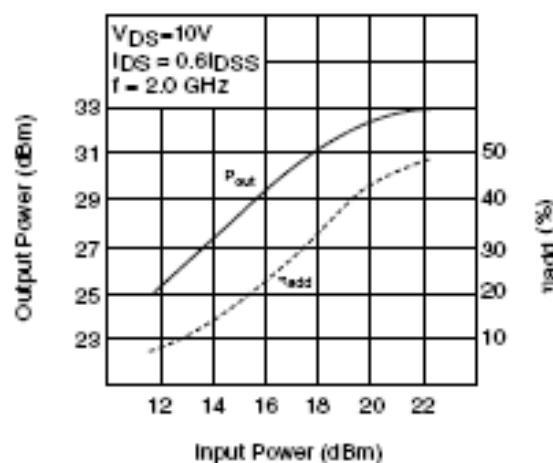
POWER DERATING CURVE



DRAIN CURRENT vs. DRAIN-SOURCE VOLTAGE

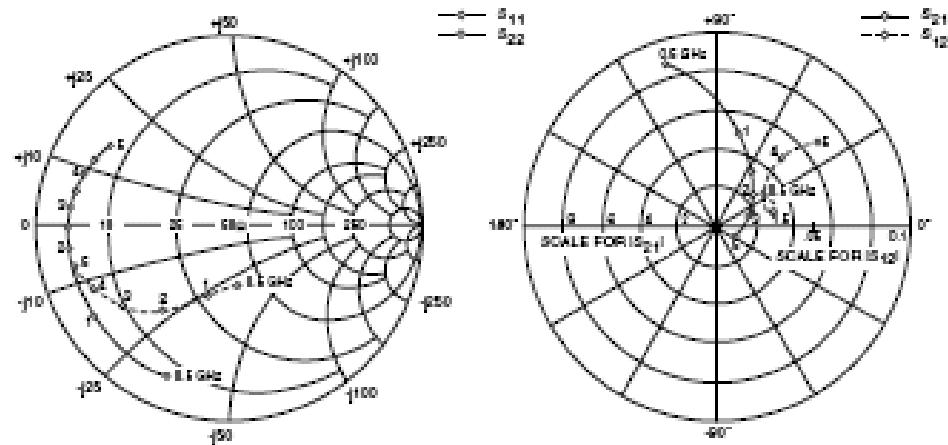


OUTPUT POWER vs. INPUT POWER



FLU17XM

L-Band Medium & High Power GaAs FET



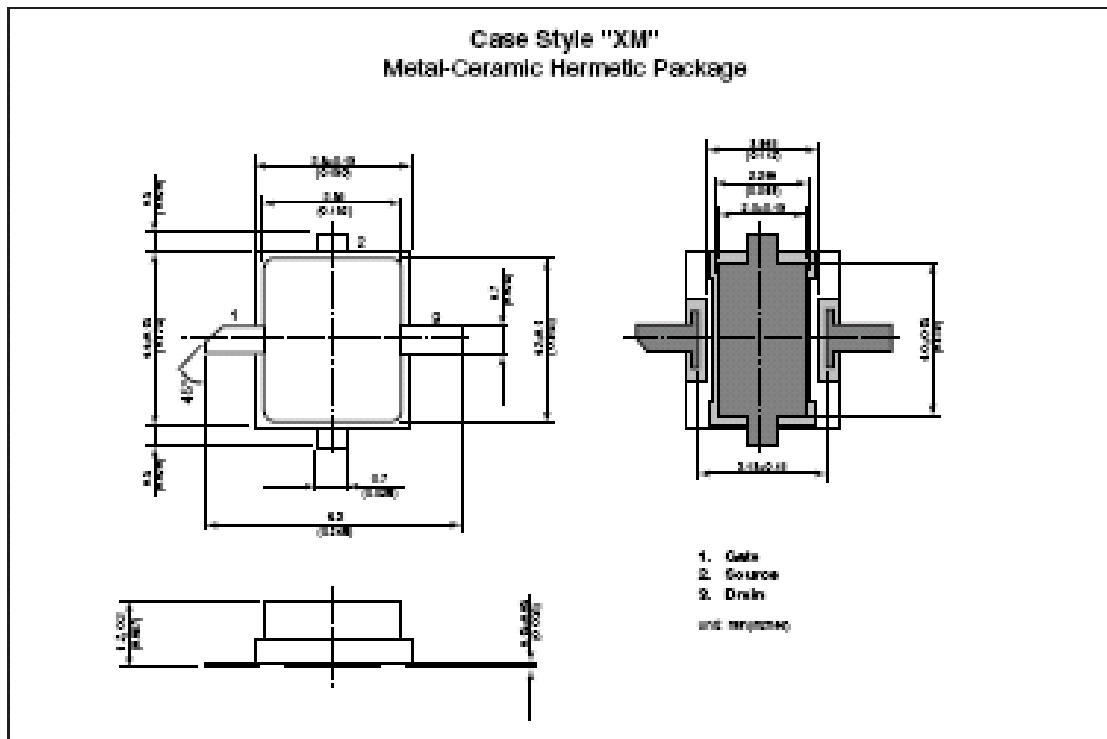
S-PARAMETERS
 $V_{DS} = 10V$, $I_{DS} = 380mA$

FREQUENCY (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	.864	-33.9	18.330	160.4	.012	72.2	.395	-16.7
500	.839	-112.8	8.817	107.0	.028	39.4	.307	-80.7
1000	.831	-148.9	4.930	78.0	.030	18.4	.378	-105.7
1500	.824	-152.5	3.299	58.2	.029	16.8	.472	-119.8
2000	.825	-172.5	2.428	42.0	.027	21.1	.555	-128.3
2500	.825	179.7	1.912	28.1	.028	35.2	.628	-135.0
3000	.820	172.8	1.587	15.2	.032	39.3	.682	-143.3
3500	.809	165.9	1.337	9.3	.038	43.3	.726	-149.3
4000	.794	159.2	1.183	-8.3	.048	45.0	.781	-155.1
4500	.775	152.5	1.079	-19.8	.057	43.5	.790	-160.5
5000	.759	145.6	1.015	-32.1	.067	39.4	.816	-166.9

[Download S-Parameters, click here](#)

FLU17XM

L-Band Medium & High Power GaAs FET





**PRACTICAL WORK
PW5:
DESIGN OF A LINEAR AMPLIFIER AT 2GHZ
USINKEYSIGHT ADS**

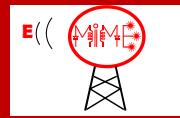
- Student Help Manual for PW 3, 4 and 5

Copy to be left
on site



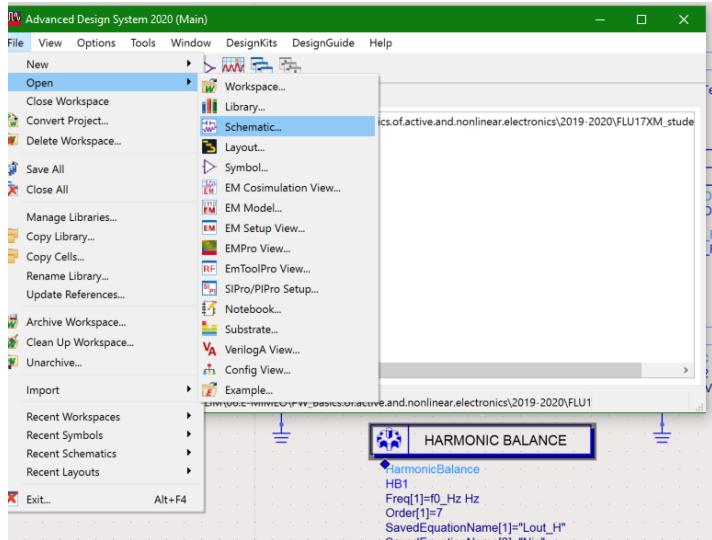
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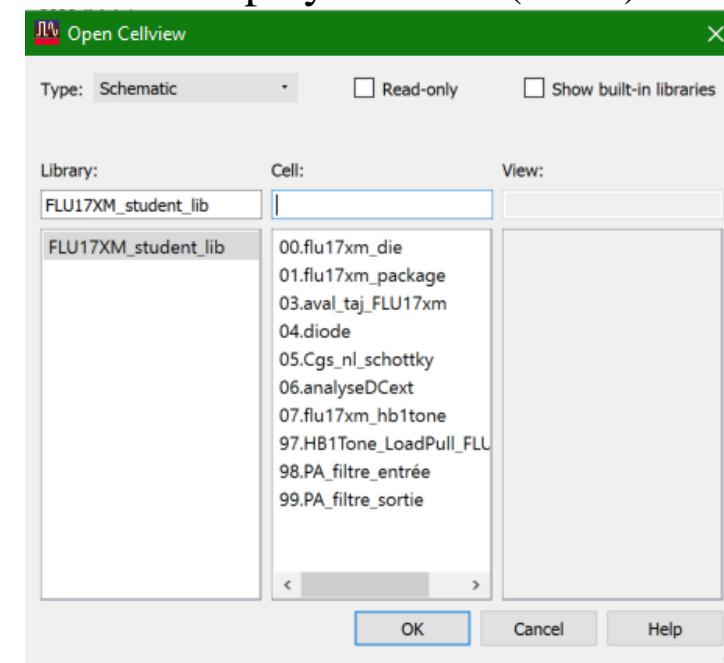


This booklet presents the architecture of the ADS project you will use.

After launching ADS, click on *file/open Schematic* to obtain the following list of schematics :

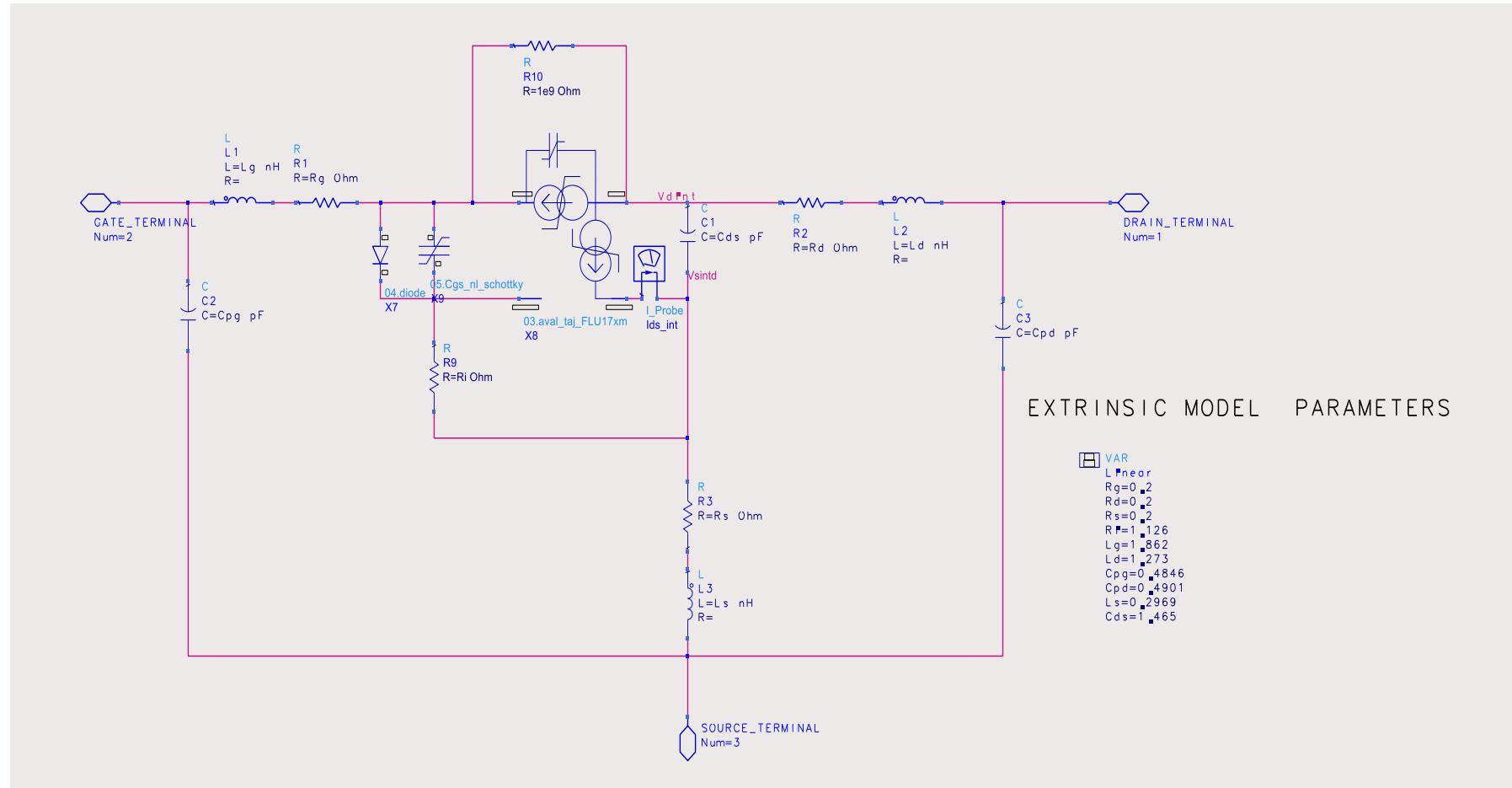


Each schematic file (*.dsn) is detailed hereafter as well as the corresponding data display window (*.dds).

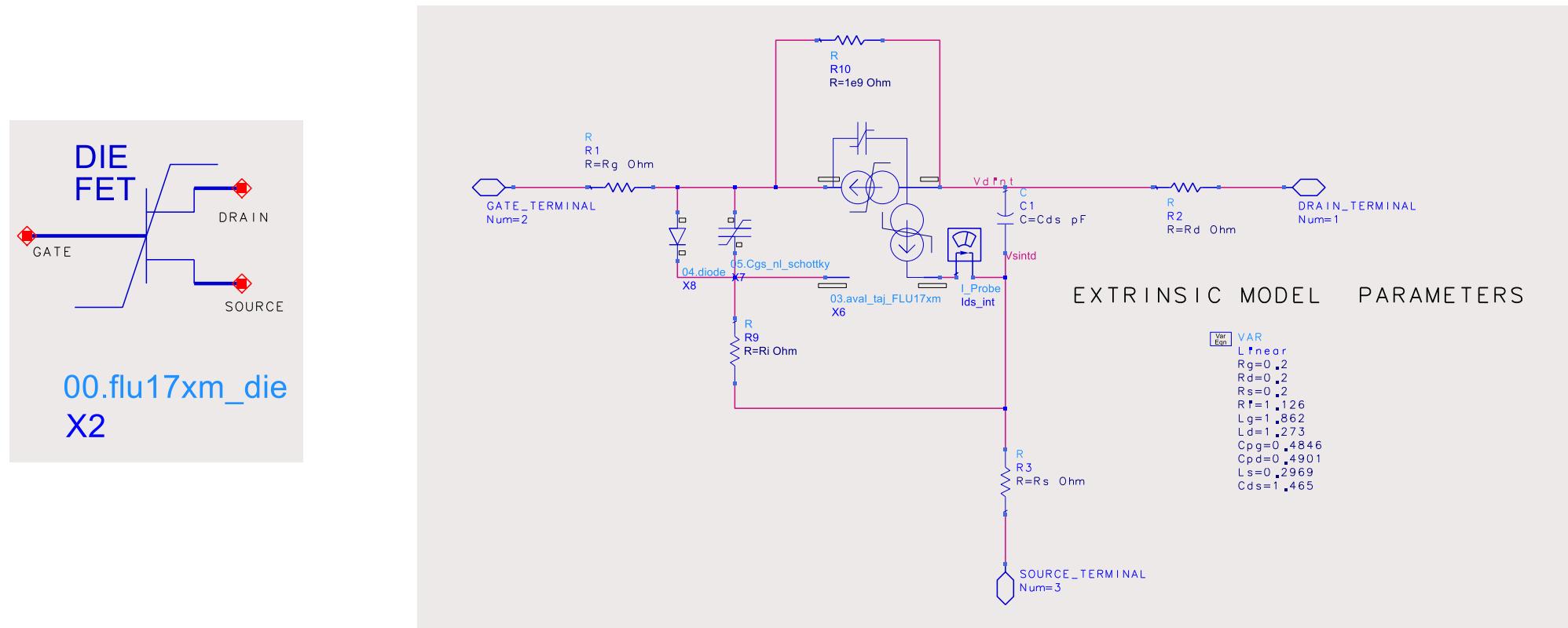




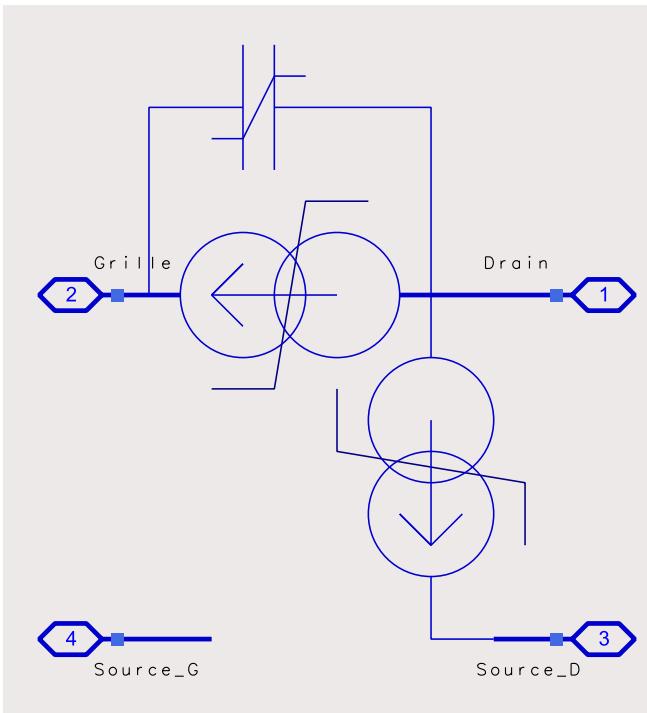
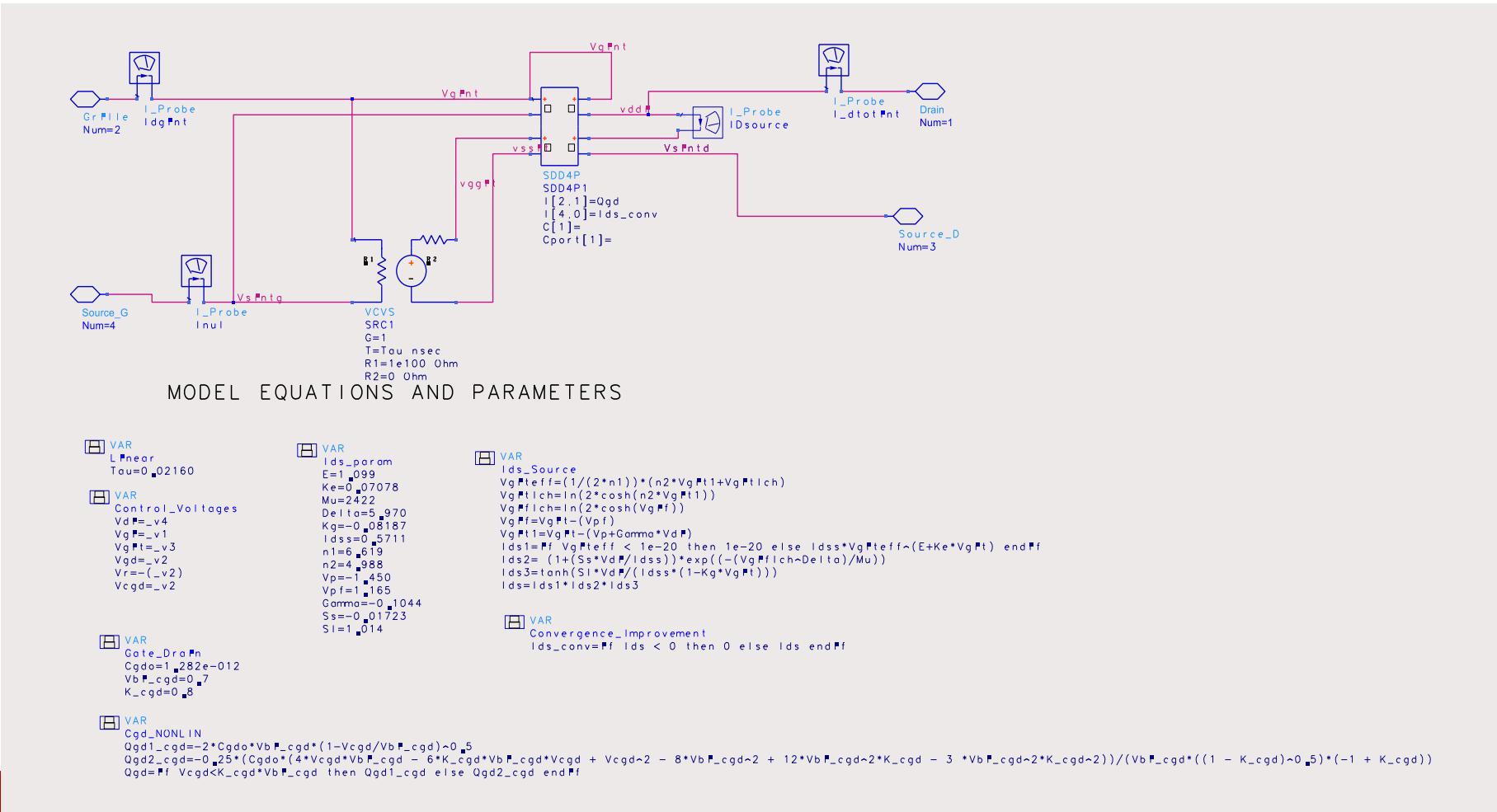
The *01.flu17xm_package.dsn* file defines the non-linear packaged model of the FET. The figure below represents the symbol associated to this model (and to this file). You can click on *Window/symbol* in the *Window* menu.



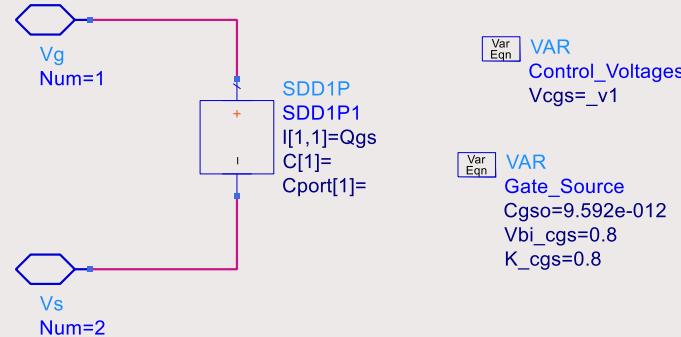
The *00.flu17xm_package.dsn* file defines the non-linear packaged model of the FET. The figure below represents the symbol associated to this model (and to this file). You can click on *Window/symbol* in the *Window* menu.



The *aval_taj.dsn* file defines the non-linear intrinsic model of the FET. The figure below represents the symbol associated to this model (and to this file). You can click on *Window/symbol* in the *Window* menu.



Cgs Non linear EQUATIONS AND PARAMETERS

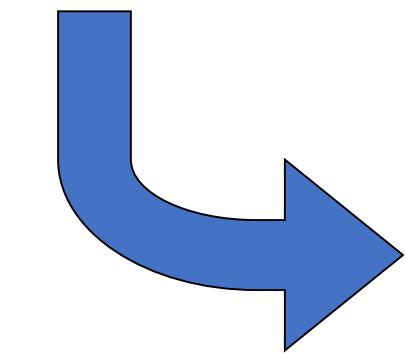


Var Eqn
Control_Voltages
 $V_{cgs} = v_1$

Var Eqn
Gate_Source
 $C_{gso} = 9.592e-012$
 $V_{bi_cgs} = 0.8$
 $K_{cgs} = 0.8$

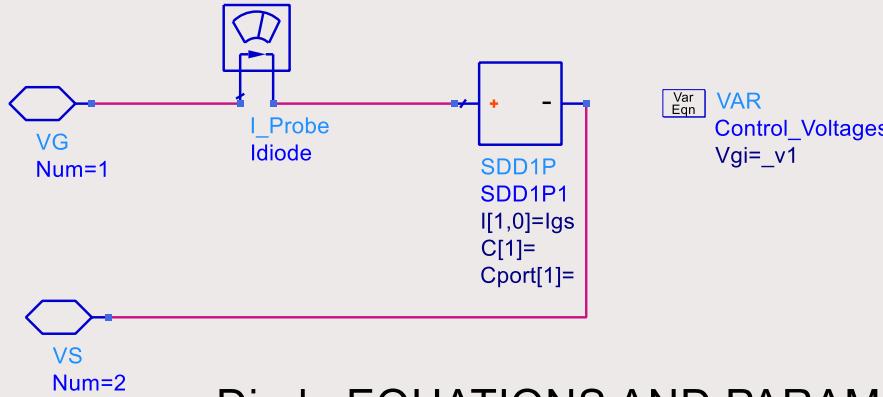
Var Eqn
VAR
Cgs_NONLIN
 $Q_{gs1_cgs} = -2 * C_{gso} * V_{bi_cgs} * (1 - V_{cgs} / V_{bi_cgs})^{0.5}$
 $Q_{gs2_cgs} = -0.25 * (C_{gso} * (4 * V_{cgs} * V_{bi_cgs} - 6 * K_{cgs} * V_{bi_cgs} * V_{cgs} + V_{cgs}^2 - 8 * V_{bi_cgs}^2 + 12 * V_{bi_cgs}^2 * K_{cgs} - 3 * V_{bi_cgs}^2 * K_{cgs}^2)) / (V_{bi_cgs} * ((1 - K_{cgs})^{0.5} * (-1 + K_{cgs}))$
 Qgs1 if $V_{cgs} < K_{cgs} * V_{bi_cgs}$ else Qgs2 endif

The *Cgs_nl_schottky.dsn* file defines the non-linear model of the C_{GS} capacitance of the FET.



Associated symbol



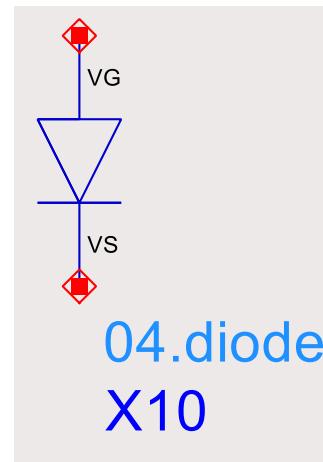


Diode EQUATIONS AND PARAMETERS

```
Var Eqn VAR
lgS_NONLIN
as_igs=Alphas_igs*Vgi
bs_igs=Alphas_igs*Vgi-Ms_igs
I1_igs=Ins_igs*(exp(Ms_igs)*(1+bs_igs+bs_igs^2/2)-1)
I2_igs;if as_igs<-20 then -Ins_igs else Ins_igs*(exp(as_igs)-1) endif
Igs;if bs_igs>0 then I1_igs else I2_igs endif
```

```
Var Eqn VAR
Gate_Source
Ins_igs=4.822e-011
Ms_igs=40
Alphas_igs=29.1
Cgso=9.592e-012
Vbi_cgs=0.8
K_cgs=0.8
```

Associated symbol



The *Diode.dsn* file defines the non-linear model of the input Diode of the FET.



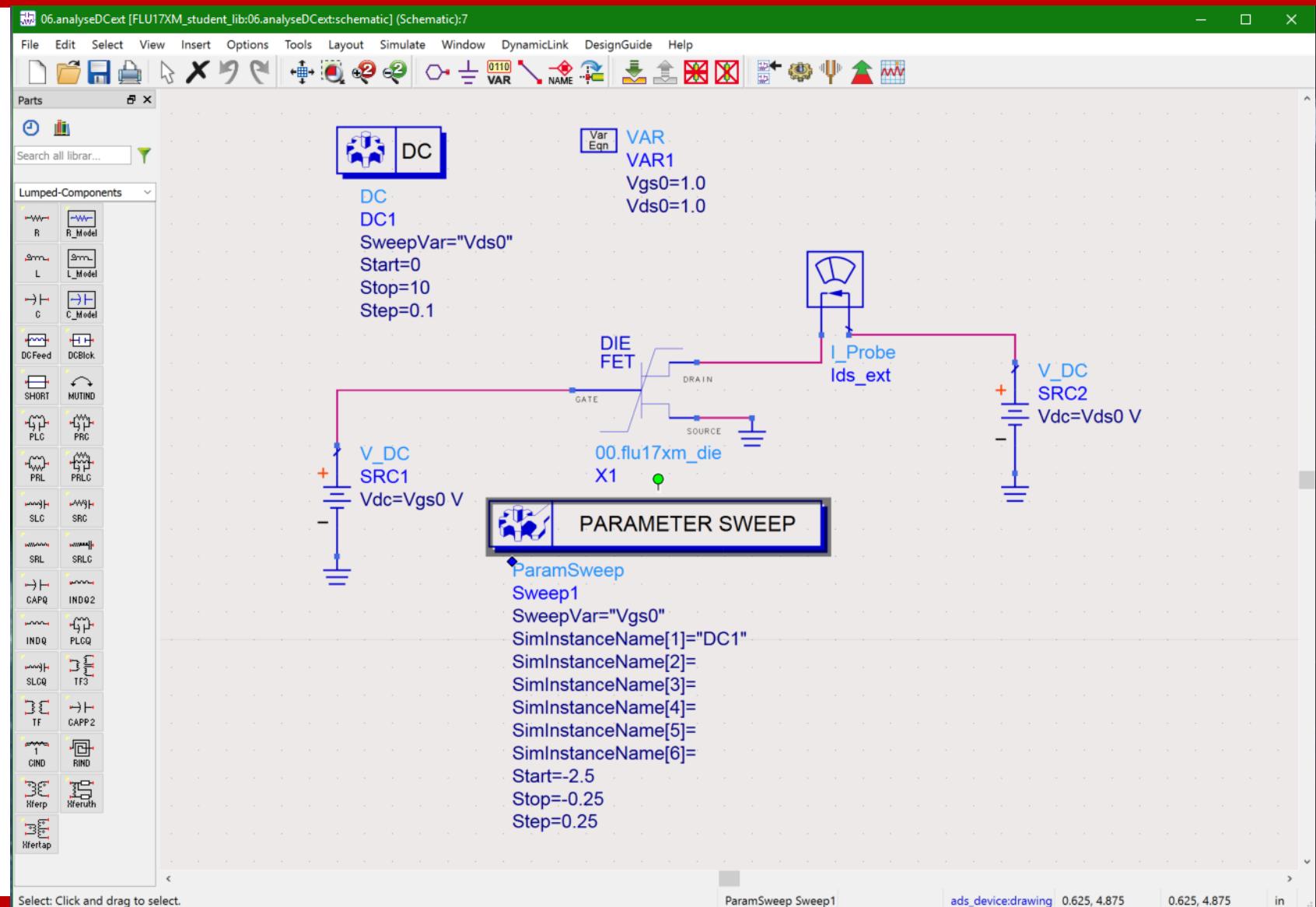
I/V Static Characteristics

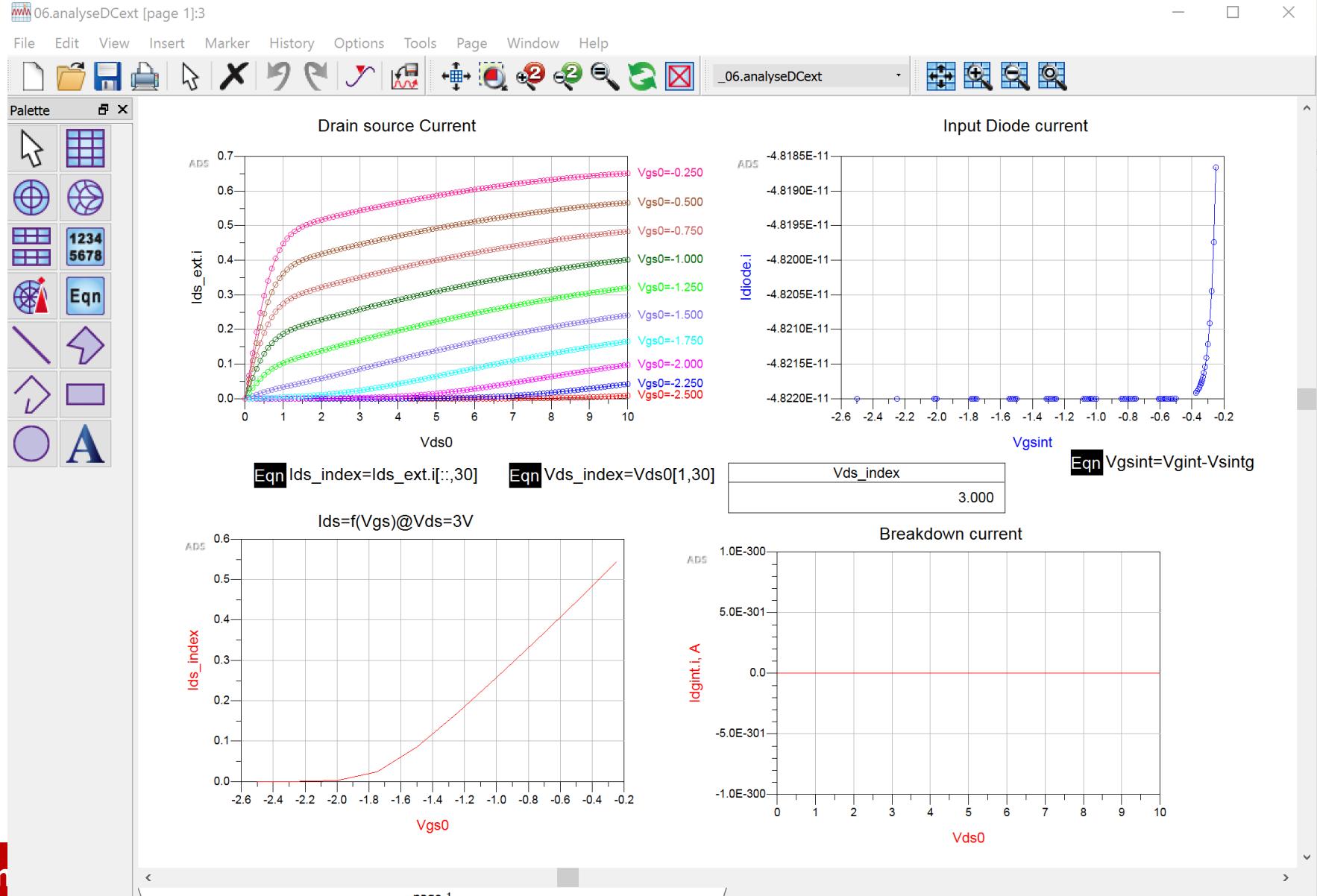


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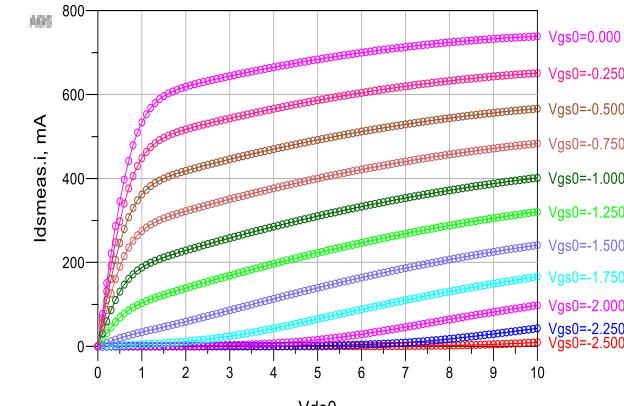
Schematic to plot the extrinsic I/V curves of the Die transistor



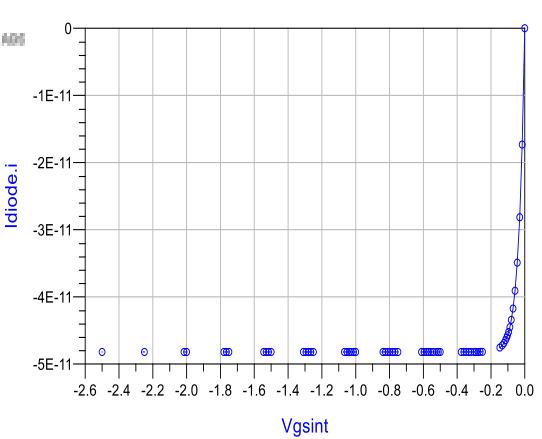


E(rasmus) Mundus on Innovative Microwave Electronics and Optics

Drain Source Current



Input Diode Current

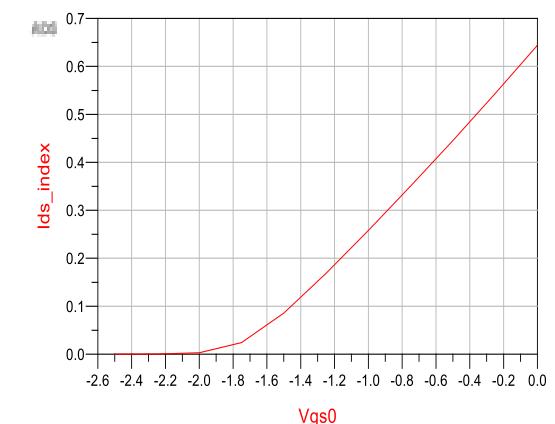


Eqn lds_index=Idsmeas.i[::,30] Eqn Vds_index=Vds0[1,30]

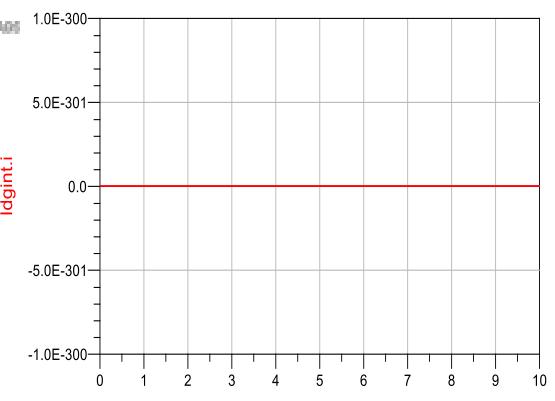
Vds_index
3.000

Eqn Vgsint=Vgint-Vsintg

Ids=f(Vgs) @ Vds=3V

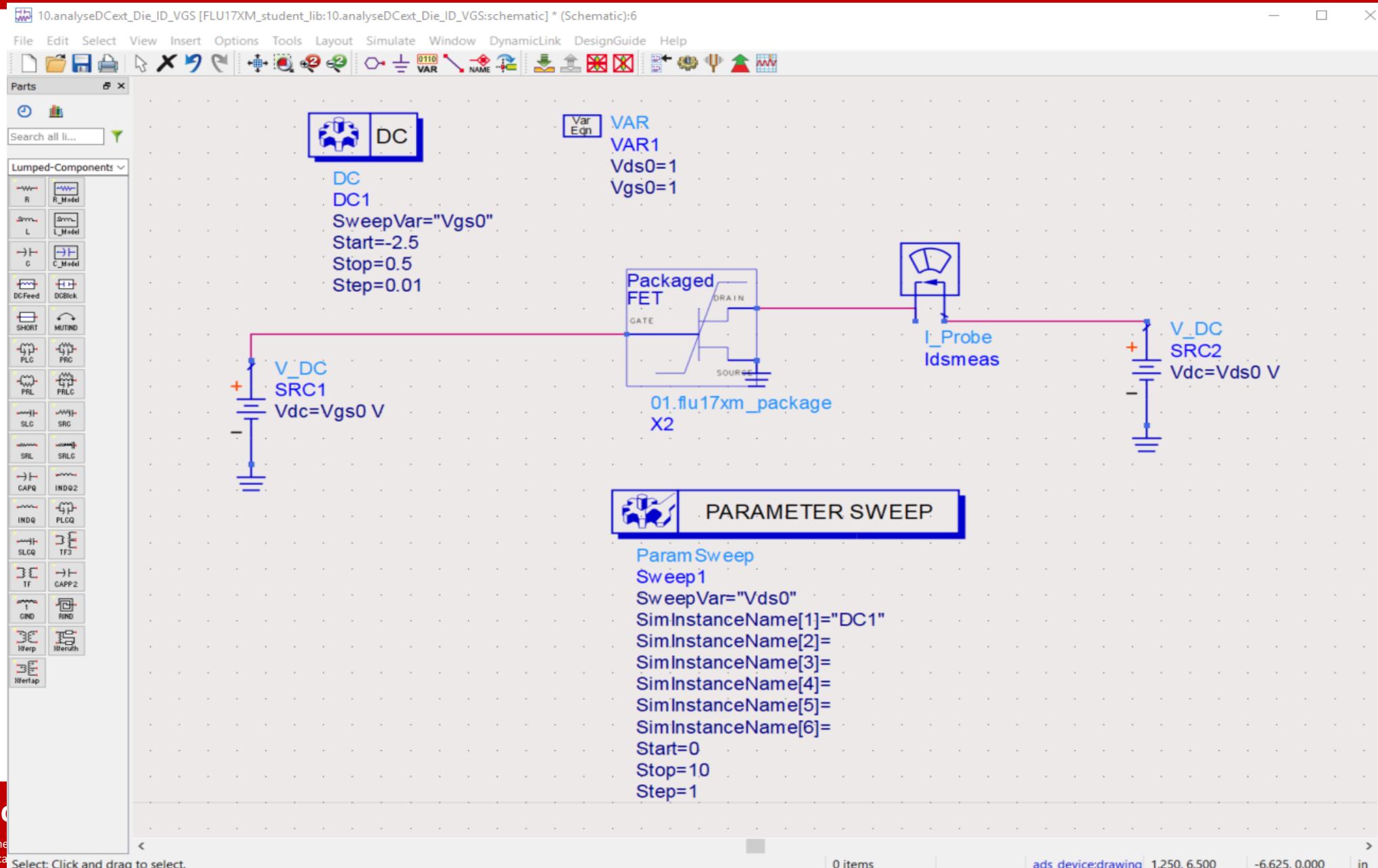


Breakdown Current

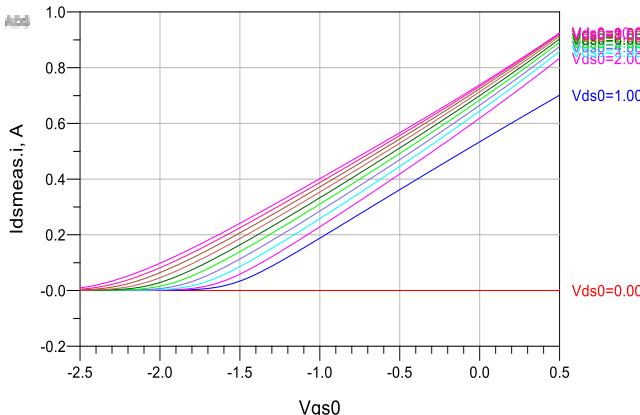


Vds0	Idsmeas.i										
	...0=-2.500	...0=-2.250	...0=-2.000	...0=-1.750	...0=-1.500	...0=-1.250	...0=-1.000	...0=-0.750	...0=-0.500	...0=-0.250	...0=0.000
0.000	2.500 nA	2.250 nA	2.000 nA	1.750 nA	1.500 nA	1.250 nA	1000 pA	750.0 pA	500.0 pA	250.0 pA	0.0000 A
0.100	312.6 nA	3.492 uA	38.72 uA	425.2 uA	3.831 mA	15.57 mA	30.48 mA	44.15 mA	56.21 mA	66.90 mA	76.51 mA
0.200	651.9 nA	7.338 uA	81.70 uA	897.4 uA	7.905 mA	30.89 mA	59.73 mA	86.46 mA	110.3 mA	131.5 mA	150.7 mA
0.300	997.2 nA	11.29 uA	126.3 uA	1.389 mA	11.97 mA	45.15 mA	86.57 mA	125.5 mA	160.6 mA	192.3 mA	221.0 mA
0.400	1.333 uA	15.19 uA	170.7 uA	1.878 mA	15.84 mA	57.87 mA	110.2 mA	160.2 mA	206.1 mA	247.9 mA	286.2 mA
0.500	1.654 uA	18.95 uA	213.9 uA	2.356 mA	19.42 mA	68.85 mA	130.3 mA	190.1 mA	245.8 mA	297.4 mA	345.2 mA
0.600	1.962 uA	22.58 uA	256.1 uA	2.820 mA	22.71 mA	78.16 mA	147.0 mA	215.0 mA	279.5 mA	340.2 mA	397.1 mA
0.700	2.262 uA	26.15 uA	297.7 uA	3.276 mA	25.74 mA	85.99 mA	160.5 mA	235.3 mA	307.4 mA	376.2 mA	441.6 mA
0.800	2.562 uA	29.73 uA	339.5 uA	3.730 mA	28.55 mA	92.62 mA	171.5 mA	251.6 mA	329.9 mA	405.7 mA	478.8 mA
0.900	2.869 uA	33.41 uA	382.5 uA	4.191 mA	31.20 mA	98.30 mA	180.4 mA	264.5 mA	347.8 mA	429.4 mA	509.2 mA
1.000	3.189 uA	37.24 uA	427.5 uA	4.668 mA	33.75 mA	103.3 mA	187.7 mA	274.8 mA	361.9 mA	448.2 mA	533.6 mA
1.100	3.528 uA	41.32 uA	475.2 uA	5.166 mA	36.24 mA	107.7 mA	193.9 mA	283.1 mA	373.0 mA	462.9 mA	552.8 mA
1.200	3.892 uA	45.69 uA	526.4 uA	5.693 mA	38.69 mA	111.8 mA	199.1 mA	289.9 mA	381.8 mA	474.5 mA	567.8 mA
1.300	4.285 uA	50.41 uA	581.7 uA	6.253 mA	41.14 mA	115.5 mA	203.7 mA	295.6 mA	389.0 mA	483.6 mA	579.5 mA
1.400	4.712 uA	55.55 uA	641.8 uA	6.852 mA	43.59 mA	119.1 mA	207.9 mA	300.4 mA	394.9 mA	491.0 mA	588.8 mA
1.500	5.177 uA	61.17 uA	707.4 uA	7.494 mA	46.05 mA	122.6 mA	211.7 mA	304.8 mA	399.9 mA	497.0 mA	596.2 mA
1.600	5.686 uA	67.30 uA	779.1 uA	8.182 mA	48.54 mA	125.9 mA	215.3 mA	308.7 mA	404.3 mA	502.0 mA	602.2 mA
1.700	6.242 uA	74.03 uA	857.6 uA	8.920 mA	51.05 mA	129.1 mA	218.8 mA	312.3 mA	408.1 mA	506.3 mA	607.2 mA
1.800	6.852 uA	81.41 uA	943.6 uA	9.710 mA	53.59 mA	132.3 mA	222.1 mA	315.7 mA	411.7 mA	510.1 mA	611.4 mA
1.900	7.519 uA	89.51 uA	1.038 mA	10.56 mA	56.17 mA	135.5 mA	225.3 mA	318.9 mA	415.0 mA	513.6 mA	615.1 mA
2.000	8.252 uA	98.40 uA	1.141 uA	11.46 mA	58.76 mA	138.6 mA	228.5 mA	322.0 mA	418.1 mA	516.8 mA	618.5 mA
2.100	9.055 uA	108.2 uA	1.255 uA	12.43 mA	61.39 mA	141.7 mA	231.6 mA	325.1 mA	421.1 mA	519.8 mA	621.5 mA
2.200	9.935 uA	118.9 uA	1.379 mA	13.46 mA	64.04 mA	144.8 mA	234.6 mA	328.1 mA	424.0 mA	522.6 mA	624.4 mA
2.300	10.90 uA	130.7 uA	1.515 uA	14.55 mA	66.71 mA	147.8 mA	237.6 mA	331.0 mA	426.9 mA	525.4 mA	627.1 mA
2.400	11.96 uA	143.6 uA	1.664 uA	15.71 mA	69.40 mA	150.8 mA	240.6 mA	333.9 mA	429.7 mA	528.1 mA	629.7 mA
2.500	13.12 uA	157.8 uA	1.827 mA	16.93 mA	72.10 mA	153.8 mA	243.6 mA	336.7 mA	432.4 mA	530.7 mA	632.2 mA
2.600	14.40 uA	173.4 uA	2.006 mA	18.22 mA	74.82 mA	156.8 mA	246.5 mA	339.5 mA	435.1 mA	533.2 mA	634.6 mA
2.700	15.80 uA	190.6 uA	2.201 mA	19.58 mA	77.55 mA	159.8 mA	249.4 mA	342.3 mA	437.7 mA	535.7 mA	637.0 mA
2.800	17.33 uA	209.4 uA	2.415 mA	21.00 mA	80.29 mA	162.7 mA	252.3 mA	345.1 mA	440.3 mA	538.2 mA	639.3 mA
2.900	19.01 uA	230.1 uA	2.648 mA	22.49 mA	83.03 mA	165.7 mA	255.1 mA	347.8 mA	442.9 mA	540.7 mA	641.6 mA
3.000	20.86 uA	252.8 uA	2.902 mA	24.04 mA	85.78 mA	168.6 mA	258.0 mA	350.5 mA	445.5 mA	543.1 mA	643.9 mA
3.100	22.89 uA	277.8 uA	3.179 mA	25.66 mA	88.53 mA	171.5 mA	260.8 mA	353.2 mA	448.0 mA	545.5 mA	646.1 mA
3.200	25.11 uA	305.2 uA	3.481 mA	27.34 mA	91.29 mA	174.3 mA	263.6 mA	355.9 mA	450.5 mA	547.8 mA	648.3 mA
3.300	27.54 uA	335.2 uA	3.810 mA	29.08 mA	94.04 mA	177.2 mA	266.3 mA	358.5 mA	453.0 mA	550.1 mA	650.4 mA
3.400	30.22 uA	368.2 uA	4.166 mA	30.88 mA	96.78 mA	180.0 mA	269.1 mA	361.1 mA	455.5 mA	552.5 mA	652.6 mA
3.500	33.15 uA	404.4 uA	4.554 mA	32.73 mA	99.53 mA	182.9 mA	271.8 mA	363.7 mA	457.9 mA	554.7 mA	654.7 mA
3.600	36.36 uA	444.2 uA	4.973 mA	34.64 mA	102.3 mA	185.7 mA	274.5 mA	366.3 mA	460.4 mA	557.0 mA	656.8 mA
3.700	39.89 uA	487.8 uA	5.427 mA	36.59 mA	105.0 mA	188.4 mA	277.2 mA	368.8 mA	462.8 mA	559.2 mA	658.9 mA
3.800	43.76 uA	535.6 uA	5.918 mA	38.59 mA	107.7 mA	191.2 mA	279.8 mA	371.4 mA	465.1 mA	561.4 mA	660.9 mA
3.900	48.00 uA	588.1 uA	6.448 mA	40.63 mA	110.4 mA	193.9 mA	282.5 mA	373.9 mA	467.5 mA	563.6 mA	662.9 mA
4.000	52.65 uA	645.6 uA	7.018 mA	42.71 mA	113.1 mA	196.6 mA	285.1 mA	376.3 mA	469.8 mA	565.8 mA	664.9 mA
4.100	57.75 uA	708.6 uA	7.631 mA	44.82 mA	115.8 mA	199.3 mA	287.7 mA	378.8 mA	472.1 mA	567.9 mA	666.9 mA
4.200	63.35 uA	777.7 uA	8.288 mA	46.97 mA	118.5 mA	202.0 mA	290.3 mA	381.2 mA	474.4 mA	570.0 mA	668.8 mA
4.300	69.48 uA	853.4 uA	8.992 mA	49.15 mA	121.1 mA	204.7 mA	292.8 mA	383.7 mA	476.7 mA	572.1 mA	670.7 mA
4.400	76.21 uA	936.3 uA	9.744 mA	51.35 mA	123.8 mA	207.3 mA	295.4 mA	386.0 mA	478.9 mA	574.2 mA	672.6 mA
4.500	83.58 uA	1.027 mA	10.55 mA	53.58 mA	126.4 mA	209.9 mA	297.9 mA	388.4 mA	481.1 mA	576.2 mA	674.5 mA
4.600	91.67 uA	1.126 mA	11.40 mA	55.82 mA	129.0 mA	212.5 mA	300.4 mA	390.8 mA	483.3 mA	578.3 mA	676.3 mA

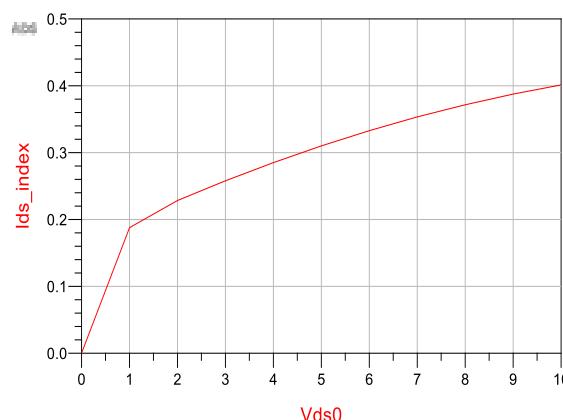
Schematic to plot the
extrinsic I/V curves of the
Packaged transistor



Drain Source Current

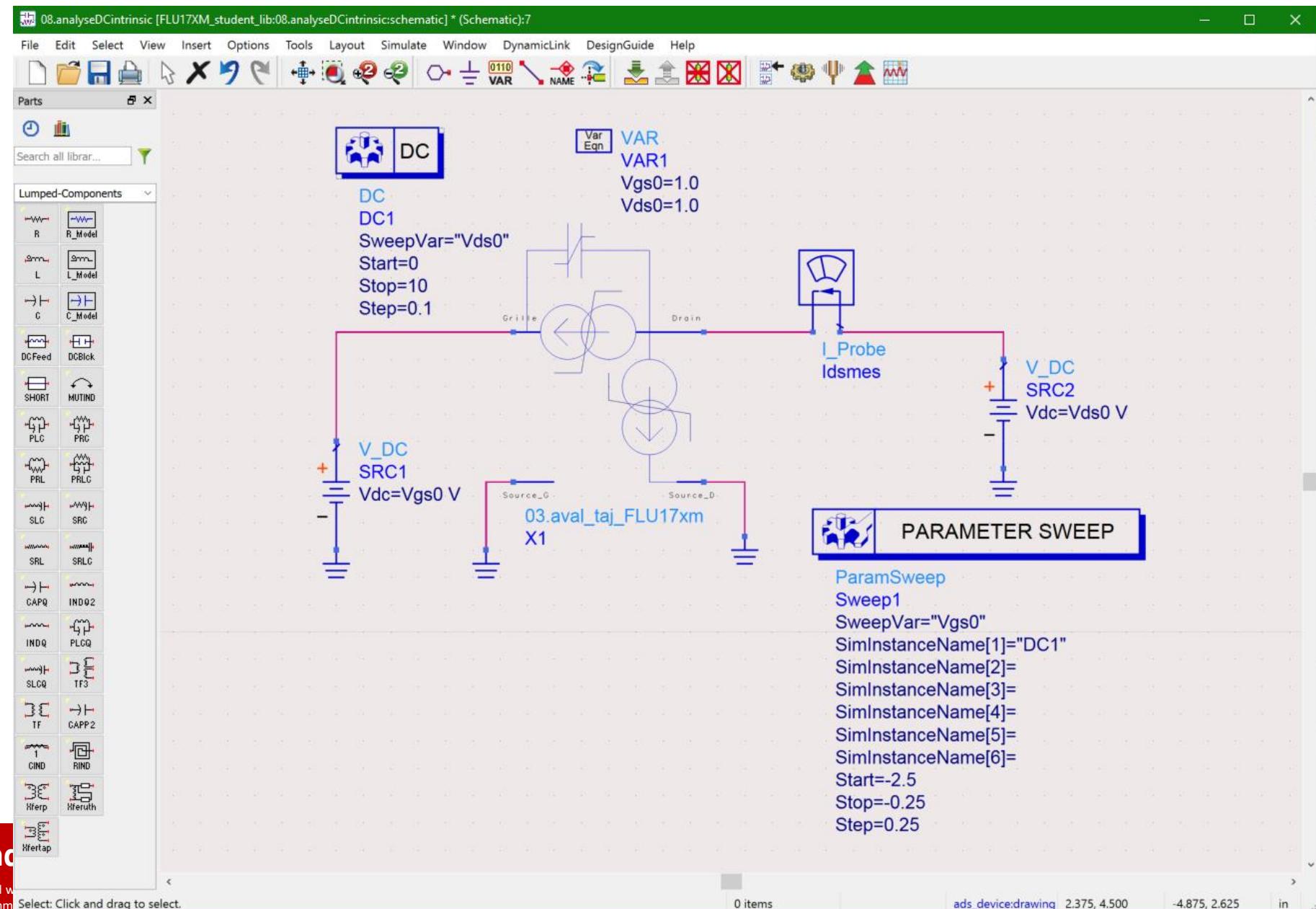

 $Eqn|Ids_index=Idsmeas.i[:,150]$ $Eqn|Vgs_index=Vgs0[1,150]$

Vgs_index
-1.000

 $Ids=f(Vds) @ Vgs=-1V$


Vgs0	Idsmeas.i										
	$Vds0=0.000$	$Vds0=1.000$	$Vds0=2.000$	$Vds0=3.000$	$Vds0=4.000$	$Vds0=5.000$	$Vds0=6.000$	$Vds0=7.000$	$Vds0=8.000$	$Vds0=9.000$	$Vds0=10.000$
-2.500	2.500 nA	3.189 uA	8.252 uA	20.86 uA	52.65 uA	132.6 uA	332.5 uA	825.6 uA	2.002 mA	4.593 mA	9.464 mA
-2.490	2.490 nA	3.520 uA	9.118 uA	23.07 uA	58.26 uA	146.8 uA	368.2 uA	913.7 uA	2.209 mA	5.034 mA	10.24 mA
-2.480	2.480 nA	3.886 uA	10.07 uA	25.50 uA	64.46 uA	162.5 uA	407.7 uA	1.011 mA	2.437 mA	5.510 mA	11.06 mA
-2.470	2.470 nA	4.289 uA	11.13 uA	28.20 uA	71.31 uA	179.9 uA	451.3 uA	1.118 mA	2.686 mA	6.024 mA	11.93 mA
-2.460	2.460 nA	4.734 uA	12.29 uA	31.17 uA	78.89 uA	199.1 uA	499.5 uA	1.236 mA	2.959 mA	6.578 mA	12.85 mA
-2.450	2.450 nA	5.225 uA	13.58 uA	34.46 uA	87.26 uA	220.3 uA	552.8 uA	1.366 mA	3.257 mA	7.174 mA	13.82 mA
-2.440	2.440 nA	5.767 uA	15.00 uA	38.09 uA	96.52 uA	243.8 uA	611.7 uA	1.510 mA	3.582 mA	7.813 mA	14.83 mA
-2.430	2.430 nA	6.364 uA	16.57 uA	42.10 uA	106.8 uA	269.8 uA	676.7 uA	1.667 mA	3.936 mA	8.497 mA	15.89 mA
-2.420	2.420 nA	7.023 uA	18.30 uA	46.53 uA	118.1 uA	298.5 uA	748.4 uA	1.841 mA	4.322 mA	9.227 mA	17.00 mA
-2.410	2.410 nA	7.750 uA	20.21 uA	51.43 uA	130.6 uA	330.2 uA	827.6 uA	2.031 mA	4.741 mA	10.01 mA	18.15 mA
-2.400	2.400 nA	8.551 uA	22.32 uA	56.83 uA	144.4 uA	365.2 uA	915.0 uA	2.240 mA	5.195 mA	10.83 mA	19.36 mA
-2.390	2.390 nA	9.435 uA	24.65 uA	62.80 uA	159.6 uA	403.9 uA	1.011 mA	2.469 mA	5.687 mA	11.71 mA	20.61 mA
-2.380	2.380 nA	10.41 uA	27.22 uA	69.40 uA	176.5 uA	446.6 uA	1.118 mA	2.720 mA	6.219 mA	12.64 mA	21.91 mA
-2.370	2.370 nA	11.48 uA	30.05 uA	76.68 uA	195.1 uA	493.8 uA	1.235 mA	2.995 mA	6.792 mA	13.62 mA	23.25 mA
-2.360	2.360 nA	12.67 uA	33.18 uA	84.72 uA	215.7 uA	545.9 uA	1.363 mA	3.296 mA	7.410 mA	14.65 mA	24.64 mA
-2.350	2.350 nA	13.98 uA	36.64 uA	93.60 uA	238.4 uA	603.4 uA	1.505 mA	3.624 mA	8.073 mA	15.74 mA	26.07 mA
-2.340	2.340 nA	15.42 uA	40.45 uA	103.4 uA	263.5 uA	666.8 uA	1.661 mA	3.981 mA	8.784 mA	16.88 mA	27.55 mA
-2.330	2.330 nA	17.01 uA	44.65 uA	114.2 uA	291.2 uA	736.8 uA	1.833 mA	4.371 mA	9.544 mA	18.07 mA	29.07 mA
-2.320	2.320 nA	18.76 uA	49.29 uA	126.2 uA	321.7 uA	814.0 uA	2.021 mA	4.794 mA	10.36 mA	19.31 mA	30.63 mA
-2.310	2.310 nA	20.69 uA	54.42 uA	139.4 uA	355.5 uA	899.2 uA	2.228 mA	5.254 mA	11.22 mA	20.61 mA	32.23 mA
-2.300	2.300 nA	22.82 uA	60.07 uA	153.9 uA	392.8 uA	993.0 uA	2.454 mA	5.752 mA	12.14 mA	21.96 mA	33.87 mA
-2.290	2.290 nA	25.17 uA	66.30 uA	170.0 uA	433.9 uA	1.096 mA	2.703 mA	6.292 mA	13.11 mA	23.36 mA	35.55 mA
-2.280	2.280 nA	27.76 uA	73.19 uA	187.8 uA	479.3 uA	1.210 mA	2.975 mA	6.874 mA	14.14 mA	24.80 mA	37.27 mA
-2.270	2.270 nA	30.62 uA	80.78 uA	207.3 uA	529.4 uA	1.336 mA	3.272 mA	7.502 mA	15.23 mA	26.30 mA	39.03 mA
-2.260	2.260 nA	33.77 uA	89.15 uA	229.0 uA	584.6 uA	1.473 mA	3.597 mA	8.177 mA	16.37 mA	27.85 mA	40.82 mA
-2.250	2.250 nA	37.24 uA	98.40 uA	252.8 uA	645.6 uA	1.625 mA	3.952 mA	8.903 mA	17.57 mA	29.44 mA	42.65 mA
-2.240	2.240 nA	41.07 uA	108.6 uA	279.1 uA	712.8 uA	1.792 mA	4.338 mA	9.680 mA	18.83 mA	31.08 mA	44.51 mA
-2.230	2.230 nA	45.29 uA	119.8 uA	308.2 uA	786.8 uA	1.975 mA	4.759 mA	10.51 mA	20.14 mA	32.77 mA	46.41 mA
-2.220	2.220 nA	49.95 uA	132.2 uA	340.2 uA	868.5 uA	2.176 mA	5.216 mA	11.40 mA	21.52 mA	34.50 mA	48.34 mA
-2.210	2.210 nA	55.08 uA	145.9 uA	375.6 uA	958.4 uA	2.397 mA	5.711 mA	12.34 mA	22.94 mA	36.28 mA	50.30 mA
-2.200	2.200 nA	60.73 uA	161.0 uA	414.6 uA	1.057 mA	2.638 mA	6.249 mA	13.34 mA	24.43 mA	38.09 mA	52.30 mA
-2.190	2.190 nA	66.97 uA	177.7 uA	457.6 uA	1.167 mA	2.903 mA	6.830 mA	14.40 mA	25.97 mA	39.95 mA	54.32 mA
-2.180	2.180 nA	73.85 uA	196.1 uA	505.0 uA	1.287 mA	3.193 mA	7.457 mA	15.53 mA	27.56 mA	41.84 mA	56.37 mA
-2.170	2.170 nA	81.42 uA	216.3 uA	557.3 uA	1.419 mA	3.509 mA	8.133 mA	16.71 mA	29.21 mA	43.78 mA	58.46 mA
-2.160	2.160 nA	89.78 uA	238.7 uA	615.0 uA	1.564 mA	3.855 mA	8.861 mA	17.95 mA	30.90 mA	45.75 mA	60.57 mA
-2.150	2.150 nA	98.99 uA	263.3 uA	678.5 uA	1.724 mA	4.232 mA	9.641 mA	19.26 mA	32.65 mA	47.76 mA	62.71 mA
-2.140	2.140 nA	109.1 uA	290.5 uA	748.5 uA	1.899 mA	4.643 mA	10.48 mA	20.63 mA	34.45 mA	49.80 mA	64.88 mA
-2.130	2.130 nA	120.3 uA	320.5 uA	825.6 uA	2.091 mA	5.090 mA	11.37 mA	22.06 mA	36.30 mA	51.88 mA	67.08 mA
-2.120	2.120 nA	132.7 uA	353.5 uA	910.6 uA	2.303 mA	5.576 mA	12.32 mA	23.55 mA	38.19 mA	53.99 mA	69.30 mA
-2.110	2.110 nA	146.3 uA	390.0 uA	1.004 mA	2.534 mA	6.102 mA	13.34 mA	25.10 mA	40.13 mA	56.14 mA	71.55 mA
-2.100	2.100 nA	161.3 uA	430.1 uA	1.107 mA	2.788 mA	6.673 mA	14.42 mA	26.71 mA	42.11 mA	58.31 mA	73.82 mA
-2.090	2.090 nA	177.8 uA	474.4 uA	1.221 mA	3.066 mA	7.290 mA	15.56 mA	28.38 mA	44.13 mA	60.52 mA	76.12 mA
-2.080	2.080 nA	196.0 uA	523.2 uA	1.345 mA	3.370 mA	7.956 mA	16.76 mA	30.11 mA	46.19 mA	62.75 mA	78.44 mA

Schematic to plot the
intrinsic I/V curves of the
Die transistor



Basics of Active and

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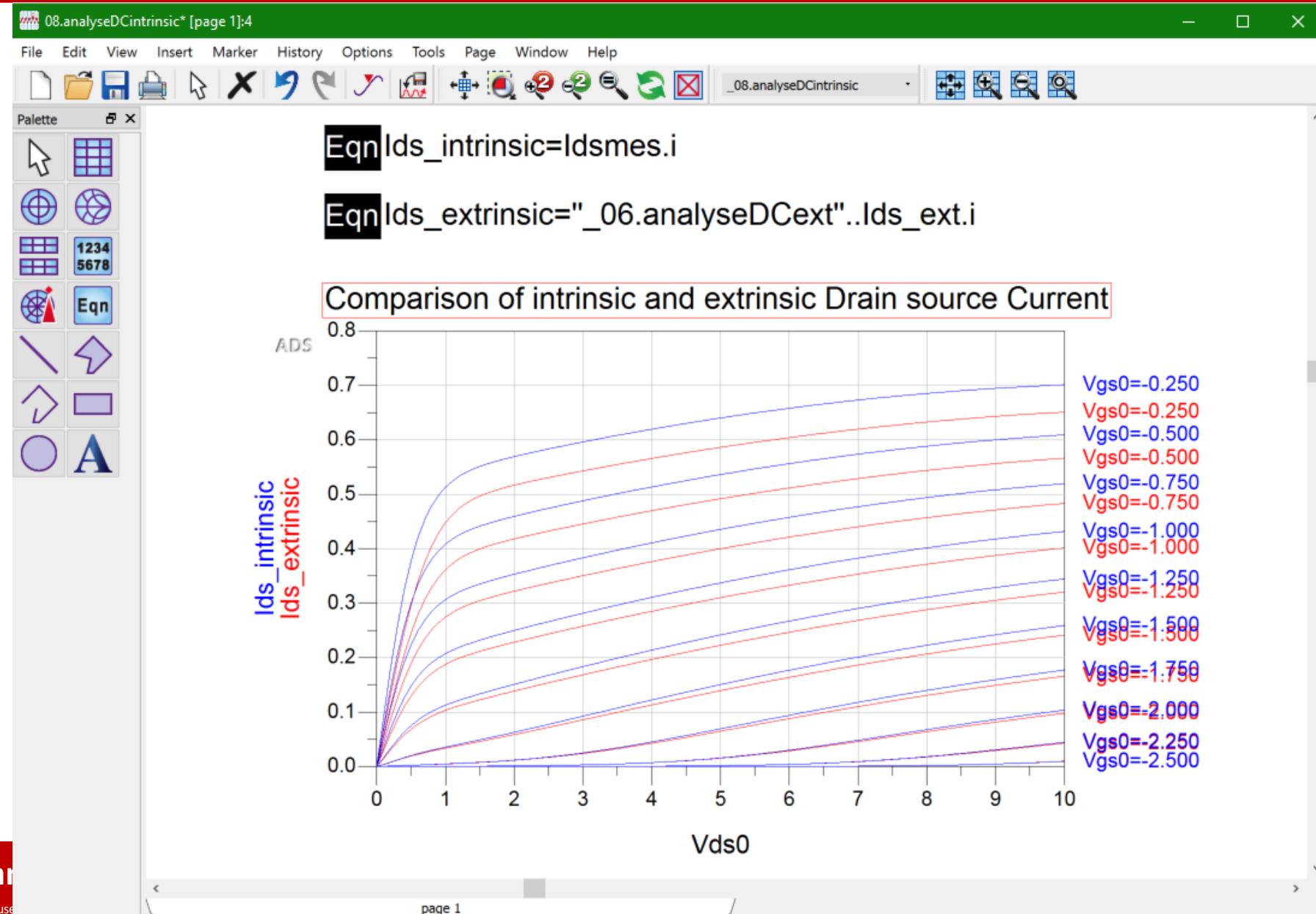
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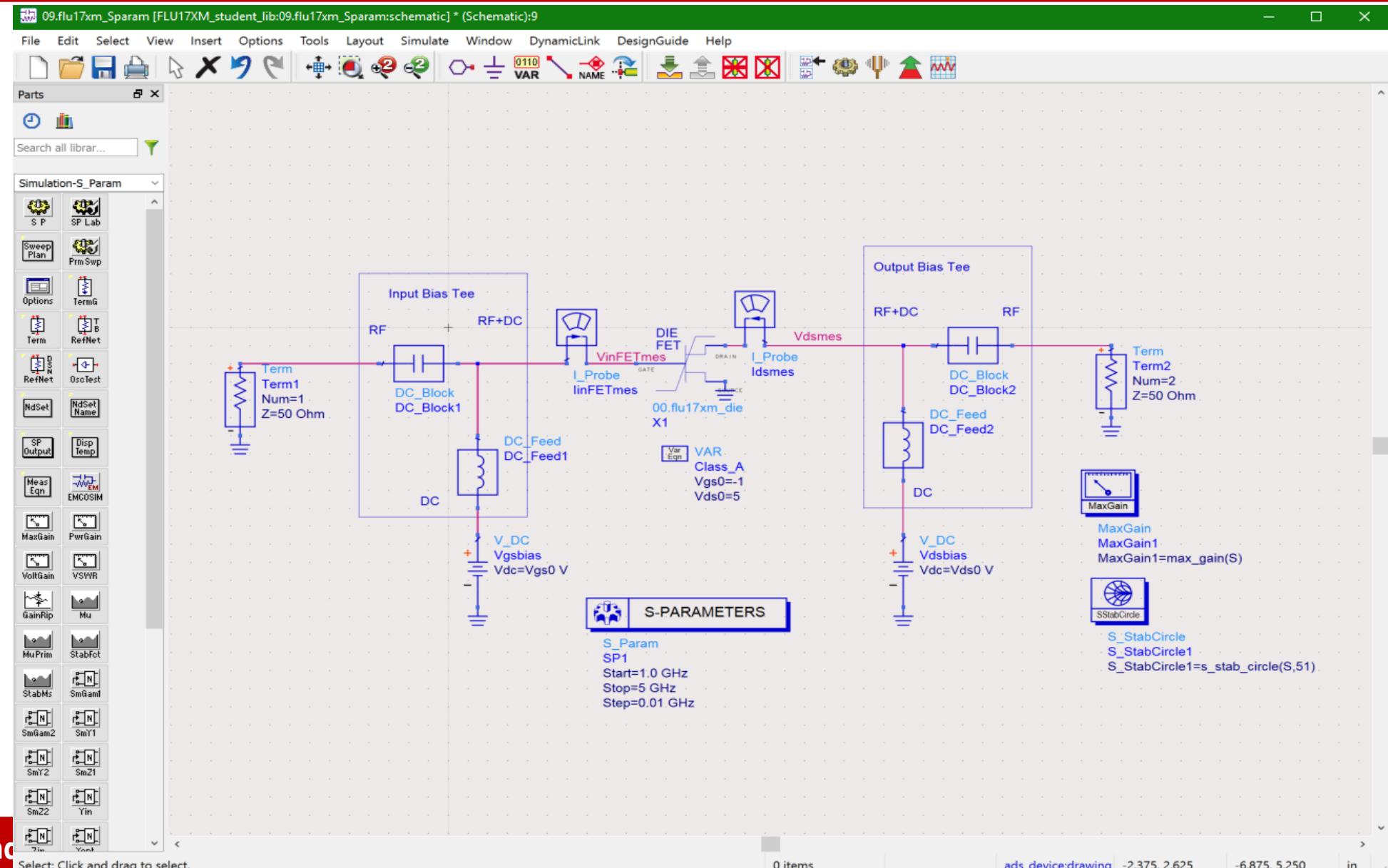
S Parameter Characteristics

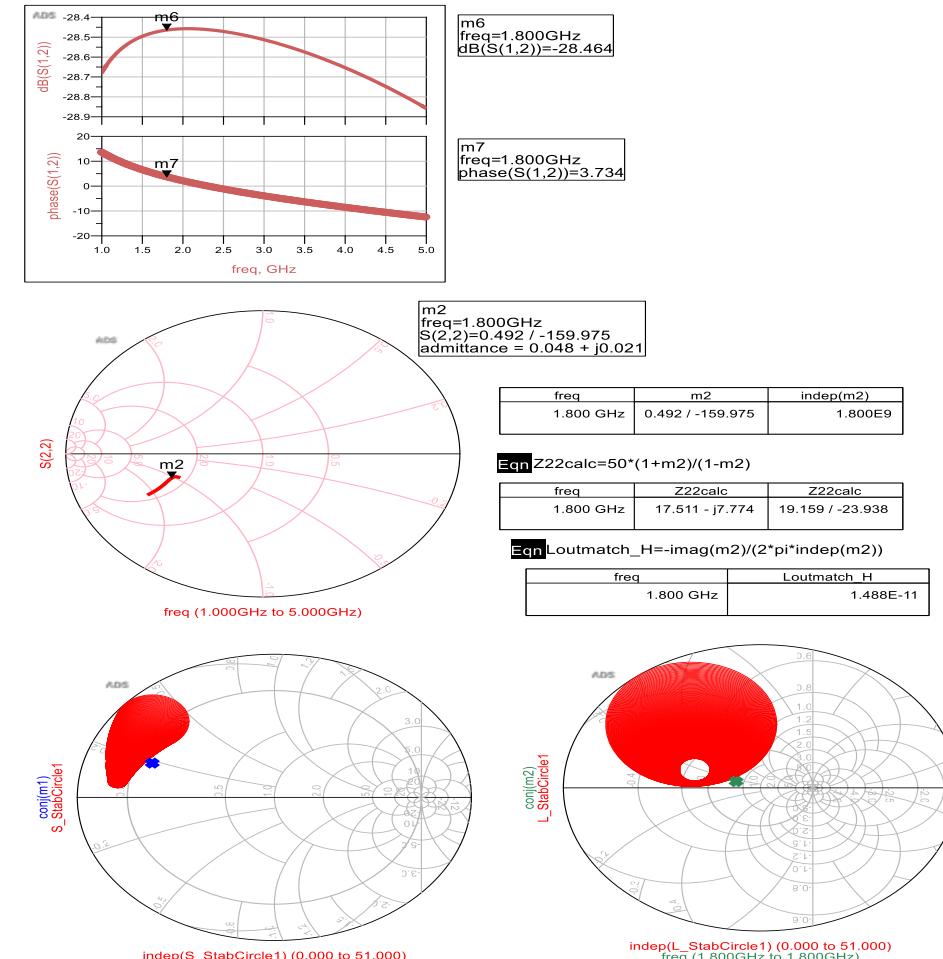
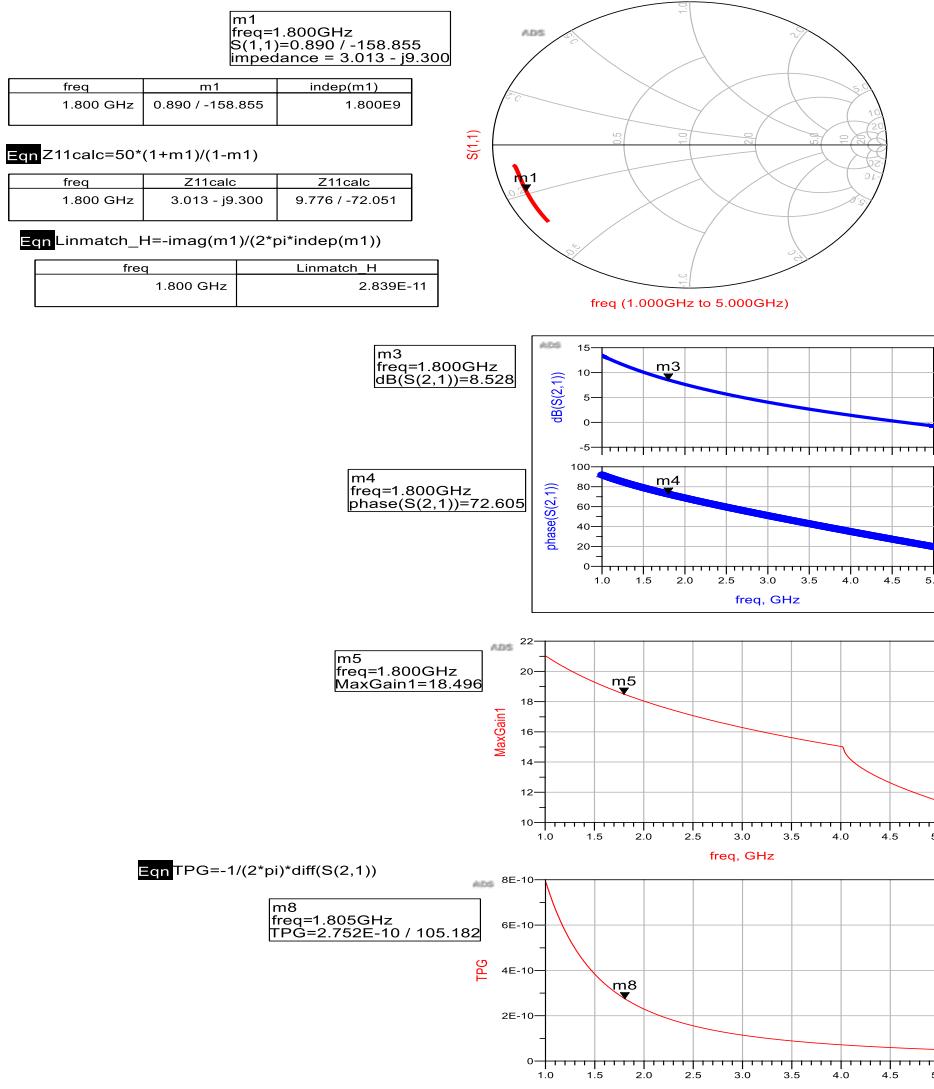


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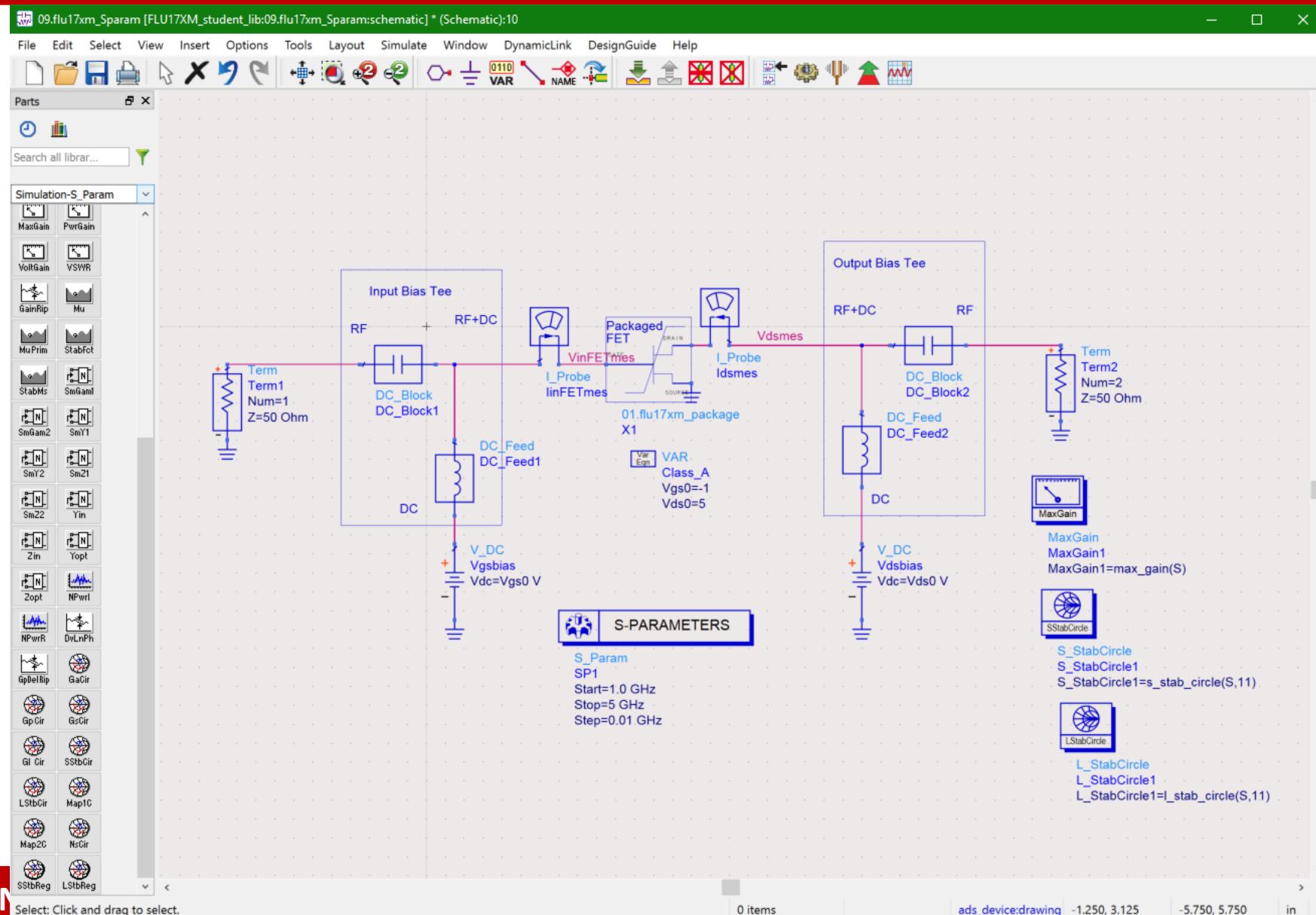


Schematic to plot the S parameter curves of the Die transistor





Schematic to plot the S parameter curves of the Packaged transistor



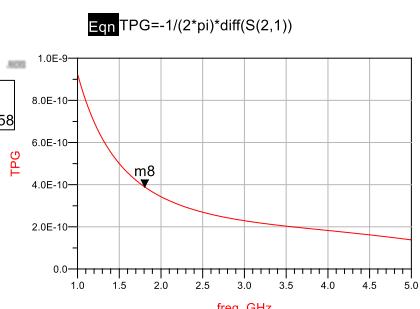
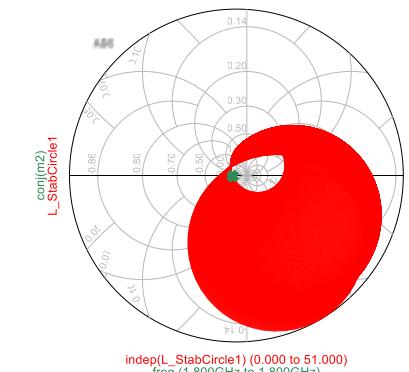
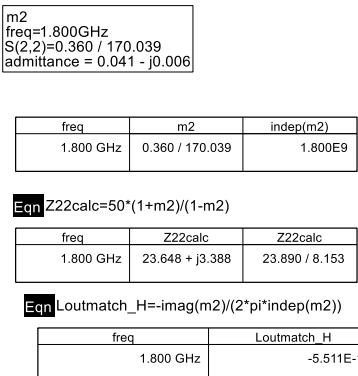
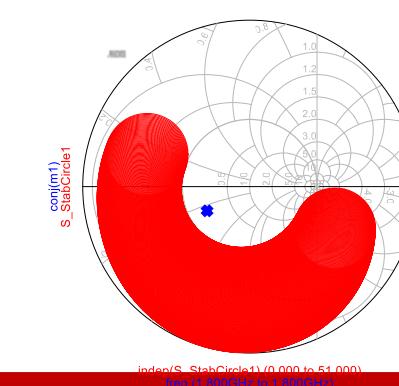
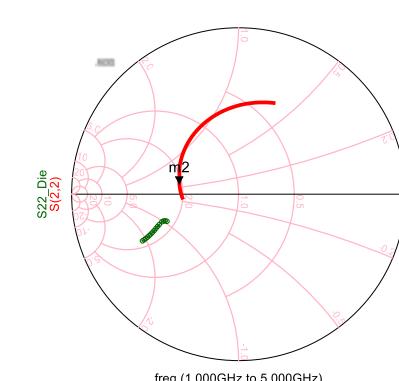
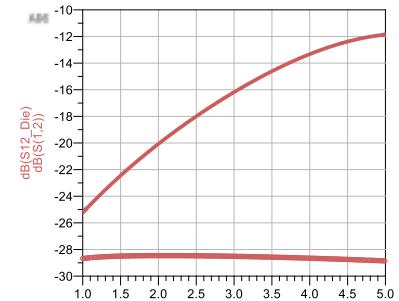
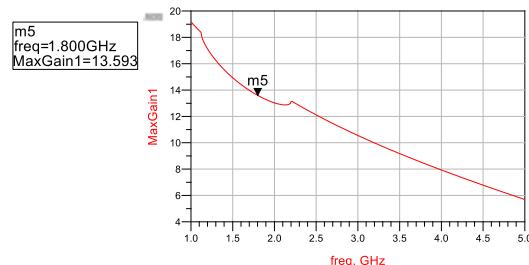
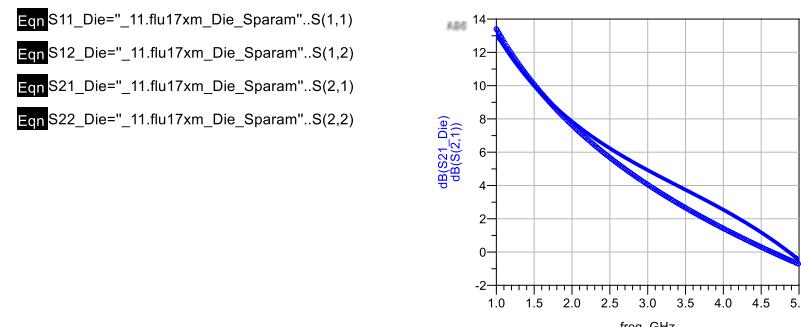
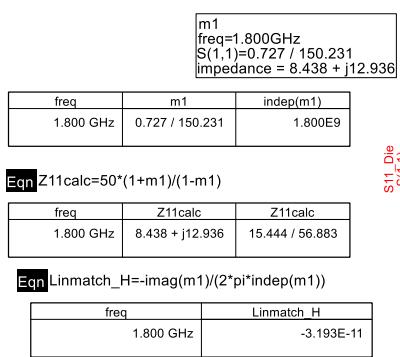
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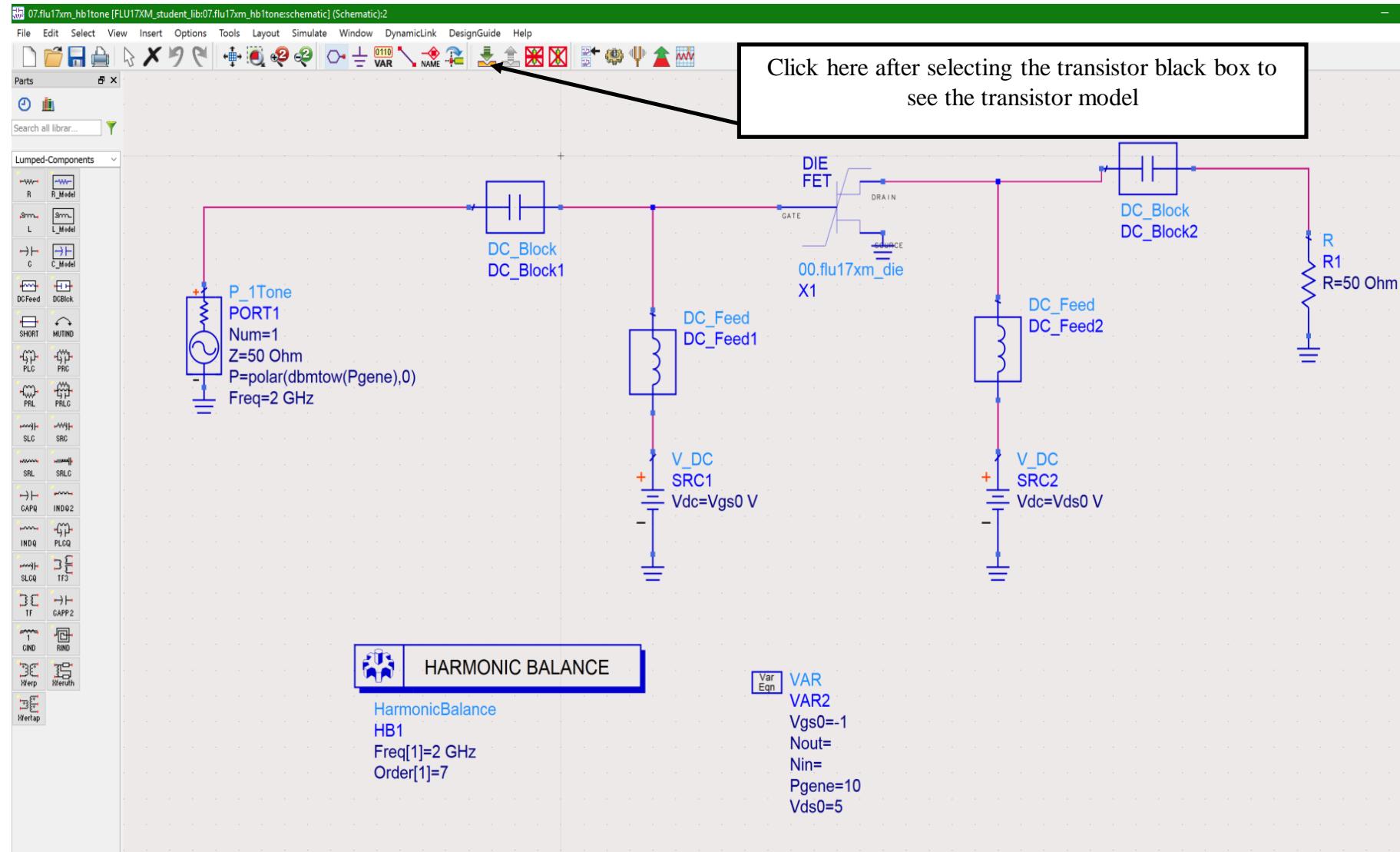


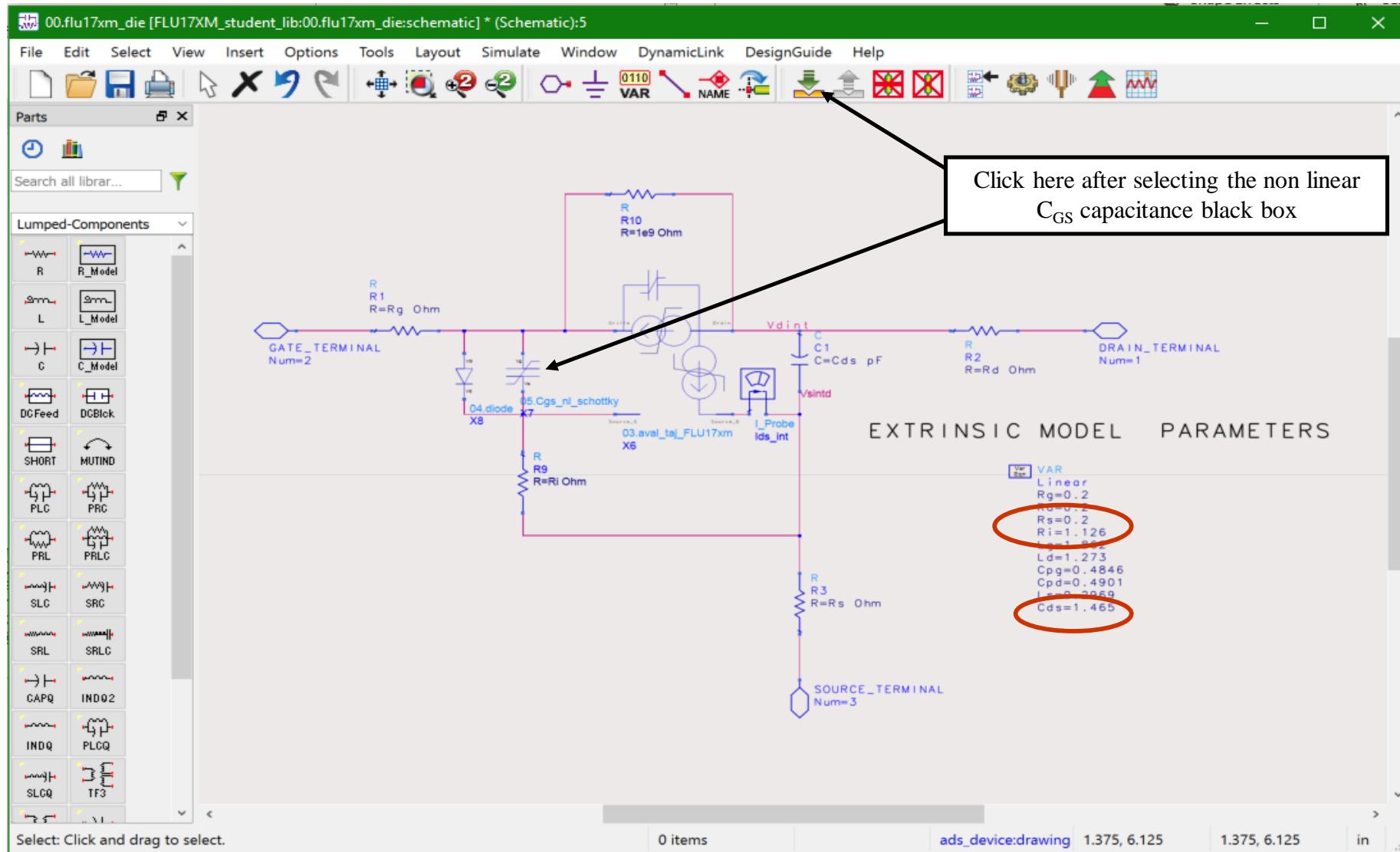
PA Design with Die transistor and Lumped components

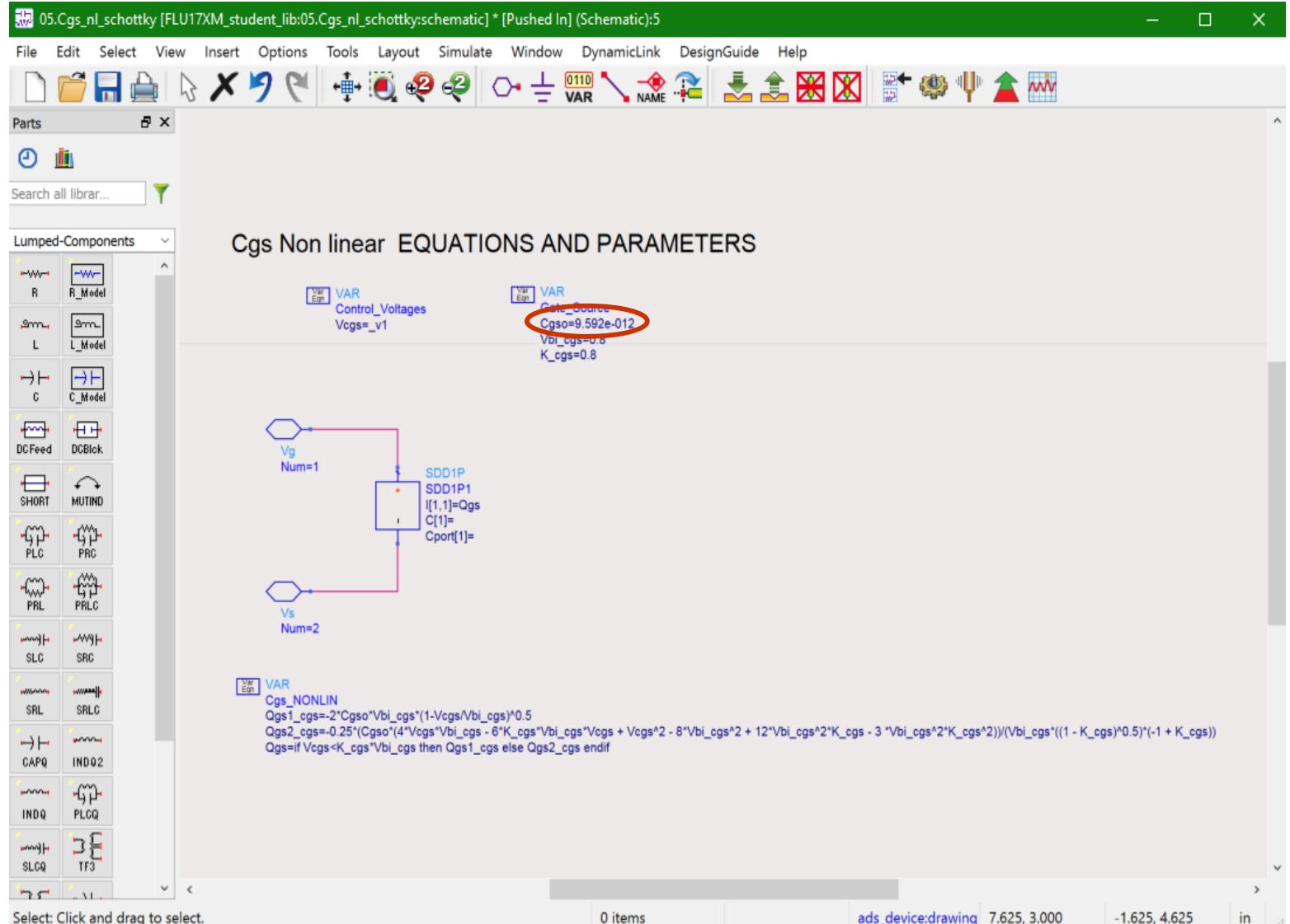


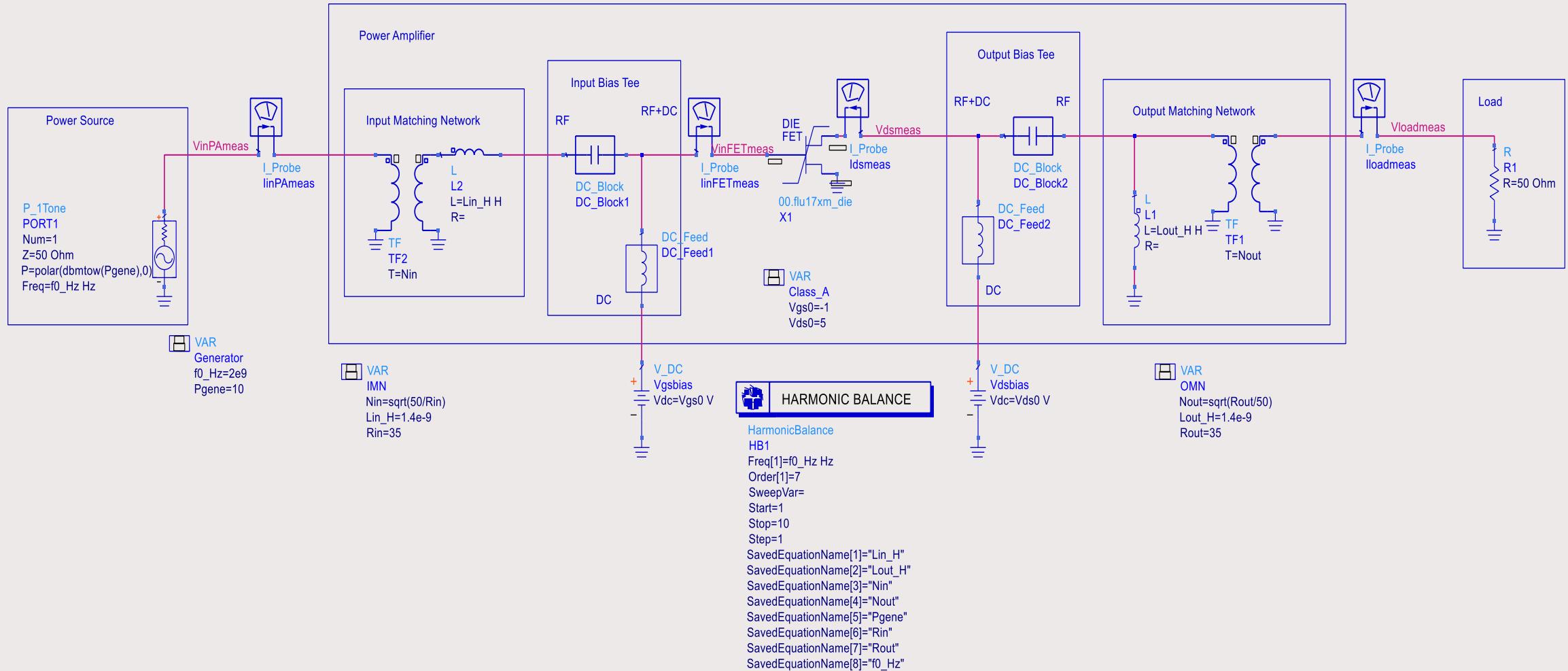
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$$\text{Eqn} \quad \text{VinPA_f0} = \text{VinPAmeas}[1]$$

$$\text{Eqn} \quad \text{VoutPA_f0} = \text{Vloadmeas}[1]$$

$$\text{Eqn} \quad \text{linPA_f0} = \text{linPAmeas.i}[1]$$

$$\text{Eqn} \quad \text{outPA_f0} = \text{lloadmeas.i}[1]$$

$$\text{Eqn} \quad \text{PinPA_f0_mW} = 0.5 * 1000 * \text{real}(\text{VinPA_f0} * \text{conj}(\text{linPA_f0}))$$

$$\text{Eqn} \quad \text{PinPA_f0_dBm} = 10 * \log10(\text{PinPA_f0_mW})$$

$$\text{Eqn} \quad \text{GPA_f0} = \text{PoutPA_f0_mW} / \text{PinPA_f0_mW}$$

$$\text{Eqn} \quad \text{GPA_f0_dBm} = 10 * \log10(\text{GPA_f0})$$

$$\text{Eqn} \quad \text{VinPA_DC} = \text{mag}(\text{VinFETmeas}[0]) \quad \text{Eqn} \quad \text{linPA_DC} = \text{mag}(\text{linFETmeas.i}[0])$$

$$\text{Eqn} \quad \text{VoutPA_DC} = \text{mag}(\text{Vdsmeas}[0]) \quad \text{Eqn} \quad \text{outPA_DC} = \text{mag}(\text{Idsmeas.i}[0])$$

$$\text{Eqn} \quad \text{PoutPA_f0_mW} = 0.5 * 1000 * \text{real}(\text{VoutPA_f0} * \text{conj}(\text{outPA_f0}))$$

$$\text{Eqn} \quad \text{PoutPA_f0_dBm} = 10 * \log10(\text{PoutPA_f0_mW})$$

$$\text{Eqn} \quad \text{PaddPA_f0_mW} = \text{PoutPA_f0_mW} - \text{PinPA_f0_mW}$$

$$\text{Eqn} \quad \text{PaddPA_f0_dBm} = 10 * \log10(\text{PaddPA_f0_mW})$$

$$\text{Eqn} \quad \text{Drain_Efficiency} = \text{PoutPA_f0_mW} / \text{PDC_mW} * 100$$

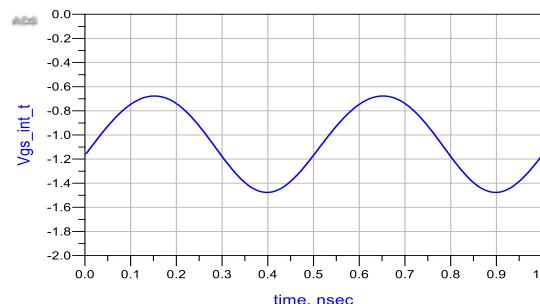
$$\text{Eqn} \quad \text{PAE} = \text{PaddPA_f0_mW} / \text{PDC_mW} * 100$$

$$\text{Eqn} \quad \text{ZinFET_f0} = \text{VinFETmeas}[1] / \text{linFETmeas.i}[1]$$

$$\text{Eqn} \quad \text{ZinPA_f0} = \text{VinPAmeas}[1] / \text{linPAmeas.i}[1]$$

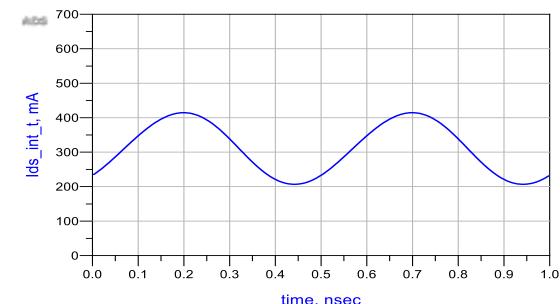
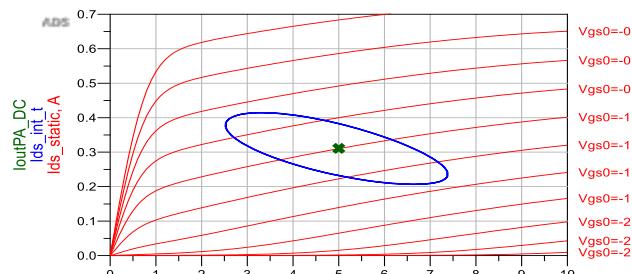
$$\text{Eqn} \quad \text{GamainFET_f0} = (\text{ZinFET_f0} - 50) / (\text{ZinFET_f0} + 50)$$

$$\text{Eqn} \quad \text{GamainPA_f0} = (\text{ZinPA_f0} - 50) / (\text{ZinPA_f0} + 50)$$



PinPA_f0_mW	PoutPA_f0_mW	GPA_f0	PDC_mW	Drain_Efficiency	PAE
0.045	82.285	1816.913	1554.143	5.295	5.292

PinPA_f0_dBm	PoutPA_f0_dBm	GPA_f0_dB	PDC_mW	Drain_Efficiency	PAE
-13.440	19.153	32.593	1554.143	5.295	5.292



$$\text{Eqn} \quad \text{ds_static} = \text{"_06.analyseDCext".Ids_int.i}$$

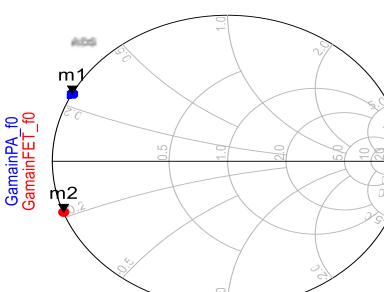
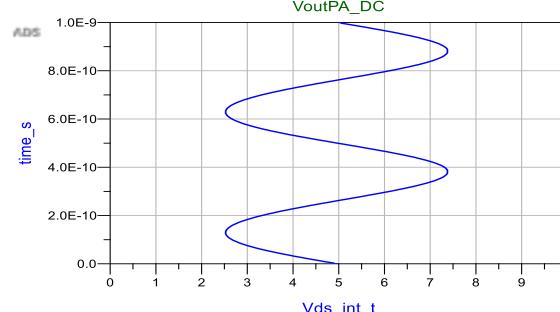
$$\text{Eqn} \quad \text{time_s} = \text{ts(freq)}$$

$$\text{Eqn} \quad \text{Vds_int} = \text{Vdint} - \text{Vsintd}$$

$$\text{Eqn} \quad \text{Vds_int_t} = \text{ts(Vds_int)}$$

$$\text{Eqn} \quad \text{Vgs_int_t} = \text{ts(Vgint-Vsintg)}$$

$$\text{Eqn} \quad \text{Ids_int_t} = \text{ts(Ids_int.i)}$$



$$\begin{array}{ll} \text{ZinFET_f0} & \text{GamainFET_f0} \\ 0.042 - j9.045 & 0.998 / -159.492 \end{array}$$

$$\begin{array}{ll} \text{ZinPA_f0} & \text{GamainPA_f0} \\ 0.060 + j12.211 & 0.998 / 152.552 \end{array}$$

$$\begin{array}{l} \text{m2} \\ \text{indep}(\text{m2})=0 \\ \text{GamainFET_f0}=0.998 / -159.492 \\ \text{impedance} = Z_0 * (8.417E-4 - j0.181) \end{array}$$

$$\begin{array}{l} \text{m1} \\ \text{indep}(\text{m1})=0 \\ \text{GamainPA_f0}=0.998 / 152.552 \\ \text{impedance} = Z_0 * (0.001 + j0.244) \end{array}$$

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- SLCQ
- TF
- CIND
- Kfrep
- Kfertap

Power Source

Power Amplifier

Input Matching Network

RF

Input Bias Tee

RF+DC

DIE FET

Vdsmeas

I_Probe

lntFETmeas

DC_Block

DC_Feed

DC_Feed1

DC

V_DC

Vgsbias

Vgs0=V

HARMONIC BALANCE

HarmonicBalance

HB1

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Order[1]=7

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Stop=10

Step=1

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SaveEquationName[2]=“Lout_H”

SaveEquationName[3]=“Rin”

SaveEquationName[4]=“Nout”

SaveEquationName[5]=“Pgen”

SaveEquationName[6]=“Rin”

SaveEquationName[7]=“Rout”

SaveEquationName[8]=“Rout”

IMN

Nout=sqrt(50/Rin)

Lin_H=2.03e-11

Rin=3.013

V_DC

Vdsbias

Vdc=Vds0 V

Output Bias Tee

RF+DC

DC_Block

DC_Feed2

DC_Feed

DC

V_DC

Vdsbias

Vdc=Vds0 V

Output Matching Network

RF

Output

Vloadmeas

I_Probe

lloadmeas

R

R1

R=50 Ohm

Load

1°) Click the « tuning » button

2°) Select the Parameters to tune : they appear in the « Tune Parameters » window

FLU17XM_student.lib:13.flu17xm_PA_lumped_imag_out:schematic

Rout	Lout_H	Lin_H	Rin	Pgen
Value 17.511	1.488e-1	2.839e-1	3.013	10
Max 26.2665	2.232e-1	4.2585e-1	4.5195	15
Min 8.7555	7.44e-12	1.4195e-1	1.5065	5
Step 1.7511	1.488e-1	2.839e-1	0.3013	1
Scale Lin	Lin	Lin	Lin	Lin

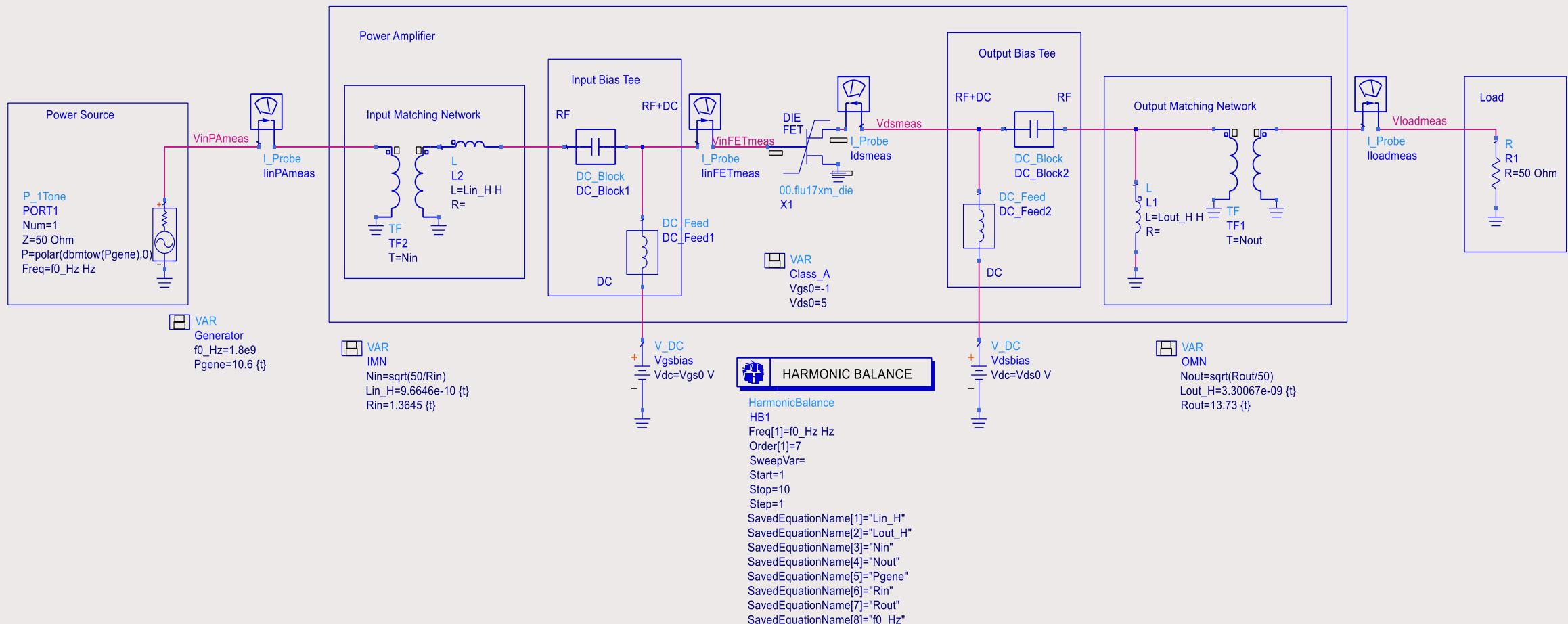
Click a parameter to toggle tuning. Click an instance to open a tuning dialog.

VAR Generator

ads_device:drawing 0.125, -0.500 6.625, 3.125 in

- 28 -

After the tuning of the 5 parameters



E(rasmus) Mundus on Innovative Microwave Electronics and Optics

Results after the tuning of the 5 parameters to maximise the output power of the PA.

Method to tune the parameters

- 1) Tune first Lout_H
- 2) Tune Secondly Rout
- 3) Modify Pgene if required
- 4) Tune again Lout_H
- 5) Tune again Rout
- 6) Tune then Lin_H to cancel Imag(ZinPA)
- 7) Tune Secondly Rin (To match ZinPA=50Ω)
- 8) Modify Pgene if required
- 9) Tune again Lout_H if required
- 10) Tune again Rout if required
- 11) Tune again Lin_H to cancel Imag(ZinPA)
- 12) Tune again Rin (To match ZinPA=50Ω)
- 13) Repeat again step 8 to 12 to maximise the Gain or the output power or the PAE

$$\text{Eqn} \quad \text{VinPA_f0} = \text{VinPAmeas}[1]$$

$$\text{Eqn} \quad \text{VoutPA_f0} = \text{Vloadmeas}[1]$$

$$\text{Eqn} \quad \text{VinPA_DC} = \text{mag}(\text{VinFETmeas}[0])$$

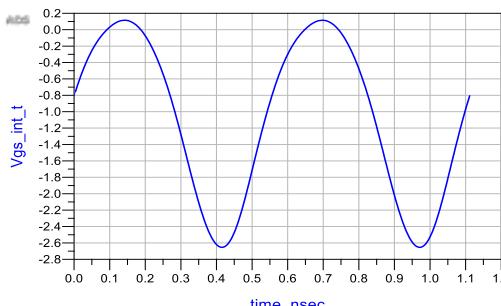
$$\text{Eqn} \quad \text{VoutPA_DC} = \text{mag}(\text{Vdsmeas}[0])$$

$$\text{Eqn} \quad \text{ZinFET_f0} = \text{VinFETmeas}[1]/\text{linFETmeas.i}[1]$$

$$\text{Eqn} \quad \text{ZinPA_f0} = \text{VinPAmeas}[1]/\text{linPAmeas.i}[1]$$

$$\text{Eqn} \quad \text{GamainFET_f0} = (\text{ZinFET_f0}-50)/(\text{ZinFET_f0}+50)$$

$$\text{Eqn} \quad \text{GamainPA_f0} = (\text{ZinPA_f0}-50)/(\text{ZinPA_f0}+50)$$



$$\text{Eqn} \quad \text{ids_static} = "_06.analyseDCext"\..ids_int.i$$

$$\text{Eqn} \quad \text{time_s} = \text{ts(freq)}$$

$$\text{Eqn} \quad \text{Vds_int} = \text{Vdint}\text{-Vsintd}$$

$$\text{Eqn} \quad \text{Vds_int_t} = \text{ts(Vds_int)}$$

$$\text{Eqn} \quad \text{Vgs_int_t} = \text{ts(Vgint-Vsintg)}$$

$$\text{Eqn} \quad \text{Ids_int_t} = \text{ts(Ids_int.i)}$$

$$\text{Eqn} \quad \text{linPA_f0} = \text{linPAmeas.i}[1]$$

$$\text{Eqn} \quad \text{loutPA_f0} = \text{lloadmeas.i}[1]$$

$$\text{Eqn} \quad \text{PinPA_f0_mW} = 0.5 * 1000 * \text{real}(\text{VinPA_f0} * \text{conj}(\text{linPA_f0}))$$

$$\text{Eqn} \quad \text{PinPA_f0_dBm} = 10 * \log10(\text{PinPA_f0_mW})$$

$$\text{Eqn} \quad \text{PoutPA_f0_mW} = 0.5 * 1000 * \text{real}(\text{VoutPA_f0} * \text{conj}(\text{loutPA_f0}))$$

$$\text{Eqn} \quad \text{PoutPA_f0_dBm} = 10 * \log10(\text{PoutPA_f0_mW})$$

$$\text{Eqn} \quad \text{PDC_mW} = 1000 * (\text{VinPA_DC} * \text{linPA_DC} + \text{VoutPA_DC} * \text{loutPA_DC})$$

$$\text{Eqn} \quad \text{GPA_f0} = \text{PoutPA_f0_mW}/\text{PinPA_f0_mW}$$

$$\text{Eqn} \quad \text{GPA_f0_dB} = 10 * \log10(\text{GPA_f0})$$

$$\text{Eqn} \quad \text{PaddPA_f0_mW} = \text{PoutPA_f0_mW} - \text{PinPA_f0_mW}$$

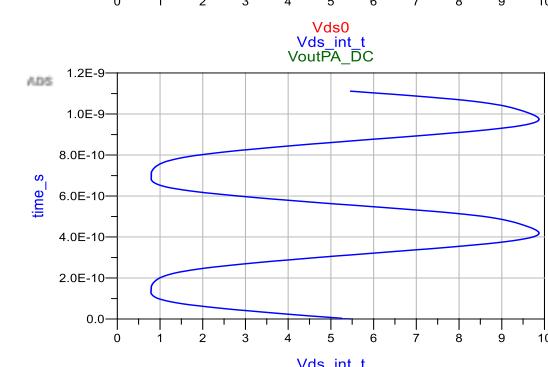
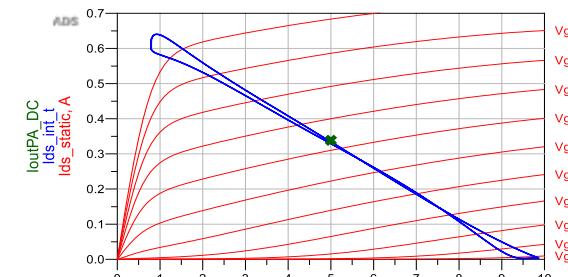
$$\text{Eqn} \quad \text{PaddPA_f0_dBm} = 10 * \log10(\text{PaddPA_f0_mW})$$

$$\text{Eqn} \quad \text{Drain_Efficiency} = \text{PoutPA_f0_mW}/\text{PDC_mW} * 100$$

$$\text{Eqn} \quad \text{PAE} = \text{PaddPA_f0_mW}/\text{PDC_mW} * 100$$

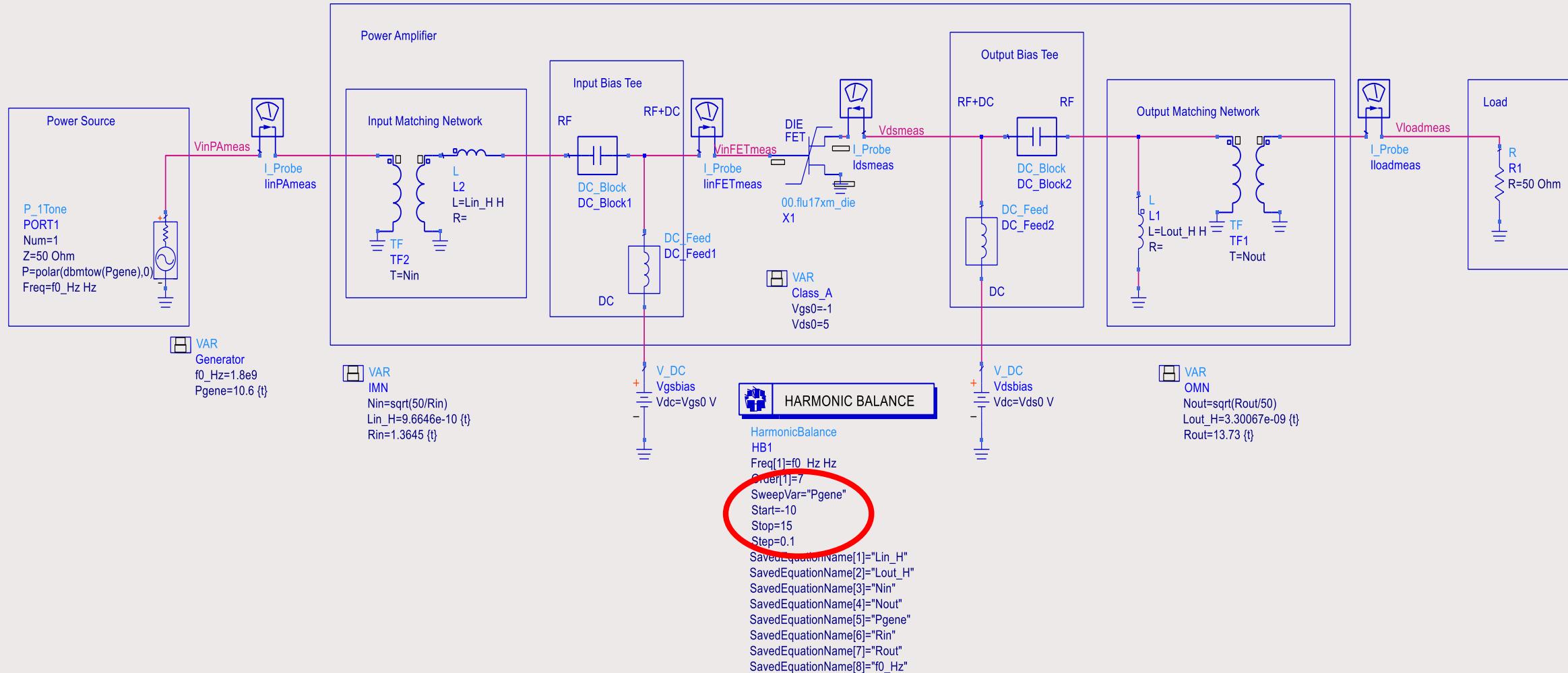
PinPA_f0_mW	PoutPA_f0_mW	GPA_f0	PDC_mW	Drain_Efficiency	PAE
11.482	790.611	68.859	1692.671	46.708	46.030

PinPA_f0_dBm	PoutPA_f0_dBm	GPA_f0_dB	PDC_mW	Drain_Efficiency	PAE
10.600	28.980	18.380	1692.671	46.708	46.030



ZinFET_f0	GamainFET_f0
1.365 - j10.931	0.949 / -155.320

ZinPA_f0	GamainPA_f0
50.024 - j0.004	2.428E-4 / -8.749

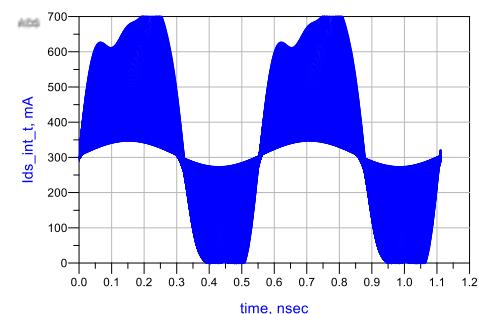
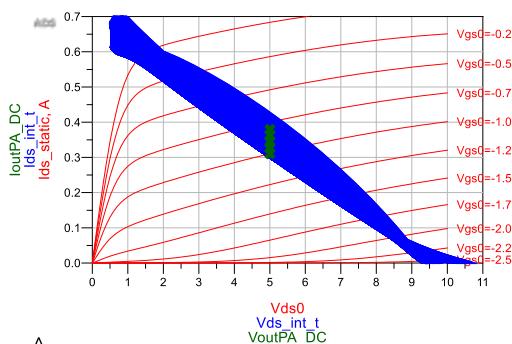
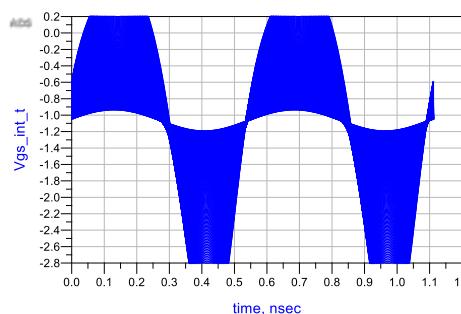


$$\begin{aligned} \text{Eqn } & \text{VinPA_f0=VinPAmeas[1]} & \text{Eqn } & \text{linPA_f0=linPAmeas.i[1]} \\ \text{Eqn } & \text{VoutPA_f0=Vloadmeas[1]} & \text{Eqn } & \text{loutPA_f0=lloadmeas.i[1]} \end{aligned}$$

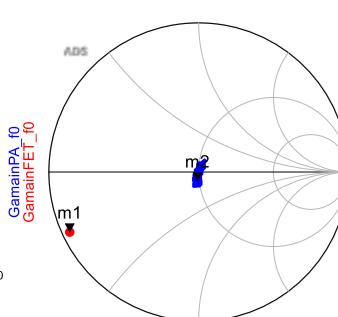
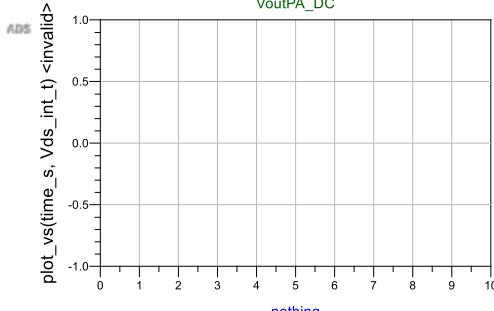
$$\begin{aligned} \text{Eqn } & \text{VinPA_DC=mag(VinFETmeas[i[0])} & \text{Eqn } & \text{linPA_DC=mag(linFETmeas.i[0])} \\ \text{Eqn } & \text{VoutPA_DC=mag(Vdsmeas[0])} & \text{Eqn } & \text{loutPA_DC=mag(ldsmeas.i[0])} \\ \text{Eqn } & \text{PinPA_f0_mW=0.5*1000*real(VinPA_f0*conj(linPA_f0))} \\ \text{Eqn } & \text{PinPA_f0_dBm=10*log10(PinPA_f0_mW)} \\ \text{Eqn } & \text{PoutPA_f0_mW=0.5*1000*real(VoutPA_f0*conj(loutPA_f0))} \\ \text{Eqn } & \text{PoutPA_f0_dBm=10*log10(PoutPA_f0_mW)} \\ \text{Eqn } & \text{PDC_mW=1000*(VinPA_DC*linPA_DC+VoutPA_DC*loutPA_DC)} \\ \text{Eqn } & \text{GPA_f0=PoutPA_f0_mW/PinPA_f0_mW} \\ \text{Eqn } & \text{GPA_f0_dB=10*log10(GPA_f0)} \\ \text{Eqn } & \text{PaddPA_f0_mW=PoutPA_f0_mW-PinPA_f0_mW} \\ \text{Eqn } & \text{PaddPA_f0_dBm=10*log10(PaddPA_f0_mW)} \\ \text{Eqn } & \text{Drain_Efficiency=PoutPA_f0_mW/PDC_mW*100} \\ \text{Eqn } & \text{PAE=PaddPA_f0_mW/PDC_mW*100} \end{aligned}$$

$$\begin{aligned} \text{Eqn } & \text{ZinFET_f0=VinFETmeas[1]/linFETmeas.i[1]} \\ \text{Eqn } & \text{ZinPA_f0=VinPAmeas[1]/linPAmeas.i[1]} \\ \text{Eqn } & \text{GamainFET_f0=(ZinFET_f0-50)/(ZinFET_f0+50)} \\ \text{Eqn } & \text{GamainPA_f0=(ZinPA_f0-50)/(ZinPA_f0+50)} \end{aligned}$$

Pgene	PinPA_f0_mW	...tPA_f0_mW	GPA_f0	PDC_mW	...in_Efficiency	PAE
-10.000	0.099	9.234	92.811	1551.479	0.595	0.589
Pgene	...PA_f0_dBm	...tPA_f0_dBm	GPA_f0_dB	PDC_mW	...in_Efficiency	PAE
-10.000	-10.022	9.654	19.676	1551.479	0.595	0.589



$$\begin{aligned} \text{Eqn } & \text{Ids_static="06.analyseDCext"..Ids_int.i} \\ \text{Eqn } & \text{time_s=ts(freq)} \\ \text{Eqn } & \text{Vds_int=Vdint-Vsintd} \\ \text{Eqn } & \text{Vds_int_t=ts(Vds_int)} \\ \text{Eqn } & \text{Vgs_int_t=ts(Vgint-Vsintg)} \\ \text{Eqn } & \text{Ids_int_t=ts(Ids_int.i)} \end{aligned}$$

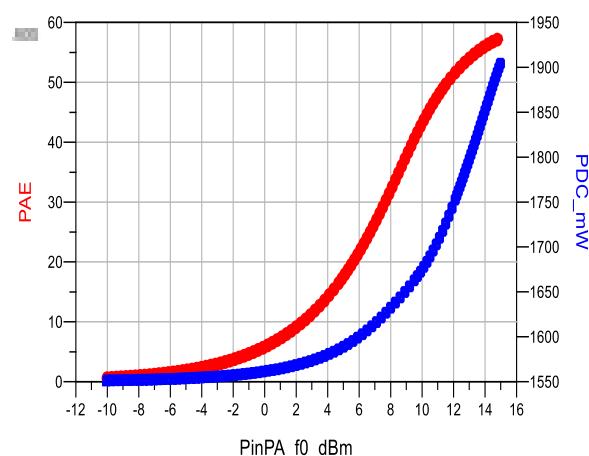
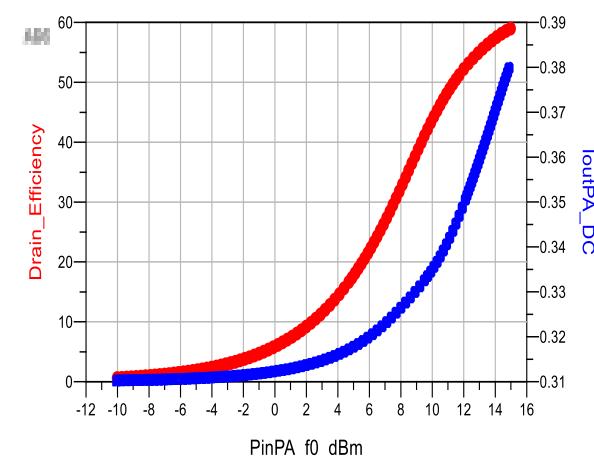
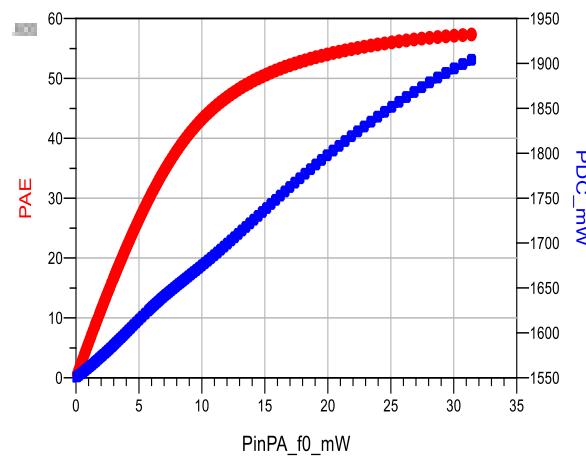
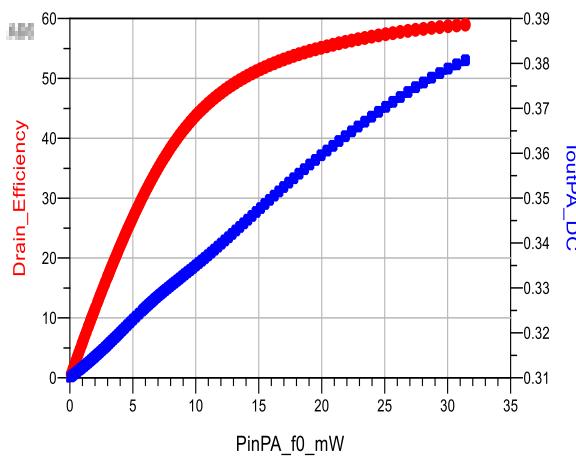
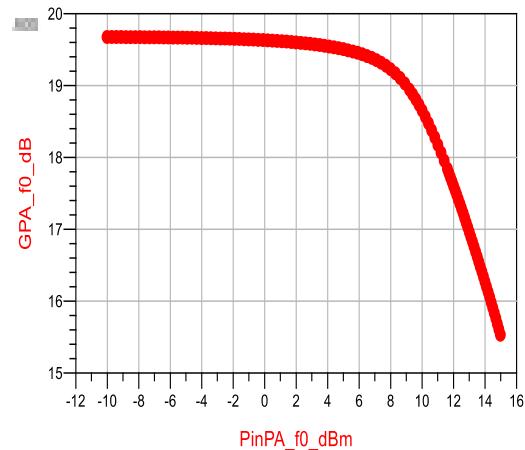
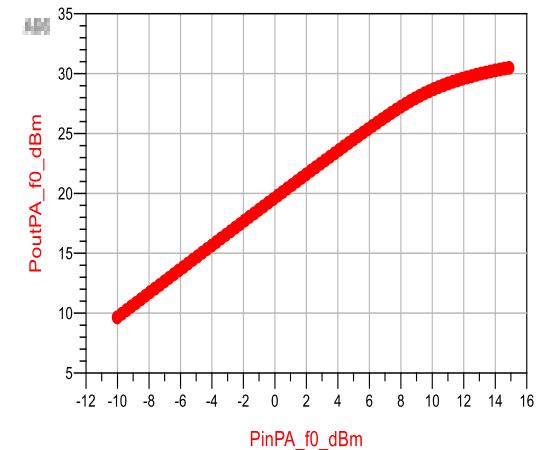
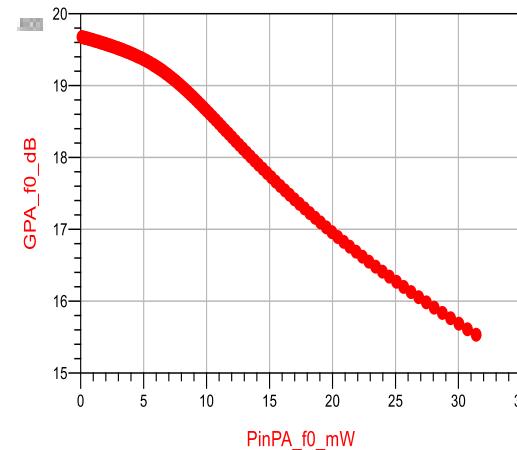
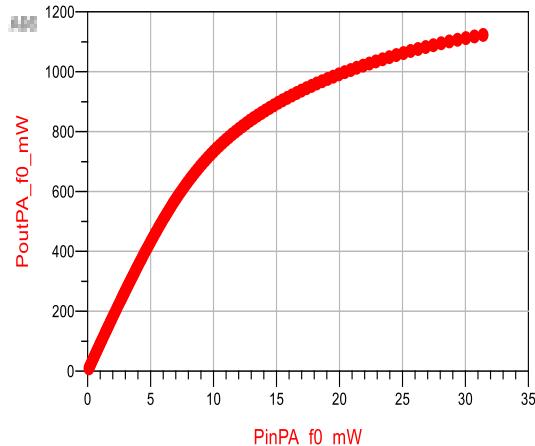


Pgene	ZinFET_f0	...ainFET_f0
-10.000	$1.332 + j11.11$	$0.951 / -154.2^\circ$
-9.900	$1.332 - j11.11$	$0.951 / -154.2^\circ$

Pgene	ZinPA_f0	...mainPA_f0
-10.000	$48.798 - j6.66$	$0.071 / -95.0^\circ$
-9.900	$48.798 - j6.66$	$0.071 / -95.0^\circ$

m1
Pgene=1.879E-14
GamainFET_f0=0.950 / -154.969
impedance = $Z_0 * (0.027 + j0.222)$

m2
Pgene=1.879E-14
GamainPA_f0=0.061 / -97.558
impedance = $Z_0 * (0.977 + j0.118)$



PA Design with the packaged transistor and transmission Lines

LineCalc/untitled

File Simulation Options Help

Lumpers

Component

Type MLIN ID MLIN: MLIN_DEFAULT

Substrate Parameters

ID MSUB_DEFAULT

Er	4.700	N/A
Mur	1.000	N/A
H	1.590	mm
Hu	3.9e+34	mil
T	25.000	um
Cond	1e50	N/A

Physical

W 2.876950 mm
L 22.219500 mm

Synthesize **Analyze**

Calculated Results

K_Eff = 3.511
A_DB = 0.125
SkinDepth = 0.000

Component Parameters

Freq 1.800 GHz
Wall1 mil
Wall2 mil

Values are consistent

MSub

MSUB
MSub1
H=1.59 mm
Er=4.7
Mur=1
Cond=1.0E+50
Hu=3.9e+034 mil
T=35 um
TanD=0.02
Rough=0 mil

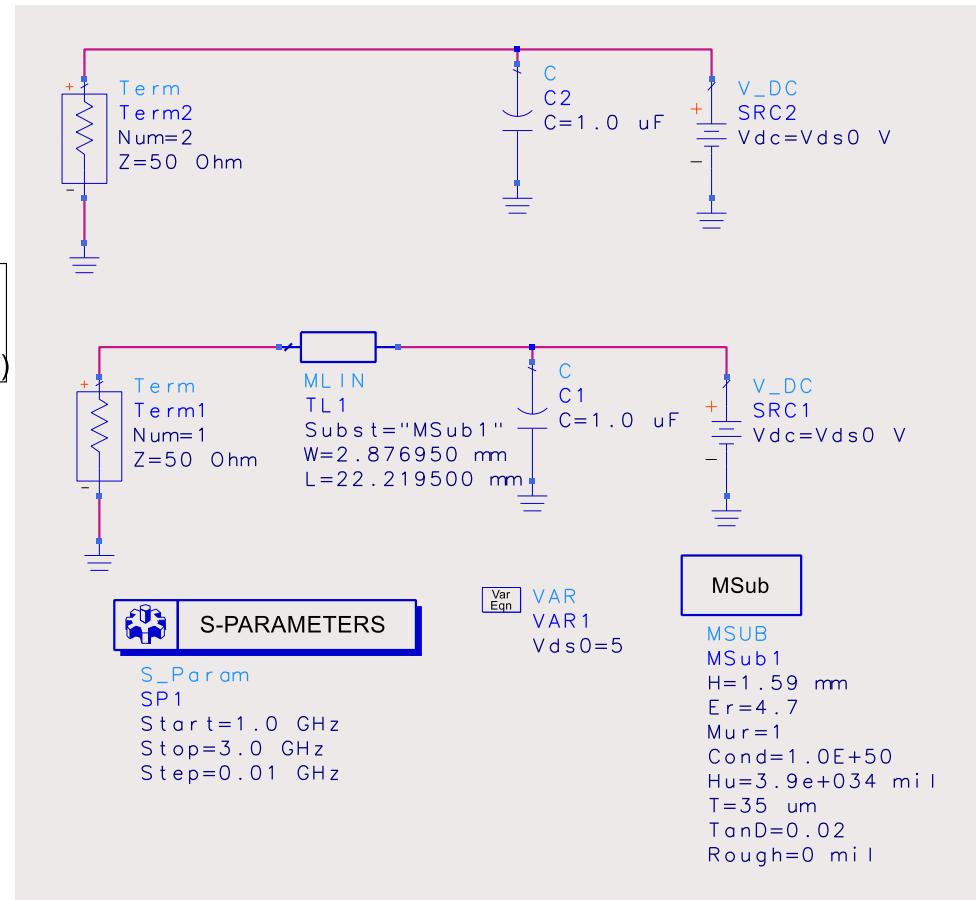
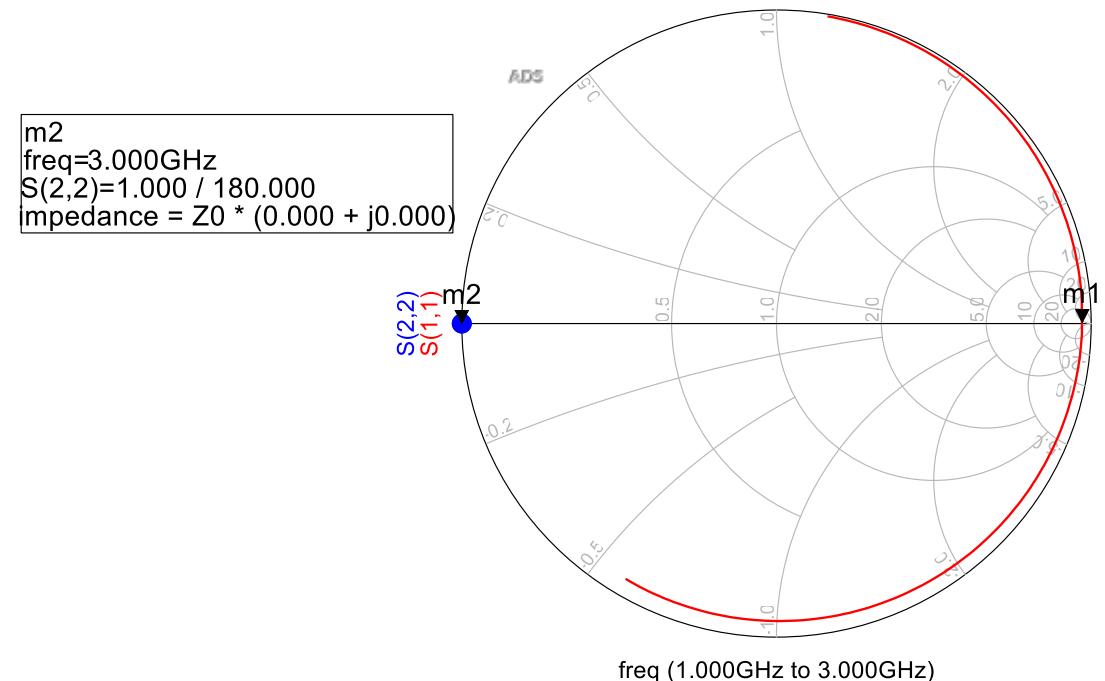
Circuit Diagram

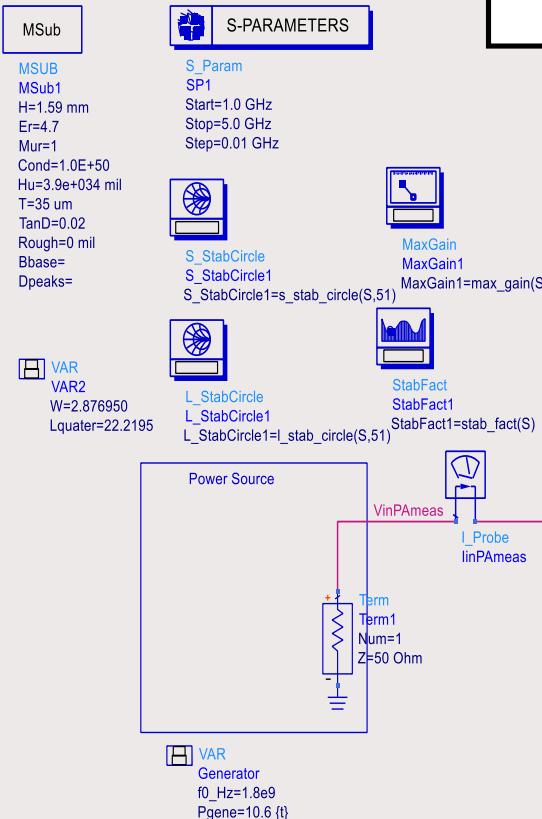
```

    graph LR
        VDC1[V_DC SRC1] --> C1[C1 1.0 uF]
        C1 --> MLIN[MLIN TL1]
        MLIN --> C2[C2 1.0 uF]
        C2 --> VDC2[V_DC SRC2]
        MLIN --> SParam[S-PARAMETERS]
        SParam --> VAR1[VAR1 Vds0=5]
    
```

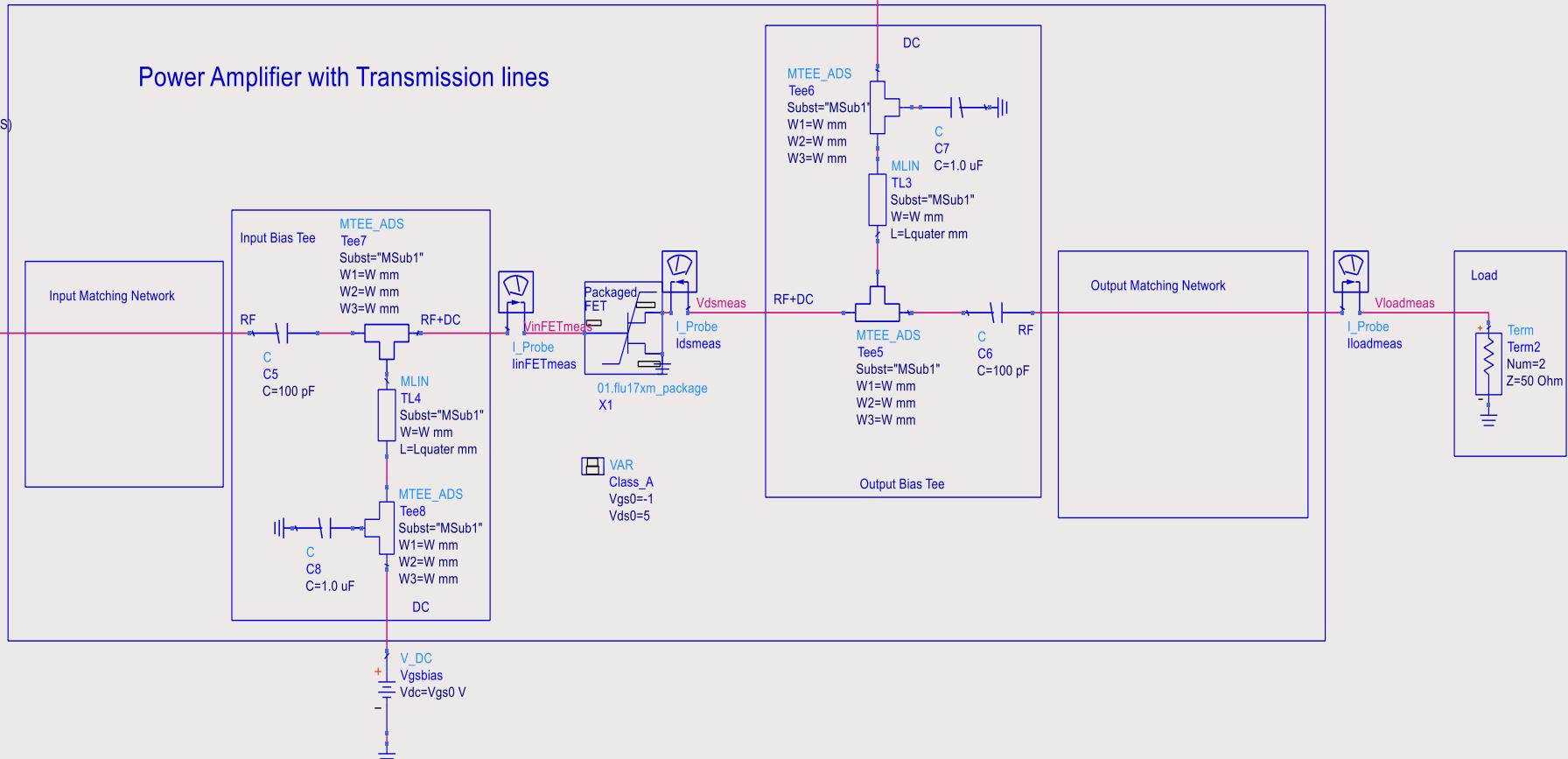
S-PARAMETERS

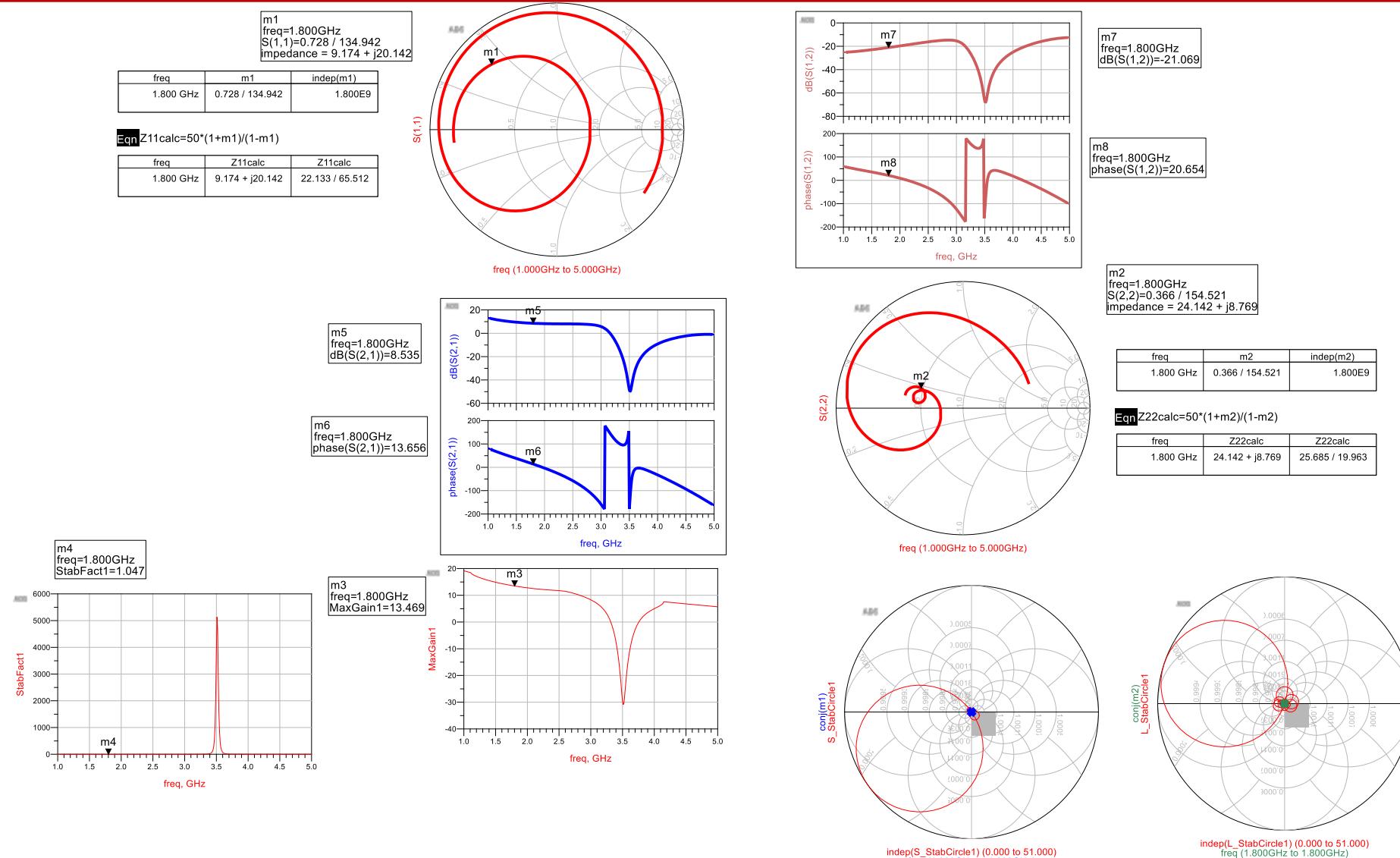
S_Param
SP1
Start=1.0 GHZ
Stop=3.0 GHZ
Step=0.01 GHZ



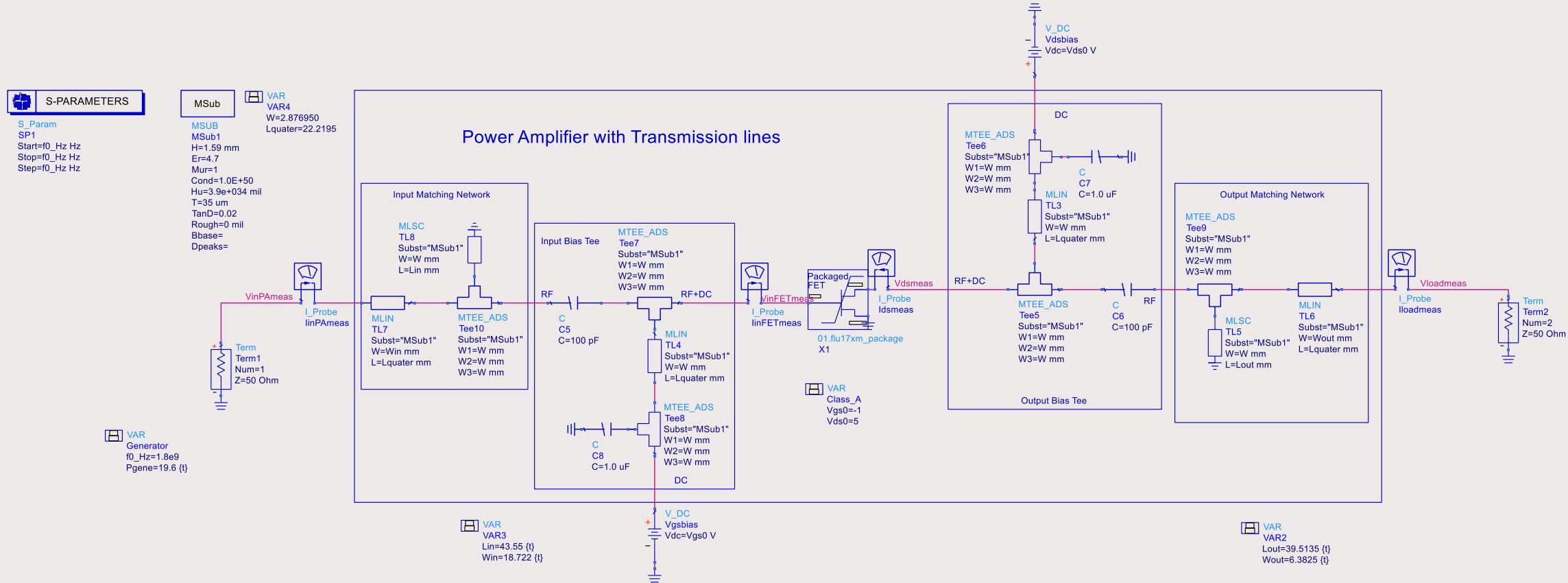


Initial Schematic to plot the Sparameter of the packaged transistor:
 « 16.flu17xm_packaged_PA_TL_step_02_bias tee_Sparam »





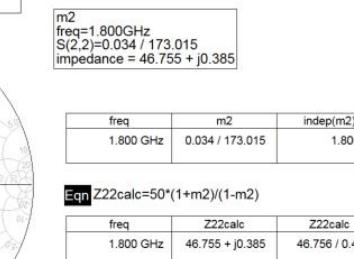
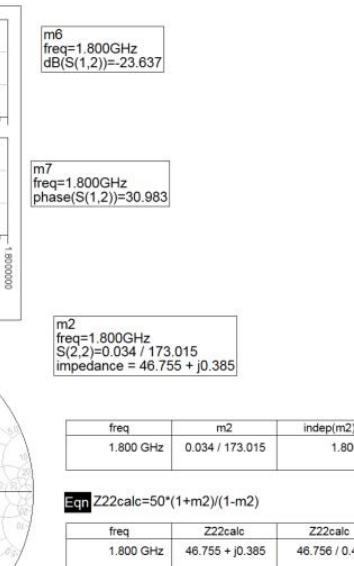
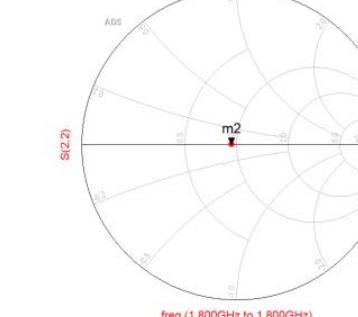
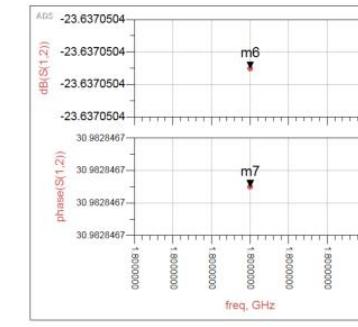
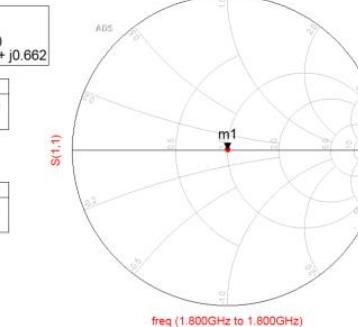
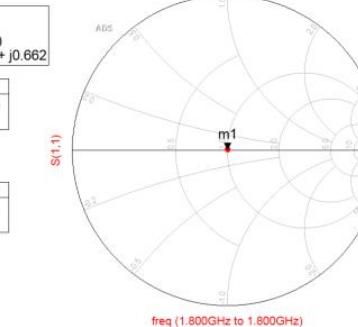
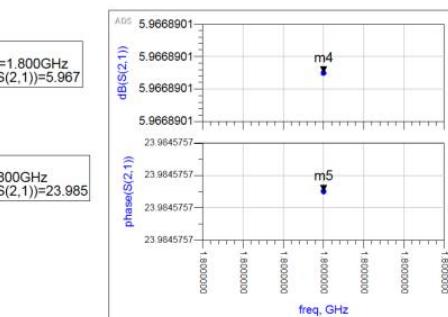
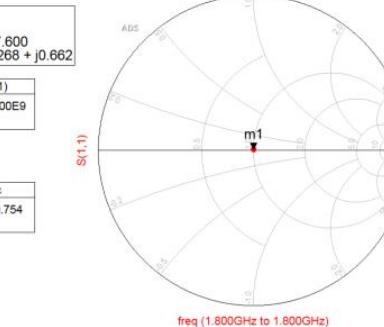
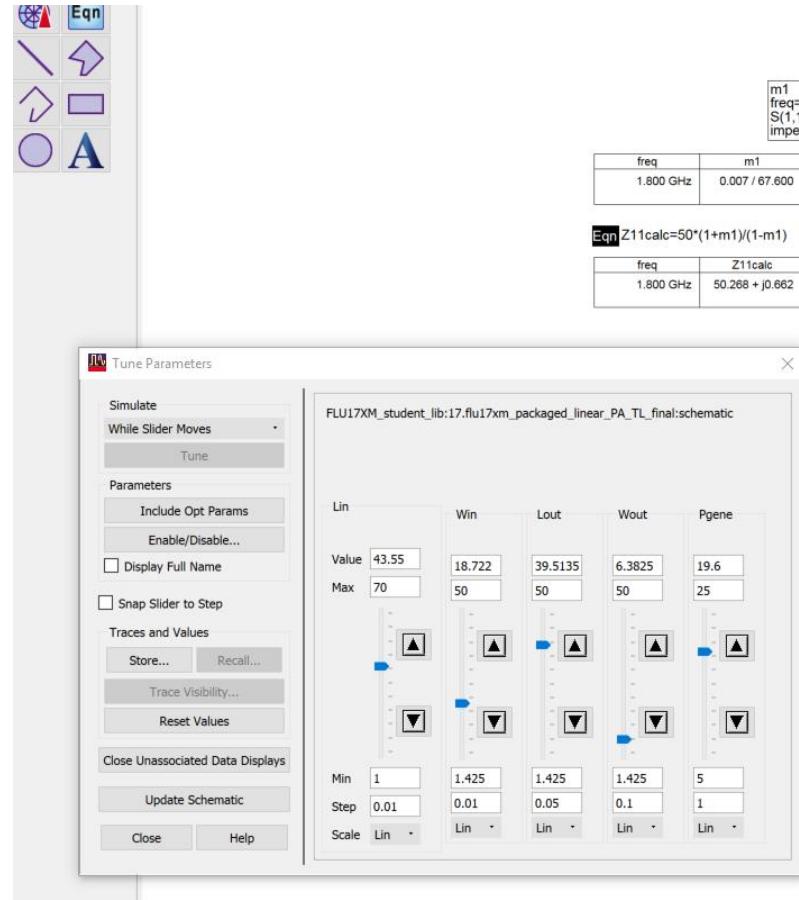
Final Schematic to design a linear PA : « 17.flu17xm_packaged_linear_PA_TL_final »

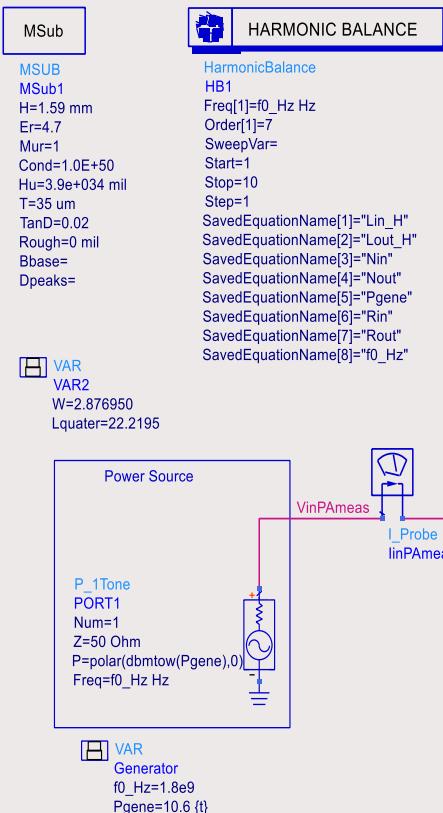


Results after the tuning of the 4 parameters to match the PA.

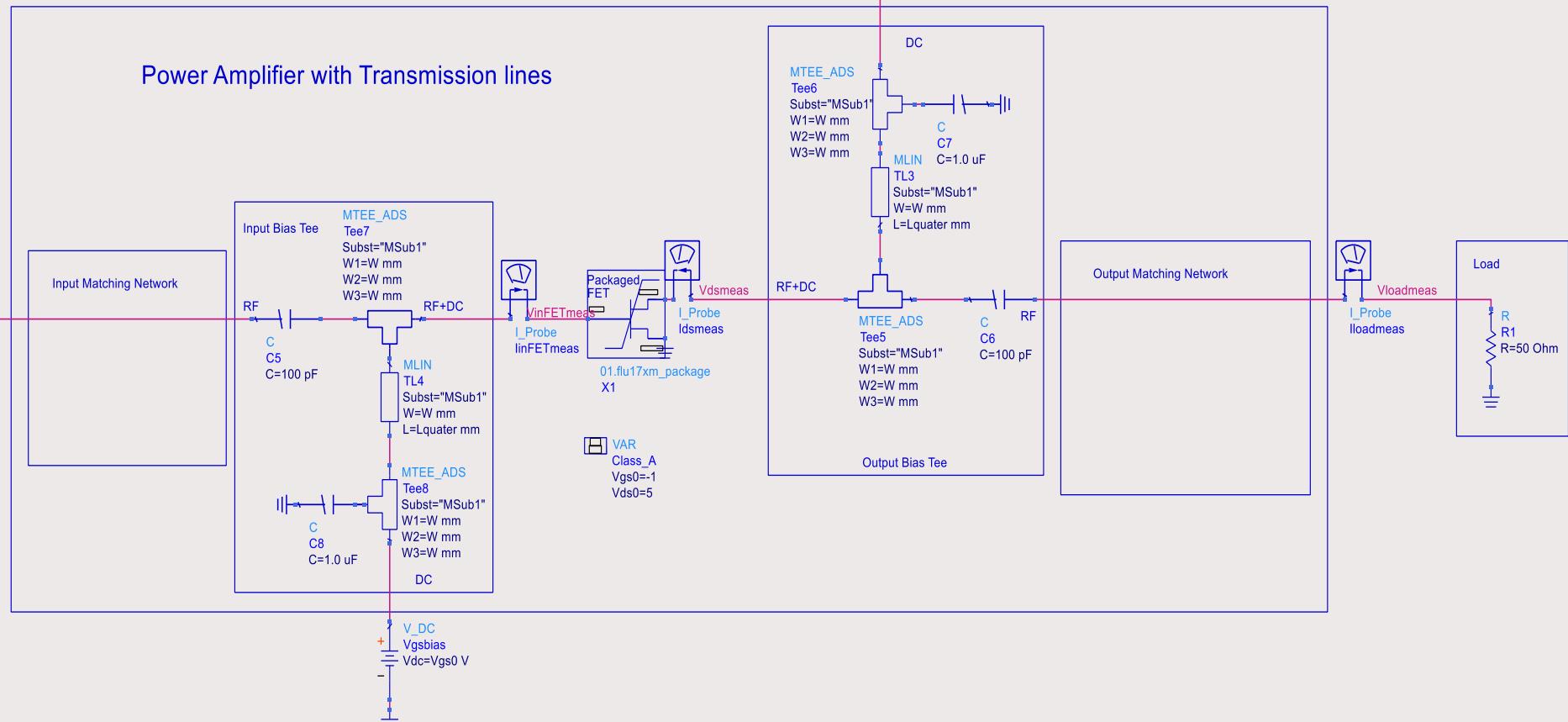
Method to tune the parameters

- 1) Tune first Lout
- 2) Tune Secondly Wout
- 3) Tune then Lin to cancel Imag(ZinPA)
- 4) Tune Secondly Win (To match ZinPA=50Ω)
- 5) Tune again Lout_H if required
- 6) Tune again Rout if required
- 7) Tune again Lin_H to cancel Imag(ZinPA)
- 8) Tune again Rin (To match ZinPA=50Ω)
- 9) Repeat again step 5 to 8 to better match the PA





Initial Schematic to design a Power PA :
« 18.flu17xm_packaged_Power_PA_TL_final »



$$\text{Eqn } \text{VinPA_f0} = \text{VinPAmeas[1]}$$

$$\text{Eqn } \text{VoutPA_f0} = \text{Vloadmeas[1]}$$

$$\text{Eqn } \text{linPA_f0} = \text{linPAmeas.i[1]}$$

$$\text{Eqn } \text{loutPA_f0} = \text{lloadmeas.i[1]}$$

$$\text{Eqn } \text{PinPA_f0_mW} = 0.5 * 1000 * \text{real}(\text{VinPA_f0} * \text{conj}(\text{linPA_f0}))$$

$$\text{Eqn } \text{PinPA_f0_dBm} = 10 * \log10(\text{PinPA_f0_mW})$$

$$\text{Eqn } \text{GPA_f0} = \text{PoutPA_f0_mW} / \text{PinPA_f0_mW}$$

$$\text{Eqn } \text{GPA_f0_dB} = 10 * \log10(\text{GPA_f0})$$

$$\text{Eqn } \text{VinPA_DC} = \text{mag}(\text{VinFETmeas[0]}) \quad \text{Eqn } \text{linPA_DC} = \text{mag}(\text{linFETmeas.i[0]})$$

$$\text{Eqn } \text{VoutPA_DC} = \text{mag}(\text{Vdsmeas[0]}) \quad \text{Eqn } \text{loutPA_DC} = \text{mag}(\text{ldsmeas.i[0]})$$

$$\text{Eqn } \text{PoutPA_f0_mW} = 0.5 * 1000 * \text{real}(\text{VoutPA_f0} * \text{conj}(\text{loutPA_f0}))$$

$$\text{Eqn } \text{PoutPA_f0_dBm} = 10 * \log10(\text{PoutPA_f0_mW})$$

$$\text{Eqn } \text{PaddPA_f0_mW} = \text{PoutPA_f0_mW} - \text{PinPA_f0_mW}$$

$$\text{Eqn } \text{PaddPA_f0_dBm} = 10 * \log10(\text{PaddPA_f0_mW})$$

$$\text{Eqn } \text{ZinFET_f0} = \text{VinFETmeas[1]} / \text{linFETmeas.i[1]}$$

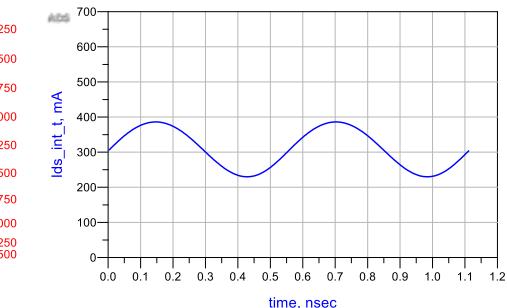
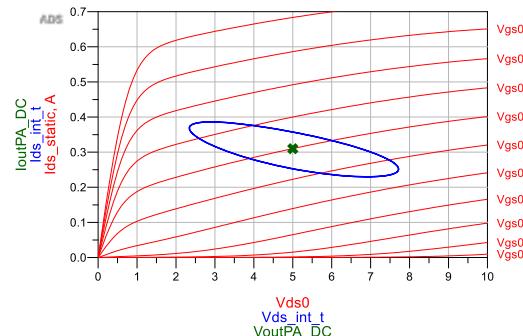
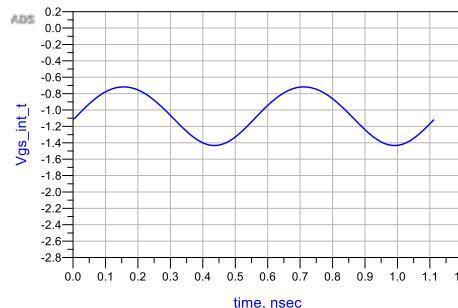
$$\text{Eqn } \text{ZinPA_f0} = \text{VinPAmeas[1]} / \text{linPAmeas.i[1]}$$

$$\text{Eqn } \text{GamainFET_f0} = (\text{ZinFET_f0} - 50) / (\text{ZinFET_f0} + 50)$$

$$\text{Eqn } \text{GamainPA_f0} = (\text{ZinPA_f0} - 50) / (\text{ZinPA_f0} + 50)$$

PinPA_f0_mW	PoutPA_f0_mW	GPA_f0	PDC_mW	Drain_Efficiency	PAE
5.381	81.252	15.099	1548.953	5.246	4.898

PinPA_f0_dBm	PoutPA_f0_dBm	GPA_f0_dB	PDC_mW	Drain_Efficiency	PAE
7.309	19.098	11.790	1548.953	5.246	4.898



$$\text{Eqn } \text{ids_static} = \text{"_06.analyseDCext".Ids_int.i}$$

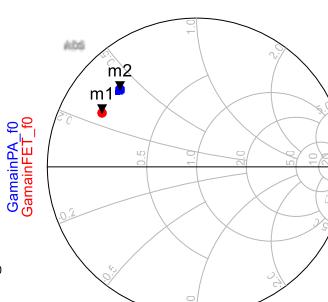
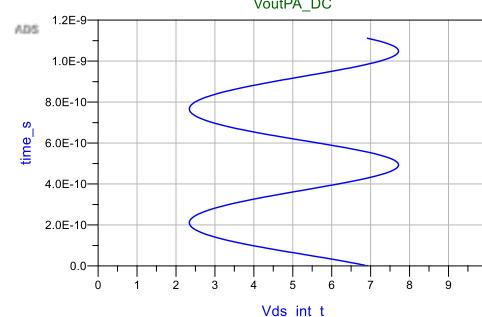
$$\text{Eqn } \text{time_s} = \text{ts(freq)}$$

$$\text{Eqn } \text{Vds_int} = \text{Vdint-Vsintd}$$

$$\text{Eqn } \text{Vds_int_t} = \text{ts(Vds_int)}$$

$$\text{Eqn } \text{Vgs_int_t} = \text{ts(Vgint-Vsintg)}$$

$$\text{Eqn } \text{Ids_int_t} = \text{ts(Ids_int.i)}$$



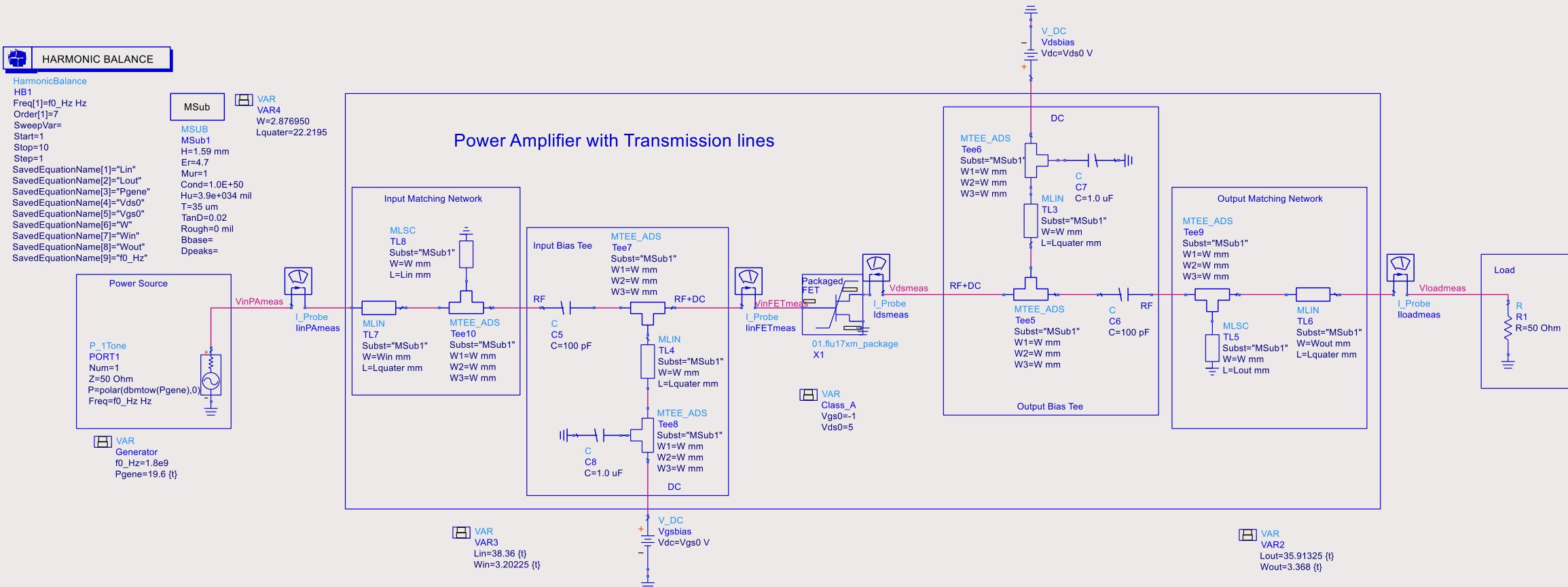
$$\begin{array}{|c|c|} \hline \text{ZinFET_f0} & \text{GamainFET_f0} \\ \hline 8.359 + j12.951 & 0.729 / 150.212 \\ \hline \end{array}$$

$$\begin{array}{|c|c|} \hline \text{ZinPA_f0} & \text{GamainPA_f0} \\ \hline 9.161 + j20.229 & 0.729 / 134.772 \\ \hline \end{array}$$

$$\begin{array}{|c|} \hline \text{m1} \\ \hline \text{indep(m1)=0} \\ \text{GamainFET_f0}=0.729 / 150.212 \\ \text{impedance} = Z_0 * (0.167 + j0.259) \\ \hline \end{array}$$

$$\begin{array}{|c|} \hline \text{m2} \\ \hline \text{indep(m2)=0} \\ \text{GamainPA_f0}=0.729 / 134.772 \\ \text{impedance} = Z_0 * (0.183 + j0.405) \\ \hline \end{array}$$

Final Schematic to design a Power PA : « 18.flu17xm_packaged_Power_PA_TL_final »



E(rasmus) Mundus on Innovative Microwave Electronics and Optics

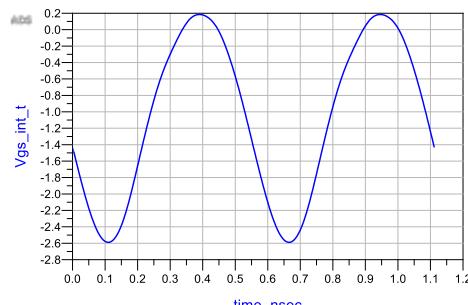
Results after the tuning of the 5 parameters to maximise the output power of the PA.

Method to tune the parameters

- 1) Tune first Lout
- 2) Tune Secondly Wout
- 3) Modify Pgene if required
- 4) Tune again Lout
- 5) Tune again Wout
- 6) Tune then Lin to cancel Imag(ZinPA)
- 7) Tune Secondly Win (To match ZinPA=50Ω)
- 8) Modify Pgene if required
- 9) Tune again Lout_H if required
- 10) Tune again Rout if required
- 11) Tune again Lin_H to cancel Imag(ZinPA)
- 12) Tune again Rin (To match ZinPA=50Ω)
- 13) Repeat again step 8 to 12 to maximise the Gain or the output power or the PAE

$\text{Eqn} \text{VinPA_f0}=\text{VinPAmeas}[1]$	$\text{Eqn} \text{loutPA_f0}=\text{loutPAmeas}.i[1]$	$\text{Eqn} \text{PinPA_f0_mW}=0.5*1000*\text{real}(\text{VinPA_f0}*\text{conj}(\text{loutPA_f0}))$	$\text{Eqn} \text{GPA_f0}=\text{PoutPA_f0_mW}/\text{PinPA_f0_mW}$
$\text{Eqn} \text{VoutPA_f0}=\text{Vloadmeas}[1]$	$\text{Eqn} \text{lloadmeas}.i[1]$	$\text{Eqn} \text{PinPA_f0_dBm}=10*\log10(\text{PinPA_f0_mW})$	$\text{Eqn} \text{GPA_f0_dB}=10*\log10(\text{GPA_f0})$
$\text{Eqn} \text{VinPA_DC}=\text{mag}(\text{VinFETmeas}[0])$	$\text{Eqn} \text{loutPA_DC}=\text{mag}(\text{loutFETmeas}.i[0])$	$\text{Eqn} \text{PoutPA_f0_mW}=0.5*1000*\text{real}(\text{VoutPA_f0}*\text{conj}(\text{loutPA_f0}))$	$\text{Eqn} \text{PaddPA_f0_mW}=\text{PoutPA_f0_mW}-\text{PinPA_f0_mW}$
$\text{Eqn} \text{VoutPA_DC}=\text{mag}(\text{Vdsmeas}[0])$	$\text{Eqn} \text{loutPA_DC}=\text{mag}(\text{ldsmeas}.i[0])$	$\text{Eqn} \text{PoutPA_f0_dBm}=10*\log10(\text{PoutPA_f0_mW})$	$\text{Eqn} \text{PaddPA_f0_dBm}=10*\log10(\text{PaddPA_f0_mW})$
		$\text{Eqn} \text{PDC_mW}=1000*(\text{VinPA_DC}*\text{loutPA_DC}+\text{VoutPA_DC}*\text{loutPA_DC})$	$\text{Eqn} \text{Drain_Efficiency}=\text{PoutPA_f0_mW}/\text{PDC_mW}*100$
		$\text{Eqn} \text{PAE}=\text{PaddPA_f0_mW}/\text{PDC_mW}*100$	

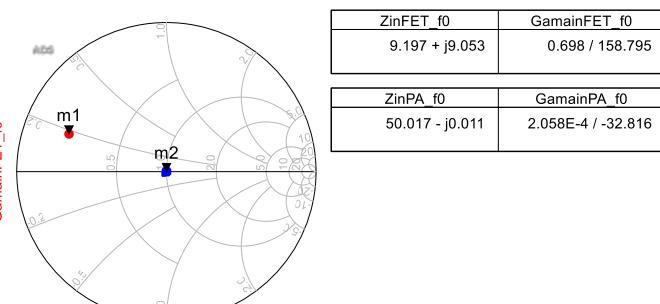
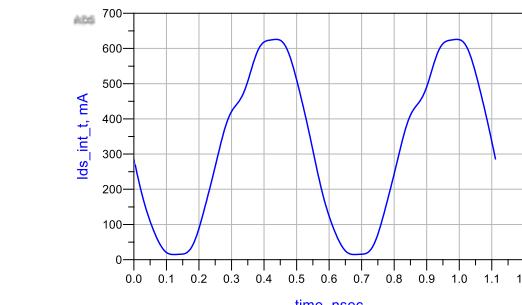
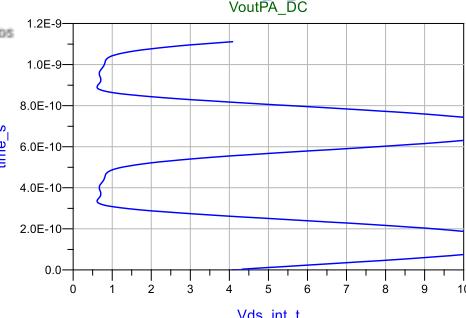
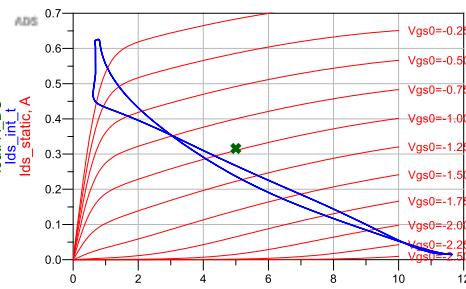
$\text{Eqn} \text{ZinFET_f0}=\text{VinFETmeas}[1]/\text{linFETmeas}.i[1]$
$\text{Eqn} \text{ZinPA_f0}=\text{VinPAmeas}[1]/\text{linPAmeas}.i[1]$
$\text{Eqn} \text{GamainFET_f0}=(\text{ZinFET_f0}-50)/(\text{ZinFET_f0}+50)$
$\text{Eqn} \text{GamainPA_f0}=(\text{ZinPA_f0}-50)/(\text{ZinPA_f0}+50)$



$\text{Eqn} \text{ds_static}=\text{"_06.analyseDCext"}.i.\text{lds_int.i}$
$\text{Eqn} \text{time_s}=\text{ts(freq)}$
$\text{Eqn} \text{Vds_int}=\text{Vdint}-\text{Vsintd}$
$\text{Eqn} \text{Vds_int_t}=\text{ts(Vds_int)}$
$\text{Eqn} \text{Vgs_int_t}=\text{ts(Vgint-Vsintg)}$
$\text{Eqn} \text{Ids_int_t}=\text{ts(Ids_int.i)}$

PinPA_f0_mW	PoutPA_f0_mW	GPA_f0	PDC_mW	Drain_Efficiency	PAE
91.201	851.197	9.333	1580.144	53.868	48.097

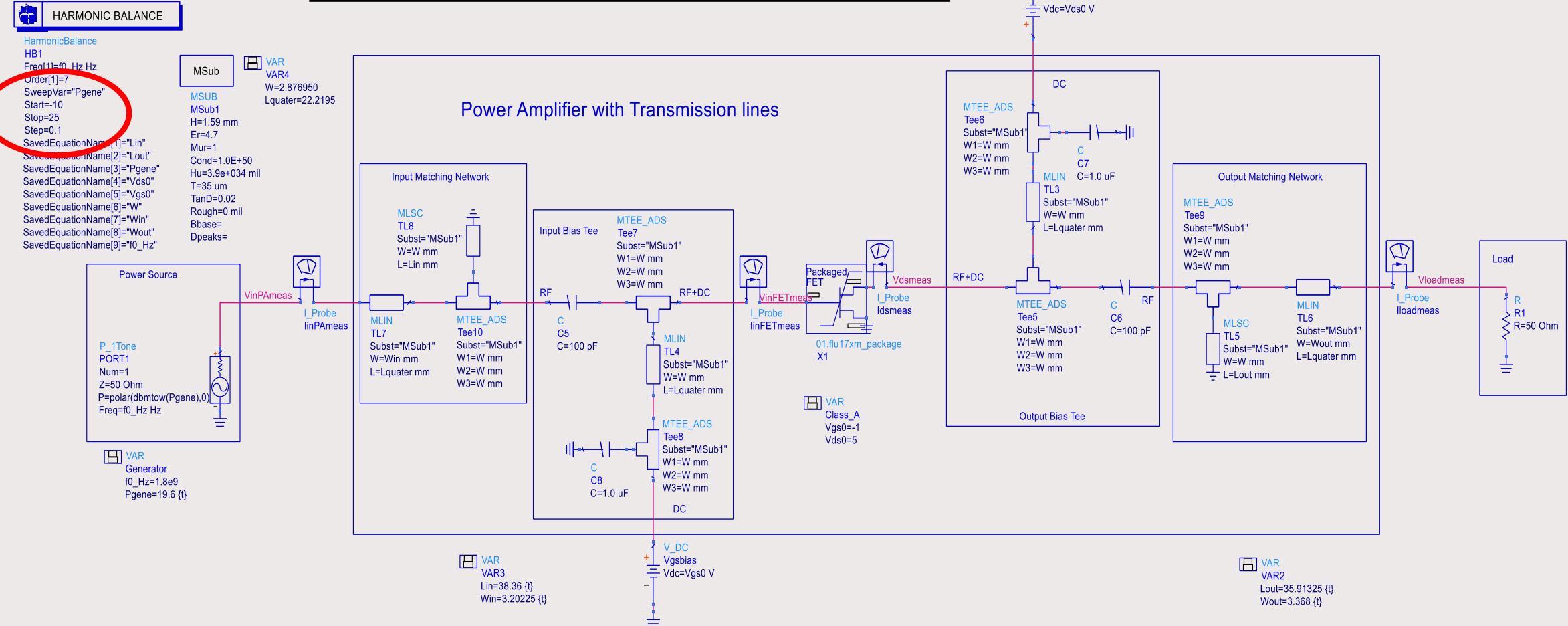
PinPA_f0_dBm	PoutPA_f0_dBm	GPA_f0_dB	PDC_mW	Drain_Efficiency	PAE
19.600	29.300	9.700	1580.144	53.868	48.097



$m1$	$\text{indep}(m1)=0$
	$\text{GamainFET_f0}=0.698 / 158.795$
	$\text{Impedance} = Z_0 * (0.184 + j0.181)$

$m2$	$\text{indep}(m2)=0$
	$\text{GamainPA_f0}=2.058E-4 / -32.816$
	$\text{Impedance} = Z_0 * (1.000 - j2.231E-4)$

Schematic to plot the power characteristics of the designed Power PA :
 « 18.flu17xm_packaged_Power_PA_TL_final »



Eqn VinPA_f0=VinPAmeas[1]	Eqn linPA_f0=linPAmeas.i[1]	Eqn PinPA_f0_mW=0.5*1000*real(VinPA_f0*conj(linPA_f0))	Eqn GPA_f0=PoutPA_f0_mW/PinPA_f0_mW
Eqn VoutPA_f0=Vloadmeas[1]	Eqn loutPA_f0=lloadmeas.i[1]	Eqn PinPA_f0_dBm=10*log10(PinPA_f0_mW)	Eqn GPA_f0_dB=10*log10(GPA_f0)
Eqn VinPA_DC=mag(VinFETmeas[0])	Eqn linPA_DC=mag(linFETmeas.i[0])	Eqn PoutPA_f0_mW=0.5*1000*real(VoutPA_f0*conj(loutPA_f0))	Eqn PaddPA_f0_mW=PoutPA_f0_mW-PinPA_f0_mW
Eqn VoutPA_DC=mag(Vdsmeas[0])	Eqn loutPA_DC=mag(ldsmeas.i[0])	Eqn PoutPA_f0_dBm=10*log10(PoutPA_f0_mW)	Eqn PaddPA_f0_dBm=10*log10(PaddPA_f0_mW)
		Eqn PDC_mW=1000*(VinPA_DC*linPA_DC+VoutPA_DC*loutPA_DC)	Eqn Drain_Efficiency=PoutPA_f0_mW/PDC_mW*100
			Eqn PAE=PaddPA_f0_mW/PDC_mW*100

Eqn ZinFET_f0=VinFETmeas[1]/linFETmeas.i[1]

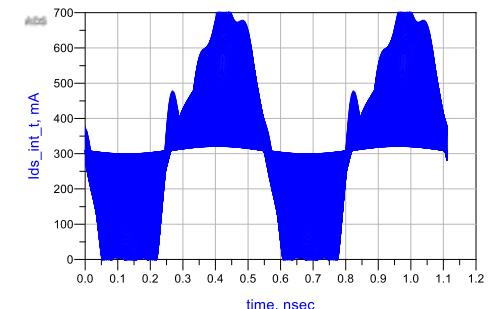
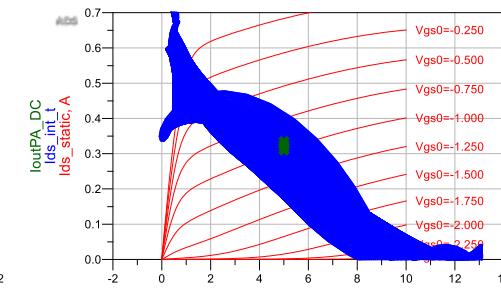
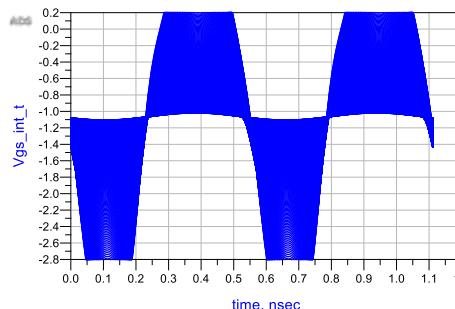
Eqn ZinPA_f0=VinPAmeas[1]/linPAmeas.i[1]

Eqn GamainFET_f0=(ZinFET_f0-50)/(ZinFET_f0+50)

Eqn GamainPA_f0=(ZinPA_f0-50)/(ZinPA_f0+50)

Pgene	PinPA_f0_mW	...tPA_f0_mW	GPA_f0	PDC_mW	...in_Efficiency	PAE
-10.000	0.100	1.112	11.174	1550.420	0.072	0.065

Pgene	...PA_f0_dBm	...tPA_f0_dBm	GPA_f0_dB	PDC_mW	...in_Efficiency	PAE
-10.000	-10.021	0.461	10.482	1550.420	0.072	0.065



Eqn Ids_static=".06.analyseDCext"..Ids_int.i

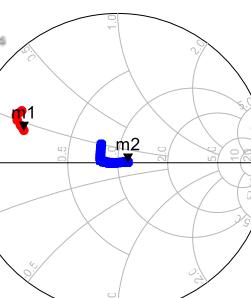
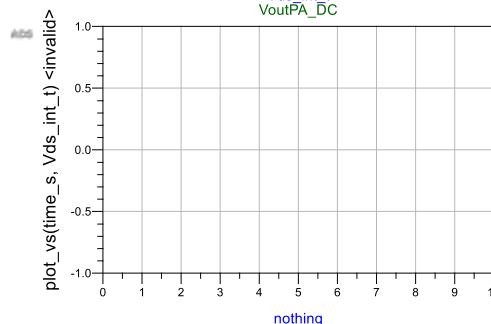
Eqn time_s=ts(freq)

Eqn Vds_int=Vdint-Vsintd

Eqn Vds_int_t=ts(Vds_int)

Eqn Vgs_int_t=ts(Vgint-Vsintg)

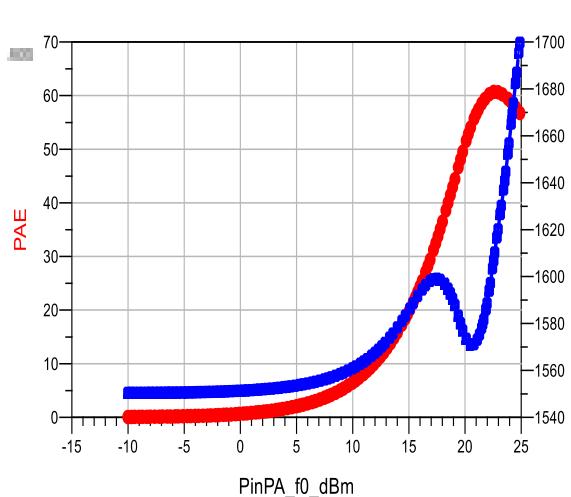
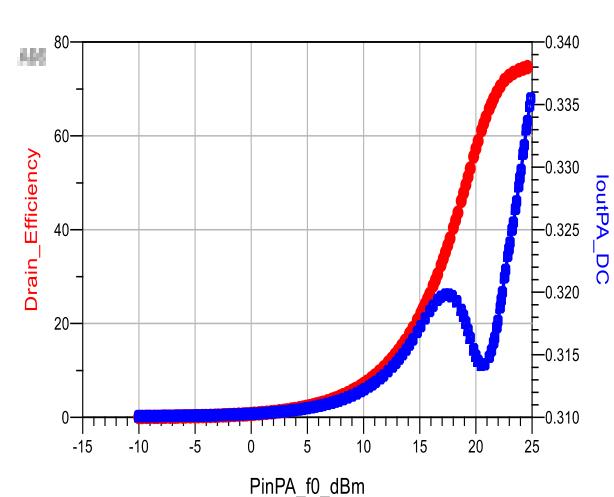
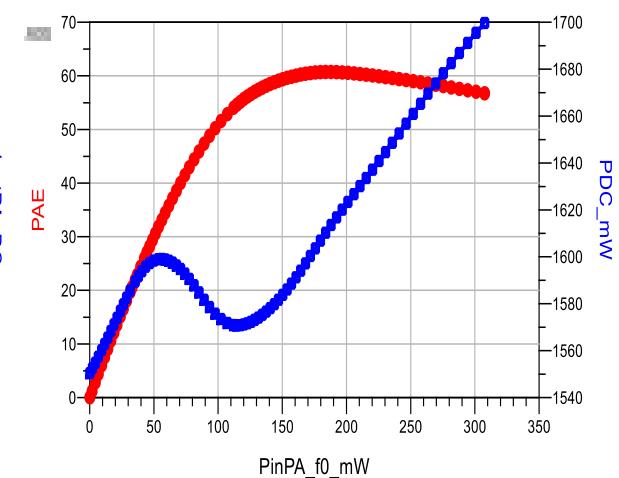
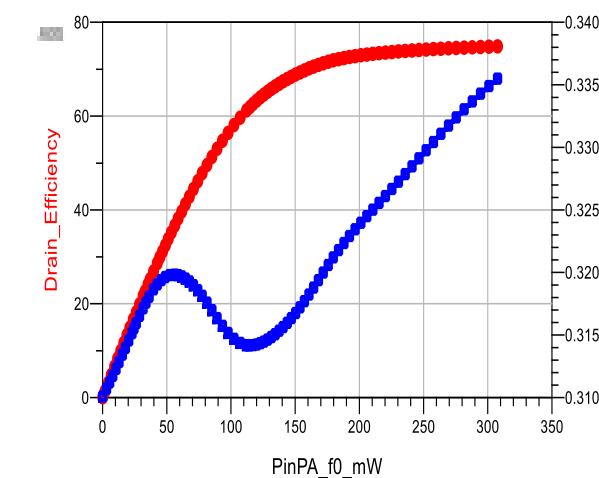
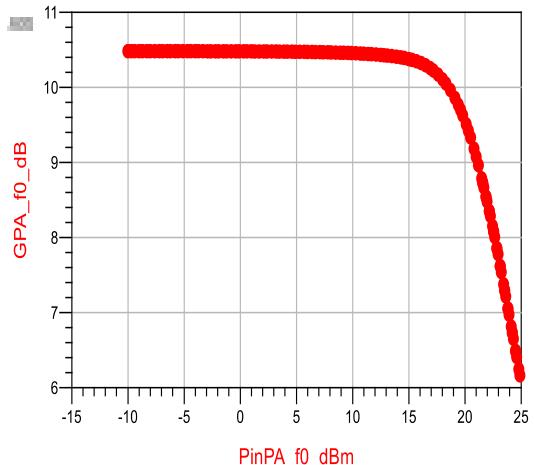
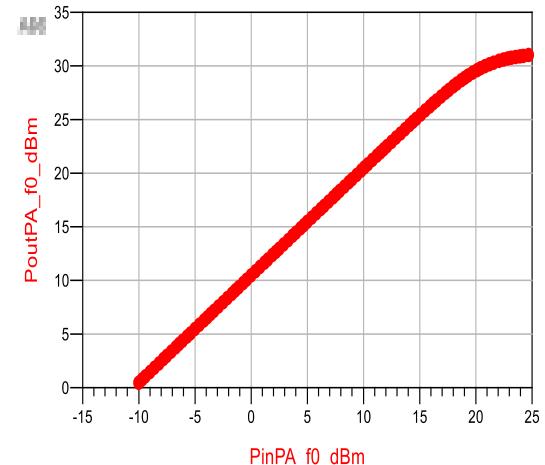
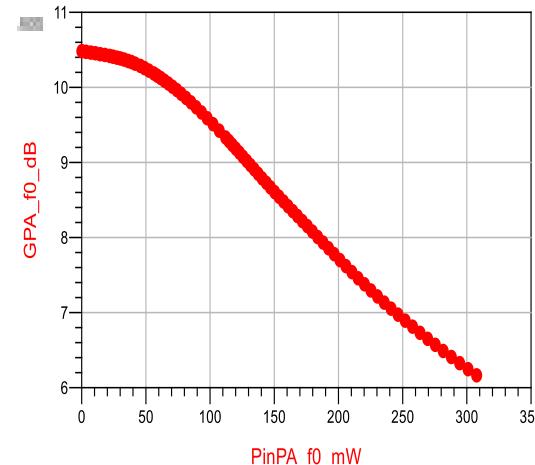
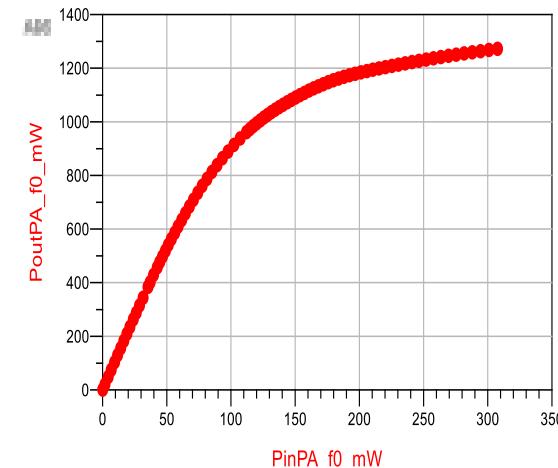
Eqn Ids_int_t=ts(Ids_int.i)



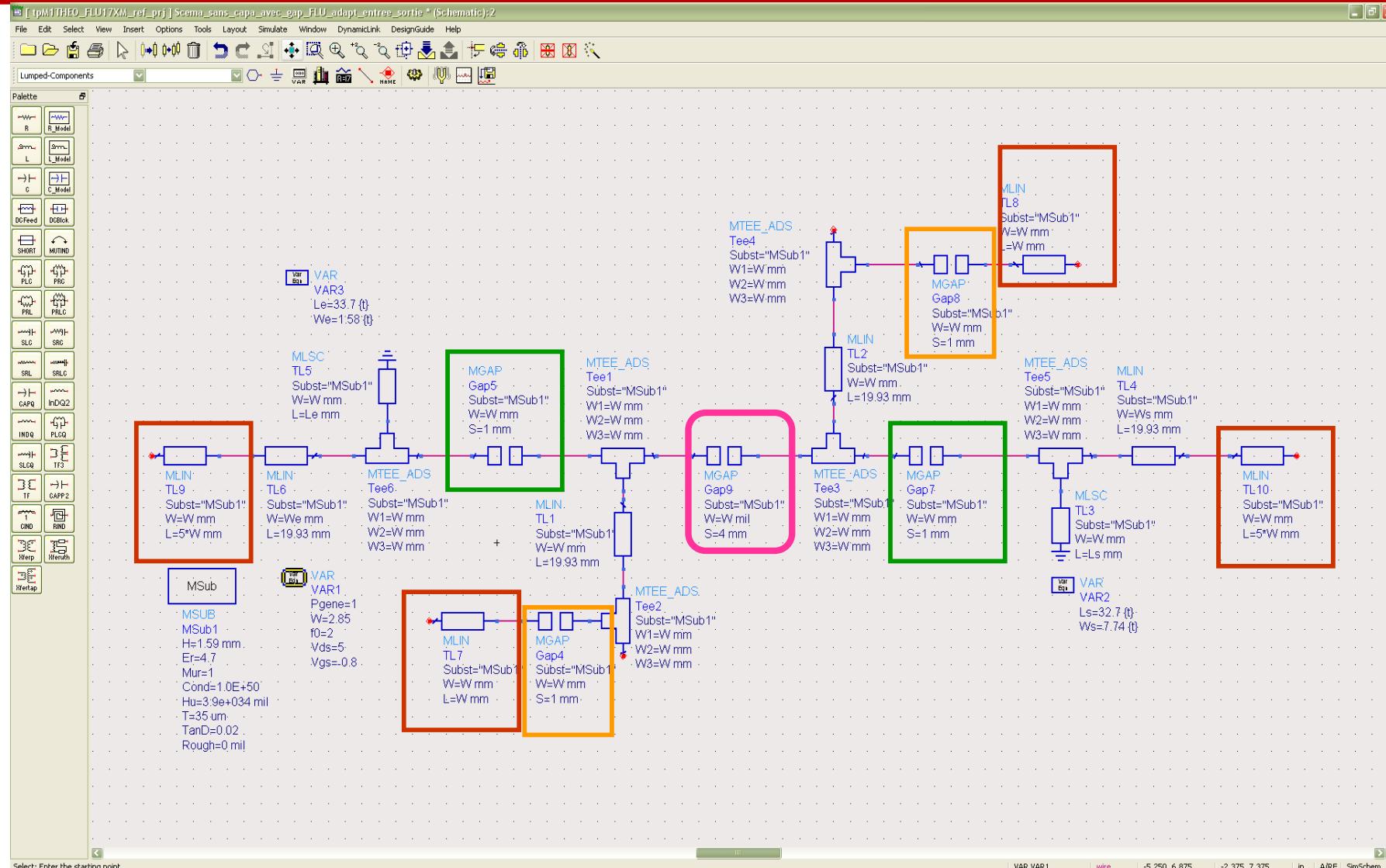
Pgene	ZinFET_f0	...ainFET_f0
-10.000	$10.409 + j8...$	$0.663 / 160...$
-9.900	$10.409 + j8...$	$0.663 / 160...$

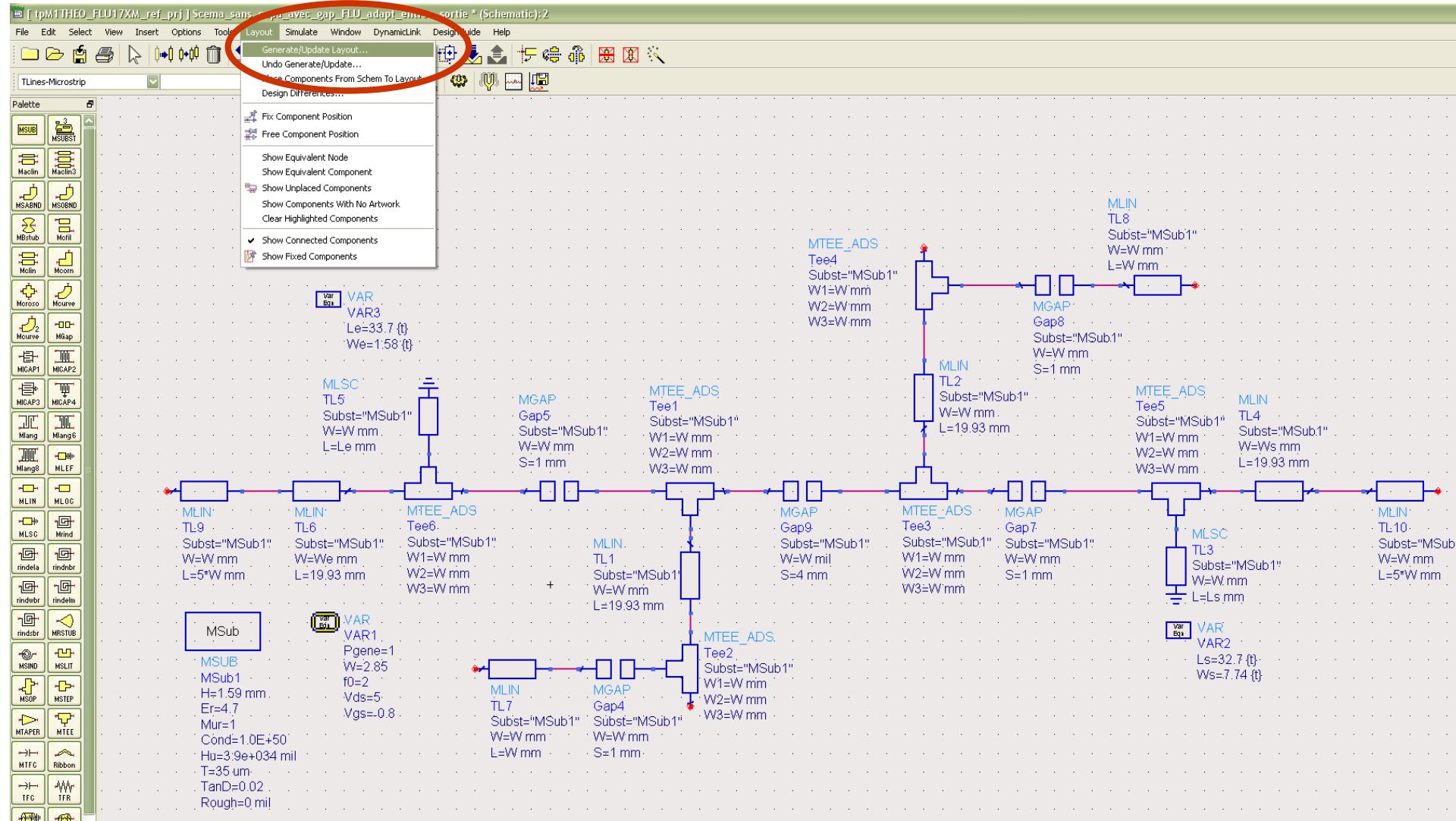
Pgene	ZinPA_f0	...mainPA_f0
-10.000	$57.370 + j0...$	$0.069 / 2.855$
-9.900	$57.370 + j0...$	$0.069 / 2.855$

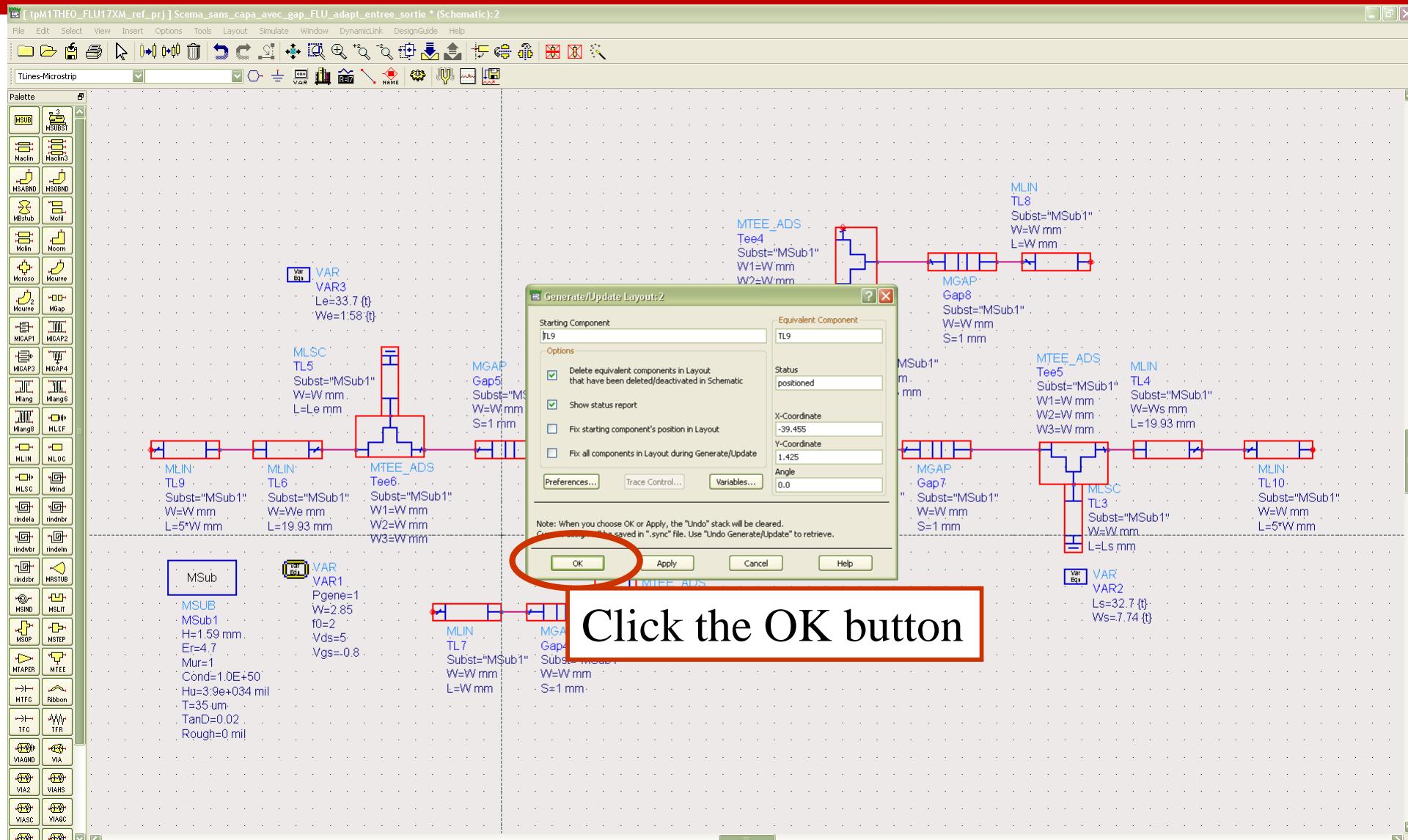
m1 Pgene=-1.879E-14 GamainFET_f0=0.663 / 160.907 impedance = $Z_0 * (0.208 + j0.161)$	m2 Pgene=1.879E-14 GamainPA_f0=0.068 / 2.946 impedance = $Z_0 * (1.147 + j0.008)$
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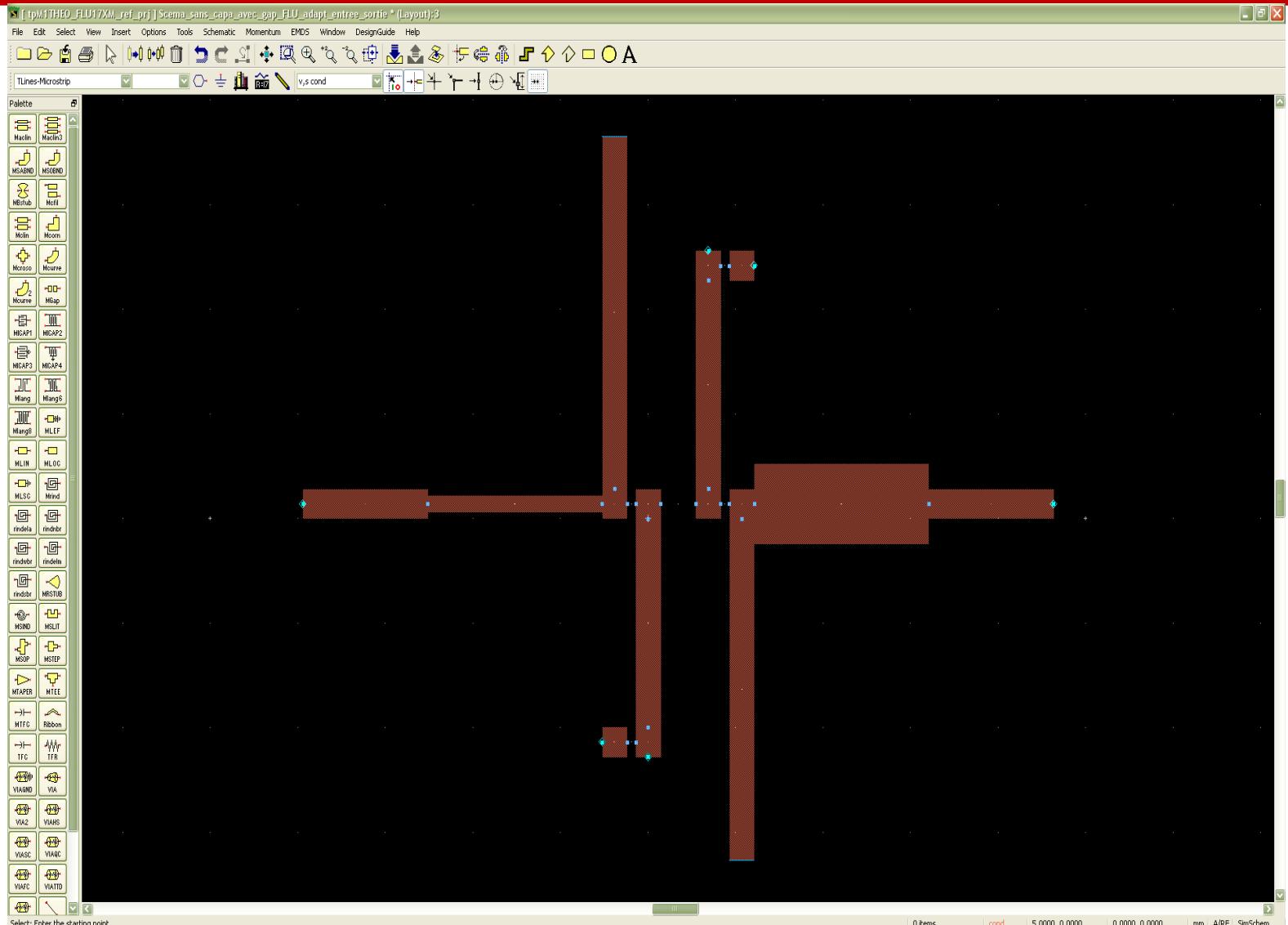


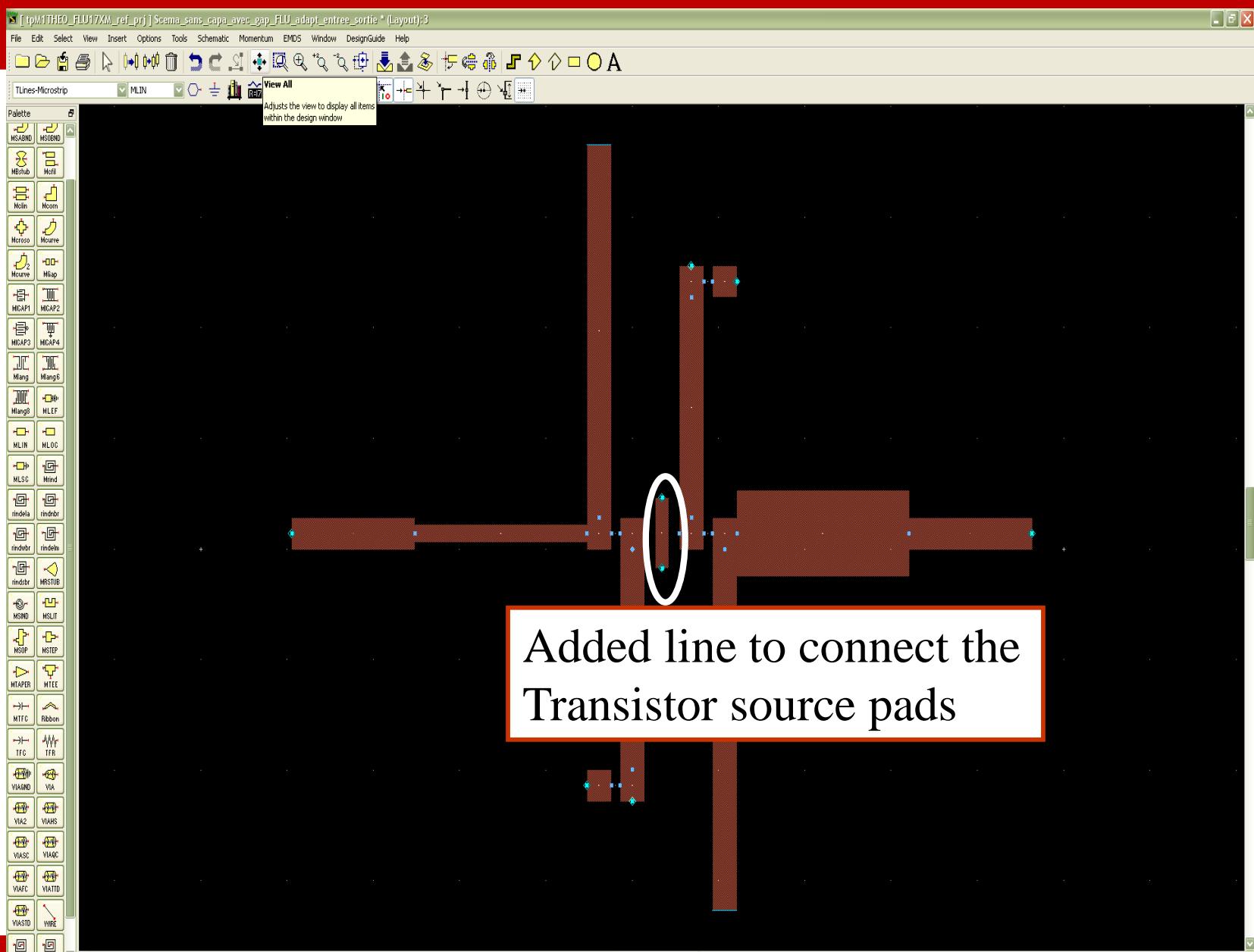
Layout of the PA Design with the packaged transistor and transmission Lines

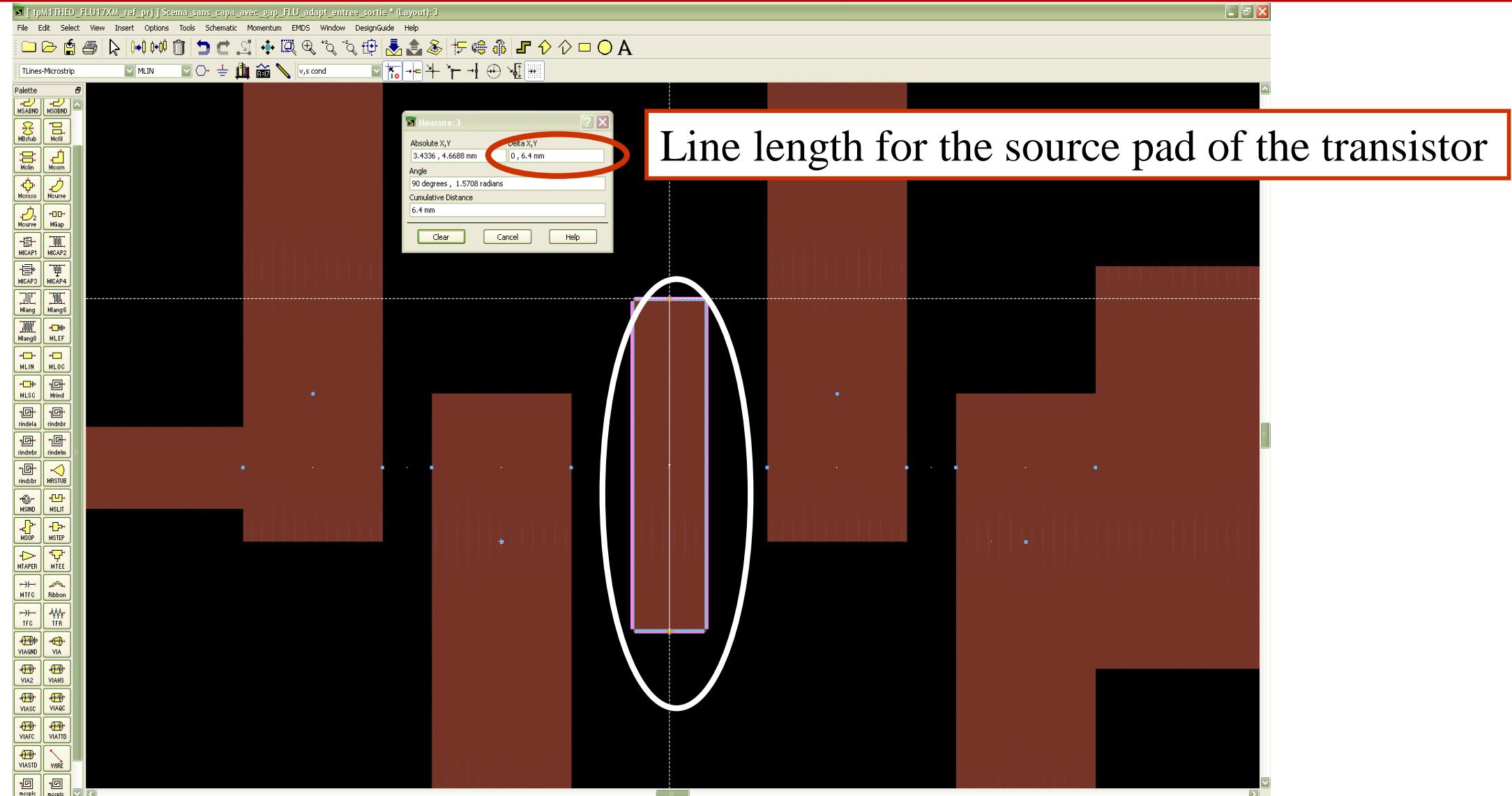


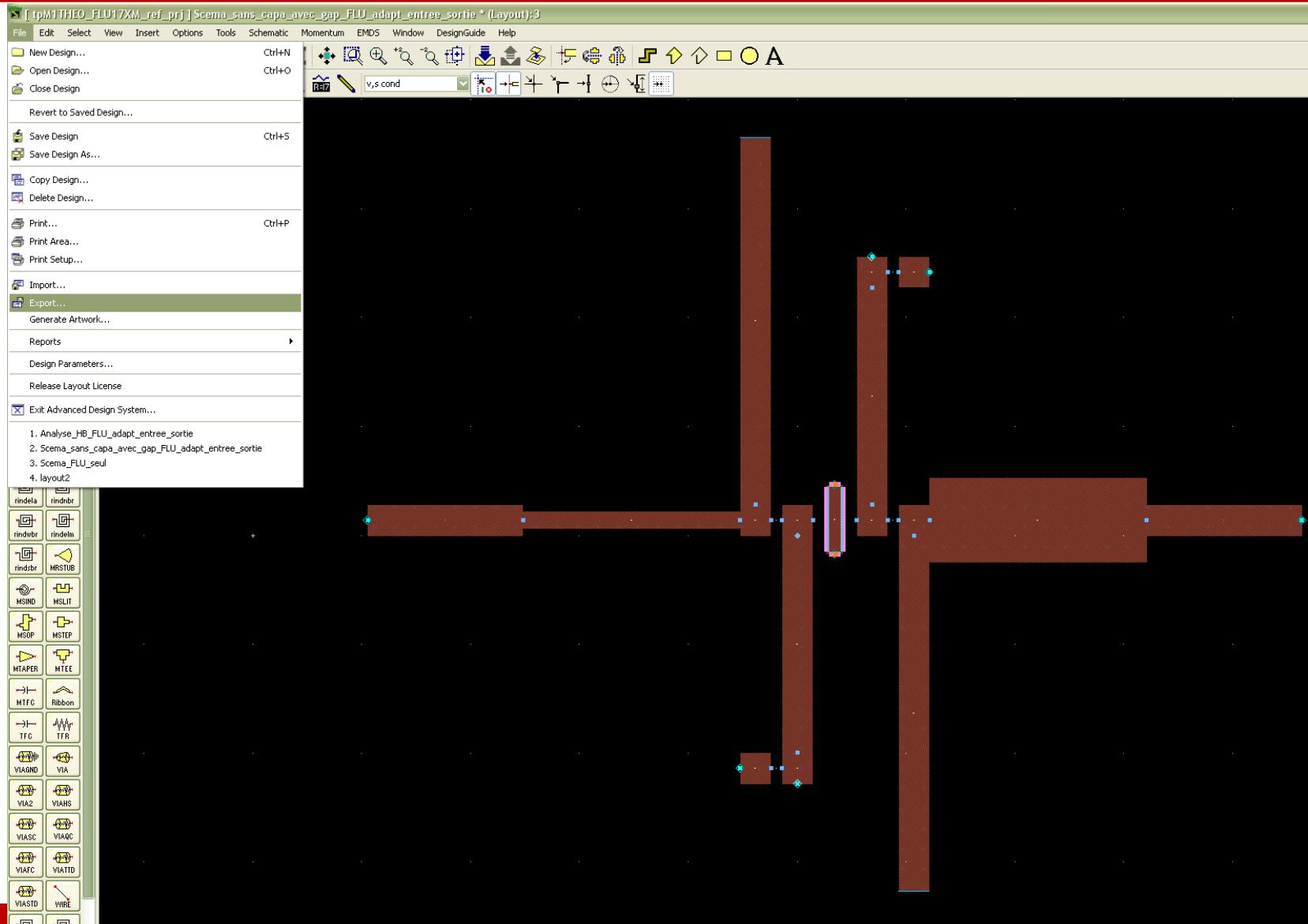


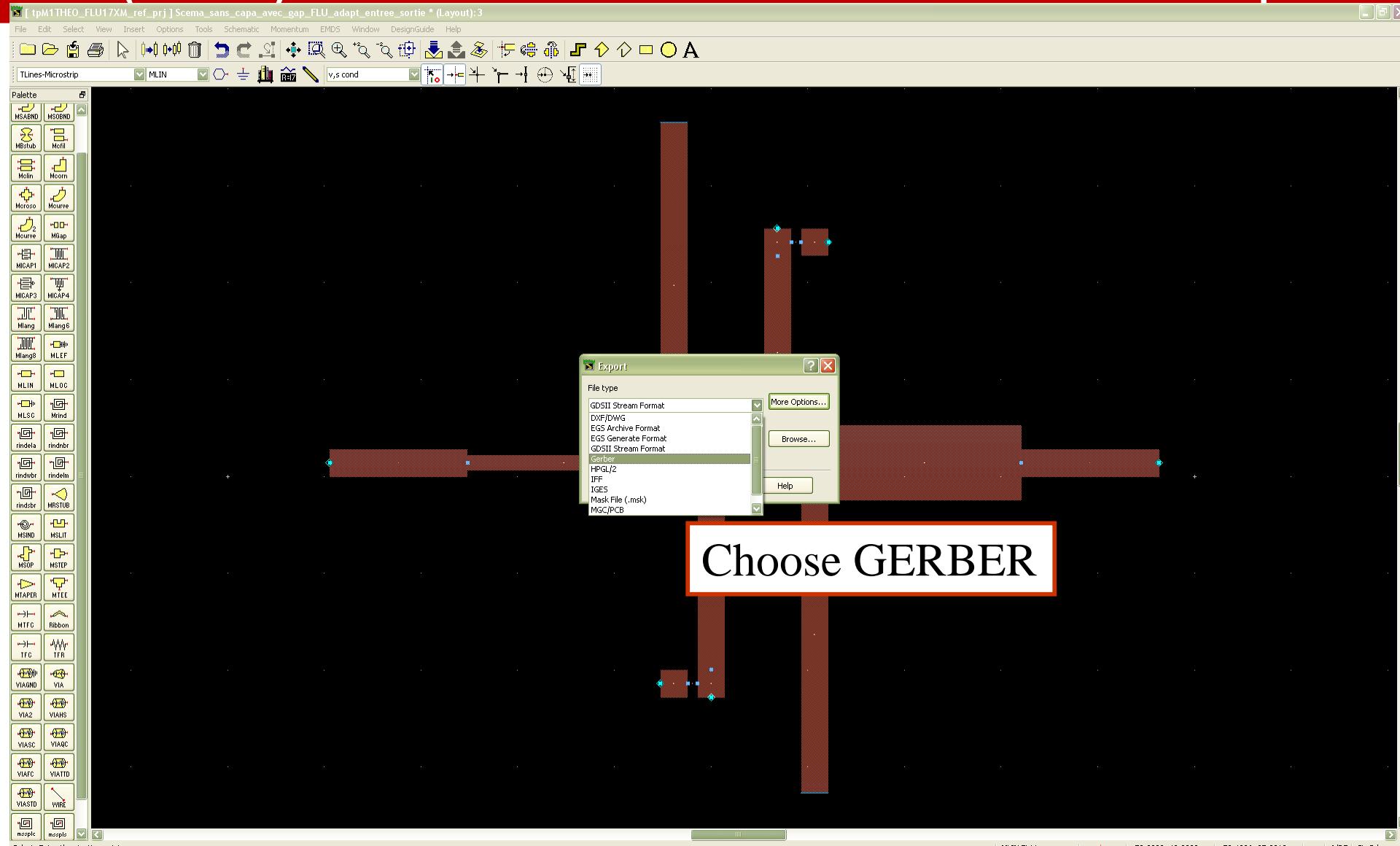


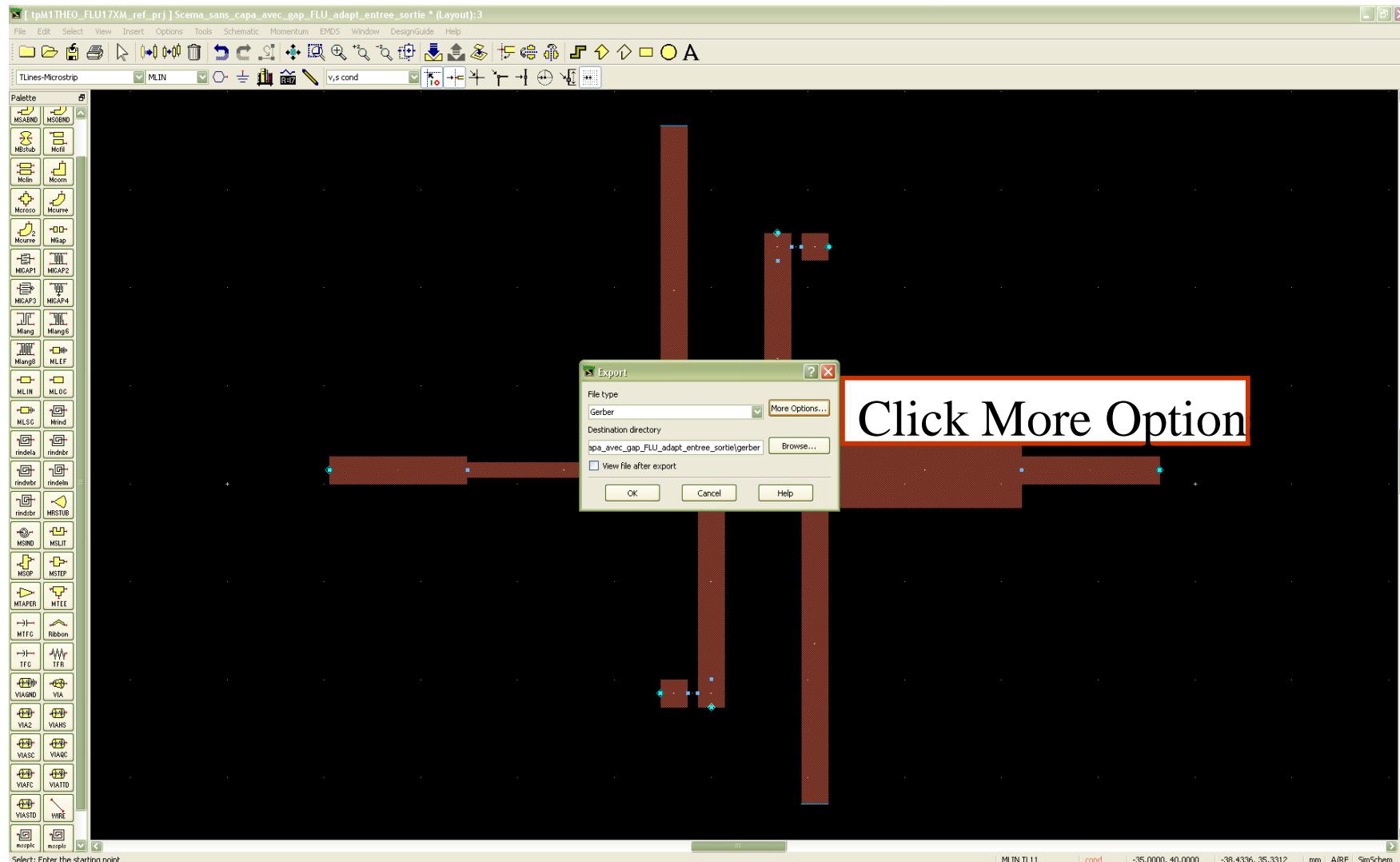


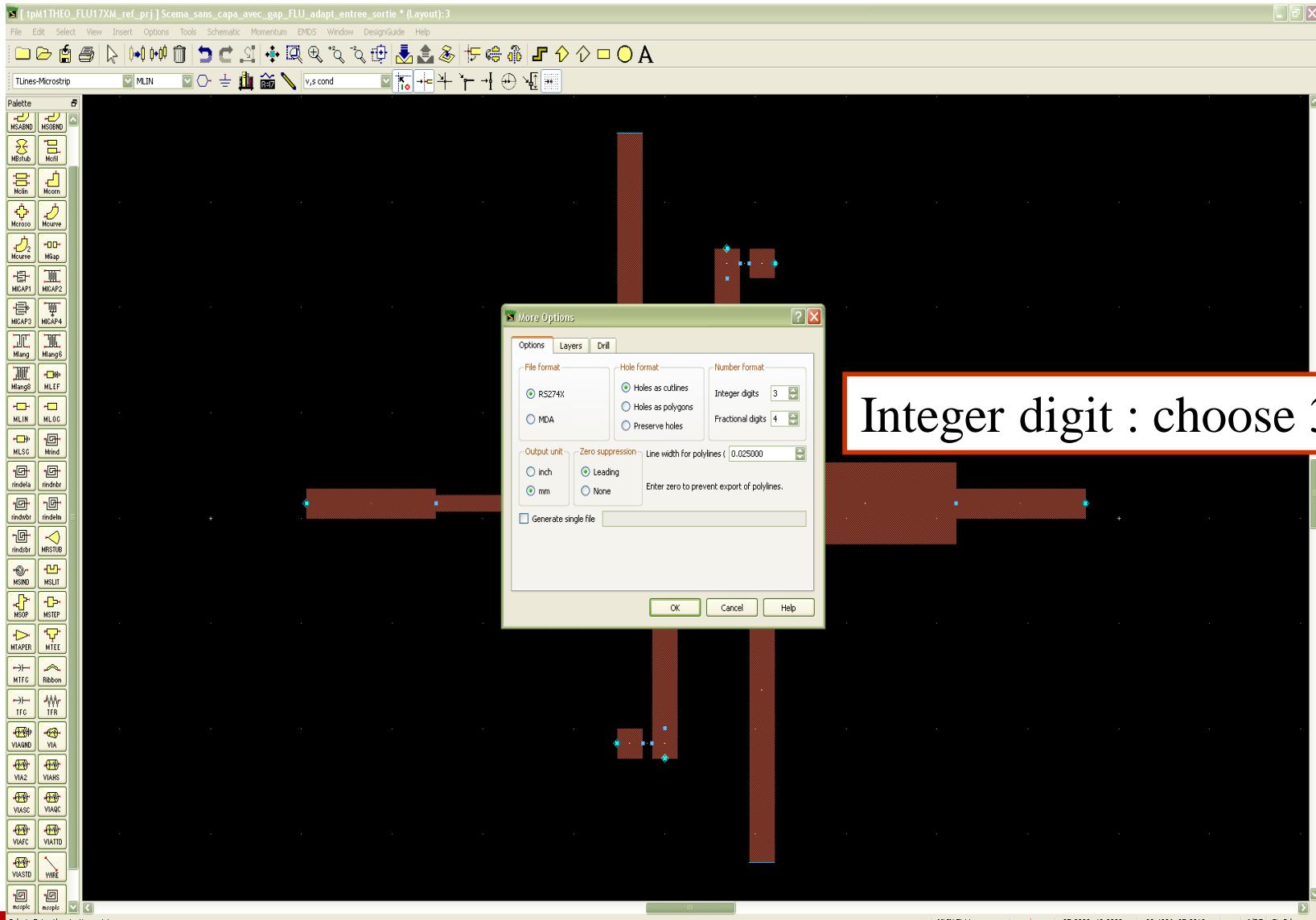




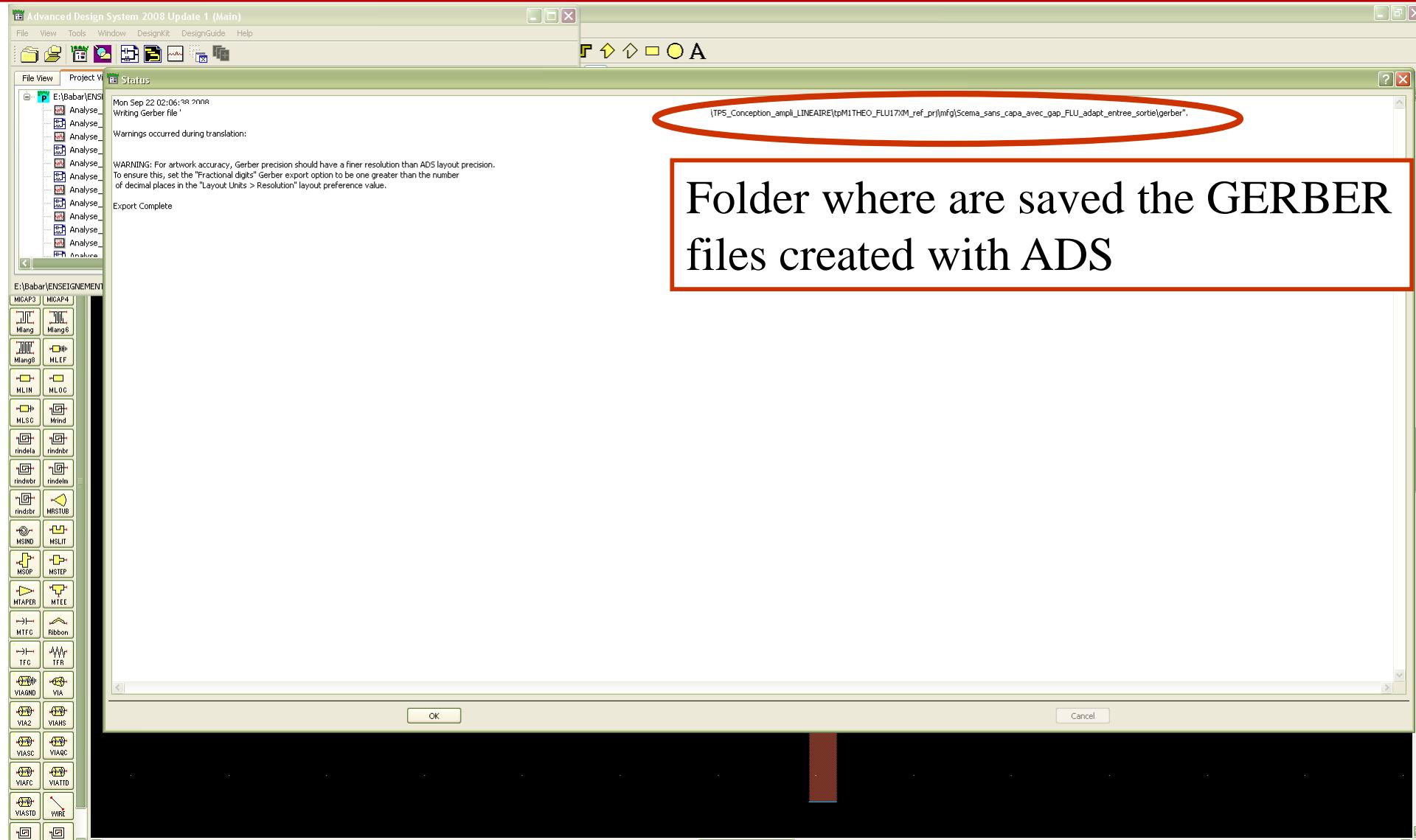


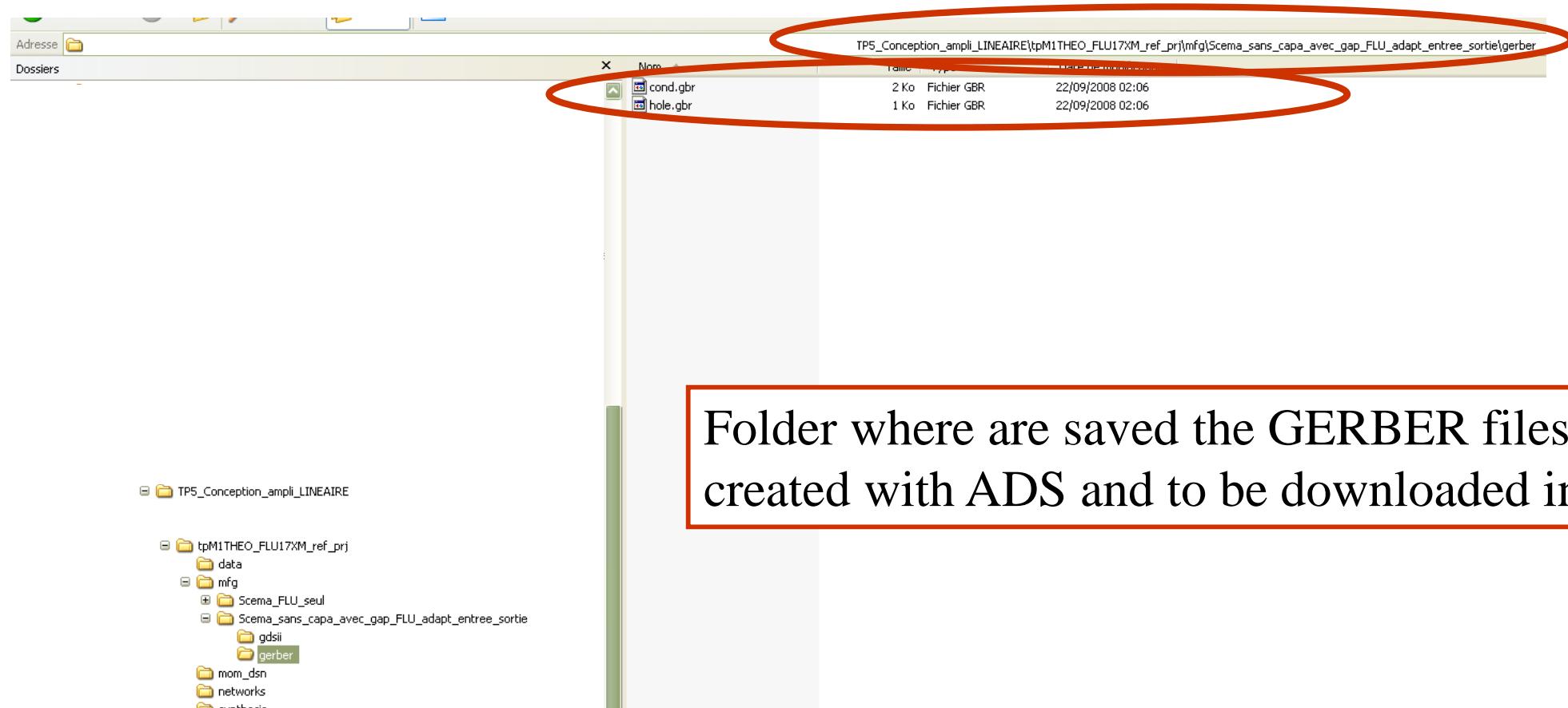




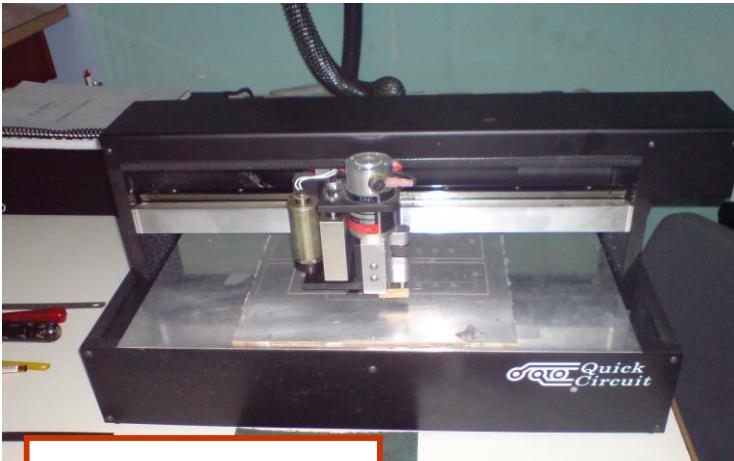


Integer digit : choose 3

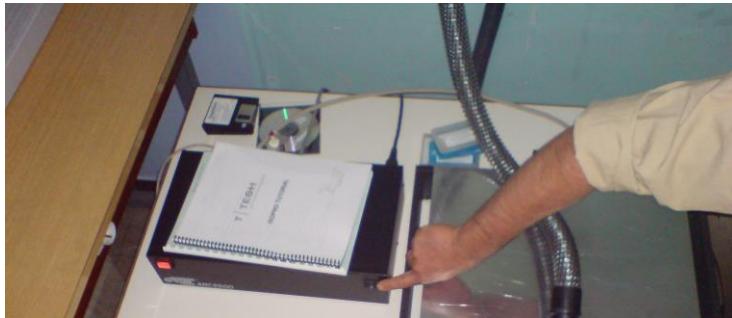




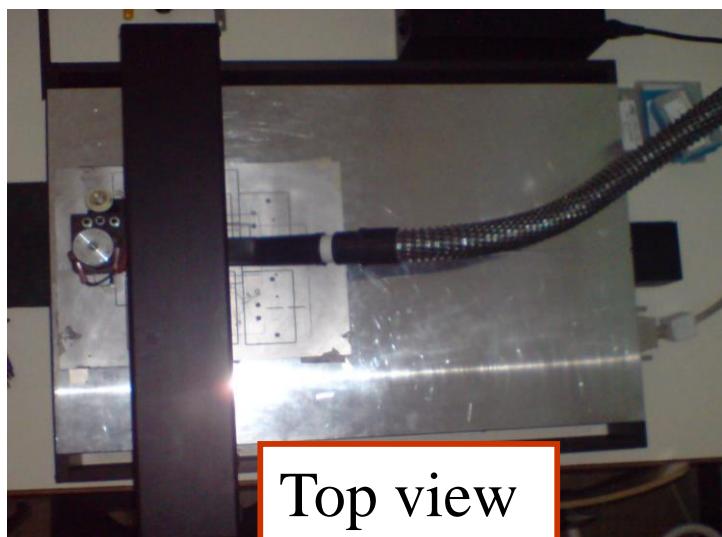
Folder where are saved the GERBER files created with ADS and to be downloaded in ISOPRO



Front view



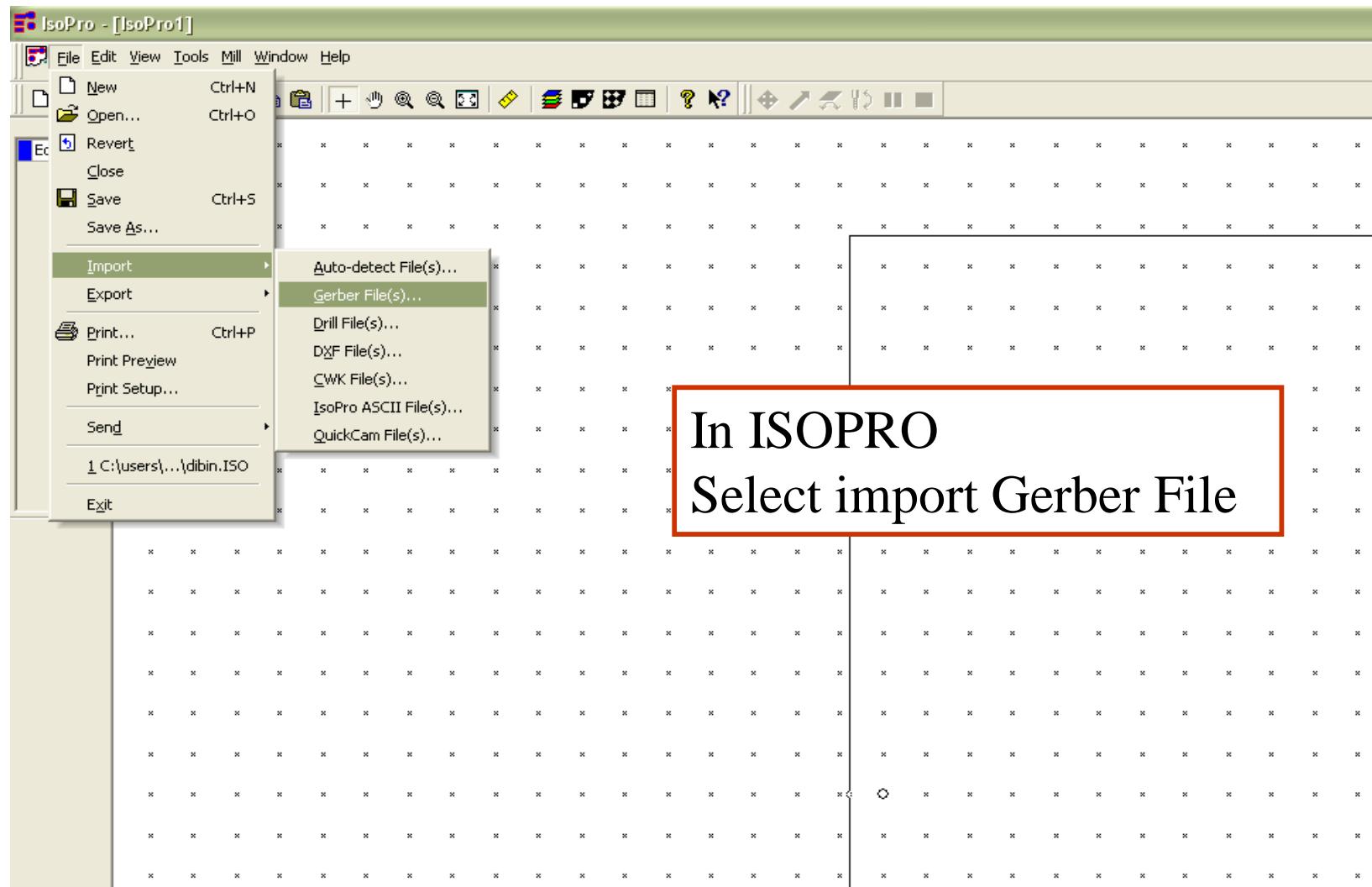
1°) Switch « ON »
The general power supply

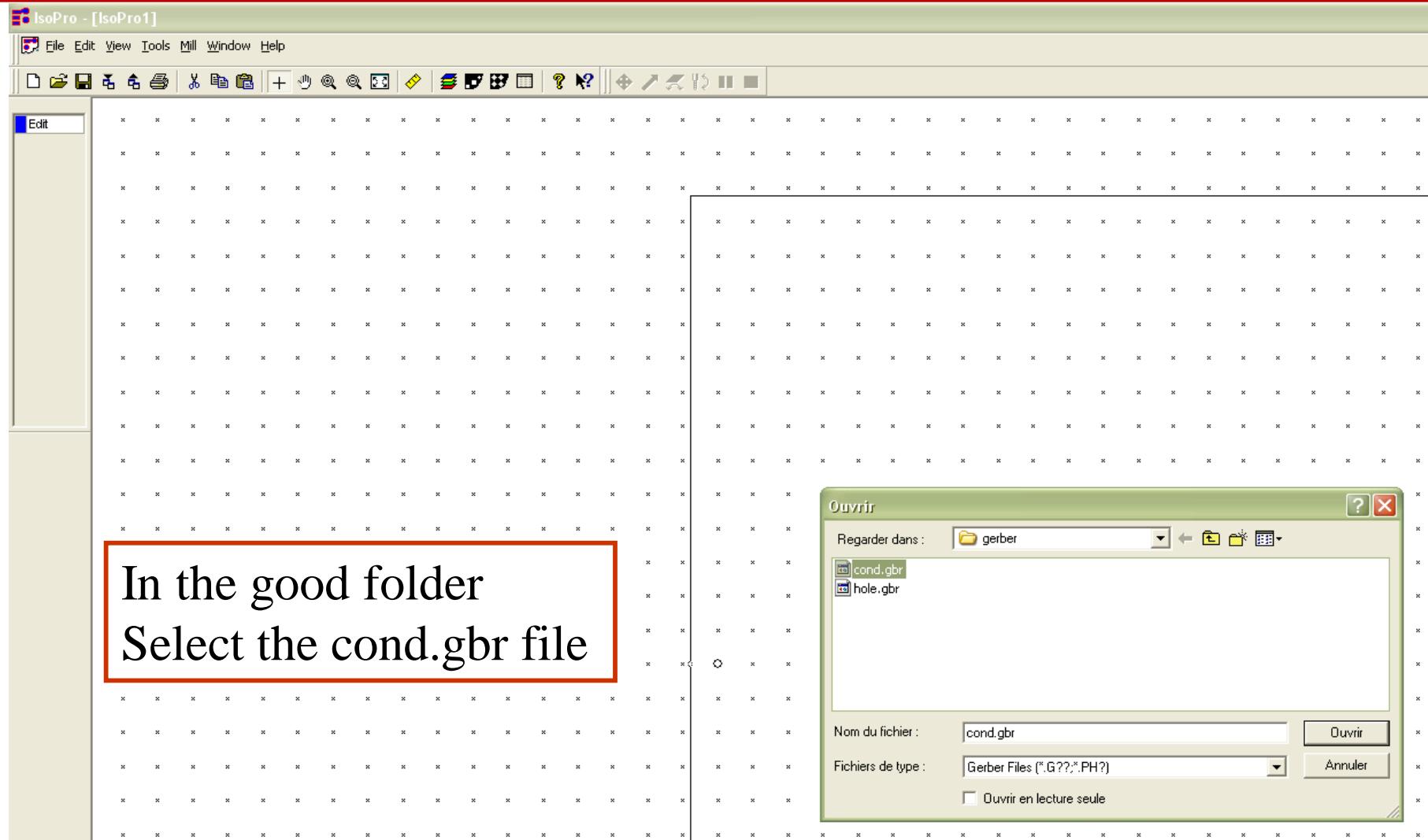


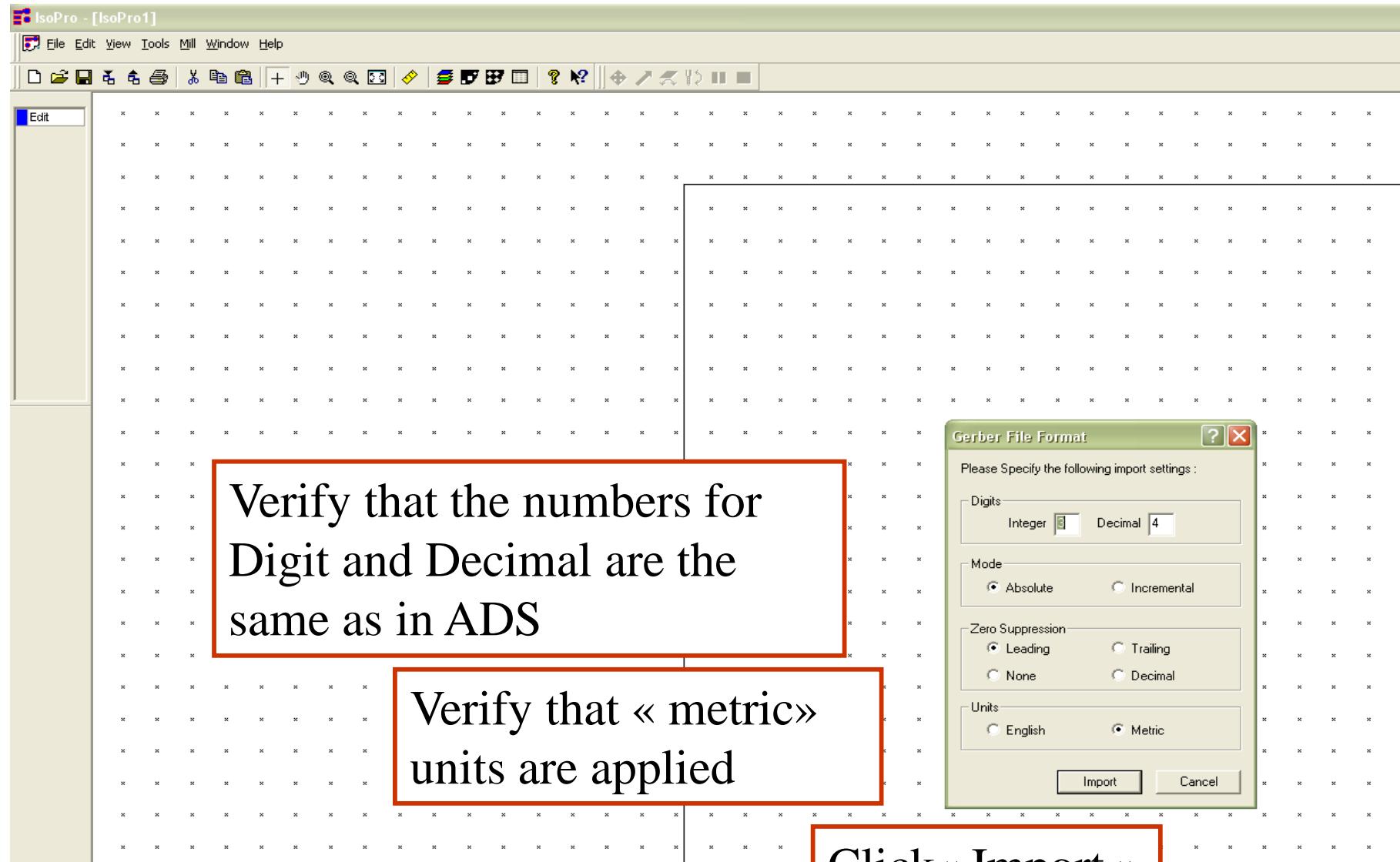
Top view

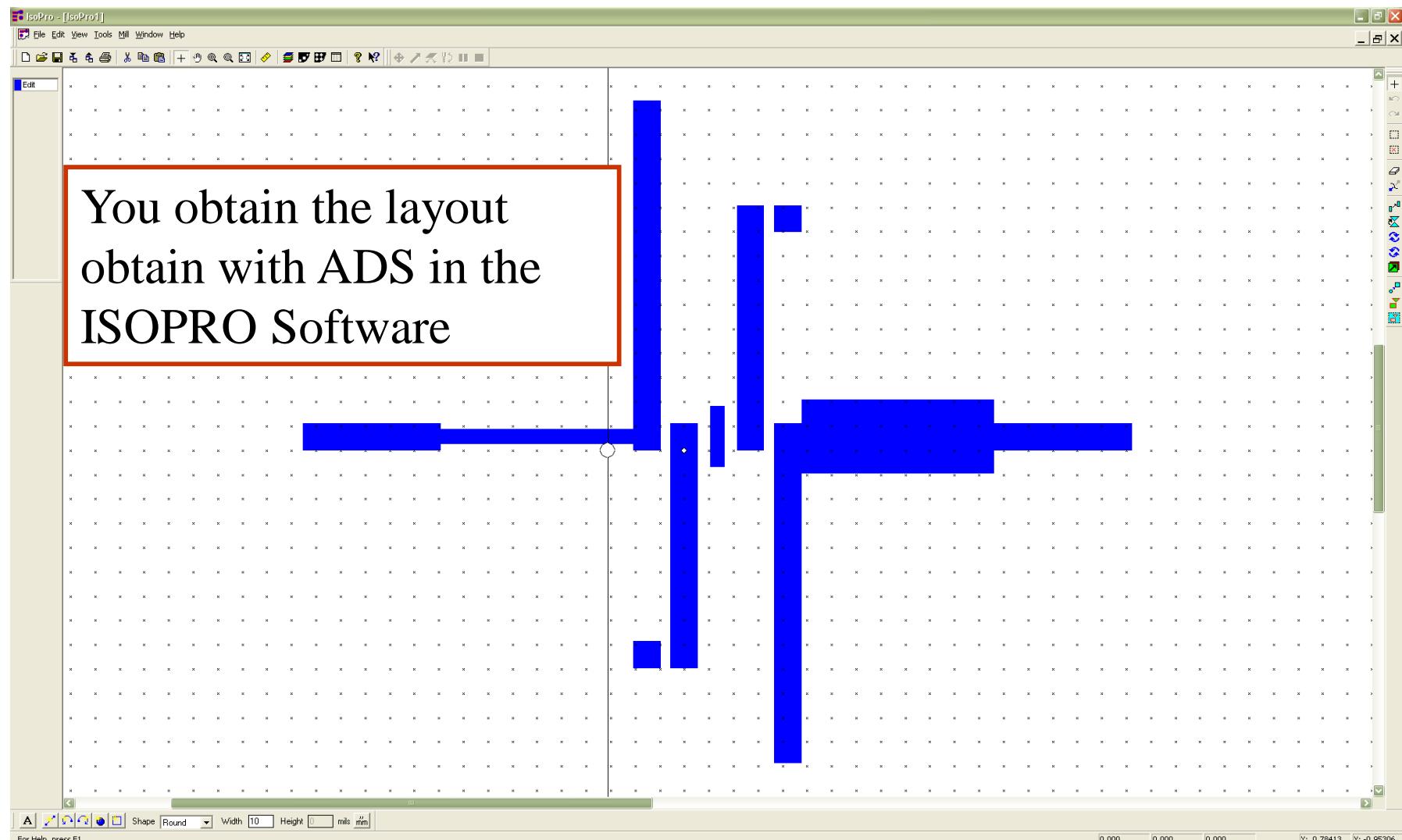


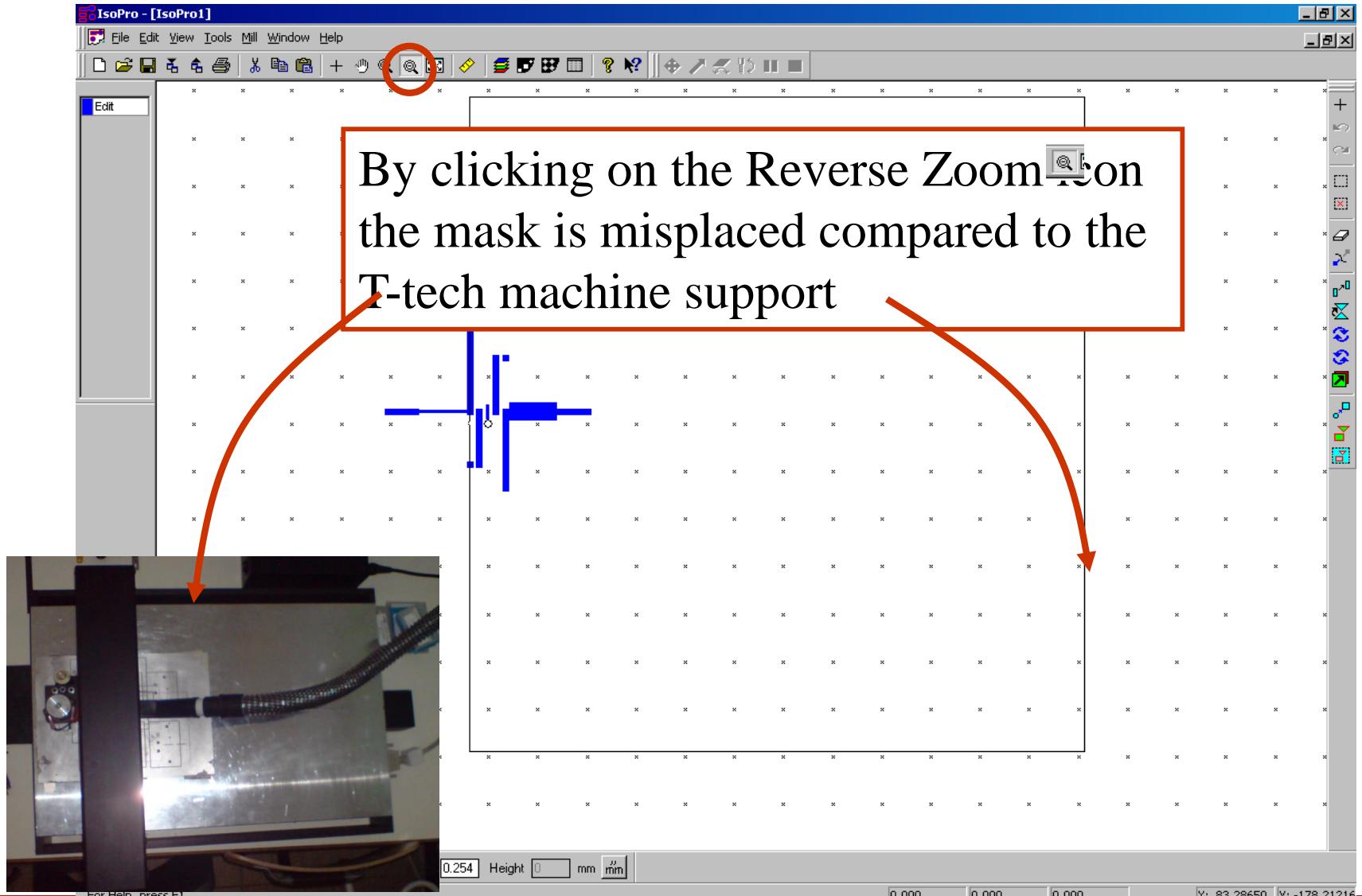
2°) Press "ON"
Solenoid rear face

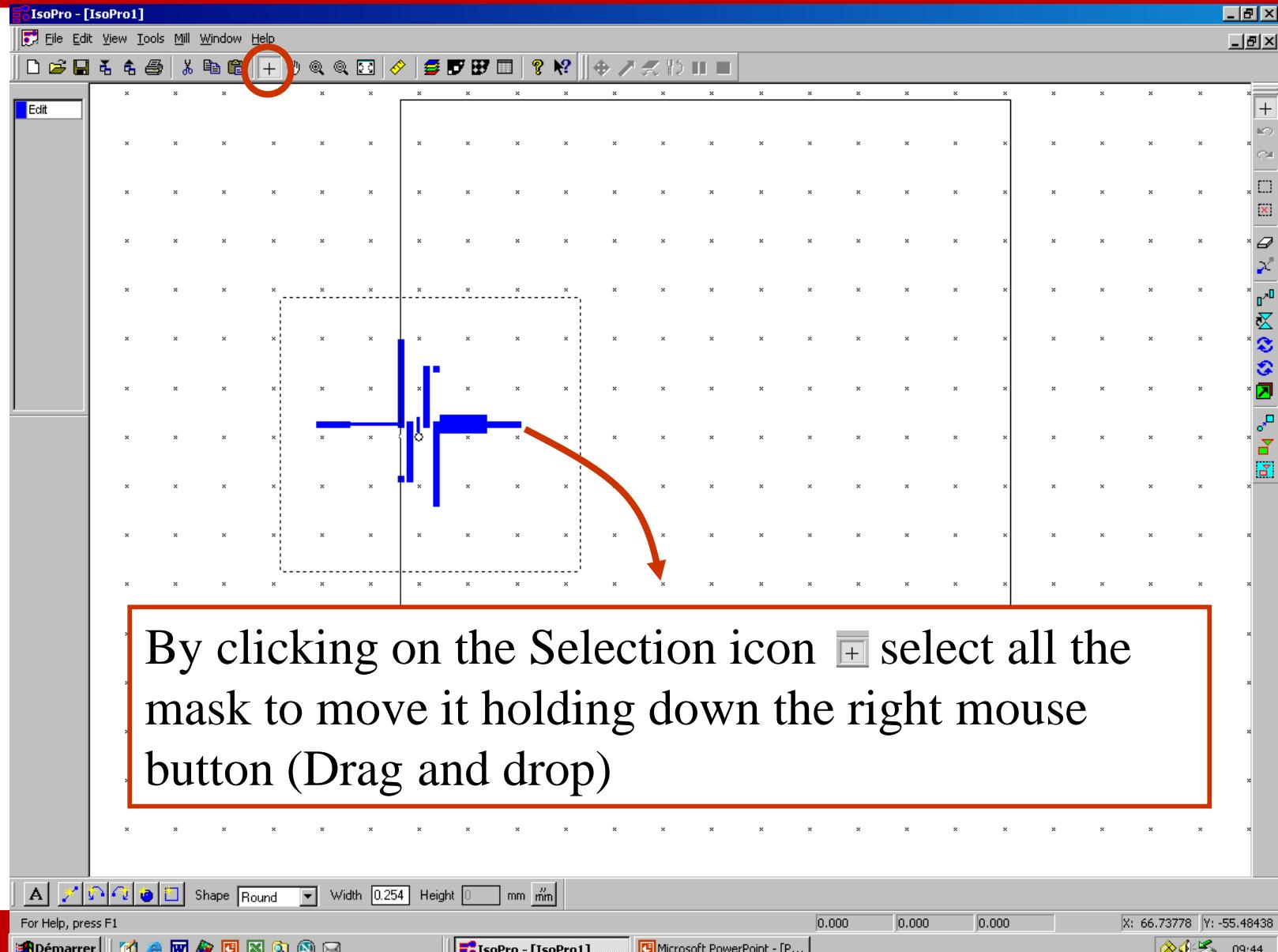


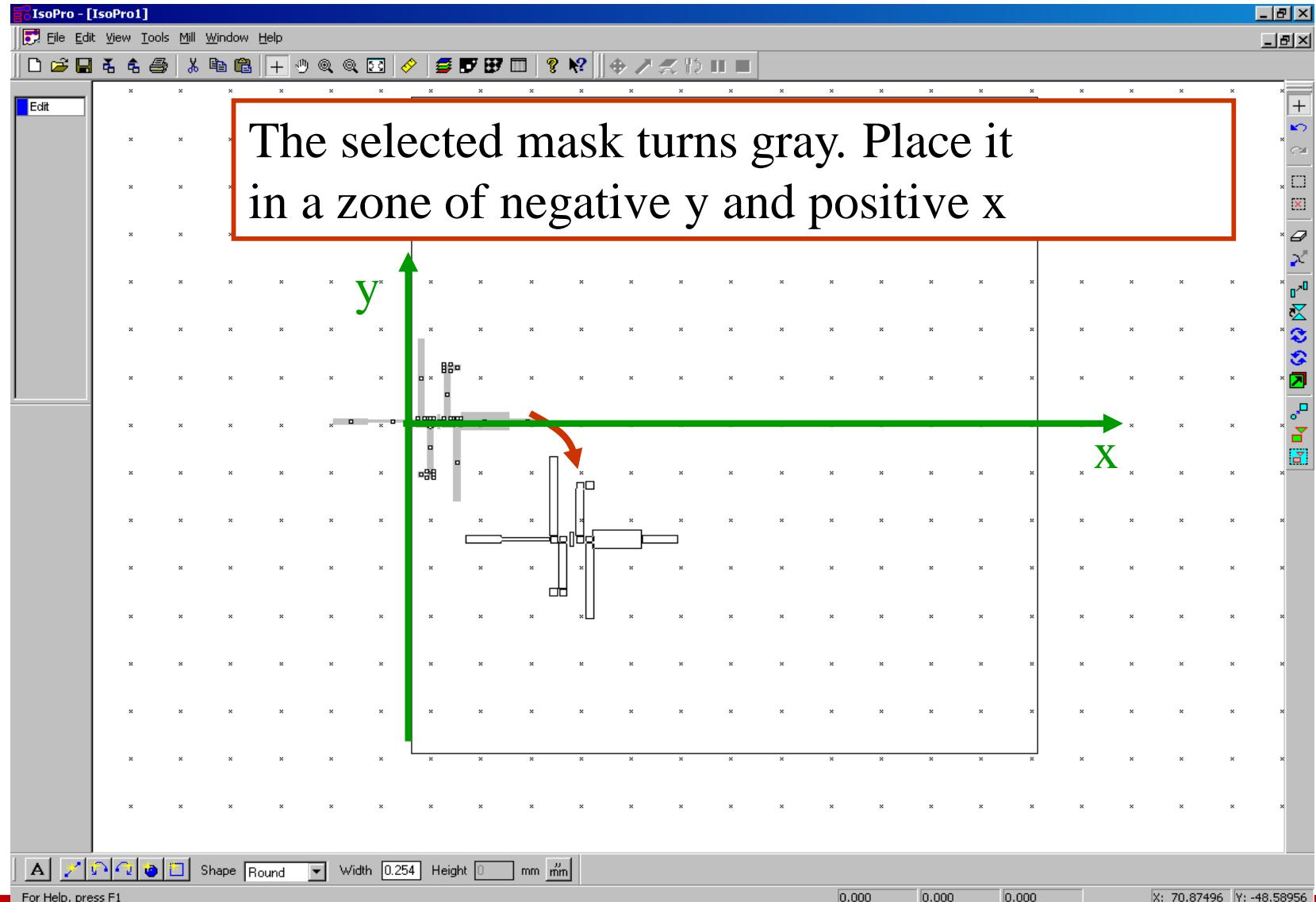


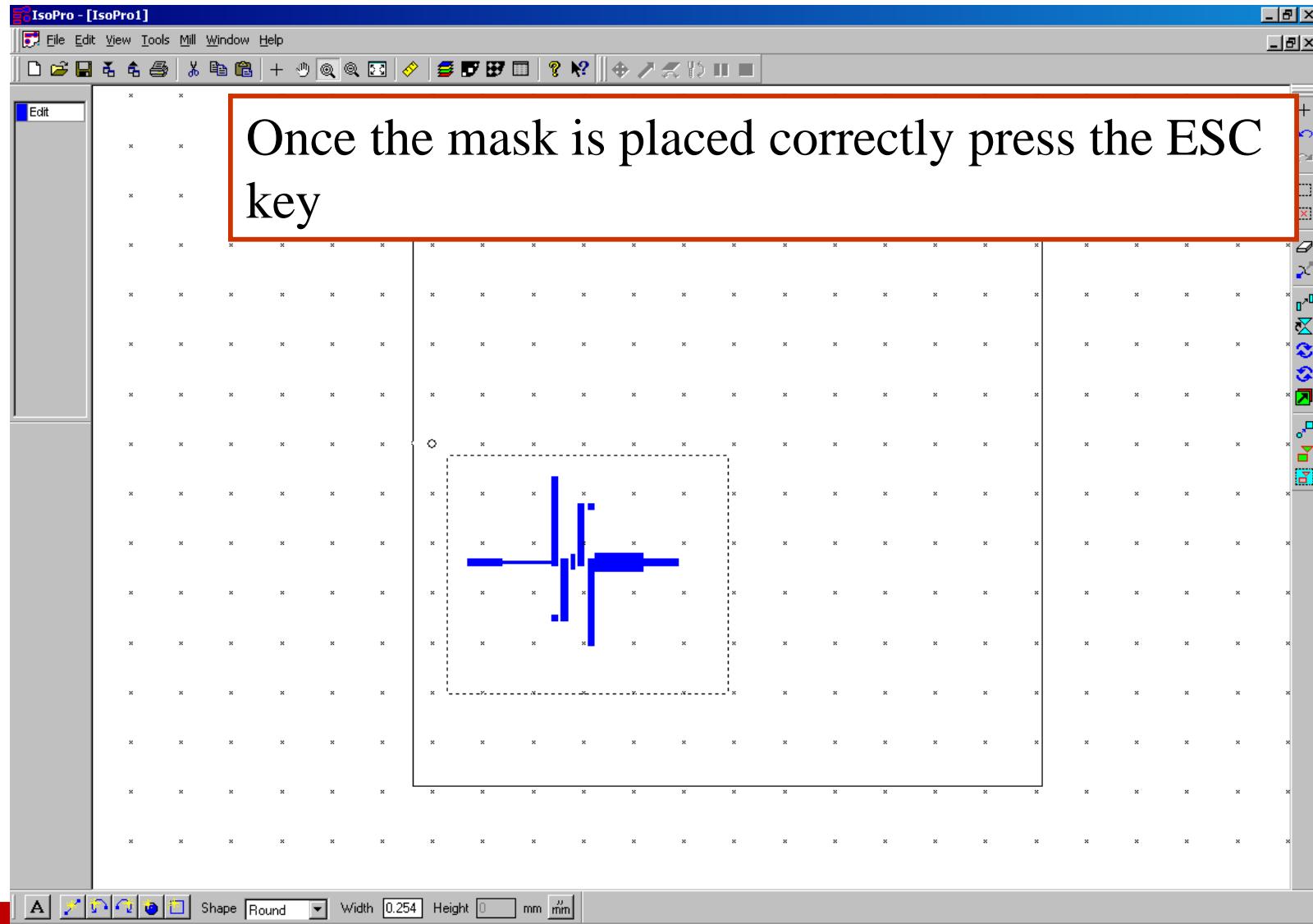


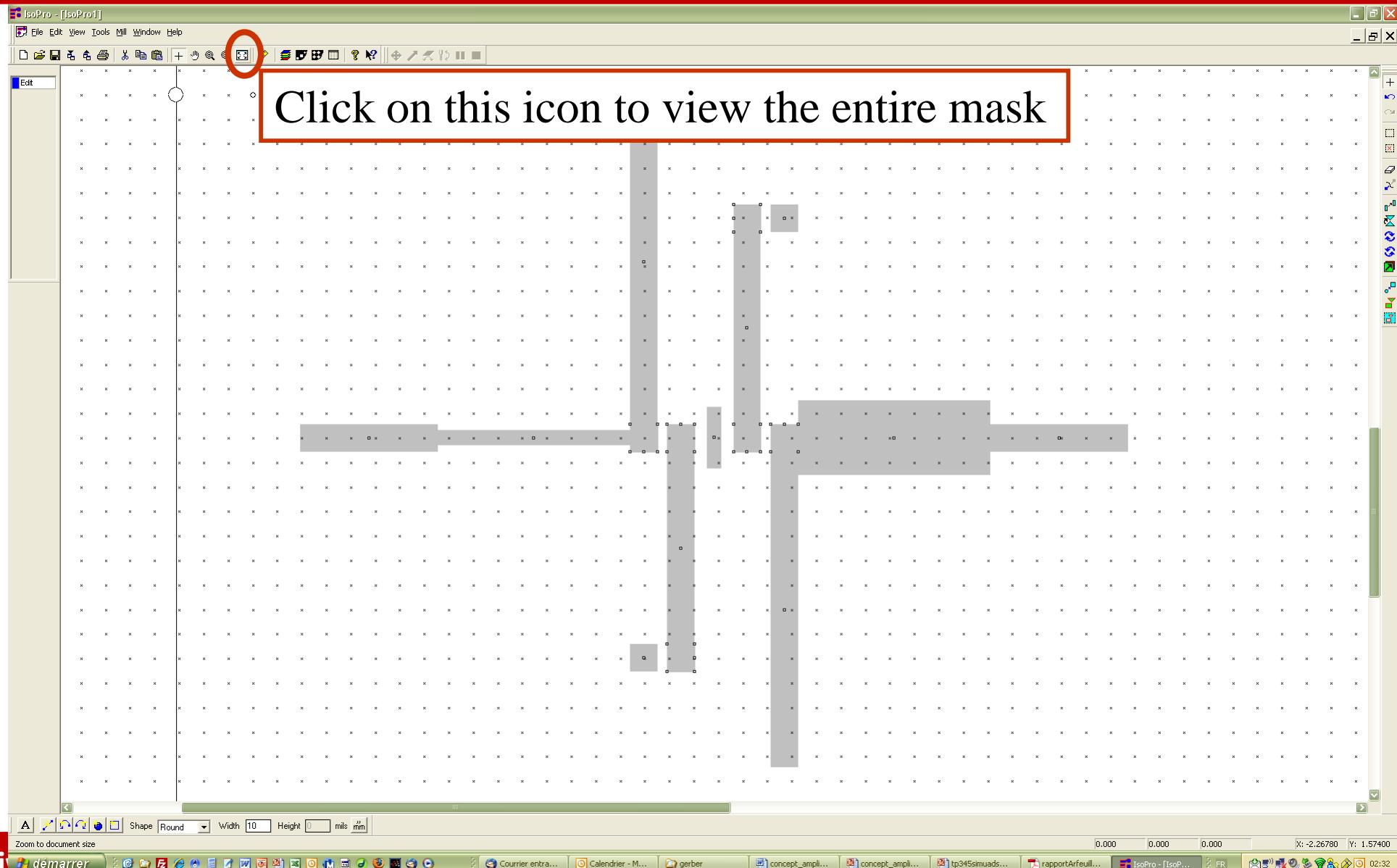


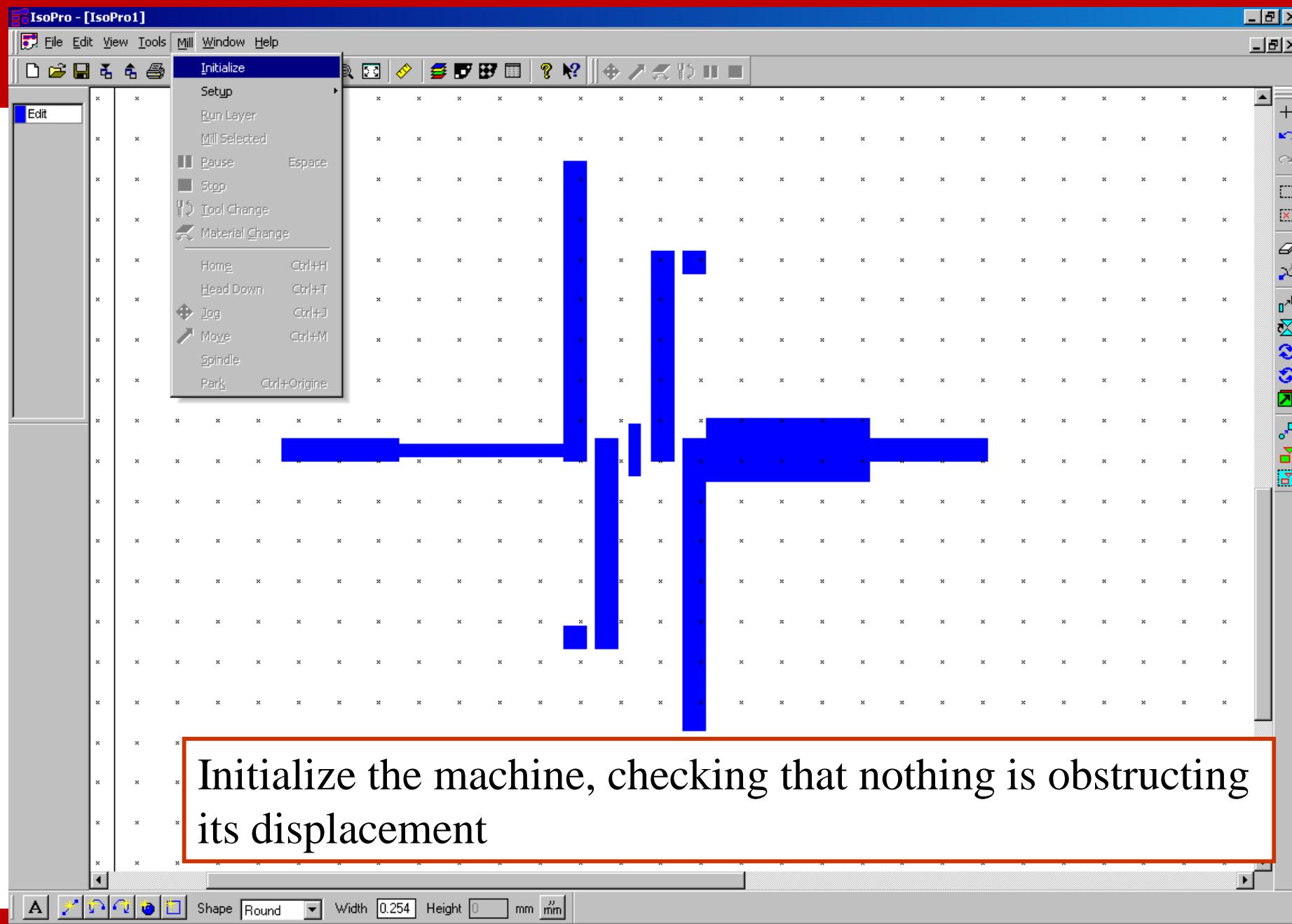


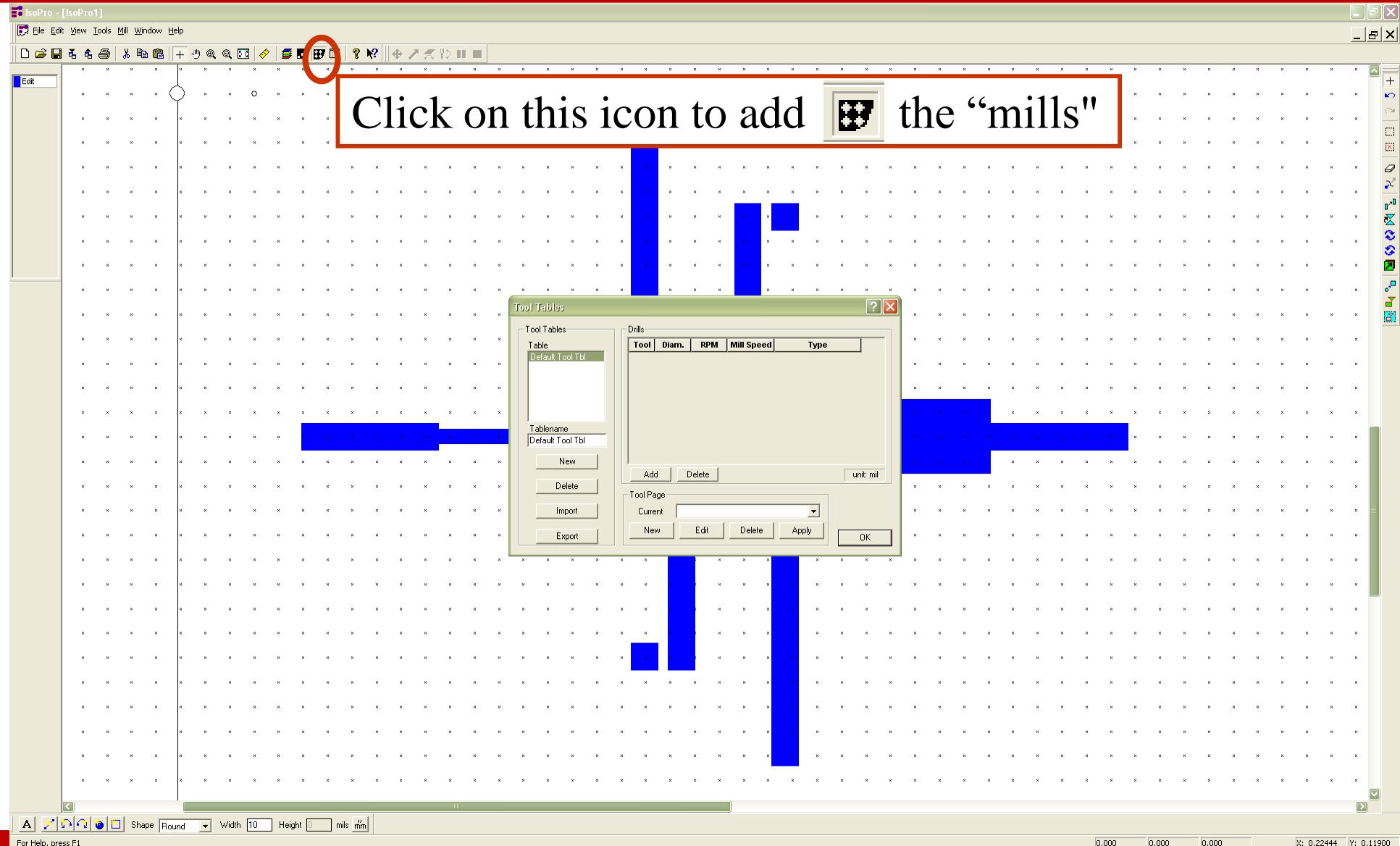
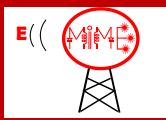


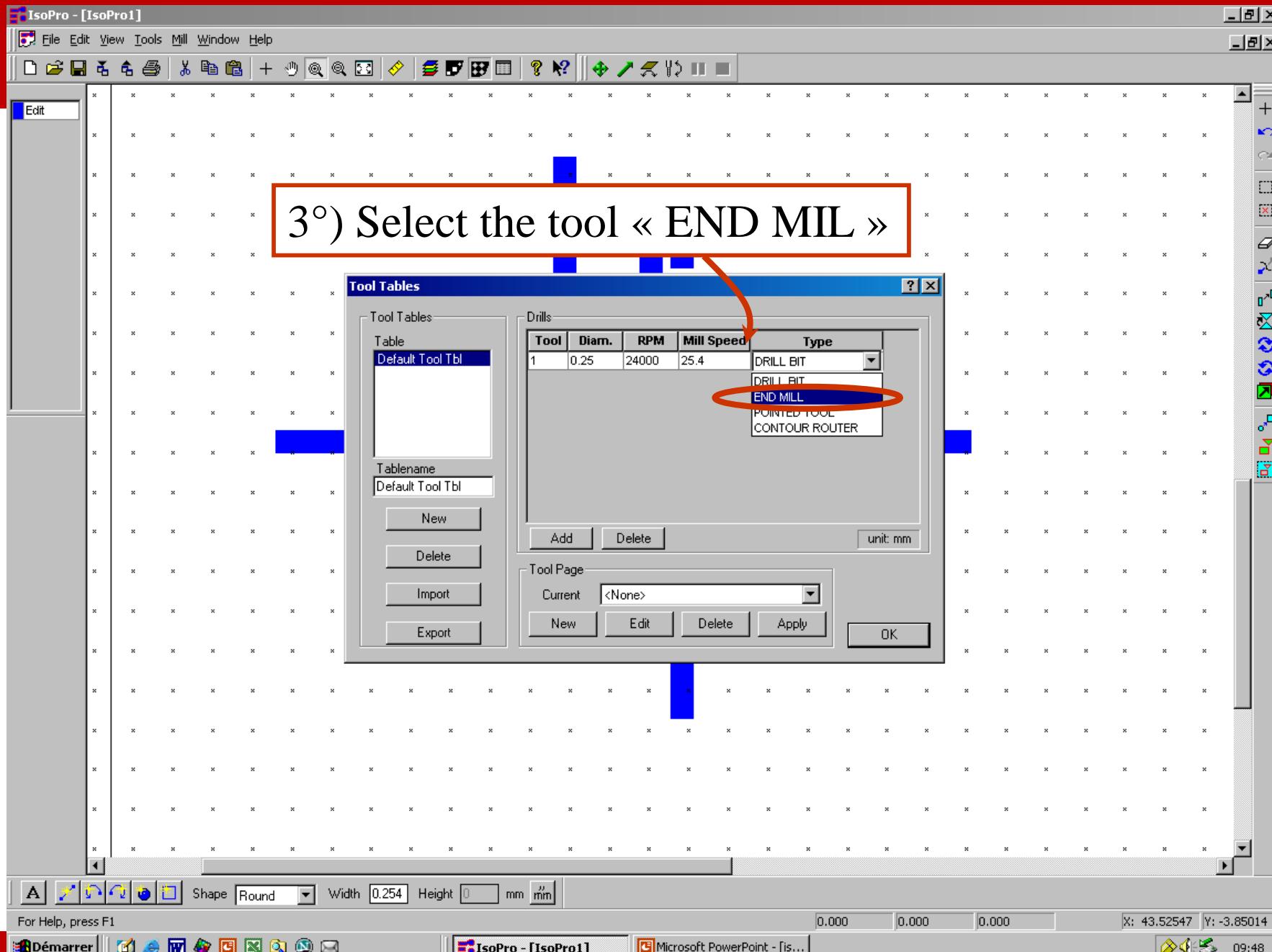


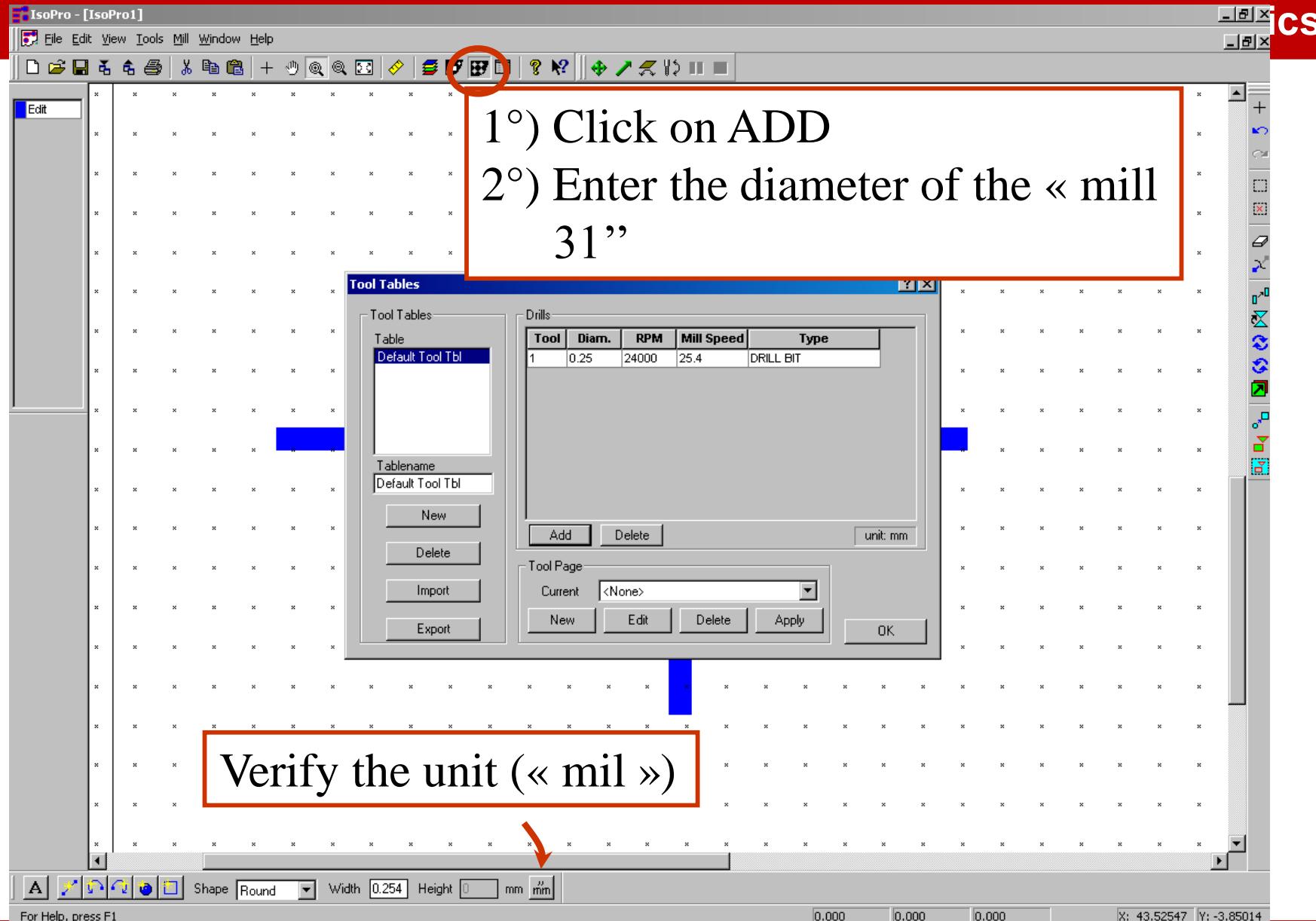


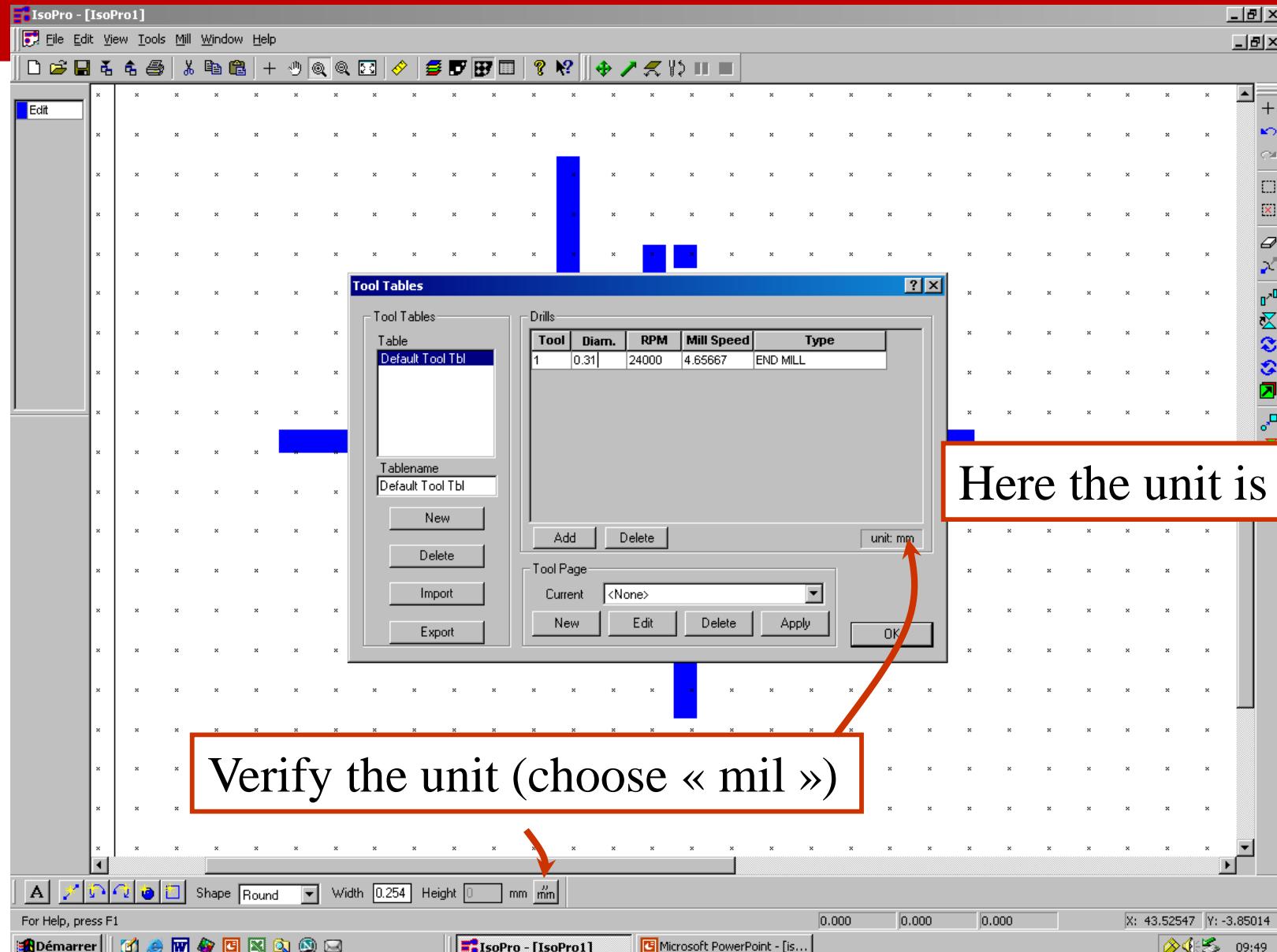


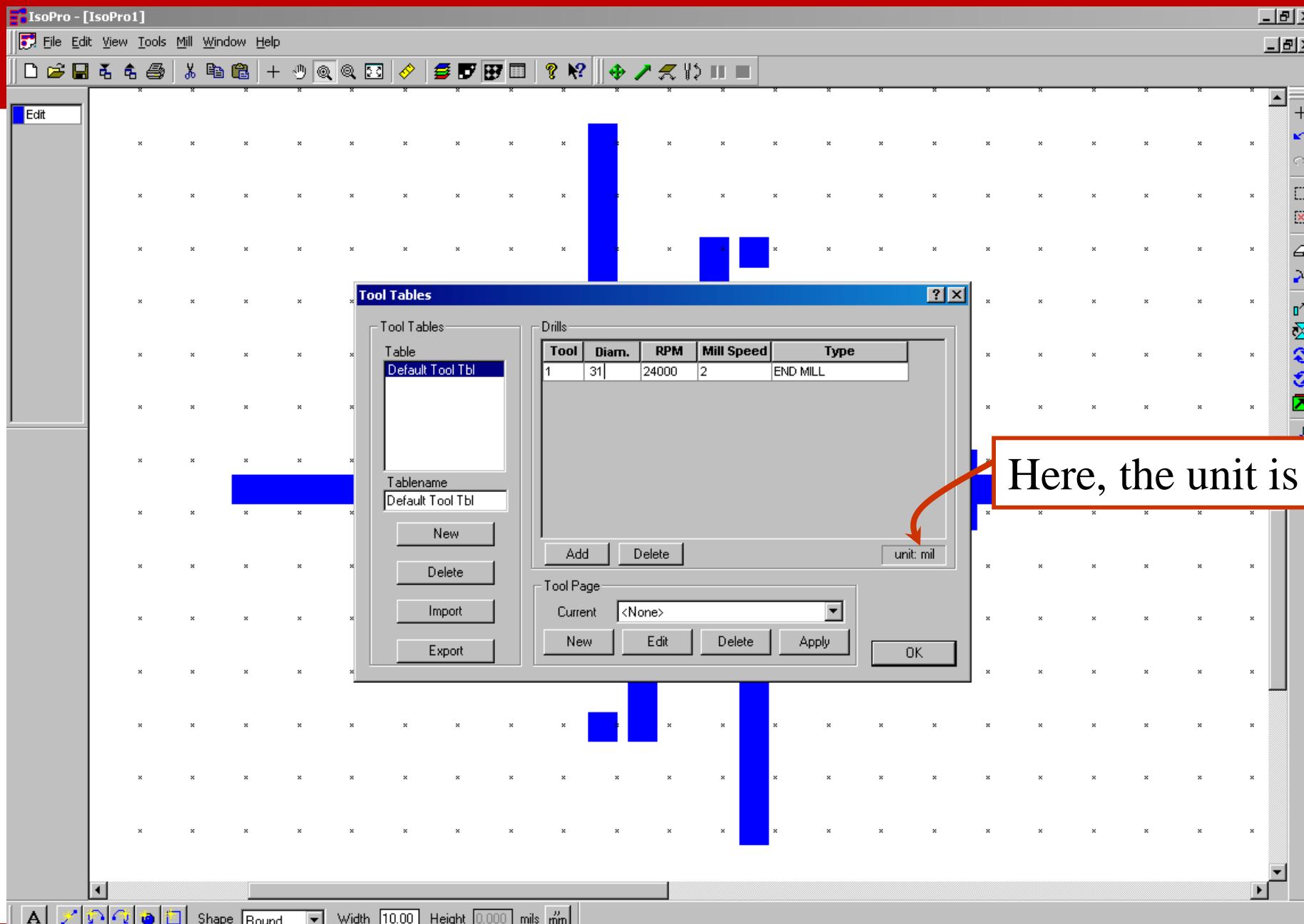




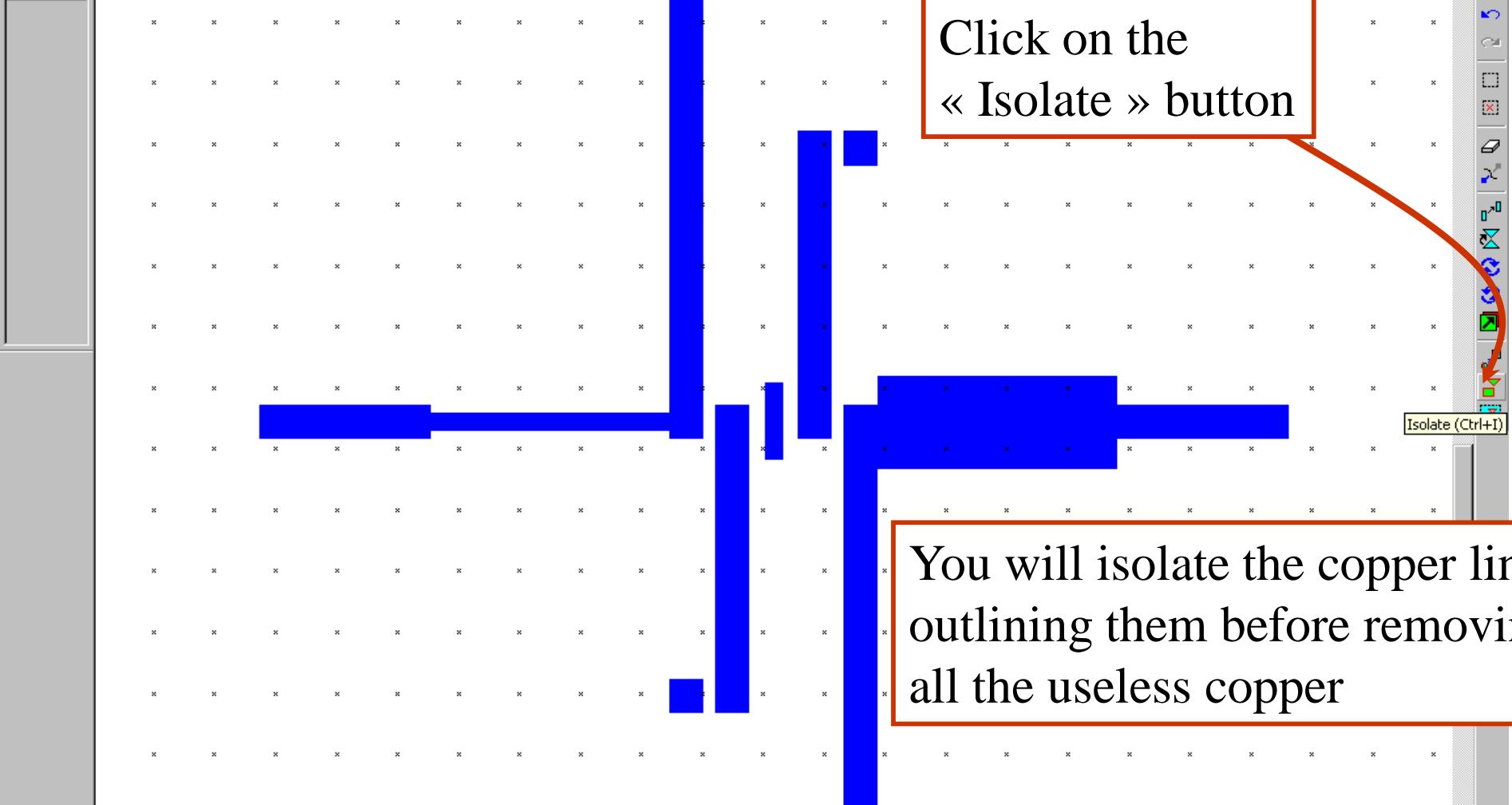








Edit



You will isolate the copper lines by outlining them before removing all the useless copper

A

Y

N

D

C

S

R

L

F

E

T

P

M

H

V

W

G

B

J

K

L

O

P

Q

R

S

T

U

V

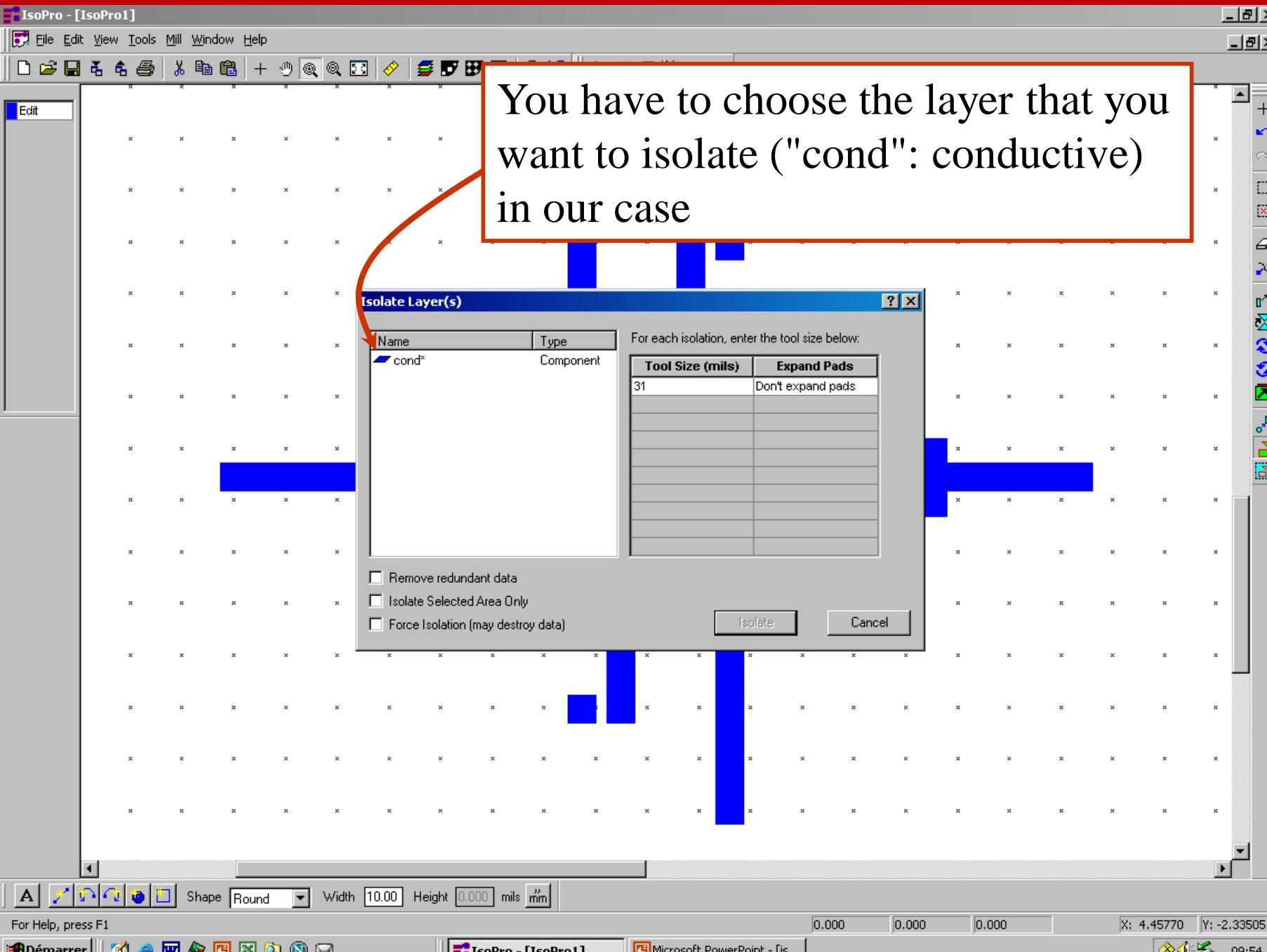
W

X

Y

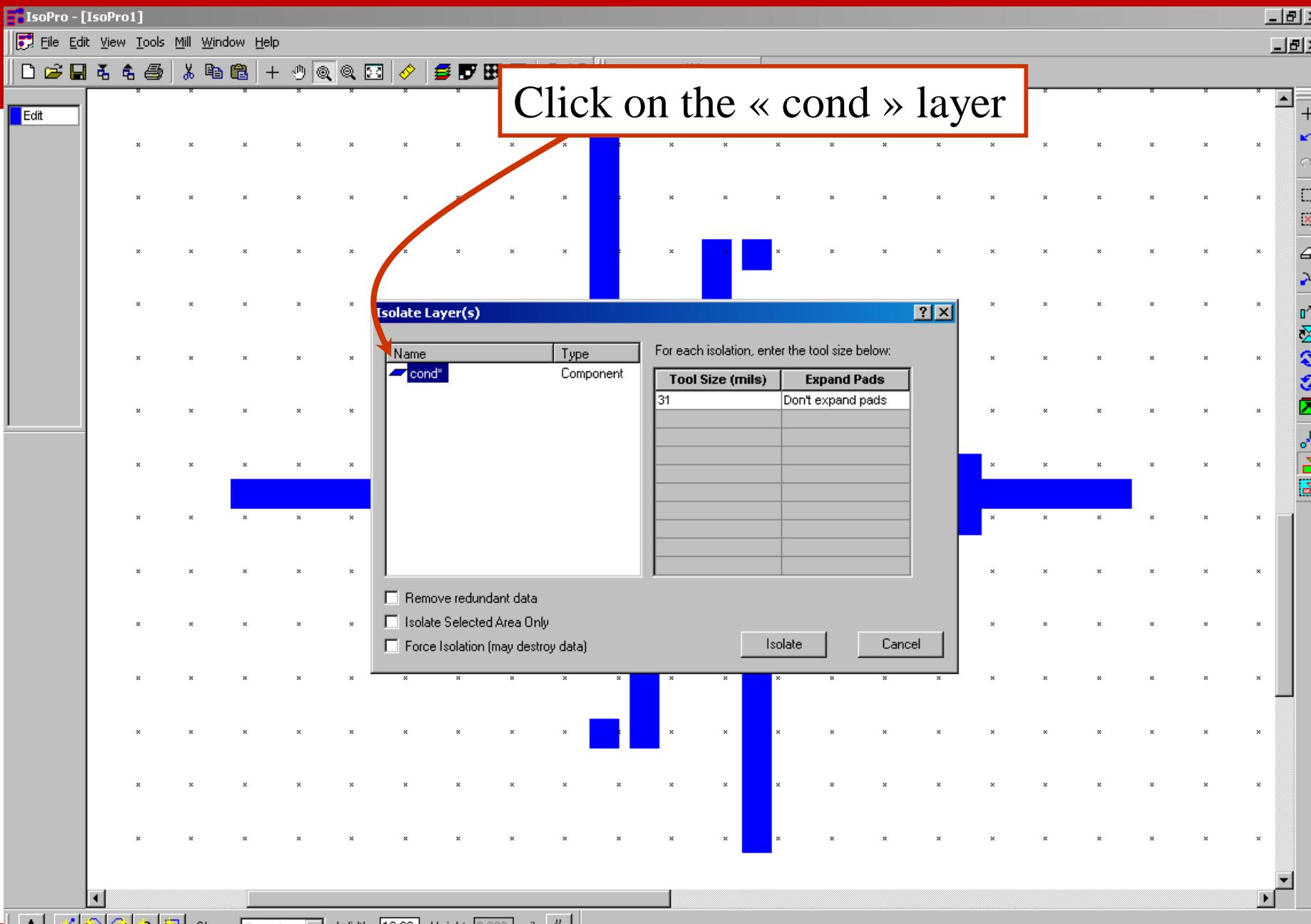
Z

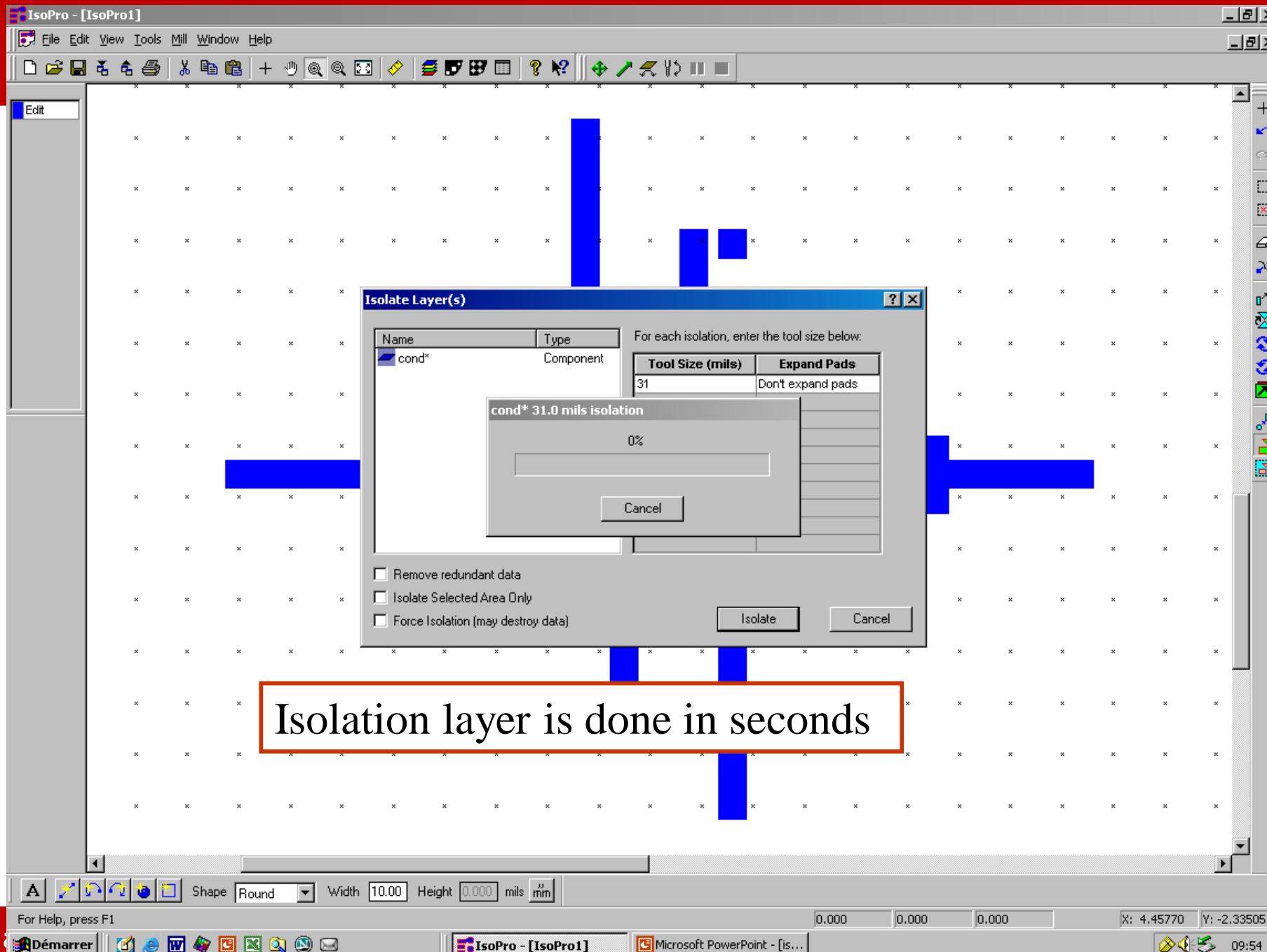
_

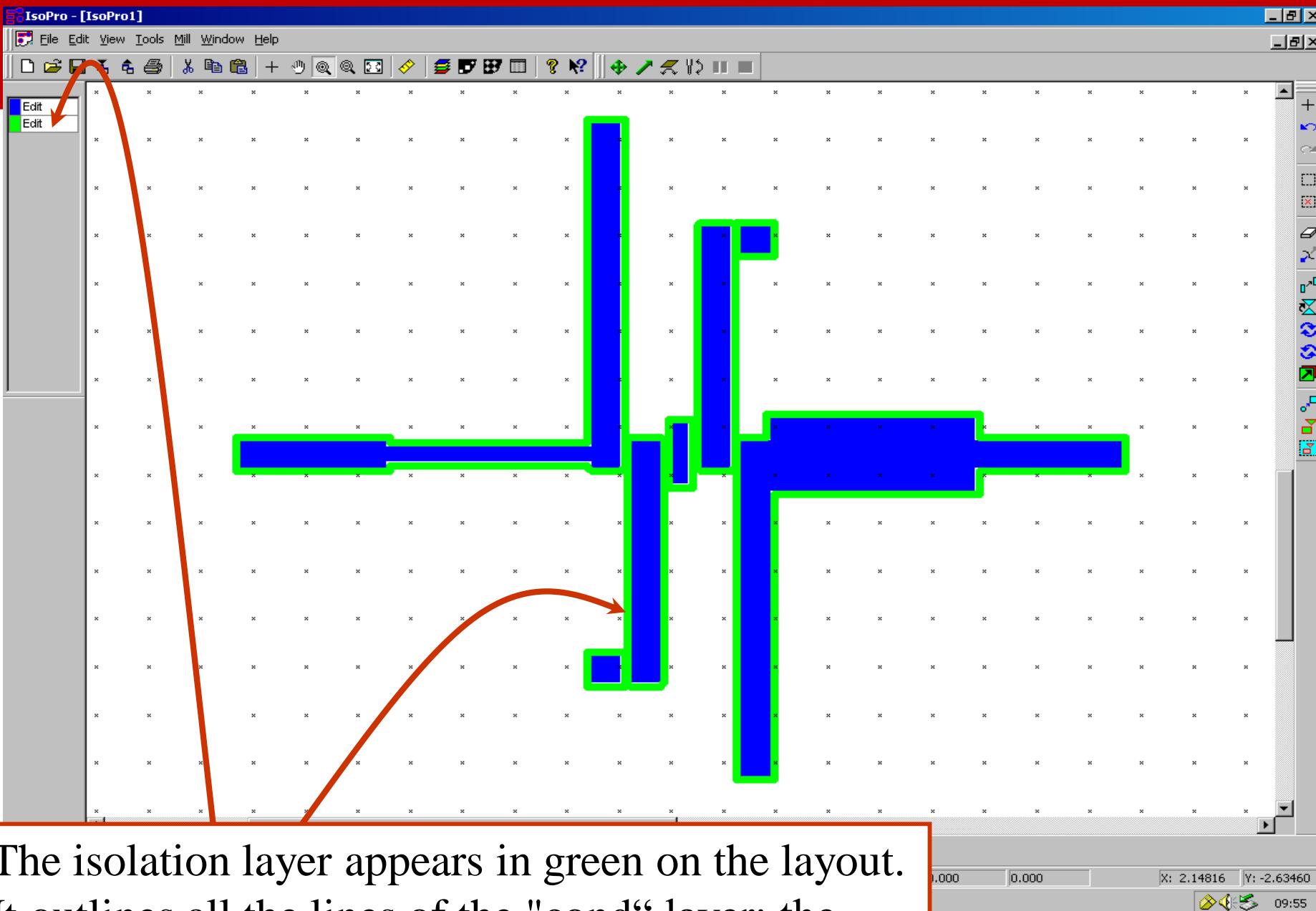


You have to choose the layer that you want to isolate ("cond": conductive) in our case

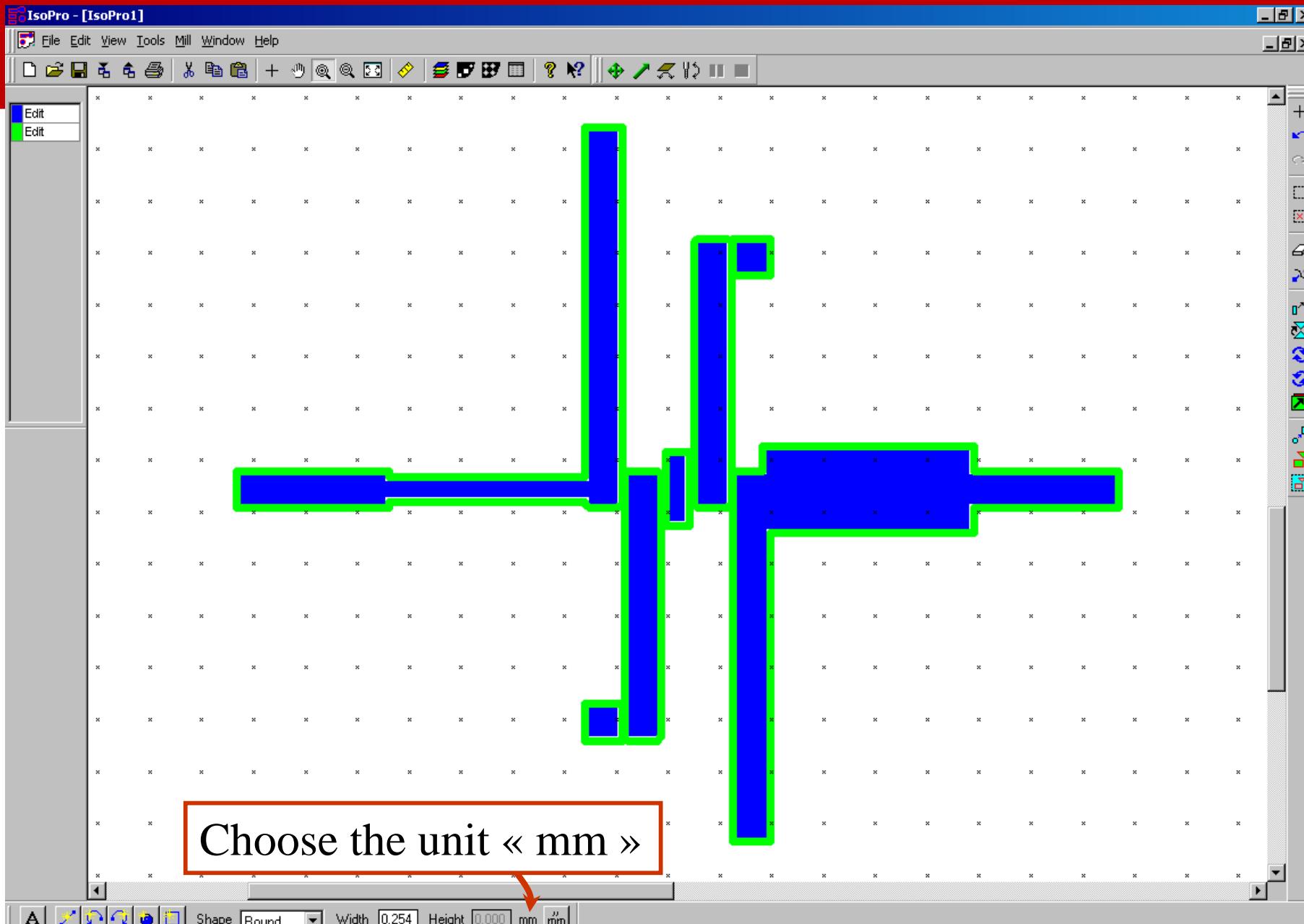
Click on the « cond » layer

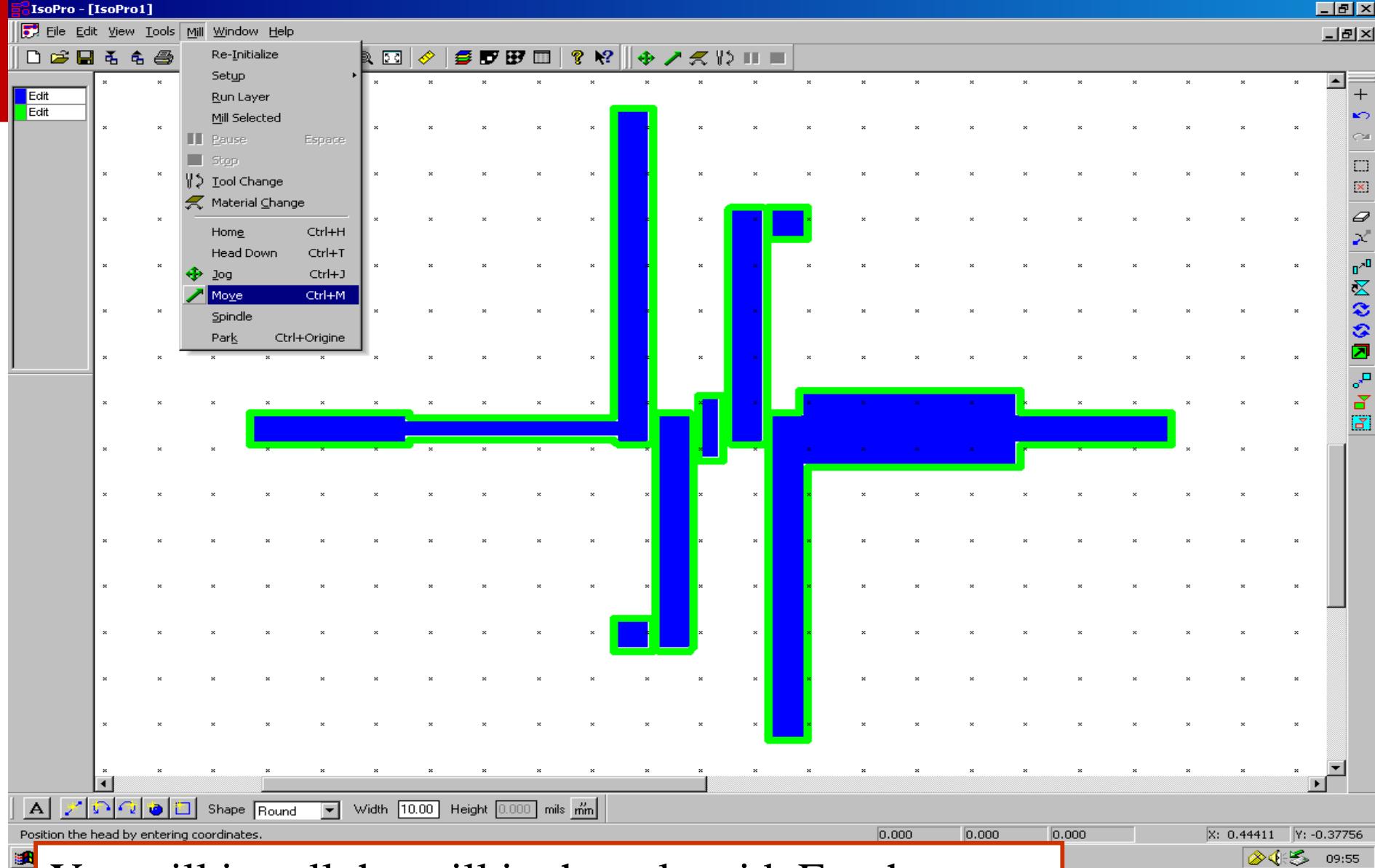




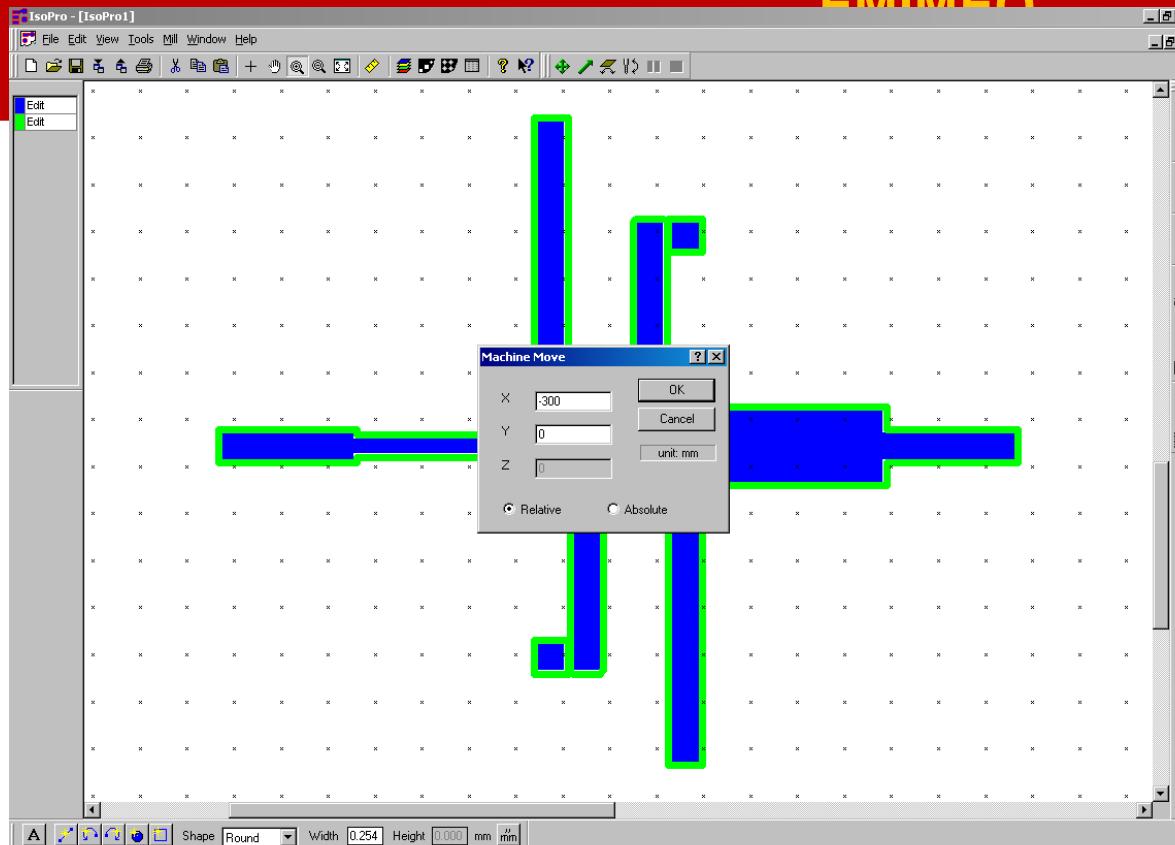


The isolation layer appears in green on the layout.
It outlines all the lines of the "cond" layer: the
copper will be removed by the selected "Edit"





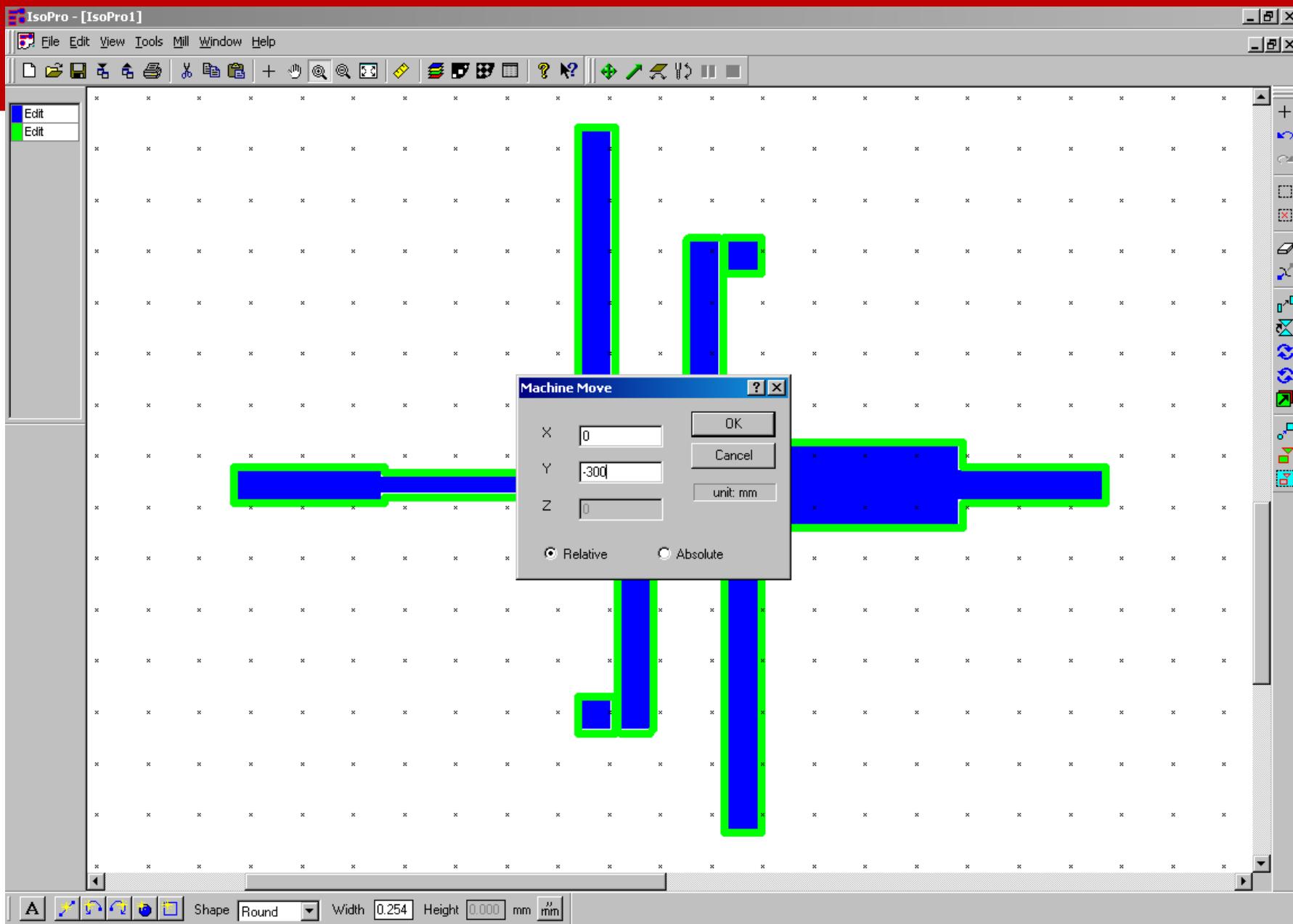
You will install the mill in the solenoid. For that, move the solenoid out of the table. Select the menu Mill / Move



Move the solenoid on the bench : -300 on the x

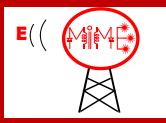
The following normal message appears
meaning you want to go too far away
=> go to the next step.

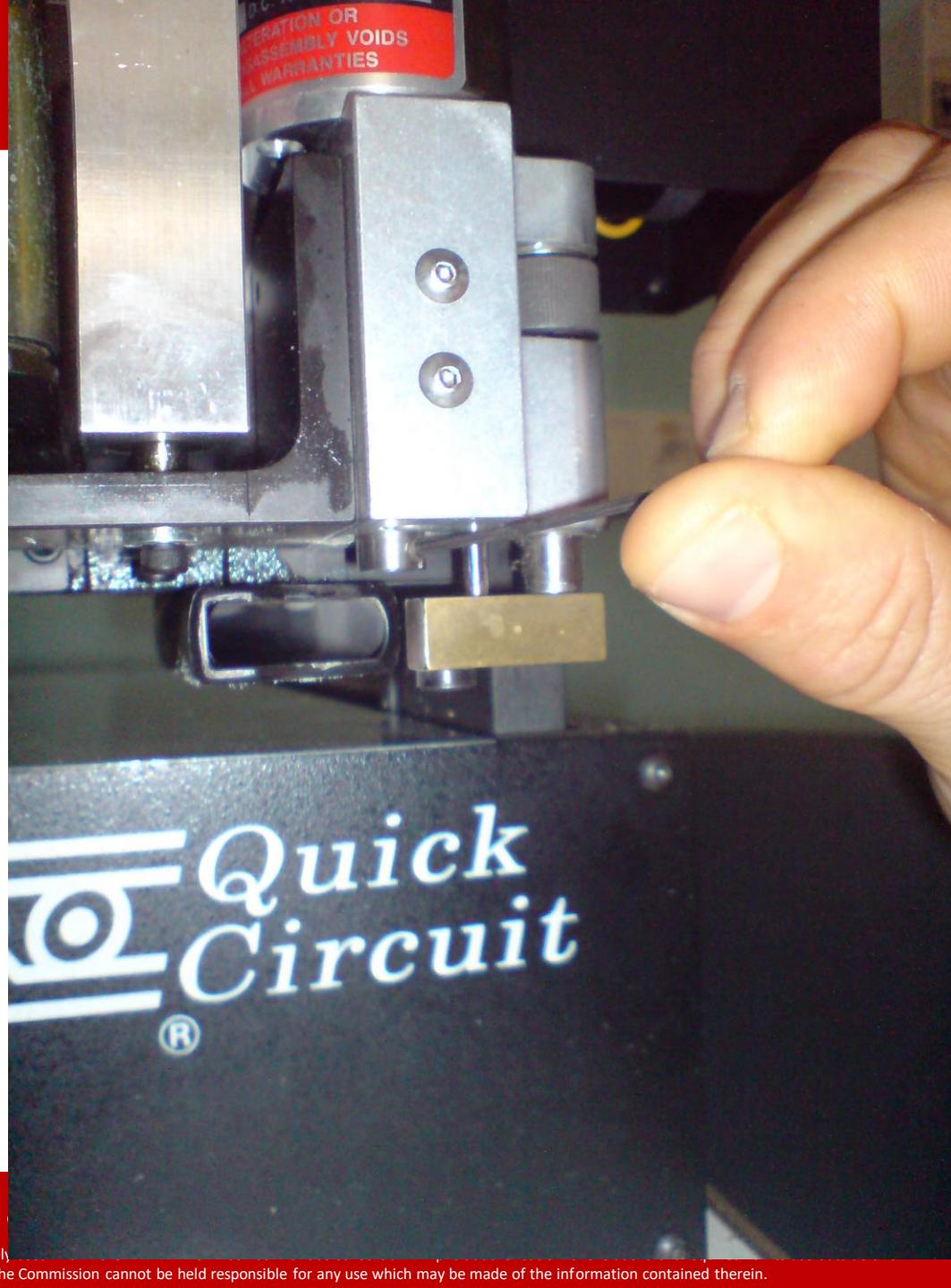




Move the solenoid on the bench : -300 on y

S

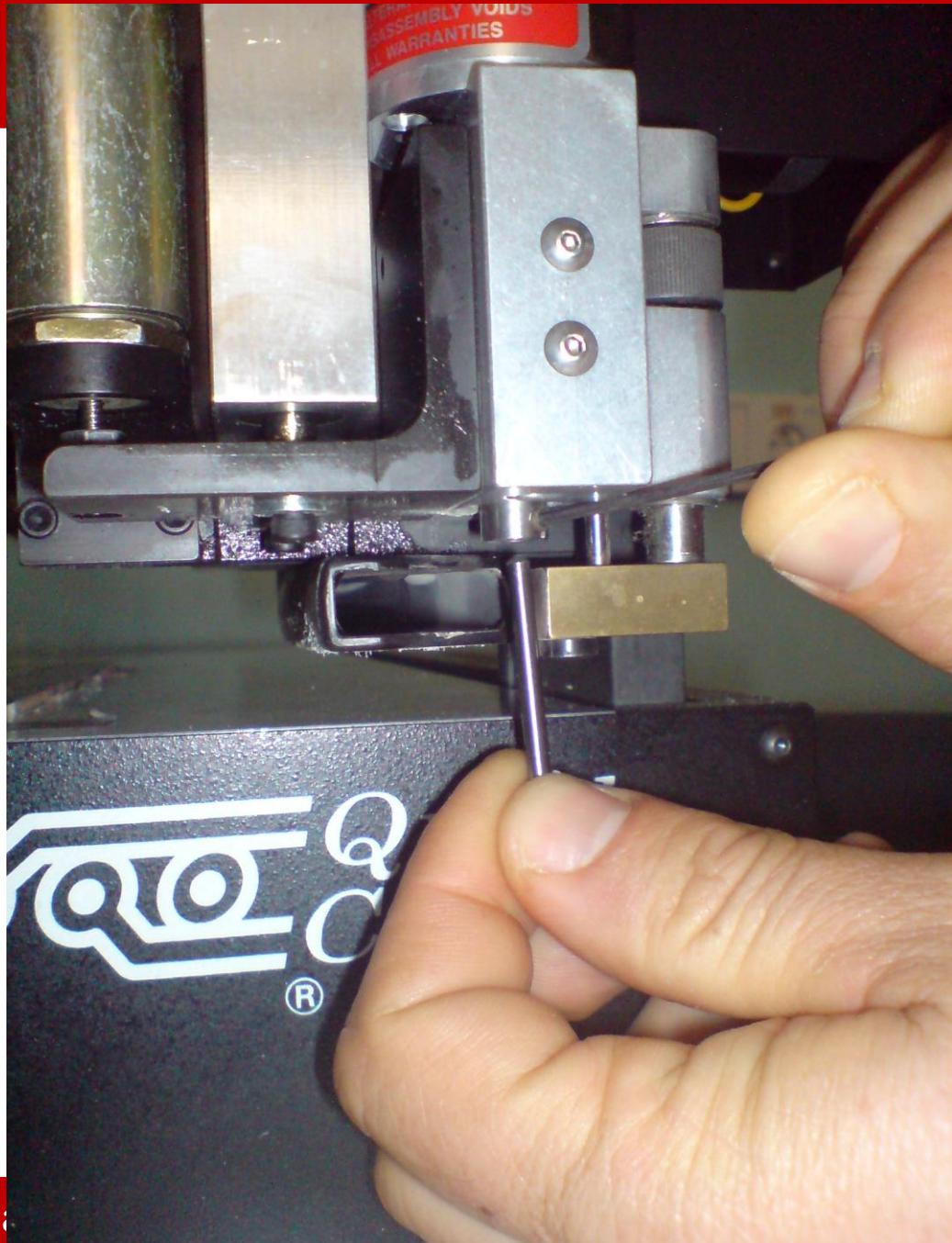




owa

The solenoid and
chuck are outside the
machine.

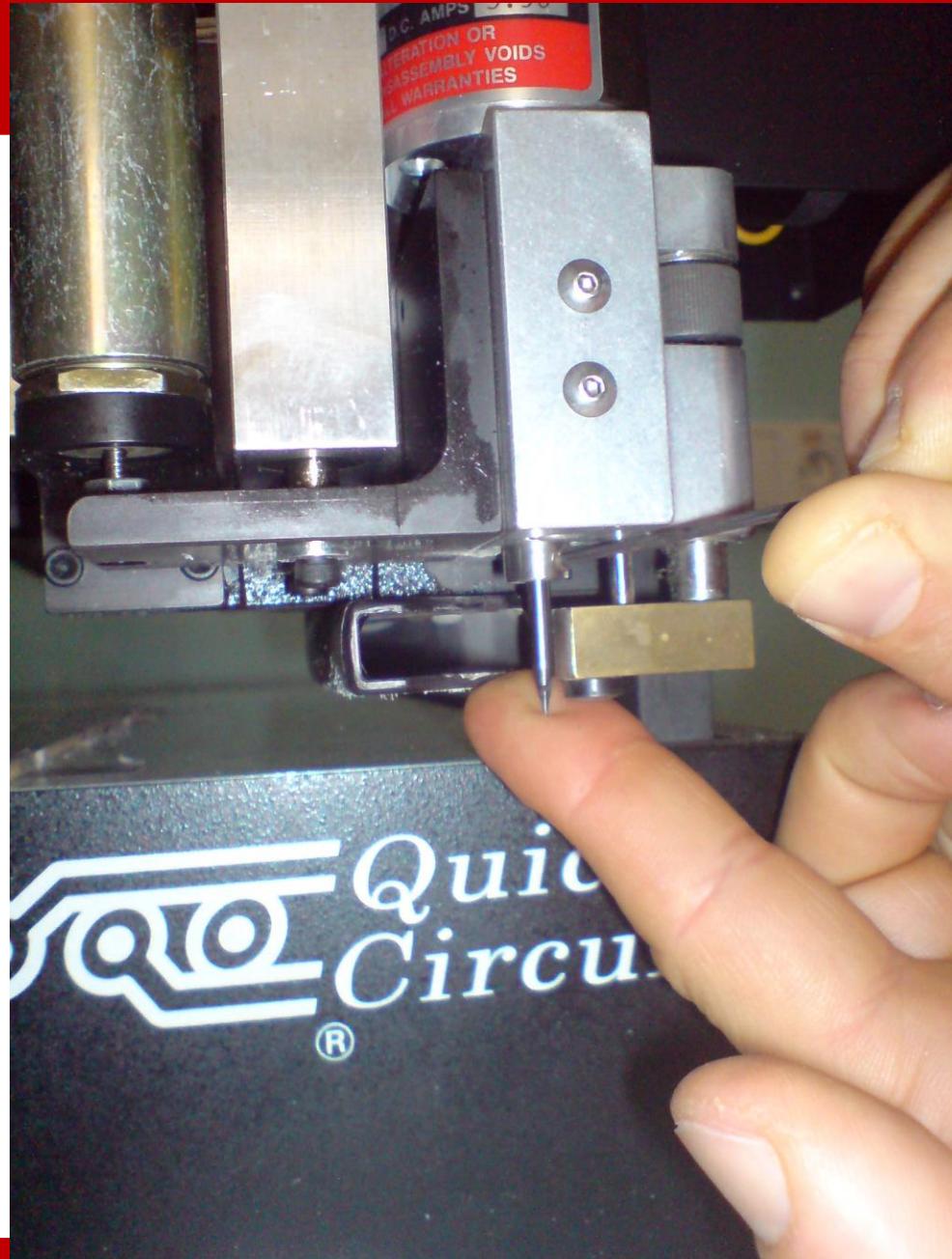
Unscrew the
clamping screw with
a wrench.



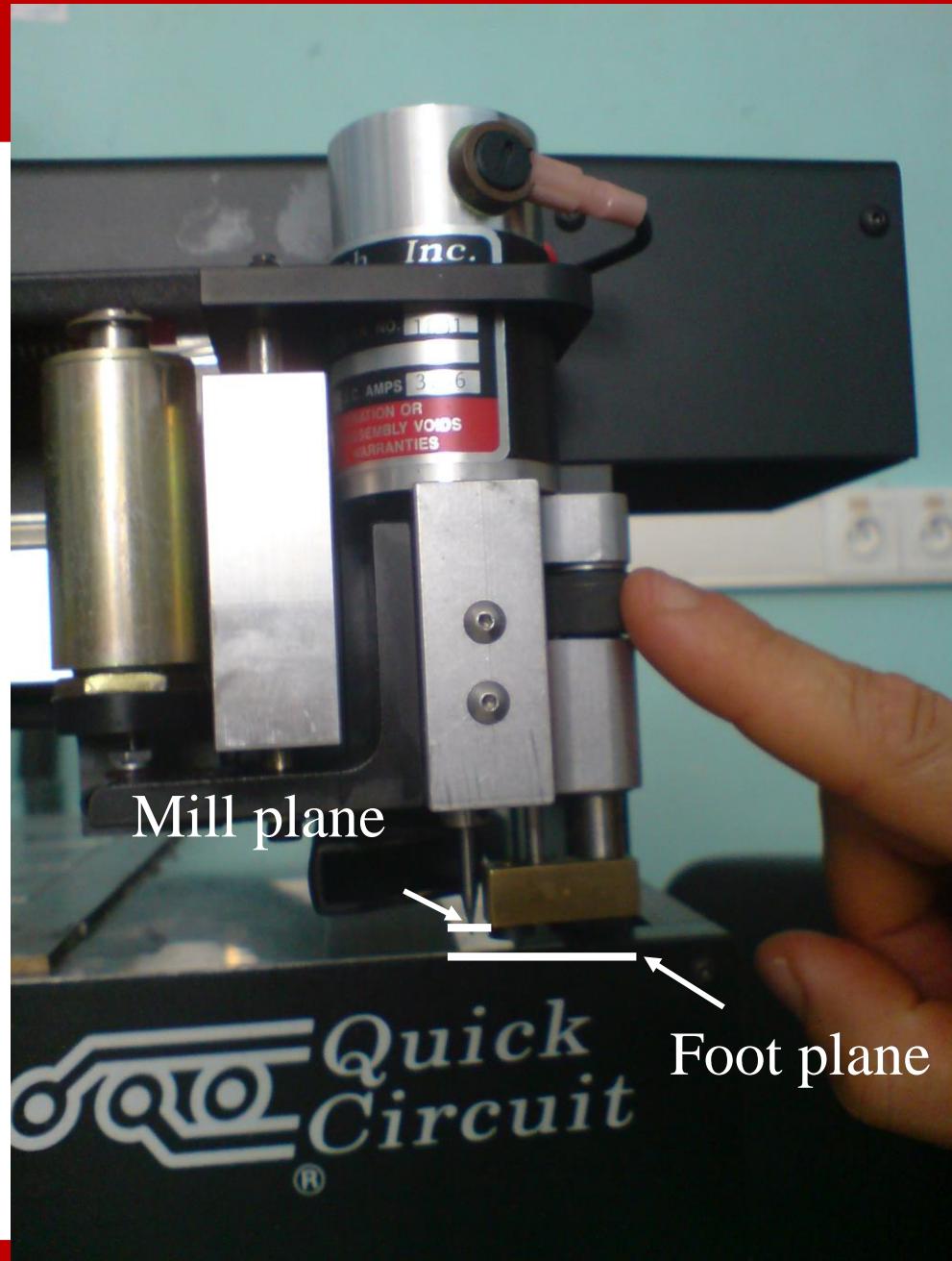
rowa Insert the selected mill into the chuck

Date

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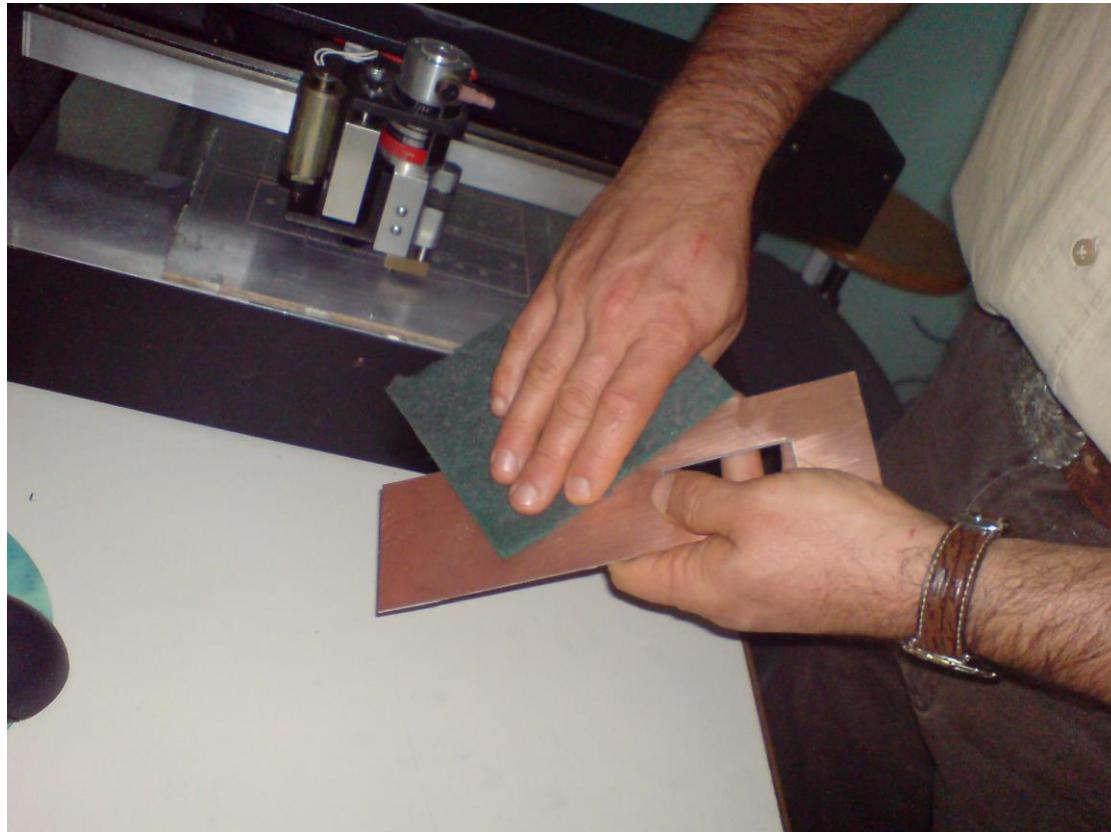


Hold the mill in the chuck and tighten the clamping screw with the wrench.

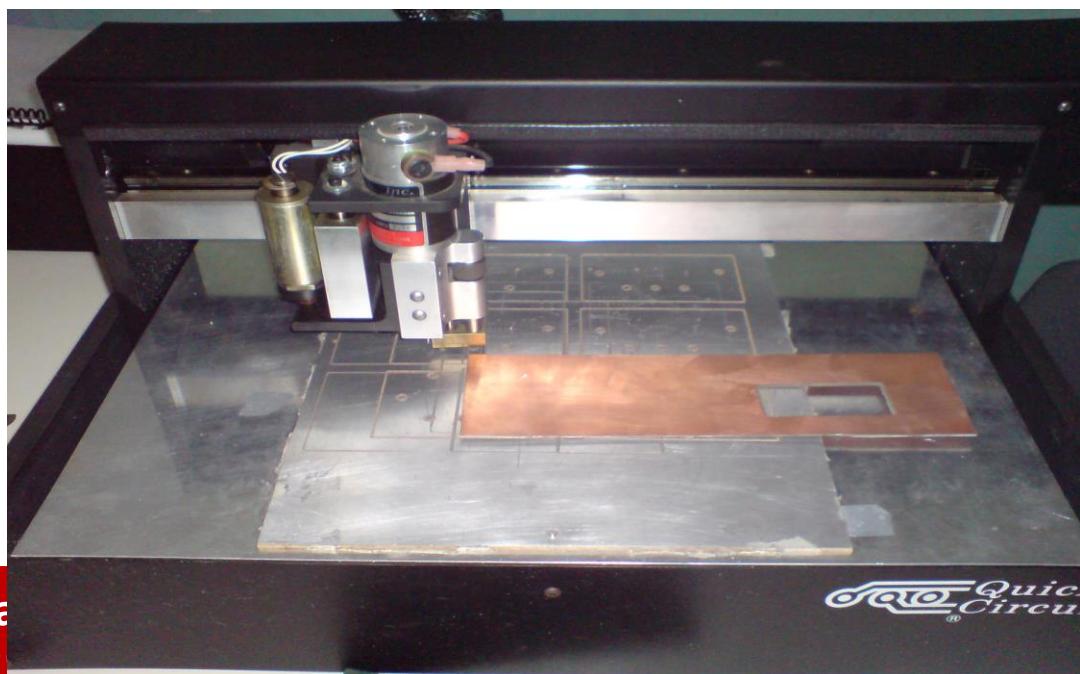
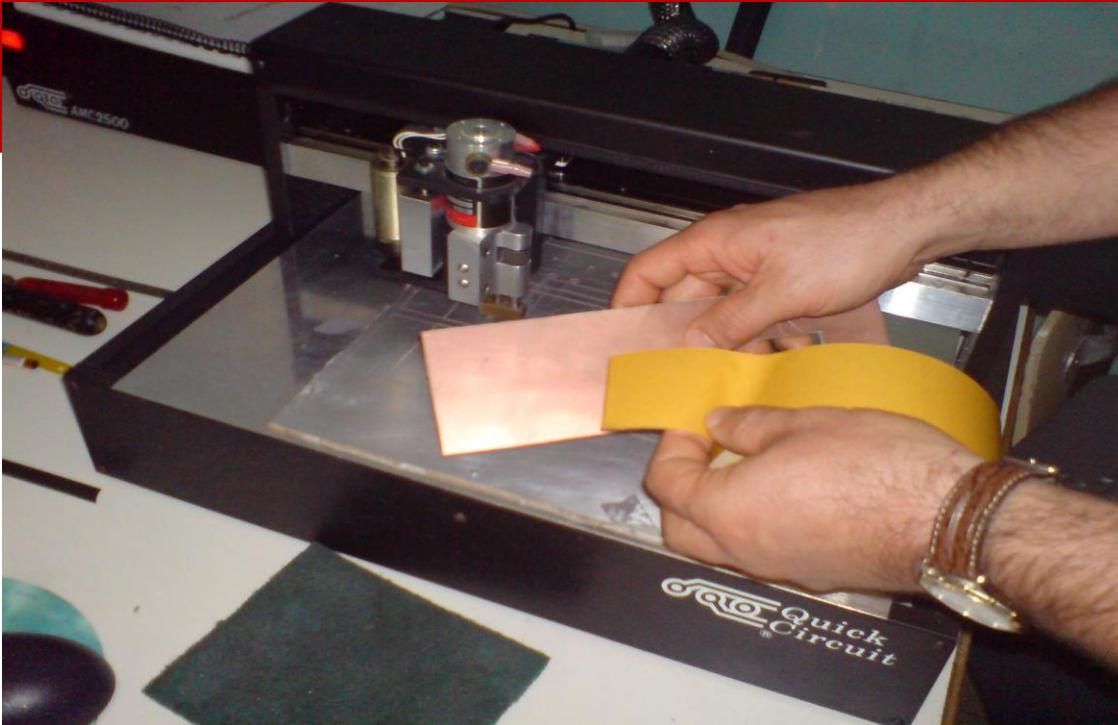


Microwave Electronics and Optics

Use the screw on the side of the solenoid so that the foot is placed under the mill.



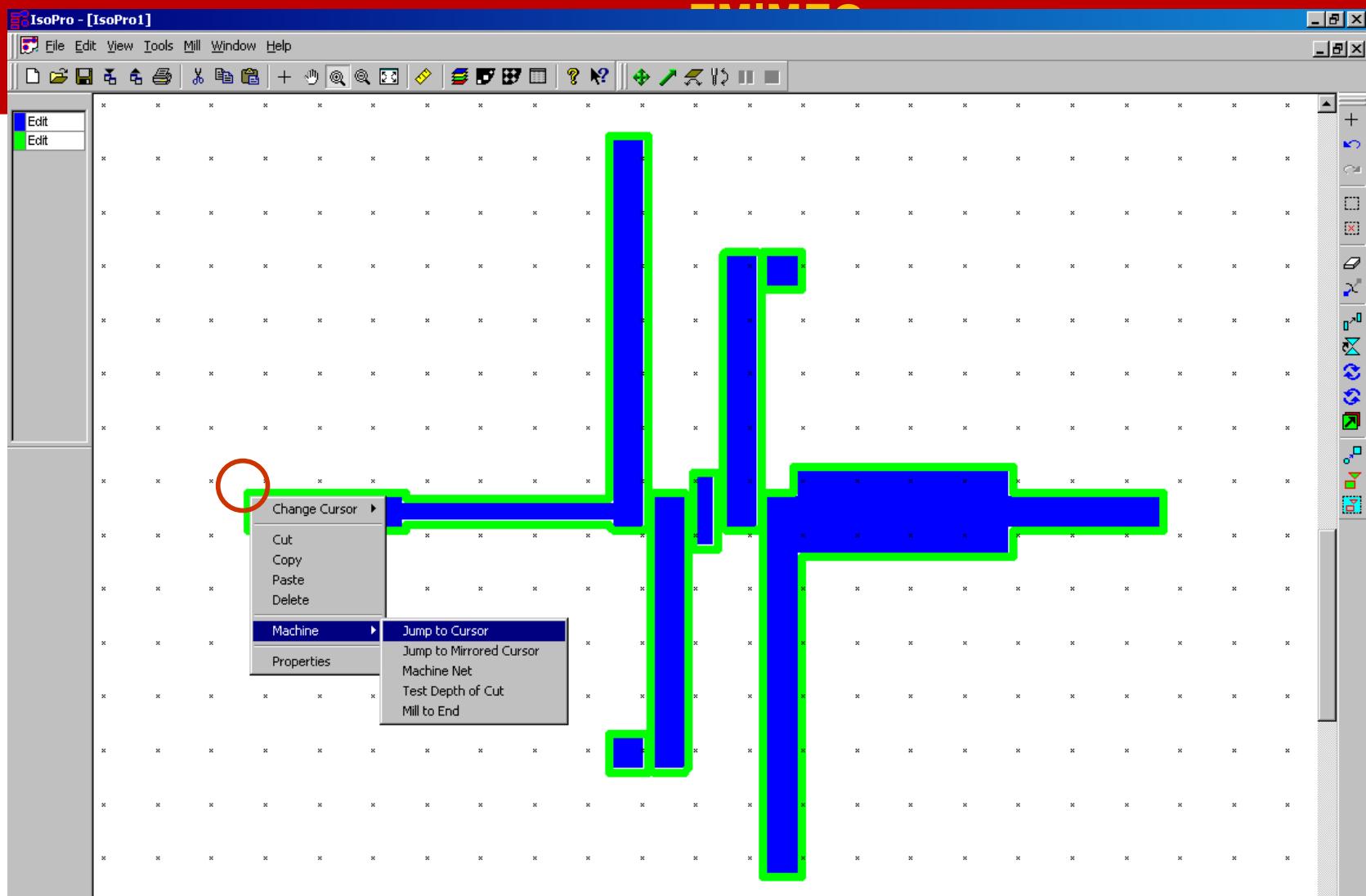
Take a piece of FR4
plate and clean it



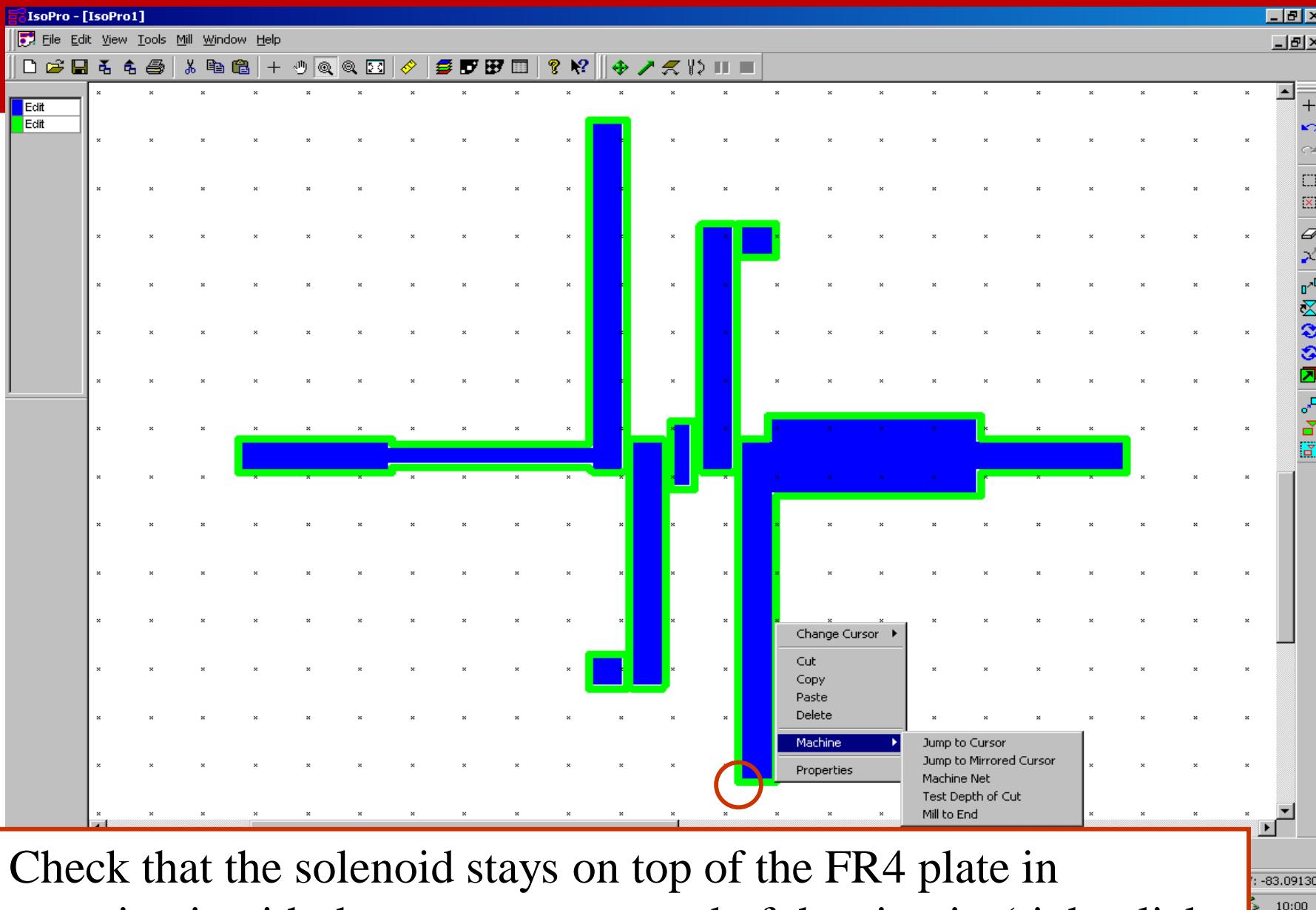
va After moving the
solenoid : +600 in y,

Use double-sided
tape to glue your FR4
layer to the engraving
table.

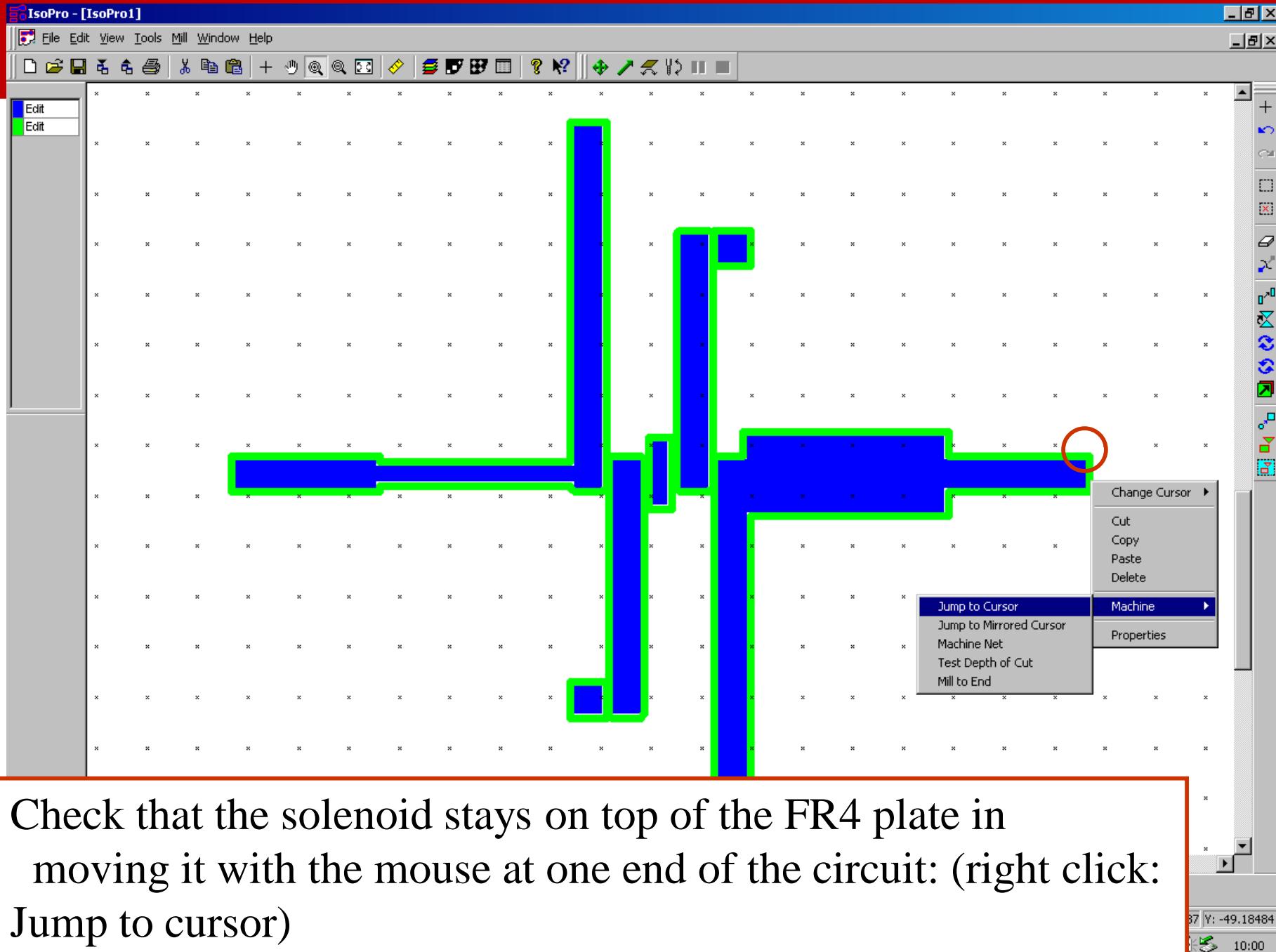
Make sure the
location of the plate
coincides with the
location of the mask
on ISOPRO



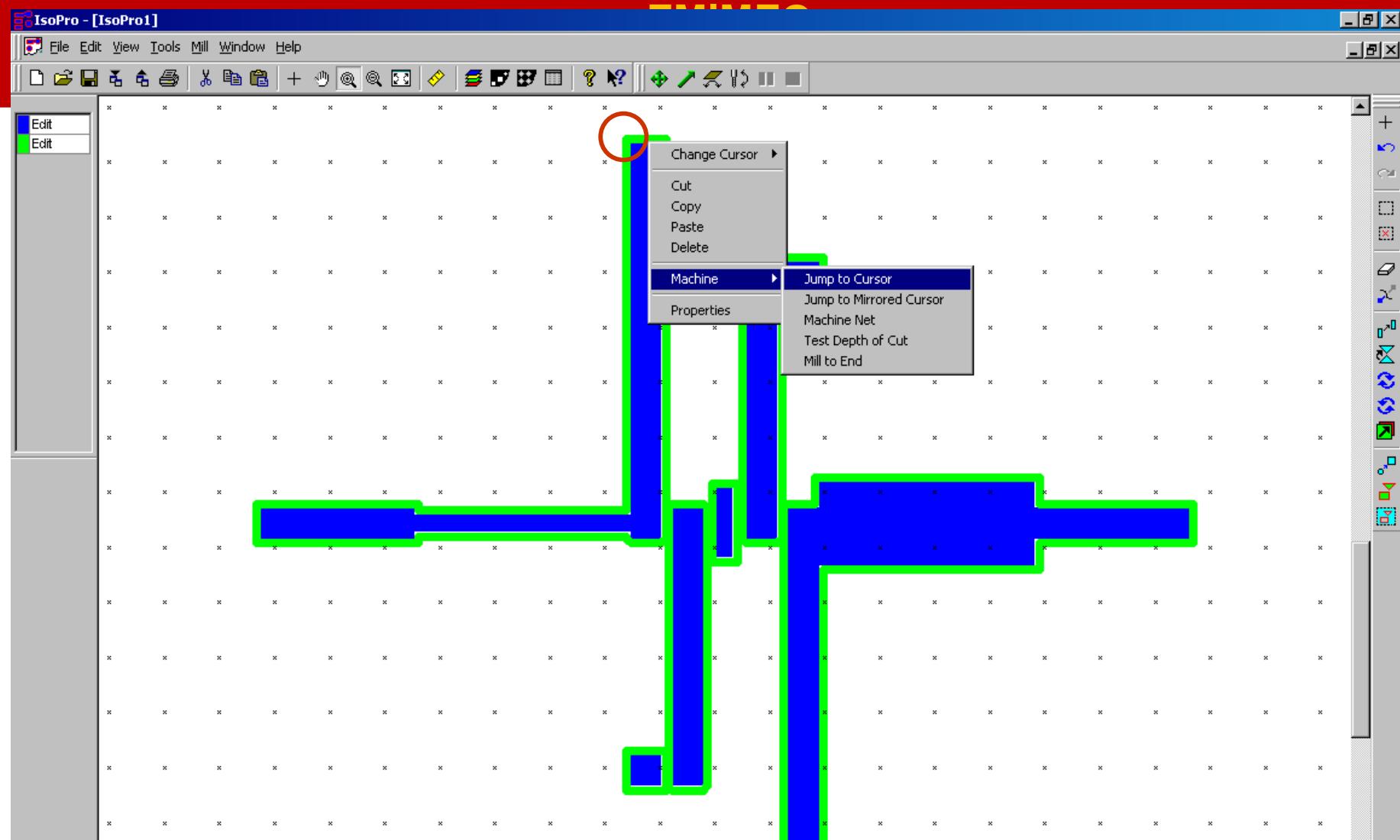
Check that the solenoid stays on top of the FR4 plate by moving it with the mouse at one end of the circuit: (right click: Jump to cursor)



Check that the solenoid stays on top of the FR4 plate in moving it with the mouse at one end of the circuit: (right click: Jump to cursor)

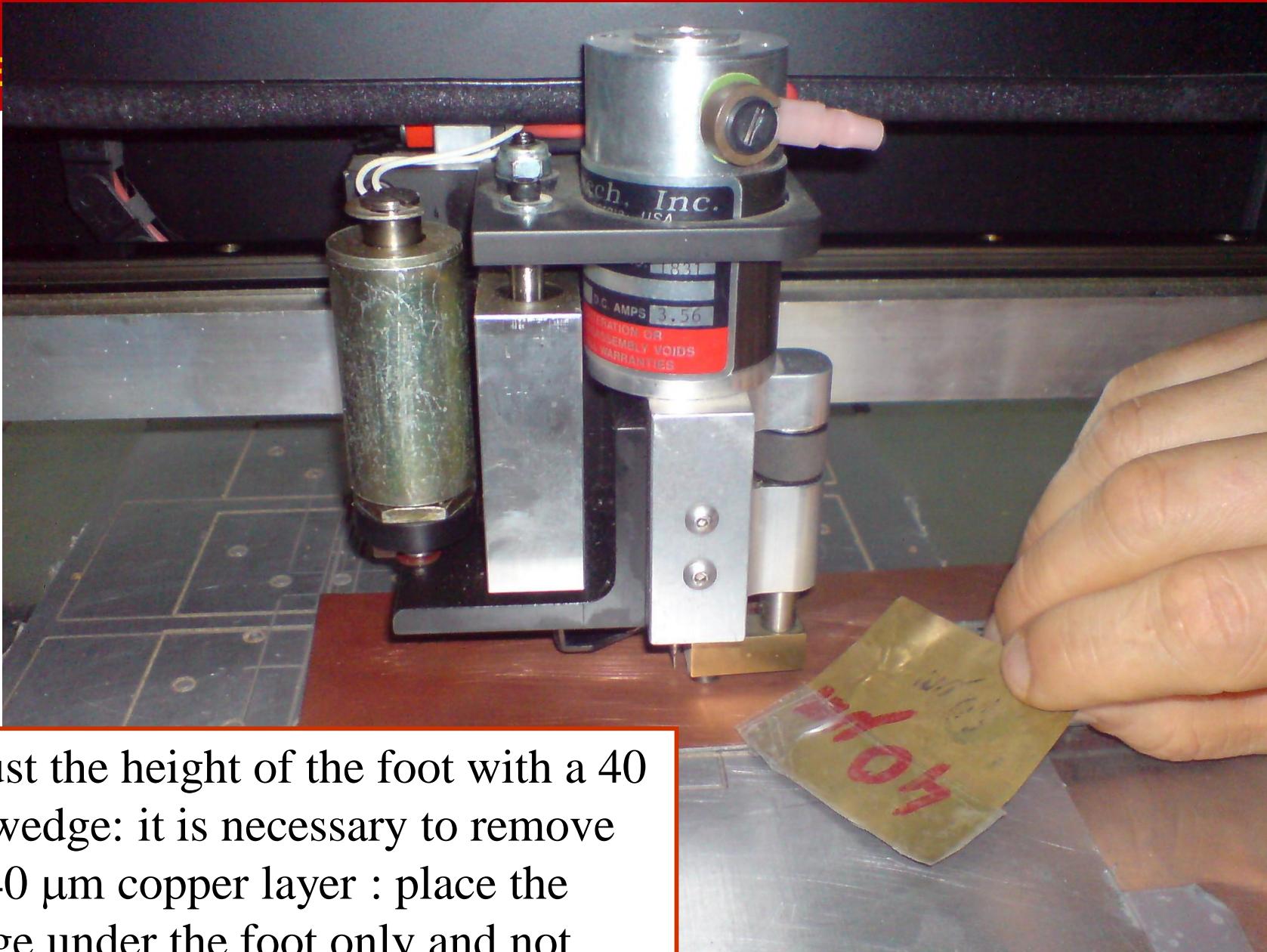


Check that the solenoid stays on top of the FR4 plate in moving it with the mouse at one end of the circuit: (right click: Jump to cursor)

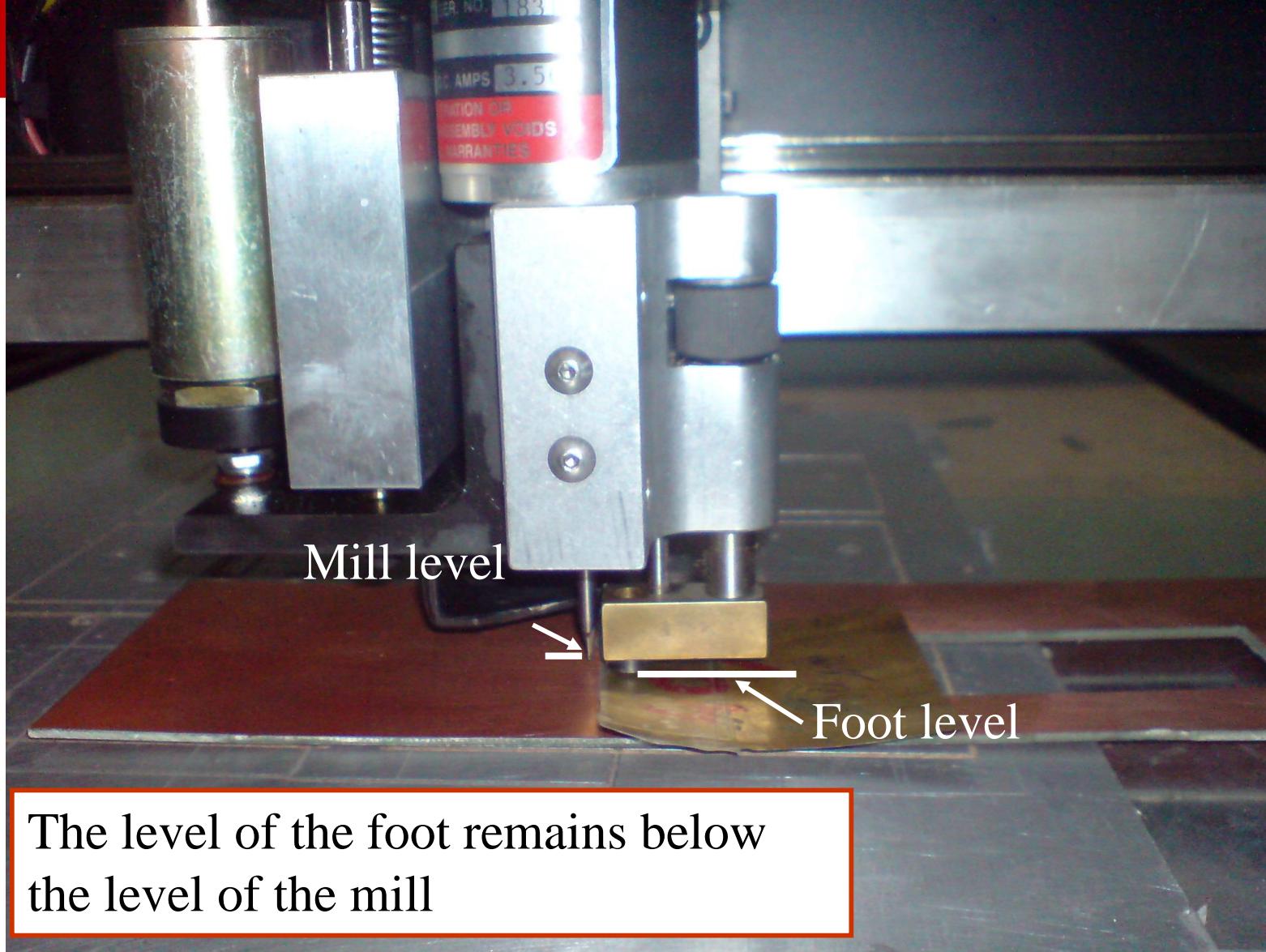


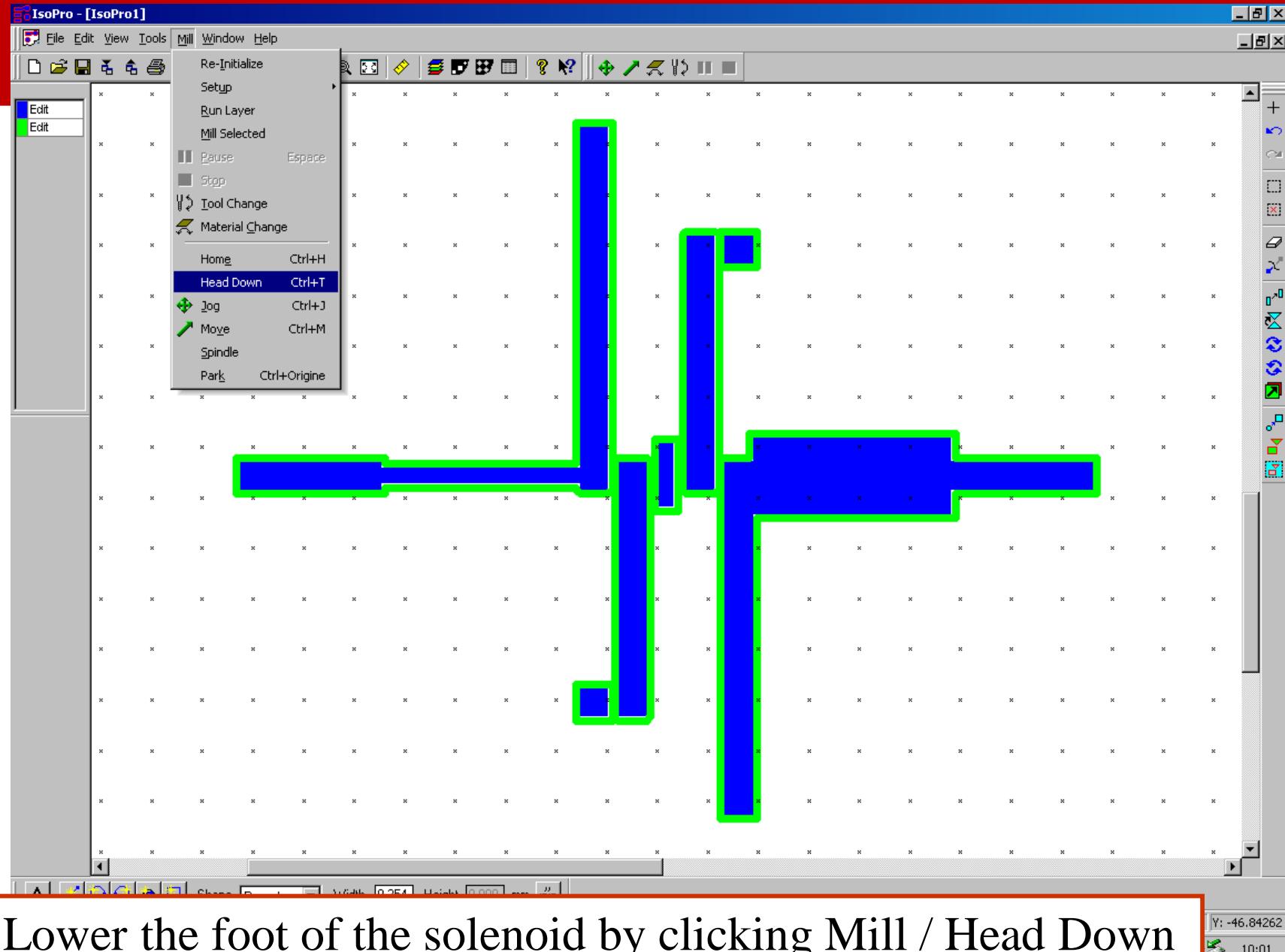
Check that the solenoid stays on top of the FR4 plate in moving it with the mouse at one end of the circuit: (right click: Jump to cursor)

E

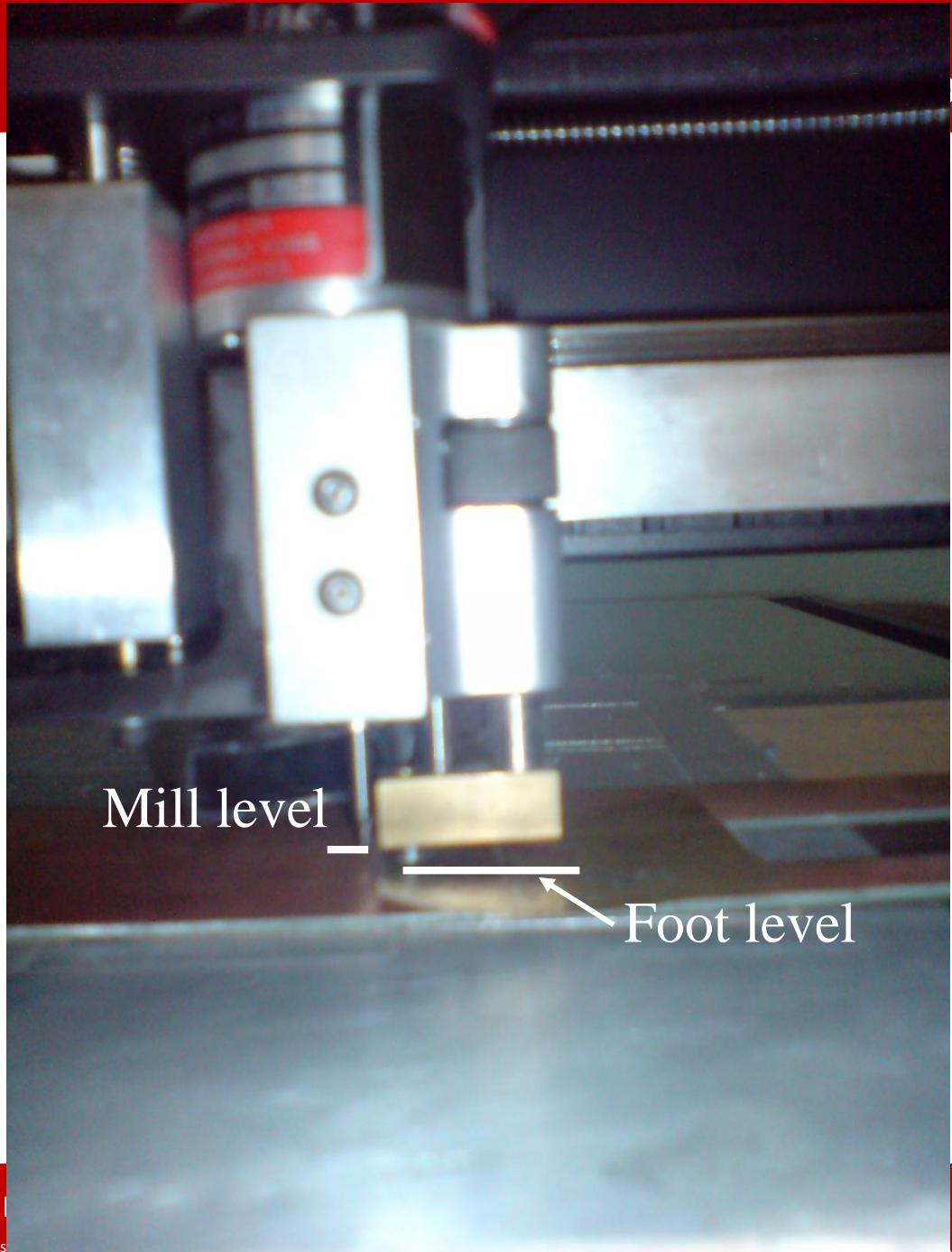


Adjust the height of the foot with a 40 µm wedge: it is necessary to remove the 40 µm copper layer : place the wedge under the foot only and not under the mill



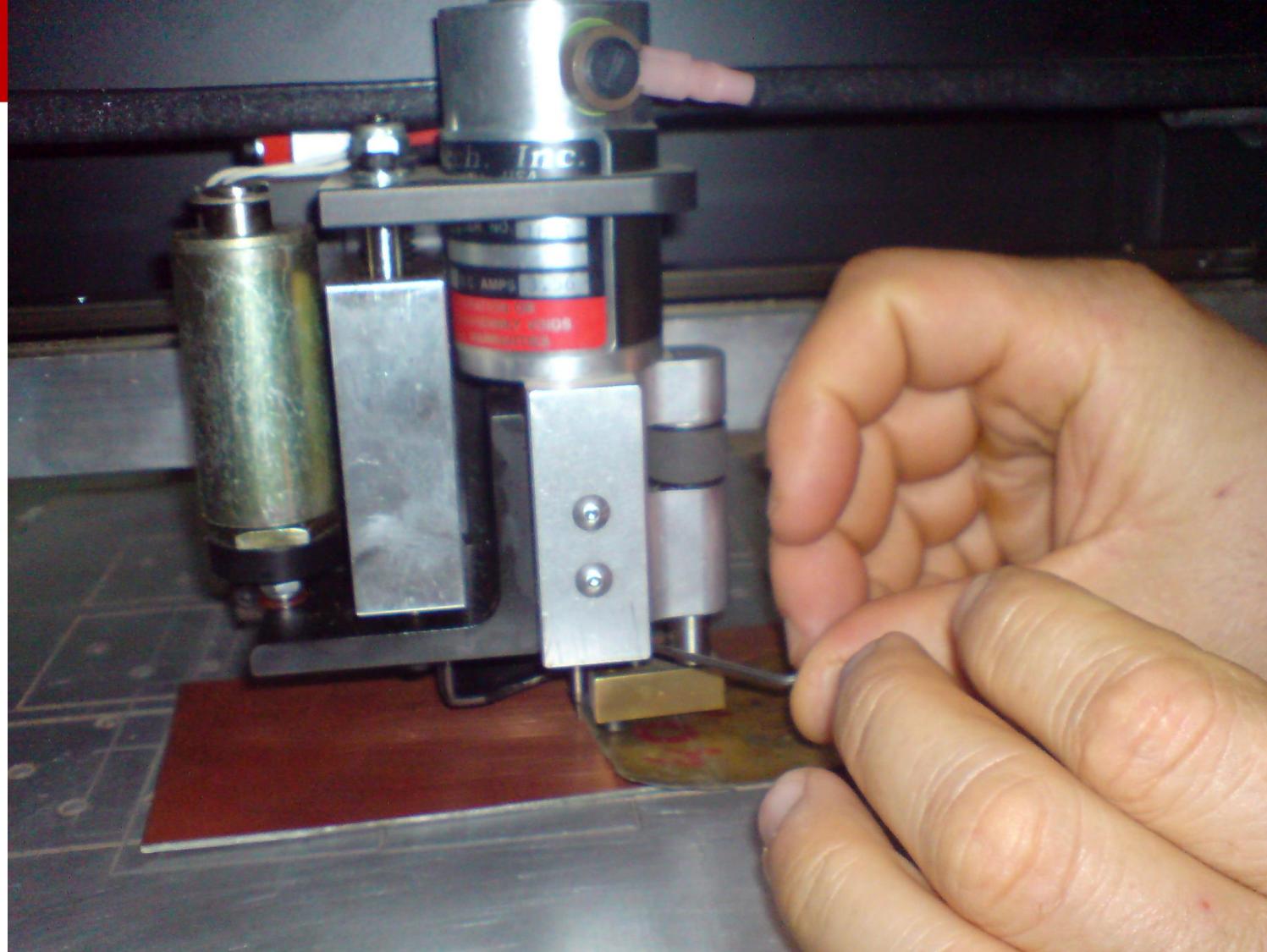


Lower the foot of the solenoid by clicking Mill / Head Down



The foot blocks the hold.

The mill is always above the foot.

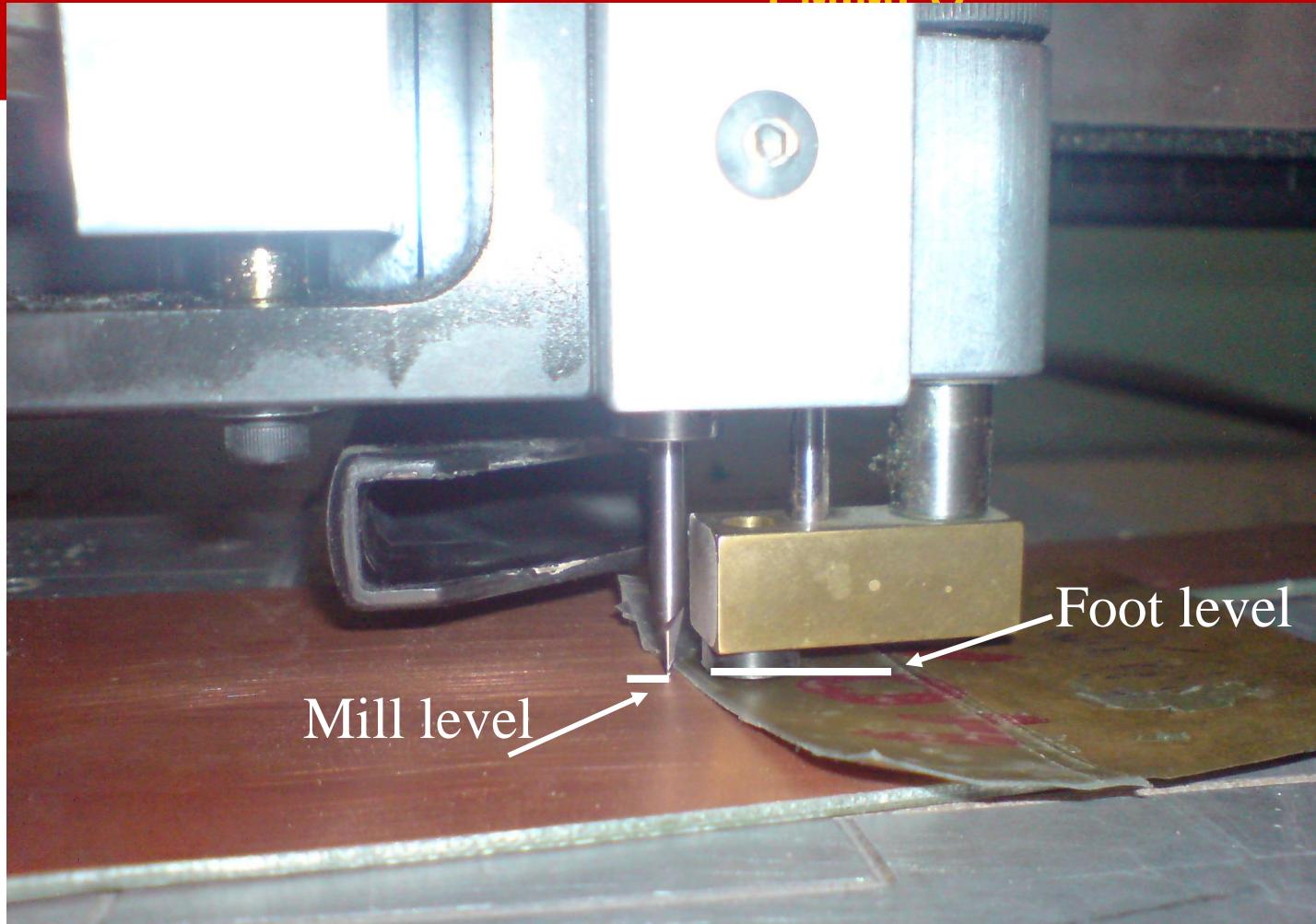


Lower the mill by unscrewing the clamping screw and tapping the solenoid

Basics of Active

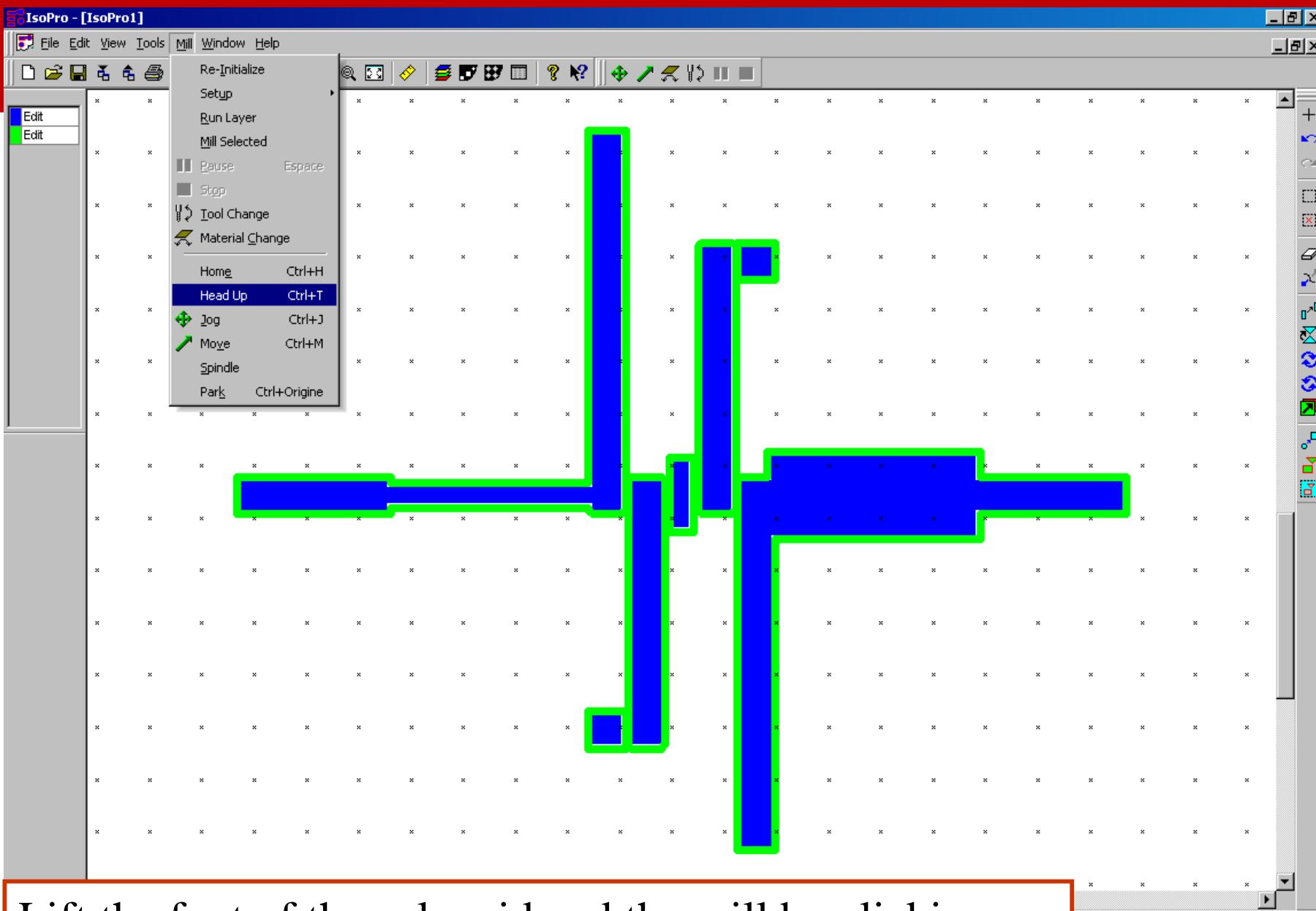
Date

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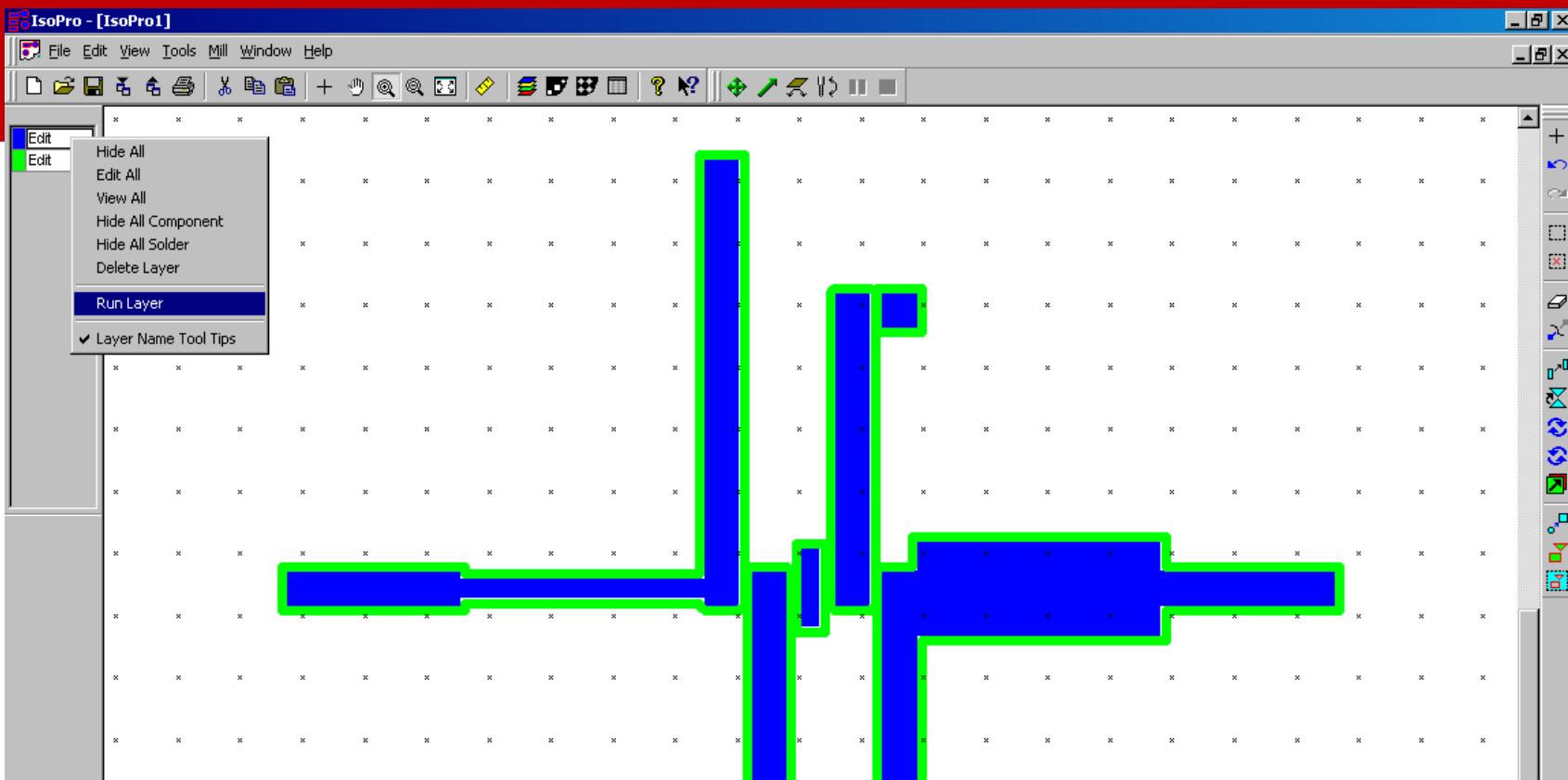


The foot blocks the hold.

The mill is now below the foot level.

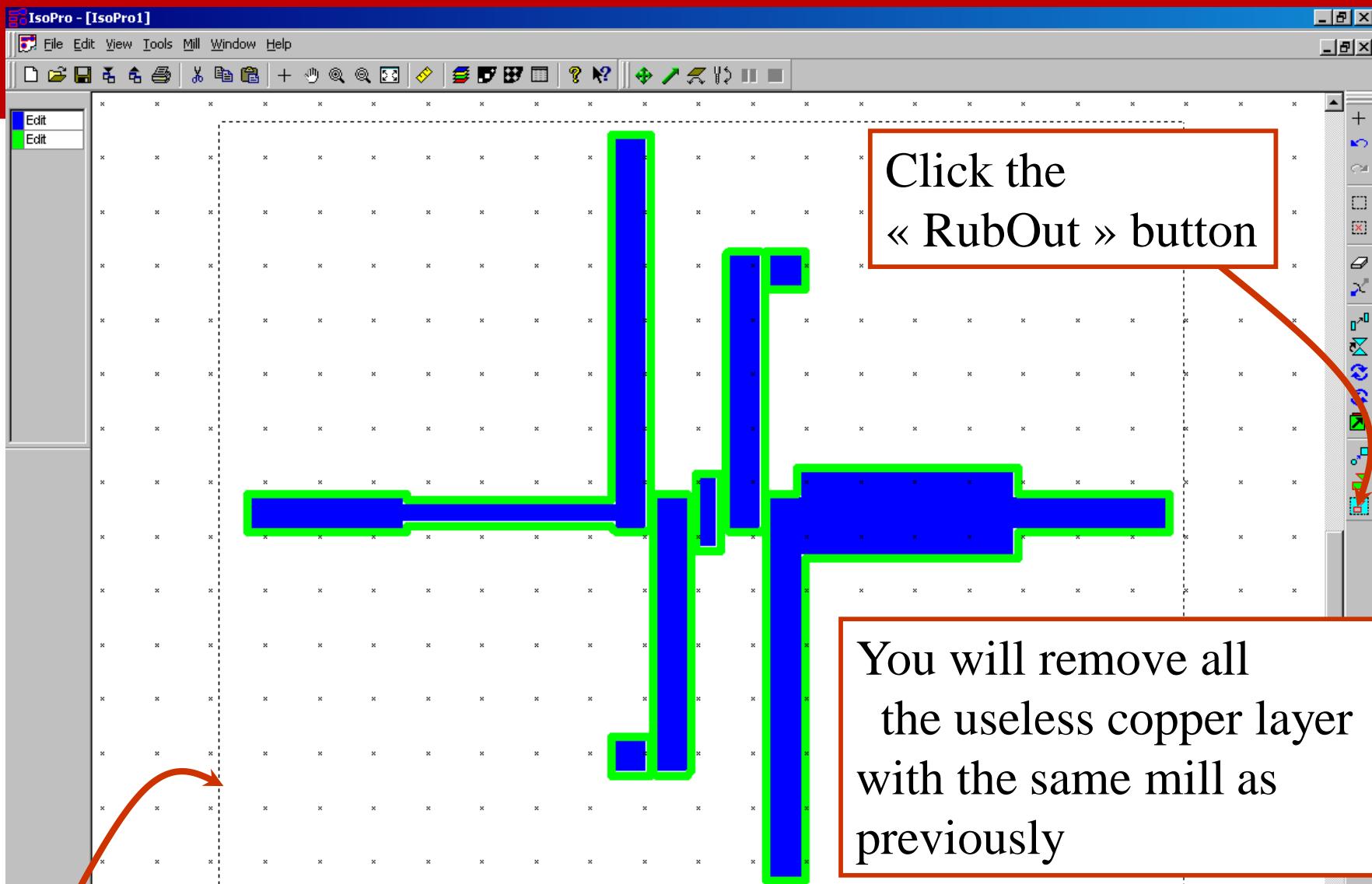


Lift the foot of the solenoid and the mill by clicking on
Mill / Head up



Bring the mouse to the left menu and the green layer: click button right and select RUN LAYER: the vacuum starts, the mill rotates and the machine will outline the lines.

If it does not work the first time, select RUN LAYER a second time.



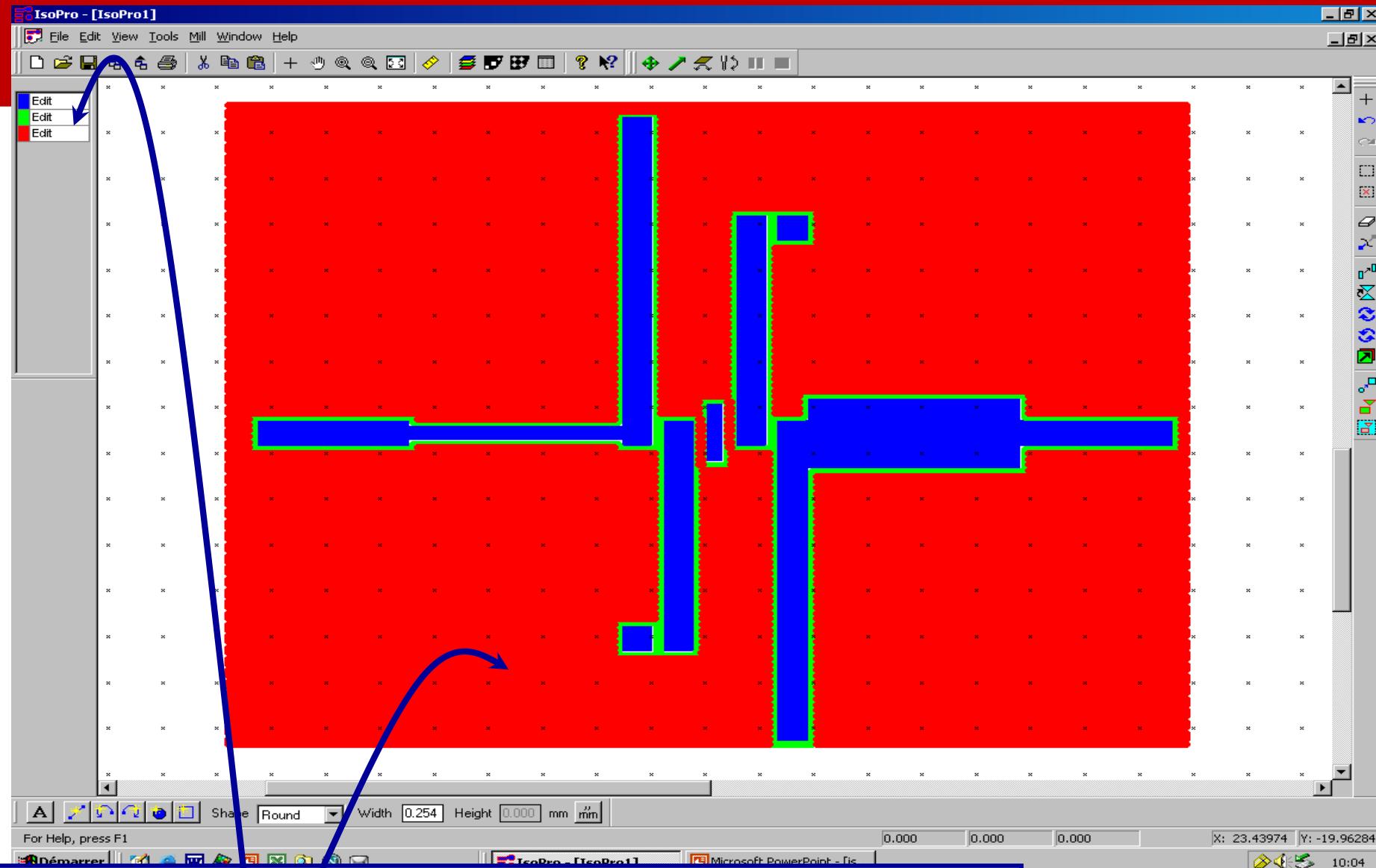
Click the
« RubOut » button

You will remove all
the useless copper layer
with the same mill as
previously

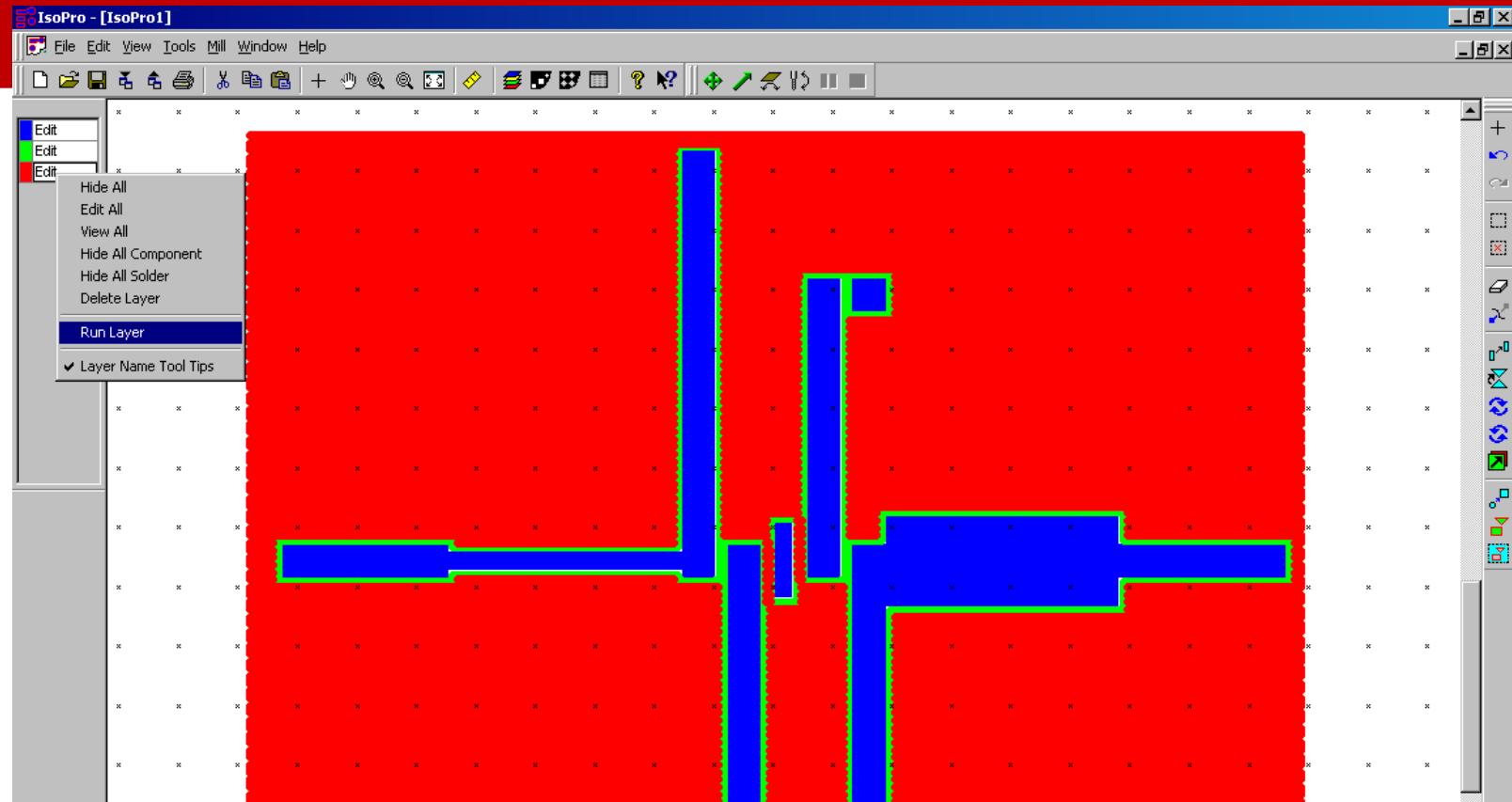
Draw with the mouse the area of copper you wish to remove:
Left and right boundaries near lines. Leave some margin up and
down

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mission. This publication



The layer of "Rub Out" appears in red on the layout
and in the menu at the top left



Bring the mouse to the left menu and the red layer: click button right and select RUN LAYER: the vacuum starts, the mill rotates and the machine will remove unnecessary copper.

If it does not work the first time, select RUN LAYER a second time.

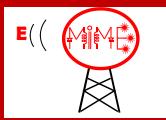
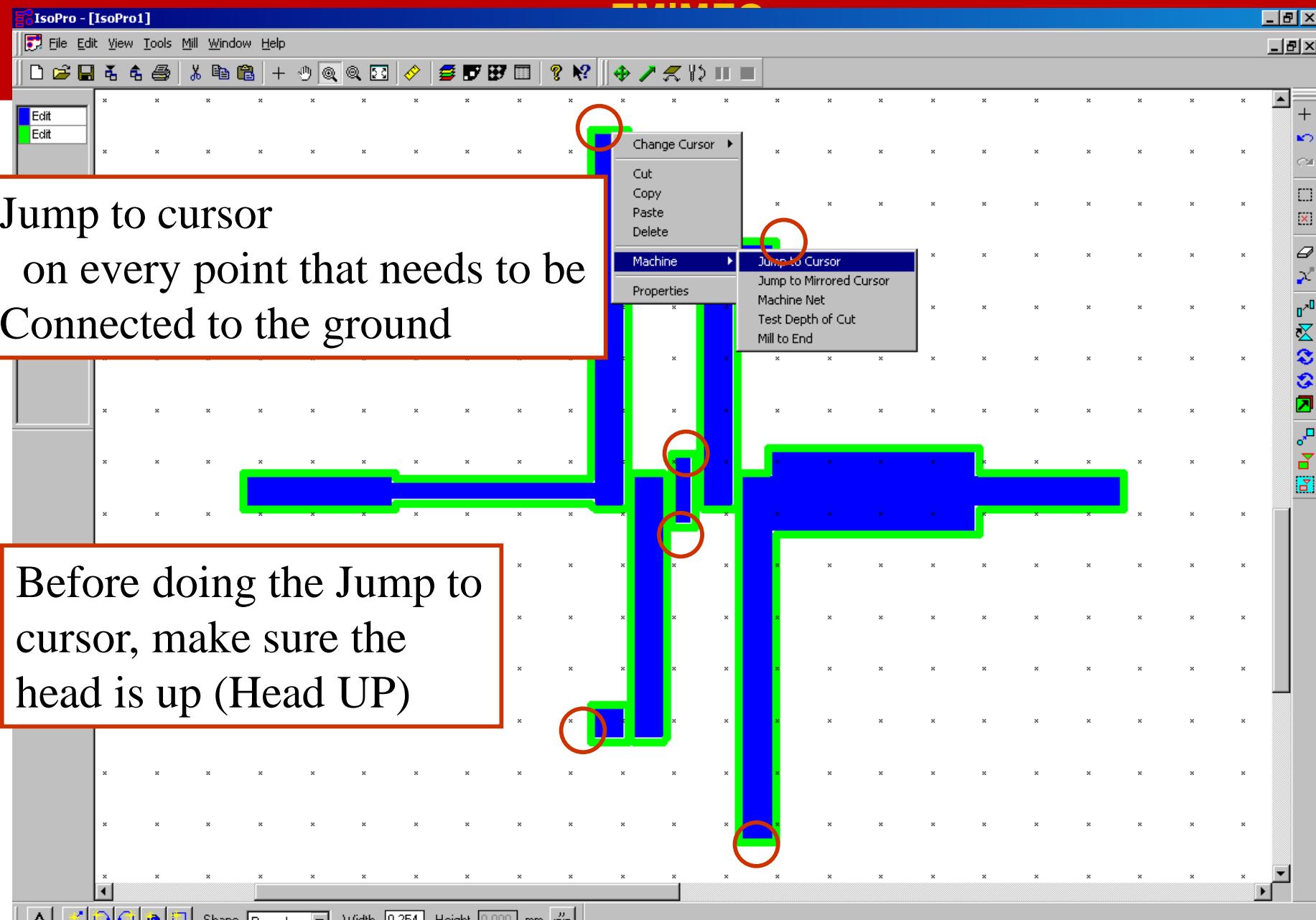
Date

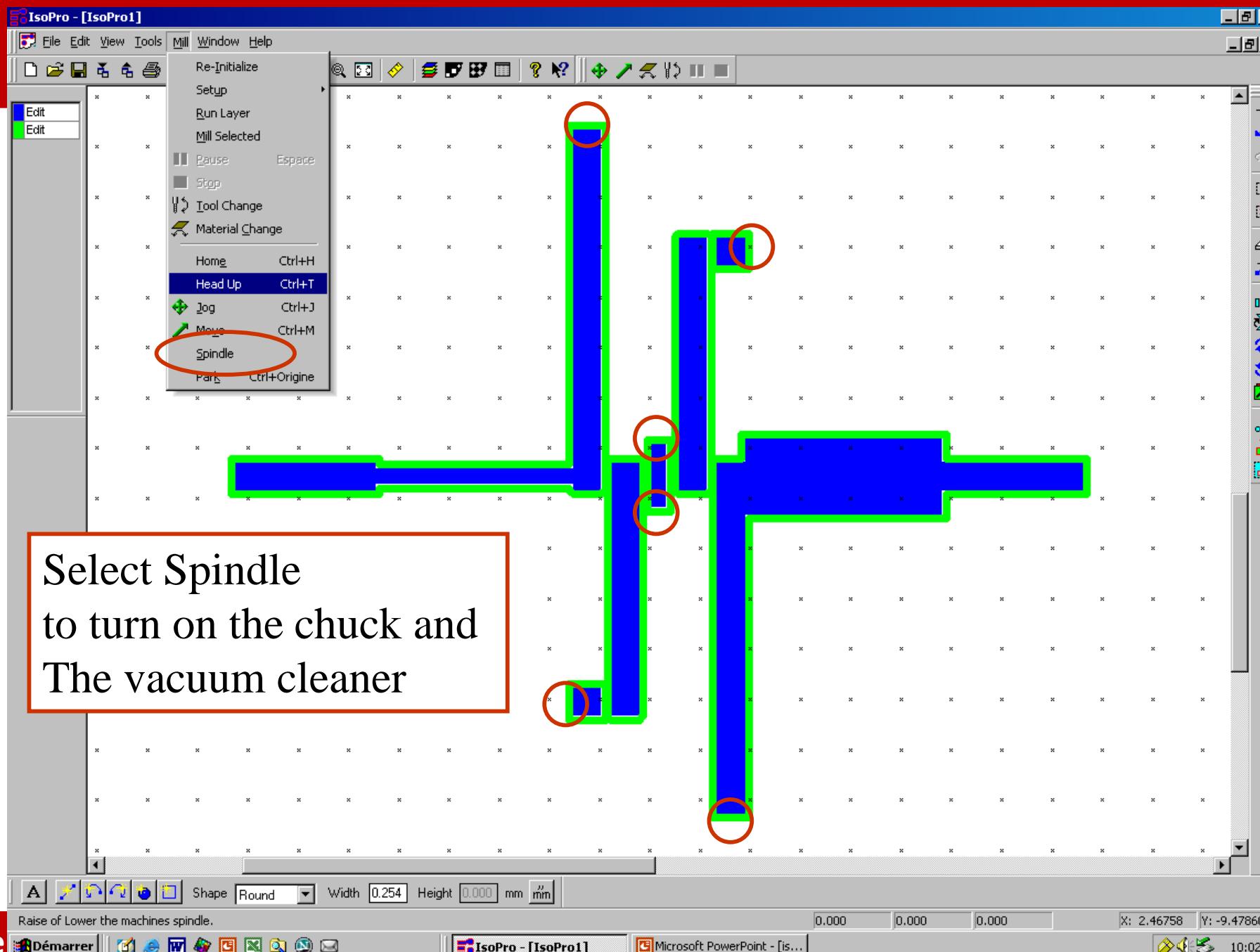
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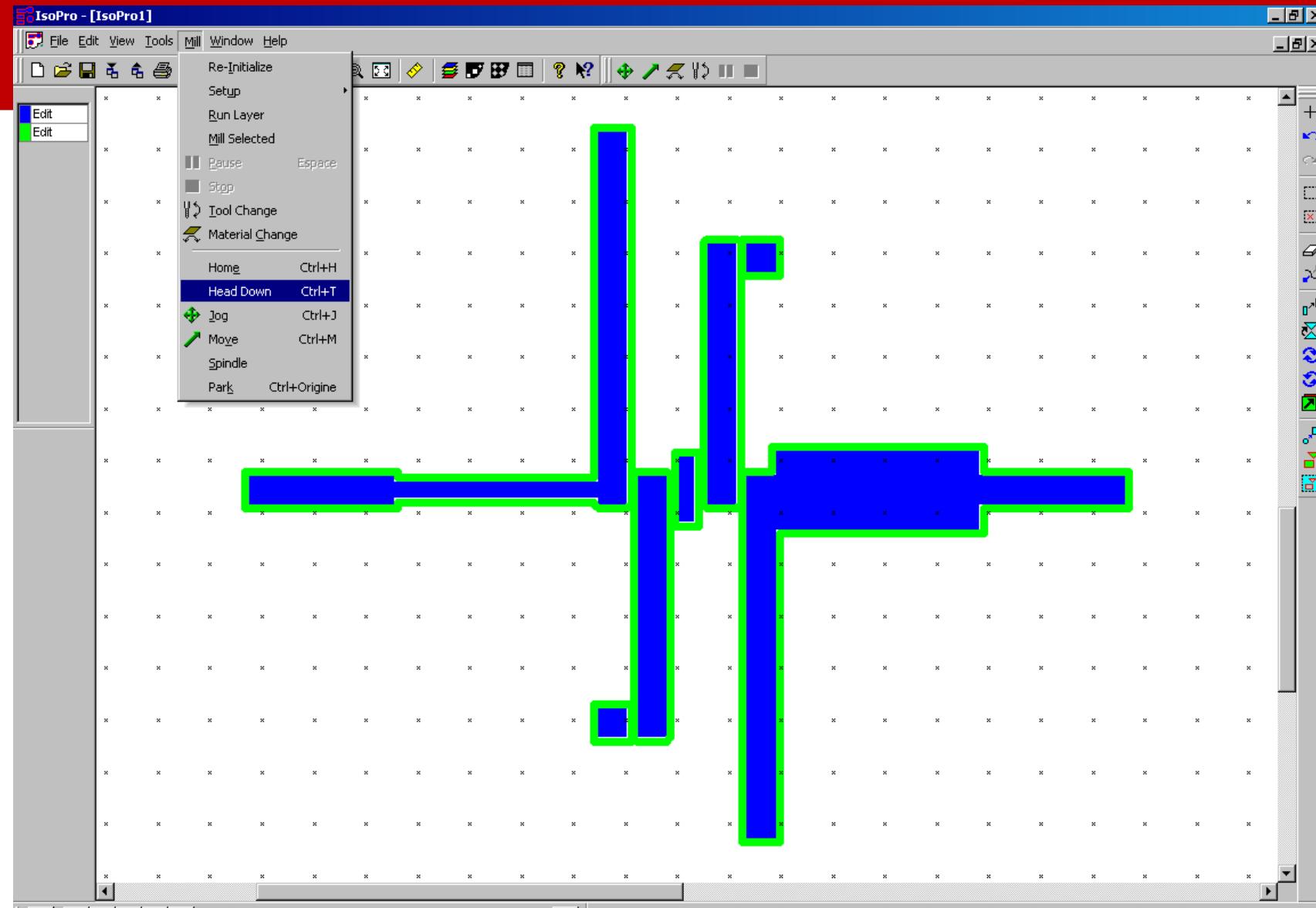
Once the copper layer is removed:

- 1°) move the bench and the solenoid as previously in
 $x = -300$ then $y = -300$
- 2°) when the chuck is out of the table, unscrew the clamping screw and remove the mill. Replace it immediately in its box.
- 3°) Replace the mill with a drill bit (Drill bit) which will allow to make the holes for the ground and screw the tightening screw.
- 4°) adjust the depth of the drill using a plate of FR4 + 2 wedges (20 and 40 μm). Proceed as explained previously for adjusting the depth of the mill.

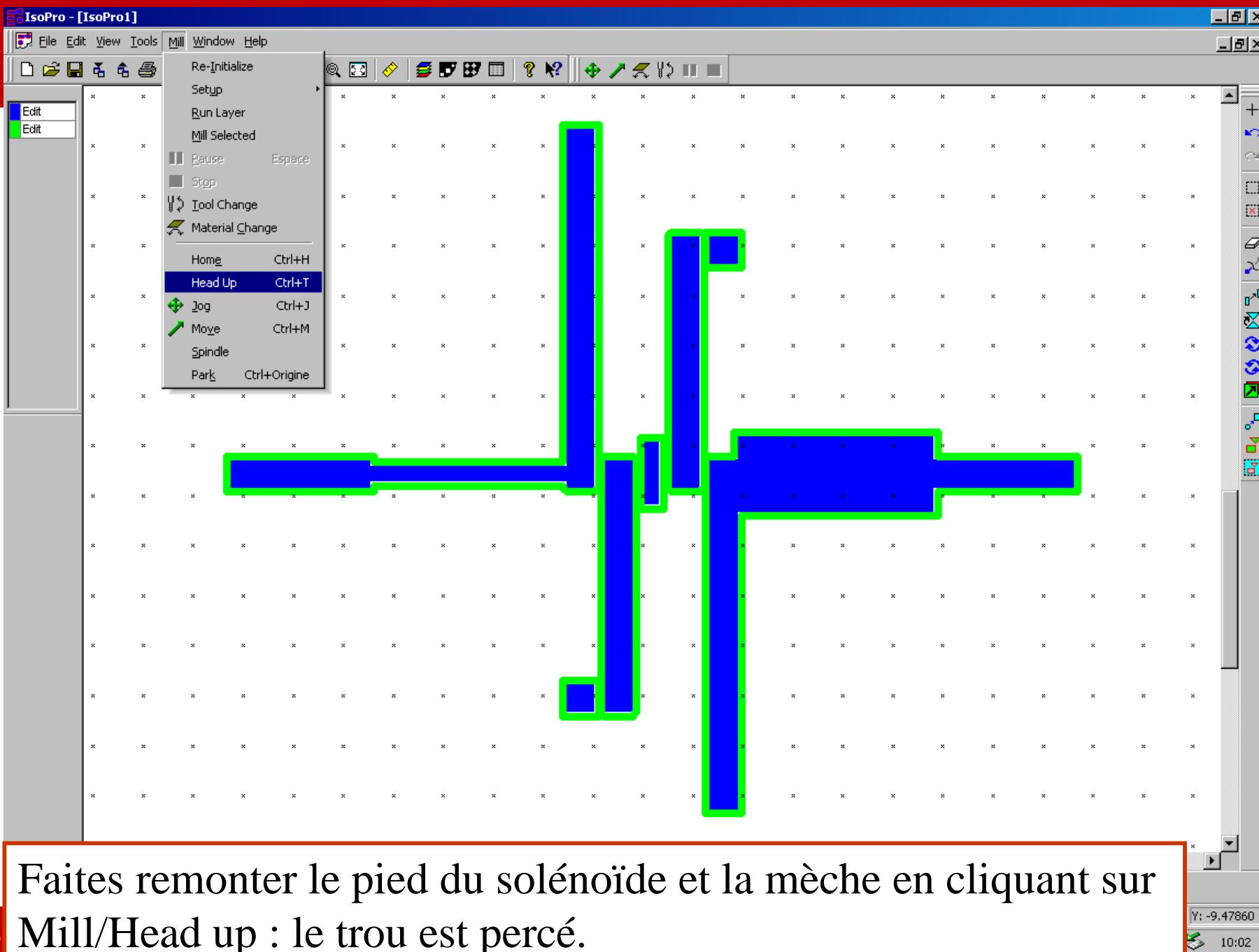
Another solution: you can also use the small drill in the room. In this case, in step 2 simply remove the mill and screw back the clamping screw then go to step 4 of the "Once copper layer removed" slide below



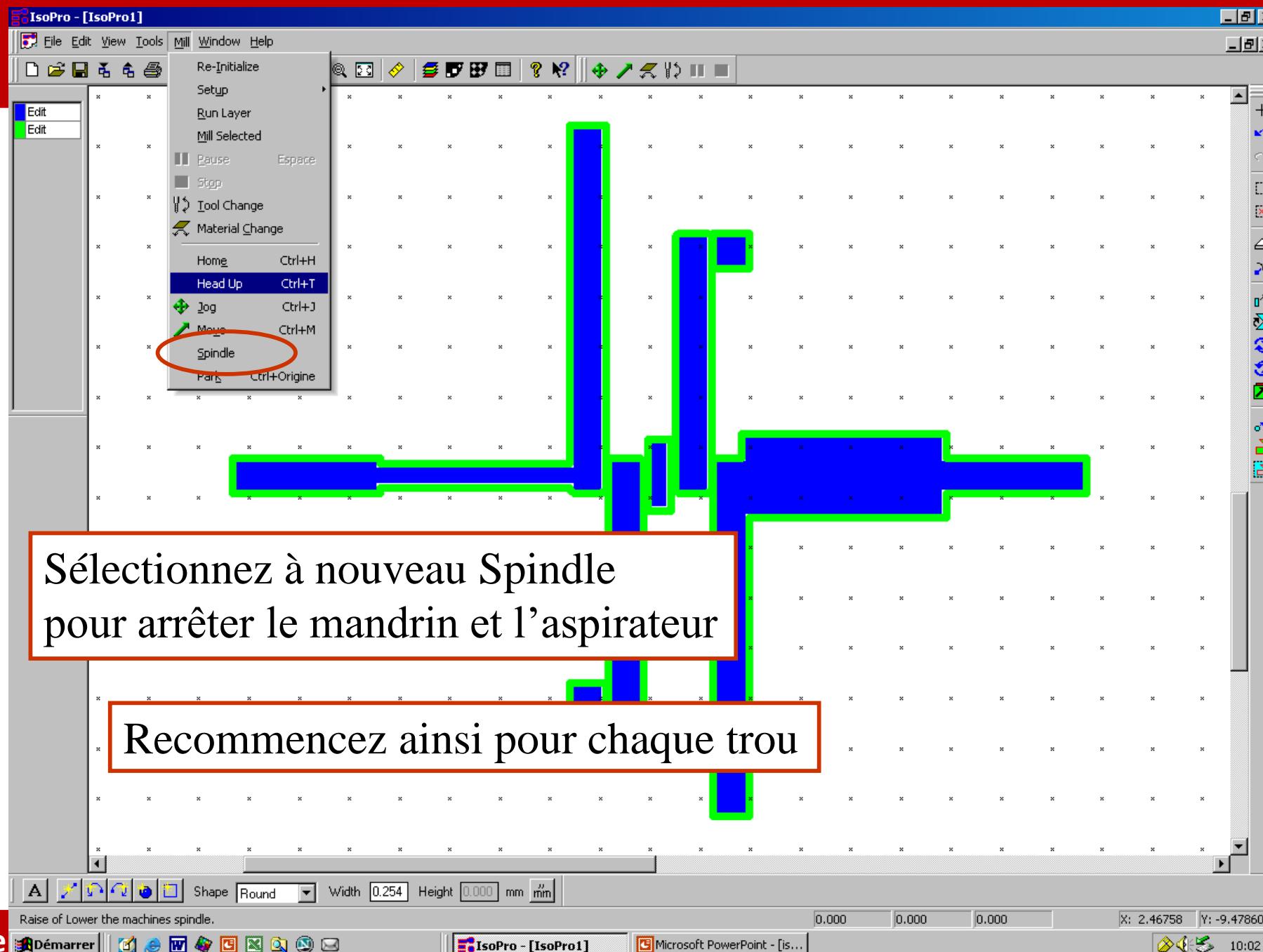




Faites descendre le pied du solénoïde en cliquant sur Mill/Head Down



Faites remonter le pied du solénoïde et la mèche en cliquant sur Mill/Head up : le trou est percé.



Once the copper layer is removed:

- 1°) move the bench and the solenoid as previously in
 $x = -300$ then $y = -300$
- 2°) when the chuck is out of the table, unscrew the clamping screw and remove the drill. Replace it immediately in its box.
- 3°) screw back the clamping screw
- 4°) move the bench and the solenoid as previously in
 $x = +600$.
- 5°) Unplug the vacuum at the back of the bench
- 6°) select Spindle and vacuum the chips on your plate
- 7°) Select Spindle again to stop vacuuming
- 8°) Clean your plate with the "scotch brite"
- 9°) peel off your FR4 plate from the table with a screwdriver
- 10°) Peel off the double-sided tape on the back of the plate and clean it with the "scotch brite"

11°) Look for soldering components: capacitors, transistors, ground wire, power supply wires, connectors

12°) Pass the wires in the ground holes and weld.

13°) Solder the other components.

The PA is complete: you must get:

