Basics of Active and Nonlinear High-Frequency Electronics

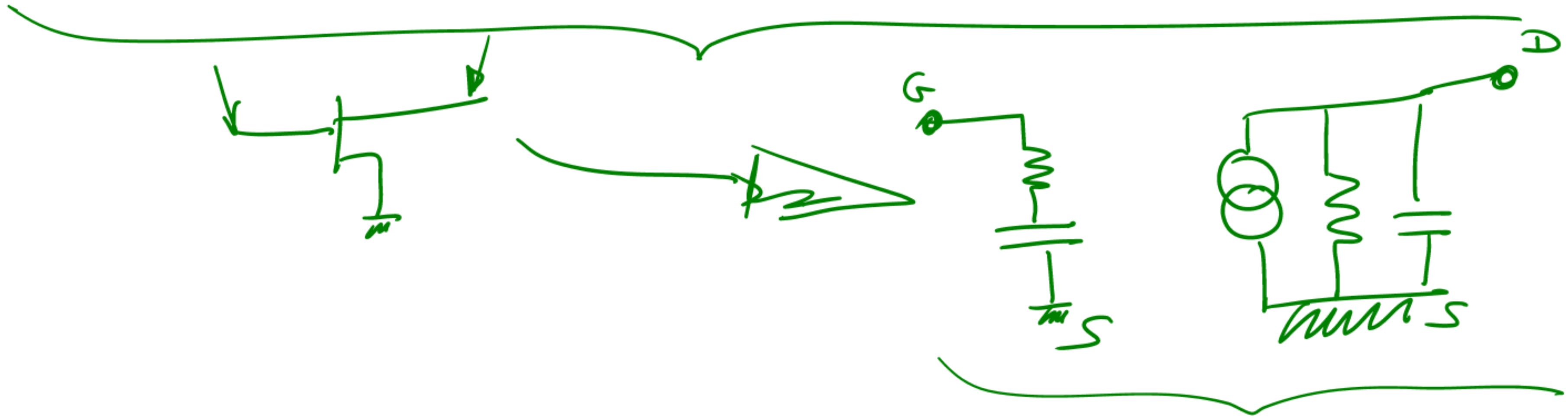
Basics of Active and Nonlinear High-Frequency Electronics

- Chapter I : Introduction to active high-frequency circuits in communication systems
- Chapter II : Introduction to the Non-linear Electrical Modeling of microwave transistors
- Chapter III : Design method of narrow-band power amplifiers
- Chapter IV : Architectures of high-frequency mixers
- Chapter V : Architectures of wideband resistive and distributed power amplifiers
- Chapter VI : Architectures of non-linear active circuits controlled by cold HEMTs

Chapter II :

Introduction to

the Non-linear Electrical Modeling of microwave transistors

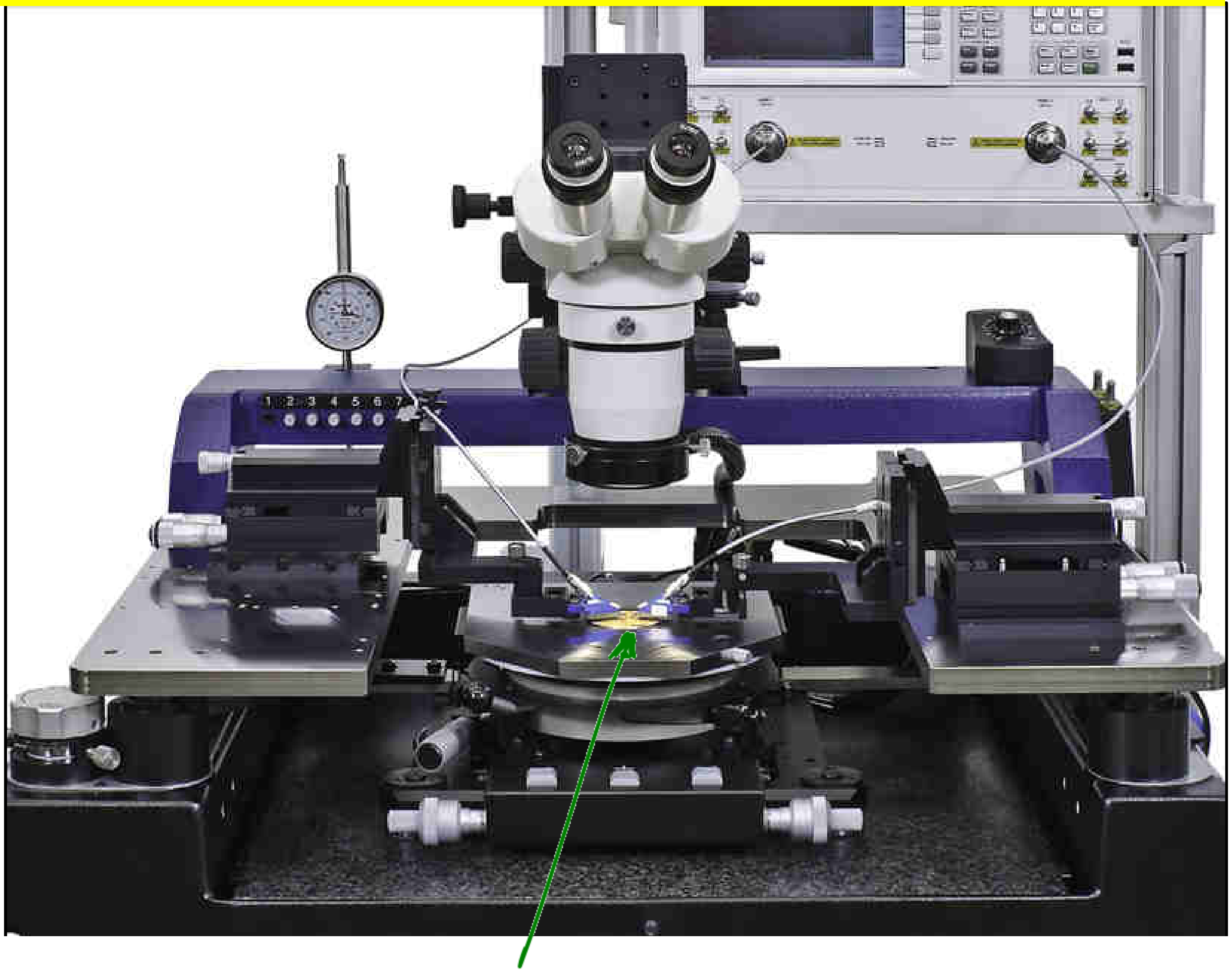


High-frequency Pulsed Measurement Systems

On–wafer Probing Stations

for RF/Microwave circuits

On-wafer probing stations



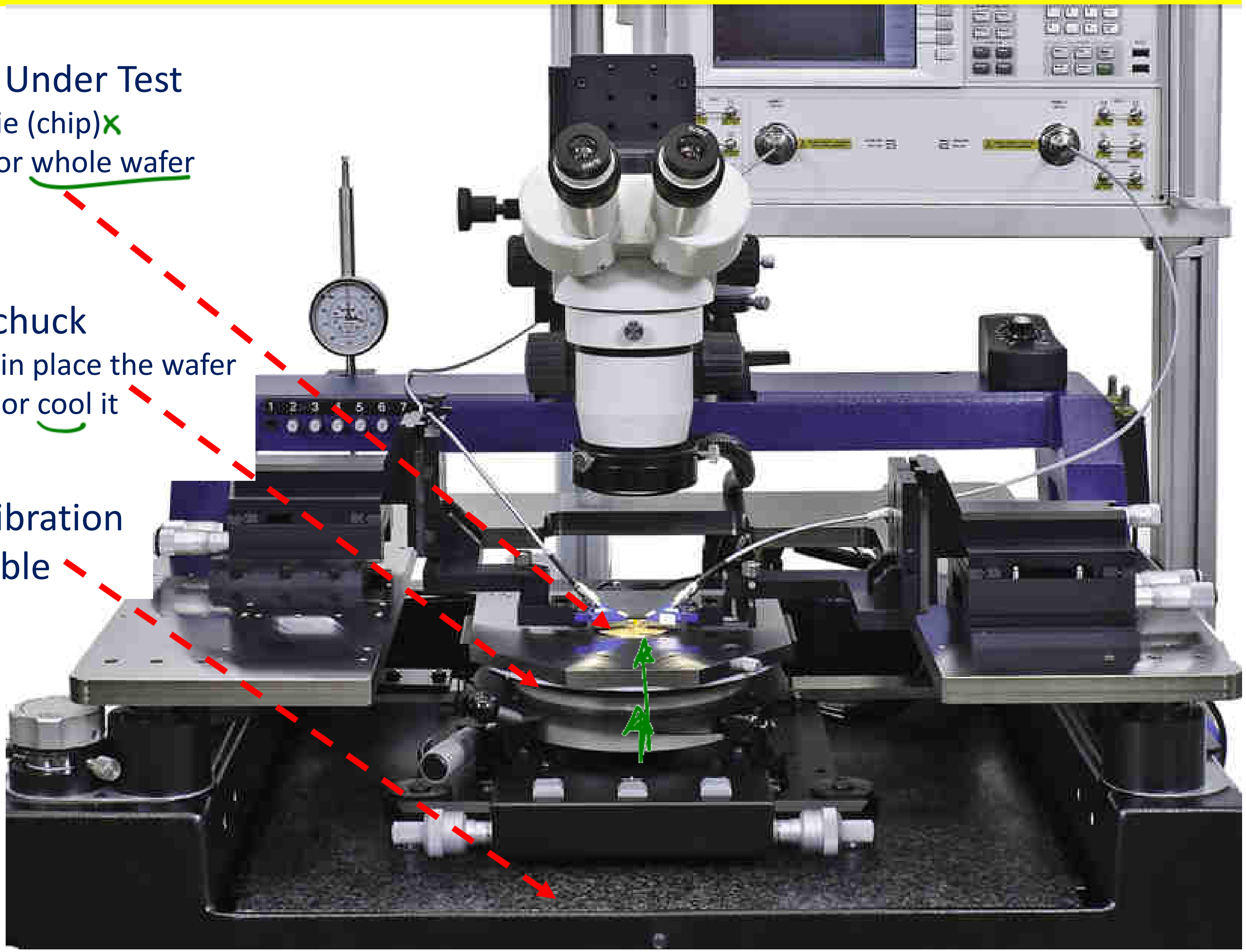
On-wafer probing stations

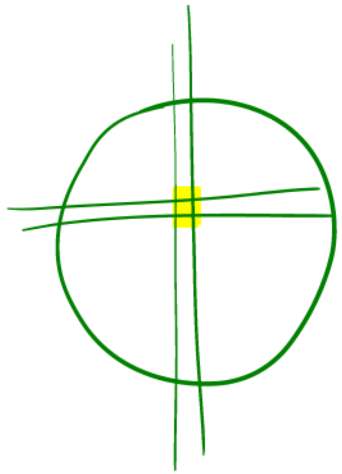
DUT

Device Under Test
- small die (chip)x
- partial or whole wafer

Wafer chuck
- to hold in place the wafer
- to heat or cool it

Anti- Vibration Table



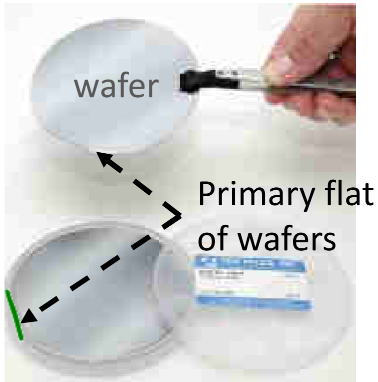


Thales Alenia Space

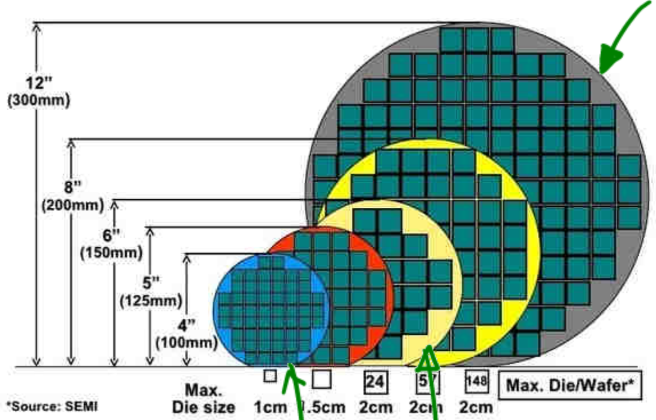
ESA

400 k€ "wafer run"

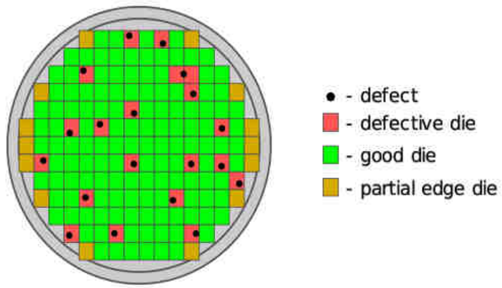
Wafer chuck and Anti-vibration table



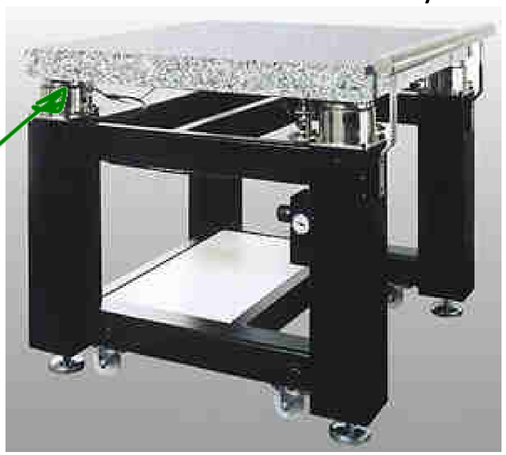
On-wafer size



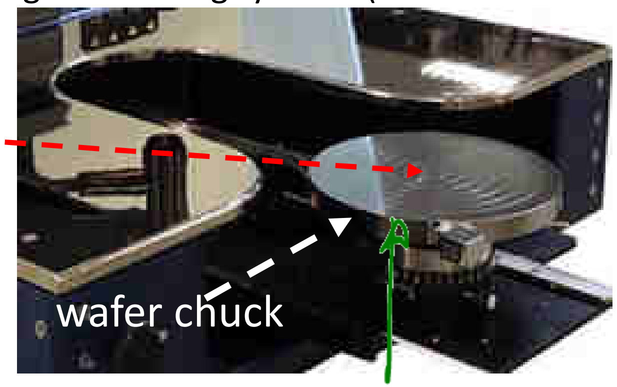
On-wafer test and sorting



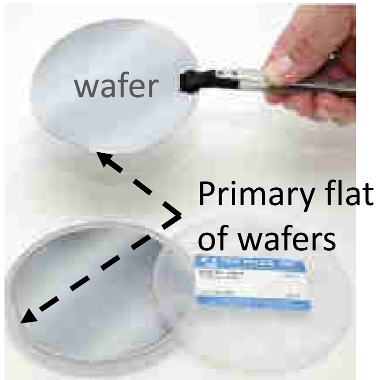
Vibration Isolation Table (Marble)
- keep high mechanical stability
- reliable sub-micron stability



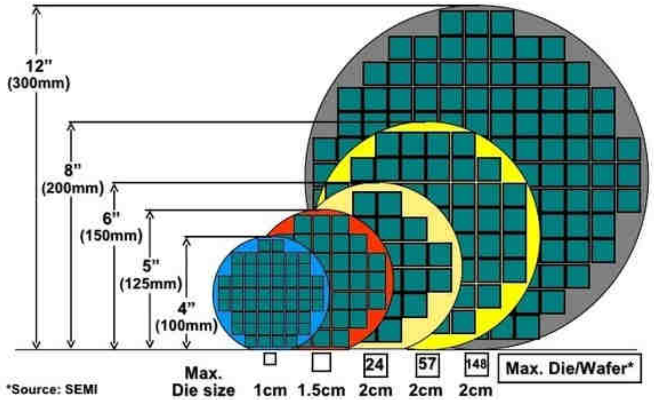
Wafer Chuck → Thermal chuck (-60°C → 300°C)
Thermal enclosure
- hold wafers in place while they are being probed
- apply a small amount of vacuum to the wafer backside
- can hold small die and partial or whole wafer
- cooling and heating systems (air flow conditioning)



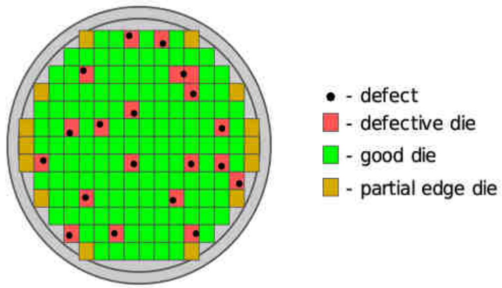
Wafer composition



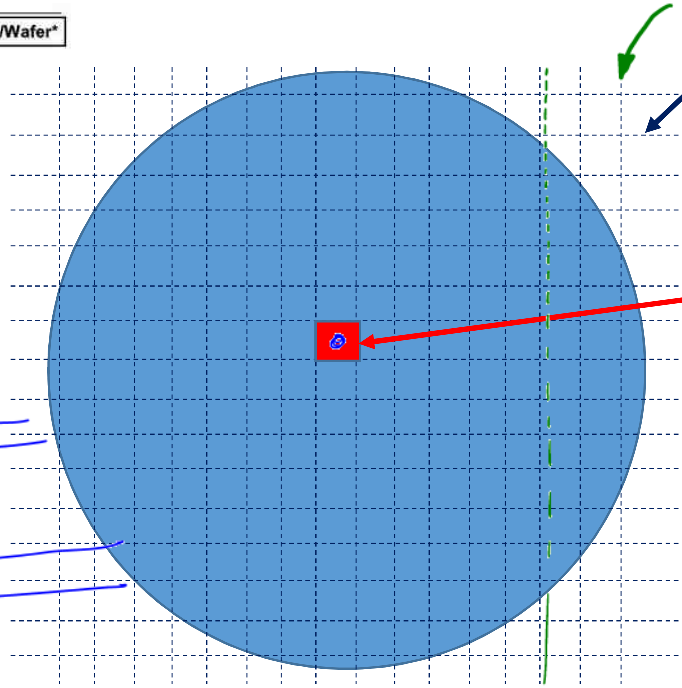
On-wafer size



On-wafer test and sorting

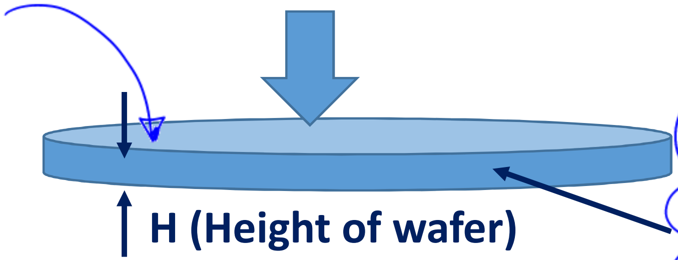


Dicing streets



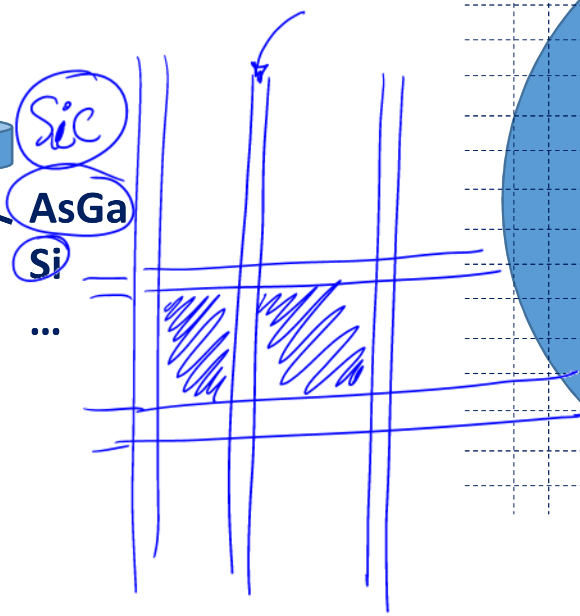
Chip (die)

Front side of the wafer

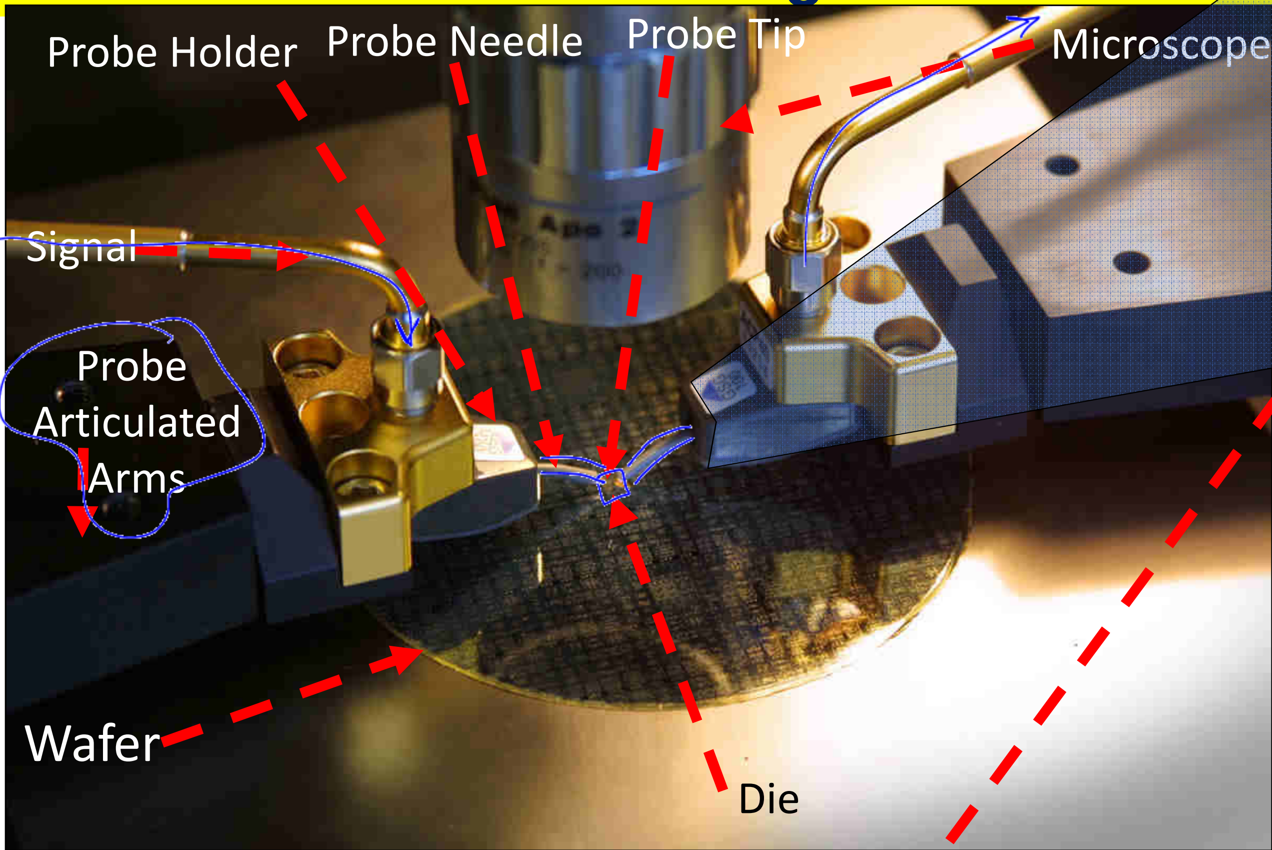


H (Height of wafer)
Example 100-200µm)

Backside of the wafer

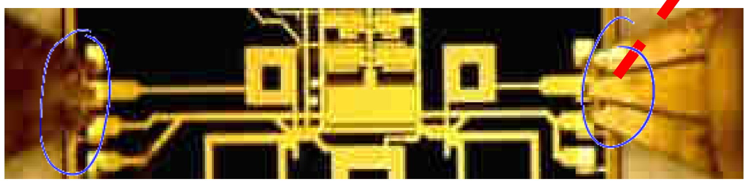


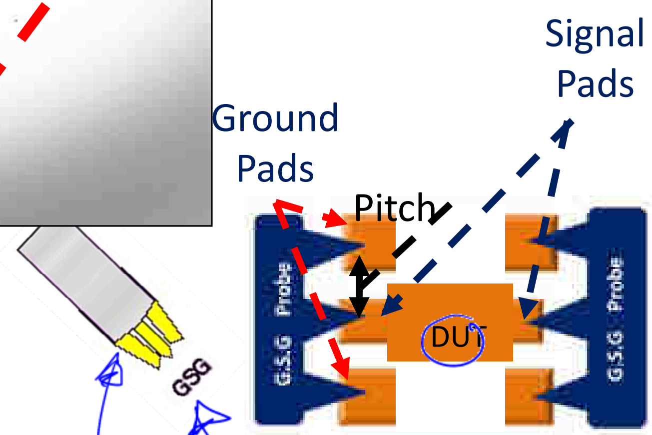
On-Wafer Probing



GSG
Probe Tip

GSG is the most common type of RF probe.
Many standard pitches

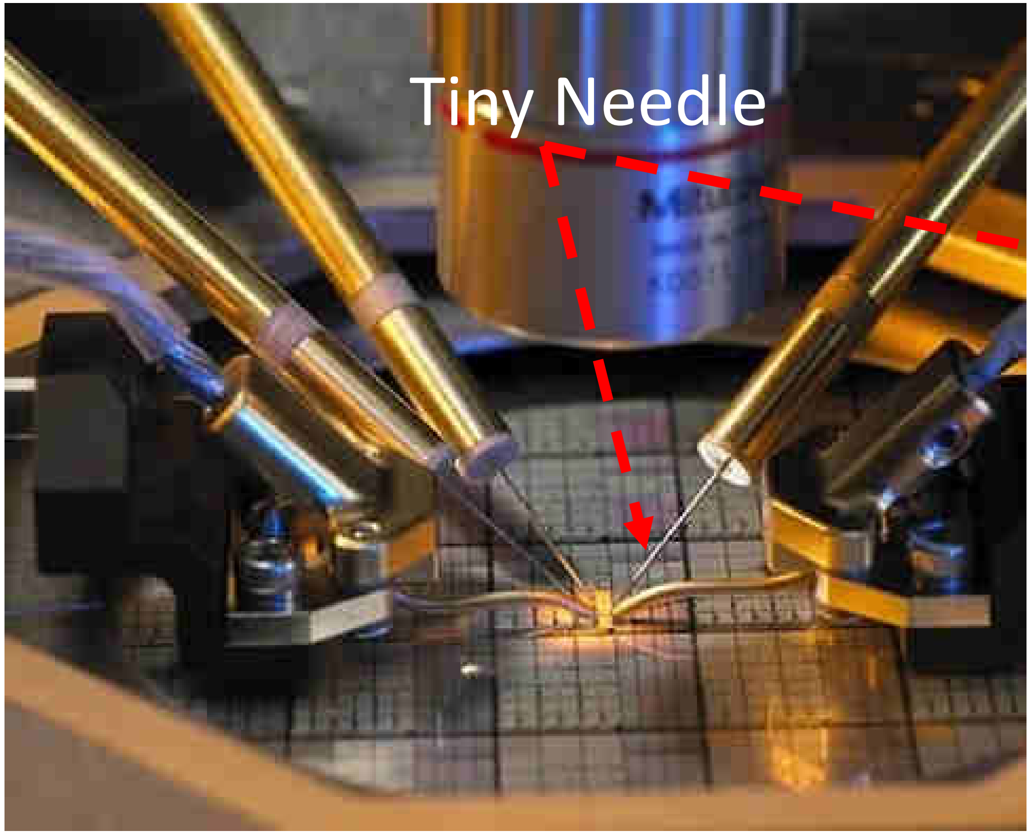


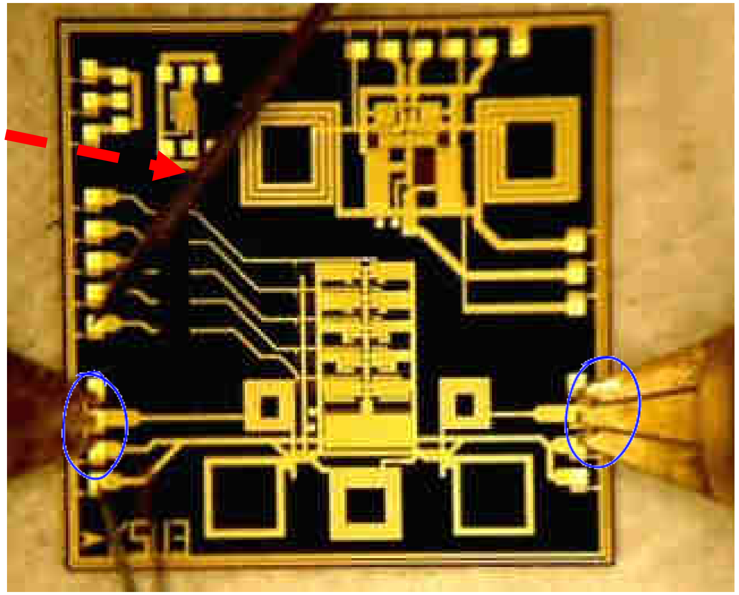


G
S
G

GSG probes

On-Wafer Probing

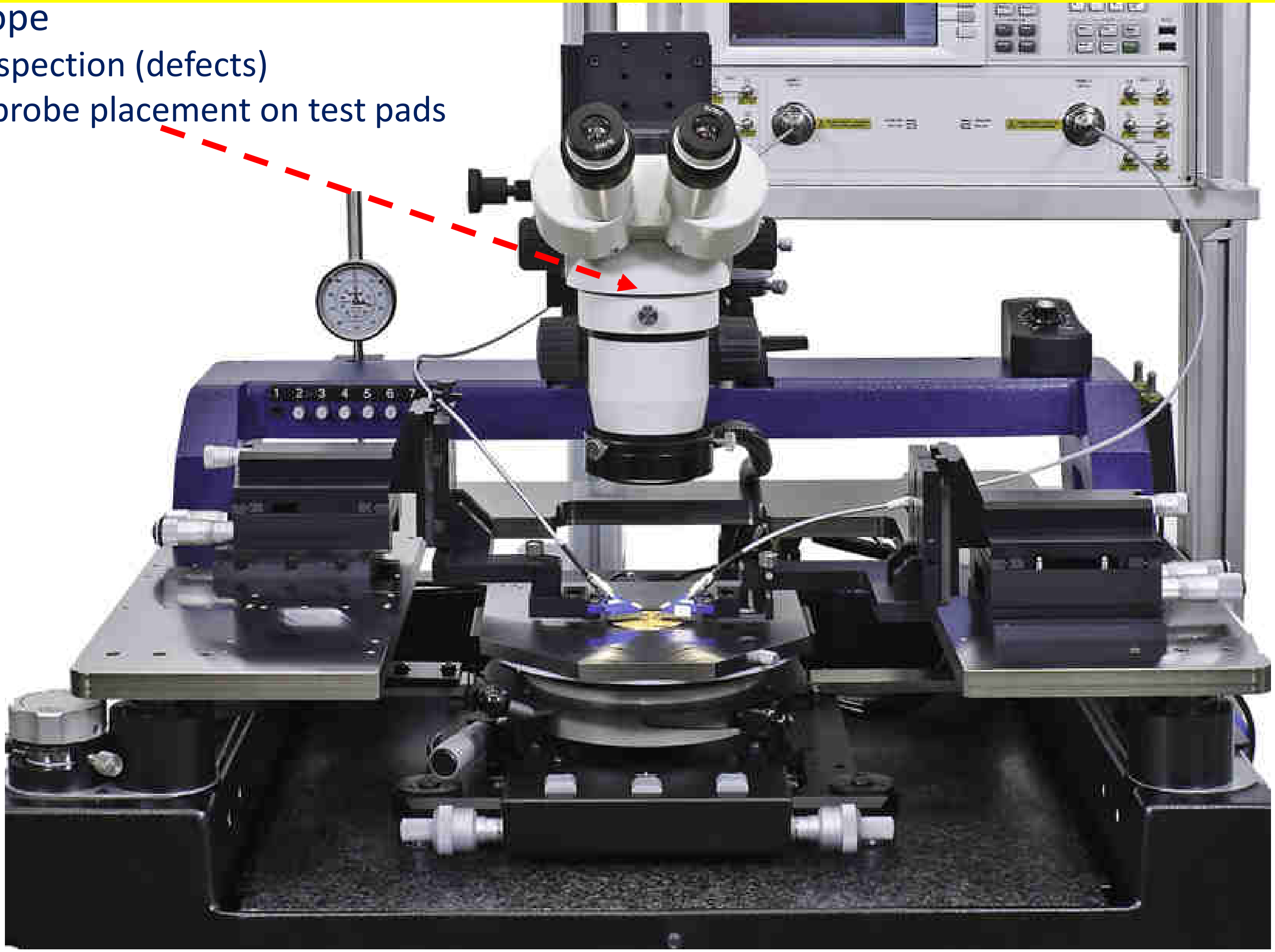




HF probe stations   On-wafer Probing System

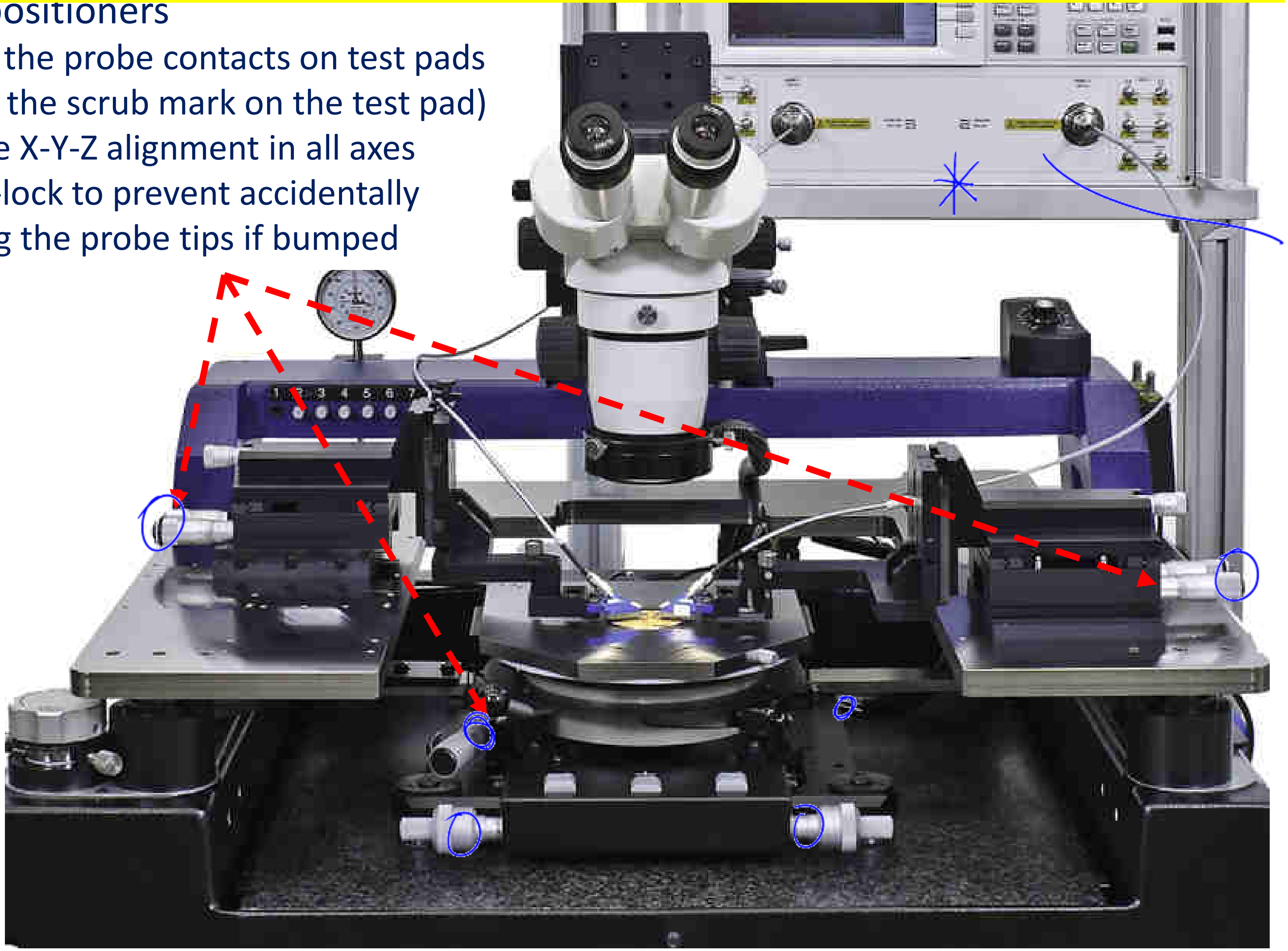
Microscope

- wafer inspection (defects)
- precise probe placement on test pads



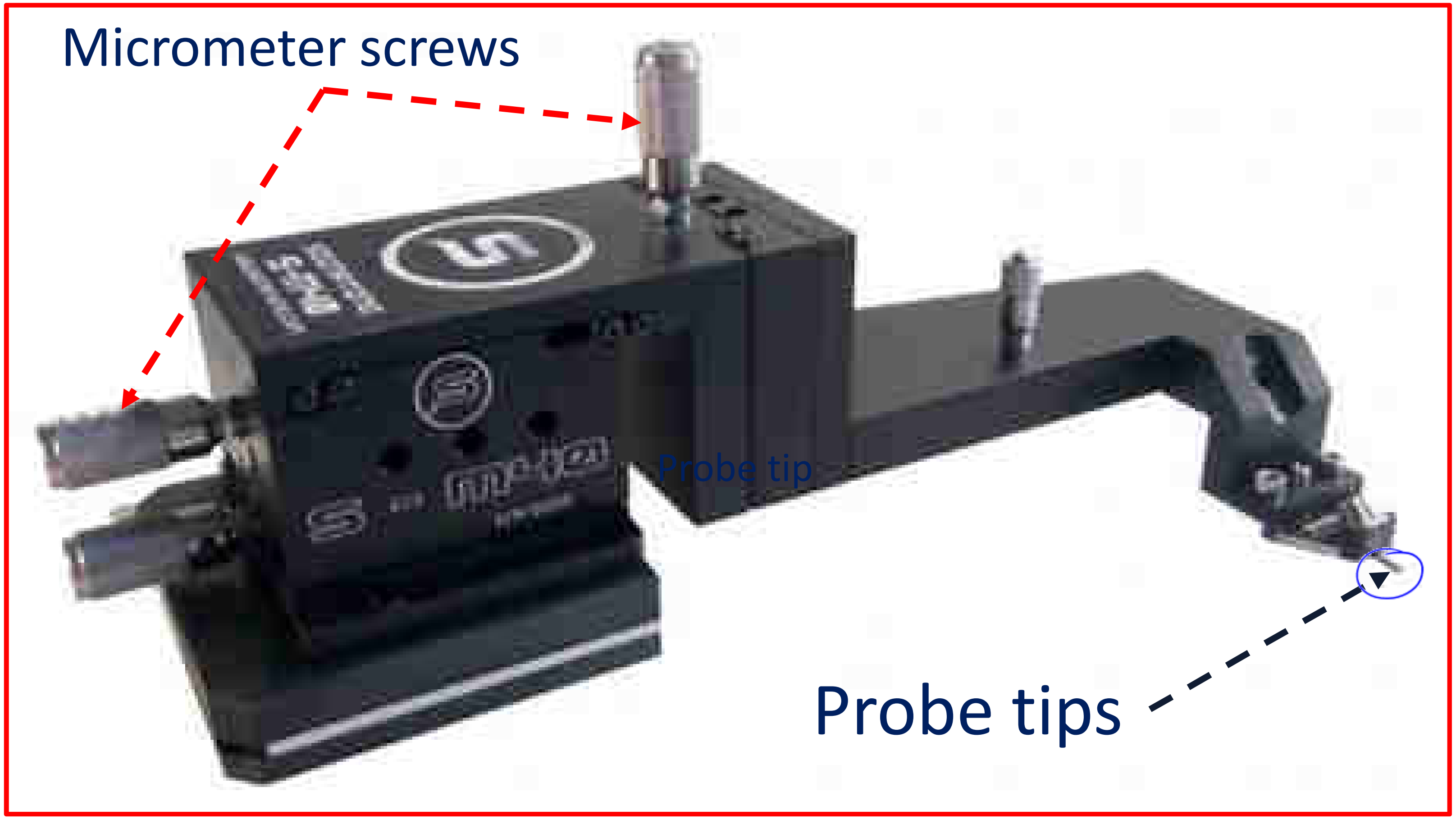
HF probe stations On-wafer Probing System

Micropositioners
- adjust the probe contacts on test pads
  (check the scrub mark on the test pad)
- precise X-Y-Z alignment in all axes
- screw-lock to prevent accidentally
  moving the probe tips if bumped



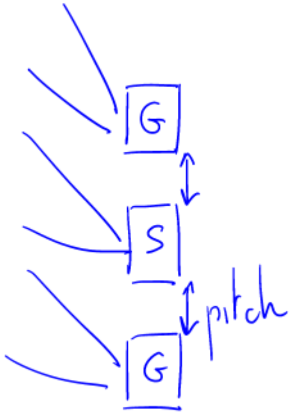
measurement
equipment

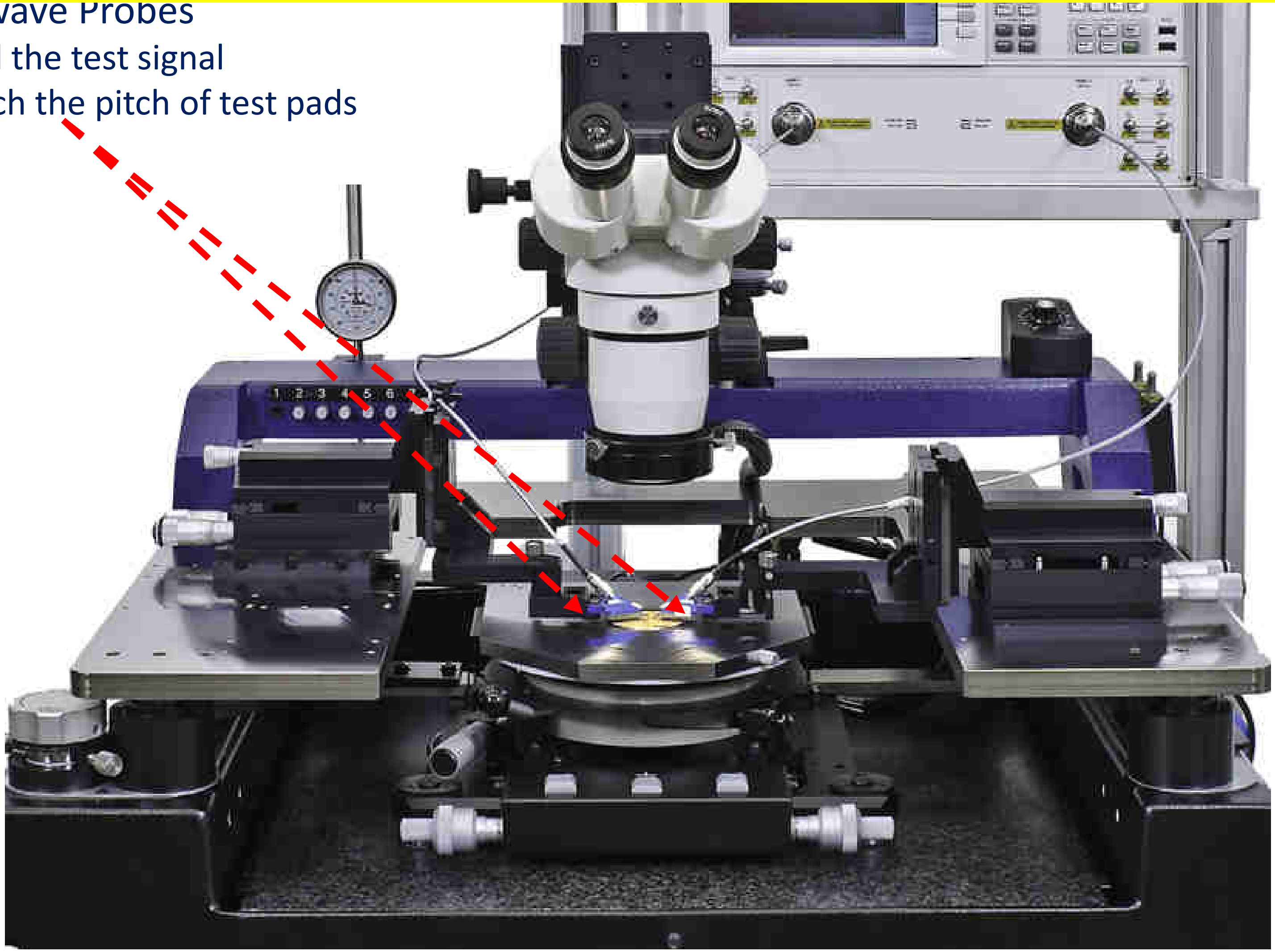
Micropositioner of probe tips



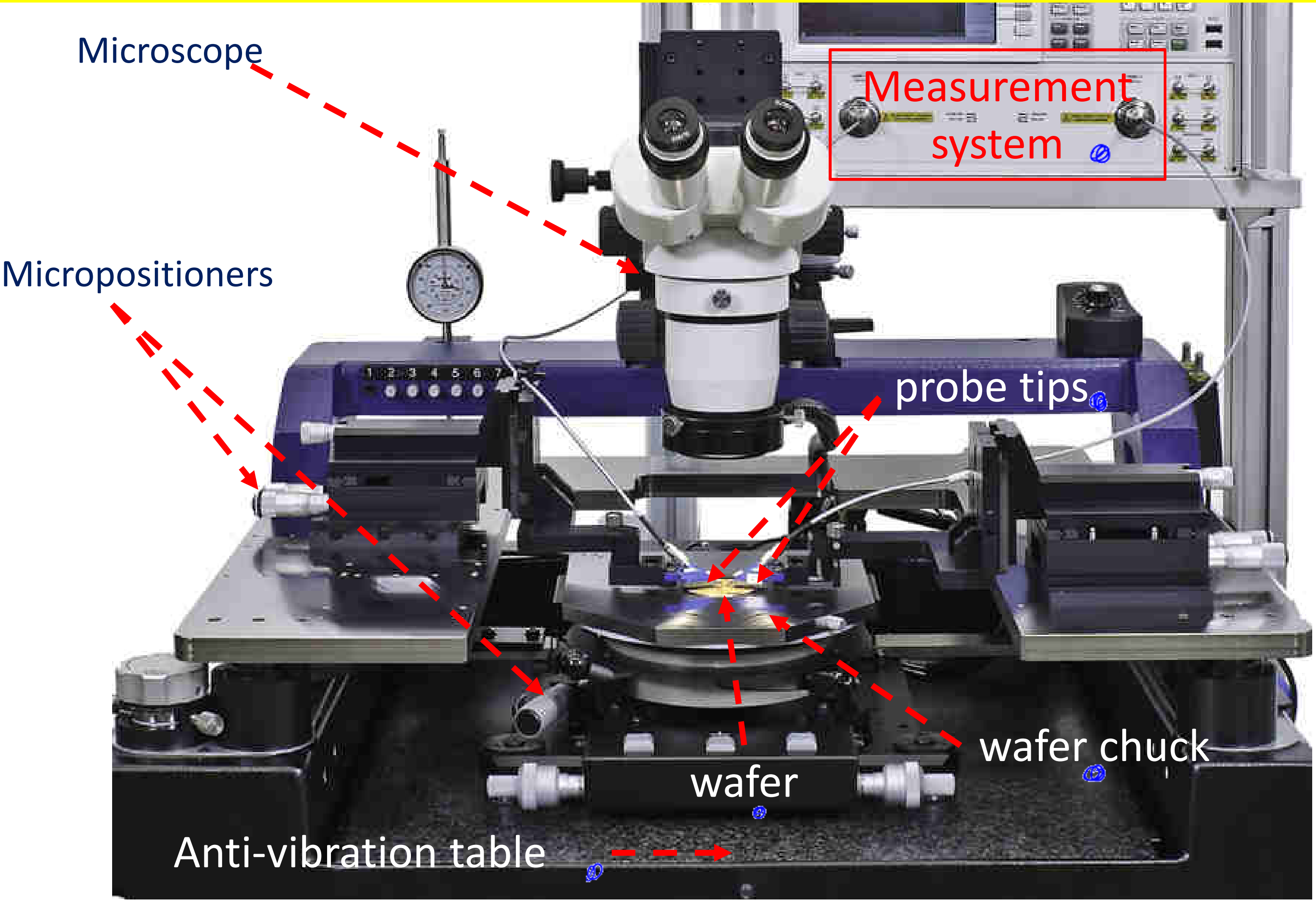
HF probe stations On-wafer Probing System

Microwave Probes
- Feed the test signal
- Match the pitch of test pads





HF probe stations On-wafer Probing System



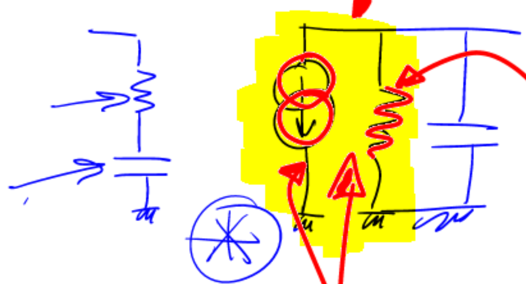
I – Basics of MESFET operation

HEMT ⇒ Same model topology.

- Low-Frequency Bipolar transistors are based on the well-known PN Junction (P-type-SC / N-type-SC)

- High-Frequency MESFET (MEtal Semiconductor Field Effect Transistor) based on Schottky Junction (Metal / N-type-SC)

HEMT



→ Simplified planar representation of FETs

→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)

→ Localization of electrical equivalent elements that gives the nonlinear electrical model

→ Successive simplification to derive the simplified linear electrical FET model

→ Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point

ohmic contact

wire ($r=0$)

slope $= \frac{1}{r}$

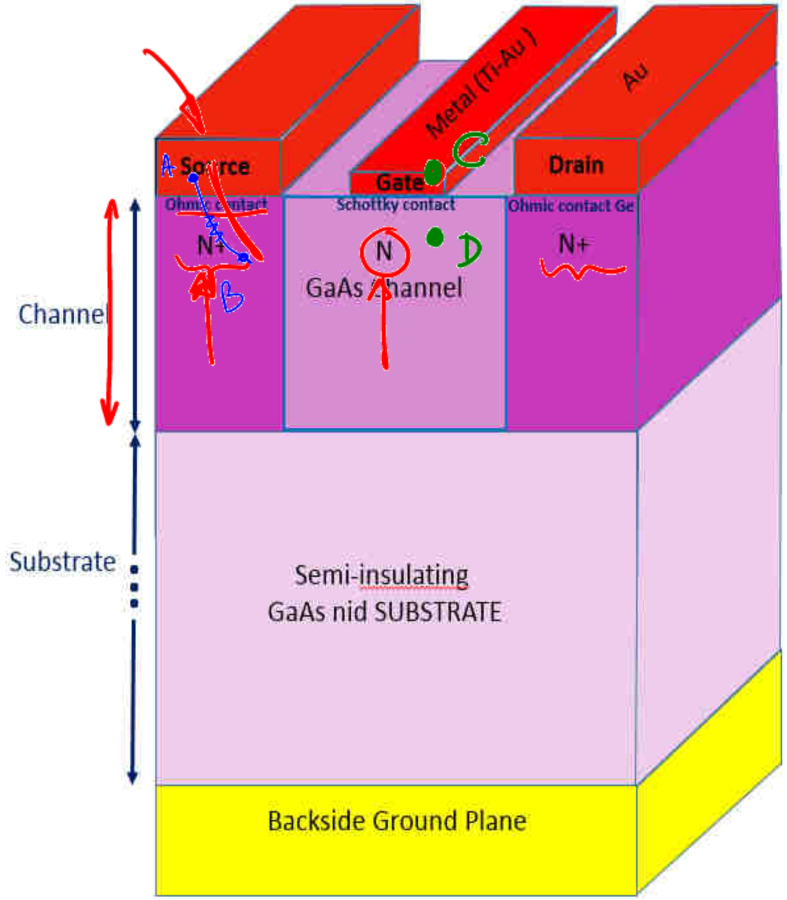
$(V_B - V_A)$

shottky

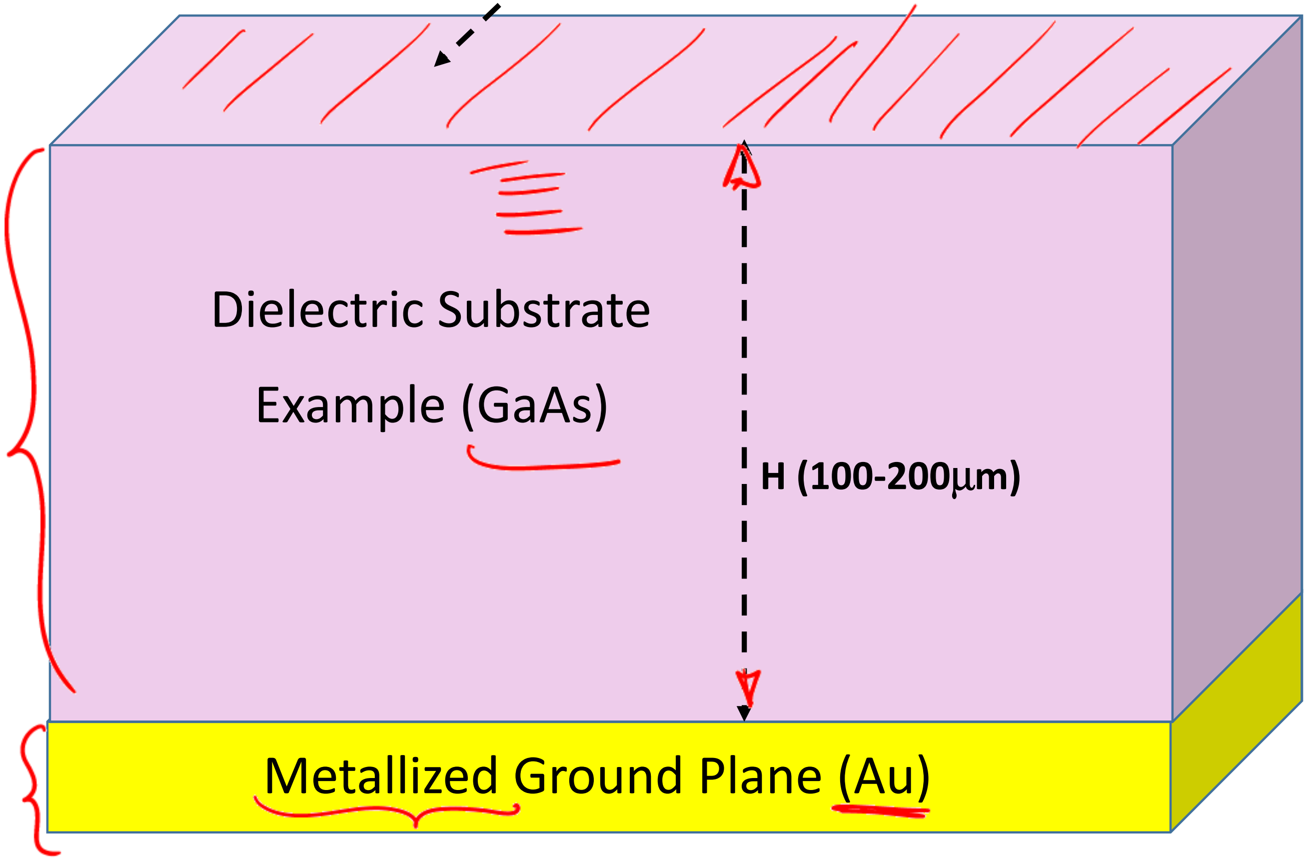
$V_c - V_D$

I – Basics of MESFET operation

→ Simplified planar representation of FETs (Depletion Mode)



Front Side of the wafer where active and passive elements are placed



Operating principles (FET / HEMT)

- **FET** → Gate voltage controls the flow of drain current by modifying the available section W of the doped channel (Impureties, Ionized scattering → Low mobility)

Schottky Junction (Metal / SC_N channel) in reverse mode I_{DS} S D e^-
G

- **HEMT** → Gate voltage controls the flow of drain Current by modifying the carrier density n_S of a 2DEG in the undoped channel (no impureties → Very high mobility)

The (two-dimensional Electron Gas) **2DEG** is located at the **heterojunction** between a **wide bandgap semi-conductor (AlGaN)** and a **narrow bandgap semi-conductor (GaN).**

The electrons of the 2 DEG are free to move in a two-dimensional plane (x,z) but tightly confined in the 3rd dimension (y) because they are trapped in a potential well created at the heterojunction surface

heterostructure (Wide bandgap SC / Narrow bandgap SC)

I – Basics of MESFET operation

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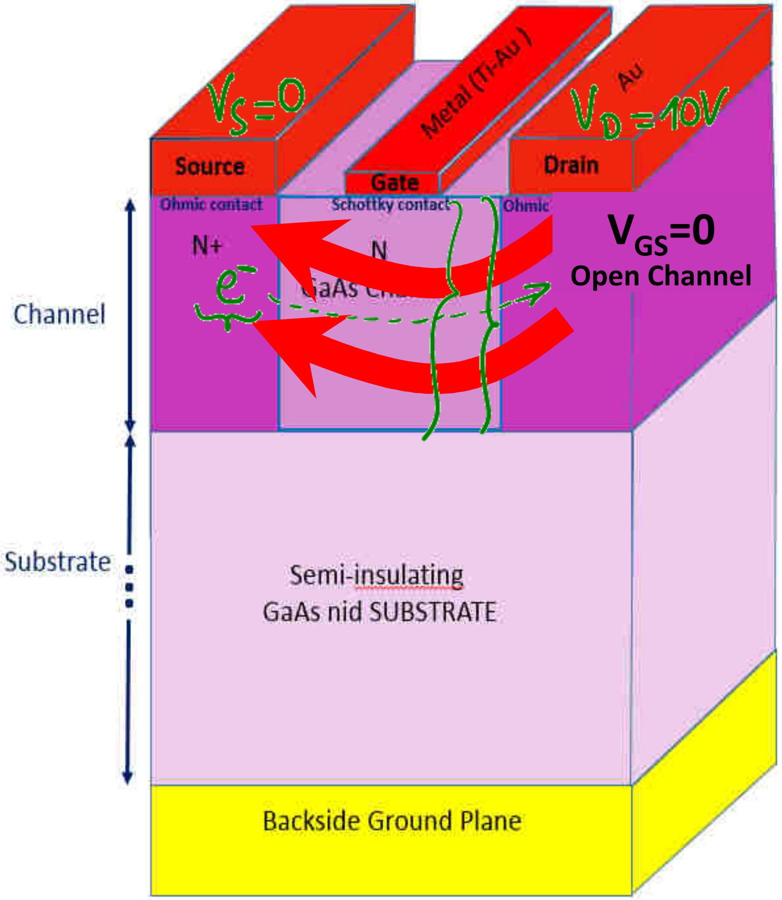
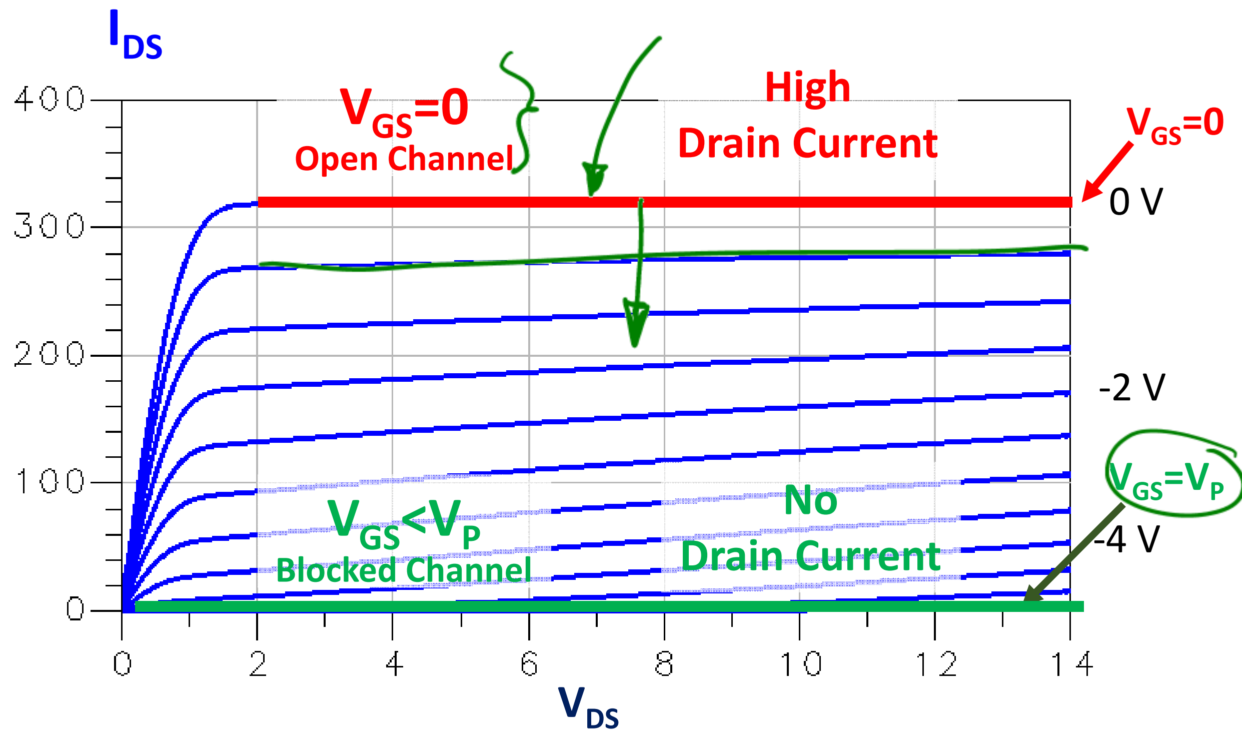
→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)





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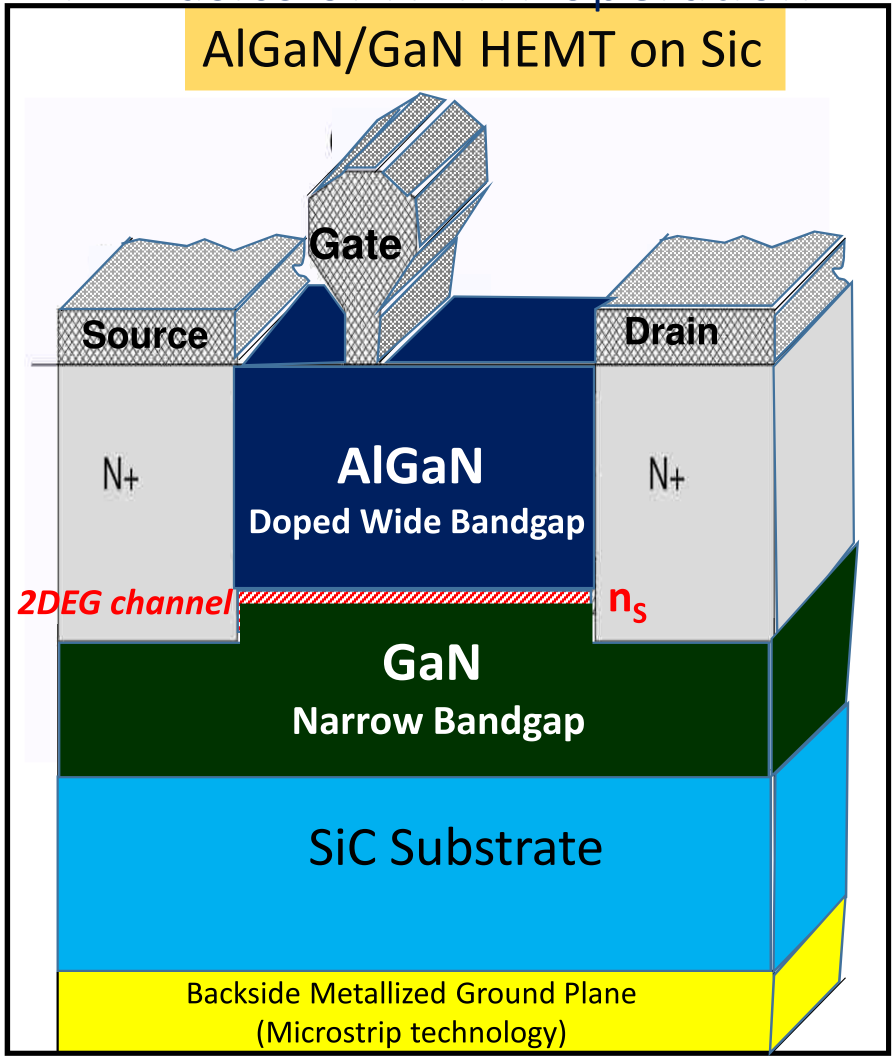
I – Basics of HEMT operation → Same Electrical Circuit Model than FET



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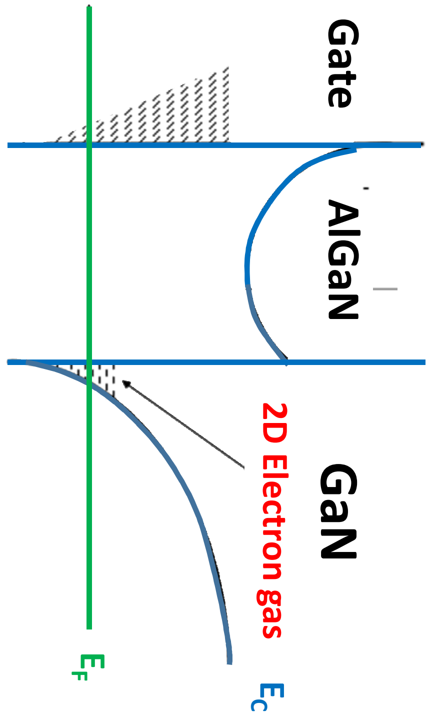

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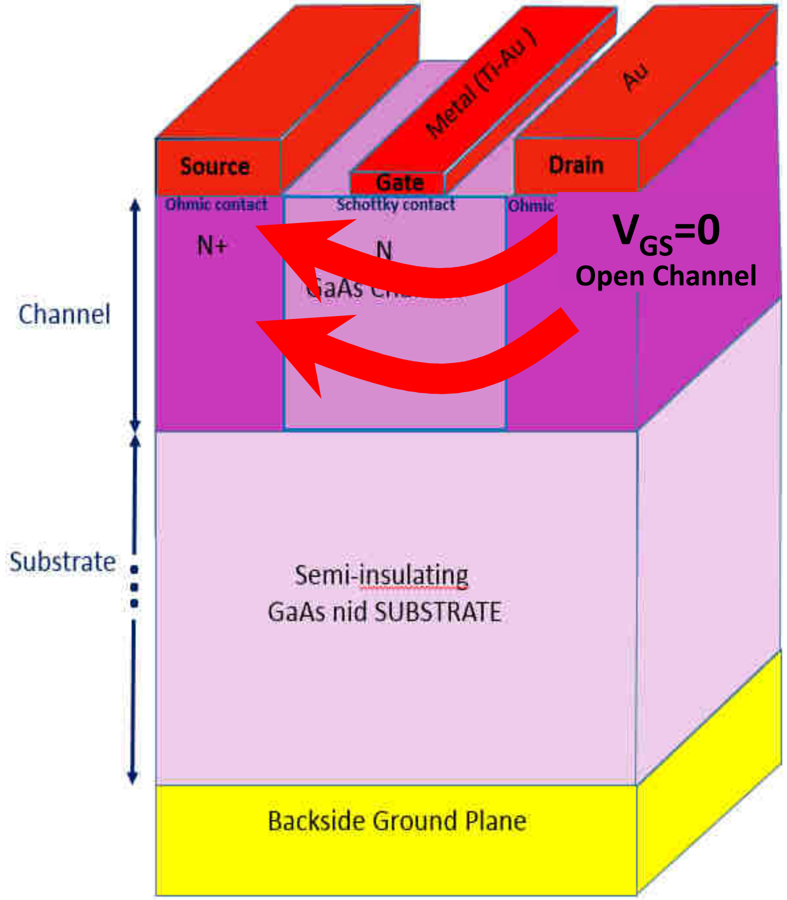
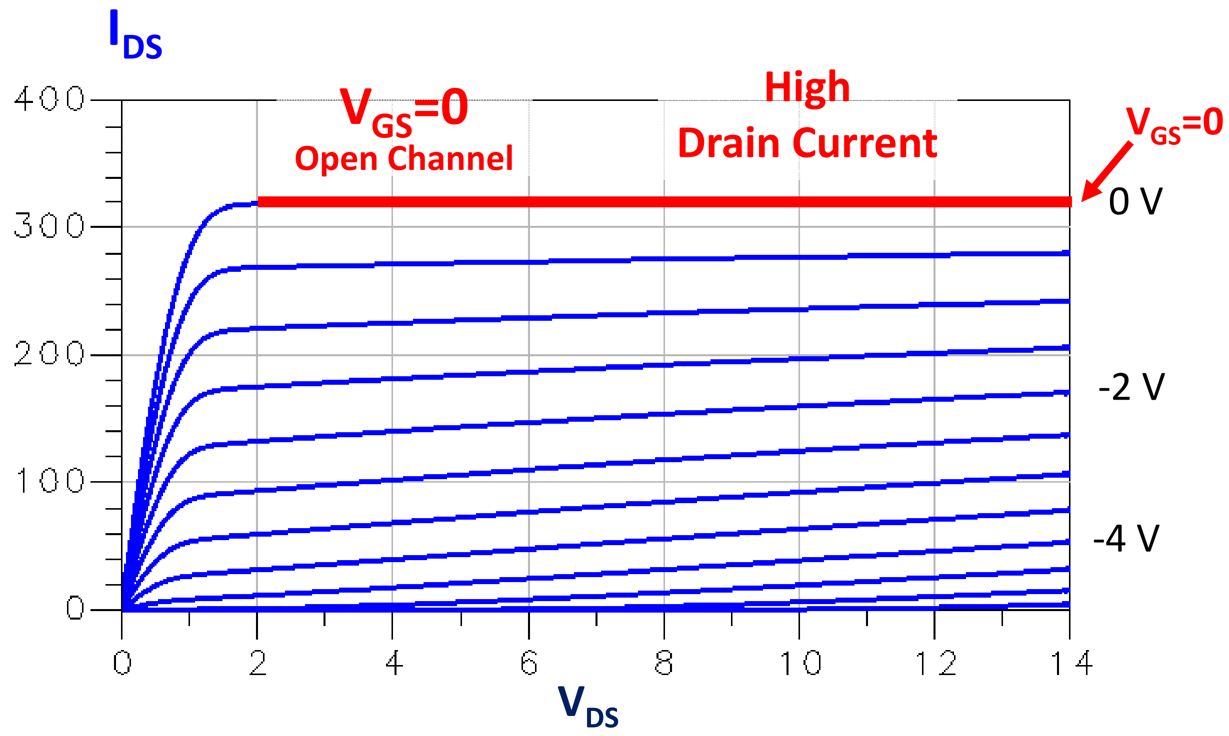
I – Basics of MESFET operation

FET → Gate voltage controls the flow of drain current by modifying the available section W of the doped channel (Impureties, Ionized scattering → Low mobility)

→ I-V transfer characteristic (Ohmic & Saturated regions, Diode conduction, Breakdown & Pinch-off voltages)





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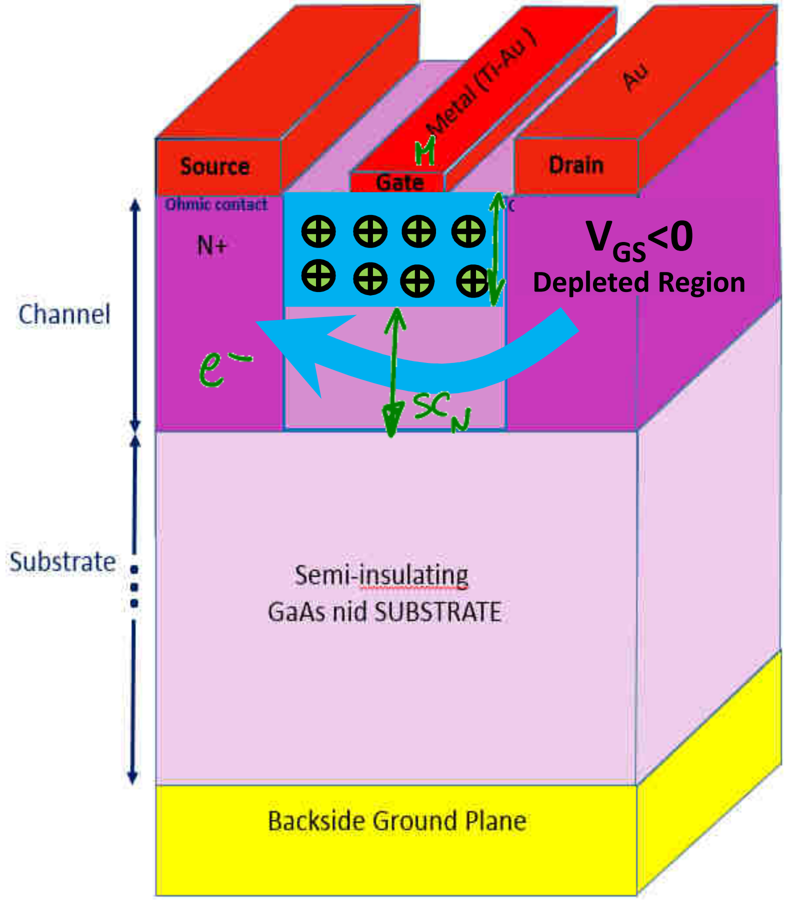

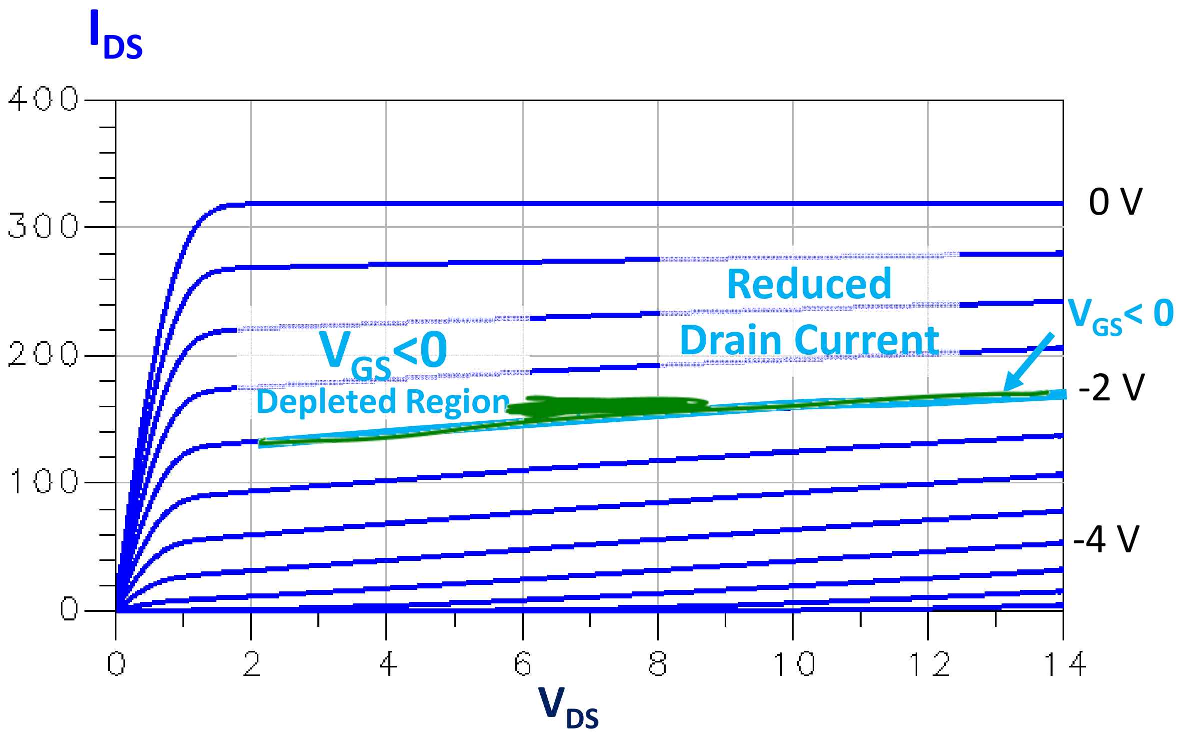

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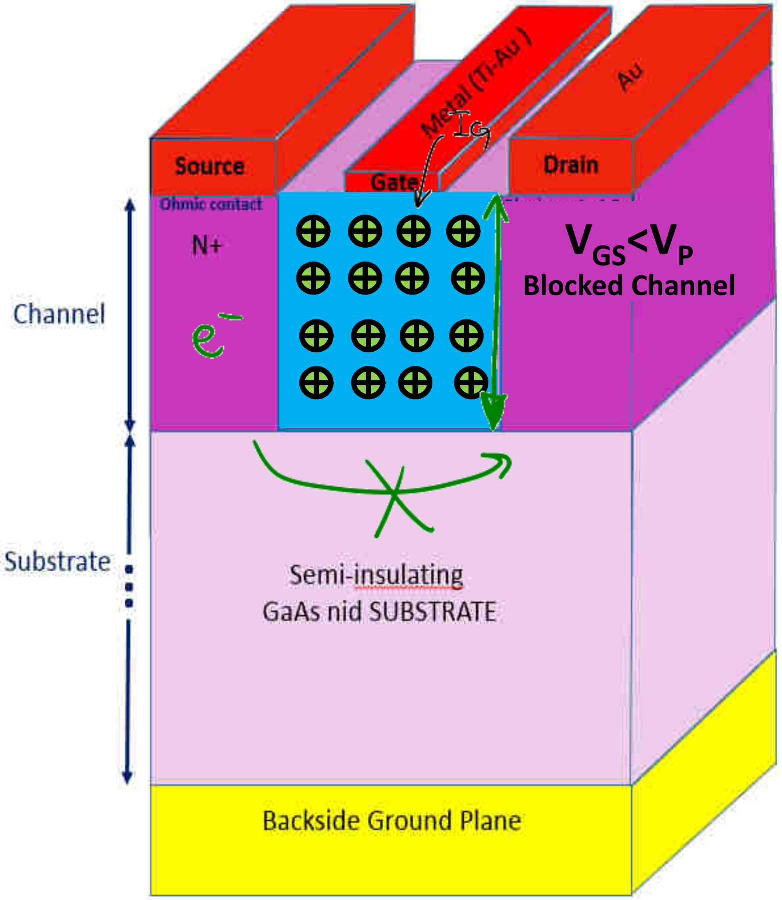
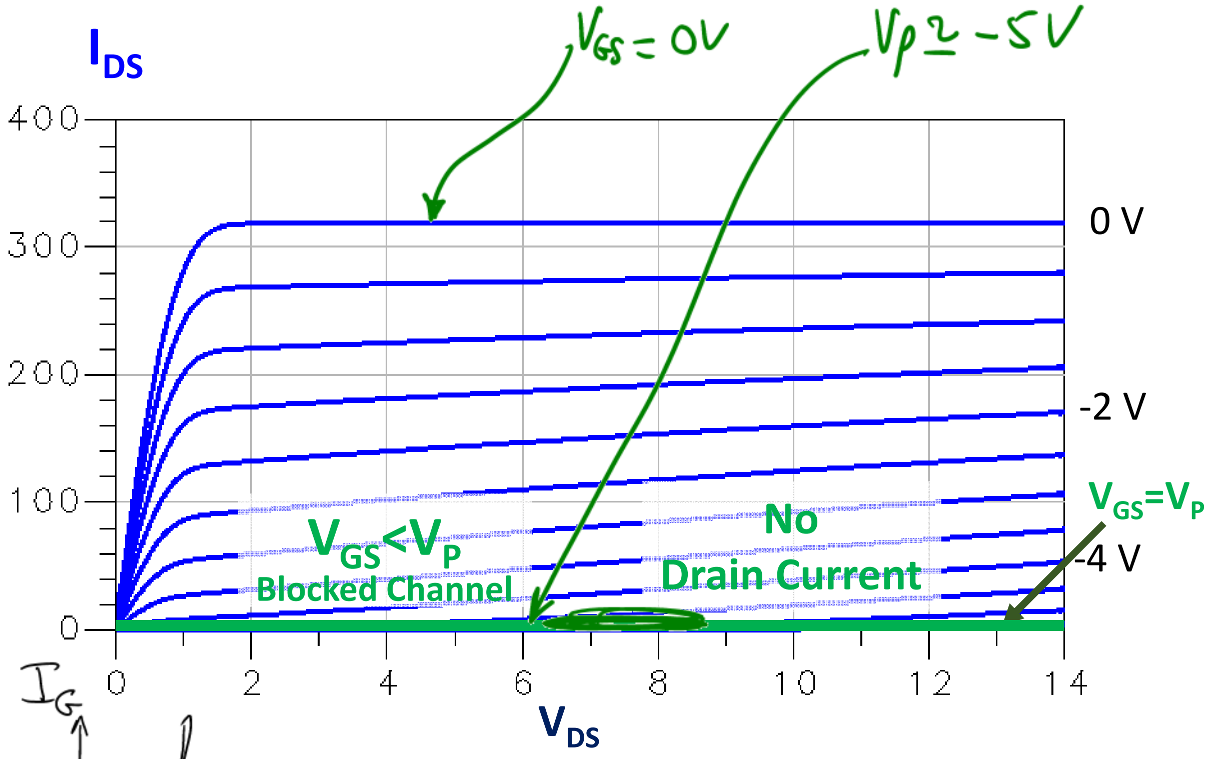
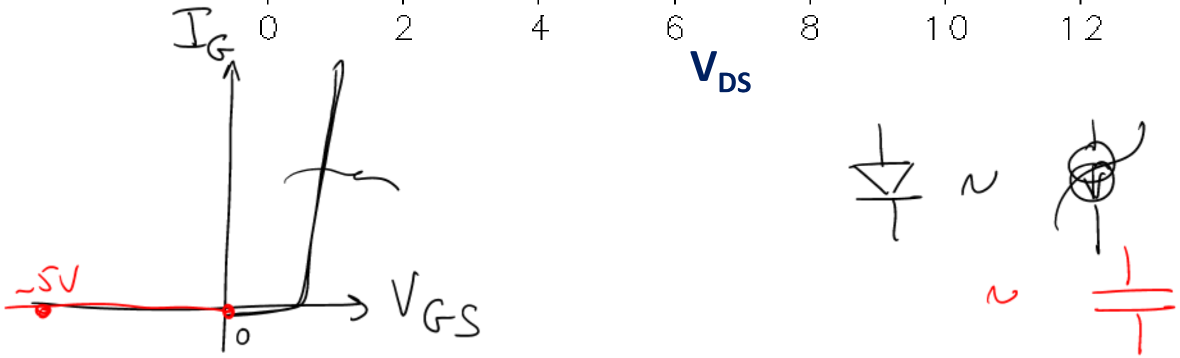


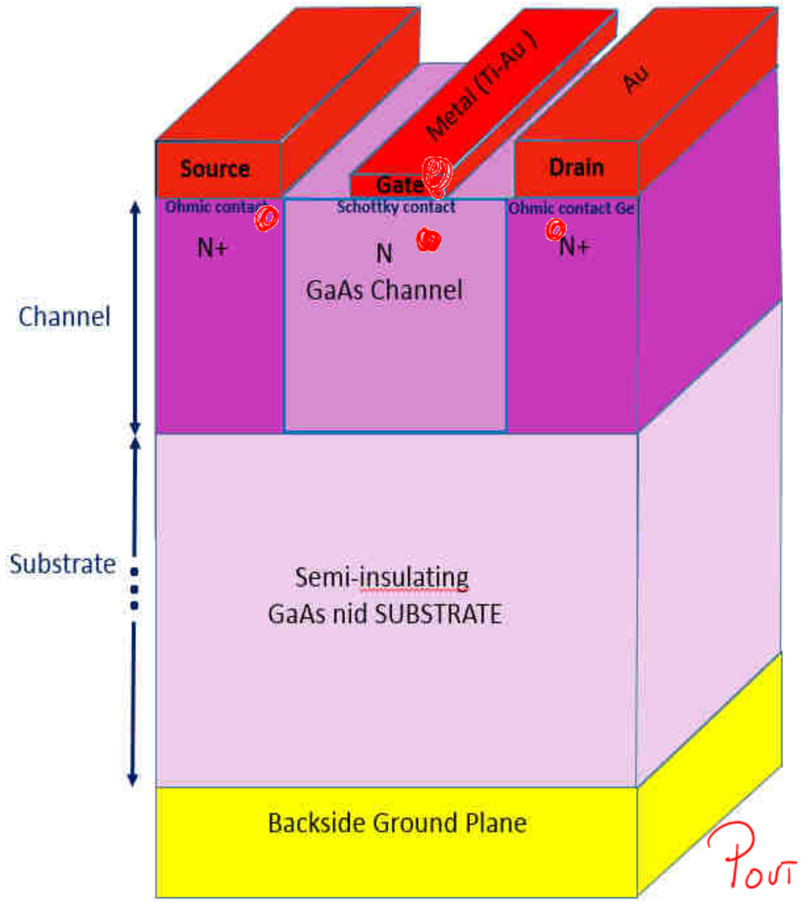


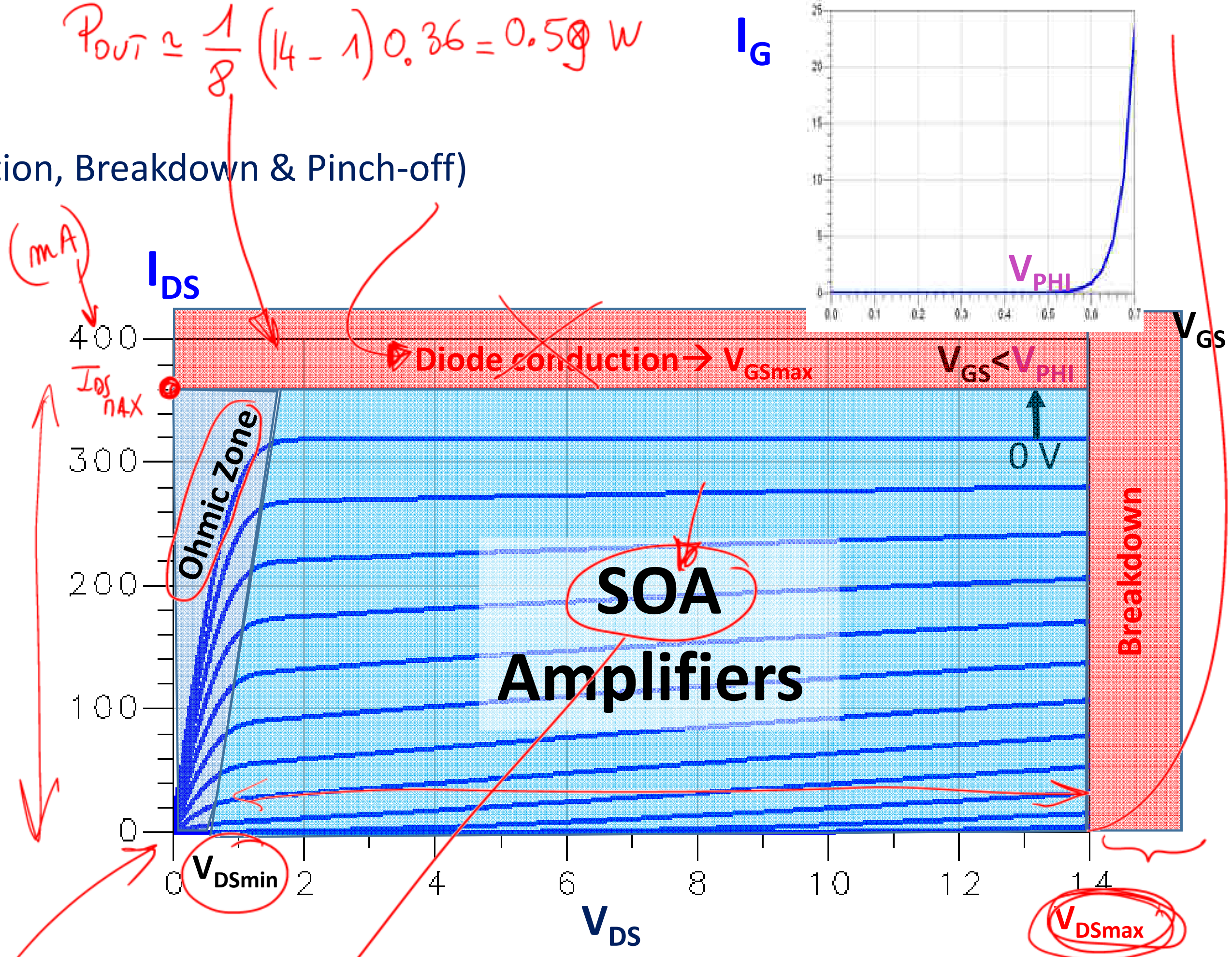


I – Basics of MESFET operation

→ I-V regions (Ohmic, Saturated, Diode conduction, Breakdown & Pinch-off)

$P_{OUT} \simeq \frac{1}{8}(14-1)\,0.36 = 0.59\ W$



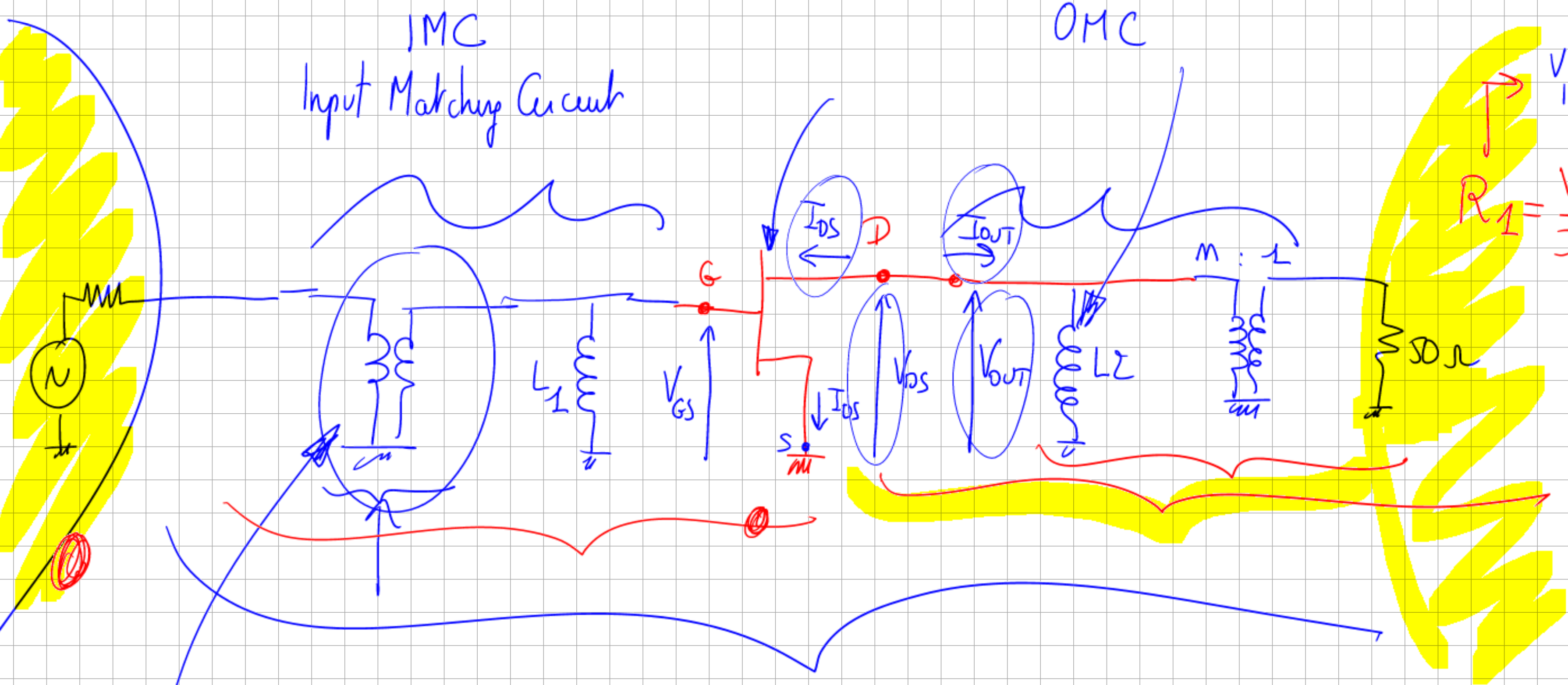


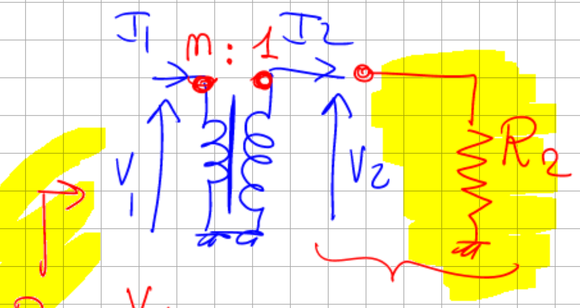
$P_{OUT\,MAX} \simeq \frac{1}{2} \times \frac{V_{DSMAX}-V_{DSMIN}}{2} \times \frac{I_{DSMAX}}{2}$

Safe Operating Area

FET → $V_{DSMAX} \simeq 20V$

HEMT → $V_{DSMAX} \simeq 100\ V$

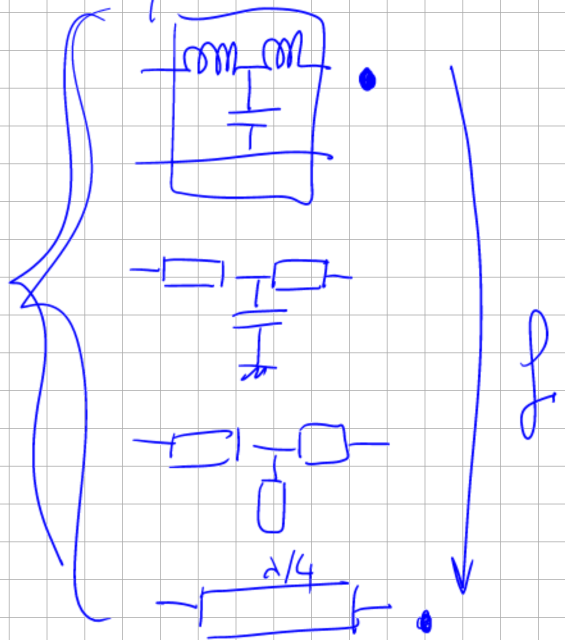


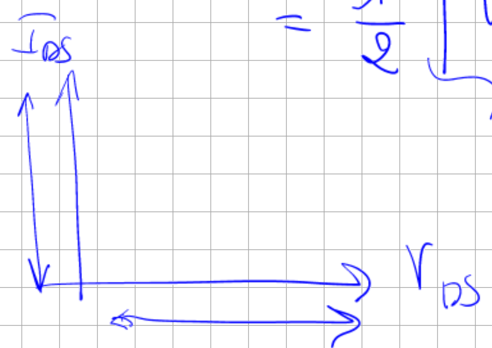


$$R_1 = \frac{V_1}{I_1}$$

$$m = \frac{m_2}{m_1}$$

$$m = \sqrt{\frac{R_2}{R_1}}$$



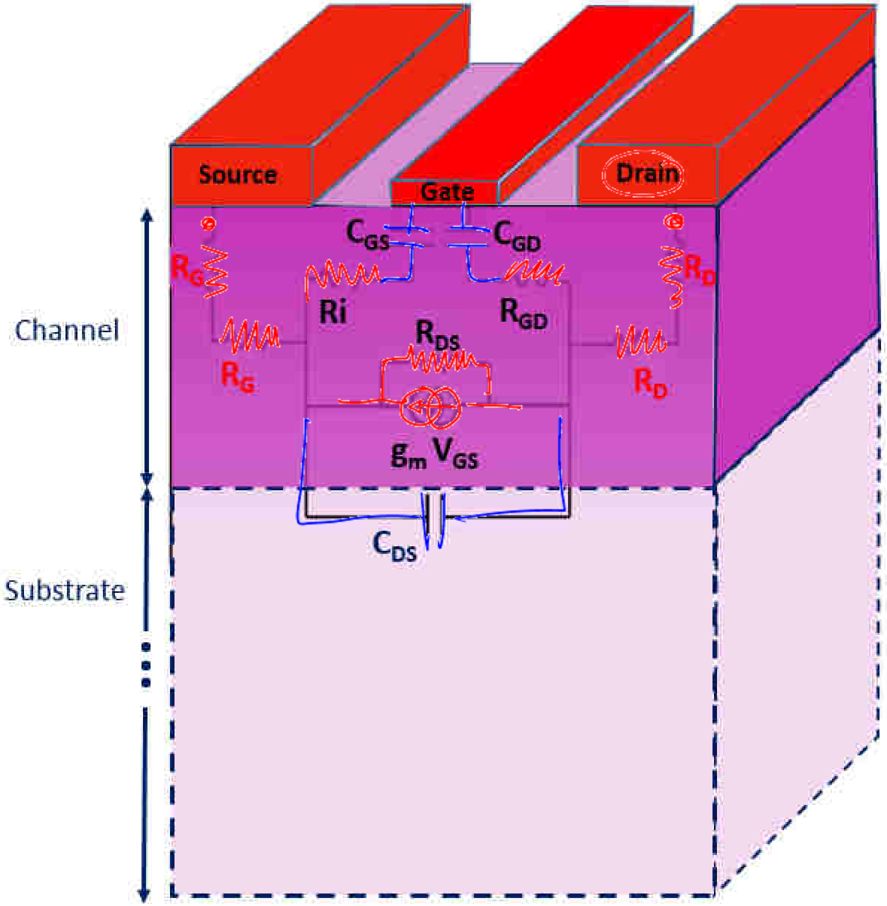


$$P_{OUT} = \frac{1}{2}\,\mathrm{Re}\left(V_{OUT} \times I_{OUT}^{*}\right)$$

$$= \frac{1}{2}\,|V_{OUT}|\,|I_{OUT}|\,\underbrace{\cos\left(\varphi_{V_{OUT}} - \varphi_{I_{OUT}}\right)}_{1}$$

I – Basics of MESFET operation

→ Simplified planar representation of FETs (localization of electrical lumped elements)



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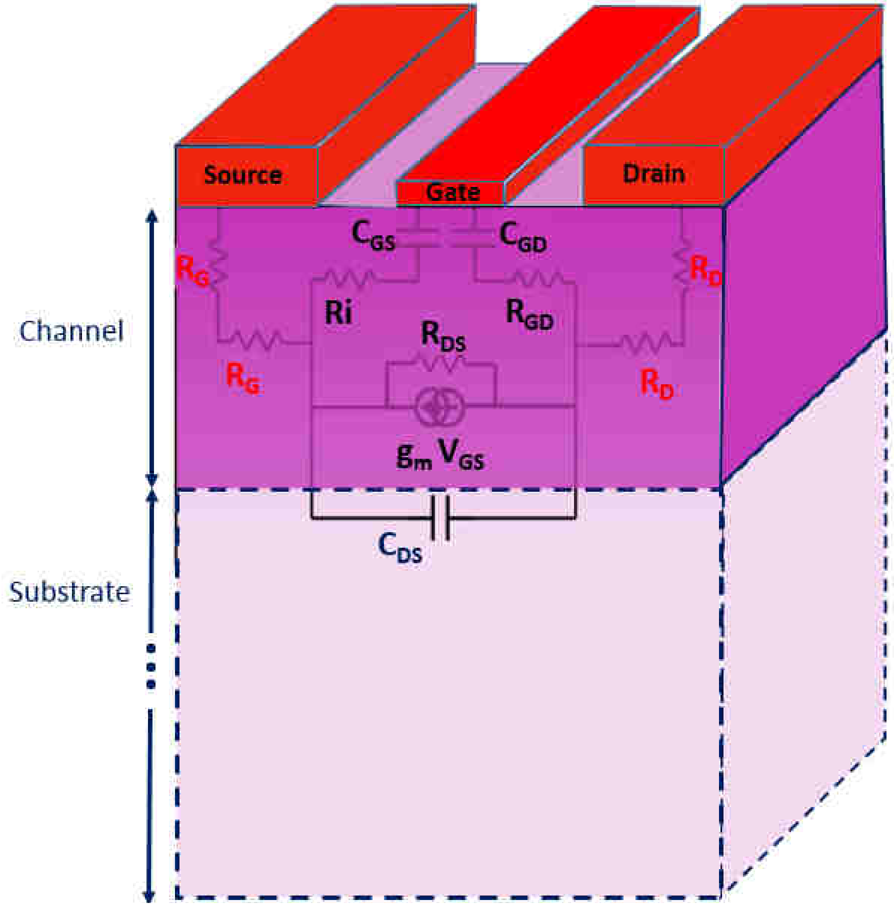
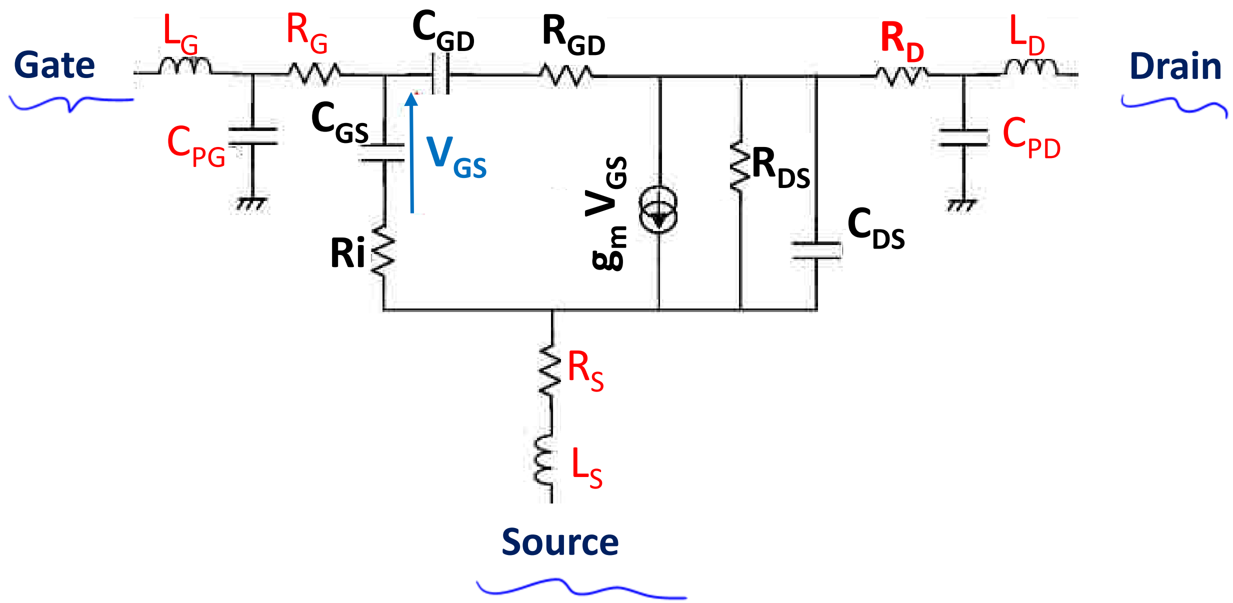
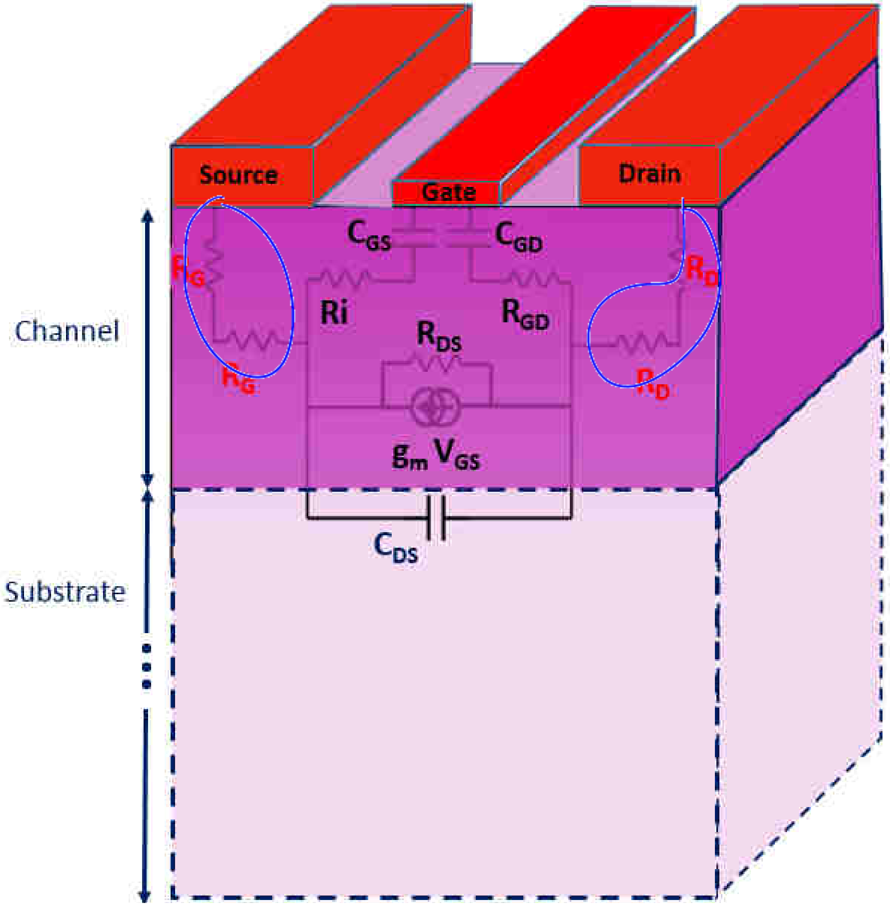


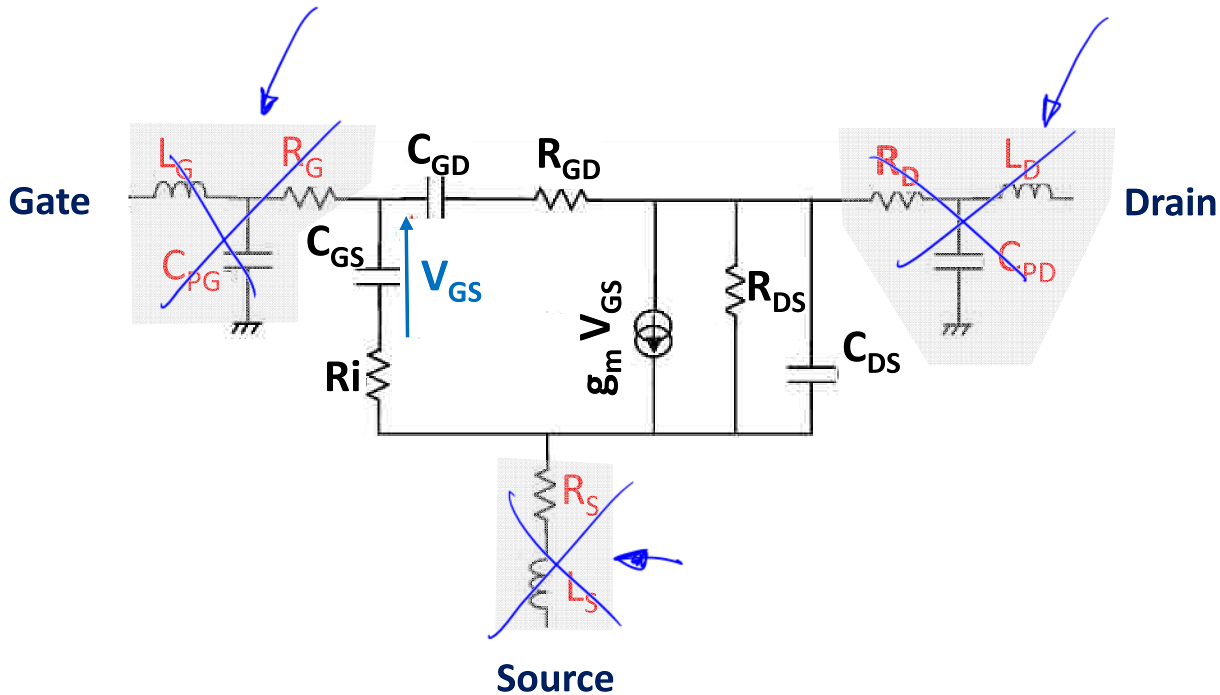


I – Basics of MESFET operation

G = 14dB 15 13

→ Simplified planar representation of FETs (localization of electrical lumped elements)

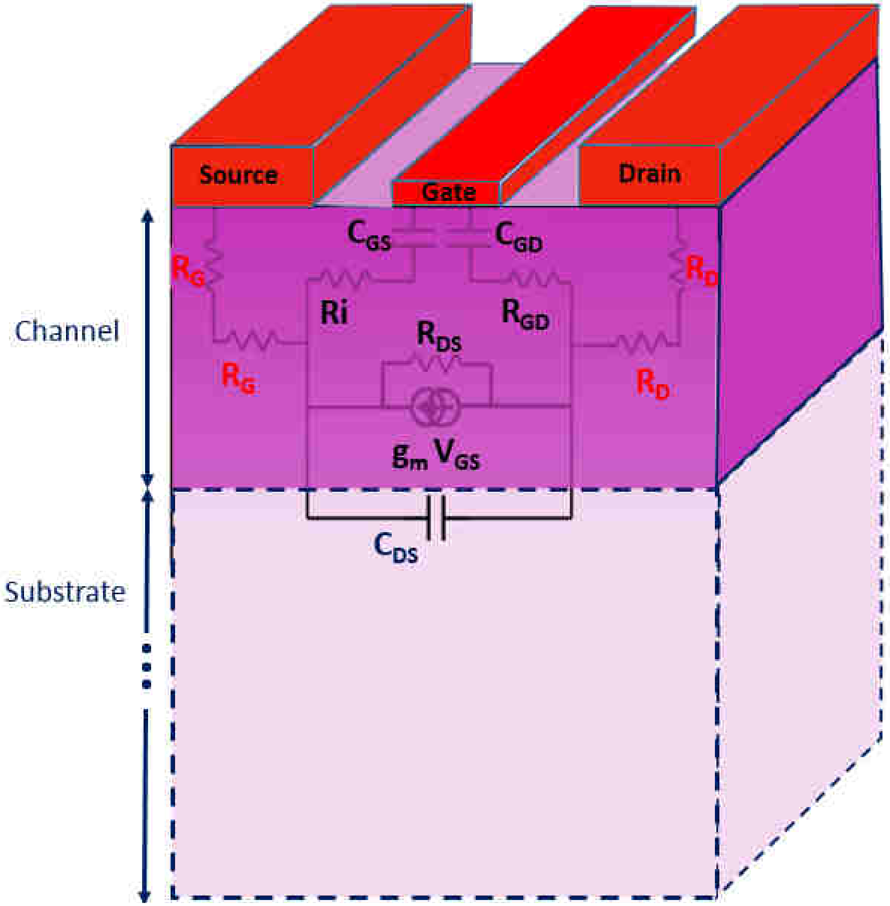


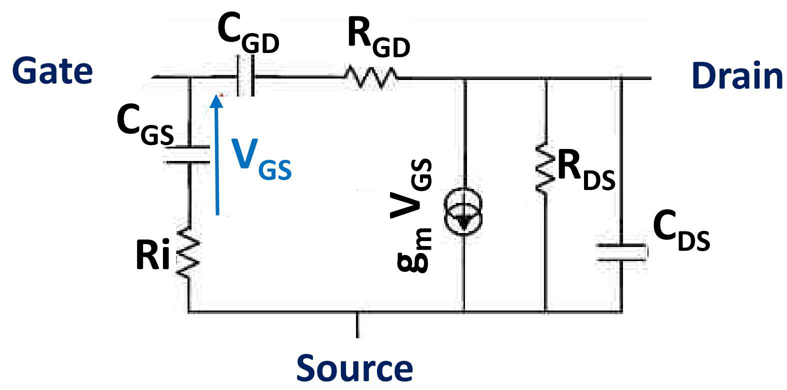


Extrinsic elements are the first ones that can be neglected when compared to other elements

I – Basics of MESFET operation

→ Simplified planar representation of FETs (localization of electrical lumped elements)





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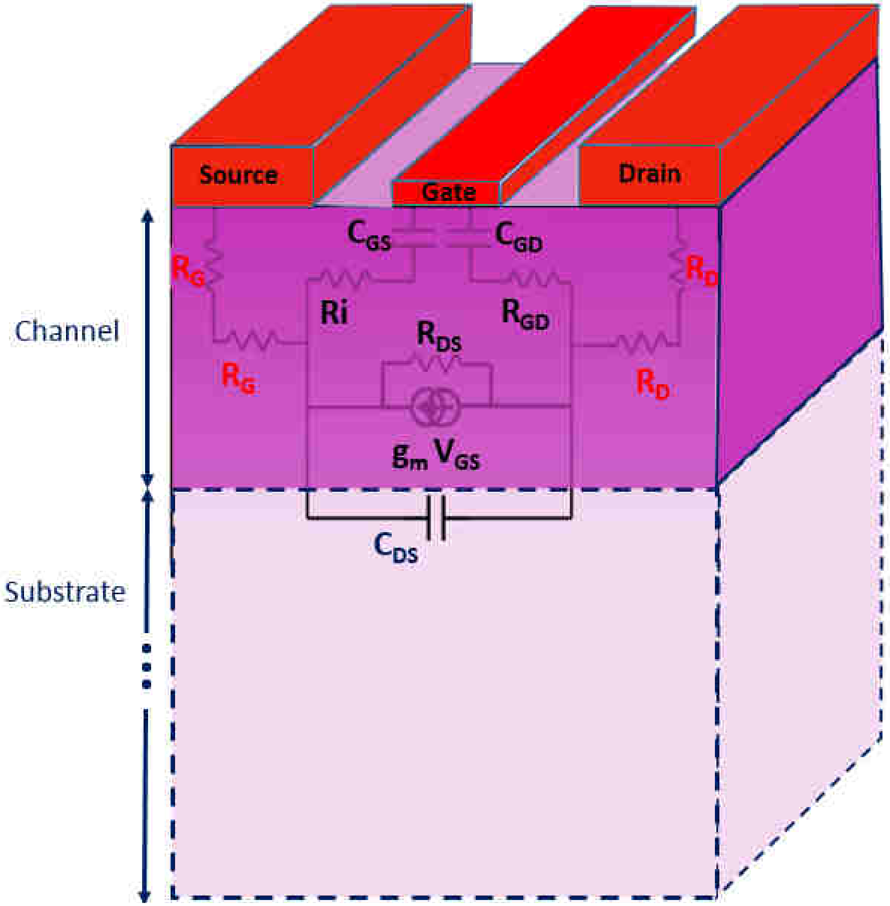
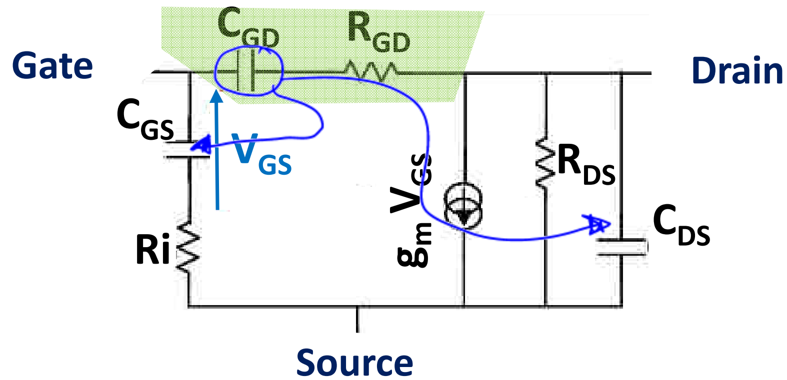
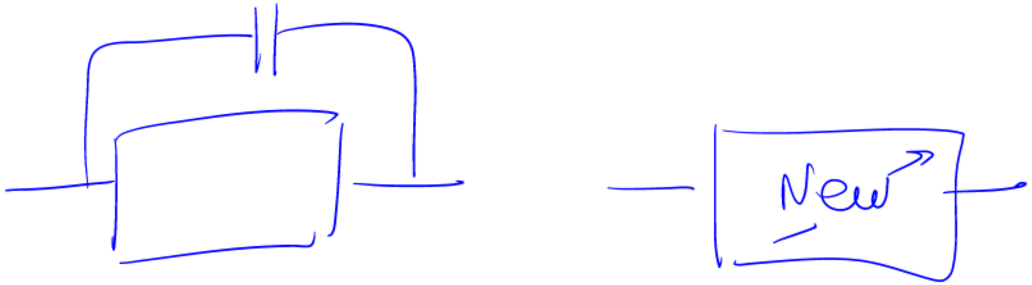


Miller Effect



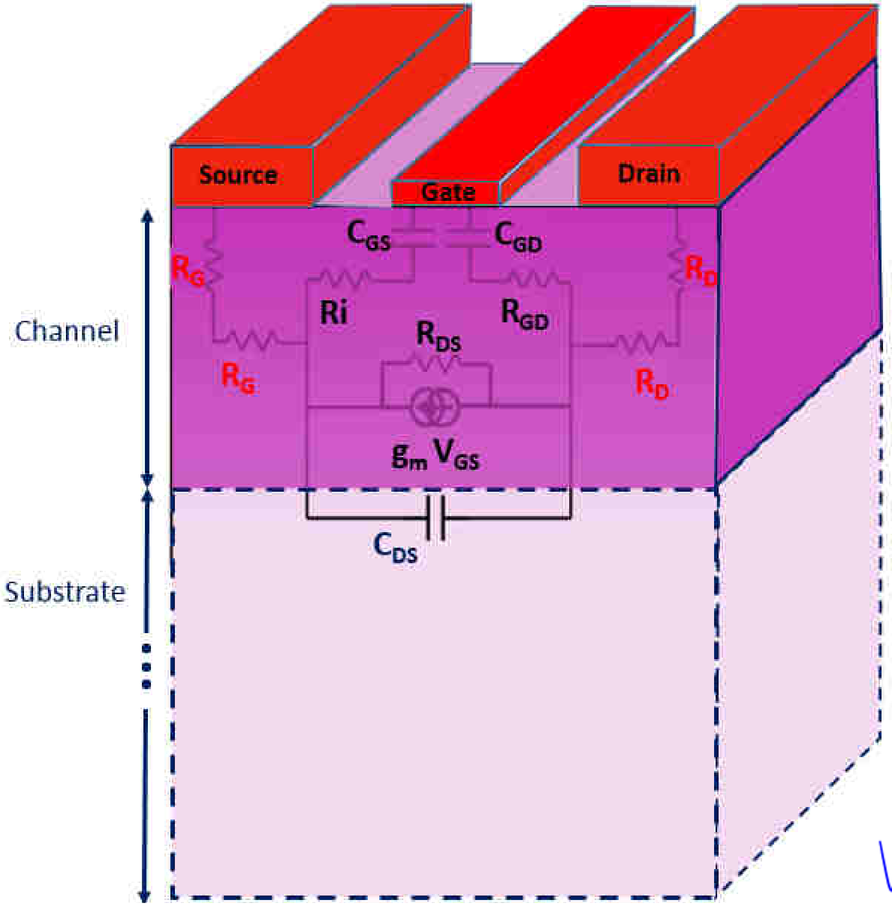
Feedback elements Gate-to-Drain can also be neglected.

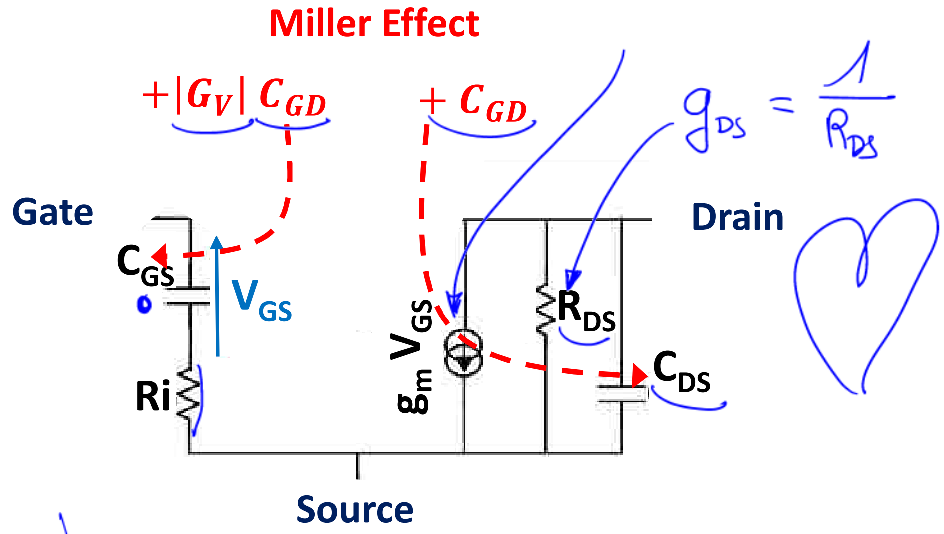


I – Basics of MESFET operation

→ Simplified planar representation of FETs (localization of electrical lumped elements)

Voltage controlled current source





Feedback elements Gate-to-Drain can also be neglected.

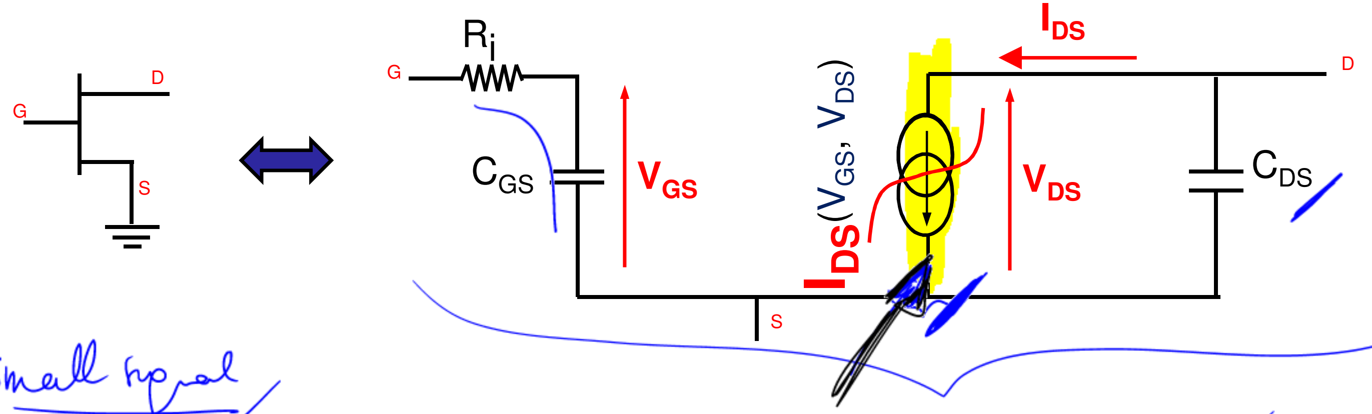
However, the capacitive feedback is taken into account by **Miller Effect**

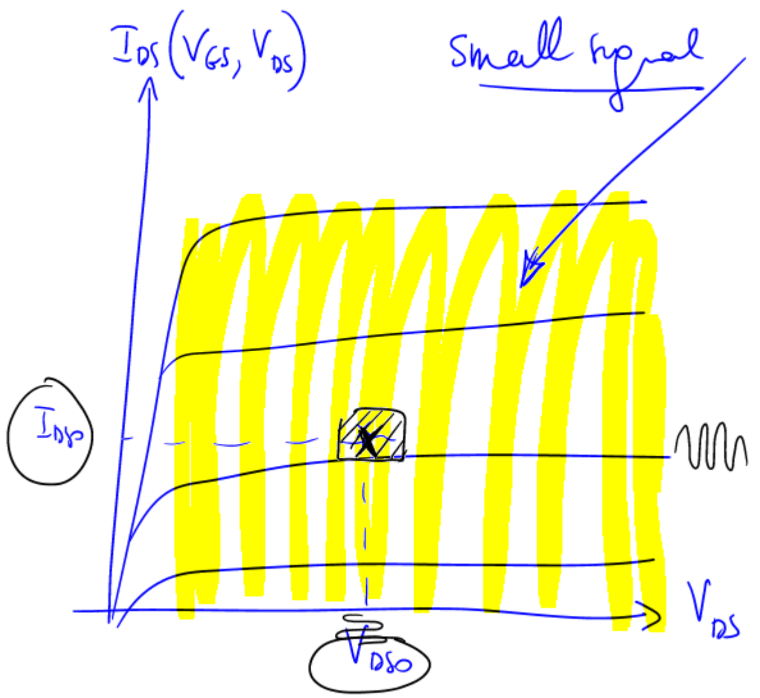
$V = RI$

$I = GV$ with $G = 1/R$

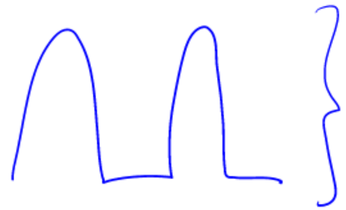
I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point





$$I_{DS} = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2\left(1+K V_{DS}\right)$$



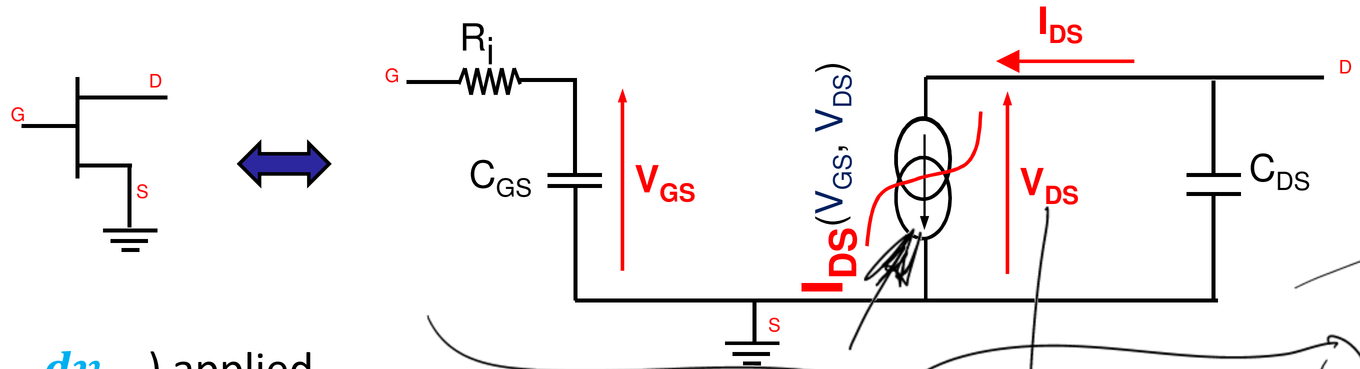
$$I_{DS}(t) = I_{DS0} + I_{DS1}\cos(\omega t+\varphi) + I_{DS2}\cos(2\omega t+\varphi)$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point

$f_{NL}(x,y)$

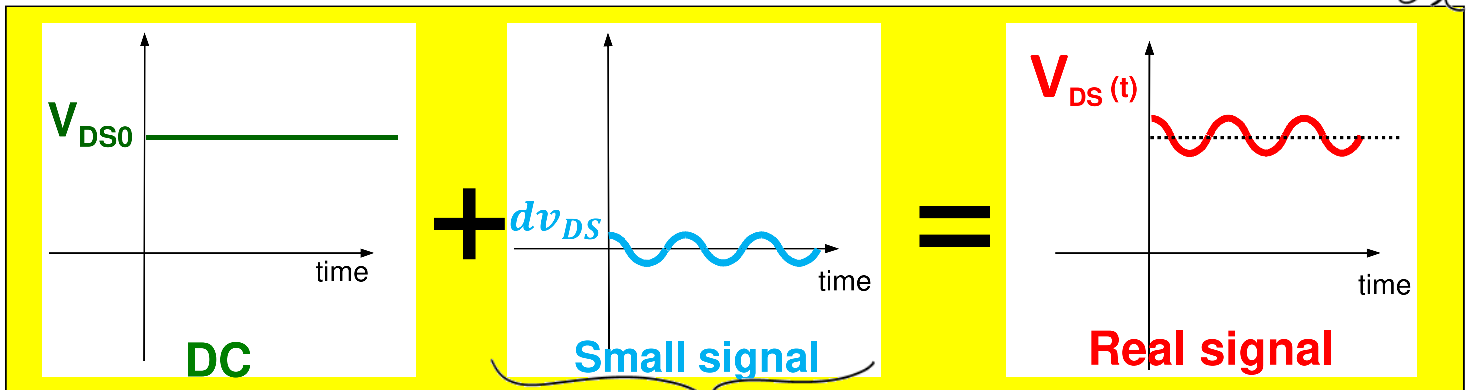
$dx \quad dy$



$df = \left(\frac{\partial f}{\partial x}\right)_{(x_0,y_0)} dx + \left(\frac{\partial f}{\partial y}\right)_{(x_0,y_0)} dy$

Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

$f(x,y) = f(x_0,y_0) + df$



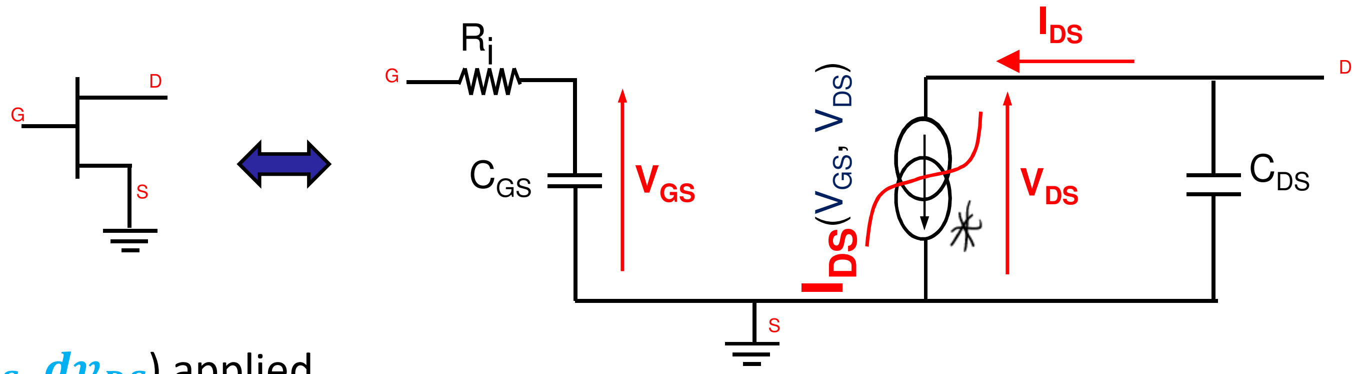
$y = y_0 + dy$

$x = x_0 + dx$

$V_{DS0} + dv_{DS}(t) = v_{DS}(t)$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point



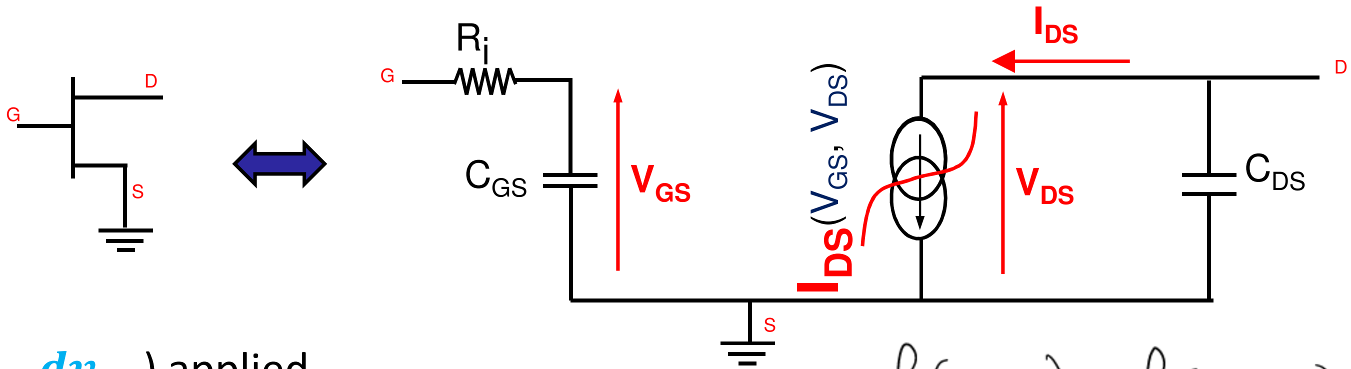
Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

$$V_{GS}(t) = V_{GS0} + dv_{GS}(t)$$

$$V_{DS}(t) = V_{DS0} + dv_{DS}(t)$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point



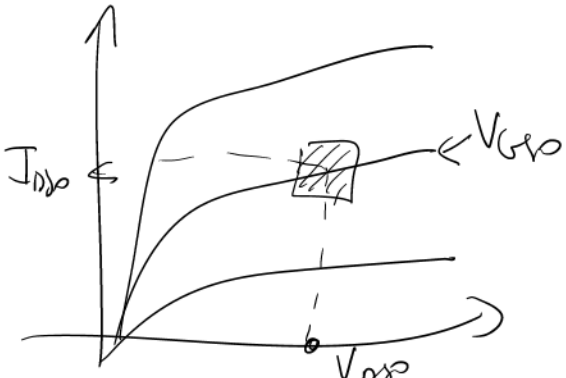
Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

$$f(x,y) = f(x_0, y_0) + df$$

$$V_{GS}(t) = V_{GS0} + dv_{GS}(t)$$
$$V_{DS}(t) = V_{DS0} + dv_{DS}(t)$$

$$I_{DS}(t) = F_{NL}(V_{GS}, V_{DS}) = F_{NL}(V_{GS0}, V_{DS0}) + dF_{NL}$$
$$= I_{DS0} + dF_{NL}$$
$$I_{DS}(t) = I_{DS0} + di_{DS}$$

Taylor expansion

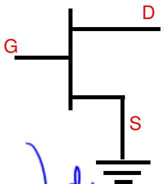


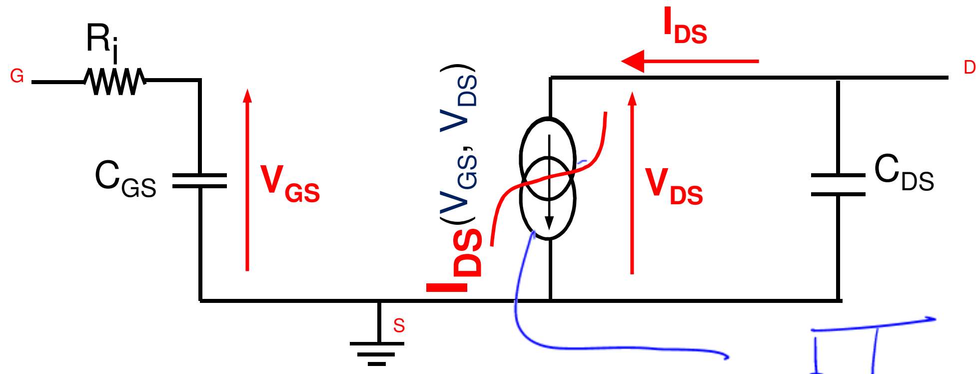
I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point

$f(x,y)$

$df = (\quad) dx + (\quad) dy$





Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

$$V_{GS}(t) = V_{GS0} + dv_{GS}(t)$$

$$V_{DS}(t) = V_{DS0} + dv_{DS}(t)$$

$$\rightarrow \quad I_{DS}(t) = I_{DS0} + di_{DS}$$

Taylor expansion

$$di_{DS} = dF_{NL} = \underbrace{\left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\Bigg|_{(V_{GS0}, V_{DS0})}}_{gm} . \, dv_{GS} + \underbrace{\left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\Bigg|_{(V_{GS0}, V_{DS0})}}_{gd = 1/R_{DS}} . \, dv_{DS}$$

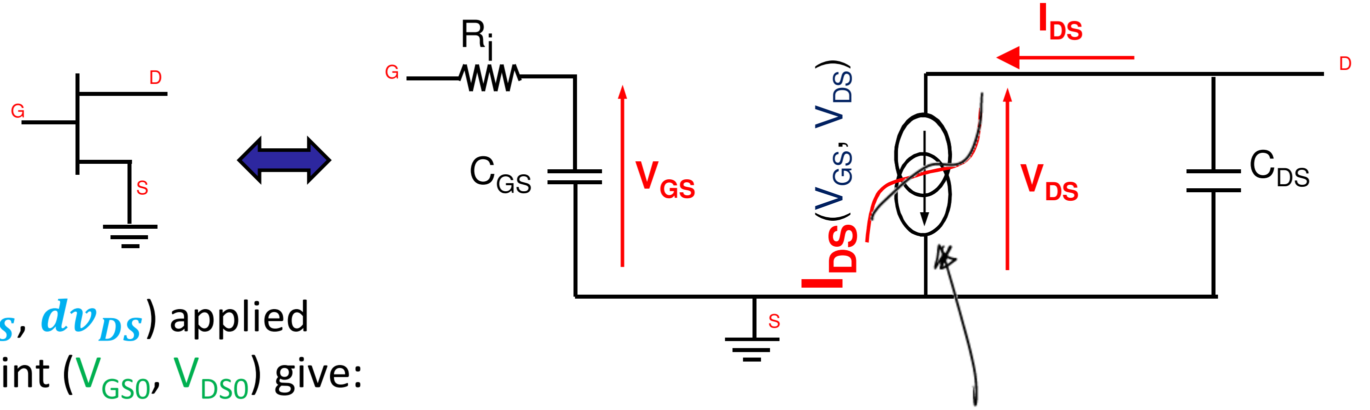
$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{(V_{GS0},\, V_{DS0})} = \text{FET transconductance} = S = \Omega^{-1}$$

$$g_D \simeq g_{DS} = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{(V_{GS0},\, V_{DS0})} = \text{Drain\_Source conductance} = \Omega^{-1}$$

$$\boxed{R_{DS} = \frac{1}{g_{DS}}}$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point



Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

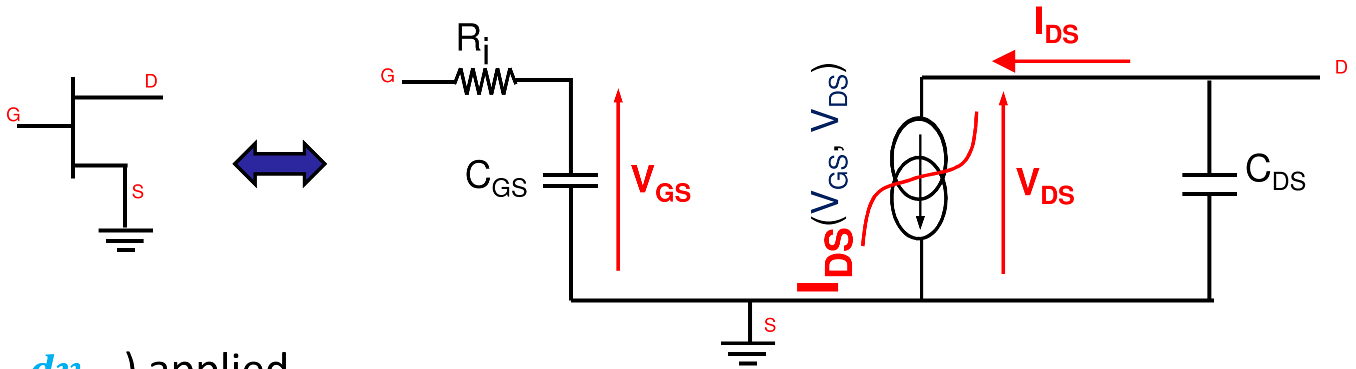
dv_{GS}(t)
dv_{DS}(t)

$$\Longrightarrow \quad I_{DS}(t) = I_{DS0} + di_{DS}$$

$$di_{DS} = dF_{NL} = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\bigg|_{(V_{GS0},\, V_{DS0})} . \, dv_{GS} + \left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\bigg|_{(V_{GS0},\, V_{DS0})} . \, dv_{DS} = g_m . dv_{GS} + g_{DS} . dv_{DS}$$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point



Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

$dv_{GS}(t)$
$dv_{DS}(t)$

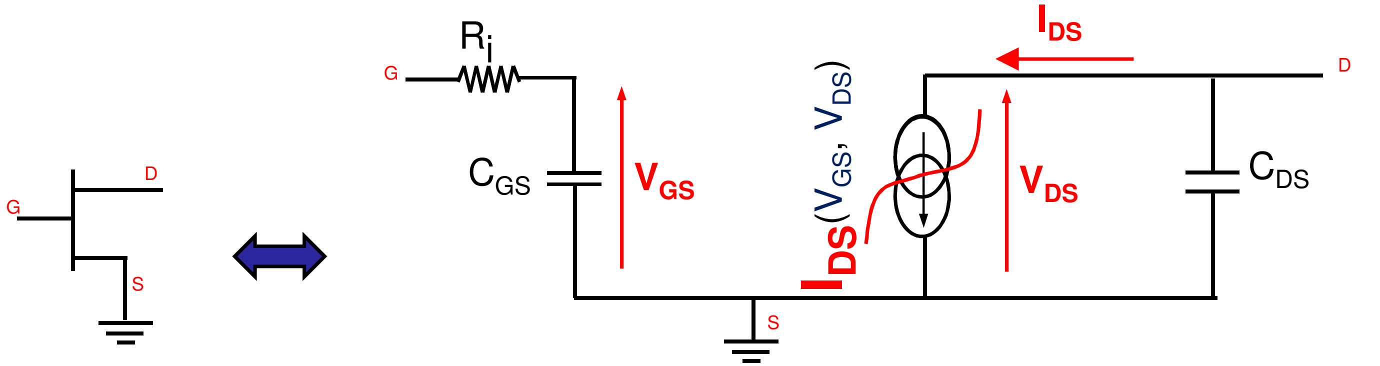
$$\cancel{d}i_{DS} = g_m \cdot \cancel{d}v_{GS} + g_{DS} \cdot \cancel{d}v_{DS}$$

$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\Bigg|_{(V_{GS0},\, V_{DS0})} \qquad g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\Bigg|_{(V_{GS0},\, V_{DS0})}$$

$$i_{ds} = g_m \cdot v_{gs} + g_{ds} \cdot v_{ds} \longleftarrow$$

$$v_{DS} = V_{DS0} + v_{ds}$$

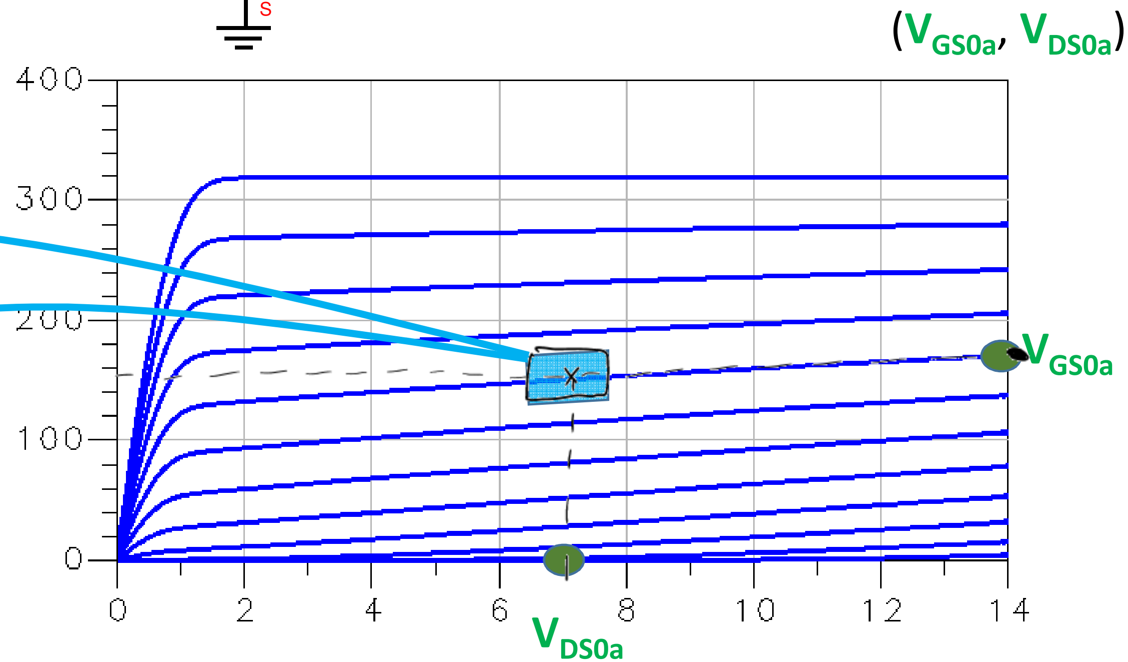
I – Basics of FET operation



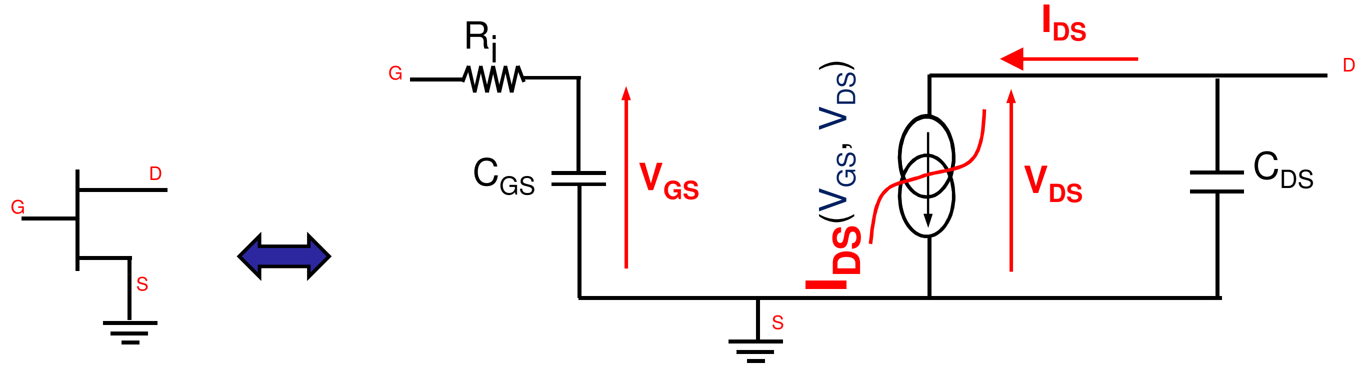
Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\Bigg|_{(V_{GS0},\, V_{DS0})} X$$

$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\Bigg|_{(V_{GS0},\, V_{DS0})} X$$



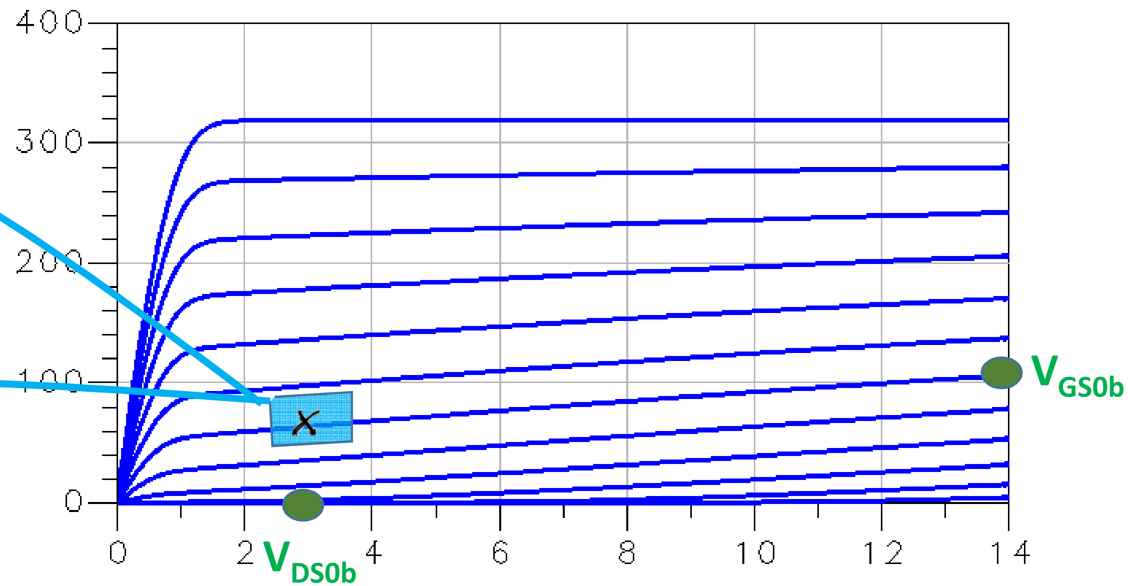
I – Basics of FET operation



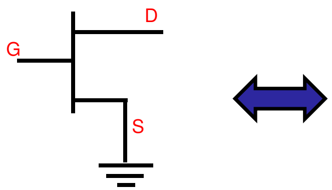
Small signals (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

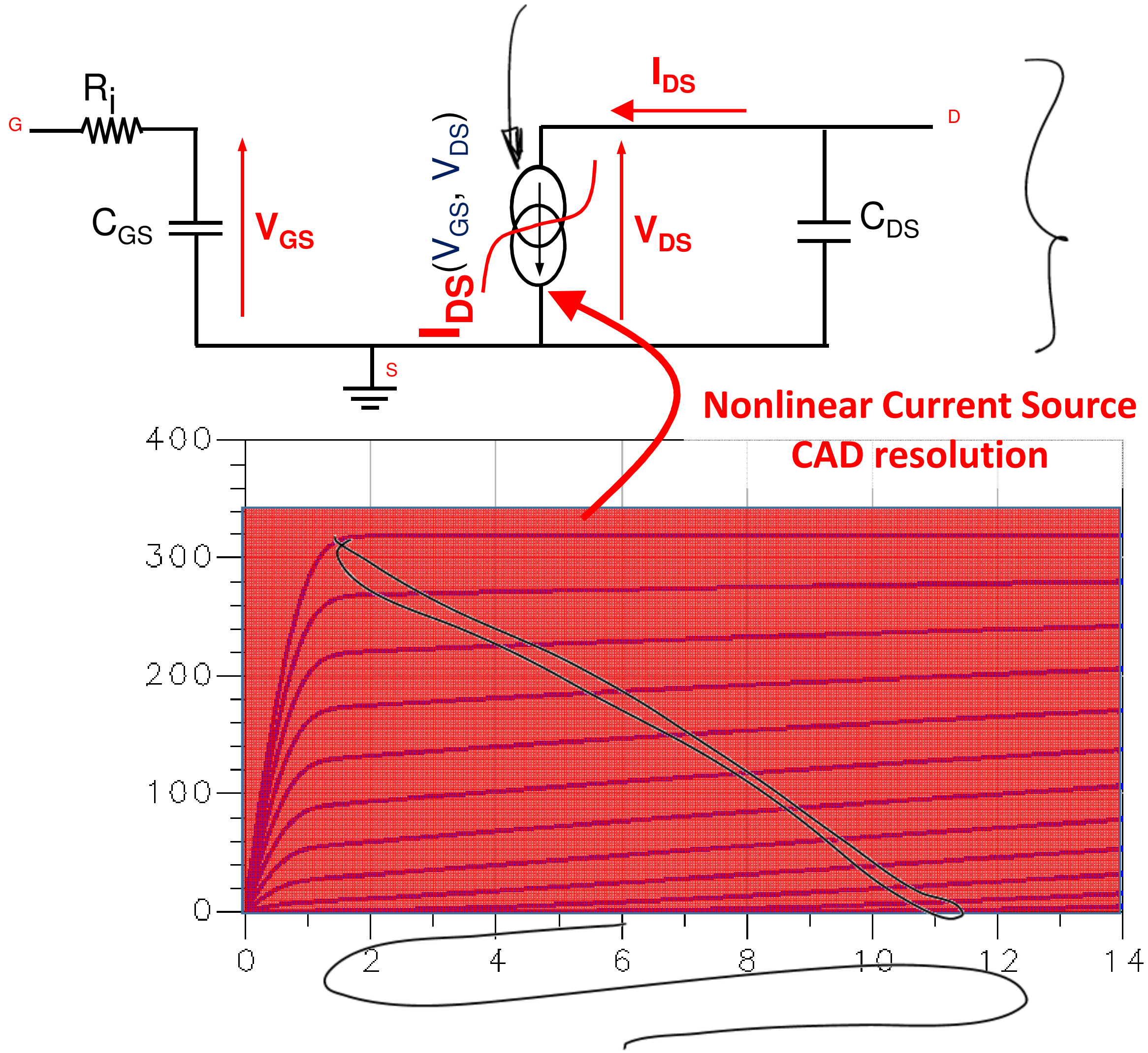
$$g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\Bigg|_{(V_{GS0},\ V_{DS0})}$$

$$g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\Bigg|_{(V_{GS0},\ V_{DS0})}$$



I – Basics of FET operation





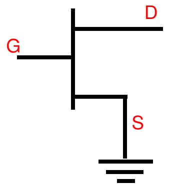
Large signals (ΔV_{GS}, ΔV_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

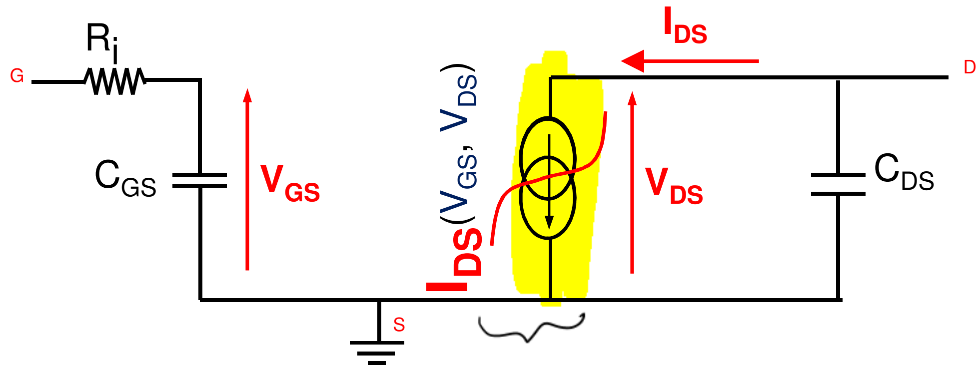
$$\cancel{g_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)\Bigg|_{(V_{GS0},\, V_{DS0})}}$$

$$\cancel{g_{DS} = \left(\frac{\delta I_{DS}}{\delta V_{DS}}\right)\Bigg|_{(V_{GS0},\, V_{DS0})}}$$

I – Basics of FET operation

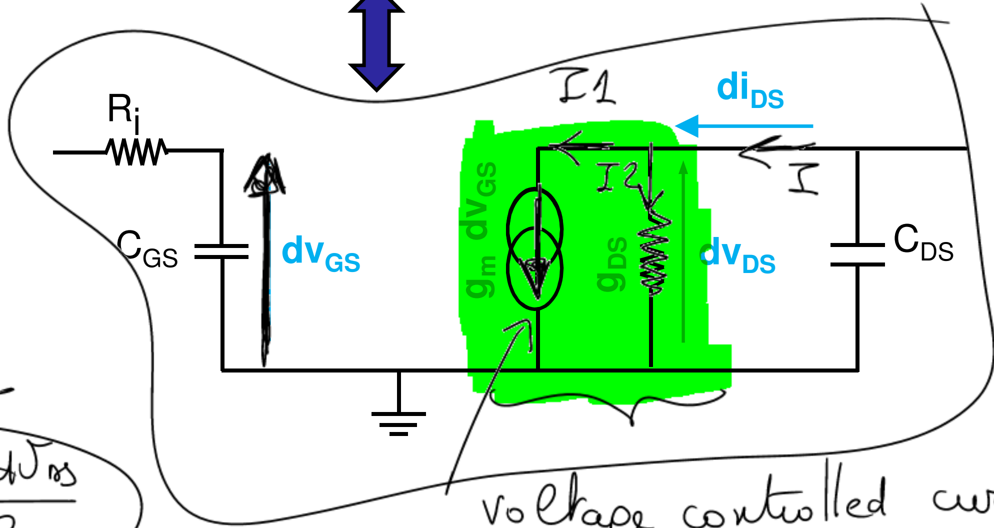
→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point





➢ **Small signals** (dv_{GS}, dv_{DS}) applied around the bias point (V_{GS0}, V_{DS0}) give:

$$\left.\begin{aligned} V_{GS} &= V_{GS0} + dv_{GS} \\ V_{DS} &= V_{DS0} + dv_{DS} \end{aligned}\right\}$$



$V = RI$

$I = \frac{V}{R}$

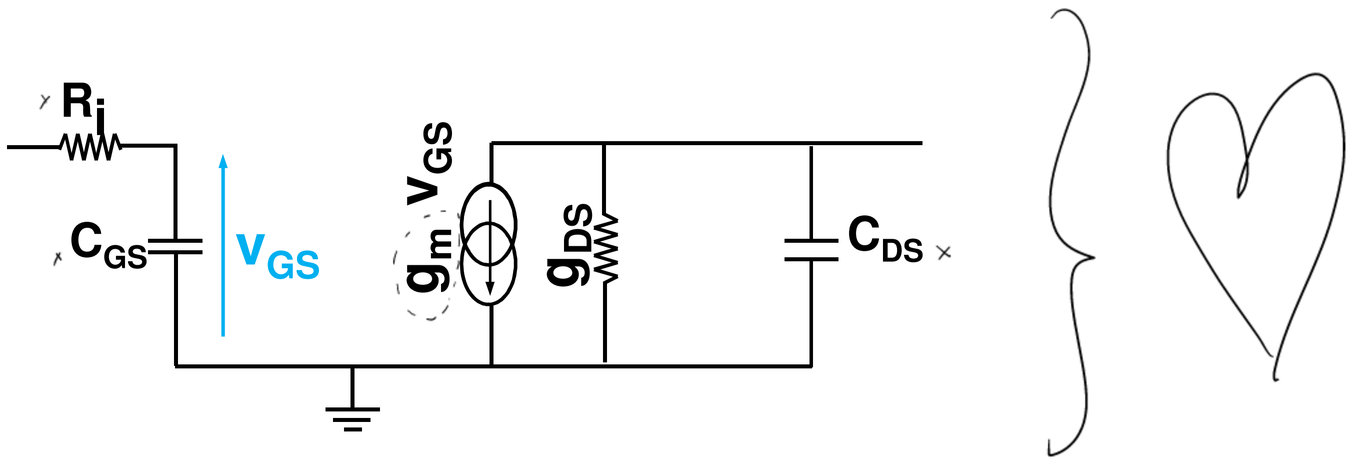
Ohm's law

$$\underbrace{di_{DS}}_{I} = \underbrace{g_m \times dv_{gs}}_{I1} + \underbrace{g_{ds} \times dv_{ds}}_{I2 = \frac{dv_{ds}}{R_{ds}}}$$

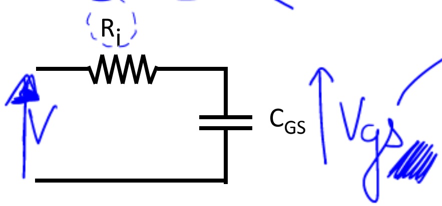
voltage controlled current source $g_m \times dv_{gs}$

I – Basics of FET operation

→ Simplified Small-signal equivalent of the nonlinear drain current (gm, gd) around a specific bias point



II – Intrinsic figures of merit for FETs



$g_m \cdot V_{gs}$

1) Low-Pass Frequency (Low-Pass Input RC circuit)

$$\boxed{f_{LP} = \frac{1}{2\pi R_i C_{GS}}}$$

The FET is efficiently used at frequencies $f \ll f_{LP}$ → $\boxed{R_i C_{GS}\omega \ll 1}$

$f \ll f_{LP}$

$\omega \ll \omega_{LP} = \dfrac{1}{R_i C_{gs}}$

2) Cutoff frequency of gain current

I_{IN} I_{OUT} Short Circuit

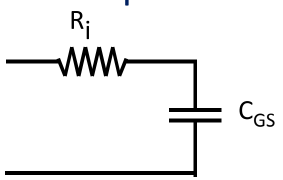
Current Gain in Short-Circuit

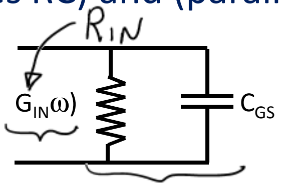
$$Gi_{SC} = \frac{I_{OUT\,SC}}{I_{IN}} = \frac{g_m V_{GS}}{j\, C_{GS}\,\omega\, V_{GS}} = \frac{g_m}{j\, C_{GS}\omega} \Rightarrow |Gi_{SC}(f_C)| \overset{\text{def}}{=} 1 \Leftrightarrow \frac{g_m}{C_{GS}\omega_C} = 1 \Leftrightarrow \omega_C = \frac{g_m}{C_{GS}}$$

$$\boxed{f_C = \frac{g_m}{2\pi C_{GS}}}$$

f_C is widely used to compare FETs with each other

→ Narrowband equivalence between (series RC) and (parallel RC) circuit at the FET input



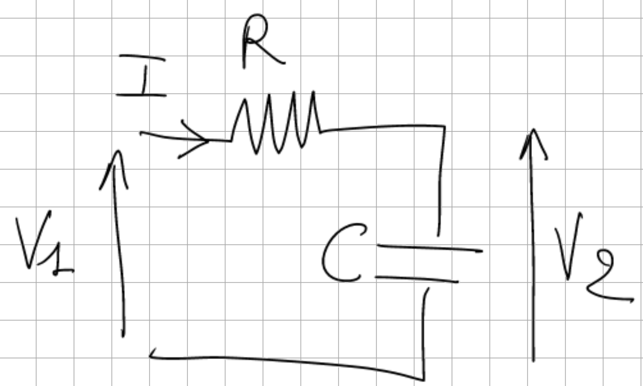


$$\boxed{G_{IN}(\omega) = R_i\, C_{GS}^2\, \omega^2}$$

$R_{IN} = \dfrac{1}{G_{IN}}$

$\Leftrightarrow Y_{eq} =$

$Y_{eq} = \left(\dfrac{1}{R_{IN}}\right) + j\left(C_{GS}\,\omega\right)$



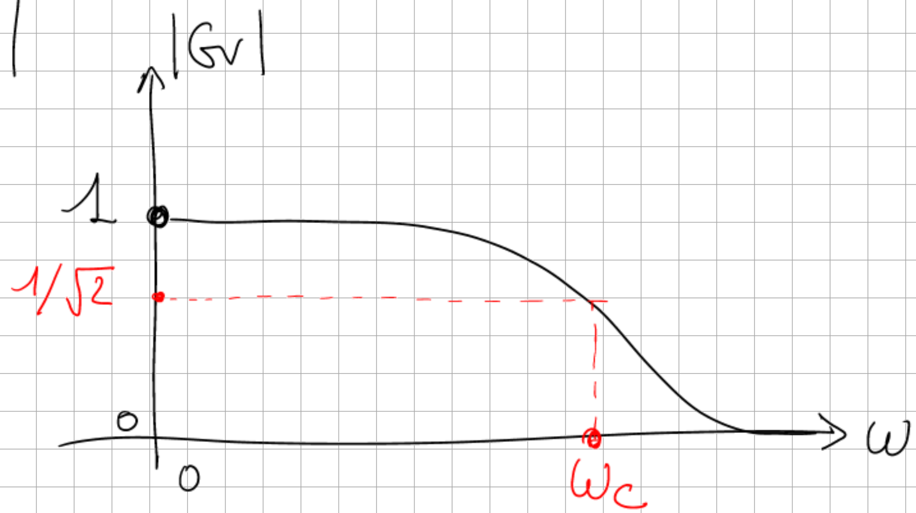
$$\begin{cases} V_2 = Z_C \times I \\ V_1 = (R + Z_C)\, I \end{cases}$$

$$\boxed{Z_C = \frac{1}{jC\omega}}$$

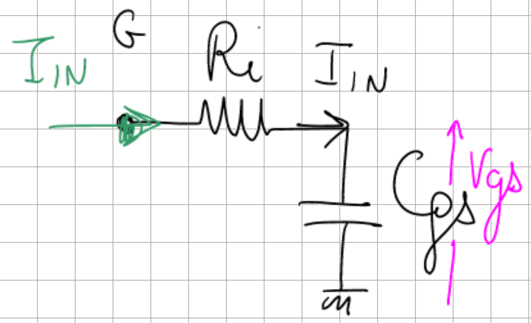
$$\frac{V_2}{V_1} = \frac{Z_C}{R + Z_C} = \frac{1}{1 + \frac{R}{Z_C}}$$

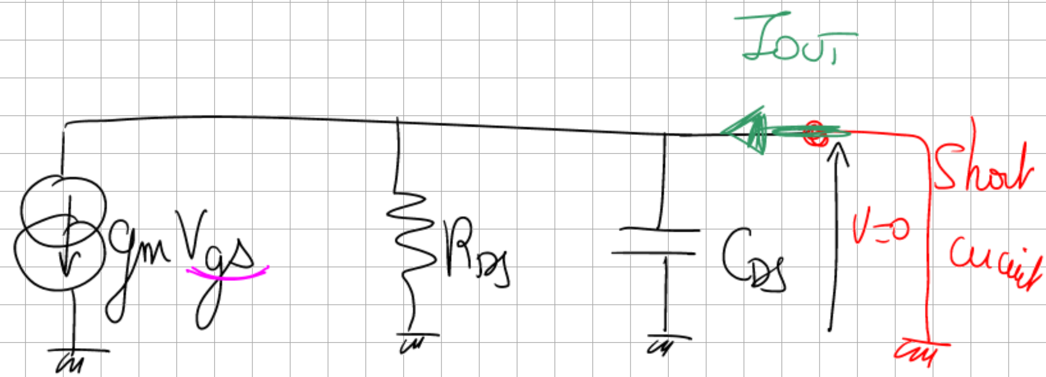
$$\boxed{\frac{V_2}{V_1} = \frac{1}{1 + jRC\omega}}$$

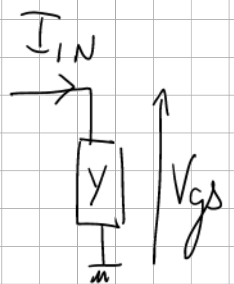
$$\left|\frac{V_2}{V_1}\right| = \frac{1}{\sqrt{1 + \underbrace{(RC\omega)^2}_{1}}} = |G_V|$$

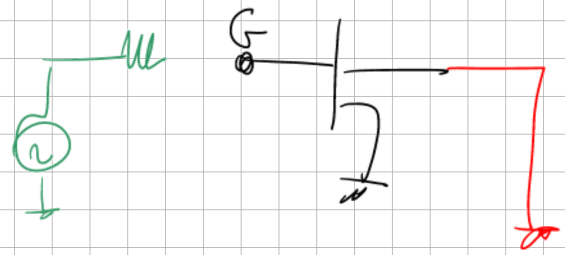


$$\omega_c = \frac{1}{RC} \rightarrow \underbrace{f_c = \frac{1}{2\pi RC}}$$









$$I_{IN} = Y_{gs} \times V_{gs}$$

$$\underline{V} = \underline{Z}\,\underline{I}$$

$$\underline{I} = \frac{\underline{V}}{\underline{Z}} = \underline{Y} \times \underline{V}$$

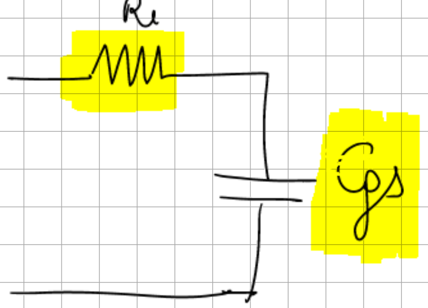
$$\boxed{I_{IN} = (j C_{gs} \omega)\, V_{gs}} \qquad \boxed{I_{OUT} = g_m \cdot V_{gs}}$$

$$G_{I(sc)} = \frac{I_{OUT}}{I_{IN}} = \frac{g_m \cdot V_{gs}}{(j C_{gs} \omega) V_{gs}} = \frac{g_m}{j C_{gs} \omega}$$

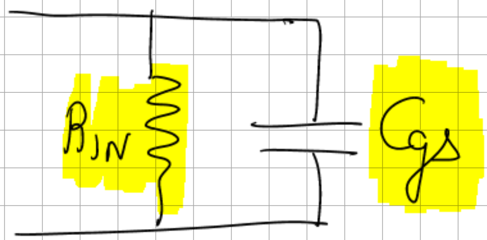
$$|G_{I_{sc}}(f_c)| = 1$$

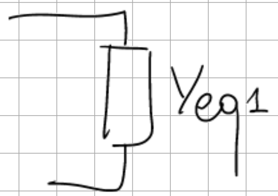
$$\frac{g_m}{C_{gs} \omega_c} \triangleq 1 \rightarrow \omega_c = \frac{g_m}{C_{gs}} \rightarrow \boxed{f_c = \frac{g_m}{2\pi C_{gs}}}$$

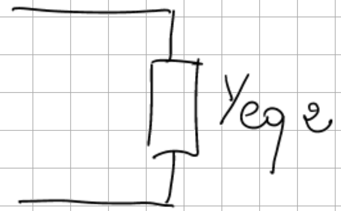
Equivalent Parallel circuit at the input



$\equiv$







$$Z_{eq1} = R_i + \frac{1}{j C_{gs} \omega} = \frac{1 + j R_i C_{gs} \omega}{j C_{gs} \omega}$$

$$Y_{eq2} = \frac{1}{R_{IN}} + j C_{gs} \omega$$

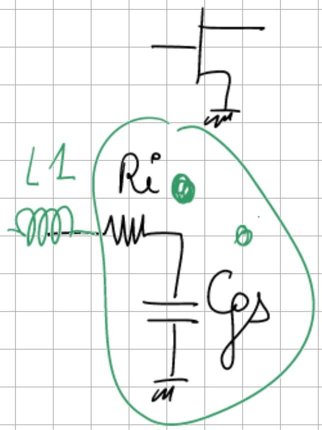
$$Y_{eq1} = \frac{j C_{gs} \omega}{1 + j R_i C_{gs} \omega}$$

$$= \frac{j C_{gs} \omega (1 - j R_i C_{gs} \omega)}{1 + \cancel{(R_i C_{gs} \omega)^2}} = R_i C_{gs}^2 \omega^2 + j C_{gs} \omega$$

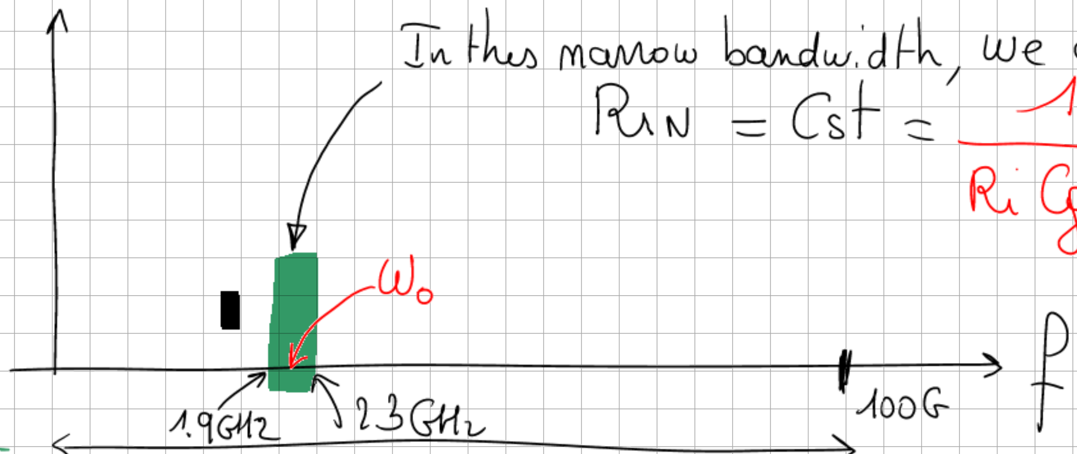
$f \ll f_{LP}$

$$\boxed{R_i C_{gs} \omega \ll 1}$$

$$\boxed{R_{IN} = \frac{1}{R_i C_{gs}^2 \omega^2}} \boxed{= R_{IN}(\omega)}$$



$$L1 = \frac{1}{C_{gs}\,\omega_0^2}$$



In this narrow bandwidth, we can assume that

$$R_{IN} = Cst = \frac{1}{R_i\,C_{gs}^2\,\omega_0^2}$$

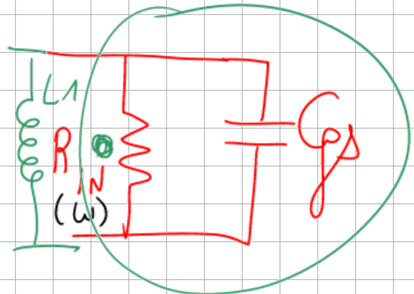
Operating frequency domain where $R_i C_{gs} \omega \ll 1$

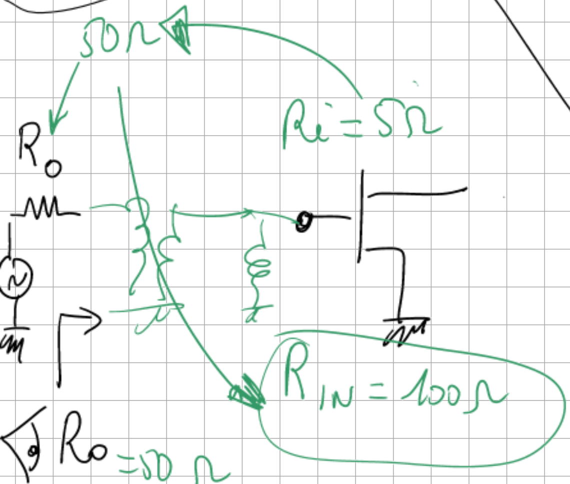
eg: $R_i = 4\,\Omega$

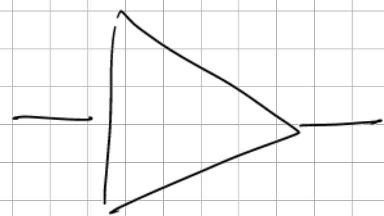
$C_{gs} = 2\,pF$

$R_{IN} = 100\,\Omega$

$R_{IN} = 10$



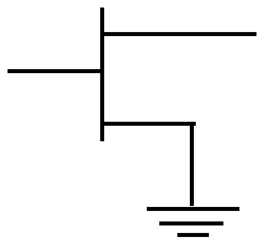


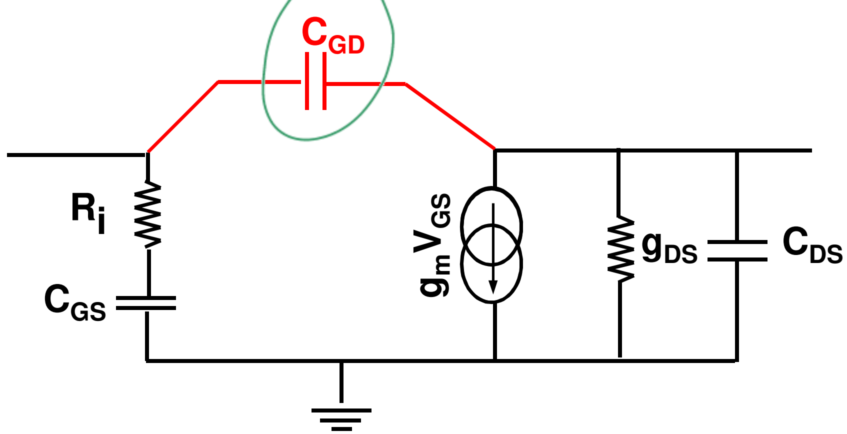


$R_i \propto R_{IN}$

II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)





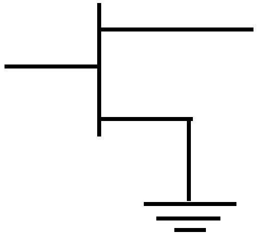
II – Intrinsic figures of merit for FETs

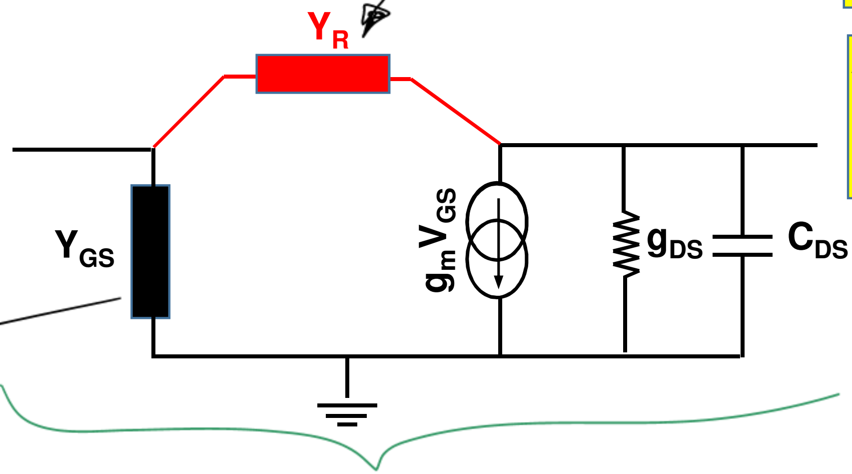
$Y_R = j\, C_{gd}\, \omega$

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

$$Y_R = j\, C_{GD}\omega$$

$$Y_{GS} = \frac{1}{R_i + \frac{1}{jC_{GS}\omega}}$$

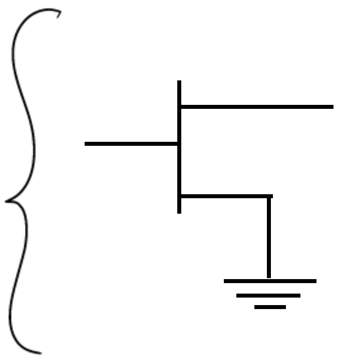


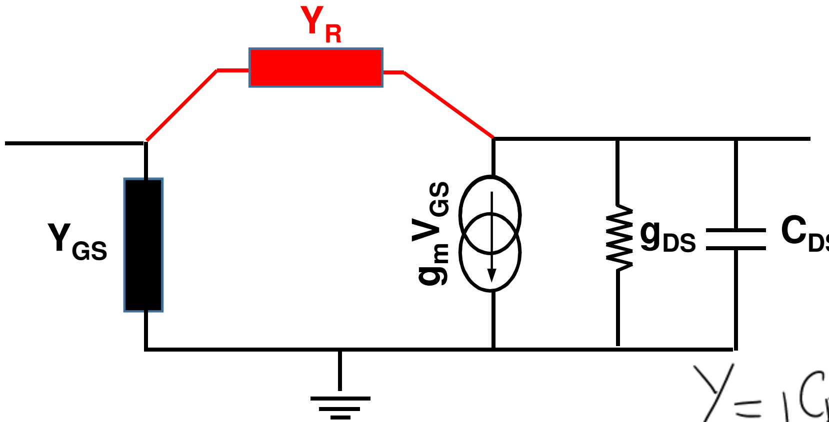


$$Y_{GS} = \frac{1}{R_{IN}} + j\, C_{gs}\, \omega$$

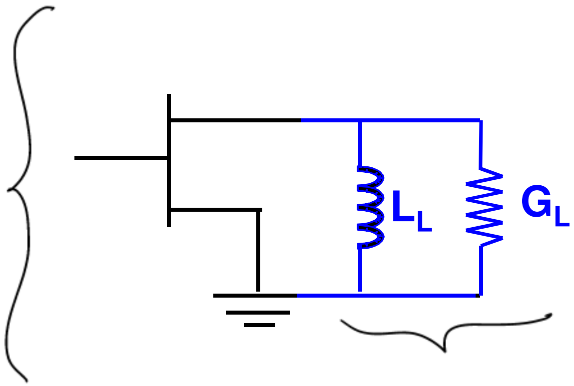
II – Intrinsic figures of merit for FETs

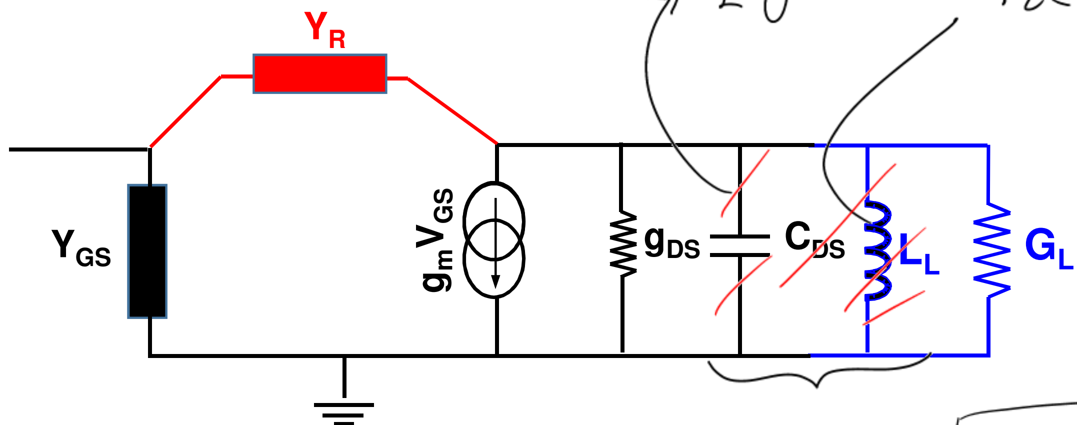
3) Miller Effect (Feedback admittance Y_R and conductance load G_L)





$Y_1 = j C_{DS} \omega$ $Y_2 = \frac{1}{j L_L \omega}$





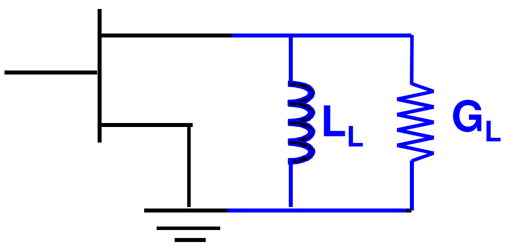
$$Y_1 + Y_2 = 0 \Leftarrow j C_{DS} \omega = \frac{-1}{j L_L \omega} \Rightarrow \boxed{L_L C_{DS} \omega^2 = 1}$$

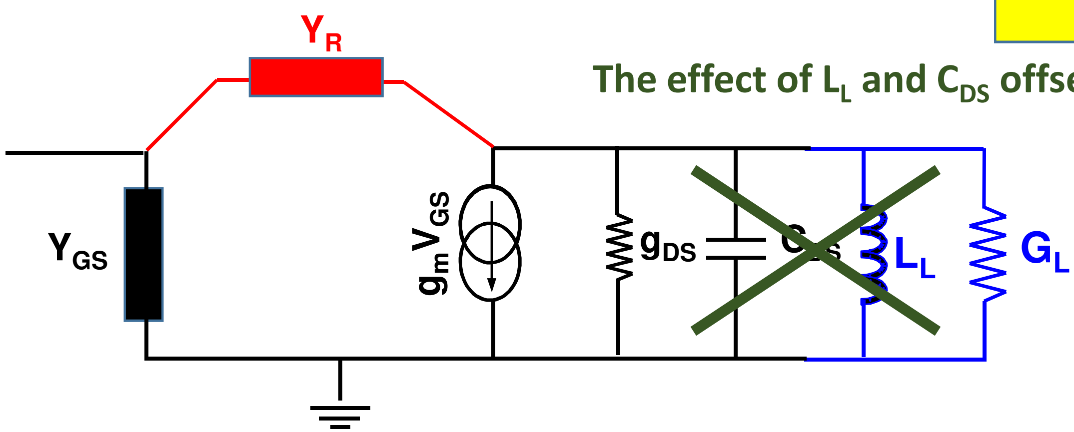
II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

$$L_L\, C_{DS}\, \omega_o^2 = 1 \quad \rightarrow \quad \boxed{L_L = \frac{1}{C_{DS}\omega_o^2}}$$

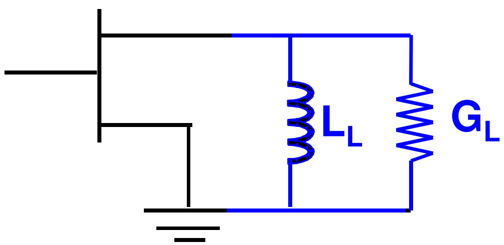
The effect of L_L and C_{DS} offset each other

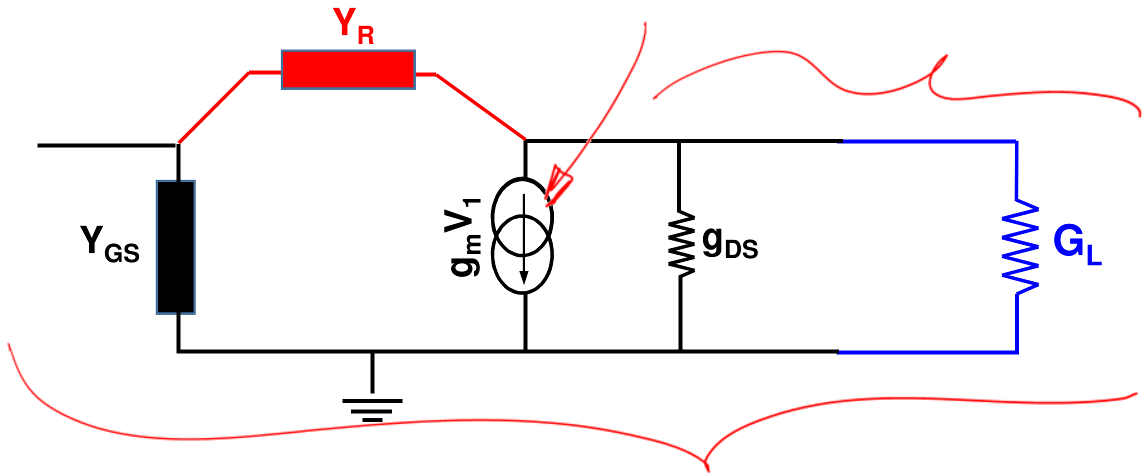




II – Intrinsic figures of merit for FETs

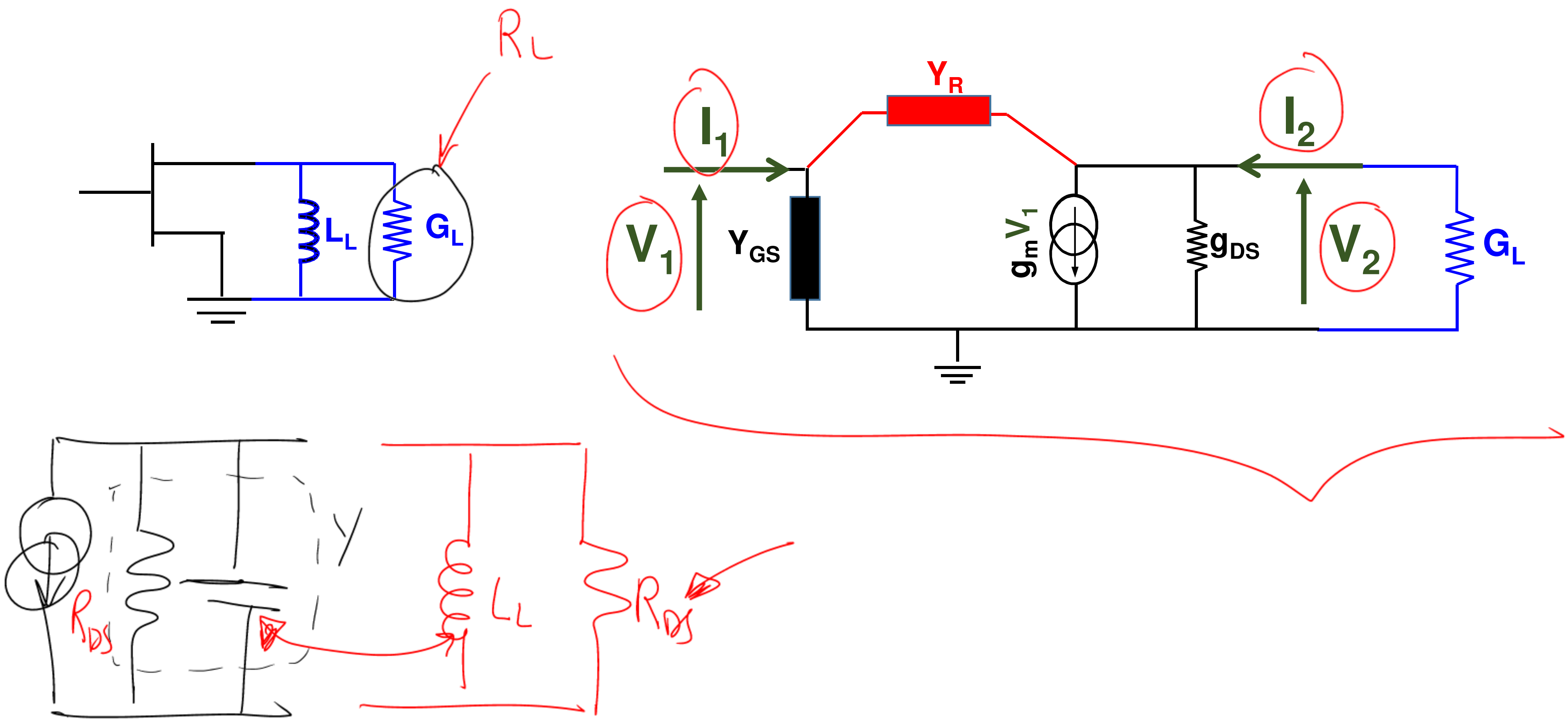
3) Miller Effect (Feedback admittance Y_R and conductance load G_L)





II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)



II – Intrinsic figures of merit for FETs

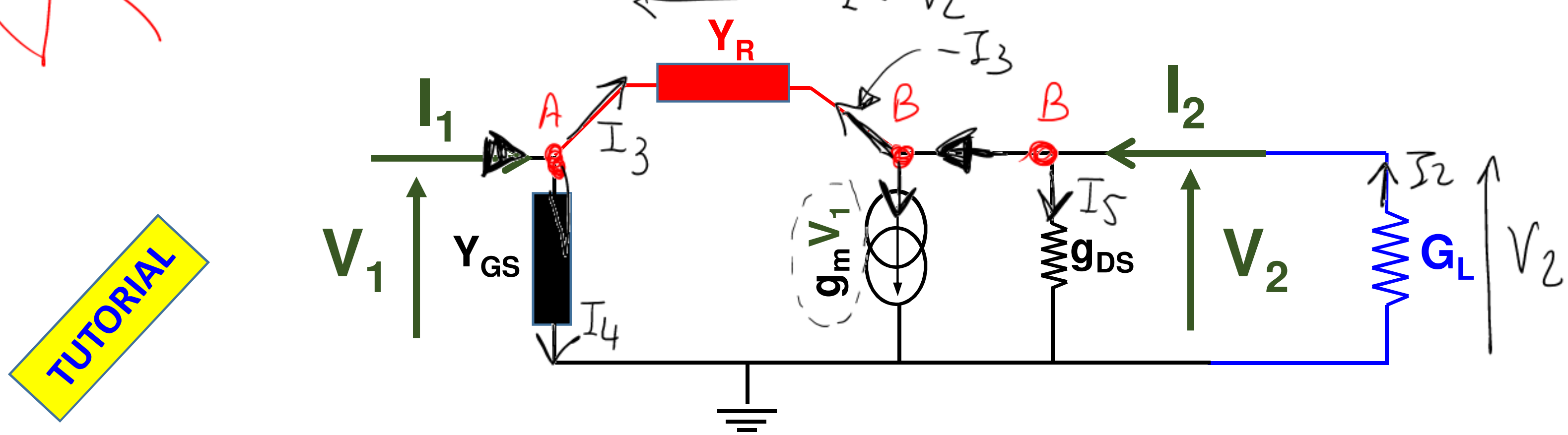
3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

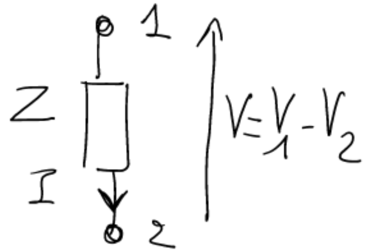
a) Voltage gain G_V

$$G_V = \frac{V_2}{V_1} = -\frac{g_m - Y_R}{g_{DS} + G_L + Y_R} \rightarrow -\frac{g_m}{g_{DS} + G_L} \rightarrow -\frac{g_m}{2g_{DS}}$$

G_{DS}

$V_A - V_B = V_1 - V_2$





$V = Z\, I$

$I = Y\, V$

(1) $I_1 = I_3 + I_4 = Y_R(V_1 - V_2) + Y_{GS} V_1$

(2) $I_2 = I_5 + g_m V_1 - I_3 = g_{DS} V_2 + g_m V_1 - Y_R(V_1 - V_2) = -G_L V_2$

(2) $\rightarrow V_2 \left[g_{DS} + Y_R + G_L \right] = \left(-g_m + Y_R \right) V_1$

$$\hookrightarrow \boxed{\frac{V_2}{V_1} = \frac{-g_m + Y_R}{g_{DS} + G_L + Y_R}} = -\frac{(g_m - Y_R)}{g_{DS} + G_L + Y_R}$$

$$Y_{IN} = \frac{I_1}{V_1}$$

II – Intrinsic figures of merit for FETs

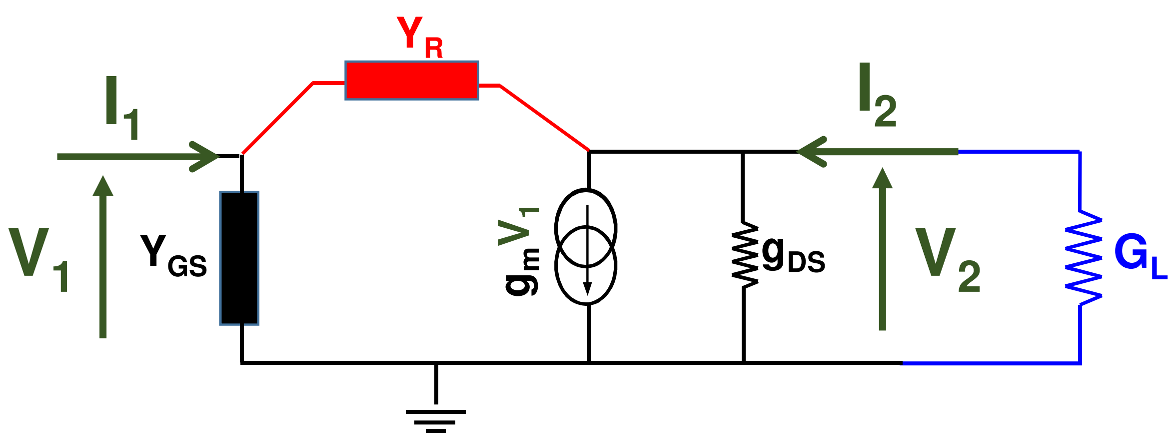
Gv negative

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

b) Input admittance Y_{IN}

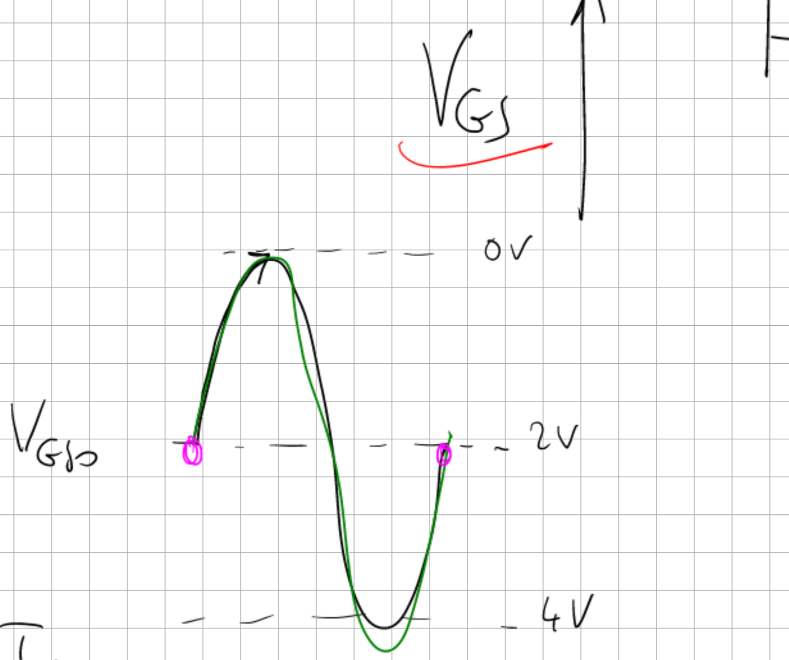
$$Y_{IN} = \frac{I_1}{V_1} = Y_{GS} + Y_R[1 - G_V]$$

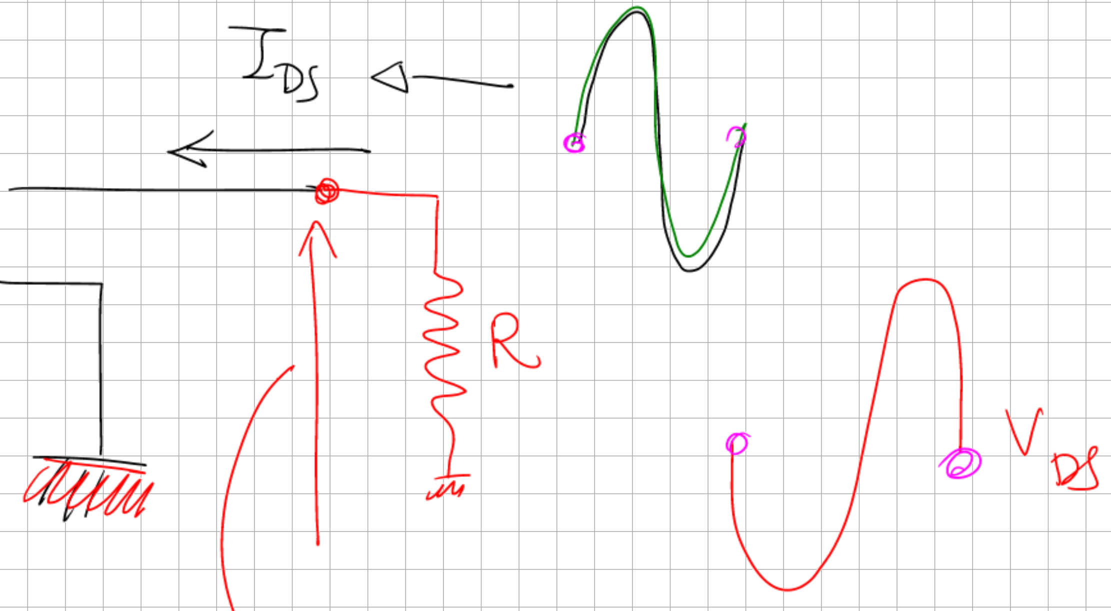
TUTORIAL



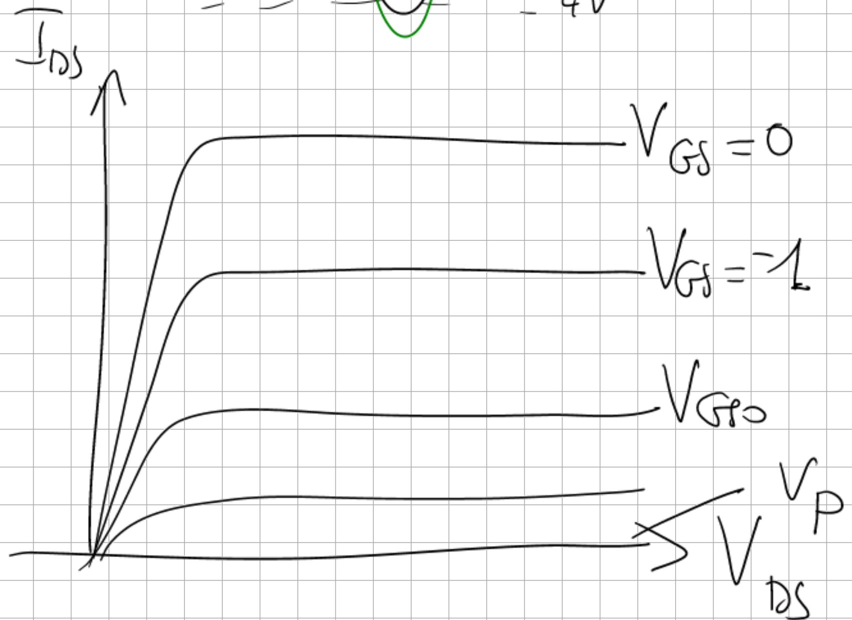
① $\underbrace{I_1 = Y_{GS} V_1 + Y_R (V_1 - V_2)}$ $\longrightarrow$ $Y_{IN} = \frac{I_1}{V_1} = Y_{GS} + Y_R(1 - G_V)$

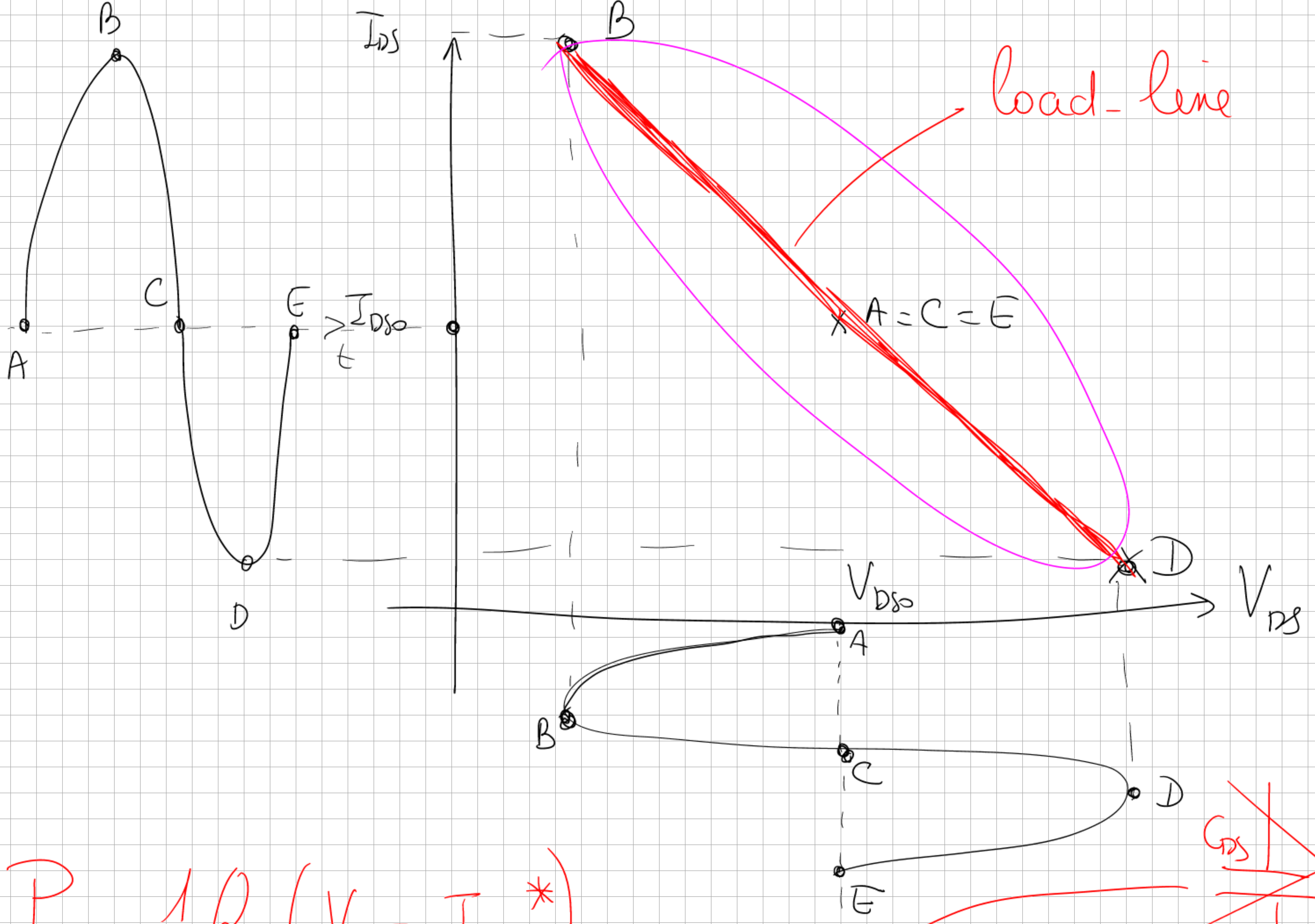
In the case of FETs, $|G_V| \gg 1$

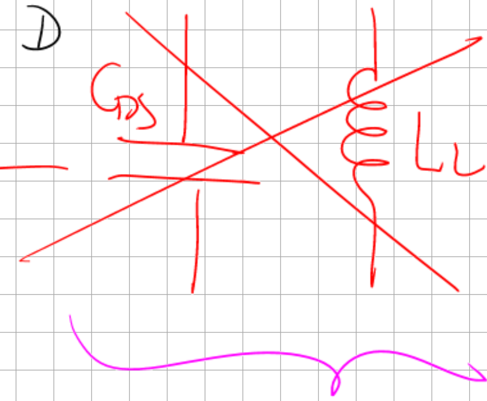




$$V_{DS} = - R I_{DS}$$







$$P_{OUT} = \frac{1}{2} Re\left(V_{OUT}\, I_{OUT}^{*}\right)$$

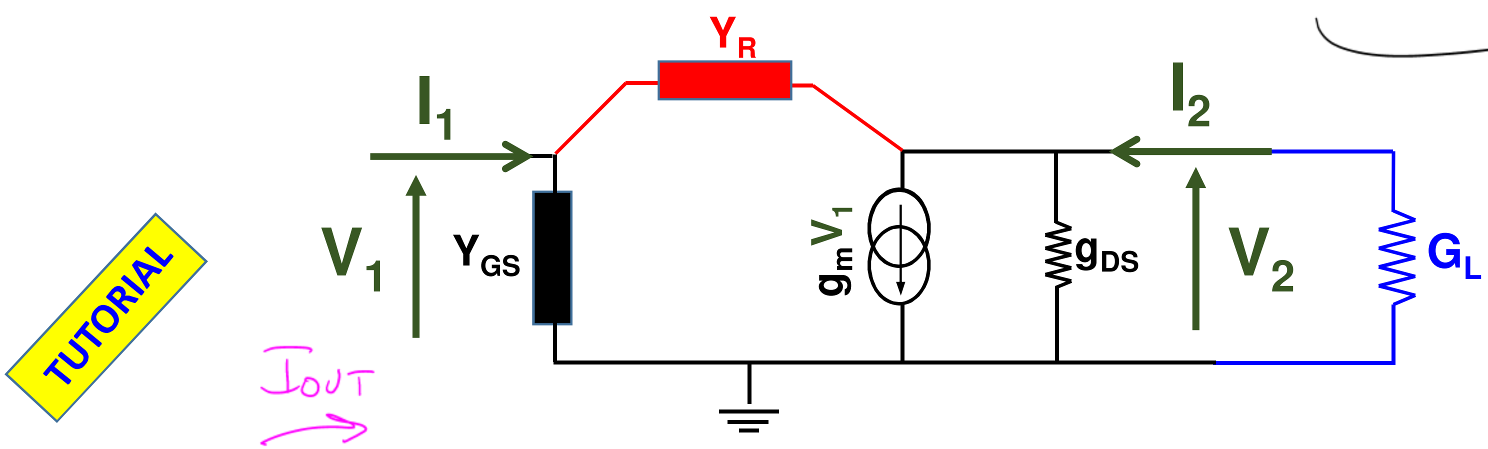
$$= \frac{1}{2}\, |V_{OUT}|\, |I_{OUT}| \cos\left(\varphi_{V_{OUT}} - \varphi_{I_{OUT}}\right)$$

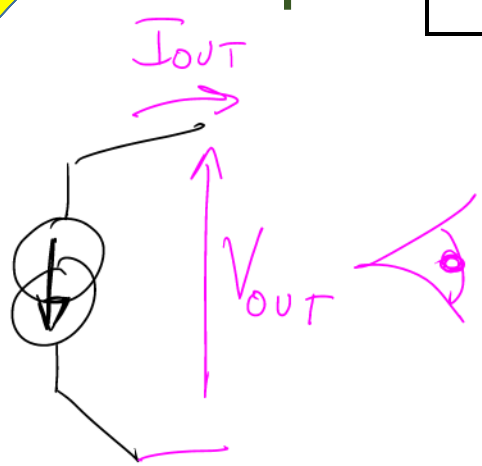
II – Intrinsic figures of merit for FETs

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

c) Output admittance seen by the drain current source Y_{OUT}

$$Y_{OUT} = \frac{-g_m V_1}{V_2} = g_{DS} + G_L + Y_R\left[1 - \frac{1}{G_V}\right]$$





$$Y_{OUT} = \frac{I_{OUT}}{V_{OUT}}$$

① $I_1 = Y_{GS} V_1 + Y_R (V_1 - V_2)$

② $I_2 = g_{DS} V_2 + \underbrace{g_m V_1} + Y_R (V_2 - V_1) = - G_L V_2$

$$Y_{OUT} = \frac{I_{OUT}}{V_{OUT}} = \frac{-g_m \cdot V_1}{V_2} = \frac{-g_m}{G_V} = \cancel{\frac{-g_m}{-\frac{g_m - Y_R}{g_{ds} + G_L + Y_R}}}$$

$$g_m V_1 = - g_{ds} \underset{\times}{V_2} - Y_R (\underset{\times}{V_2} - V_1) - G_L \underset{\times}{V_2}$$

$$Y_{OUT} = \frac{-g_m V_1}{V_2} = g_{DS} + Y_R \left(1 - \frac{V_1}{V_2}\right) + G_L$$

$$Y_{OUT} = g_{DS} + G_L + Y_R \left(1 - \frac{1}{G_V}\right)$$

II – Intrinsic figures of merit for FETs

$G_V<0$ and $|G_V|>>1$

3) Miller Effect (Feedback admittance Y_R and conductance load G_L)

b) Input admittance Y_{IN}

$$Y_{IN} = Y_{GS} + Y_R[1 - G_V] \rightarrow \boxed{Y_{GS} + Y_R|G_V|}$$

c) Output admittance seen by the drain current source Y_{OUT}

$$Y_{\cancel{OUT}\ DS} = g_{DS} + G_L + Y_R\left[1 - \frac{1}{G_V}\right] \rightarrow \boxed{g_{DS} + G_L + Y_R}$$

$$1 - \frac{1}{G_V} = 1 + \frac{1}{|G_V|} \rightarrow 1$$

$$1 - G_V = 1 + |G_V| \rightarrow |G_V|$$

because $G_V<0$

$|G_V|>>1$

$j C_{GD}\,\omega$

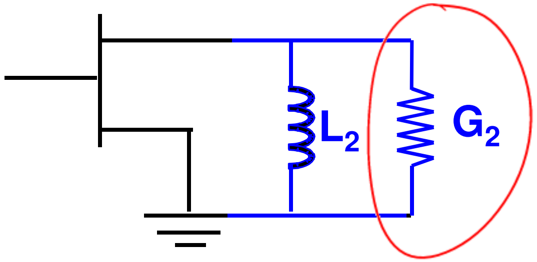
II – Intrinsic figures of merit for FETs

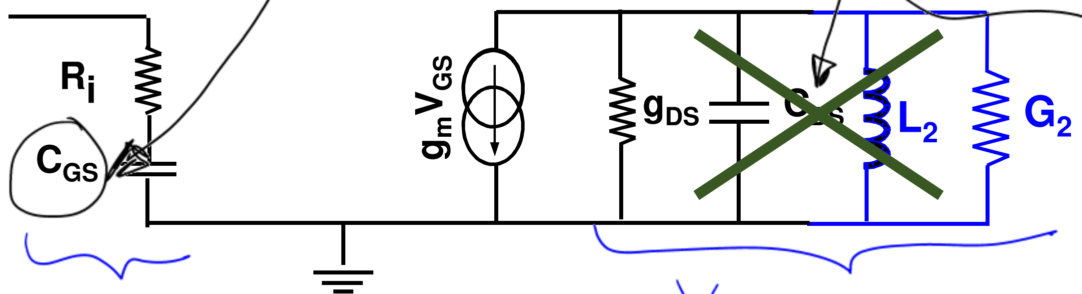
3) Maximum Power Gain $\mathbf{G_{MAX}}$ → Simplified Electrical Small-Signal FET Model

$$C_{GS} = C_{GS} + |G_V|\,C_{gd}$$

$$L_2\, C_{DS}\,\omega^2 = 1 \;\rightarrow\; \boxed{L_2 = \frac{1}{C_{DS}\,\omega^2}}$$

$$C_{DS} = C_{DS} + C_{GD}$$





$$Y_R = j\,C_{GD}\,\omega$$

$$Y_{IN} = Y_{GS}$$

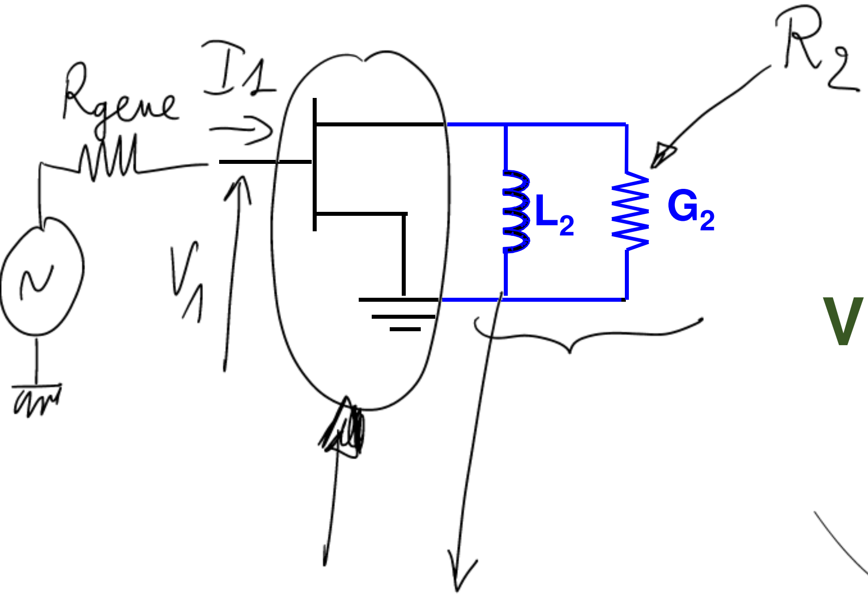
$$Y_{OUT} = g_{DS} + G_2$$

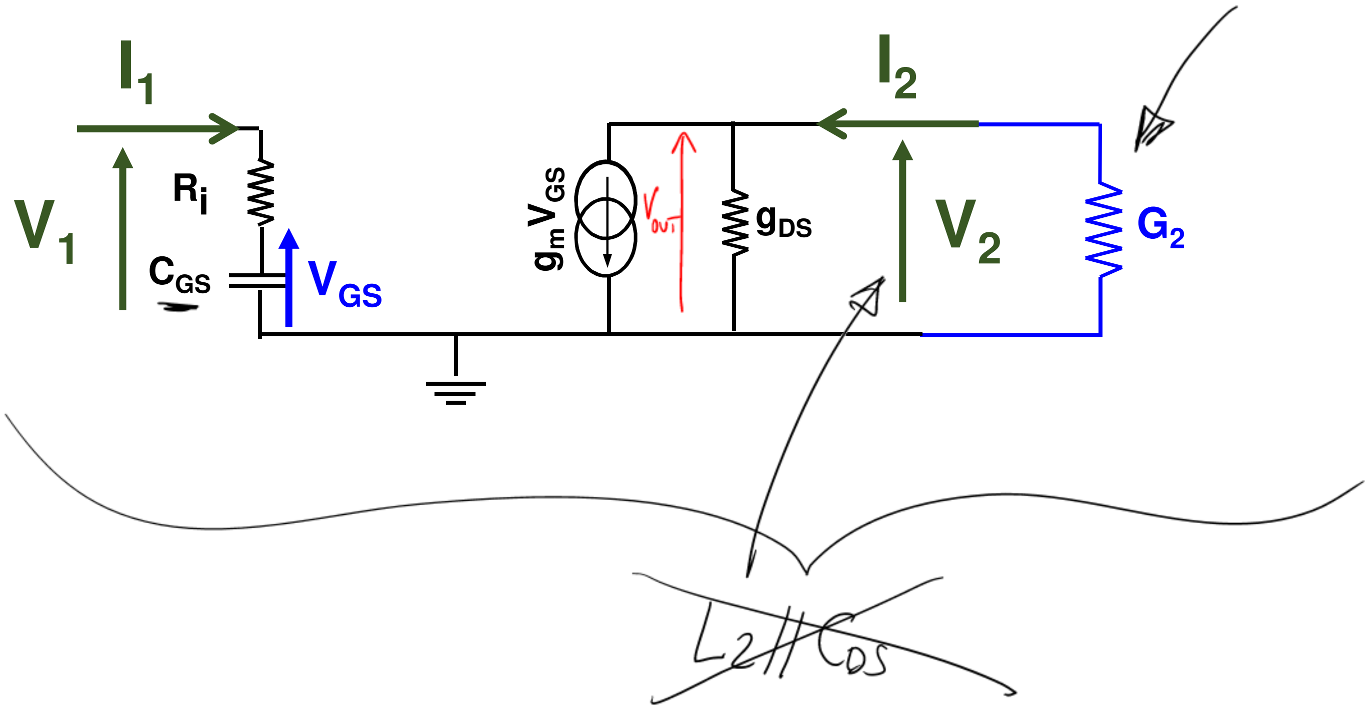
$$Y_{IN} = \frac{1}{R_{IN}} + \underbrace{j\,C_{gs}\,\omega + j\,|G_V|\,C_{GD}\,\omega}_{j\,C_{eq}\,\omega}$$

where $C_{eq} = C_{gs} + |G_V|\,C_{gd}$

II – Intrinsic figures of merit for FETs

3) Maximum Power Gain G_{MAX} → Simplified Electrical Small-Signal FET Model



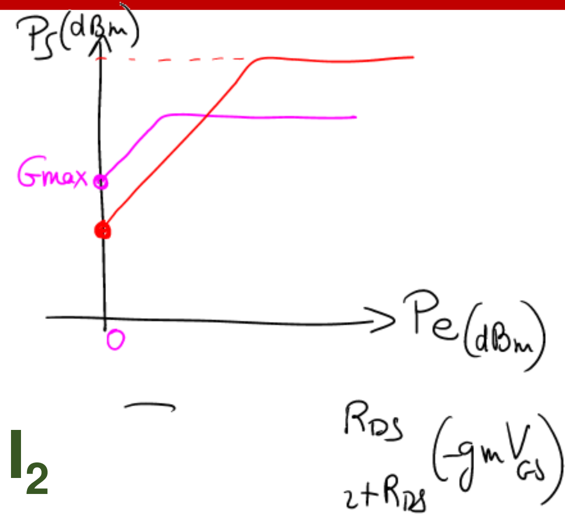


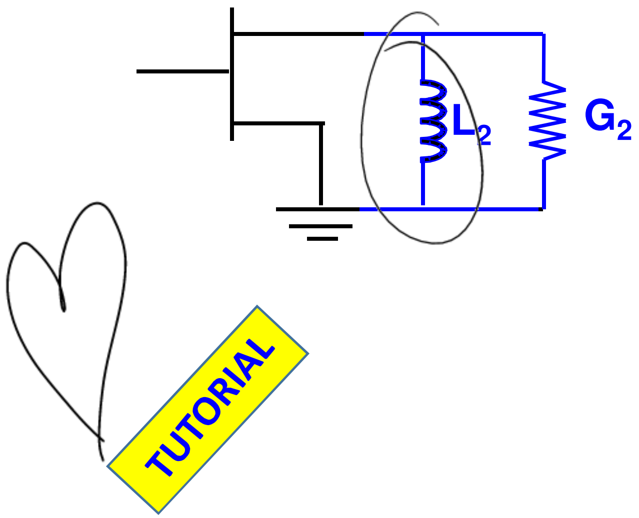
$$\boxed{L_2 = \frac{1}{C_{DS}\,\omega^2}}$$

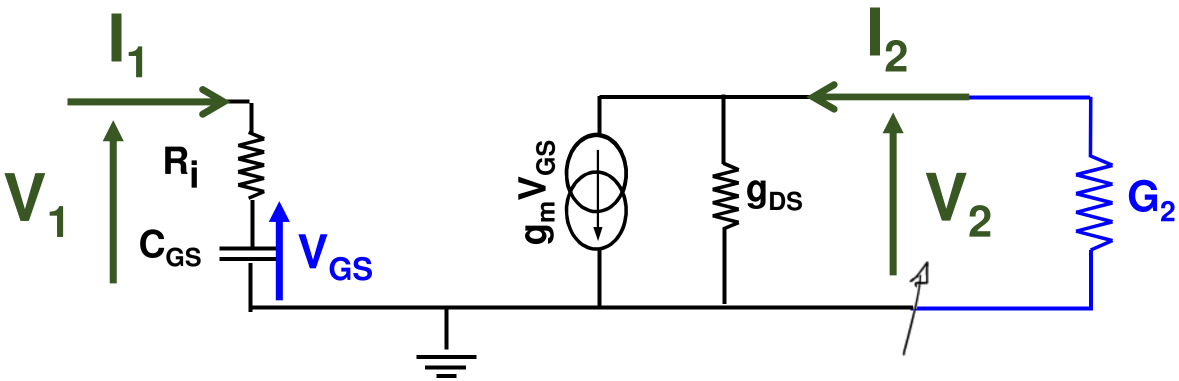
II – Intrinsic figures of merit for FETs

3) Maximum Power Gain G_{MAX} → Simplified Electrical Small-Signal FET Model

1 $R_L = R_{DS}$ or $R_2 = R_{opt}$ 2







General case $(G_2 \neq g_{DS})$ → Not maximum Power Gain G_P

$$G_P = \frac{\dfrac{G_2}{[G_2 + g_{DS}]^2}\, g_m^2}{R_i\, C_{GS}^2\, \omega^2}$$

$$P_{IN} = \frac{1}{2} Re(V_1 I_1^*)$$

$$P_{OUT} = \frac{1}{2} Re(V_{OUT} I_{OUT}^*)$$

Calculation of Input Power

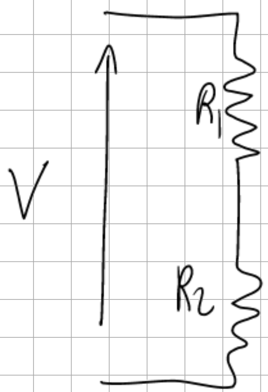
$$I_1 = j C_{gs}\omega \times V_{GS}$$

$$V_1 = \left(R_i + \frac{1}{jC_{gs}\omega}\right) I_1$$

$$\mathrm{Re}\left(V_1 I_1^*\right) = \mathrm{Re}\left[\left(R_i + \frac{1}{jC_{gs}\omega}\right)\underbrace{I_1 I_1^*}_{|I_1|^2}\right] = \underbrace{|I_1|^2}\,\mathrm{Re}\left(R_i + \frac{1}{jC_{gs}\omega}\right)$$

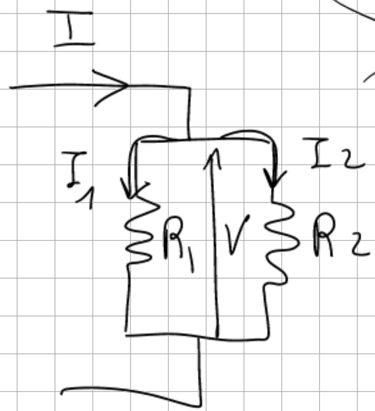
$$= R_i\,|I_1|^2 = R_i\left|jC_{gs}\omega V_{gs}\right|^2$$

$$\boxed{P_{IN} = \frac{1}{2} R_i C_{gs}^2 \omega^2 |V_{GS}|^2}$$



$$V_2 = \left(\frac{R_2}{R_1+R_2}\right) V$$

Voltage Divider



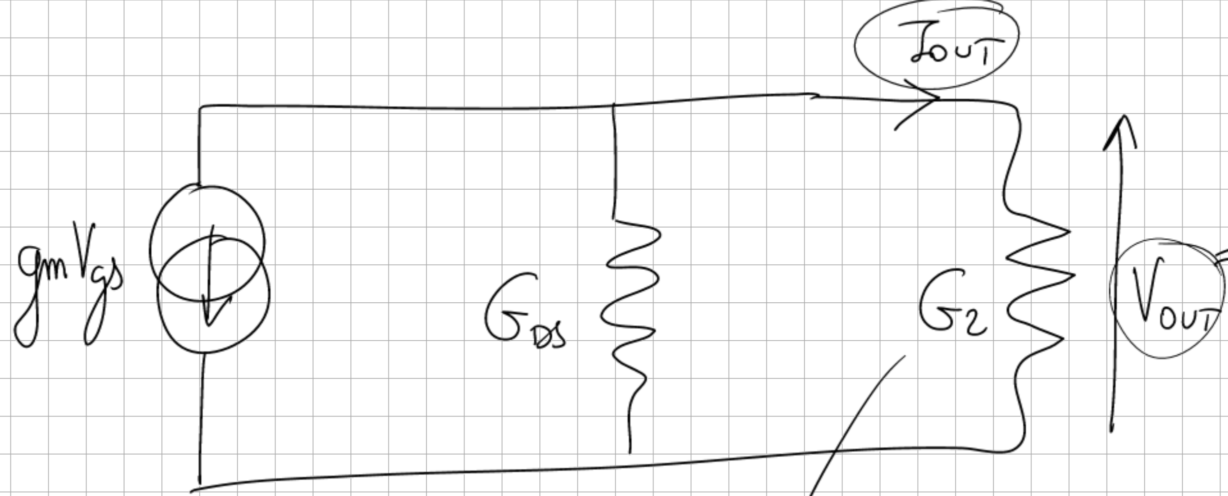
$$I = I_1 + I_2$$

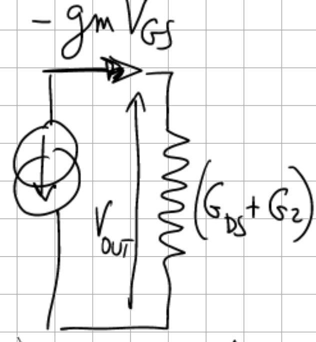
$$I_1 = \frac{V}{R_1} \quad \& \quad I_2 = \frac{V}{R_2} = \frac{\left(\frac{R_1R_2}{R_1+R_2}\right) I}{R_2}$$

$$I = \frac{V(R_1+R_2)}{R_1R_2}$$

$$I_2 = \left(\frac{R_1}{R_1+R_2}\right) I$$

Current divider





$$P_{OUT} = \frac{1}{2} Re\left(V_{OUT}\, I_{OUT}^*\right)$$

$$I_{OUT} = G_2 V_{OUT}$$

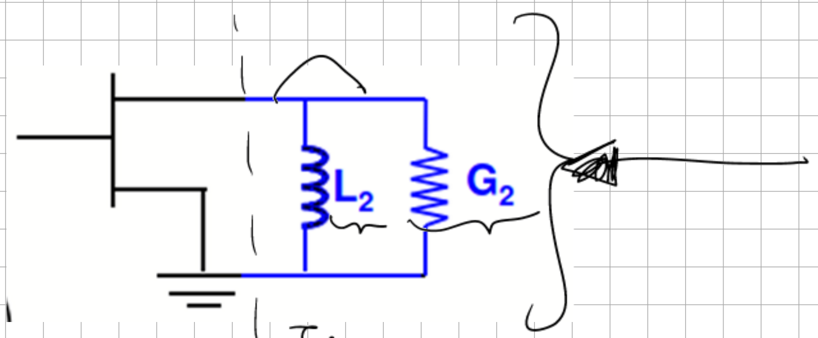
$$V_{OUT}\,(V_{gs})$$

$$= \frac{1}{2} Re\left(V_{OUT}\,(G_2 V_{OUT})^*\right)$$

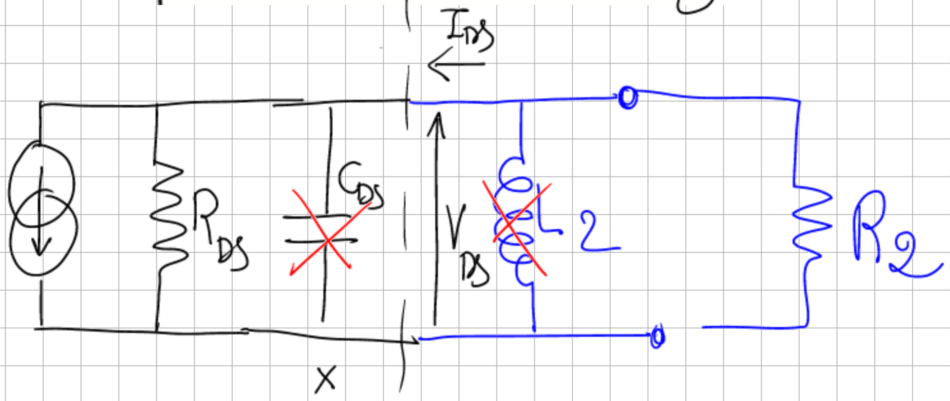
$$= \frac{1}{2} Re\left(\underbrace{V_{OUT}\, V_{OUT}^*}_{|V_{OUT}|^2}\ \underbrace{G_2^*}_{G_2}\right)$$

$$V_{OUT} = \frac{-g_m V_{GS}}{G_2 + G_{DS}}$$

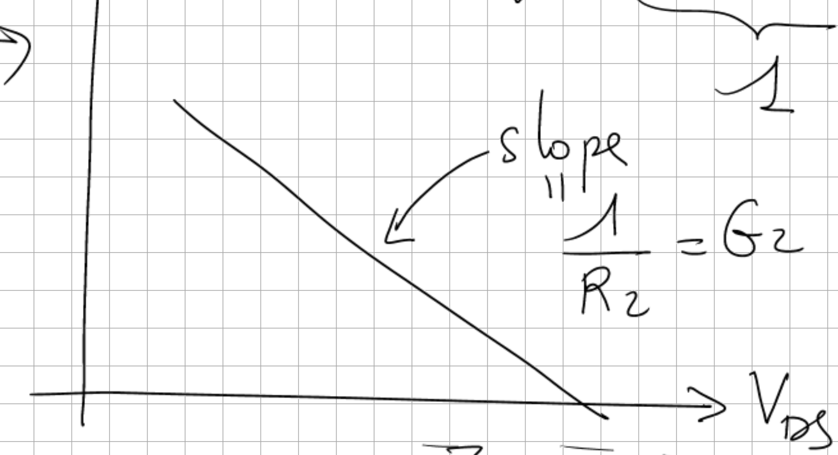
$$\boxed{P_{OUT}} = \frac{1}{2} G_2 \left|V_{OUT}\right|^2 = \frac{1}{2} G_2 \left|\frac{-g_m V_{gs}}{G_2 + G_{DS}}\right|^2 = \boxed{\frac{1}{2}\,\frac{G_2}{(G_2+G_{DS})^2}\, g_m^2 \left|V_{GS}\right|^2}$$



$$G_P = \frac{\frac{G_2}{[G_2 + g_{DS}]^2}\, g_m^2}{R_i\, C_{GS}^2\, \omega^2}$$



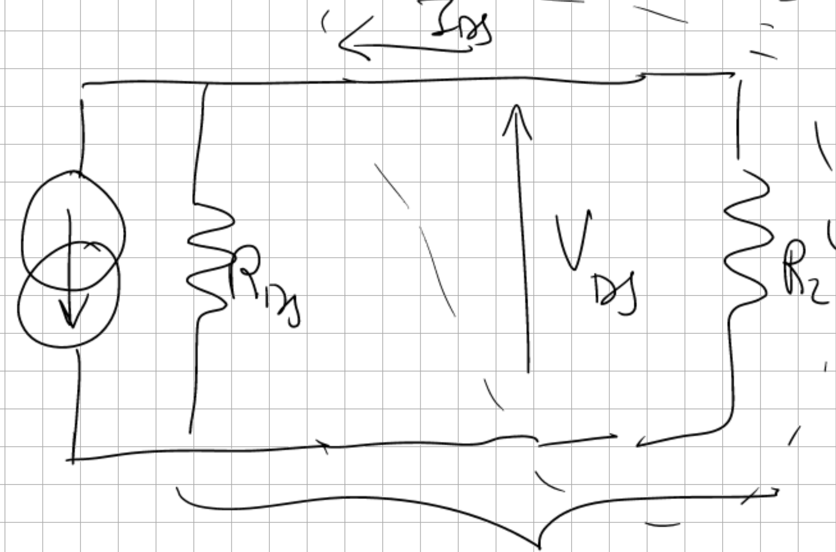
$$P_{OUT} = \frac{1}{2}\, \underbrace{|V_{OUT}|\,|I_{OUT}|}\; \underbrace{\cos(\varphi_{V_{OUT}} - \varphi_{I_{OUT}})}_{1}$$

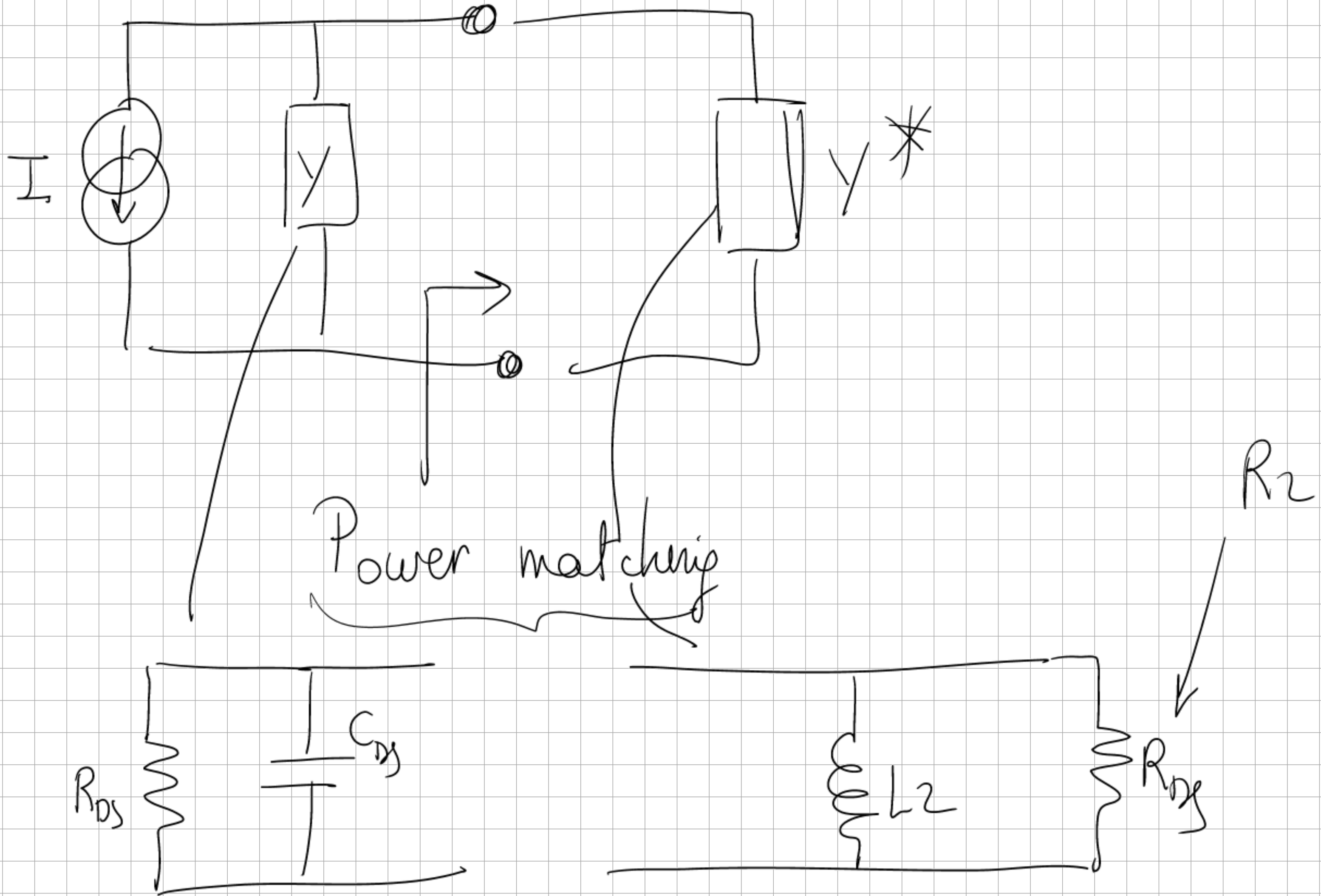


$$Y_{C_{DS}} = j\, C_{DS}\, \omega_0 \qquad Y_{L_2} = \frac{-j}{L_2\, \omega_0}$$

$$Y_{C_{DS}} + Y_{L_2} = 0 \quad \text{(compensation)}$$

$$C_{DS}\, \omega_0 = \frac{1}{L_2\, \omega_0} \Longrightarrow \boxed{L_2 = \frac{1}{C_{DS}\, \omega_0^2}}$$





maximum power gain $\Longrightarrow G_{max} \quad (R_2 = R_{DS}$

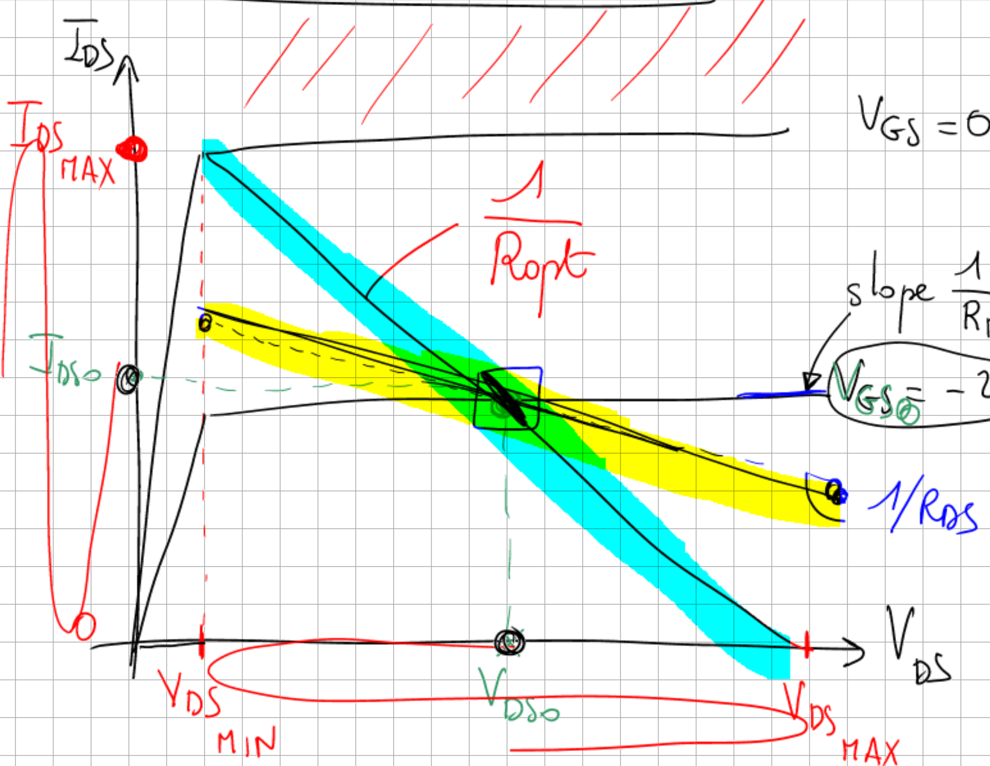
$G_2 = G_{DS})$

$$\boxed{G_{max} = \frac{R_{DS}\, g_m^2}{4 R_i C_{gs}^2 \omega_0^2}}$$

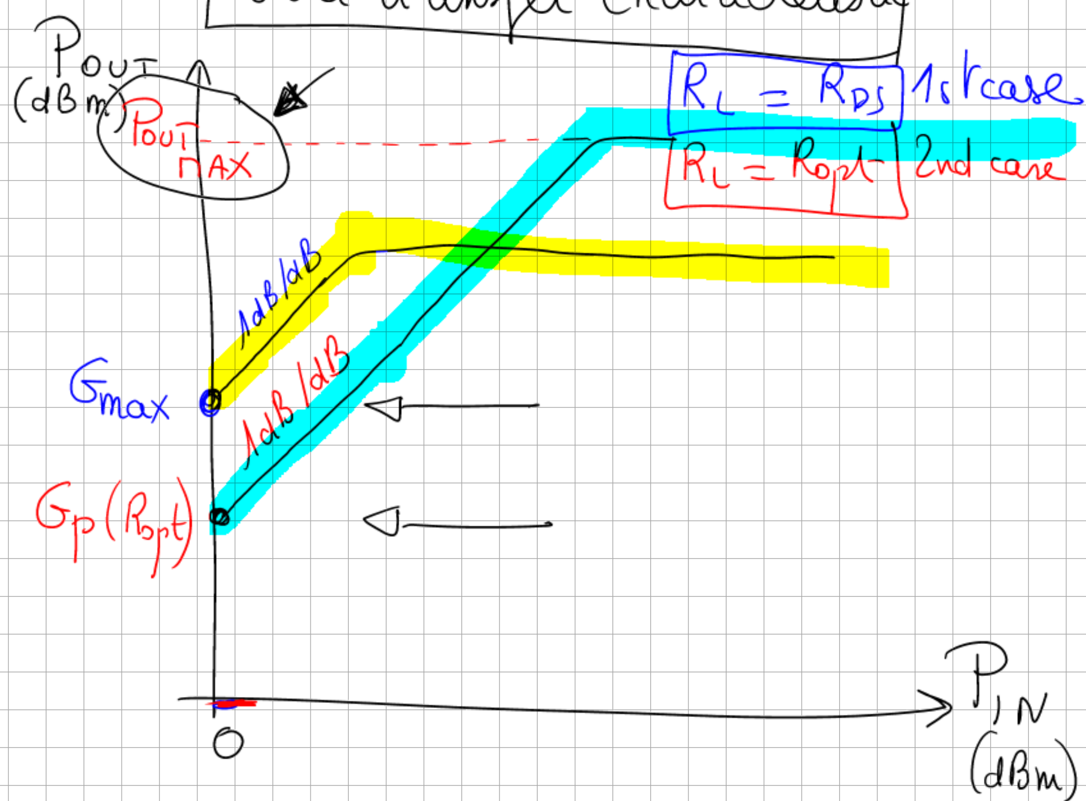
Difference between (Maximum power gain) and (Maximum output power)

$R_L = R_{DS}$ $\qquad$ $R_L = R_{opt}$

I-V characteristic



Power transfer characteristic

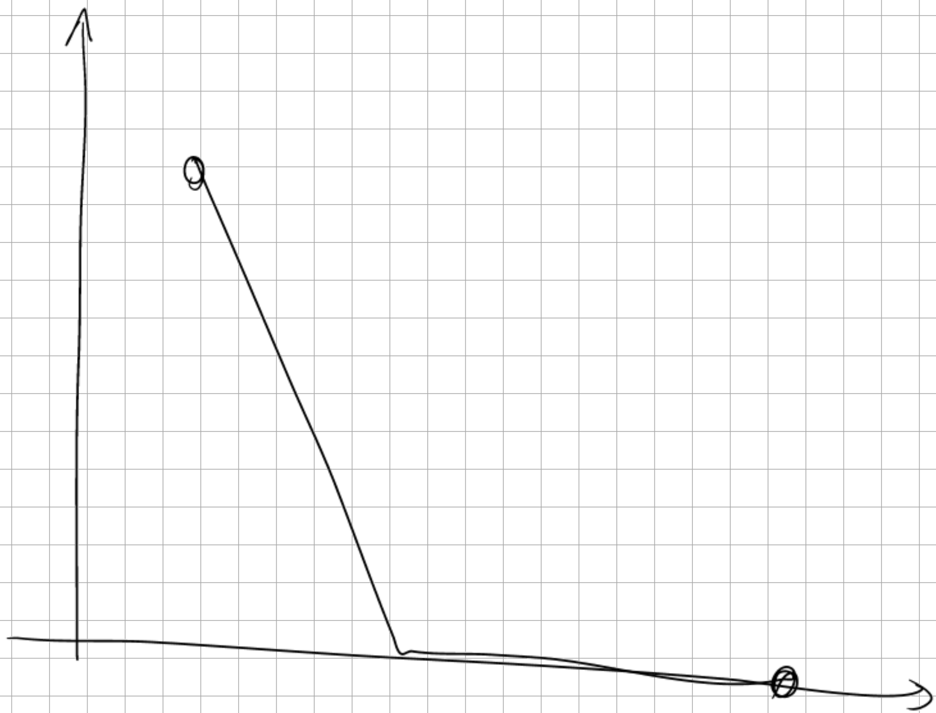


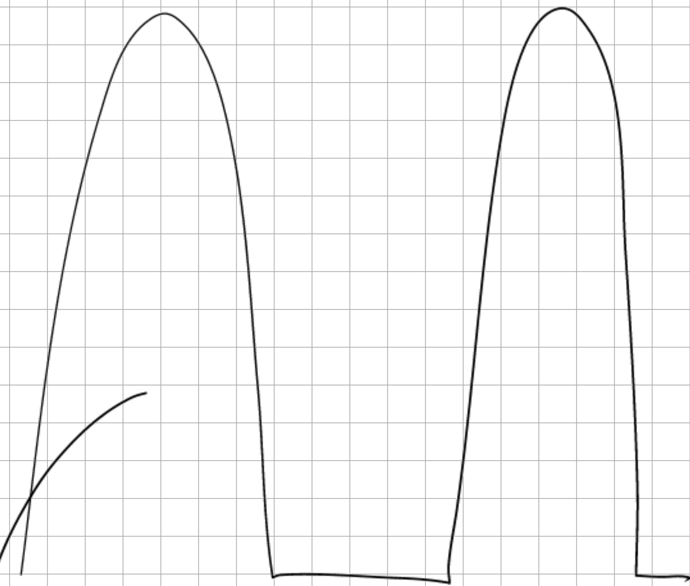
$$P_{OUT_{MAX}} \text{ (A class)} = \frac{1}{2} Re(VI^*) = \frac{1}{2} |V| \, |I| \underbrace{\cos(\varphi_V - \varphi_I)}_{1}$$

$$\boxed{P_{MAX} = \frac{1}{2} \times \frac{V_{DS_{MAX}} - V_{DS_{MIN}}}{2} \times \frac{I_{DS_{MAX}}}{2}}$$

$$R_{opt} = \frac{V_{DS_{MAX}} - V_{DS_{MIN}}}{I_{DS_{MAX}}}$$

Class A





$$I_{DS0} + \underline{\underline{I_{DS1}}} \cos(\omega_0 t + \varphi_1) + I_{DS2} \cos(2\omega_0 t + \ldots)$$

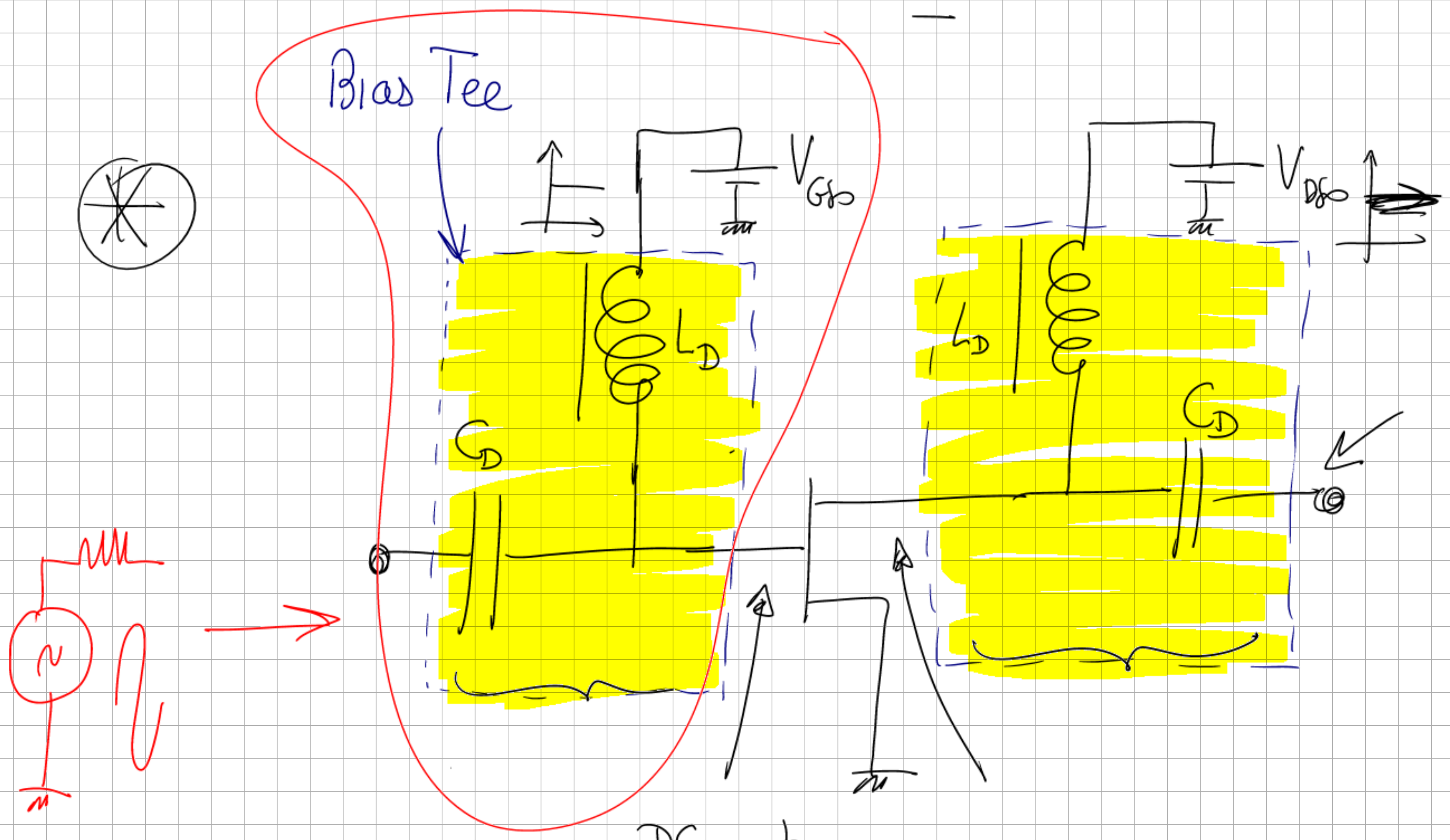
$$V_{DS} = V_{DS0} + \underline{\underline{V_{DS1}}} \cos(\omega_0 t + \varphi_1)$$

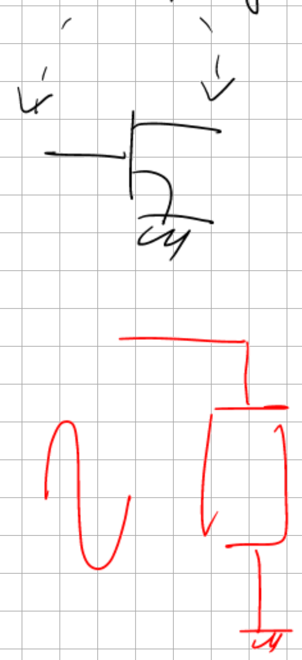
$$R_{opt_{AB}} \sim R_{opt_A}$$

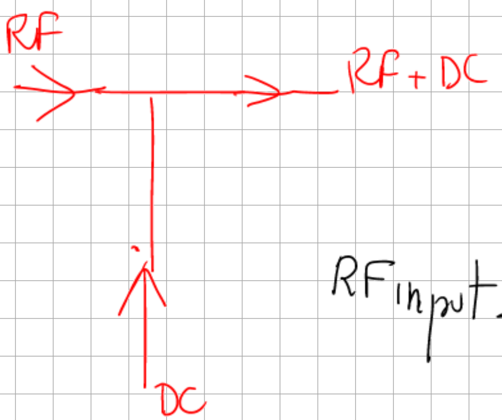
$$R_{opt_B} = \frac{V_{DS1}}{I_{DS1}} = \underbrace{R_{opt_A}}$$

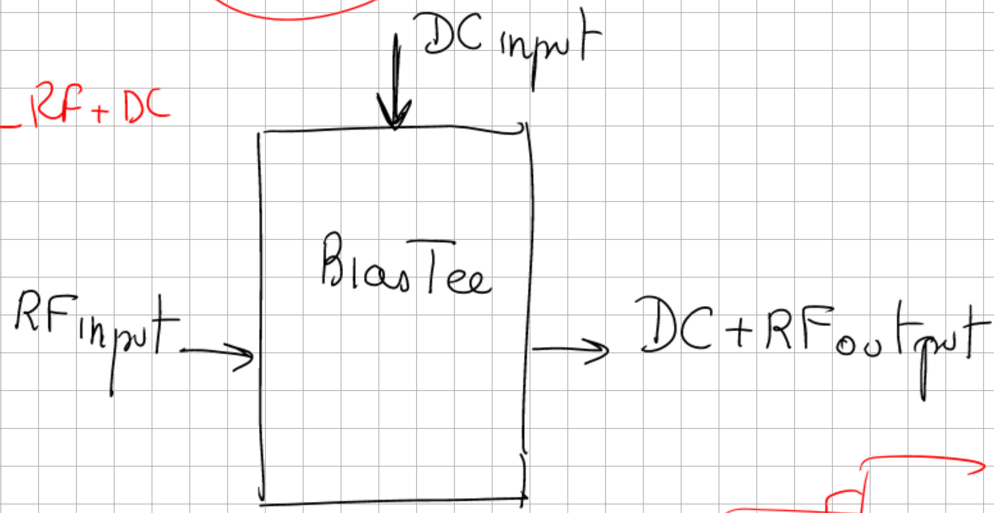
easy to calculate

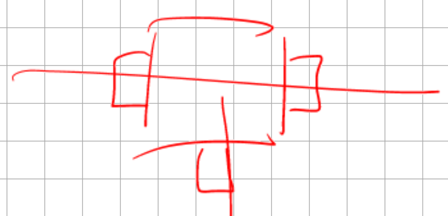
L_D & C_D = Decoupling values

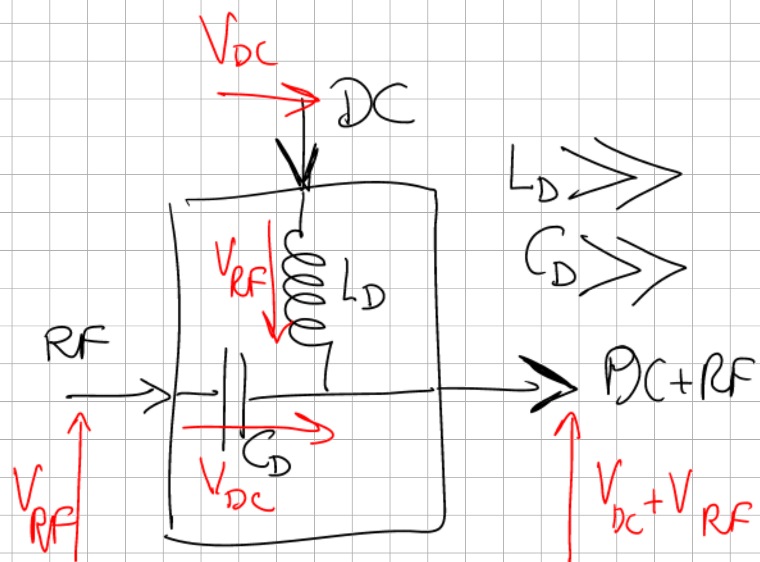


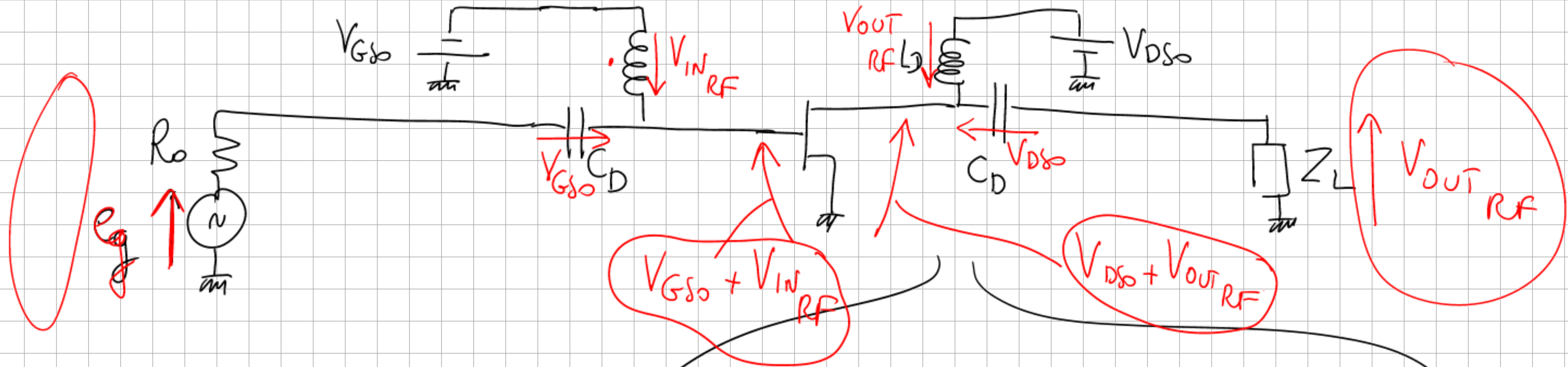








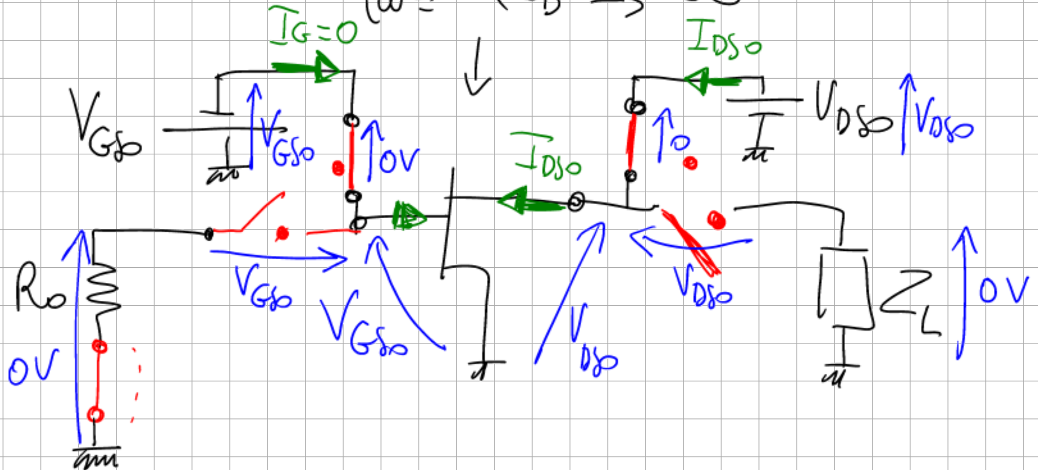


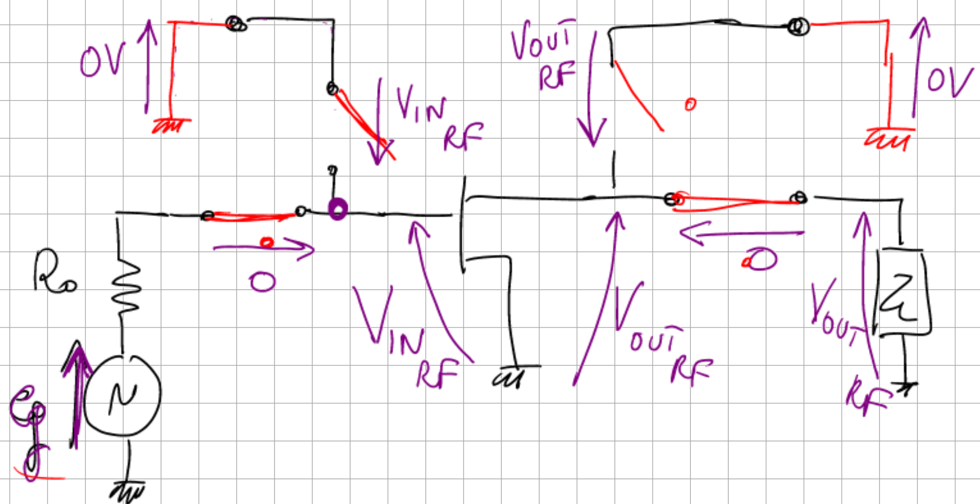


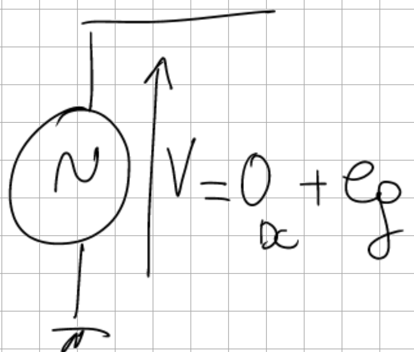
equivalent DC $\begin{pmatrix} L_D \rightarrow SC \\ C_D \rightarrow OC \end{pmatrix}$ $(\omega =$

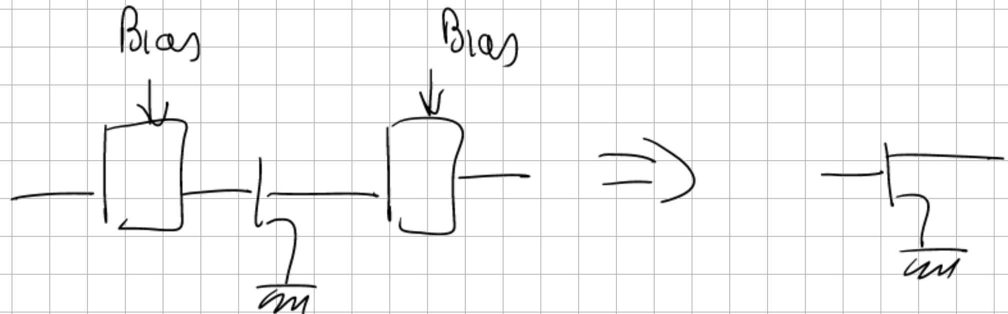
$\oplus$

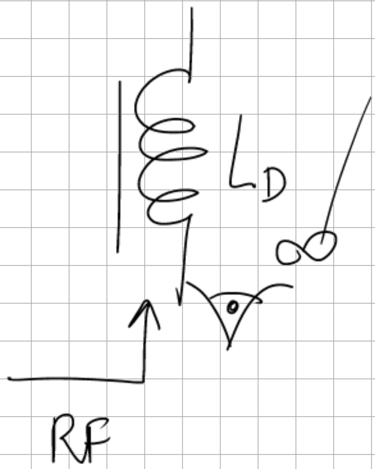
equivalent RF $\begin{pmatrix} L_D \rightarrow OC \\ C_D \rightarrow SC \end{pmatrix}$

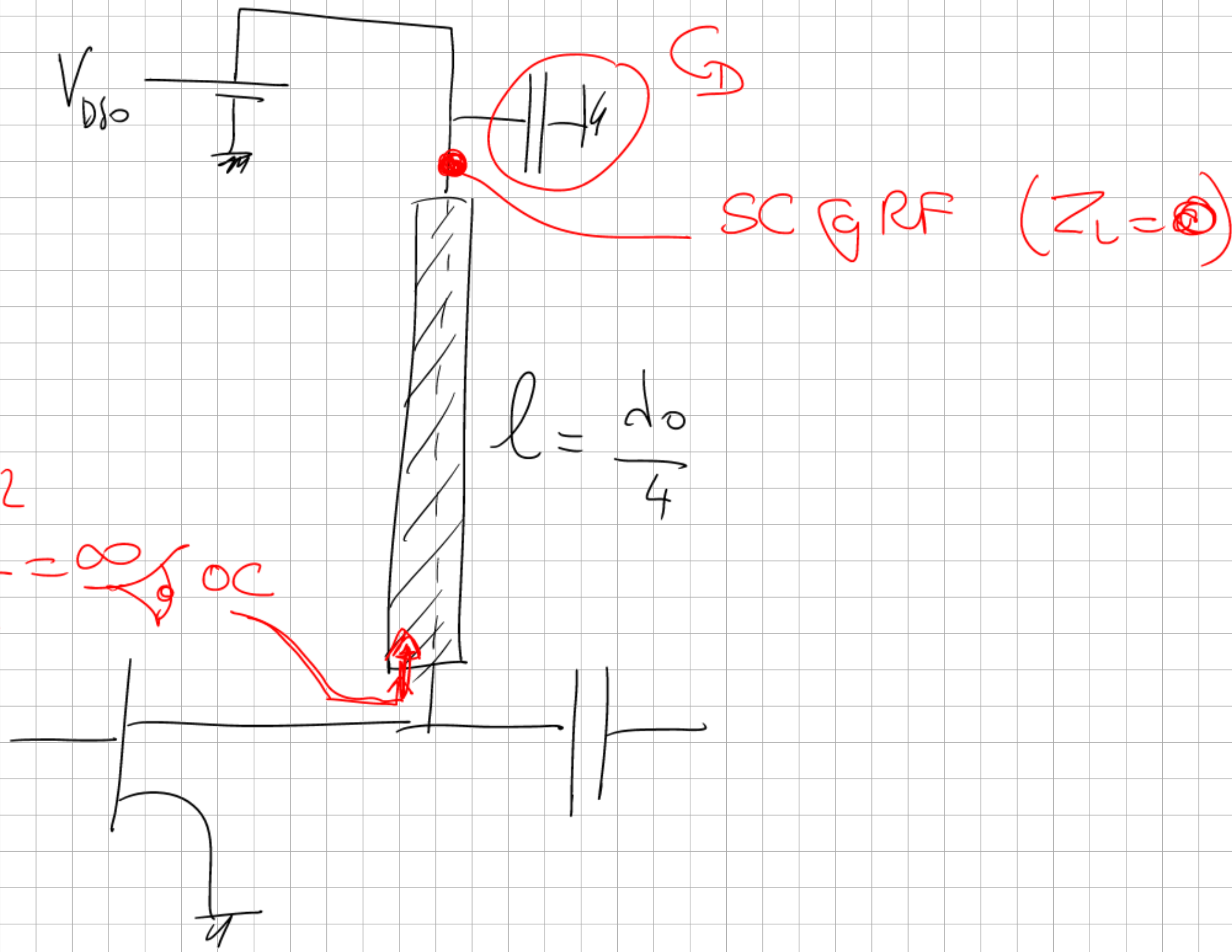




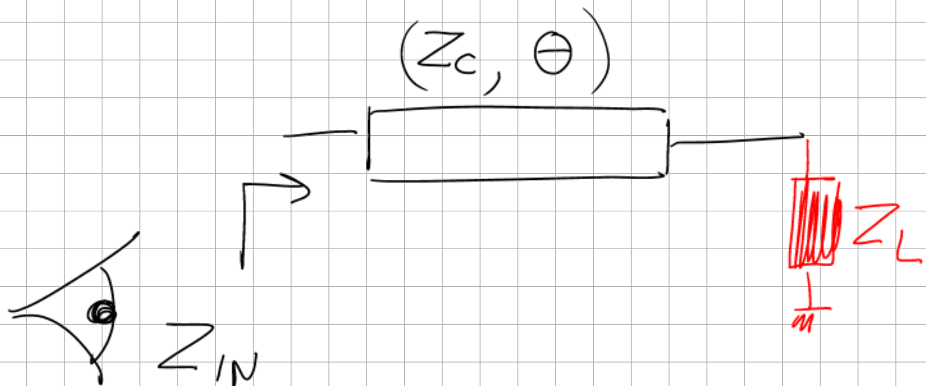




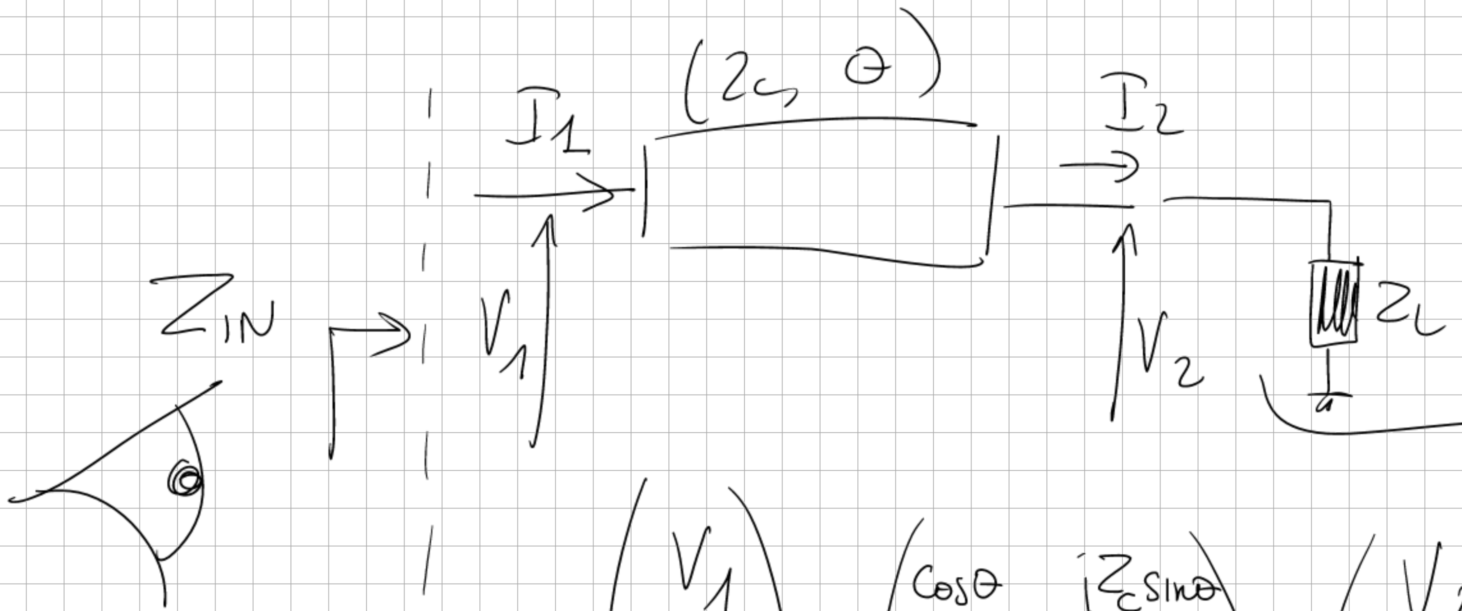




$$Z_{IN} = \frac{Z_c^2}{Z_L} = \infty \quad OC$$



$Z_{IN} =$



$\theta = d\beta$

$V_2 = Z_L \times I_2$

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} \cos\theta & jZ_c \sin\theta \\ j\dfrac{\sin\theta}{Z_c} & \cos\theta \end{pmatrix} \begin{pmatrix} V_2 \\ I_2 \end{pmatrix}$$

$$Z_{IN} = \frac{V_1}{I_1} = \frac{\cos\theta \overbrace{V_2}^{Z_L I_2} + jZ_c \sin\theta \, I_2}{j\dfrac{\sin\theta}{Z_c} V_2 + \cos\theta \, I_2} = \frac{Z_L \cos\theta + jZ_c \sin\theta}{j\dfrac{\sin\theta}{Z_c} Z_L + \cos\theta}$$

$$\boxed{Z_{IN} = Z_c \frac{Z_L \cos\theta + jZ_c \sin\theta}{Z_c \cos\theta + jZ_L \sin\theta}}$$

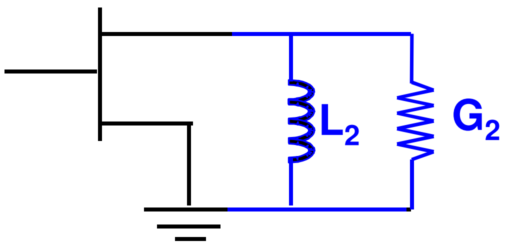
if $\ell = \frac{d_0}{4} \rightarrow \theta = 2\pi \frac{\ell}{d_0} = 2\pi \frac{d_0/4}{d_0} = \frac{\pi}{2}$

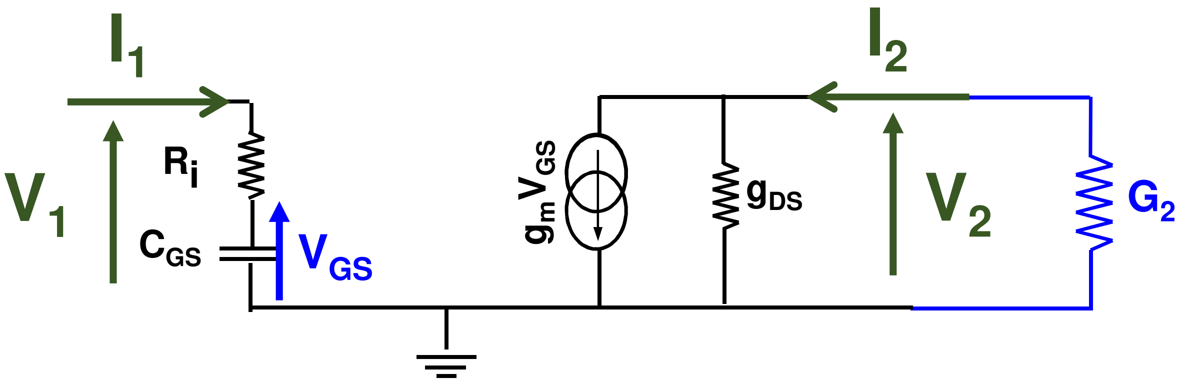
$\rightarrow Z_{IN} = \frac{Z_c^2}{Z_L}$

if $\ell = \frac{d_0}{2} \rightarrow \theta = \pi \rightarrow Z_{IN} = Z_L$

II – Intrinsic figures of merit for FETs

3) Maximum Power Gain G_{MAX} → Simplified Electrical Small-Signal FET Model





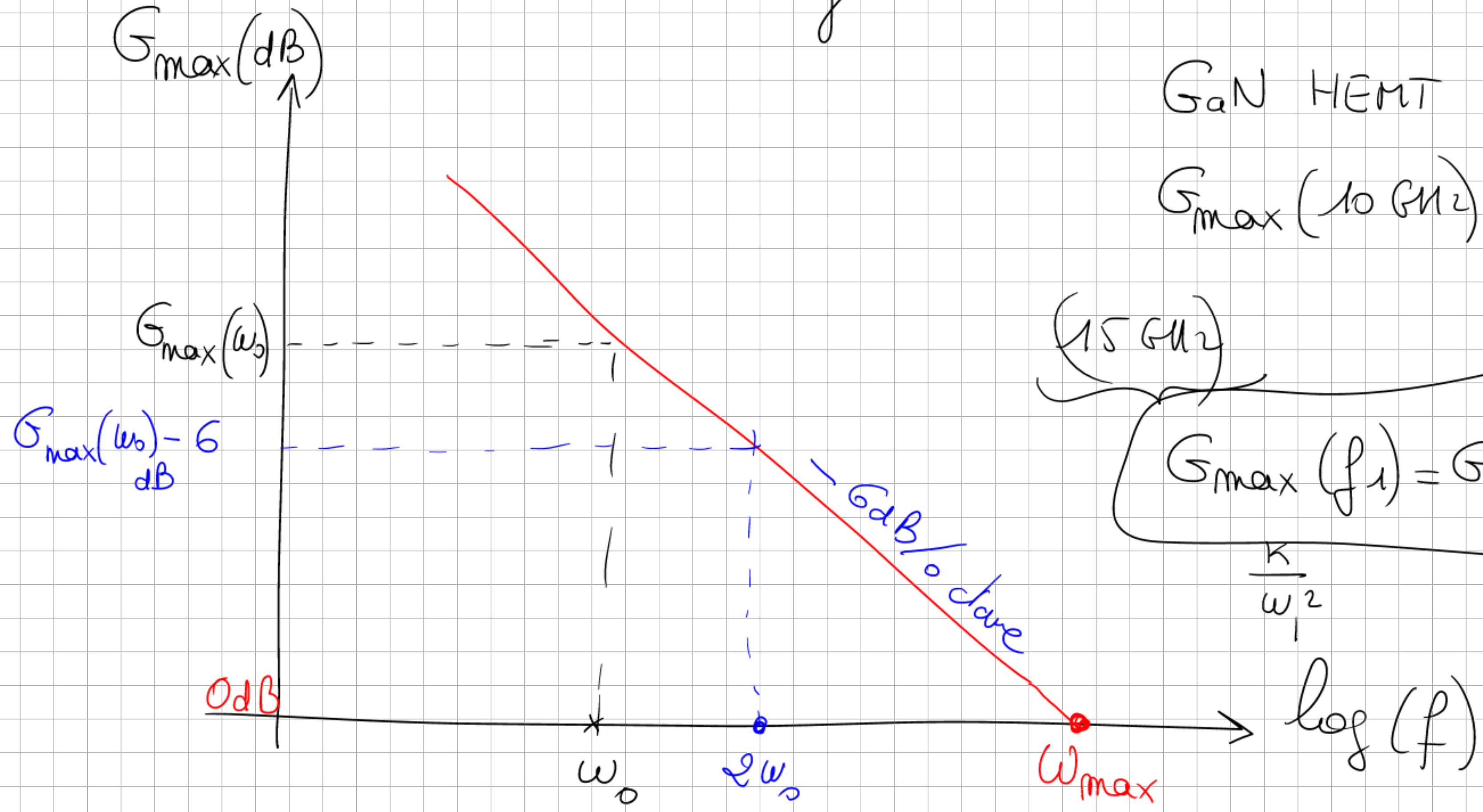
TUTORIAL

Optimum case $(G_2 = g_{DS})$ → Not maximum Power Gain G_{max}

$$\boxed{G_{max} = \frac{g_m^2}{4\, g_{DS}\, R_i\, C_{GS}^2\, \omega^2}}$$

*

$$G_{max} = \frac{g_m^2 \, R_{DS}}{4 R_i \, C_{gs}^2 \, \omega^2} = \frac{K = C^{st}}{\omega^2}$$



GaN HEMT (US Northrup)

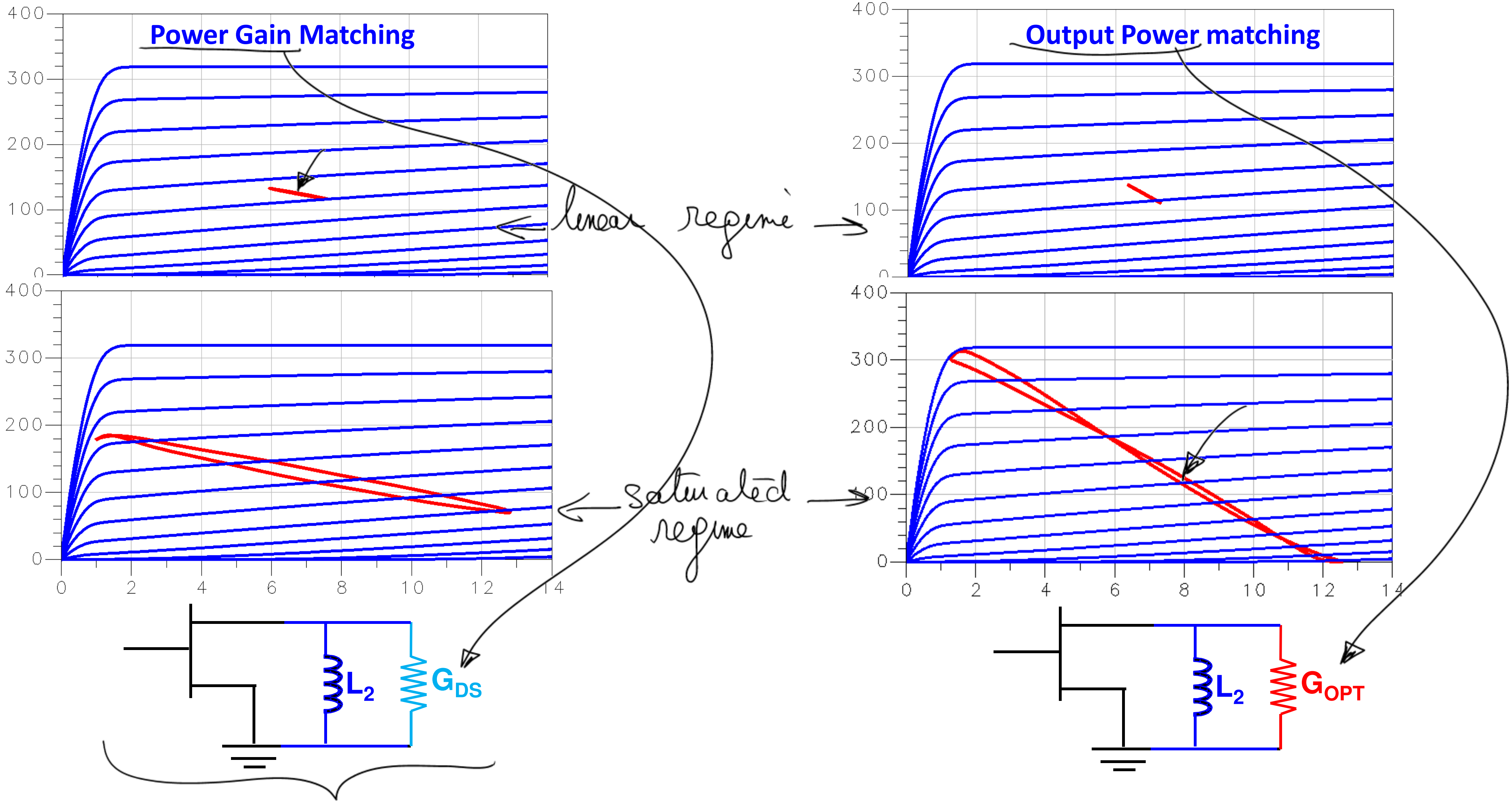
$G_{max}(10\ \text{GHz}) = 20\ \text{dB}$
$= 100$

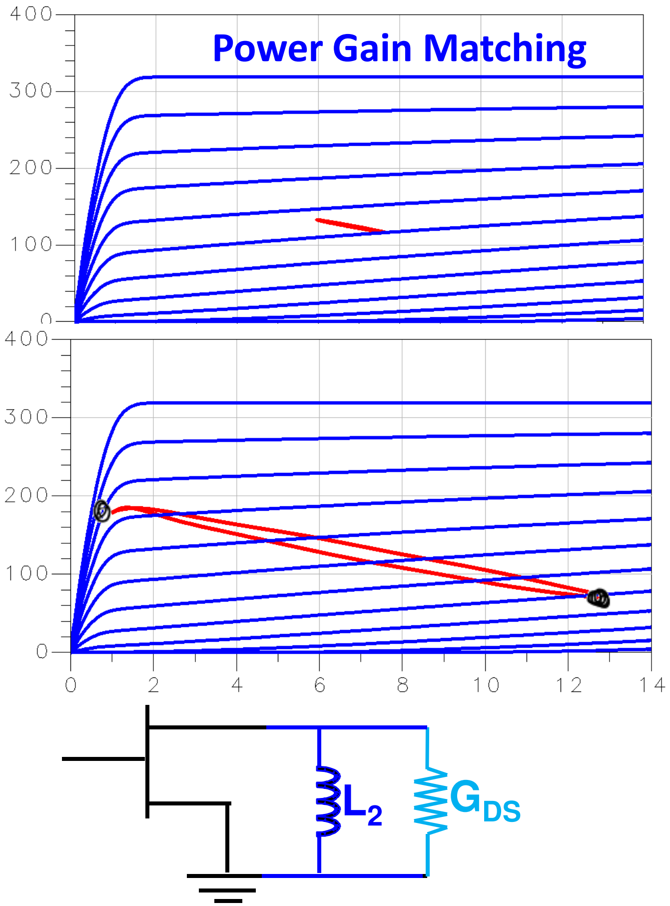
$$\overbrace{\boxed{\underbrace{G_{max}(f_1)}_{\frac{K}{\omega_1^2}} = \underbrace{G_{max}(f_2)}_{\frac{K}{\omega_2^2}} \times \left(\frac{f_2}{f_1}\right)^2}}^{(15\ \text{GHz})}$$

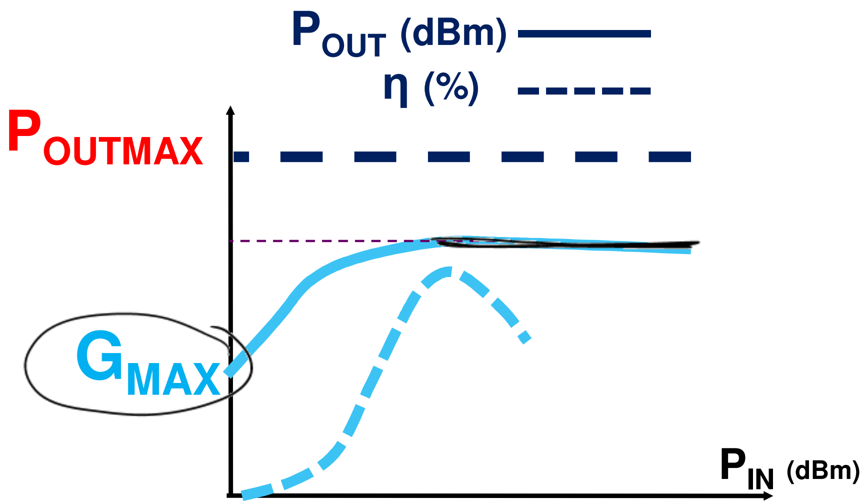
$$\underbrace{G_{max_{(dB)}}(2\omega) - G_{max_{dB}}(\omega)}_{\text{octave}} = 10 \log\left(\frac{K}{(2\omega)^2}\right) - 10 \log\left(\frac{K}{\omega^2}\right)$$

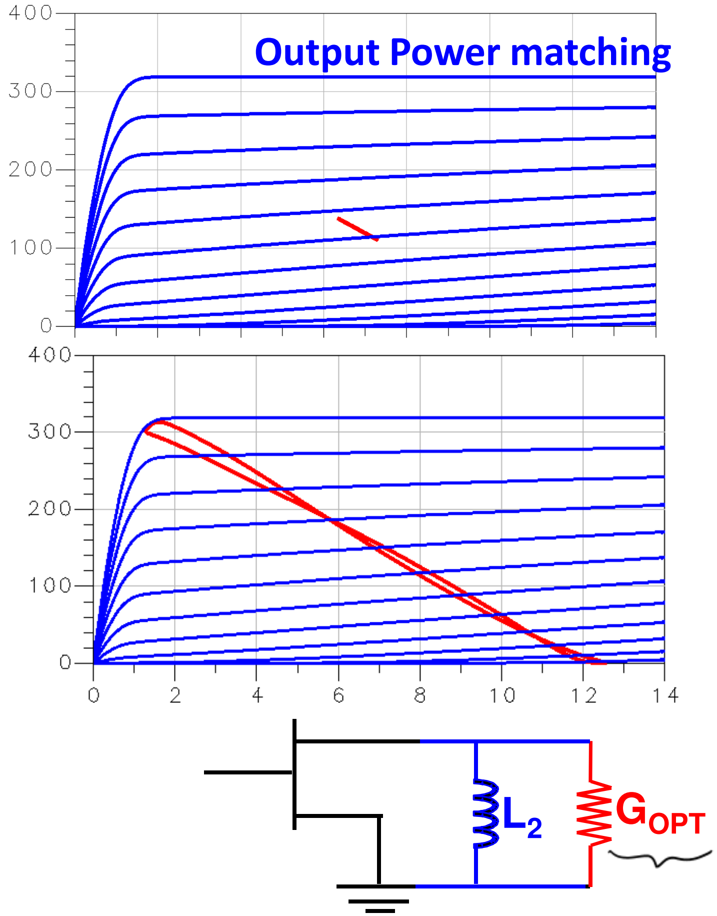
$$= 10 \log\left(\frac{K}{4\omega^2} \times \frac{\omega^2}{K}\right) = 10 \log\left(\frac{1}{4}\right) = -6\text{dB}$$

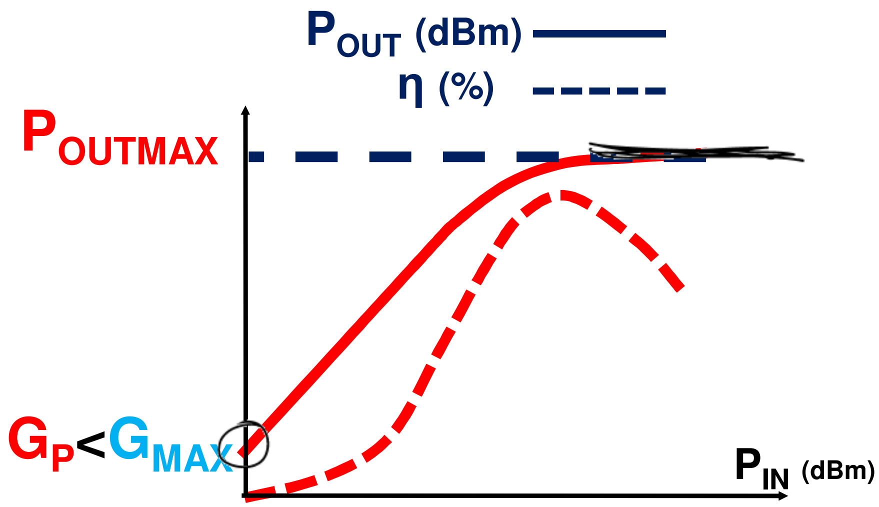
$$\begin{cases} G_{max}(10\,GHz) = 20\,dB = 10^2 = 100 \\ G_{max}(15\,GHz) = G_{max}(10\,GHz) \times \left(\dfrac{10}{15}\right)^2 \\ \qquad = 100 \times \left(\dfrac{10}{15}\right)^2 = 44 \\ \qquad = 10 \log(44) = 16.4\ dB \end{cases}$$

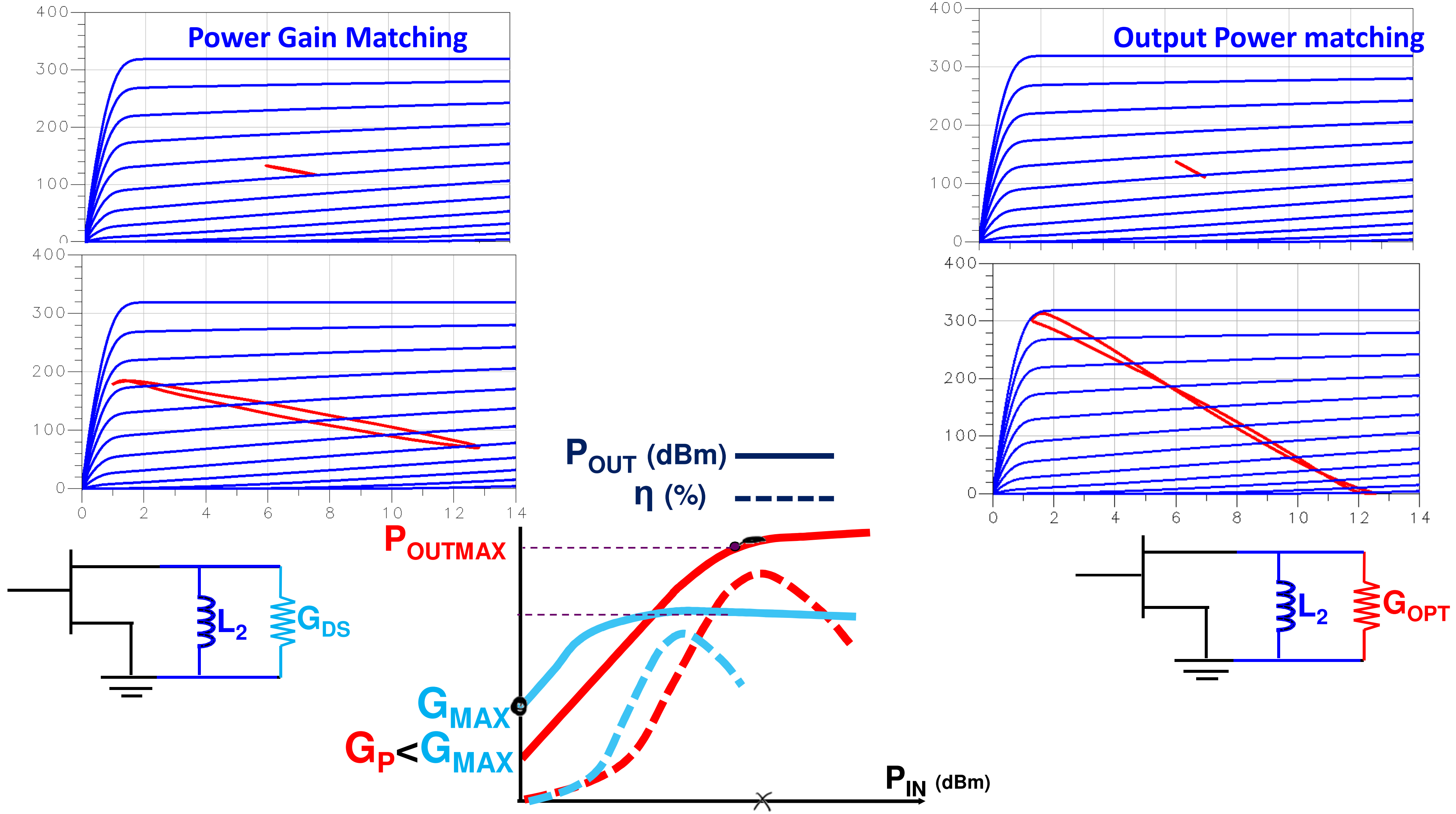

Power Gain Matching
Output Power matching
linear regime
saturated regime
L_2
G_{DS}
G_{OPT}
400
300
200
100
0
0
2
4
6
8
10
12
14


Power Gain Matching
400
300
200
100
0
0 2 4 6 8 10 12 14
L_2
G_{DS}


P_{OUT} (dBm)
η (%)
P_{OUTMAX}
G_{MAX}
P_{IN} (dBm)

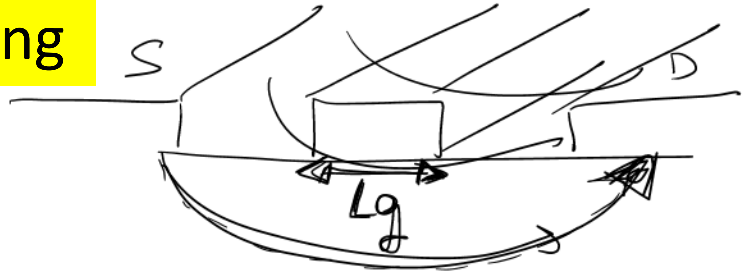

Output Power matching
400
300
200
100
0
0
2
4
6
8
10
12
14
L2
GOPT


POUT (dBm)
η (%)
POUTMAX
GP<GMAX
PIN (dBm)

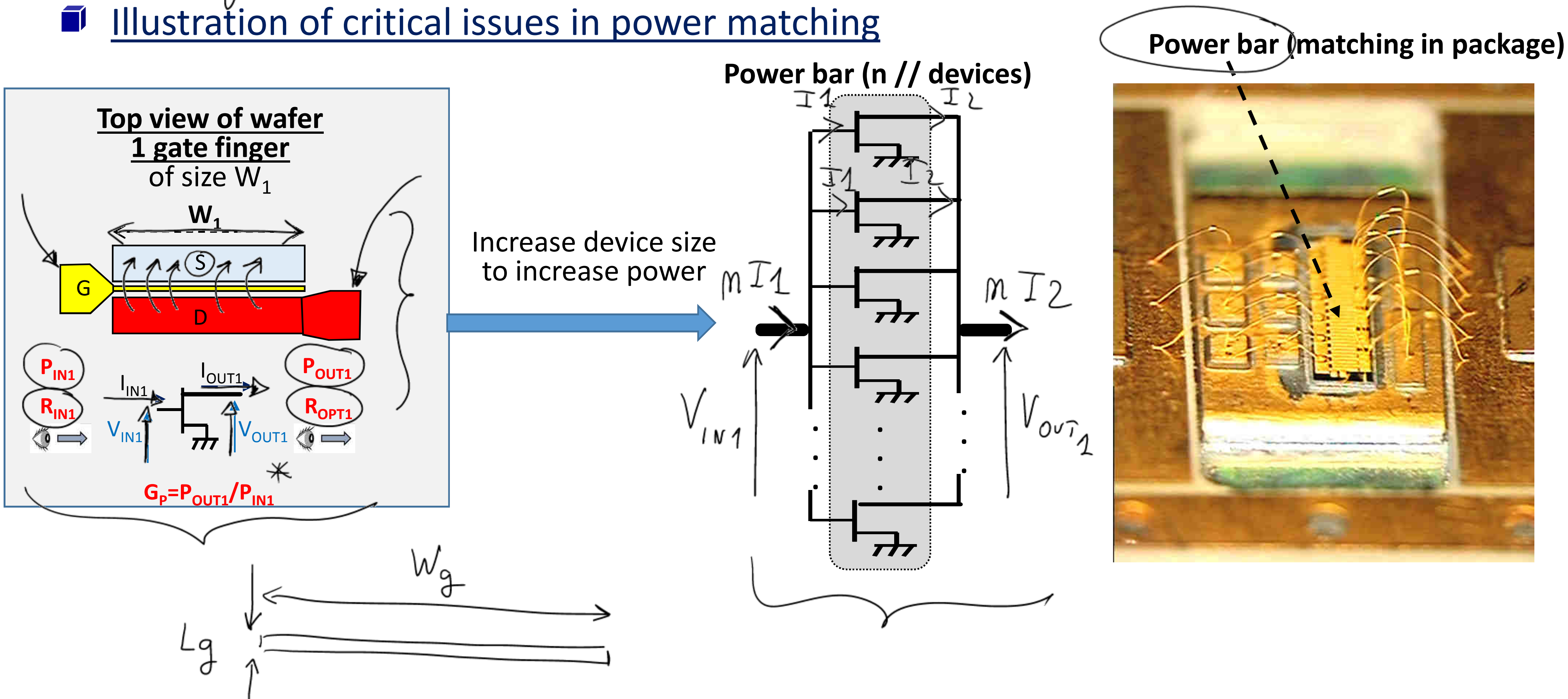

Power Gain Matching
Output Power matching
400
300
200
100
0
0 2 4 6 8 10 12 14
P_{OUT} (dBm)
η (%)
P_{OUTMAX}
G_{MAX}
G_P<G_{MAX}
P_{IN} (dBm)
L_2
G_{DS}
G_{OPT}

Power combination (Power Bars) and power matching

$$\begin{cases} L_g \simeq 0.25\,\mu m \\ W_g \simeq 50 - 300\,\mu m \end{cases}$$



- Illustration of critical issues in power matching

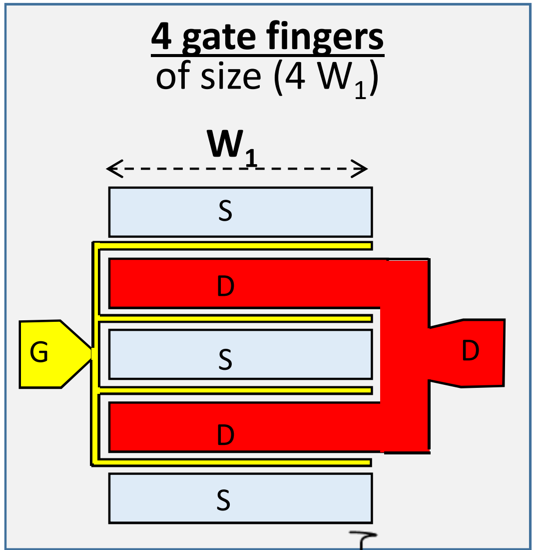


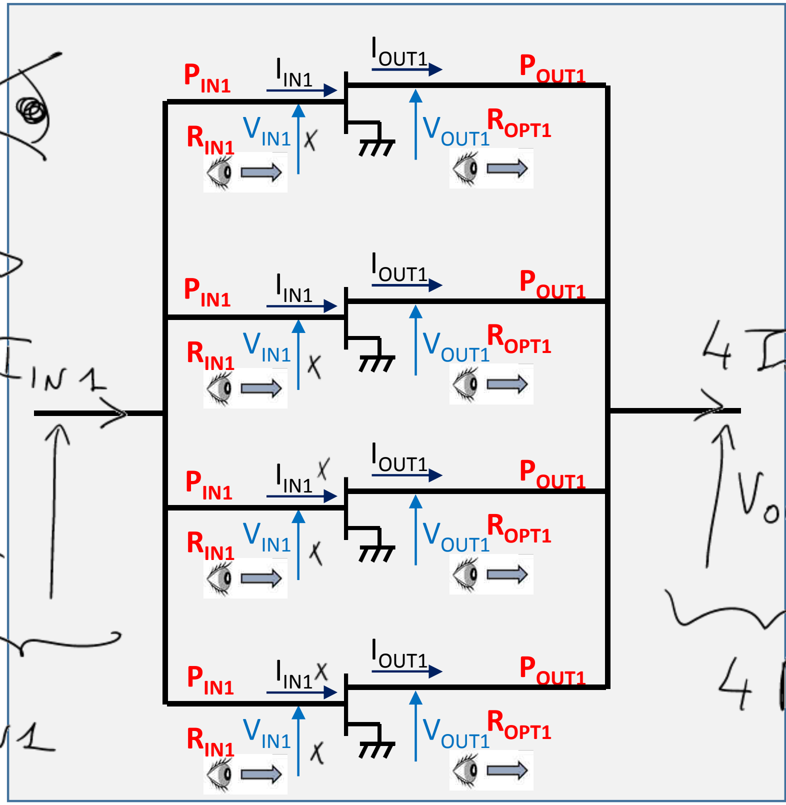
Power combination (Power Bars) and power matching

Illustration of critical issues in power matching

$I = Y V$

$2I = 2YV$





$4 I_{IN1}$

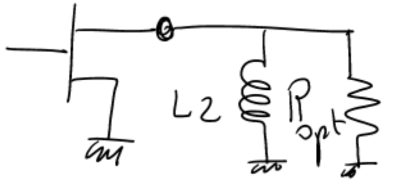
V_{IN1}

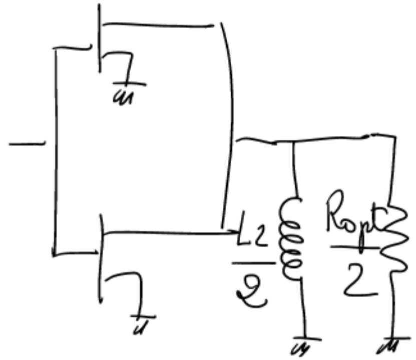
$4 P_{IN1}$

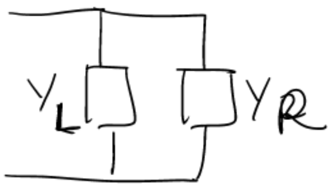
$4 I_{OUT1}$

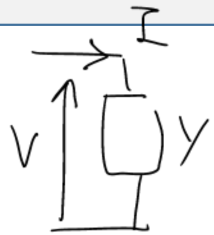
V_{OUT1}

$4 P_{OUT1}$

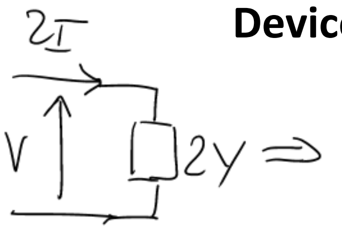


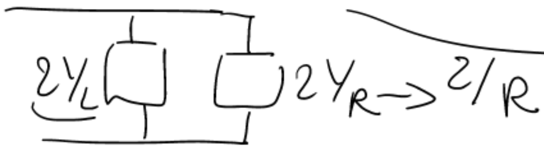






Device size = Total gate width = (N° of // gates) × (gate width) = **4 × W$_1$**



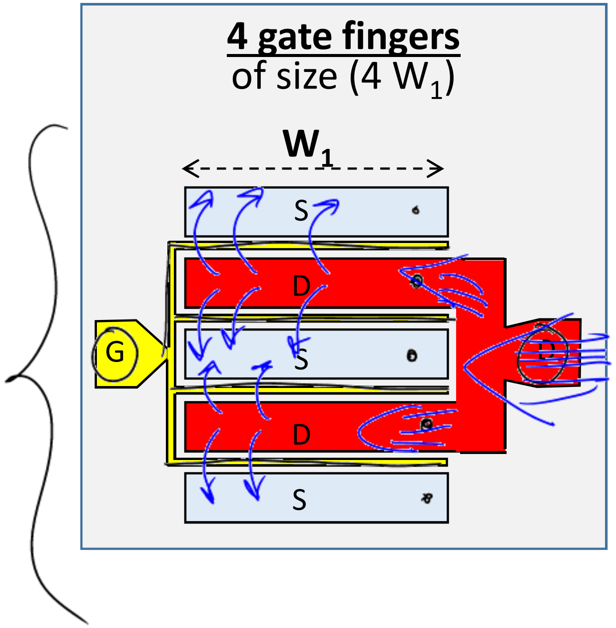


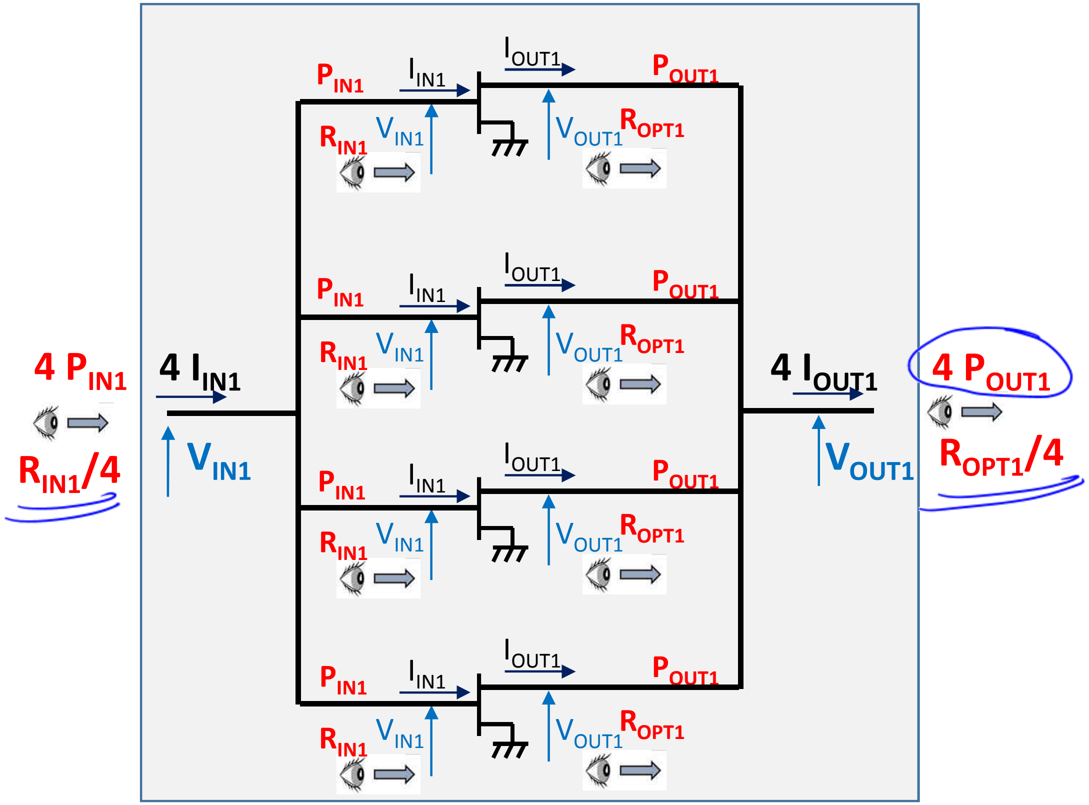
G_p

$L = \frac{1}{C \omega_0^2}$

Power combination (Power Bars) and power matching

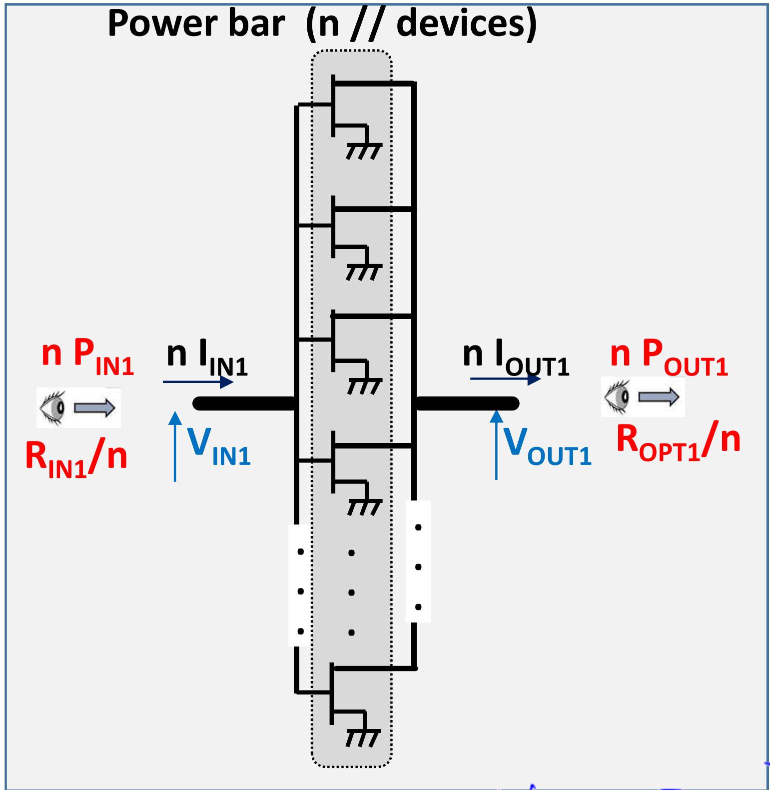
- Illustration of critical issues in power matching

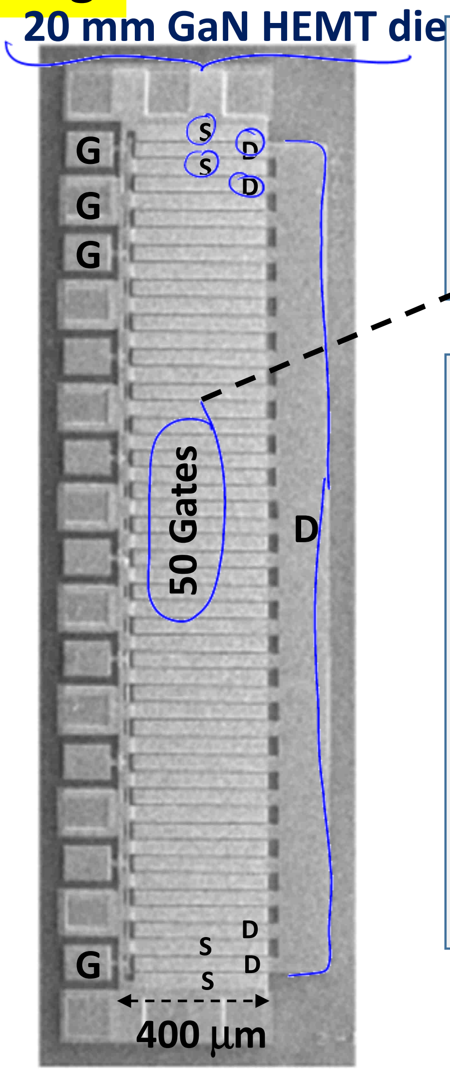




Power combination (Power Bars) and power matching

- Illustration of critical issues in power matching





Device Size
=
Total Gate Width
=
(N° of // gates) x (Gate width)
=
50 x 400 µm = **20 mm**

Scaling Rules:

- **Drain Current**
  I_{DS} (mA/mm)
- **Voltages**
  V_{GS} and V_{DS} (V)
- **Output Power**
  P_{OUT} (W/mm)
- **Optimum Output Load**
  R_{OPT} (Ω . mm)

4 gate fingers

$W_G = 75\,\mu m$

Size = $4 \times W_G$
$= 4 \times 75\,\mu m = 300\,\mu m = 0{,}3\,mm$

R_{opt}

Main transmission lines and Passive elements used in MMIC designs

MMIC (Monolithic Microwave and Millimeterwave Integrated Technology)

$f \gg 1GHz$

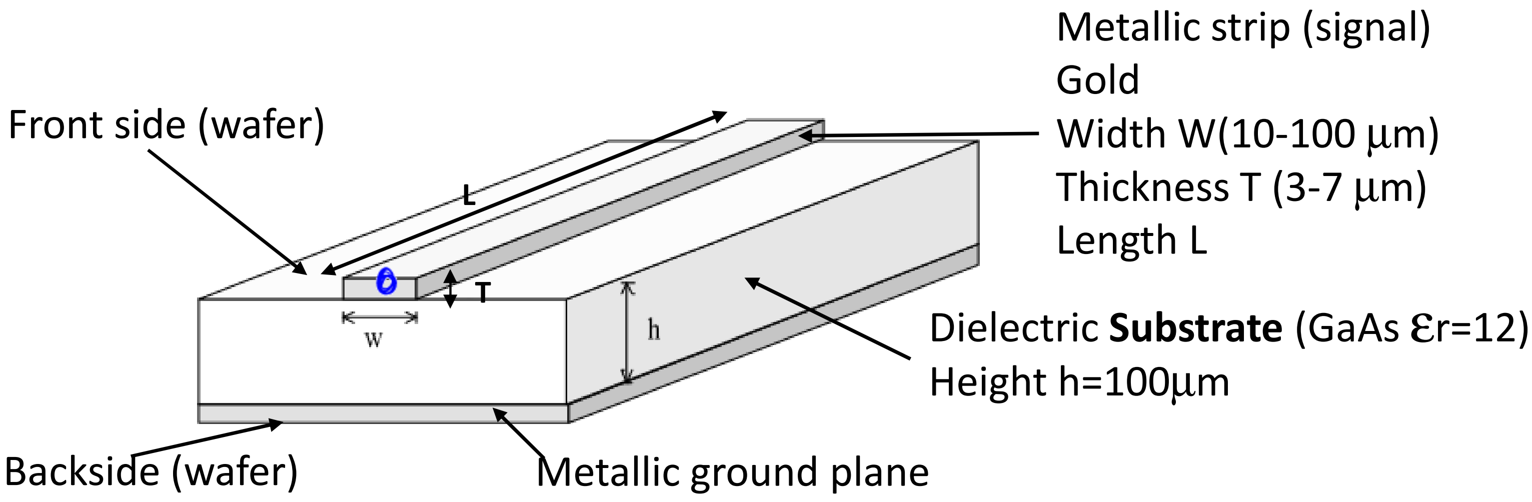
- Recall on Transmission lines

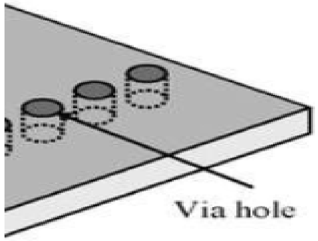
- Microstrip inductors/capacitors/resistors

- Harmonic loading and bias using $\lambda/4$ lines

- Matrix chain of a line and impedance transformation

Microstrip lines



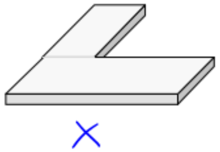


- Requirement of **metallized via holes** through the substrate to connect electrical elements from the front side to the metallic ground plane
  → expensive backside process after the front side process ☹
  → easier design of the signal paths on the front side when compared to coplanar
  → the most effective integrated technology at high frequencies ☺

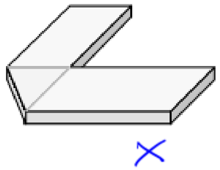
Microstrip lines = wires at Low frequencies

In order to drive the signal, these are some of the main shapes of line connections

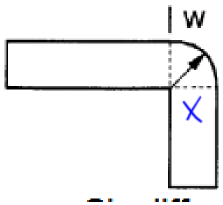
CORNER



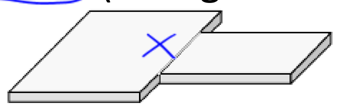
BEND



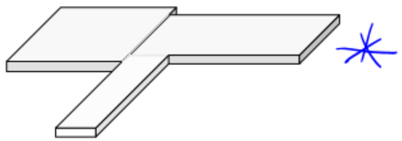
ROUND



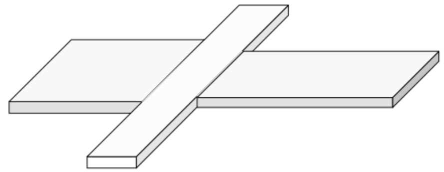
STEP (change of Zc)



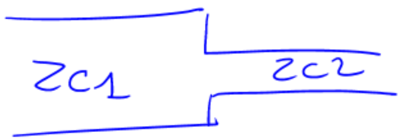
TEE junction (3 lines)

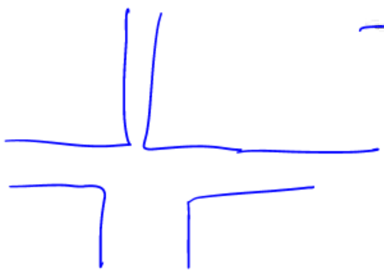


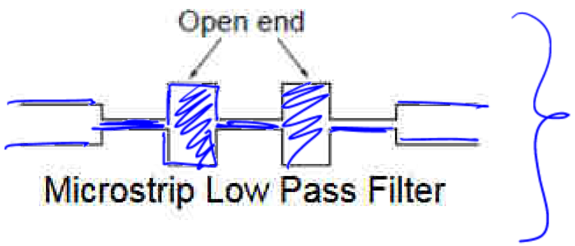
CROSS junction (4 lines)

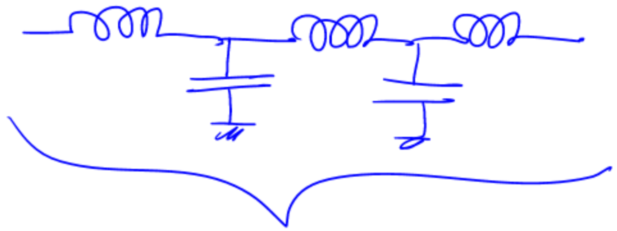


In order to design passive circuits→ Narrow Lines (Inductive) Wide Lines (Capacitive)

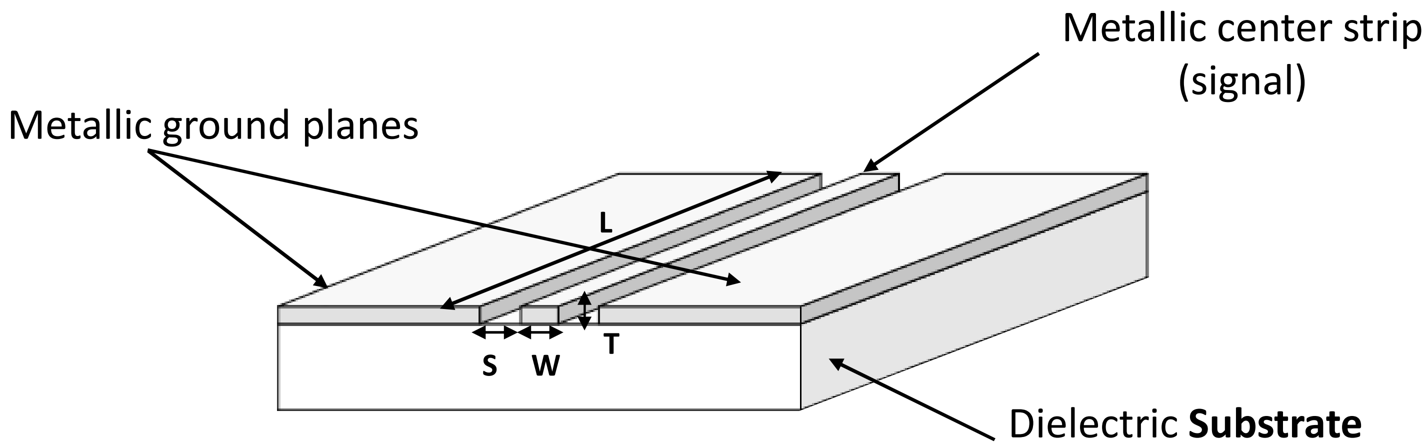








Coplanar lines



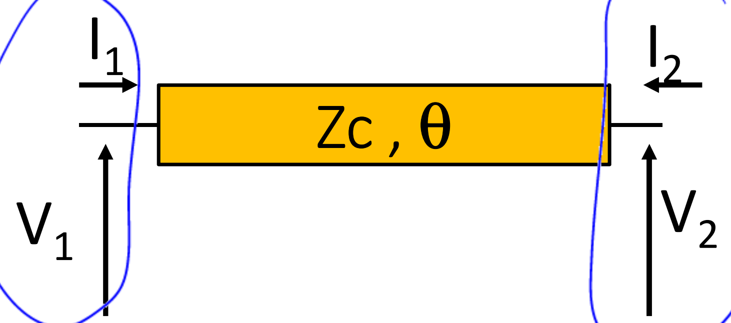
- ❑ No requirement of metallized via holes through the substrate to connect electrical elements from the front side to the metallic ground plane
  → no expensive backside process after the front side process ☺
  → complex design of the signal paths on the front side ☹
  → lower performances than microstrip designs ☹

Line = Matrix chain

Propagation constant $\Gamma = \alpha + j\,\beta$ → Attenuation constant α and Phase constant β

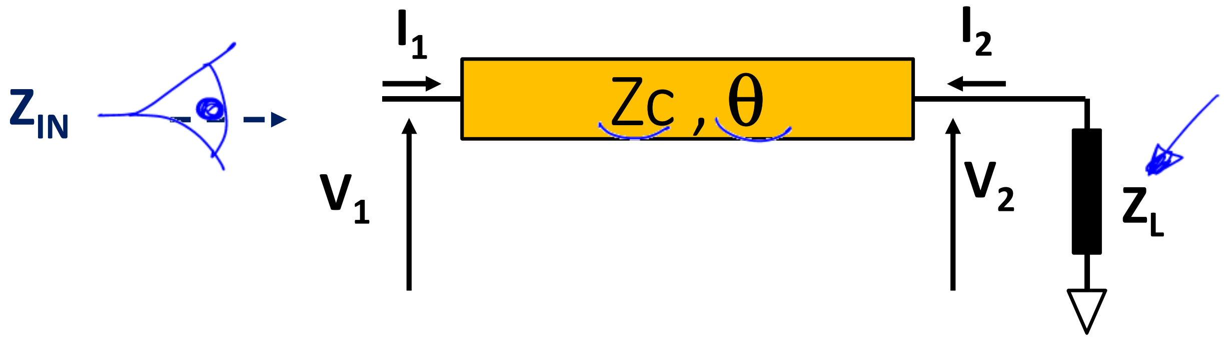
$\beta = 2\pi/\lambda$

$\theta = \beta\, L$



$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_C\sin(\theta) \\ j\sin(\theta)/Z_C & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

Equivalent input impedance of a loaded line



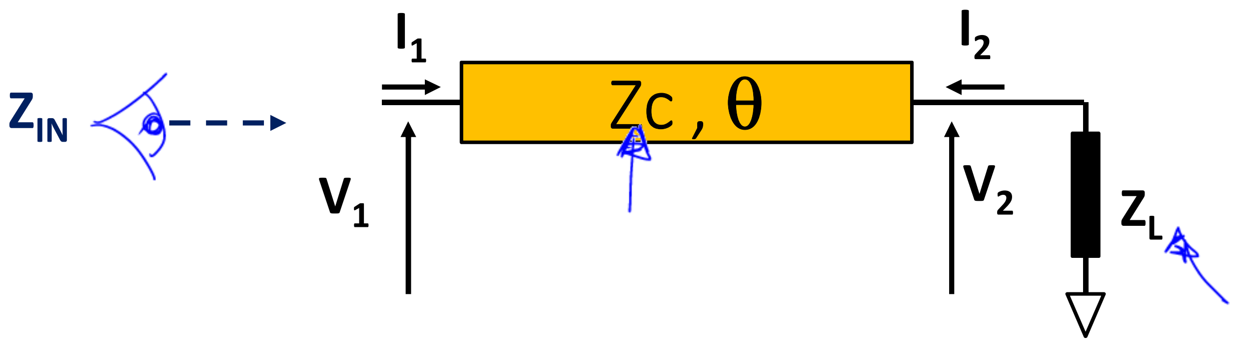
$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_C\sin(\theta) \\ j\sin(\theta)/Z_C & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

$$V_2 = -Z_L I_2$$

$$\mathbf{Z_{IN}} = \frac{V_1}{I_1} = \frac{\cos(\theta)\, V_2 - jZ_C\sin(\theta) I_2}{\left(\frac{j\sin(\theta)}{Z_C}\right) V_2 - \cos(\theta)\, I_2} = \frac{\cos(\theta)\,(-Z_L I_2) - jZ_C\sin(\theta) I_2}{\left(\frac{j\sin(\theta)}{Z_C}\right)(-Z_L I_2) - \cos(\theta)\, I_2}$$

$$\boxed{\mathbf{Z_{IN}} = \frac{\cos(\theta)\,(Z_L) + jZ_C\sin(\theta)}{\left(\frac{j\sin(\theta)}{Z_C}\right)(Z_L) + \cos(\theta)} = \mathbf{Z_C}\, \frac{\mathbf{Z_L\cos(\theta) + jZ_C\sin(\theta)}}{\mathbf{jZ_L\sin(\theta) + Z_C\cos(\theta)}}}$$

Equivalent input impedance of λ/4 and λ/2 loaded lines



$$\boldsymbol{Z_{IN}} = Z_C \frac{Z_L\cos(\theta) + jZ_C\sin(\theta)}{jZ_L\sin(\theta) + Z_C\cos(\theta)} \begin{cases} if\ \boxed{\boldsymbol{L} = \dfrac{\lambda}{\boldsymbol{4}}} \rightarrow \boldsymbol{\theta} = \dfrac{2\pi L}{\lambda} = \dfrac{\pi}{\boldsymbol{2}} \rightarrow \boxed{\boldsymbol{Z_{IN}} = \dfrac{\boldsymbol{Z_C^2}}{\boldsymbol{Z_L}}} \\ if\ \boxed{\boldsymbol{L} = \dfrac{\lambda}{\boldsymbol{2}}} \rightarrow \boldsymbol{\theta} = \dfrac{2\pi L}{\lambda} = \pi \rightarrow \boxed{\boldsymbol{Z_{IN}} = \boldsymbol{Z_L}} \end{cases}$$

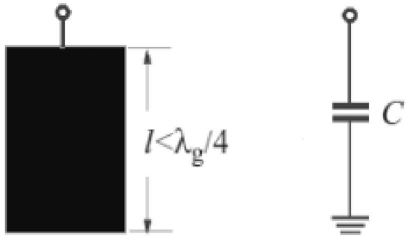
Impedance inverter

High- and Low-impedance short lines (Inductive or capacitive)

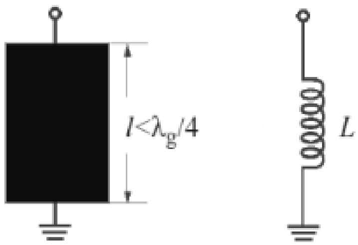
High-impedance short-line element and the Equivalent circuit

Low-impedance short-line element and the Equivalent circuit

Open and short-circuited stubs

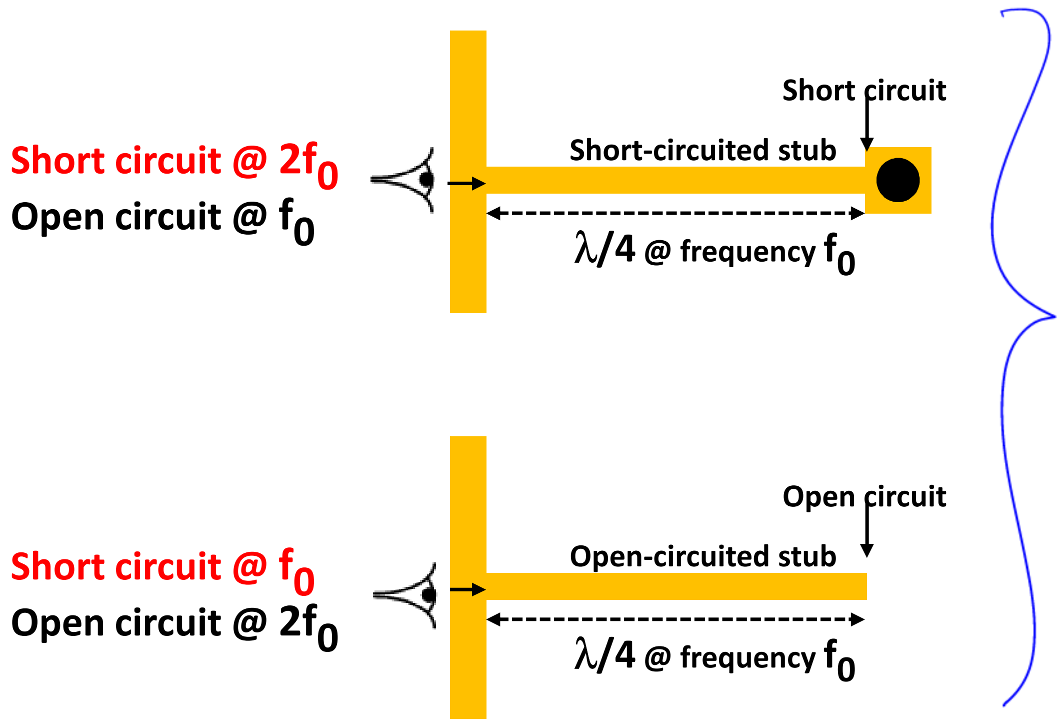


Open-Circuited Stub

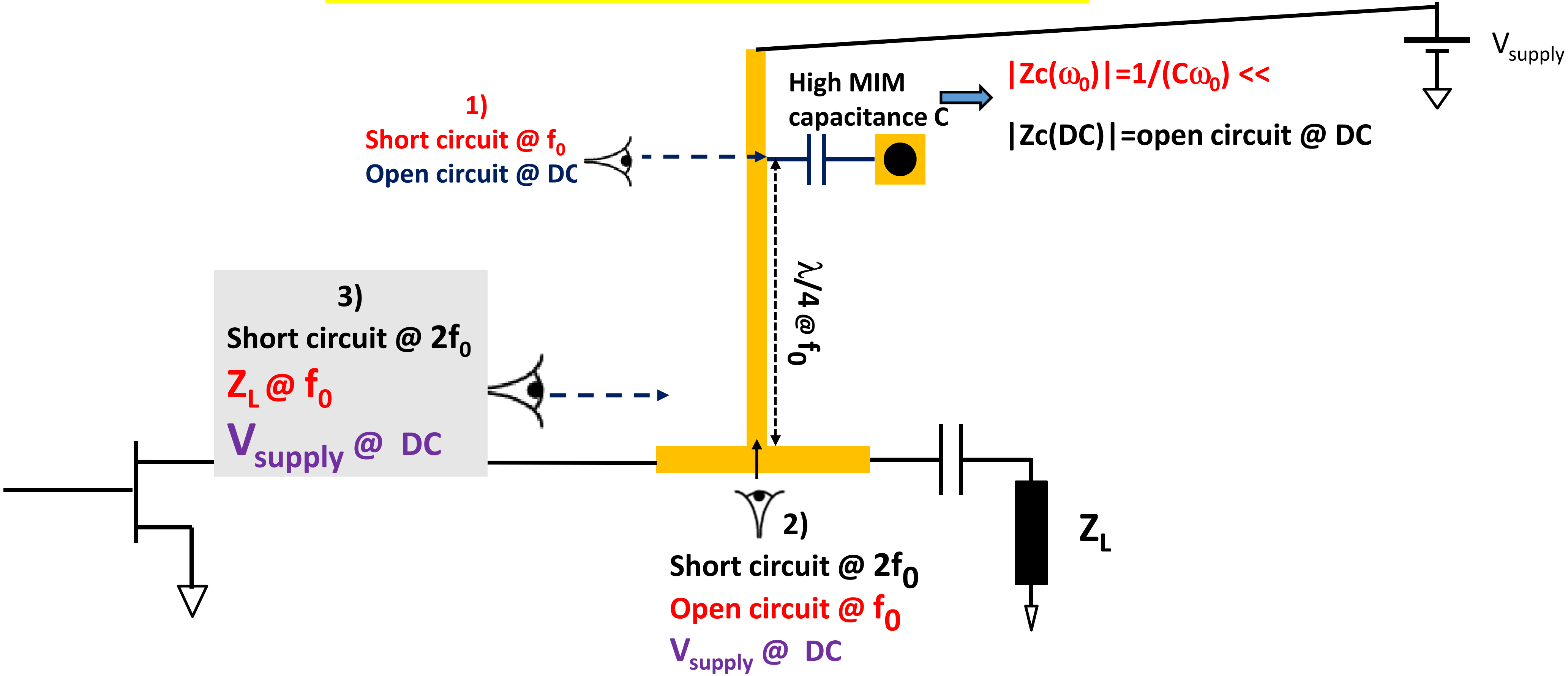


Short-Circuited Stub

Narrowband Harmonic loading using quarter wavelength line (λ/4)

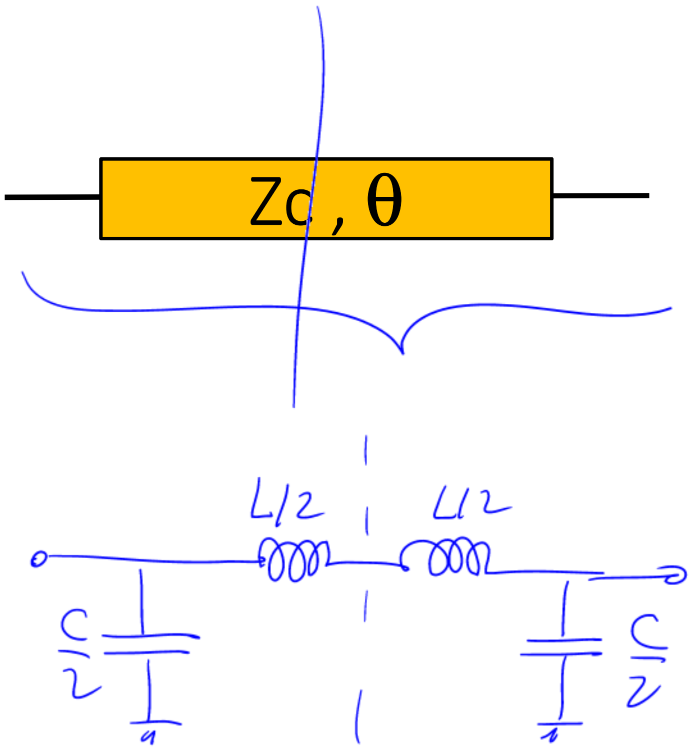


Bias network decoupling using quarter wavelength line ($\lambda/4$)

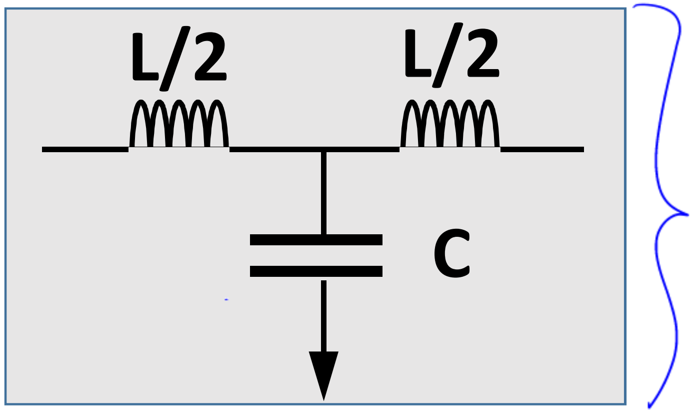


Reminder = Electrical lumped equivalent (RLC) of transmission lines

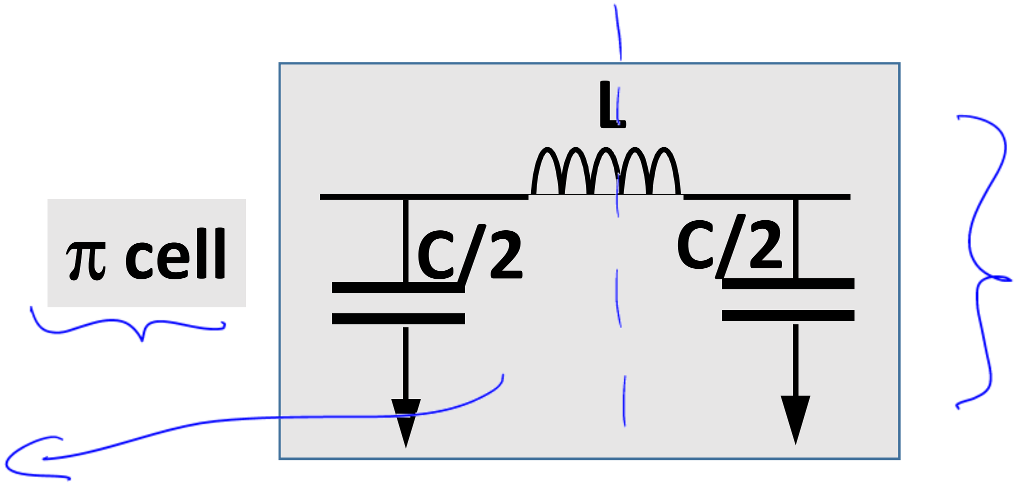
Electrical lumped equivalent (LC) of a lossless line (Zc, θ)



T cell



π cell

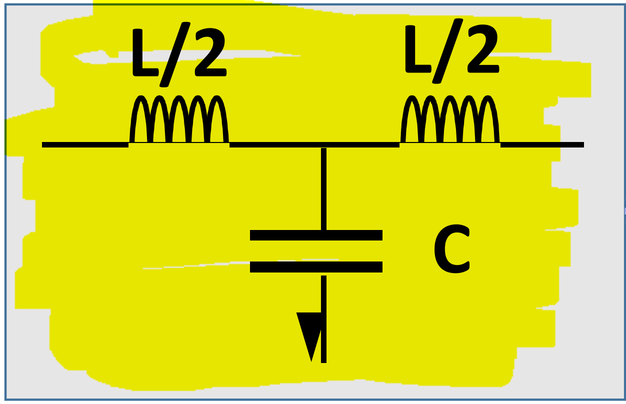


Electrical lumped equivalent (LC) of a lossless line (Zc, θ)

Cut-off frequency

$$f_C = \frac{1}{\pi\sqrt{LC}}$$

T cell



Characteristic Impedance

$$Z_C = \sqrt{\frac{L}{C}}\sqrt{1-\left[\frac{f}{f_C}\right]^2}$$

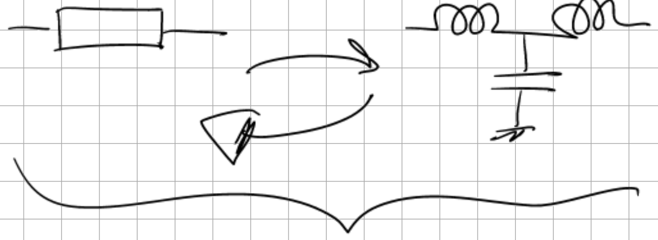
Phase Shift

$$\theta = \omega\sqrt{LC}\sqrt{1-\left[\frac{f}{f_C}\right]^2}$$

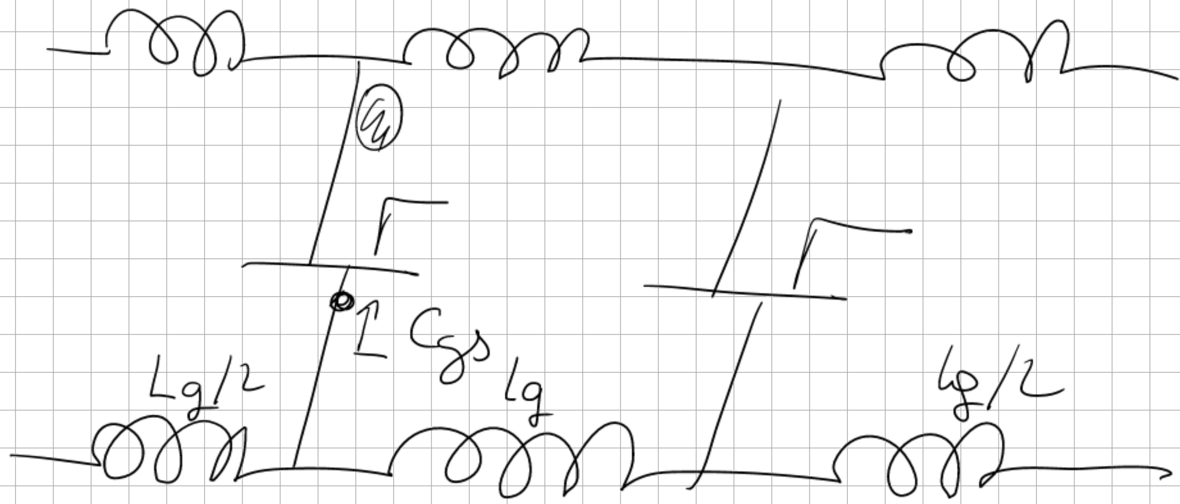
$$\boxed{f \ll f_C}$$

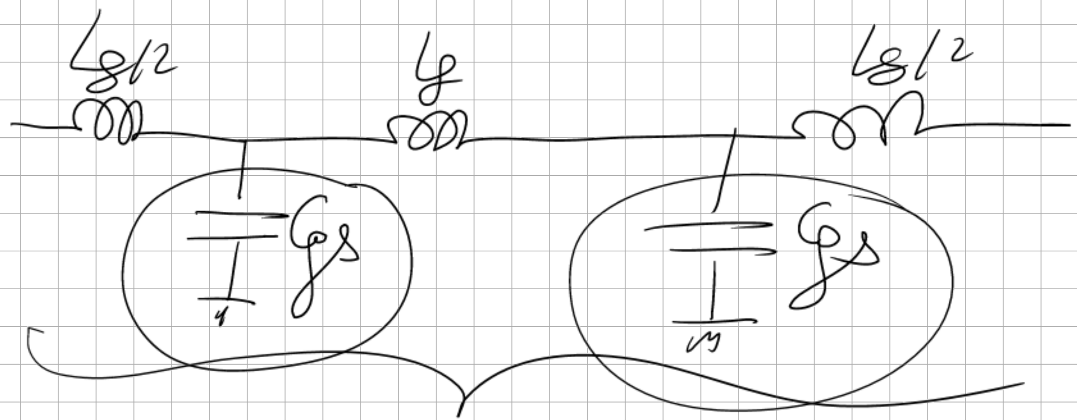
$$\sqrt{1-\left[\frac{f}{f_C}\right]^2} > 0.9 \;\Leftrightarrow\; f < 0.44\, f_C$$

$$\boxed{Z_C = \sqrt{\frac{L}{C}}} \text{ and } \boxed{\theta = \omega\sqrt{LC}}$$



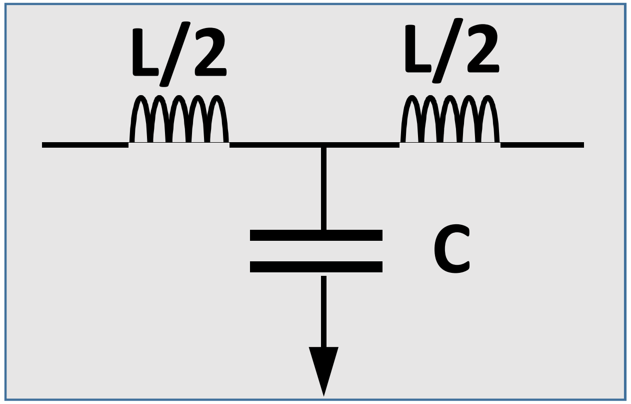

G
f


Lg/2
Cgs
Lg
Lg/2


Lg/2
Lg
Lg/2
Cgs
Cgs

Electrical lumped equivalent (LC) of a lossless line (Zc, θ)

T cell



Cut-off frequency

$$f_C = \frac{1}{\pi\sqrt{LC}}$$

Characteristic Impedance

If f<<f_C → $$Z_C \approx \sqrt{\frac{L}{C}}$$

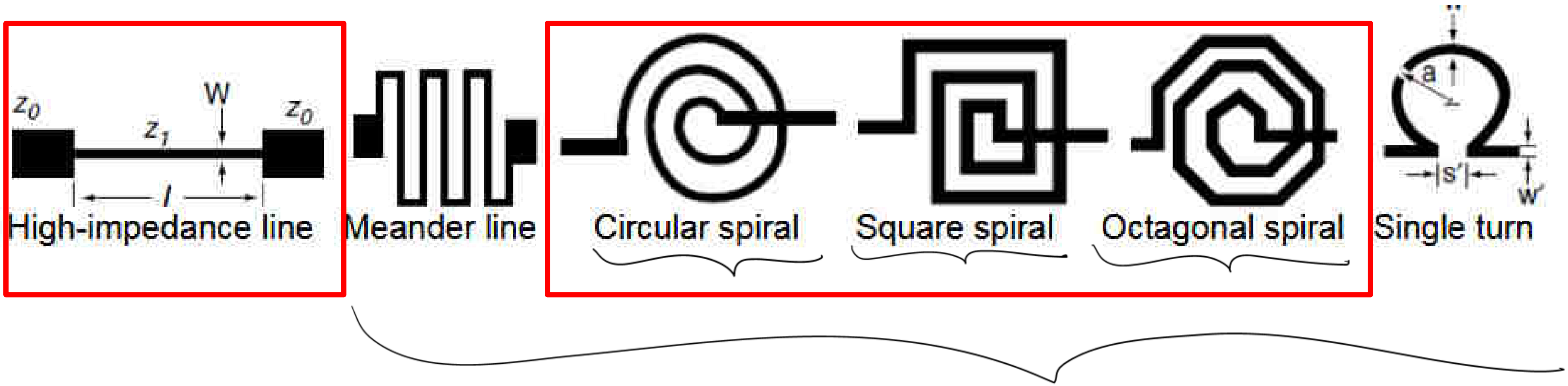
$f < 0.44\, f_C$

Phase Shift

If f<<f_C → $$\theta \approx \omega\sqrt{LC}$$

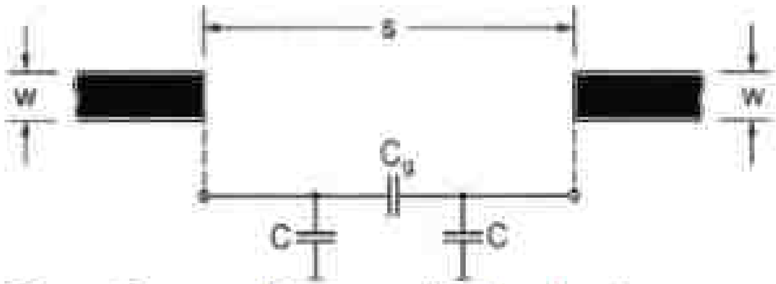
Microstrip passive inductors, capacitors and resistors

Microstrip Inductors

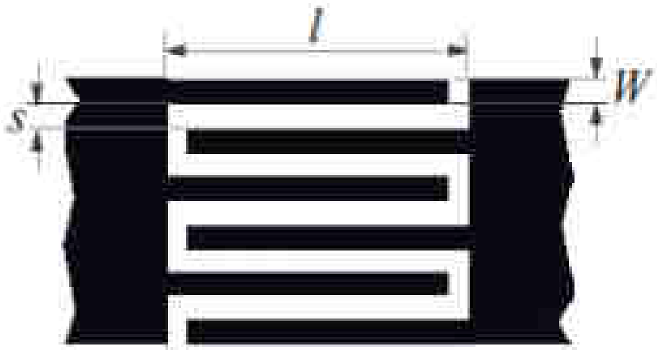


Only used at lower frequencies up to 3-4GHz because of very high losses
Achievable values up to few nH

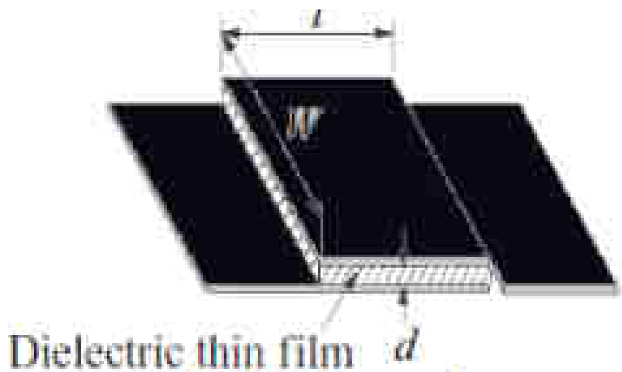
Microstrip Capacitors (MIM : Metal Insulator Metal)



Gap Capacitor and Equivalency



Interdigital Capacitor SiO_2



MIM Capacitor

$$\mathbf{C = \varepsilon \frac{S}{d}} = \varepsilon \frac{\mathbf{l \times W}}{\mathrm{d}}$$

$$\mathbf{C} = \frac{\boldsymbol{\varepsilon}}{\mathbf{d}}(\mathbf{l} \times \boldsymbol{W})$$

$$\mathbf{C = CD \times S}$$

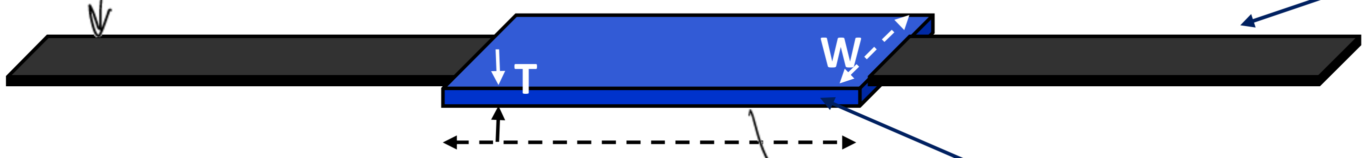
$$\mathbf{CD} = \frac{\boldsymbol{\varepsilon}}{\mathbf{d}}$$

Capacitance density (F/m²)

Ex : 300 pF/mm²→ Achievable values 0.2pF→20pF

Microstrip Resistors (TaN)

Gold
1m Ω/sq



Microstrip Lines
Highly Conductive Metal
(Au) → RS = 0.001 Ω/sq

Highly Resistive Metal
(TaN) → RS = 50 Ω/sq

$$\boxed{R = \rho_{TaN}\,\frac{L}{S} = \rho_{TaN}\,\frac{L}{T \times W}}$$

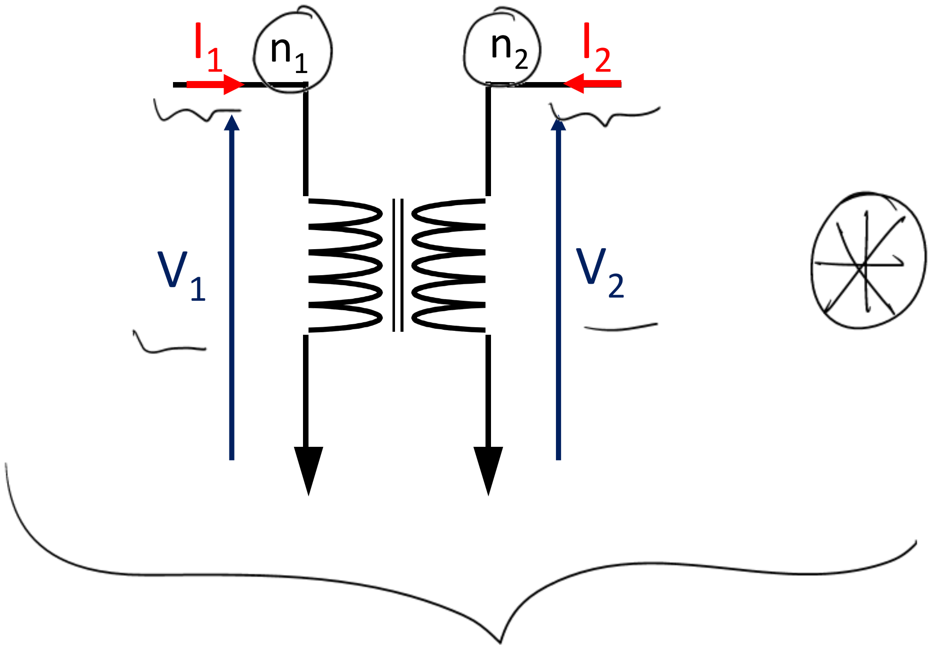
$$R = \frac{\rho_{TaN}}{T}\,\frac{L}{W} = R_S\,\frac{L}{W}$$

$$\boxed{R_S = \frac{\rho_{TaN}}{T}}$$

Sheet resistance R_S (Ω/sq)
(Ω/)

$$\boxed{R = R_S\,\frac{L}{W}}$$

Reminder = Ideal Electrical transformers
How are they realized at high frequencies ?



EMIMEO

E(rasmus) Mundus on Innovative Microwave Electronics and Optics

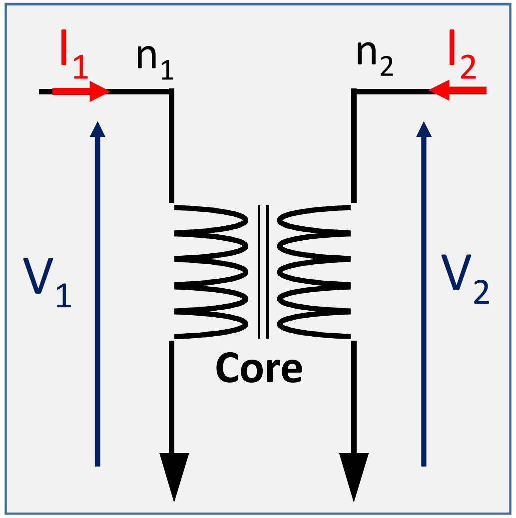
Reminder = Ideal Electrical transformer

$$\boxed{\frac{V_2}{V_1} = \frac{n_2}{n_1}}$$

$$\boxed{\frac{I_2}{I_1} = -\frac{n_1}{n_2}}$$

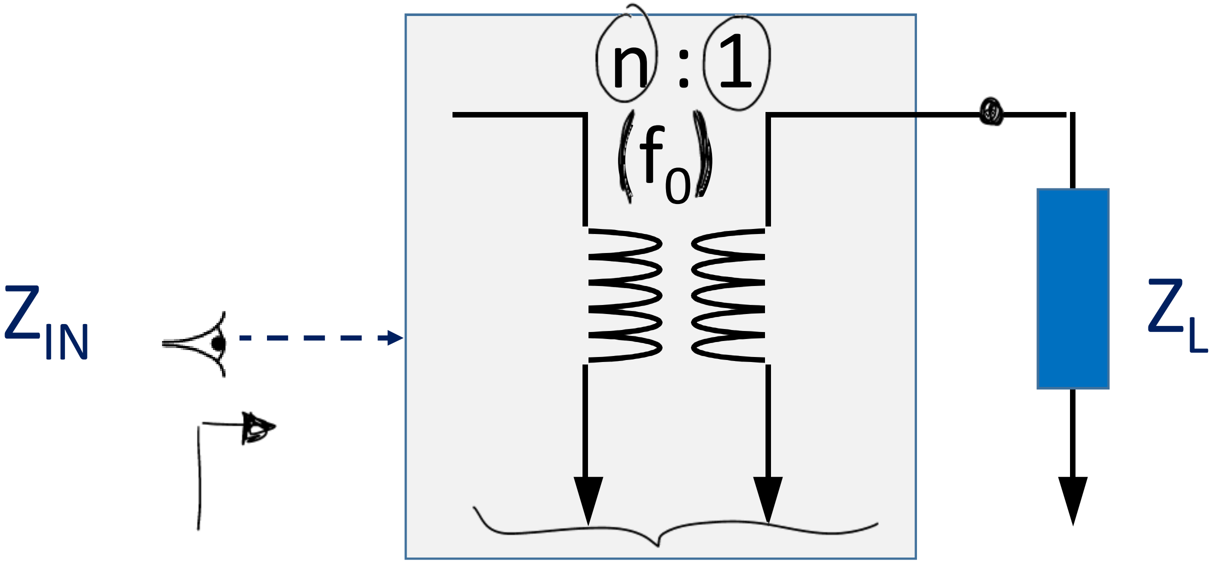
Conservation of energy

Primary Winding
(n1 turns)



Secondary Winding
(n2 turns)

Reminder = Impedance transformation



Criterion

- Transformation ratio
- Bandwidth
- Technology

$$n = \sqrt{\frac{Z_L}{Z_{IN}}} \times$$

$$Z_{IN} = \underbrace{n^2}\, Z_L$$

$$\underbrace{n} = \sqrt{\frac{Z_{IN}}{Z_L}} \times$$

$n = 0.1$ or $n = 10$

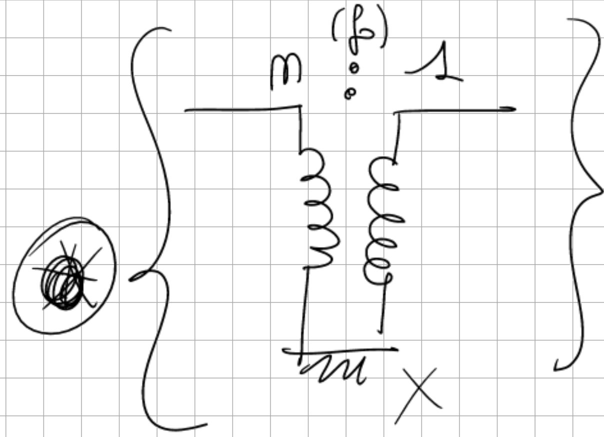
$\underbrace{m = 0.1}$ $\underbrace{m = 10}$

$\underbrace{m = 1}$

$m = 3$ 1 $n = 0.1$

0.1 1 ideal 3

$\frac{1}{3} = 0{,}33$ $\frac{1}{0{,}1} = 10$

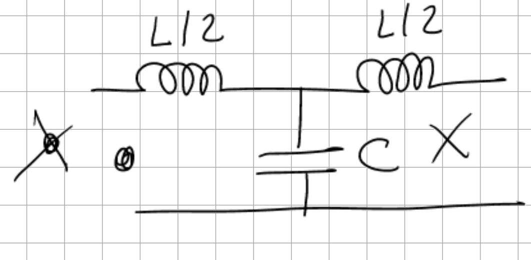


electrical symbol without losses

$m = 1 \rightarrow$ no losses

$m > 1 \rightarrow$ losses ↑

@ low frequencies ($\simeq$ 1GHz)

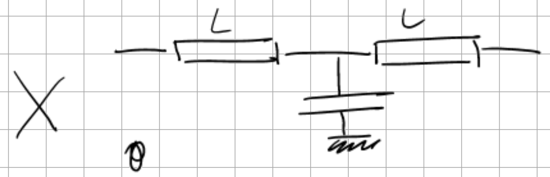


$\lambda_0/4\,(1\,\text{GHz}) = 6\,\text{mm}$

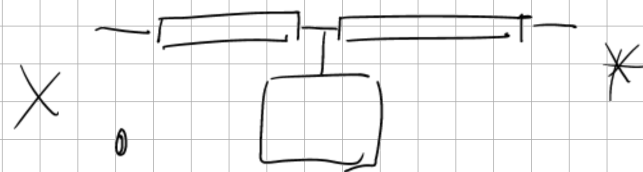
$\theta = \omega_0 \sqrt{LC}$

$Z_c = \sqrt{\frac{L}{C}}$

@ medium frequencies (5GHz)



@ — — — — — —



$$\lambda = \frac{v}{f}$$

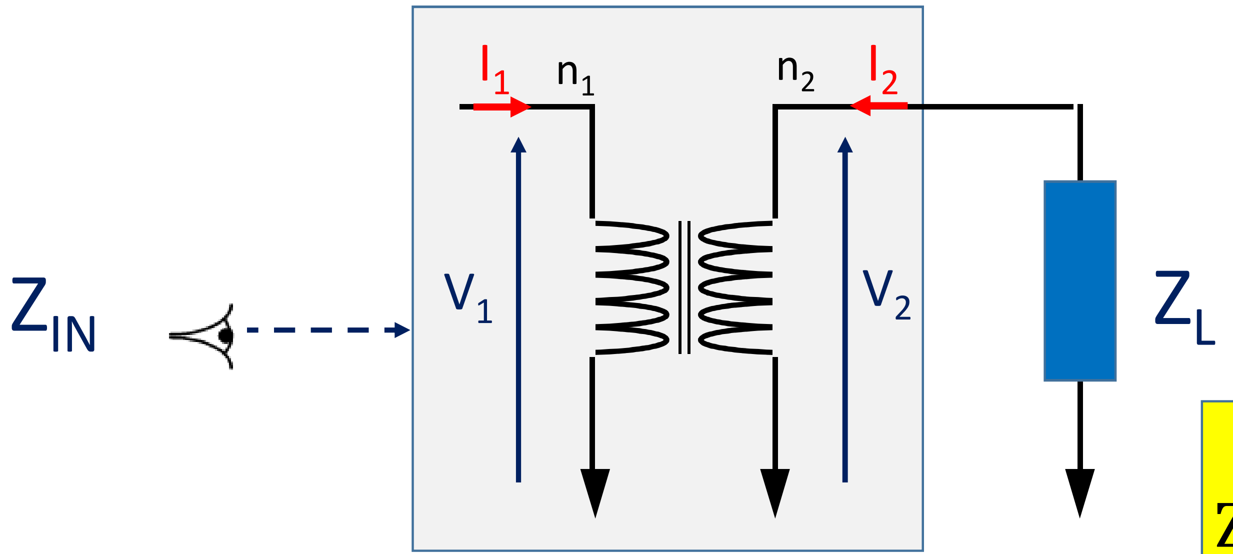
$Z_c \; (l = \lambda_0/4) \rightarrow 200\,\mu m$

@ very high frequencies (40GHz ...)

Reminder = Impedance transformation

$$\boxed{\frac{V_2}{V_1} = \frac{n_2}{n_1}}$$

$$\boxed{\frac{I_2}{I_1} = -\frac{n_1}{n_2}}$$



Load

$$\boxed{V_2 = -Z_L\, I_2}$$

$$Z_{IN} = \frac{V_1}{I_1} = \frac{V_1}{V_2}\,\frac{V_2}{I_2}\,\frac{I_2}{I_1} = \frac{n_1}{n_2}\,(-Z_L)\,\frac{-n_1}{n_2} = \left[\frac{n_1}{n_2}\right]^2 Z_L$$

$$Z_{IN} = \left[\frac{n_1}{n_2}\right]^2 Z_L$$

$$n = \left[\frac{n_1}{n_2}\right] = \sqrt{\frac{Z_{IN}}{Z_L}}$$