CACHE SUBSYSTEM

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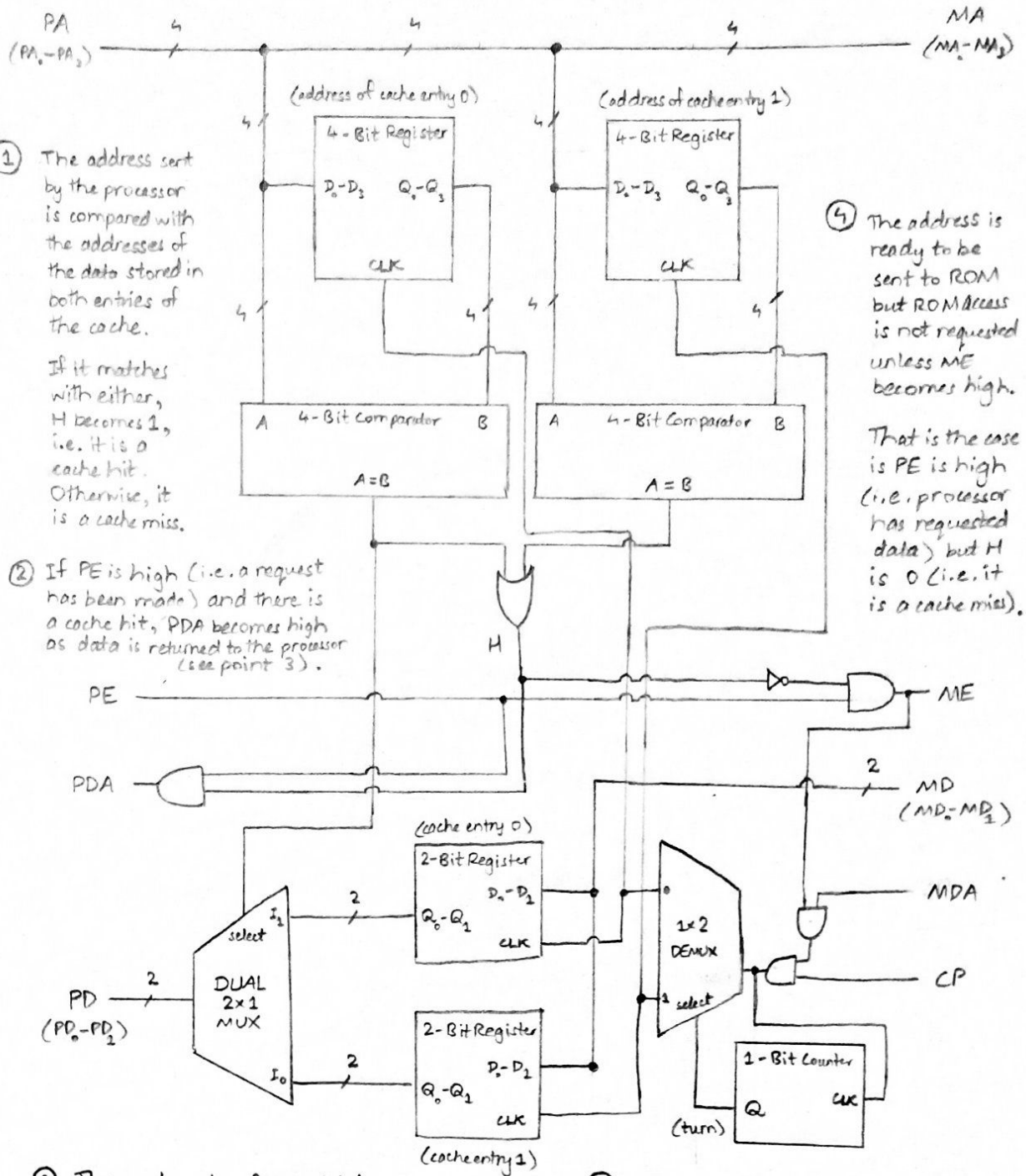

(1) The address sent by the processor is compared with the addresses of the data stored in both entries of the cache.

If it matches with either, H becomes 1, i.e. it is a cache hit. Otherwise, it is a cache miss.

(2) If PE is high (i.e. a request has been made) and there is a cache hit, PDA becomes high as data is returned to the processor (see point 3).

(3) The cache entry from which data is to be sent is chosen using a multiplexer with the output of a comparator determining which address has matched (i.e. it is the select input of the MUX).

(4) The address is ready to be sent to ROM but ROM access is not requested unless ME becomes high.

That is the case is PE is high (i.e. processor has requested data) but H is 0 (i.e. it is a cache miss).

(5) When the ROM returns the data, it is decided based upon the turn that which entry will be updated (using a DEMUX).

Enabling of the components for update is done by supplying them with a clock pulse if ME and MDA are high (i.e. if ROM access has been requested and ROM has returned data).

Turn is generated by a 1-bit counter which counts ROM accesses.

(6) Once the cache has been updated, a cache hit occurs and hence data is returned to the processor (i.e. steps 1, 2 & 3 are carried out).