Digital Design and Computer Organisation Laboratory

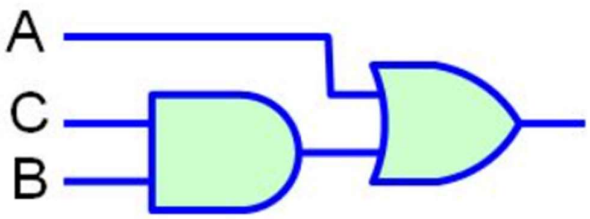
UE22CS251A

3rd Semester, Academic Year 2023

Name: **ASHLESHA.T**	SRN: **PES1UG22CS118**	Section **B**

Week# 2 Program Number: ____1___

TITLE: IMPLEMENT THE GIVEN CIRCUIT



Source code:

w2cir1.v

```
module and2(p,c,b);
input c,b;
output p;
assign p=c&b;
endmodule

module or2(x,a,p);
input a,p;
output x;
assign x=a|p;
endmodule

module w2cir1(y,a,b,c);
input a,b,c;
wire p;
output y;
and2 and_2(p,b,c);
or2 or_2(y,a,p);
endmodule
```

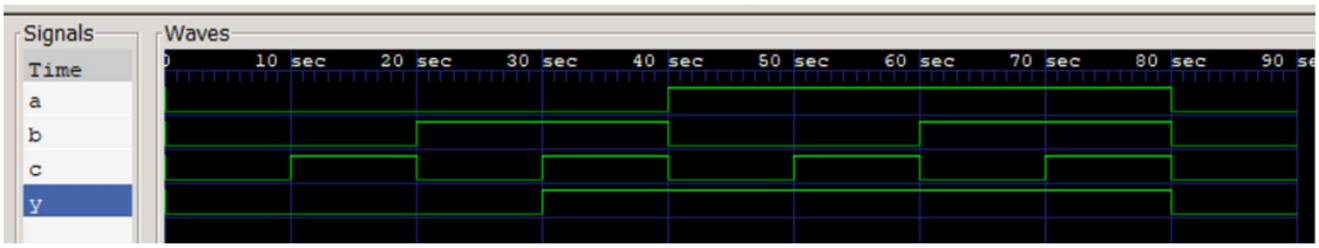
w2cir1_tb.v

```
module w2cir1_tb;
reg a,b,c;
wire y;
w2cir1 cir1_test(y,a,b,c);
initial
begin
a=0;b=0;c=0; #10;
a=0;b=0;c=1; #10;
a=0;b=1;c=0; #10;
a=0;b=1;c=1; #10;
a=1;b=0;c=0; #10;
a=1;b=0;c=1; #10;
a=1;b=1;c=0; #10;
a=1;b=1;c=1; #10;
a=0;b=0;c=0; #10;
end
initial
begin
$monitor($time," a=%b b=%b c=%b  y=%b",a,b,c,y);
end
initial
begin
$dumpfile("w2_test.vcd");
$dumpvars(0,w2cir1_tb);
end
endmodule
```

VVP OUTPUT:

```
PS C:\iverilog\bin> iverilog -o test w2cir1.v w2cir1_tb.v
PS C:\iverilog\bin> vvp test
VCD info: dumpfile w2_test.vcd opened for output.
                   0 a=0 b=0 c=0  y=0
                  10 a=0 b=0 c=1  y=0
                  20 a=0 b=1 c=0  y=0
                  30 a=0 b=1 c=1  y=1
                  40 a=1 b=0 c=0  y=1
                  50 a=1 b=0 c=1  y=1
                  60 a=1 b=1 c=0  y=1
                  70 a=1 b=1 c=1  y=1
                  80 a=0 b=0 c=0  y=0
```

GTK WAVE:

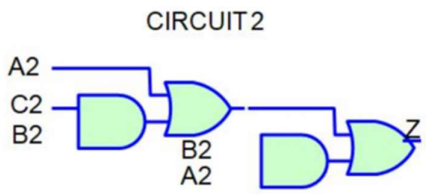


Name: **ASHLESHA.T**	SRN: **PES1UG22CS118**	Section **B**

Week# 2

Program Number: ____2___

TITLE :



Y= [A2 OR (C2 AND B2)]OR(B2 AND A2)

SOURCE CODE:

w2cir2.v

```
1   module and2(p,c,b);
2   input c,b;
3   output p;
4   assign p=c&b;
5   endmodule
6
7   module or2(x,a,p);
8   input a,p;
9   output x;
10  assign x=a|p;
11  endmodule
12
13  module circuit_2(x,a,c,b);
14  input a,c,b;
15  output x;
16  wire p;
17  and2 and2_1(p,b,c);
18  or2 or2_1(x,a,p);
19  endmodule
20
21  module w2cir1(y,a,b,c);
22  input a,b,c;
23  output y;
24  wire x;
25  circuit_2 circuit2_1(x,a,b,c);
26  circuit_2 circuit2_2(y,x,b,a);
27  endmodule
```

w2cir1_tb.v

```
1   module w2cir1_tb;
2   reg a,b,c;
3   wire y;
4   w2cir1 cir1_test(y,a,b,c);
5   initial
6   begin
7   a=0;b=0;c=0; #10;
8   a=0;b=0;c=1; #10;
9   a=0;b=1;c=0; #10;
10  a=0;b=1;c=1; #10;
11  a=1;b=0;c=0; #10;
12  a=1;b=0;c=1; #10;
13  a=1;b=1;c=0; #10;
14  a=1;b=1;c=1; #10;
15  a=0;b=0;c=0; #10;
16  end
17  initial
18  begin
19  $monitor($time," a=%b b=%b c=%b  y=%b",a,b,c,y);
20  end
21  initial
22  begin
23  $dumpfile("w2_test.vcd");
24  $dumpvars(0,w2cir1_tb);
25  end
26  endmodule
```

```
PS C:\iverilog\bin> iverilog -o test w2cir2.v w2cir1_tb.v
PS C:\iverilog\bin> vvp test
VCD info: dumpfile w2_test.vcd opened for output.
                   0 a=0 b=0 c=0  y=0
                  10 a=0 b=0 c=1  y=0
                  20 a=0 b=1 c=0  y=0
                  30 a=0 b=1 c=1  y=1
                  40 a=1 b=0 c=0  y=1
                  50 a=1 b=0 c=1  y=1
                  60 a=1 b=1 c=0  y=1
                  70 a=1 b=1 c=1  y=1
                  80 a=0 b=0 c=0  y=0
PS C:\iverilog\bin>
```

GTK WAVE: