RISC-V Exceptions and Interrupts

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1 Privilege Modes and Control Status Registers

RISC-V supports three different privilege modes: M-mode (highest priority), S-mode, and U-mode (lowest priority). Currently, hypervisor-mode (H-mode) is reserved and is not a formal part of the RISC-V ISA. RISC-V also supports an optional debug mode (D-mode) for off-chip debugging that can be considered to be an additional privilege mode with more access than M-mode. Code run in machine-mode (M-mode) is usually inherently trusted, as it has low-level access to the machine implementation. M-mode can be used to manage secure execution environments on RISC-V. User-mode (U-mode) and supervisor-mode (S-mode) are intended for conventional application and operating system usage respectively. Privilege-level actions like exception and interrupt handling rely on a set of control and status registers (CSRs). Each privilege mode supports a set of privilege-specific CSRs for the privilege-specific trap handlers. In this document, CSRs or fields in CSRs prefixed with an *x* refer to the possibility that CSRs can have three privilege-specific implementations: M-mode (x = m), S-mode (x = s), and U-mode (x = u). These privilege-specific CSRs are controlled by their respective privilege-specific trap handlers.

2 Exceptions and Interrupts

RISC-V defines exceptions as an unusual condition occurring at run time associated with an instruction in the current hart. Exceptions can be organized into six different categories: fetch, load, store, misaligned jump/branch (i.e misaligned instruction address), illegal instruction, and ECALL/EBREAK. Interrupts refer to an external, asynchronous event that may cause the RISC-V hart to experience an unexpected transfer of control. Interrupts are organized into three different categories: external, software, and timer. External interrupts are raised by devices connected to the processor, software interrupts are raised by programs, and timer interrupts are raised when the value in the `xtime` CSR is greater than or equal the value in the `xtimecmp` CSR. For multi-hart systems, interrupts also rely on an inter-processor interface (see Section 6) to handle interrupts between multiple harts.

3 Exception Handling

3.1 M-Mode Exceptions

If an exception occurs, control is relinquished by the program that is currently being executed and transferred to the trap handler. The trap handler can be thought of as a software function call the program executes in response to an erroneous hardware event. During this function call the program jumps to an address and writes to a set of CSRs before resuming the program at the location that raised the exception. Before an exception can be raised and handled, the trap handler must be initialized. By default, M-mode, S-mode, and U-mode exceptions are handled by the M-mode trap handler. Software initializes the M-mode trap handler by setting the `mtvec` CSR (see Figure 4 in the Appendix). The `mtvec` CSR contains a base address and a mode field. This mode field supports two options: direct and vectored. For both modes, the program counter is set to the base address in `mtvec`. This is the address where the M-mode trap handler is located.

Once the program jumps to the M-mode trap handler, the `mepc`, `mstatus`, `mtval`, and `mcause` CSRs are set before the program exits the trap handler and resumes execution at the instruction that raised the exception. The `mepc` CSR (see Figure 5 in the Appendix) is written with the virtual address of the instruction that took the trap. This address is stored so that the program can be returned to and resumed after the trap handler is finished. In M-mode, the two-bit MPP field in mstatus (see Figure 6 in the Appendix) is written with the privilege level encoding corresponds to the privilege level the program was in when the exception was raised. MPP can hold three values: 11 (M-mode), 01 (S-mode), and 00 (U-mode). In addition so setting MPP, the 1-bit MPIE field is set the the value in the 1-bit MIE field before the MIE field is set to zero. These fields in mstatus do not effect exception handling and are only changed so that trap handler does not process more than one interrupt at a time. The mtval CSR (see Figure 7 in the Appendix) is written with exception-specific information. For EBREAKs, misaligned addresses, access faults, and page faults, mtval will contain the faulting virtual address. When page-based virtual memory is enabled, mtval is written with the faulting virtual address, even for physical-memory access exceptions. For illegal instructions, mtval contains the faulting instruction bits of the illegal instruction i.e the faulting instruction. The mcause CSR (see Figure 8 in the Appendix) is written with the exception cause code that corresponds to the exception that was raised. If an instruction raises multiple synchronous exceptions, the exceptions are taken by the trap handler and reported in mcause according to a pre-defined priority structure. After these CSRs are set, the trap handler executes an MRET instruction to jump back to the address stored in mepc so that the program can resume. During this time, MRET also sets MIE to the value in MPIE before setting MPIE to one to indicate that the trap handler is ready for the next interrupt.

3.2 S-Mode Exceptions

Exceptions raised in S-mode can be handled in M-mode or delegated to S-mode through the medeleg CSR (see Figure 9 in the Appendix). Delegating to S-mode means that only S-mode CSRs are visible in hardware and exceptions are processed by the S-mode trap handler. The medeleg CSR delegates exceptions by raising the bits in positions that correspond to exception code numbers. This delegation process can be expressed by a single line of Verilog code as shown below.

```
assign dCSR_medeleg = 32'b1 << exception_cause_code; // Set medeleg
```

Software initializes the S-mode trap handler by setting the stvec CSR (see Figure 10 in the Appendix). The stvec CSR contains a base address and a mode field. This mode field supports two options: direct and vectored. For both modes, the program counter is set to the base address in stvec. This is the address where the S-mode trap handler is located.

Once the program jumps to the S-mode trap handler, the sepc, mstatus, stval, and scause CSRs are set before the program exits the trap handler and resumes execution at the instruction that raised the exception. The sepc CSR (see Figure 11 in the Appendix) is written with the virtual address of the instruction that took the trap. This address is stored so that the program can be returned to and resumed after the trap handler is finished. In S-mode, the two-bit SPP field in mstatus[1] is written with the privilege level encoding corresponds to the privilege level the program was in when the exception was raised. SPP can hold two values: 1 (S-mode) or 0 (U-mode). In addition to setting SPP, the 1-bit SPIE field is set the the value in the 1-bit SIE field before the SIE field is set to zero. These fields in mstatus do not effect exception handling and are only changed so that trap handler does not process more than one interrupt at a time. The stval CSR (see Figure 12 in the Appendix) is written with exception-specific information. For EBREAKs, misaligned addresses, access faults, and page faults, stval will contain the faulting virtual address.

[1] S-mode and U-mode can utilize mstatus instead of sstatus and ustatus. These CSRs simply restrict the higher privilege level fields from being visible to hardware.

When page-based virtual memory is enabled, stval is written with the faulting virtual address, even for physical-memory access exceptions. For illegal instructions, stval contains the faulting instruction bits of the illegal instruction i.e the faulting instruction. The scause CSR (see Figure 13 in the Appendix) is written with the exception cause code that corresponds to the exception that was raised. If an instruction raises multiple synchronous exceptions, the exceptions are taken by the trap handler and reported in scause according to a pre-defined priority structure. After these CSRs are set, the trap handler executes an SRET instruction to jump back to the address stored in sepc so that the program can resume. During this time, SRET also sets SIE to the value in SPIE before setting SPIE to one to indicate that the trap handler is ready for the next interrupt.

3.3 U-Mode Exceptions

Exceptions raised in U-mode can be handled in M-mode, delegated to S-mode through the medeleg CSR, or delegated to U-mode through the sedeleg CSR (see Figure 14 in the Appendix). Delegating to U-mode means that only U-mode CSRs are visible in hardware and exceptions are processed by the U-mode trap handler as shown in Figure 1. The sedeleg CSR delegates exceptions that first must be delegated by the medeleg CSR by raising the bits in positions that correspond to exception code numbers. This delegation process can be expressed by two lines of Verilog code as shown below.

```
assign dCSR_medeleg = 32'b1 << exception_cause_code; // Set medeleg
assign dCSR_sedeleg = 32'b1 << exception_cause_code; // Set sedeleg
```

Software initializes the U-mode trap handler by setting the utvec CSR (see Figure 15 in the Appendix). The utvec CSR contains a base address and a mode field. This mode field supports two options: direct and vectored. For both modes, the program counter is set to the base address in utvec. This is the address where the U-mode trap handler is located.

Once the program jumps to the S-mode trap handler, the uepc, mstatus, utval, and ucause CSRs are set before the program exits the trap handler and resumes execution at the instruction that raised the exception. The uepc CSR (see Figure 16 in the Appendix) is written with the virtual address of the instruction that took the trap. This address is stored so that the program can be returned to and resumed after the trap handler is finished. The mstatus CSR does not include a UPP field for U-mode since it is implicitly set to zero. However, mstatus does include 1-bit SPIE and SIE fields where the SPIE field is set the the value in the SIE field before the SIE field is set to zero. These fields in mstatus do not effect exception handling and are only changed so that trap handler does not process more than one interrupt at a time. The utval CSR (see Figure 17 in the Appendix) is written with exception-specific information. For EBREAKs, misaligned addresses, access faults, and page faults, utval will contain the faulting virtual address. When page-based virtual memory is enabled, utval is written with the faulting virtual address, even for physical-memory access exceptions. For illegal instructions, utval contains the faulting instruction bits of the illegal instruction i.e the faulting instruction. The ucause CSR (see Figure 18 in the Appendix) is written with the exception cause code that corresponds to the exception that was raised. If an instruction raises multiple synchronous exceptions, the exceptions are taken by the trap handler and reported in ucause according to a pre-defined priority structure. After these CSRs are set, the trap handler executes an URET instruction to jump back to the address stored in uepc so that the program can resume. During this time, URET also sets UIE to the value in UPIE before setting UPIE to one to indicate that the trap handler is ready for the next interrupt.

Priority	Exception Code	Description
Highest	12	Instruction Page Fault
	1	Instruction Access Fault
	2	Illegal Instruction
	0	Instruction Address Misaligned
	8, 9, 11	Environment Call (U, S, M)
	3	Environment Break
	6	Store/AMO Address Misaligned
	4	Load Address Misaligned
	15	Store/AMO Page Fault
	13	Load Page Fault
	7	Store/AMO Access Fault
Lowest	5	Load Access Fault

Table 1: Exception Priorities Priorities

3.4 Exception Priority

If an instruction raises multiple synchronous exceptions, the decreasing priority order of Table 1 indicates which exception is taken. Synchronous exceptions are of lower priority than all interrupts and the priority of any custom synchronous exceptions is implementation-defined.

4 Exception Definitions

4.1 Misaligned Addresses

Misaligned instruction addresses is a misleading term that refers to misaligned branch and jump targets. The misaligned instruction address should be called misaligned branch/jump target. Misaligned instruction addresses are raised when the target of a jump or branch instruction is not aligned to a 4-byte boundary or an 8-byte boundary. 4-byte alignments are associated with RV32 systems and 8-byte alignments are associated with RV64 systems. 2-byte alignments are also possible for 16-bit instruction implementations but this is a customer instruction encoding that is not a formal part of the RISC-V ISA. Misaligned loads/store addresses are raised when the data the load/store instruction accesses from memory is not aligned to the correct byte offset. In general, a data of size s bytes at byte address A is aligned if $A \bmod s = 0$.

4.2 Access Faults

Instruction, load, and store/AMO access faults are raised from failed physical memory protection checks. Physical memory protection (PMP) checks verify that the instruction is accessed from a valid address in memory by the hardware. Access fault exceptions rely on bits L, X, R, and W in an 8-bit PMP configuration register. Bits X, R, and W encode execute, read, and write privileges respectively. The L-bit indicates that the PMP entry is locked, i.e., writes to the configuration register (see Figure 19 in the Appendix) and associated address registers are ignored. In addition to locking the PMP entry, the L bit indicates whether the R/W/X permissions are enforced on M-mode accesses. When the L bit is set, these permissions are enforced for all privilege modes. When the L bit is clear, any M-mode access matching the PMP entry will succeed and the R/W/X

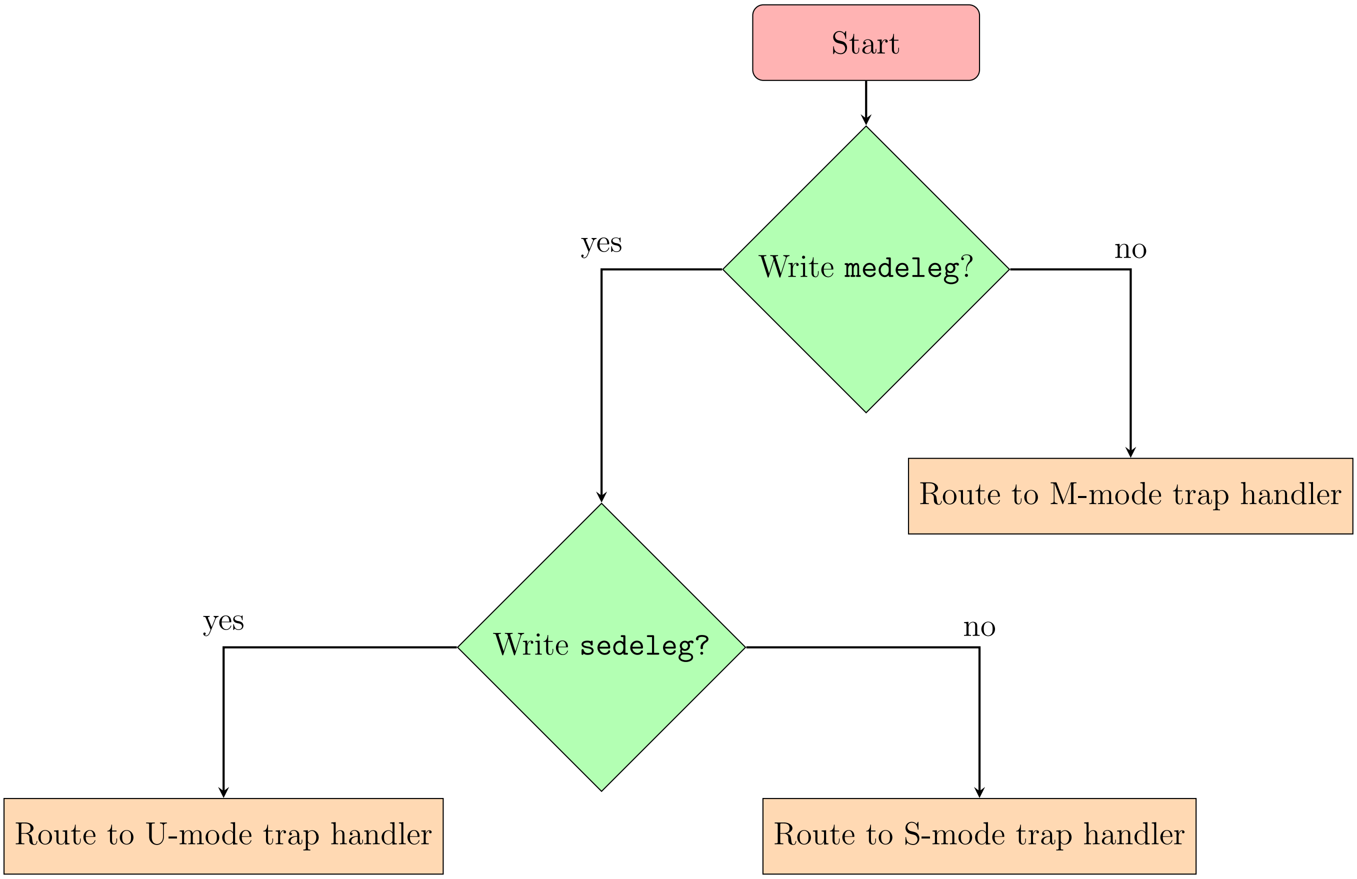
Start
Write medeleg?
yes
no
Route to M-mode trap handler
Write sedeleg?
yes
no
Route to U-mode trap handler
Route to S-mode trap handler

Figure 1: Flow Chart of Delegation Process

permissions only apply to S and U modes. Access fault exceptions can only be raised if the L-bit is set or the access is in S-mode or U-mode. Attempting to fetch an instruction whose physical address lies in a PMP region that does not have execute permissions (X = 0) raises a fetch access exception. Attempting to execute a load or load-reserved instruction whose physical address lies within a PMP region without read permissions (R = 0) raises a load access exception. Attempting to execute a store, store-conditional (regardless of success), or AMO instruction whose physical address lies within a PMP region without write permissions (W = 0) raises a store access exception.

4.3 Illegal Instructions

Illegal instructions are raised by illegal instruction encodings or problems reading from and writing to certain CSRs. The following is a non-exhaustive list of illegal instructions that could be raised:

- Instructions with bits [15:0] set to zero, this is a reserved bit pattern
- Instructions with bits [ILEN-1:0][2] set to one, this a reserved bit pattern
- Bit patterns that the processor does not recognize (ex. multiply or divide)
- Instructions that set rd = x0 with the exception of CSRRW, CSRRWI, JALR, and JAL
- Attempts to write to a read-only CSR
- Attempts to access CSRs from non-exsistent CSR addresses
- Attempts to access a CSR without appropriate privilege level permissions
- Machine-mode access of debug-mode CSRs
- Attempts to read or write the `satp` CSR or execute the SFENCE.VMA instruction while executing in S-mode when the TVM bit in the `xstatus` CSR equals one
- Attempts to execute the WFI privilege instruction in any less-privileged mode, and it does not complete within an implementation-specific, bounded time limit[3] when the TW bit in the `mstatus` CSR equals one
- Attempts to execute SRET while executing in S-mode when the TSR bit in the `xstatus` register equals one
- Any instruction that attempts to read or write when the corresponding XS[1:0] field in the `xstatus` CSR is set to zero
- Attempts to read to the counter registers that correspond to the IR, TM, and CY bits in the `mcounteren` CSR when executing in a less-privileged mode

[2] ILEN is the maximum length of the maximum instruction length supported by an implementation. For RISC-V, ILEN is typically 32 or 64 bits.

[3] The time limit may always be zero, in which case WFI always causes an illegal instruction exception in less-privileged modes when TW equals one

4.4 Environment Call and Environment Break

The environment call instruction (ECALL) is used to make a request to the supporting execution environment. When executed in U-mode, S-mode, or M-mode, it generates an environment-call-from-U-mode exception, environment-call-from-S-mode exception, or environment-call-from-M-mode exception, respectively, and performs no other operation. Similarly, the environment break instruction (EBREAK) raises an exception as part of the instruction execution.

4.5 Page Faults

For RV32 systems, the supervisor has a 32-bit, page-based virtual memory system called Sv32. RISC-V identifies three different types of page faults: instruction, load, and store/AMO. Instruction page faults are raised by attempting to fetch an instruction from a page that does not have execute permissions. Load page faults are raised by load or load-reserved instructions whose address lies within a page without read permissions. Store/AMO page faults are raised by store, store-conditional, or AMO instruction whose effective address lies within a page without write permissions. In other words, all instructions can raise instruction page faults, load instructions can only raise load page faults, and store instruction can only raise store page faults. This means that load and store page faults also raise instruction page faults.

The following lists a number of error that can raise a page fault exception that corresponds to the original access type (instruction, load, and store) during the Sv32 virtual to physical address translation process:

- The physical address of the page is insufficiently aligned
- PTE bit V = 0, or PTE bit R = 0 and PTE bit W = 1
- R, W, and X are zero when the page walk is on level two
- Accessing a page in U-mode when the PTE bit U != 1
- Attempting to execute S-mode code on page where the PTE bit U = 1
- Attempting to execute loads from pages where R = 0 and X = 0 for MXR = 1 in `mstatus`
- S-mode accesses of pages that are accessible in U-mode (U = 1) when the SUM field in `mstatus` is cleared
- PTE bit A = 0, or if the memory access is a store and PTE bit D = 0

5 Exception Table

The exceptions in Table 2 fall under the following categories fetch, load, store, misaligned branch/jump, rd != x0 illegal instruction, and ECALL/EBREAK. Fetch exceptions encompass instruction access faults and instruction page faults. Load exceptions encompass misaligned load addresses, load access faults, and load page faults. Store exceptions encompass misaligned store addresses, store access faults, and store page faults. Unless otherwise specified, the fetch, store, and load categories encompass all the respective exceptions included in each category. Misaligned branch/jump exceptions are raised by jump and branch instructions according to the definition for misaligned instruction addresses. EBREAK/ECALL exceptions are raised according to the definitions of environment call and environment break.

Instruction	Fetch	Load	Store	Misaligned Branch/Jump	rd != x0	ECALL/EBREAK
LUI	×				×	
AUIPC	×				×	
JAL	×			×		
JALR	×			×		
BEQ	×			×		
BNE	×			×		
BLT	×			×		
BGE	×			×		
BLTU	×			×		
BGEU	×			×		
LB	×	×			×	
LH	×	×			×	
LW	×	×			×	
LBU	×	×			×	
LHU	×	×			×	
SB	×		×			
SH	×		×			
SW	×		×			
ADDI	×				×	
SLTI	×				×	
SLTIU	×				×	
XORI	×				×	
ORI	×				×	
ANDI	×				×	
SLLI	×				×	
SRLI	×				×	
SRAI	×				×	
ADD	×				×	
SUB	×				×	
SLL	×				×	
SLT	×				×	
SLTU	×				×	
XOR	×				×	
SRL	×				×	
SRA	×				×	
OR	×				×	
AND	×				×	
ECALL	×					×
EBREAK	×					×

Table 2: Possible Exceptions for the RV32I Instruction Set

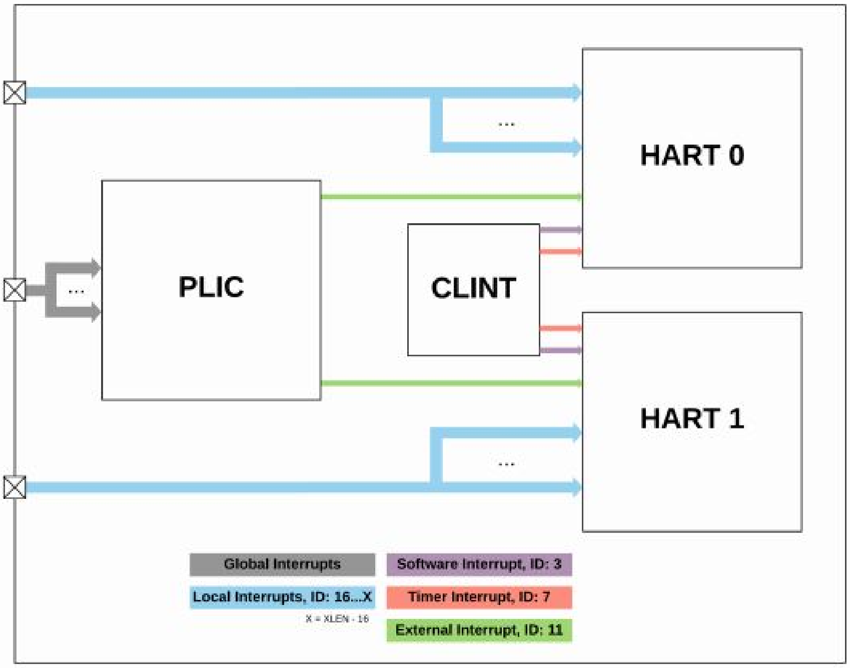
HART 0
PLIC
CLINT
HART 1
...
Global Interrupts
Local Interrupts, ID: 16...X
X = XLEN - 16
Software Interrupt, ID: 3
Timer Interrupt, ID: 7
External Interrupt, ID: 11

Figure 2: Block diagram of an example PLIC and CLINT configuration

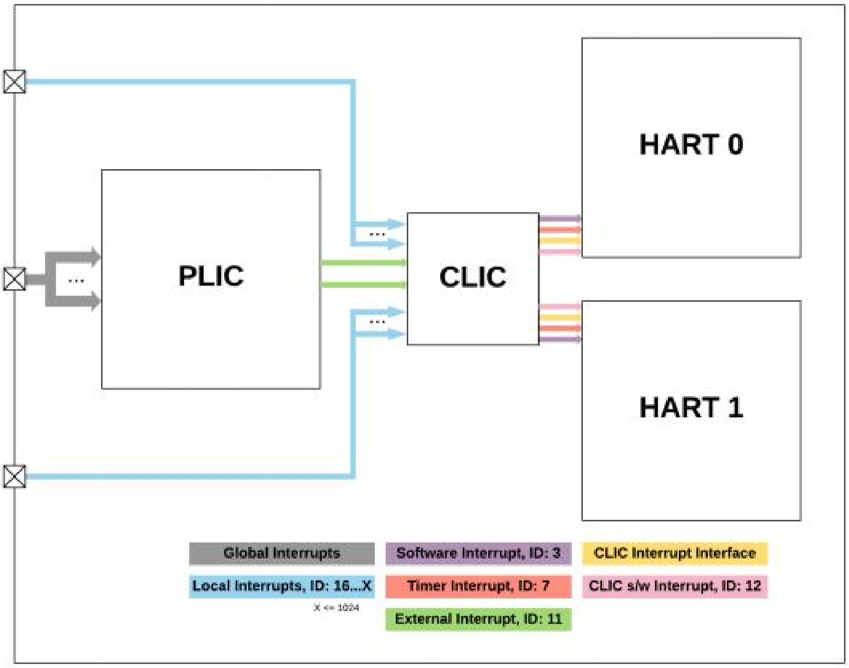
HART 0
PLIC
CLIC
HART 1
...
Global Interrupts
Local Interrupts, ID: 16...X
X <= 1024
Software Interrupt, ID: 3
Timer Interrupt, ID: 7
External Interrupt, ID: 11
CLIC Interrupt Interface
CLIC s/w Interrupt, ID: 12

Figure 3: Block diagram of an example PLIC and CLIC configuration

6 Interrupt Handling

6.1 PLIC, CLINT, and CLIC

Interrupt handling is similar to exception handling but there are some notable differences. Unlike exceptions, interrupts require additional hardware. This additional hardware includes a RISC-V Platform Level Interrupt Controller (PLIC) [1] and the option of a SiFive Core-local Interrupter (CLINT) [2] or a RISC-V Core-local Interrupt Controller (CLIC) [3]. The PLIC sources external interrupts from devices and routes them to the hart(s) as shown in Figure 2. Similarly, the CLINT sources local software and timer interrupts and routes them to the hart(s). Unlike the CLINT, the CLIC routes external, software, and timer interrupt signals to the hart(s) as shown in Figure 3. RISC-V has defined detailed CLIC and PLIC specifications that explain the interrupt control flow and define the different registers that are used to handle interrupts. For systems with multiple harts, the Wait for Interrupt (WFI) instruction can be implemented to control interrupt servicing between multiple harts by stalling a hart. If an enabled interrupt is present or later becomes present while the hart is stalled, the interrupt exception will be taken on the following instruction.

6.2 M-Mode Interrupts

If an interrupt occurs, control is relinquished by the program that is currently being executed and transferred to the trap handler. Before an interrupt can be raised and handled, the trap handler must be initialized and the interrupts must be enabled. By default, M-mode, S-mode, and U-mode interrupts are handled by the M-mode trap handler. Software initializes the M-mode trap handler by setting the `mtvec` CSR. The `mtvec` CSR contains a base address and a mode field. This mode field supports two options: direct and vectored. In direct mode, the program counter is set to the base address in `mtvec`. For vectored mode, the program counter is set to the base address plus four times the interrupt cause code as shown in Table 3[4]. In both cases, these are the address where the M-mode trap handler can be located. Interrupts are said to be enabled if they are enabled by the `mie` (see Figure 20 in the Appendix) and `mstatus` CSRs. External interrupts in M-mode, S-mode, and U-mode are enabled by raising the 1-bit MEIE, SEIE, and UEIE fields in `mie` respectively. Timer interrupts in M-mode, S-mode, and U-mode are enabled by raising the 1-bit MTIE, STIE, and UTIE fields in `mie` respectively. Software interrupts in M-mode, S-mode, and U-mode are enabled by raising the 1-bit MSIE, SSIE, and USIE fields in `mie` respectively. In addition to being enabled by raising bits in `mie`, M-mode, S-mode, and U-mode interrupts can also be globally enabled. M-mode interrupts are globally enabled if the current privilege mode is less than M or the current privilege mode is M and the 1-bit MIE field in `mstatus` is set. S-mode interrupts are globally enabled if the current privilege mode is less the S or the current privilege mode is S and the 1-bit SIE field in `mstatus` is set. U-mode interrupts are globally enabled if the current privilege mode is U and the 1-bit UPP field in `mstatus` is set.

The interrupt controllers are responsible for identifying pending interrupts that are received by the hart(s). M-mode external, software, and timer interrupts are raised by setting the 1-bit MEIP, MSIP, and MTIP fields in the `mip` CSR (see Figure 21 in the Appendix) respectively. S-mode external, software, and timer interrupts are raised by setting the 1-bit SEIP, SSIP, and STIP fields in the `mip` register respectively. U-mode external, software, and timer interrupts are raised by

[4] When vectored interrupts are enabled, interrupt cause 0, which corresponds to user-mode software interrupts, are vectored to the same location as synchronous exceptions. This ambiguity does not arise in practice, since user-mode software interrupts are either disabled or delegated to a less-privileged mode.

Interrupt	BASE + $4 * cause$
User Software Interrupt	BASE
Supervisor Software Interrupt	BASE + 0x4
Reserved	BASE + 0x8
Machine Software Interrupt	BASE + 0xC
User Timer Interrupt	BASE + 0x10
Supervisor Timer Interrupt	BASE + 0x14
Reserved	BASE + 0x18
Machine Timer Interrupt	BASE + 0x1C
User External Interrupt	BASE + 0x20
Supervisor External Interrupt	BASE + 0x24
Reserved	BASE + 0x28
Machine External Interrupt	BASE + 0x2C

Table 3: Interrupt Vector Table

setting the 1-bit UEIP, USIP, and UTIP fields in the `mip` register respectively. Raising an interrupt causes the M-mode trap handler to take control of the program. Interrupts processed by the M-mode trap handler are processed in the same manner as exceptions as specified in Section 3.1. The only difference is that interrupts do not set `mtval` and it is therefore left cleared.

6.3 S-Mode Interrupts

Interrupts raised in S-mode can be handled in M-mode or delegated to S-mode through the `mideleg` CSR. Delegating to S-mode means that only S-mode CSRs are visible in hardware and interrupts are processed by the S-mode trap handler. The S-mode trap handler can process S-mode and U-mode interrupts. Software initializes the S-mode trap handler by setting the `stvec` CSR. The `stvec` CSR contains a base address and a mode field. This mode field supports two options: direct and vectored. In direct mode, the program counter is set to the base address in `stvec`. For vectored mode, the program counter is set to the base address plus four times the interrupt cause code. In both cases, these are the address where the S-mode trap handler can be located. Interrupts are said to be enabled if they are enabled by the `mie`[5] and `mstatus` CSRs. External interrupts in S-mode and U-mode are enabled by raising the 1-bit SEIE and UEIE fields in `mie` respectively. Timer interrupts in S-mode and U-mode are enabled by raising the 1-bit STIE and UTIE fields in `mie` respectively. Software interrupts in S-mode and U-mode are enabled by raising the 1-bit SSIE and USIE fields in `mie` respectively. In addition to being enabled by raising bits in `mie`, S-mode and U-mode interrupts can also be globally enabled. S-mode interrupts are globally enabled if the current privilege mode is less the S or the current privilege mode is S and the 1-bit SIE field in `mstatus` is set. U-mode interrupts are globally enabled if the current privilege mode is U and the 1-bit UPP field in `mstatus` is set.

The interrupt controllers are responsible for identifying pending interrupts that are received by the hart(s). S-mode external, software, and timer interrupts are raised by setting the 1-bit SEIP, SSIP, and STIP fields in the `mip` CSR respectively. U-mode external, software, and timer interrupts are raised by setting the 1-bit UEIP, USIP, and UTIP fields in the `mip` register respectively. Raising

[5] S-mode and U-mode can utilize `mie` instead of `sie` and `uie`. These CSRs simply restrict the higher privilege level fields from being visible to hardware. This also holds true for `mie` relative to `sie` and `uie`.

Priority	Exception Code	Description
Highest	11	Machine External Interrupt
	3	Machine Software Interrupt
	7	Machine Timer Interrupt
	9	Supervisor External Interrupt
	1	Supervisor Software Interrupt
	5	Supervisor Timer Interrupt
	8	User External Interrupt
	0	User Software Interrupt
Lowest	4	User Timer Interrupt

Table 4: Interrupt Priorities

an interrupt causes the S-mode trap handler to take control of the program. Interrupts processed by the S-mode trap handler are processed in the same manner as exceptions as specified in Section 3.2. The only difference is that interrupts do not set `stval` and it is therefore left cleared.

6.4 U-Mode Interrupts

Interrupts raised in U-mode can be handled in M-mode, delegated to S-mode through the `mideleg` CSR, or delegated to U-mode through the *sideleg* CSR. Delegating to U-mode means that only U-mode CSRs are visible in hardware and interrupts are processed by the U-mode trap handler. The U-mode trap handler can only process U-mode interrupts. Software initializes the U-mode trap handler by setting the `utvec` CSR. The `utvec` CSR contains a base address and a mode field. This mode field supports two options: direct and vectored. In direct mode, the program counter is set to the base address in `utvec`. For vectored mode, the program counter is set to the base address plus four times the interrupt cause code. In both cases, these are the address where the U-mode trap handler can be located. Interrupts are said to be enabled if they are enabled by the `mie` and `mstatus` CSRs. External interrupts U-mode are enabled by raising the 1-bit UEIE field in `mie`. Timer interrupts in U-mode are enabled by raising the 1-bit UTIE field in `mie`. Software interrupts in U-mode are enabled by raising the 1-bit USIE field in `mie`. In addition to being enabled by raising bits in `mie`, U-mode interrupts can also be globally enabled. U-mode interrupts are globally enabled if the current privilege mode is U and the 1-bit UPP field in `mstatus` is set.

The interrupt controllers are responsible for identifying pending interrupts that are received by the hart(s). U-mode external, software, and timer interrupts are raised by setting the 1-bit UEIP, USIP, and UTIP fields in the `mip` CSR respectively. Raising an interrupt causes the U-mode trap handler to take control of the program. Interrupts processed by the U-mode trap handler are processed in the same manner as exceptions as specified in Section 3.3. The only difference is that interrupts do not set `utval` and it is therefore left cleared.

6.5 Interrupt Priority

Like exception, simultaneous interrupts are processed by the trap handler according to a fixed priority structure as show in Table 4. The exception codes for interrupts are differentiated from the exception codes for exceptions with a 1-bit interrupt field in the MSB of `xcause`. Raising this field indicates that the exception code in `xcause` is for an interrupt.

7 CSR Appendix

MXLEN-1 2	1 0
BASE[MXLEN-1:2] (**WARL**)	MODE (**WARL**)
MXLEN-2	2

Figure 4: Machine trap-vector base-address register (`mtvec`).

MXLEN-1 0
`mepc`
MXLEN

Figure 5: Machine exception program counter register.

31	30 23	22	21	20	19	18	17
SD	**WPRI**	TSR	TW	TVM	MXR	SUM	MPRV
1	8	1	1	1	1	1	1

16 15	14 13	12 11	10 9	8	7	6	5	4	3	2	1	0
XS[1:0]	FS[1:0]	MPP[1:0]	**WPRI**	SPP	MPIE	**WPRI**	SPIE	UPIE	MIE	**WPRI**	SIE	UIE
2	2	2	2	1	1	1	1	1	1	1	1	1

Figure 6: Machine-mode status register (`mstatus`) for RV32.

MXLEN-1 0
`mtval`
MXLEN

Figure 7: Machine Trap Value register.

MXLEN-1	MXLEN-2 0
Interrupt	Exception Code (**WLRL**)
1	MXLEN-1

Figure 8: Machine Cause register `mcause`.

MXLEN-1 0
Synchronous Exceptions (**WARL**)
MXLEN

Figure 9: Machine Exception Delegation Register `medeleg`.

SXLEN-1 2	1 0
BASE[SXLEN-1:2] (**WARL**)	MODE (**WARL**)
SXLEN-2	2

Figure 10: Supervisor trap vector base address register (`stvec`).

SXLEN-1 0
`sepc`
SXLEN

Figure 11: Supervisor exception program counter register.

SXLEN-1 0
`stval`
SXLEN

Figure 12: Supervisor Trap Value register.

SXLEN-1	SXLEN-2 0
Interrupt	Exception Code (**WLRL**)
1	SXLEN-1

Figure 13: Supervisor Cause register `scause`.

SXLEN-1 0
Synchronous Exceptions (**WARL**)
SXLEN

Figure 14: Supervisor Exception Delegation Register `sedeleg`.

UXLEN-1 2	1 0
BASE[UXLEN-1:2] (**WARL**)	MODE (**WARL**)
UXLEN-2	2

Figure 15: User trap vector base address register (`utvec`).

UXLEN-1 0
`uepc`
UXLEN

Figure 16: User exception program counter register.

UXLEN-1 0
`utval`
UXLEN

Figure 17: User Trap Value register.

UXLEN-1	UXLEN-2 0
Interrupt	Exception Code (**WLRL**)
1	UXLEN-1

Figure 18: User Cause register `ucause`.

7	6 5	4 3	2	1	0
L (**WARL**)	0 (**WARL**)	A (**WARL**)	X (**WARL**)	W (**WARL**)	R (**WARL**)
1	2	2	1	1	1

Figure 19: PMP configuration register format.

MXLEN-1   0
Interrupts (**WARL**)
MXLEN

Figure 20: Machine Interrupt-Enable Register (`mie`).

MXLEN-1   0
Interrupts (**WARL**)
MXLEN

Figure 21: Machine Interrupt-Pending Register (`mip`).

MXLEN-1   0
Interrupts (**WARL**)
MXLEN

Figure 22: Machine Interrupt Delegation Register `mideleg`.

SXLEN-1   0
Interrupts (**WARL**)
SXLEN

Figure 23: Supervisor Interrupt Delegation Register `sideleg`.

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