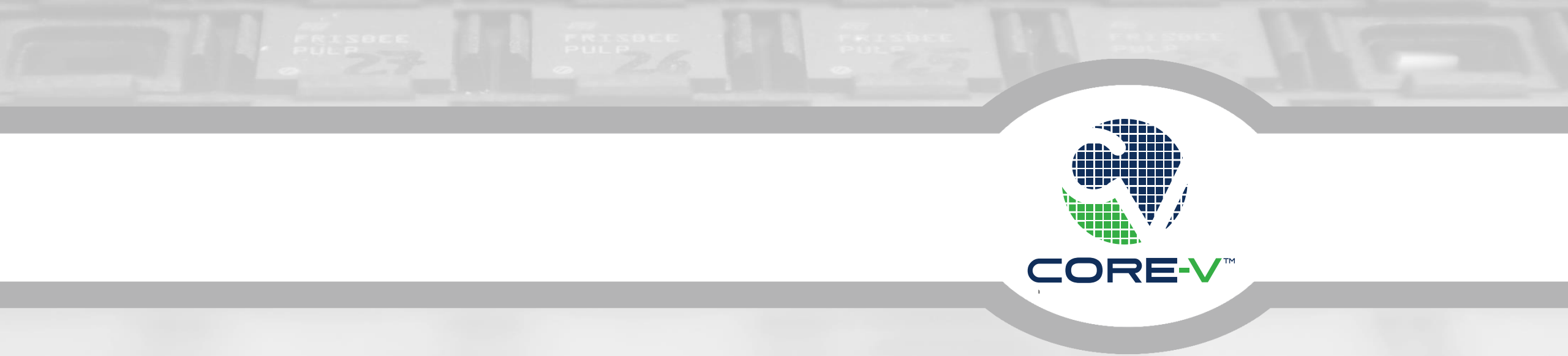


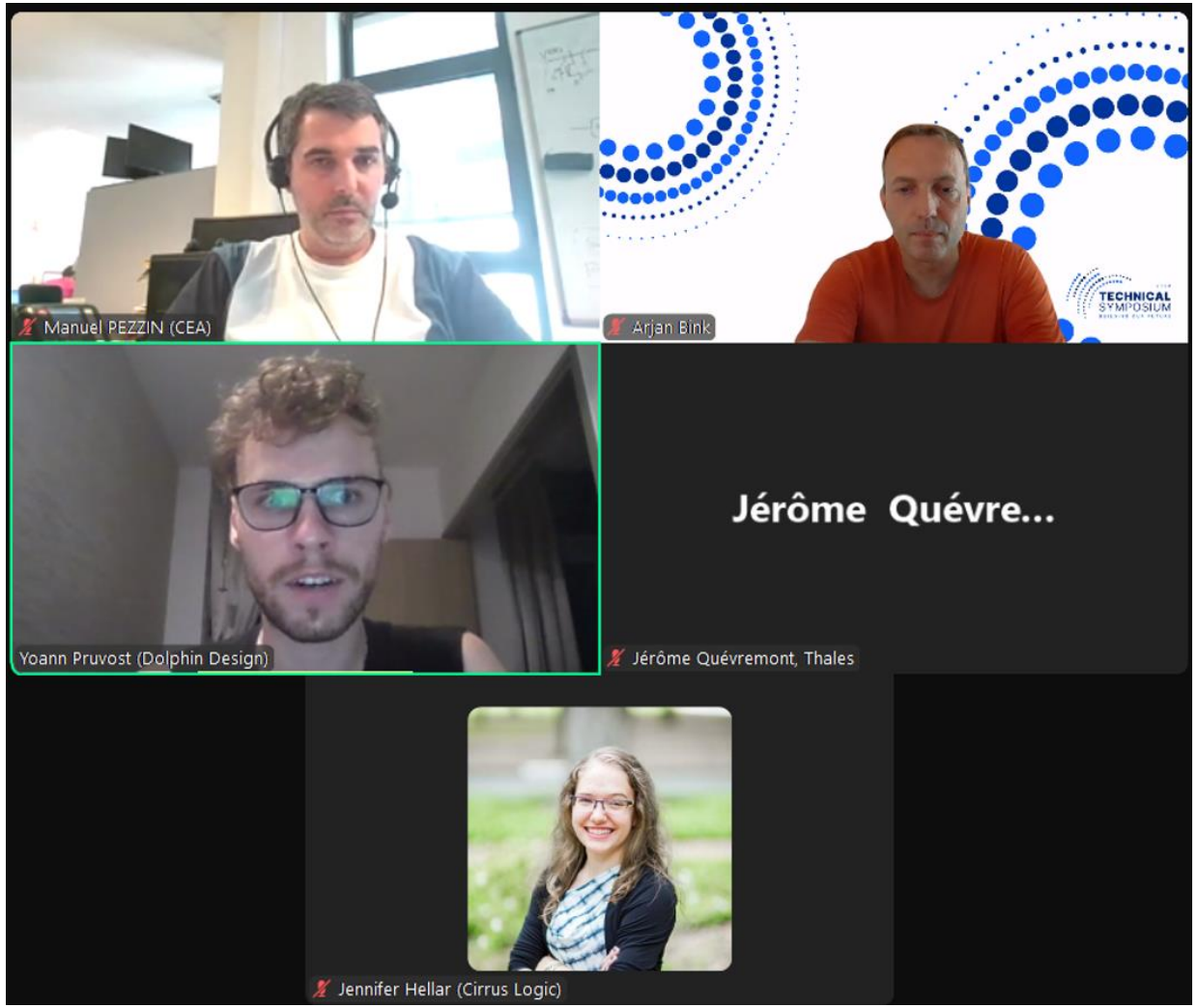
CORES TG – July 1 2024

Arjan Bink

Jérôme Quevremont

Davide Schiavone

Attendance


Manuel PEZZIN (CEA)
Arjan Bink
TECHNICAL SYMPOSIUM
Yoann Pruvost (Dolphin Design)
Jérôme Quévre...
Jérôme Quévremont, Thales
Jennifer Hellar (Cirrus Logic)

Agenda

- CV32E40Pv2: final RTL Freeze status (Yoann Pruvost)
- CV32E40PX: CV32E40P SIMD datapath refactoring (preparation work for RVP extensions support) (Manuel Pezzin)

CV32E40Pv2 final RTL Freeze status

Pascal Gouédo

Yoann Pruvost

Bee Nee Lim

OPENHW GROUP™
PROVEN PROCESSOR IP

July 1st, 2024

Project

- Project
  - Design & Verification meeting
    - Wednesday 14:00 CET every week (Ical)
  - Dedicated technical meetings when needed
  - Reporting to Cores TG

- Mattermost channels
  - TWG : Cores : CV32E4*P
  - TWG : Verification

- Resources
  - Pascal Gouédo
    - Specification, Design, Verification & Formal
  - Yoann Pruvost
    - Design, Verification & Formal
  - Bee Nee Lim
    - Verification leader
  - Xavier Aubert
    - Verification
  - Bao Shan Mak
    - Verification

- OpenHW staff
  - Mike Thompson
    - Verification support
  - Davide Schiavone
    - Architecture & Design support

User Manual

- dev branch merged to master
  Release and User Manual created from master branch

- v1.8.2
  - Update pointer to v1.0.0 coverage reports (PR #989)
  - Verification section update (PR #992)
- v1.8.3
  - Debug request management +
    Additional verification section update

Design

- No remaining opened or non-explained issues

- Last tag with RTL updates: v1.8.0

Verification : Non-regressions

- v1.8.3 RTL tag & v1.8.3 core-v-verif tag
- Non-regression results
  - Riscof Architecture tests passing on 4 PULP & PULP_FPU configurations
  - 4 non-regressions ran on 7 configurations
    - Total of 27 non-regressions
  - 32682 tests run, 4 failing tests
    - 2 new ISS mismatches on corner cases
    - 2 timeout

Verification : Coverage results

- Simulation RTL Code Coverage results
  - PULP configuration

    Statement: 99.8% Branch: 99.6% Condition: 99.2%
  - PULP_FPU_0CYCLAT configuration

    Statement: 99.9% Branch: 99.8% Condition: 99.4%

- Functional Coverage results
  - **Combined from 7 configurations** using PULP_FPU_0CYCLAT as master

    FPU: 100% HWLOOP: 100% Debug: 100%
    Interrupts: 100% OBI: 100% Assertions & Directive: 100%
    riscvISACOV covergroups: 95.1% Covergroup Bins: 98%
  - **Combined from 3 configurations** using PULP_ZFINX_0CYCLAT as master

    ZFINX: 100%

Verification : Remaining RTL coverage holes

- cv32e40p_controller: 2 causes resulting in 16 holes
  - They concern RTL lines specific to HW Loop with corner case conditions
- Uncovered RTL Code analysis file for cv32e40p_controller
- Issues created to describe all waived or remaining holes

RISC-V ISA Formal Verification

- On v1.8.3 RTL tag, Control and Datapath assertions checking runs launched on 2 configurations
  - PULP
  - PULP_FPU (0 cycle latency)
- Successful unbounded check on both configurations
- Siemens Questa Processor (formerly OneSpin) setup and script files pushed on cv32e40p repo

Tools

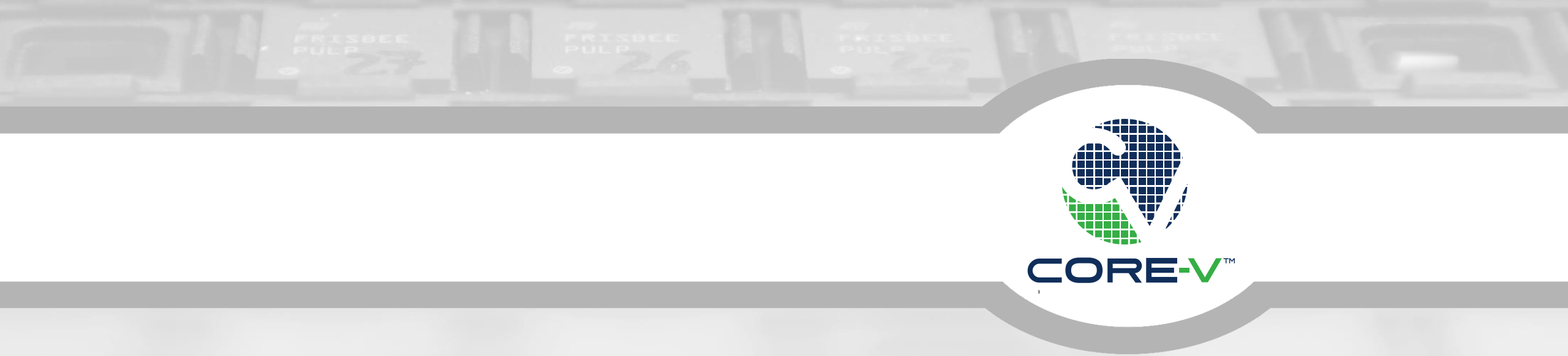
- SW toolchain
  - Final release created on May 30, 2024
  - Pre-built packages available forever on Embecosm web site
- Imperas Reference Model
  - Final release is from May 30, 2024.
  - Tagged in Imperas internal databases

RTL Freeze

- All verification documents and plans are available in core-v-verif/cv32e40p/docs/VerifPlans

- All reports are available in CV32E40Pv2/Milestone-data/RTL_v1.8.3
  - RTL Freeze checklist
  - RTL v1.8.3 verification summary
  - Verification documents html index (repo to clone to open index file)

- **All documents and links will be updated next week to point to final repositories tags and merged before creating all repos tags, releases and User Manual.**



CV32E40PX status

Manuel Pezzin

Sayri Paredes Remache

May 6, 2024

Project objectives

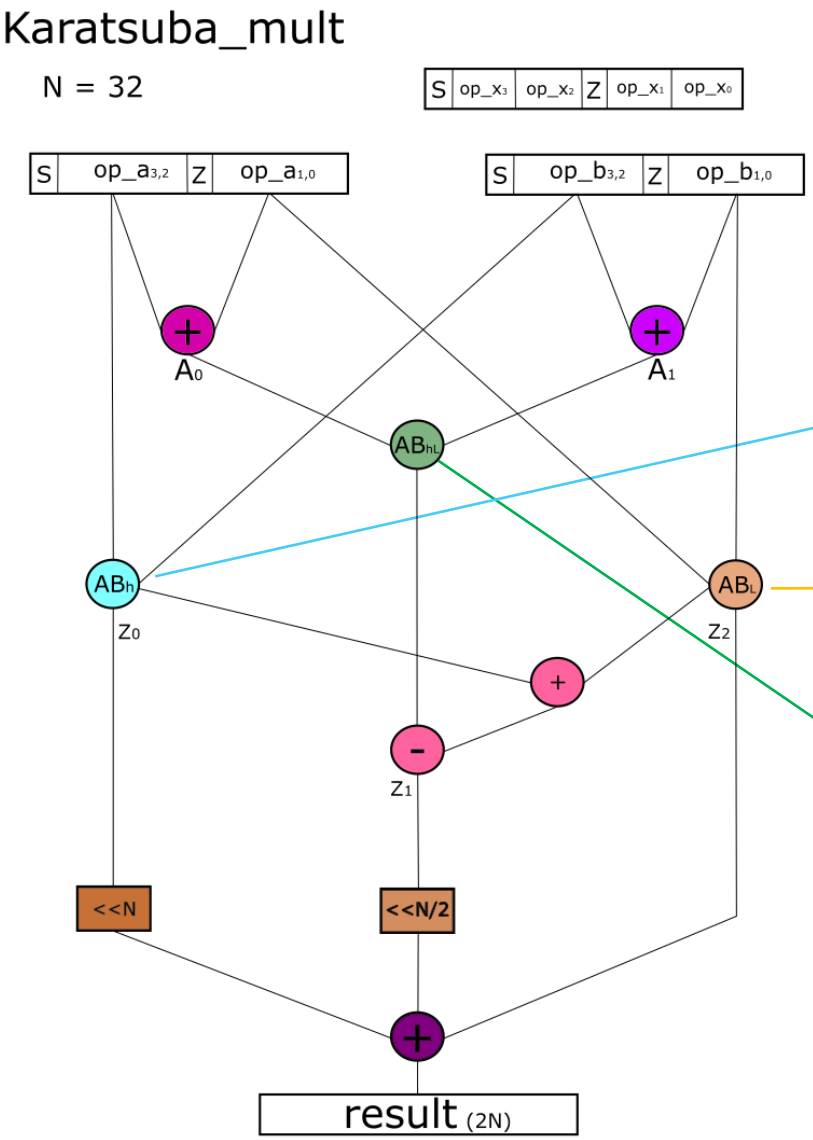
- CPU core tailored for deeply embedded real-time control/DSP
  - Main objective: support official RVB (and a part of RVK) and (upcoming) RVP extensions
  - Second objective: keeping functional backward compatibility with CV32E40Pv1/v2
    - XPULP custom extensions are kept
    - Reuse of existing verification framework
    - Effort to maintain a sequential equivalence on backward-compatible configurations
      - Efforts to improve v2 (mainly XPULP) configuration(s)
      - No effort to improve v1 (mainly IMC) configuration(s)
- “Nice-to-have” features also considered:
  - XPULP custom extensions enhancements
  - CV-X-IF support (based on Davide / EPFL current work)
  - CLIC support
  - Improved OBI interface

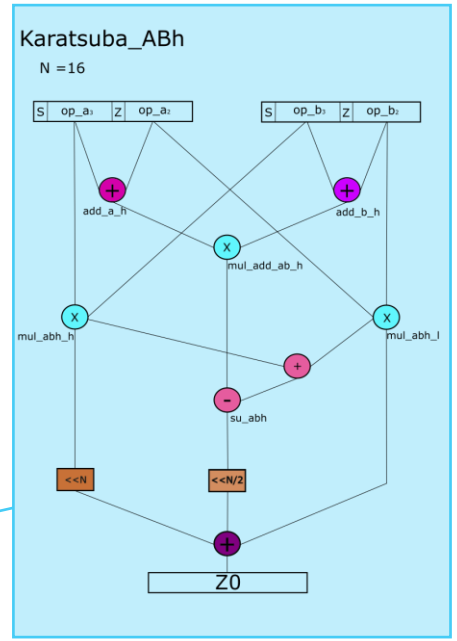
Current Design plan (subject to changes)

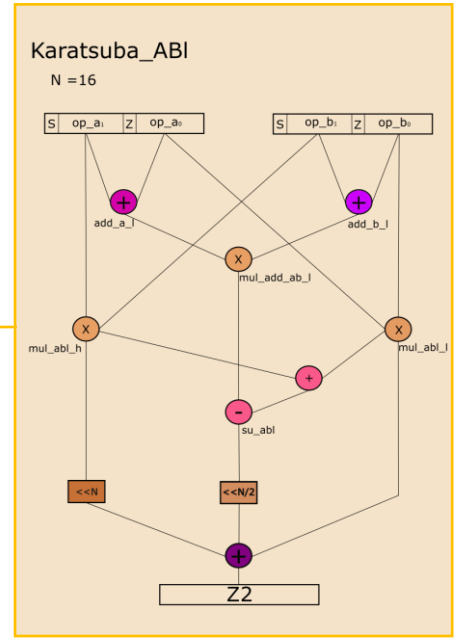
- Start from CV32E40Pv2 stable version
  - Current work aligned on tag 1.4.1, will be rebased on 1.8.3 once RTL freeze / release process is finished
- 1st step: multiplier/dot product restructuring ← we are here and will discuss this today
  - Prepare datapath to make it easier to add RVP base instructions
    - mainly MUL/MAC/DOT products variants
    - Single-cycle instructions
    - Prepare datapath for full (double size) result support
  - Share more processing resources between instructions
  - No functional change
- 2nd step: RVP MUL/MAC/DOT support
  - Add missing features to multiplier for RVP features that have (almost) an equivalent in XPULP
  - Saturation support may be added here (?)
  - Merge of SIMD/fused add/sub with multiplication datapath also considered
- 3rd step: Shift support
  - RVB, RVK and RVP will be addressed together to share resources between scalar and SIMD variants
  - Reuse of existing XPULP “post shift” feature
    - averaging variants of RVP instructions support
    - Q-Format support
- Last step: remaining stuff
  - Non-shift bit manipulation instructions
  - Merge of CV-X-IF support (may happen sooner, depending on EPFL work progress)
  - Nice-to-have features (CLIC, improved OBI)

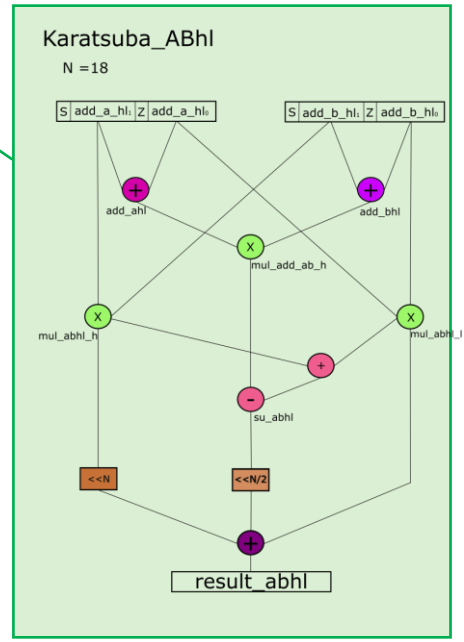
MUL/DOT modified microarchitecture

- 32-bit multiplier restructured using Karatsuba multiplication algorithm
- 2 levels of recursion to reach byte level
- This microarchitecture was slightly modified to add SIMD, DOT product and complex numbers support (see next slides)





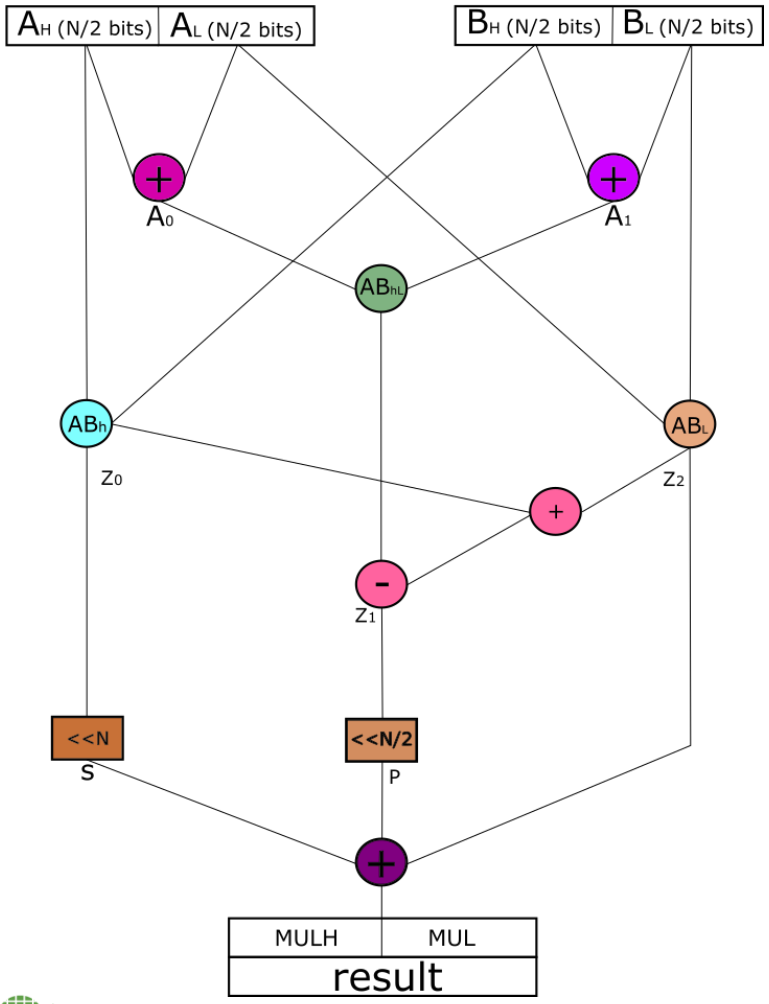




Scalar operations: MUL/MULH and complex product

MUL / MULH

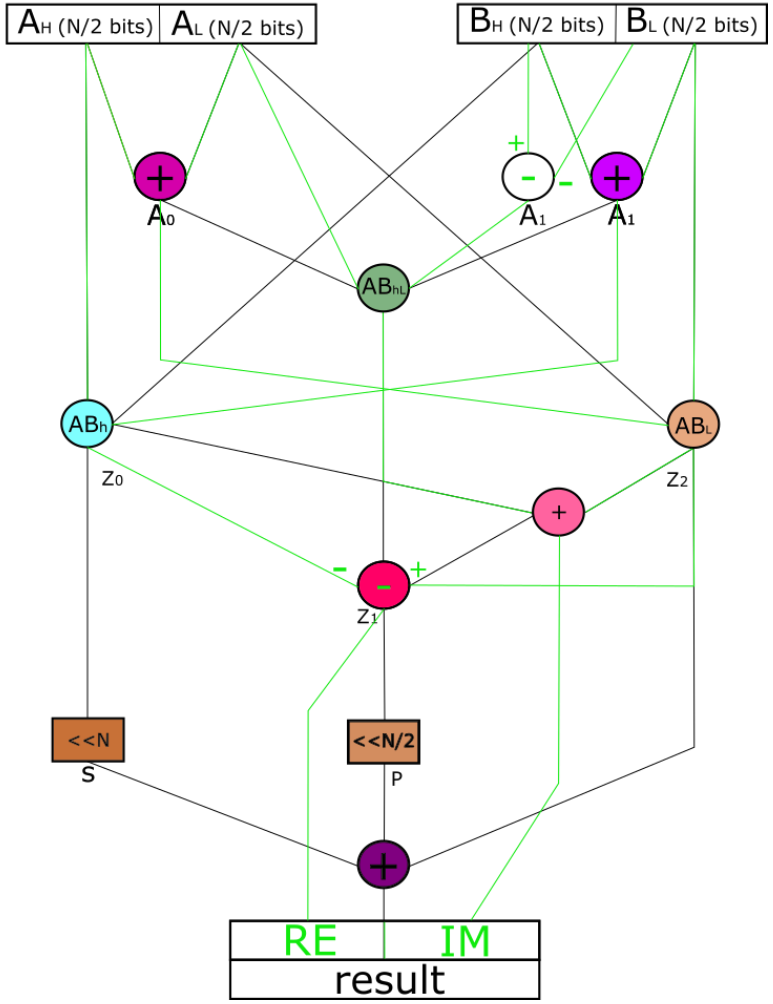
N = 32



- Modified Karatsuba algorithm is widely used in DSP HW for size-efficient complex multiplication
- One subtraction and some muxes added to compute both with the same HW
- Notes:
  - MULH is now obtained in on cycle (MUL and MULH are now computed simultaneously)→ 4x throughput improvement
  - power-efficient 16 bit multiplication may still be obtained on AB_L output thanks to datapath gating
  - Real and Imaginary part of complex product are now computed simultaneously → 2x throughput improvement if a new instruction is added

COMPLEX PRODUCT

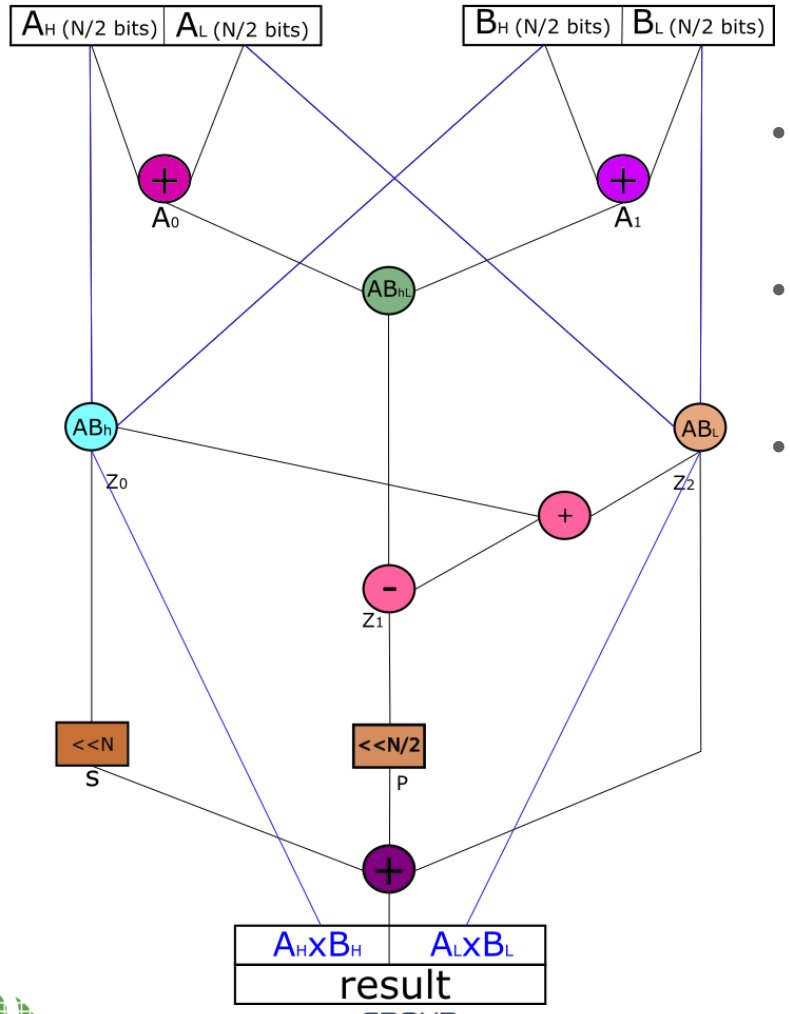
N = 2x16 (IM/RE)



SIMD operations: Parallel MUL and DOT product

PARALLEL PRODUCT

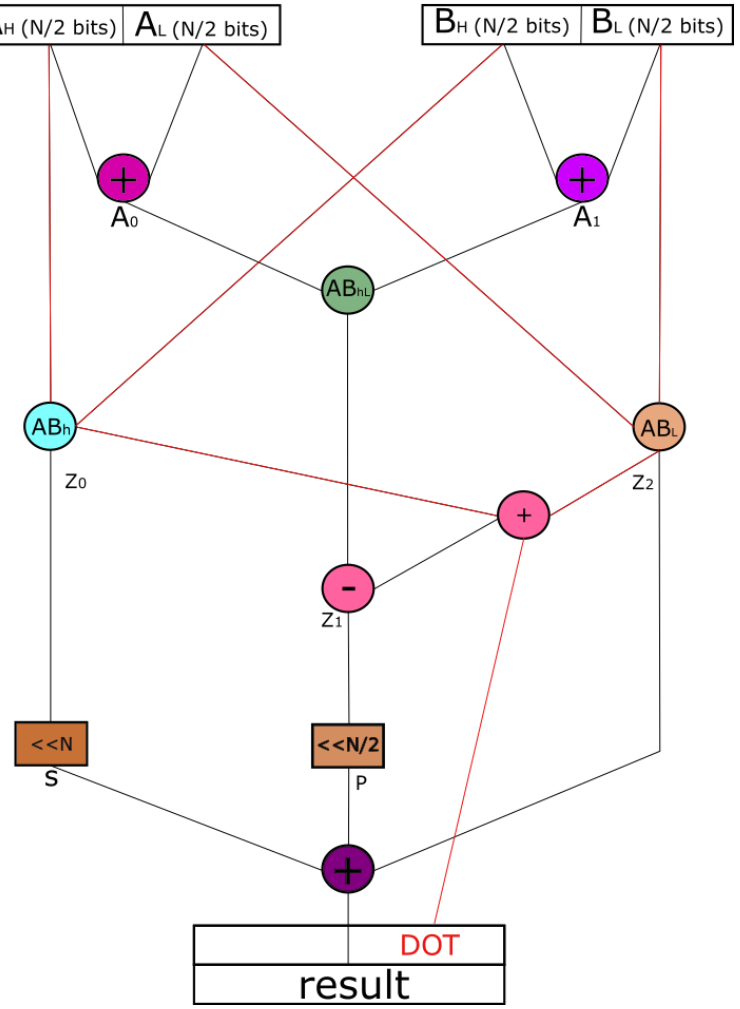
N = 2x16
N = 4x8 by recursion on AB_H and AB_L



- Parallel multiplication and dot product are intermediate results of Karatsuba algorithm
- Only a few muxes required to get the result →SIMD support "almost for free"
- Notes:
  - full multiplication result is obtained, need to isolate low/high parts
  - 9 multipliers are available. 8x4bits vectors operations support may be added with only a few muxes (but muxing routes may be complex) → may be considered by UNIBO for their "light" AI extensions

DOT PRODUCT

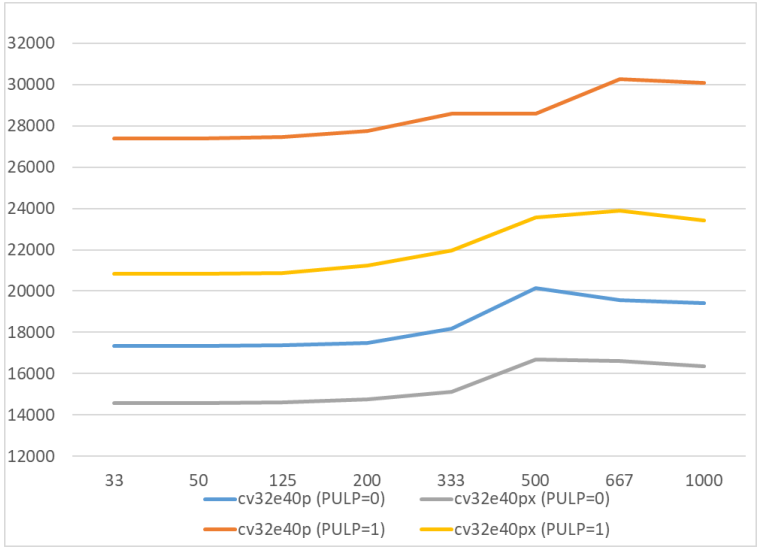
N = 2x16
N = 4x8 by recursion on AB_H and AB_L



Preliminary implementation results

- Synthesis trials on TSMC 40nm ULP process
- Frequency range from 33MHz to 500MHz (666 and 1GHz trials to be checked, given for information)
- ~20%-25% size improvement for PULP=1 config
  - Expected size improvement
  - No major change in std cells Vt distribution →~same QOR
- ~15% size improvement for PULP=0 config
  - unexpected result !
  - possible explanation: original multiplier architecture not appropriate for advanced nodes →FPGA and older nodes synthesis trials needed

		Frequency (MHz)	33	50	125	200	333	500	667	1000
AREA (µm²)	PULP=0	CV32E40P	17343	17348	17366	17493	18163	20148	19564	19434
		CV32E40PX	14567	14591	14612	14766	15127	16679	16615	16376
		Ratio	84%	84%	84%	84%	83%	83%	85%	84%
	PULP=1	CV32E40P	27382	27389	27450	27755	28583	28583	30273	30067
		CV32E40PX	20831	20843	20874	21228	21955	23570	23902	23413
		Ratio	76%	76%	76%	76%	77%	82%	79%	78%



Verification challenges

- Simulation challenges:
  - Micro-architecture optimization based on “arithmetic tricks”
    - → almost impossible to debug intermediate values visually
    - → debug helpers needed (assertions/local models)
  - Non-trivial ranges of values on intermediate results → verification plan to be carefully checked
- Formal checks trials
  - Sequential equivalence
    - Trivial approach without multipliers black-boxing leads to runtime issues
    - Multipliers black-boxing must be done carefully → CAD vendor support needed!
  - Reachability analysis being considered

Thank you!