BL702/704/706

Datasheet

Version：1.6

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Contents

List of Figures

List of Tables

1 Overview

BL702/BL704/BL706 is highly integrated BLE and Zigbee combo chipsets for IoT applications.

Wireless subsystem contains 2.4G radio, BLE+Zigbee baseband and MAC designs. Microcontroller subsystem contains 32-bit RISC CPU, high-speed cache and memories. Power Management Unit controls ultra-low-power modes. Moreover, variety of security features are supported.

Peripheral interfaces include USB2.0, Ethernet(BL704/BL706), IR-remote, SPI, UART, ISO 17987, I2C, I2S, PWM, QDEC, KeyScan, ADC, DAC, PIR, Camera(BL706), and GPIOs.

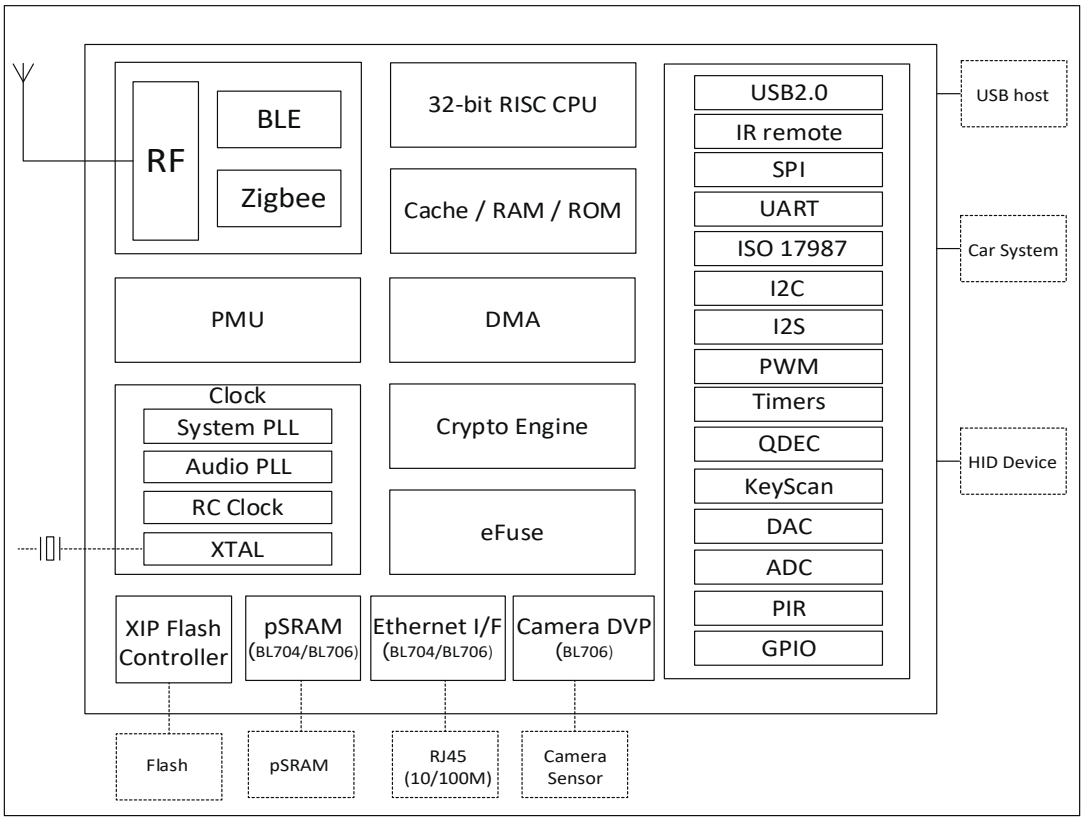

Fig. 1.1: Block Diagram

1.1 Wireless

- 2.4 GHz RF transceiver
- Bluetooth® Specification v5.0
- Bluetooth® Low Energy 1Mbps and 2Mbps
- Bluetooth® Long Range Coded 500Kbps and 125Kbps
- Zigbee 3.0, Base Device Behavior, Core Stack R21, Green Power
- IEEE 802.15.4 MAC/PHY
- Support Wi-Fi/Bluetooth/Zigbee coexistence
- Integrated balun, PA/LNA

1.2 BLE Stack Service

- Battery service
- Current Time service
- Heart Rate service
- HID service

1.3 ZigBee cluster

- Ballast Configuration cluster
- Basic cluster
- Commissioning cluster
- Device Temperature cluster
- Groups cluster
- Identify cluster
- Level Control cluster
- Metering cluster
- OnOff cluster
- OnOff Switch Configuration cluster
- RSSI Location cluster
- Scenes cluster
- Temperature Measurement cluster
- Thermostat cluster
- Window Covering cluster

1.4 MCU Subsystem

- 32-bit RISC CPU with FPU
- Level-1 cache
- One RTC timer update to one year
- Two 32-bit general purpose timers
- Eight DMA channels
- CPU frequency configurable from 1MHz to 144MHz
- JTAG development support
- XIP QSPI Flash/pSRAM with hardware encryption support

1.5 Memory

- 132KB RAM
- 192KB ROM
- 1Kb eFuse
- Embedded Flash (optional)
- Embedded pSRAM (BL704/BL706,optional)

1.6 Security

- Secure boot
- Secure debug ports
- QSPI Flash On-The-Fly AES Decryption (OTFAD) - AES-128, CTR+ mode
- Support AES 128/192/256 bits
- Support MD5, SHA-1/224/256/384/512
- Support TRNG (True Random Number Generator)
- Support PKA (Public Key Accelerator)

1.7 Peripheral

- USB2.0 FS (Full-Speed) device interface
- IR remote control interface
- One SPI master/slave
- Two UARTs

  Support ISO 17987(Local Interconnect Network)
- One I2C master
- One I2S master/slave
- Five PWM channels
- Quadrature decoder
- Key-Scan-Matrix interface
- 12-bit general ADC
- 10-bit general DAC
- PIR (Passive Infra-Red) detection
- Ethernet RMII interface(BL704/BL706)
- Camera interface(BL706)
- 15(BL702)/23(BL704)/31(BL706) Flexible GPIOs (flexible)

1.8 Power Management

- Off
- Hibernate
- Power Down Sleep (flexible)
- Active CPU
- Active Rx
- Active Tx

1.9 Clock

- External main clock XTAL 32MHz
- External low power consumption and the RTC clock XTAL 32/32.768kHz
- Internal RC 32kHz oscillator
- Internal RC 32MHz oscillator
- Internal System PLL
- Internal Audio PLL

2 Functional Description

BL702/BL704/BL706 main functions described as follows：

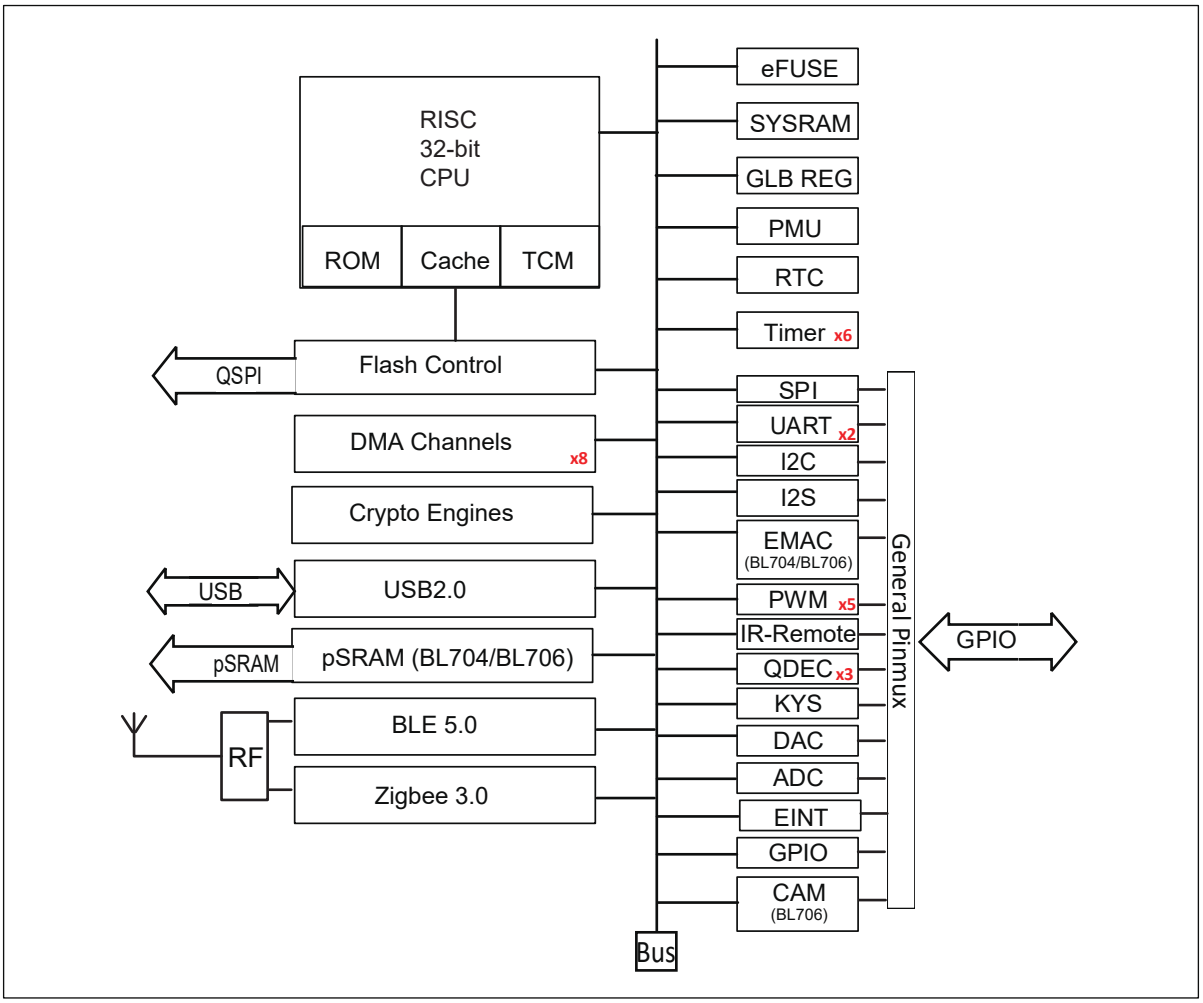

Fig. 2.1: System Architecture

2.1 CPU

BL702/BL704/BL706 32-bit RISC CPU contains FPU (floating-point unit) for 32-bit single-precision arithmetic, three-stage pipelined (IF, EXE, WB), compressed 16 and 32-bit instruction set, standard JTAG debugger port including 4 hardware-programmable breakpoints, interrupt controller including 64 interrupts and 16 interrupt levels/priorities for low latency interrupt processing. Up to 144MHz clock frequency, can be dynamically configured to change clock frequency, enter the power saving mode to achieve low power consumption.

Both ZigBee/BLE stack and application run on single 32-bit RISC CPU for simple and ultra-low power applications. CPU performance ~1.46 DMIPS/MHz. ~3.1 CoreMark/MHz.

2.2 Cache

BL702/BL704/BL706 cache improves CPU performance to access external memory. Cache memories can be partially or fully configured as TCM (tightly coupled memory).

2.3 Memory

BL702/BL704/BL706 memories include: on-chip zero-delay SRAM memories, read-only memories, write-once memories, embedded flash memory (optional), embedded pSRAM (BL704/BL706,optional).

2.4 DMA

BL702/BL704/BL706 DMA (direct memory access) controller has eight dedicated channels that manage data transfer between peripherals and memories to improve cpu/bus efficiency. There are three main types of transfers including memory to memory, memory to peripheral, and peripheral to memory. DMA also supports LLI (link list item) that multiple transfers are pre-defined by a series of linked lists, then hardware automatically complete all transfers according to each LLI size and address. DMA supports peripheral USB, UART, I2C, I2S, SPI, ADC and DAC.

2.5 Bus

BL702/BL704/BL706 bus fabric connection and memory-map summarized as follows：

Table 2.1: Bus Connectiom

Slave/ Master	CPU	Ethernet	DMA	Crypto Engine	Debug
SRAM	V	V	V	V	V
Peripheral	V	-	V	-	V
BLE/Zigbee	V	-	V	-	V

Table 2.2: Memory Map

Module	Base Address	Size	Description
RETRAM	0x40010000	4KB	Deep sleep memory (Retention RAM)
HBN	0x4000F000	4KB	Deep sleep control (Hibernate)
PDS	0x4000E000	4KB	Sleep control (Power Down Sleep)
USB	0x4000D800	1KB	USB control
EMAC	0x4000D000	2KB	Ethernet MAC control (BL704/BL706)
DMA	0x4000C000	4KB	DMA control
QSPI	0x4000B000	4KB	Flash/pSRAM QSPI control
CAM	0x4000AD00	256B	CAM control (BL706)
I2S	0x4000AA00	256B	I2S control
KYS	0x4000A900	256B	Key-Scan control
QDEC2	0x4000A880	64B	Quadrature decoder control
QDEC1	0x4000A840	64B	Quadrature decoder control
QDEC0	0x4000A800	64B	Quadrature decoder control
IRR	0x4000A600	256B	IR Remote control
TIMER	0x4000A500	256B	Timer control
PWM	0x4000A400	256B	Pulse Width Modulation *5 control
I2C	0x4000A300	256B	I2C control
SPI	0x4000A200	256B	SPI master/slave control
UART1	0x4000A100	256B	UART control (support ISO 17987)
UART0	0x4000A000	256B	UART control (support ISO 17987)
L1C	0x40009000	4KB	Cache control
eFuse	0x40007000	4KB	eFuse memory control
SEC	0x40004000	4KB	Security engine
GPIP	0x40002000	4KB	General purpose DAC/ADC/ACOMP interface control
MIX	0x40001000	4KB	Mixed signal register
GLB	0x40000000	4KB	Global control register
pSRAM	0x24000000	8MB	pSRAM memory
XIP	0x23000000	8MB	XIP Flash memory
OCRAM	0x22020000	64KB	On-chip memory
DTCM	0x22014000	48KB	Data cache memory
ITCM	0x22010000	16KB	Instruction cache memory

Table 2.2: Memory Map

Module	Base Address	Size	Description
ROM	0x21000000	192KB	Read-only memory

2.6 Interrupt

BL702/BL704/BL706 supports internal RTC wake-up and external GPIO interrupts wake-up.

CPU interrupt controller supports stack/nesting, level/pulse, and high/low active.

2.7 Boot

BL702/BL704/BL706 supports multiple boot options: UART, USB, and Flash.

2.8 Power

PMU (power management unit) manages the power of the entire chip and is divided into active, idle, sleep, and hibernate power modes. The software can be configured to enter sleep mode and wake-up via RTC timer or EINT to achieve low-power sleep and accurate wake-up management.

Power down sleep modes are flexible for applications to configure as the lowest power consumption.

2.9 Clock

Clock control unit generates clocks to the core MCU and the peripheral SOC devices. The root clock source can be XTAL, PLL or RC oscillator. Dynamic power-saved by proper configurations such as sel, div, en, etc. PMU runs at 32KHz clock to keep system low-power in sleep mode.

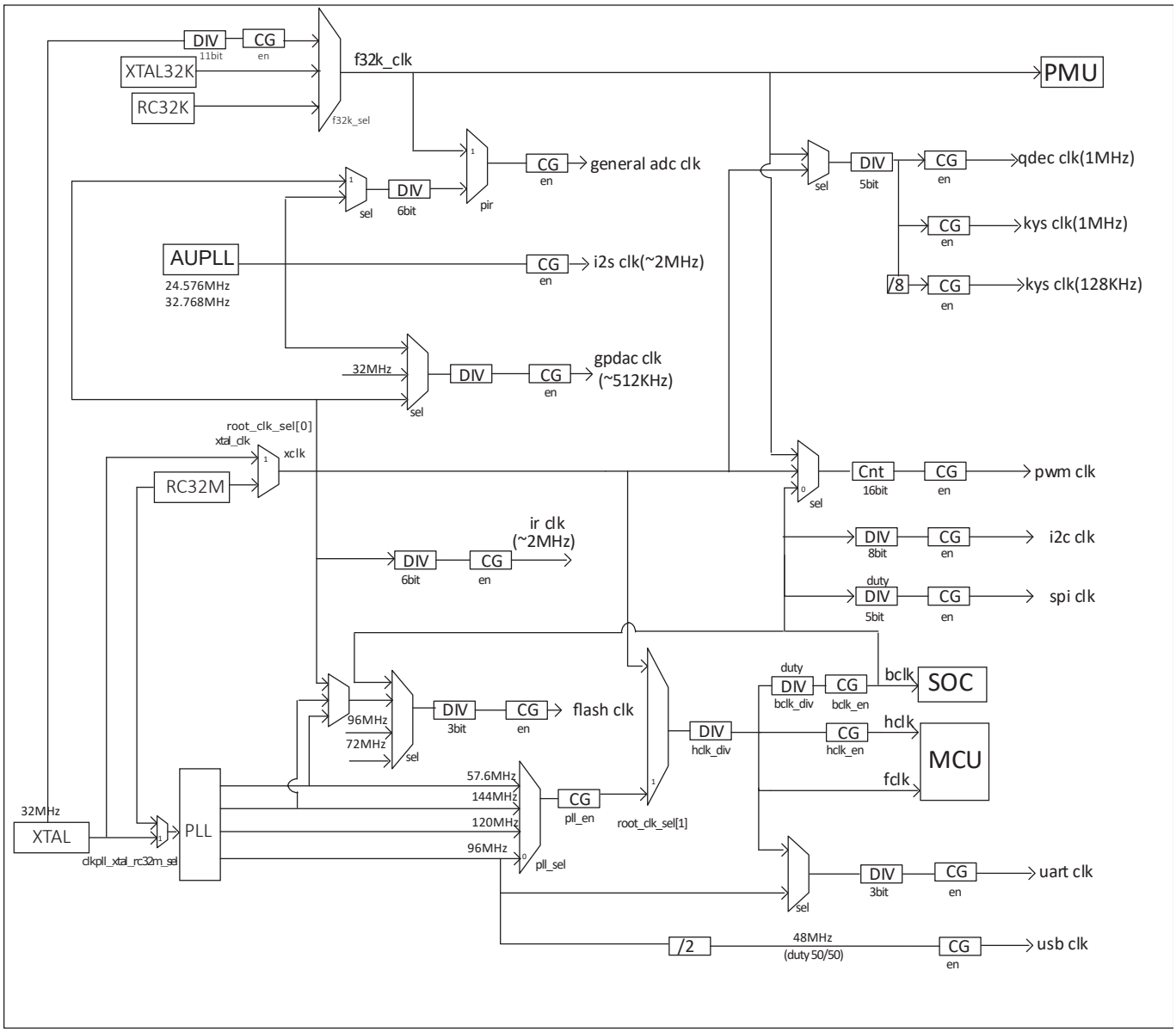

Fig. 2.2: Clock Architecture

2.10 Peripherals

Peripherals include USB2.0, Ethernet, IR-remote, SPI, UART, ISO 17987, I2C, I2S, PWM, QDEC, KeyScan, ADC, DAC, PIR, Camera. Each peripheral can be assigned to different groups of GPIOs through flexible configurations. Each GPIO can be used as a general-purpose input and output function.

3 Pin Definition

BL702 32-pin package includes 11 power pins, 6 analog pins, and 15 flexible GPIO pins.

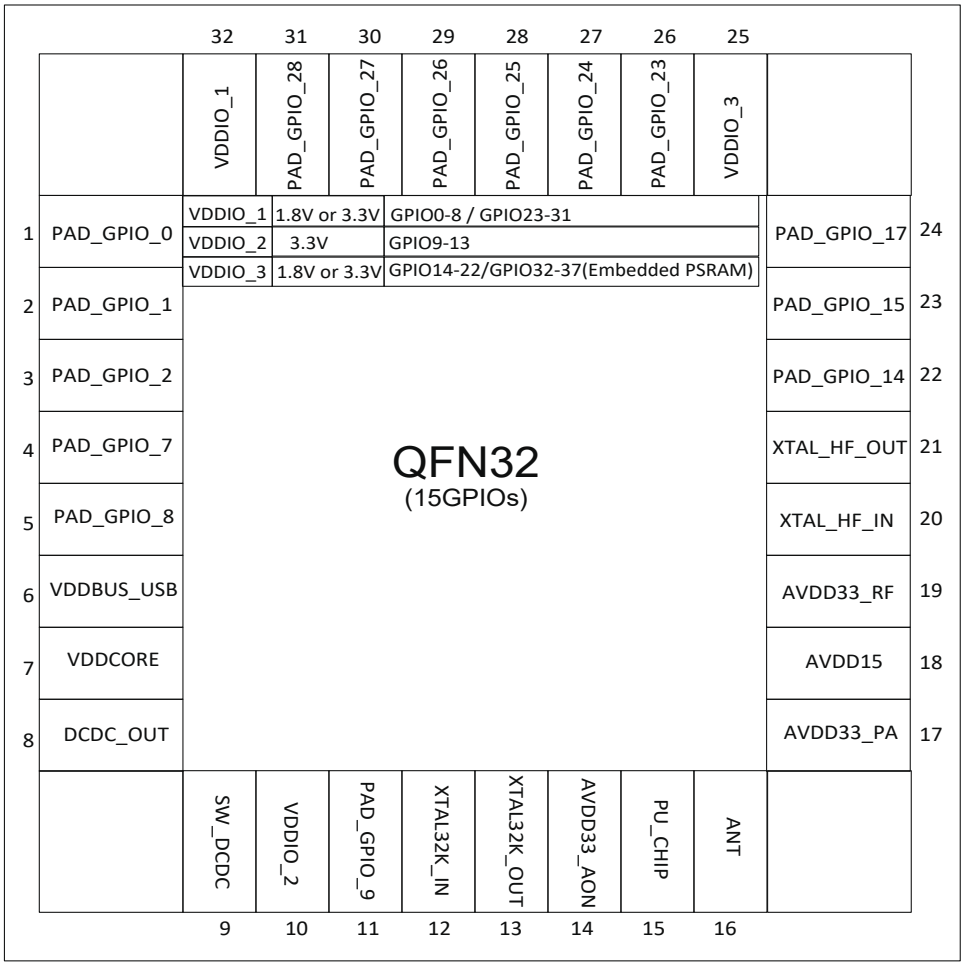

Fig. 3.1: Pin layout (QFN32)

BL704 40-pin package includes 11 power pins, 6 analog pins, and 23 flexible GPIO pins.

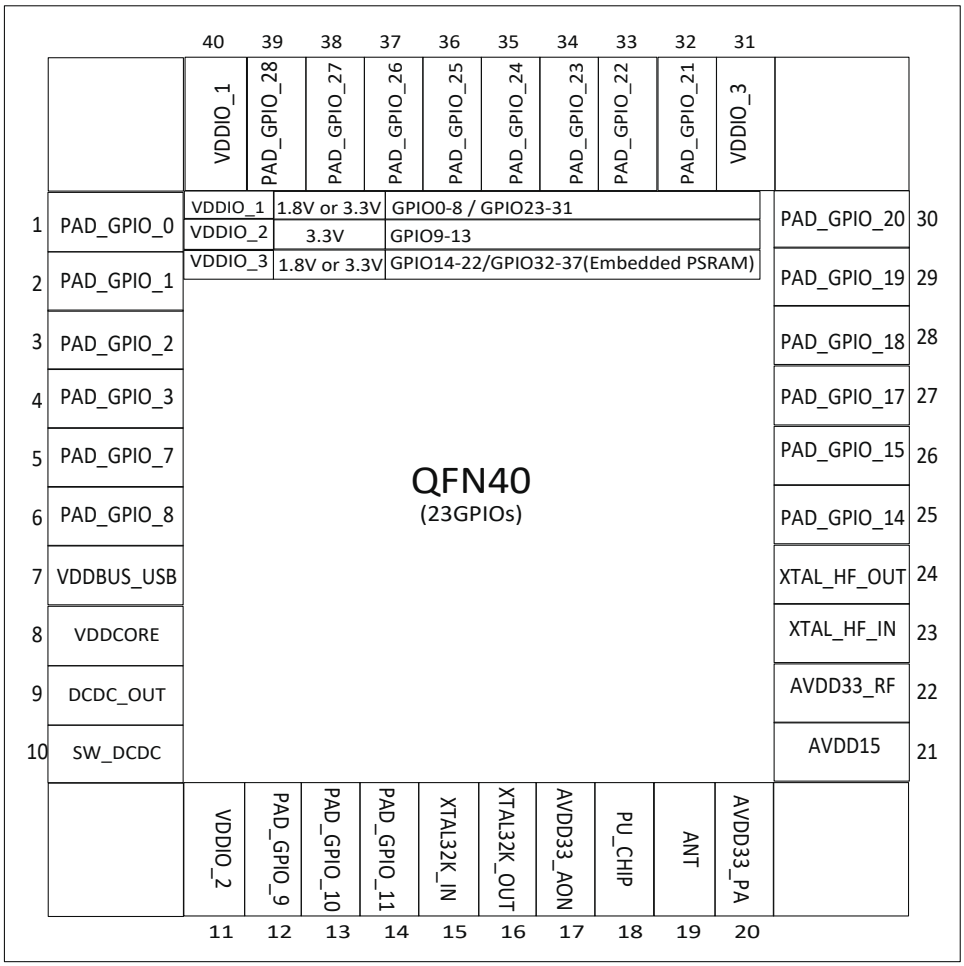

Fig. 3.2: Pin layout (QFN40)

BL706 48-pin package includes 11 power pins, 6 analog pins, and 31 flexible GPIO pins.

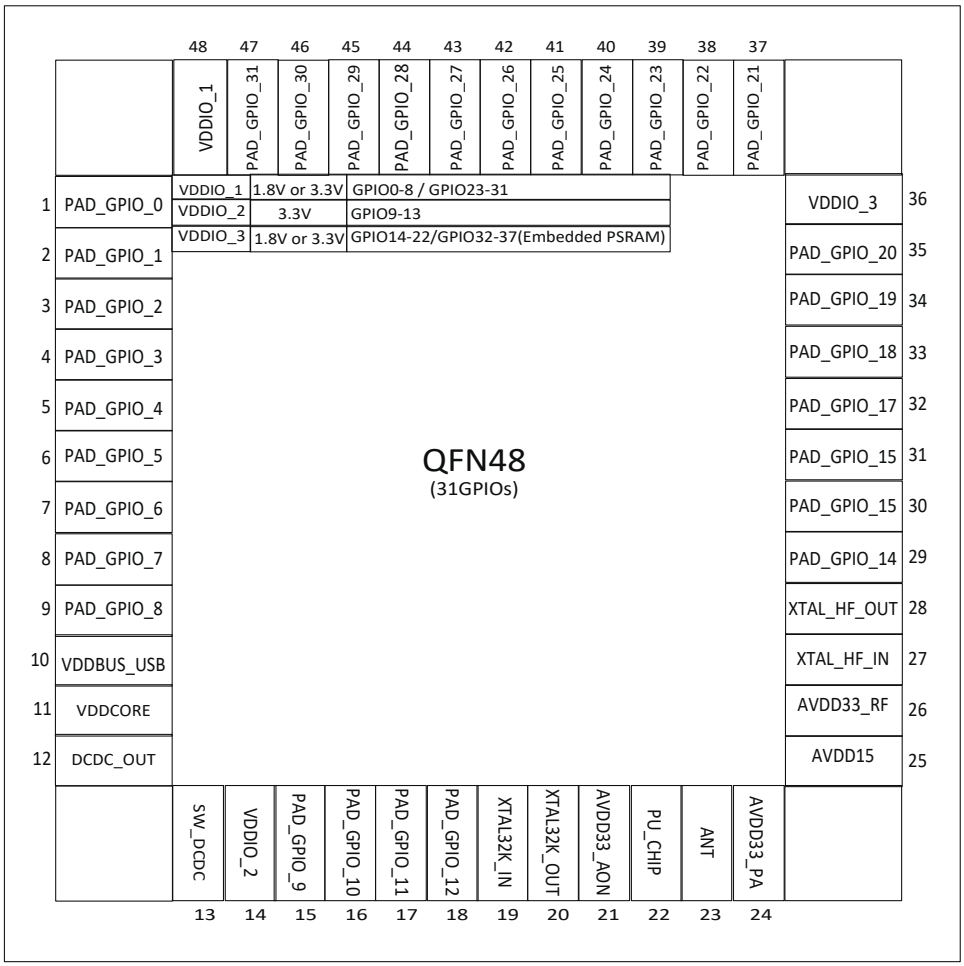

Fig. 3.3: Pin layout (QFN48)

Table 3.1: Pin description

No	Voltage Domain	BL702	BL704	BL706	I/O Type	Pin Name	Description
1	VDDIO_1	1	1	1	DI/DO	PAD_GPIO_0	-
2	VDDIO_1	2	2	2	DI/DO	PAD_GPIO_1	-
3	VDDIO_1	3	3	3	DI/DO	PAD_GPIO_2	-
4	VDDIO_1	-	4	4	DI/DO	PAD_GPIO_3	-
5	VDDIO_1	-	-	5	DI/DO	PAD_GPIO_4	-
6	VDDIO_1	-	-	6	DI/DO	PAD_GPIO_5	-
7	VDDIO_1	-	-	7	DI/DO	PAD_GPIO_6	-
8	VDDIO_1	4	5	8	DI/DO	PAD_GPIO_7	-
9	VDDIO_1	5	6	9	DI/DO	PAD_GPIO_8	-
10	VDDIO_2	11	12	15	DI/DO	PAD_GPIO_9	-
11	VDDIO_2	-	13	16	DI/DO	PAD_GPIO_10	-
12	VDDIO_2	-	14	17	DI/DO	PAD_GPIO_11	-
13	VDDIO_2	-	-	18	DI/DO	PAD_GPIO_12	-

Table 3.1: Pin description

No	Voltage Domain	BL702	BL704	BL706	I/O Type	Pin Name	Description
14	VDDIO_3	22	25	29	DI/DO	PAD_GPIO_14	-
15	VDDIO_3	23	26	30	DI/DO	PAD_GPIO_15	-
16	VDDIO_3	-	-	31	DI/DO	PAD_GPIO_16	-
17	VDDIO_3	24	27	32	DI/DO	PAD_GPIO_17	-
18	VDDIO_3	-	28	33	DI/DO	PAD_GPIO_18	-
19	VDDIO_3	-	29	34	DI/DO	PAD_GPIO_19	-
20	VDDIO_3	-	30	35	DI/DO	PAD_GPIO_20	-
21	VDDIO_3	-	32	37	DI/DO	PAD_GPIO_21	-
22	VDDIO_3	-	33	38	DI/DO	PAD_GPIO_22	-
23	VDDIO_1	26	34	39	DI/DO	PAD_GPIO_23	-
24	VDDIO_1	27	35	40	DI/DO	PAD_GPIO_24	-
25	VDDIO_1	28	36	41	DI/DO	PAD_GPIO_25	-
26	VDDIO_1	29	37	42	DI/DO	PAD_GPIO_26	-
27	VDDIO_1	30	38	43	DI/DO	PAD_GPIO_27	-
28	VDDIO_1	31	39	44	DI/DO	PAD_GPIO_28	-
29	VDDIO_1	-	-	45	DI/DO	PAD_GPIO_29	-
30	VDDIO_1	-	-	46	DI/DO	PAD_GPIO_30	-
31	VDDIO_1	-	-	47	DI/DO	PAD_GPIO_31	-
32	VDDIO_3	-	-	-	DI/DO	PAD_GPIO_32	-
33	VDDIO_3	-	-	-	DI/DO	PAD_GPIO_33	-
34	VDDIO_3	-	-	-	DI/DO	PAD_GPIO_34	-
35	VDDIO_3	-	-	-	DI/DO	PAD_GPIO_35	-
36	VDDIO_3	-	-	-	DI/DO	PAD_GPIO_36	-
37	VDDIO_3	-	-	-	DI/DO	PAD_GPIO_37	-
38	AVDD33_AON	12	15	19	Analog	XTAL32K_IN	Crystal oscillator 32.768kHz input
39	AVDD33_AON	13	16	20	Analog	XTAL32K_OUT	Crystal oscillator 32.768kHz output
40	AVDD33_AON	20	23	27	Analog	XTAL_HF_IN	External crystal input, 32MHz
41	AVDD33_AON	21	24	28	Analog	XTAL_HF_OUT	External crystal output, 32MHz
42	AVDD33_AON	15	18	22	Analog	PU_CHIP	Chip power-up
43	AVDD15	16	19	23	Analog	ANT	RF input and output (single pin)
44	-	32	40	48	Power	VDDIO_1	Externally powered 3.3V or 1.8V
45	-	10	11	14	Power	VDDIO_2	Externally powered 3.3V
46	-	25	31	36	Power	VDDIO_3	Externally powered 3.3V or 1.8V
47	-	14	17	21	Power	AVDD33_AON	Externally powered 3.3V
48	-	17	20	24	Power	AVDD33_PA	Externally powered 3.3V
49	-	19	22	26	Power	AVDD33_RF	Externally powered 3.3V

Table 3.1: Pin description

No	Voltage Domain	BL702	BL704	BL706	I/O Type	Pin Name	Description
50	-	18	21	25	Power	AVDD15	Internal LDO output (for internal use only)
51	-	9	10	13	Power	SW_DCDC	DCDC power 1.8V
52	-	8	9	12	Power	DCDC_OUT	DCDC power 1.8V
53	-	6	7	10	Power	VDDBUS_USB	USB power
54	-	7	8	11	Power	VDDCORE	Internal LDO output (for internal use only)

Table 3.2: GPIO Muxed Pins

Pin Name	Flash[1]	I2S	SPI	CAM	UART[2] (Default /SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default /SWAP=1)	Ether_Mac	QDEC	Key_Scan_In	Key_Scan_Drive	IR
PAD_GPIO_0	-	BCLK	MISO /MOSI	PIX_CLK	SIG0 /SIG4	SCL	PWM_CH0	-	FEM0	TMS/TCK	MII_REF_CLK	QDEC0_a	ROW0	COL0	-
PAD_GPIO_1	-	FS	MOSI /MISO	FRAME_VLD	SIG1 /SIG5	SDA	PWM_CH1	-	FEM1	TDI/TDO	MII_TXD[0]	QDEC0_b	ROW1	COL1	-
PAD_GPIO_2	-	DIO/DO	SS	LINE_VLD	SIG2 /SIG6	SCL	PWM_CH2	-	FEM2	TCK/TMS	MII_TXD[1]	QDEC0_led	ROW2	COL2	-
PAD_GPIO_3	-	RCLK_O /DI	SCLK	PIX_DAT0	SIG3 /SIG7	SDA	PWM_CH3	-	FEM3	TDO/TDI	-	QDEC1_a	ROW3	COL3	-
PAD_GPIO_4	-	BCLK	MISO /MOSI	PIX_DAT1	SIG4 /SIG0	SCL	PWM_CH4	-	FEM4	TMS/TCK	-	QDEC1_b	ROW4	COL4	-
PAD_GPIO_5	-	FS	MOSI /MISO	PIX_DAT2	SIG5 /SIG1	SDA	PWM_CH0	-	FEM0	TDI/TDO	-	QDEC1_led	ROW5	COL5	-
PAD_GPIO_6	-	DIO/DO	SS	PIX_DAT3	SIG6 /SIG2	SCL	PWM_CH1	-	FEM1	TCK/TMS	-	QDEC2_a	ROW6	COL6	-
PAD_GPIO_7	-	RCLK_O /DI	SCLK	-	SIG7 /SIG3	SDA	PWM_CH2	USB_DP /ADC_CH6	FEM2	TDO/TDI	MII_RXD[0]	QDEC2_b	ROW7	COL7	-
PAD_GPIO_8	-	BCLK	MISO /MOSI	-	SIG0 /SIG4	SCL	PWM_CH3	USB_DM /ADC_CH0	FEM3	TMS/TCK	MII_RXD[1]	QDEC2_led	ROW0	COL8	-
PAD_GPIO_9	-	FS	MOSI /MISO	-	SIG1 /SIG5	SDA	PWM_CH4	ADC_CH7	FEM4	TDI/TDO	-	QDEC0_a	ROW1	COL9	-
PAD_GPIO_10	-	DIO/DO	SS	-	SIG2 /SIG6	SCL	PWM_CH0	MICBIAS	FEM0	TCK/TMS	-	QDEC0_b	ROW2	COL10	-
PAD_GPIO_11	-	RCLK_O /DI	SCLK	-	SIG3 /SIG7	SDA	PWM_CH1	ADC_CH3	FEM1	TDO/TDI	-	QDEC0_led	ROW3	COL11	-
PAD_GPIO_12	-	BCLK	MISO /MOSI	PIX_DAT4	SIG4 /SIG0	SCL	PWM_CH2	ADC_CH4	FEM2	TMS/TCK	-	QDEC1_a	ROW4	COL12	-
PAD_GPIO_13	-	FS	MOSI /MISO	-	SIG5 /SIG1	SDA	PWM_CH3	-	FEM3	TDI/TDO	-	QDEC1_b	ROW5	COL13	-
PAD_GPIO_14	-	DIO/DO	SS	-	SIG6 /SIG2	SCL	PWM_CH4	ADC_CH5	FEM4	TCK/TMS	-	QDEC1_led	ROW6	COL14	-
PAD_GPIO_15	-	RCLK_O /DI	SCLK	-	SIG7 /SIG3	SDA	PWM_CH0	ADC_CH1	FEM0	TDO/TDI	-	QDEC2_a	ROW7	COL15	-
PAD_GPIO_16	-	BCLK	MISO /MOSI	-	SIG0 /SIG4	SCL	PWM_CH1	-	FEM1	TMS/TCK	-	QDEC2_b	ROW0	COL16	-
PAD_GPIO_17	SF1_IO0 /SF2_CS2	FS	MOSI /MISO	PIX_DAT4	SIG1 /SIG5	SDA	PWM_CH2	ADC_CH2 /psw_irrcv	FEM2	TDI/TDO	-	QDEC2_led	ROW1	COL17	IRRX (ir_rx_gpio_sel=1)
PAD_GPIO_18	SF1_IO1	DIO/DO	SS	PIX_DAT5	SIG2 /SIG6	SCL	PWM_CH3	ADC_CH8	FEM3	TCK/TMS	RMII_MDC	QDEC0_a	ROW2	COL18	IRRX (ir_rx_gpio_sel=2)
PAD_GPIO_19	SF1_CS	RCLK_O /DI	SCLK	PIX_DAT6	SIG3 /SIG7	SDA	PWM_CH4	ADC_CH9	FEM4	TDO/TDI	RMII_MDIO	QDEC0_b	ROW3	COL19	IRRX (ir_rx_gpio_sel=3)
PAD_GPIO_20	SF1_IO3	BCLK	MISO /MOSI	PIX_DAT7	SIG4 /SIG0	SCL	PWM_CH0	ADC_CH10	FEM0	TMS/TCK	RMII_RXERR	QDEC0_led	ROW4	COL0	IRRX (ir_rx_gpio_sel=4)
PAD_GPIO_21	SF1_CLK	FS	MOSI /MISO	-	SIG5 /SIG1	SDA	PWM_CH1	ADC_CH11	FEM1	TDI/TDO	RMII_TX_EN	QDEC1_a	ROW5	COL1	IRRX (ir_rx_gpio_sel=5)
PAD_GPIO_22	SF1_IO2	DIO/DO	SS	-	SIG6 /SIG2	SCL	PWM_CH2	IRTX	FEM2	TCK/TMS	RMII_RX_DV	QDEC1_b	ROW6	COL2	IRRX (ir_rx_gpio_sel=6)

Table 3.2: GPIO Muxed Pins

Pin Name	Flash[1]	I2S	SPI	CAM	UART[2] (Default /SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default /SWAP=1)	Ether_Mac	QDEC	Key_Scan_In	Key_Scan_Drive	IR
PAD_GPIO_23	SF2_IO2	RCLK_O /DI	SCLK	PIX_DAT4	SIG7 /SIG3	SDA	PWM_CH3	IRTX	FEM3	TDO/TDI	-	QDEC1_led	ROW7	COL3	IRRX (ir_rx_gpio_sel=7)
PAD_GPIO_24	SF2_IO1	BCLK	MISO /MOSI	PIX_DAT5	SIG0 /SIG4	SCL	PWM_CH4	-	FEM4	TMS/TCK	RMII_MDC	QDEC2_a	ROW0	COL4	IRRX (ir_rx_gpio_sel=8)
PAD_GPIO_25	SF2_CS	FS	MOSI /MISO	PIX_DAT6	SIG1 /SIG5	SDA	PWM_CH0	-	FEM0	TDI/TDO	RMII_MDIO	QDEC2_b	ROW1	COL5	IRRX (ir_rx_gpio_sel=9)
PAD_GPIO_26	SF2_IO3	DIO/DO	SS	PIX_DAT7	SIG2 /SIG6	SCL	PWM_CH1	-	FEM1	TCK/TMS	RMII_RXERR	QDEC2_led	ROW2	COL6	IRRX (ir_rx_gpio_sel=10)
PAD_GPIO_27	SF2_CLK	RCLK_O /DI	SCLK	-	SIG3 /SIG7	SDA	PWM_CH2	-	FEM2	TDO/TDI	RMII_TX_EN	QDEC0_a	ROW3	COL7	IRRX (ir_rx_gpio_sel=11)
PAD_GPIO_28	SF2_IO0	BCLK	MISO /MOSI	PIX_DAT4	SIG4 /SIG0	SCL	PWM_CH3	-	FEM3	TMS/TCK	RMII_RX_DV	QDEC0_b	ROW4	COL8	IRRX (ir_rx_gpio_sel=12)
PAD_GPIO_29	-	FS	MOSI /MISO	PIX_DAT5	SIG5 /SIG1	SDA	PWM_CH4	-	FEM4	TDI/TDO	-	QDEC0_led	ROW5	COL9	IRRX (ir_rx_gpio_sel=13)
PAD_GPIO_30	-	DIO/DO	SS	PIX_DAT6	SIG6 /SIG2	SCL	PWM_CH0	-	FEM0	TCK/TMS	-	QDEC1_a	ROW6	COL10	IRRX (ir_rx_gpio_sel=14)
PAD_GPIO_31	-	RCLK_O /DI	SCLK	PIX_DAT7	SIG7 /SIG3	SDA	PWM_CH1	-	FEM1	TDO/TDI	-	QDEC1_b	ROW7	COL11	IRRX (ir_rx_gpio_sel=15)
PAD_GPIO_32	SF3_IO0	Same as PAD_GPIO_23													
PAD_GPIO_33	SF3_IO2	Same as PAD_GPIO_24													
PAD_GPIO_34	SF3_IO1	Same as PAD_GPIO_25													
PAD_GPIO_35	SF3_CS	Same as PAD_GPIO_26													
PAD_GPIO_36	SF3_CLK	Same as PAD_GPIO_27													
PAD_GPIO_37	SF3_IO3	Same as PAD_GPIO_28													

[1] There are 3 groups of Flash, and the smallest selection unit is group, which is configured according to group when used.

In Dual CS mode, PAD_GPIO_17 can be configured as SF2_CS2 function. If the Flash is enclosed, the numbers of PAD_GPIO_23 28 are changed to PAD_GPIO_32 37, and the GPIO function remains the same as PAD_GPIO_23 28.

[2] The default UART signal mapping table is shown below.

BL702/704/706 Datasheet

Table 3.3: UART Signal Mapping(Default)

UART Signal	uart_sig_x_sel	Mapping Signal
UART_SIG0	uart_sig_0_sel=0	UART0_RTS
UART_SIG1	uart_sig_1_sel=1	UART0_CTS
UART_SIG2	uart_sig_2_sel=2	UART0_TXD
UART_SIG3	uart_sig_3_sel=3	UART0_RXD
UART_SIG4	uart_sig_4_sel=4	UART1_RTS
UART_SIG5	uart_sig_5_sel=5	UART1_CTS
UART_SIG6	uart_sig_6_sel=6	UART1_TXD
UART_SIG7	uart_sig_7_sel=7	UART1_RXD

Note: UART_SIG0-UART_SIG7 can be configured as any of 8 Mapping Signals. For example: UART_SIG0 can also be configured as UART_RXD. The specific signal mapping example is shown in the table below.

Table 3.4: UART Signal Mapping(Example)

UART Signal	uart_sig_x_sel	Mapping Signal
UART_SIG0	uart_sig_0_sel=7	UART1_RXD
UART_SIG1	uart_sig_1_sel=6	UART1_TXD
UART_SIG2	uart_sig_2_sel=5	UART1_CTS
UART_SIG3	uart_sig_3_sel=4	UART1_RTS
UART_SIG4	uart_sig_4_sel=3	UART0_RXD
UART_SIG5	uart_sig_5_sel=2	UART0_TXD
UART_SIG6	uart_sig_6_sel=1	UART0_CTS
UART_SIG7	uart_sig_7_sel=0	UART0_RTS

4 RF Characteristsic

RF Characteristics of Receiving and Transmitting modes.

Table 4.1: RX RF Characteristics

Mode		Note	Performance @25°C			
			Min.	Typ	Max.	Unit
Zigbee Sensitivity	250 Kbps			-104		dBm
BLE Sensitivity	125 Kbps			-104	-98	
	500 Kbps			-100	-97	
	1 Mbps			-97	-94	
	2 Mbps			-94	-92	

Table 4.2: TX RF Characteristics

Mode		Note	Performance @25°C			
			Min.	Typ	Max.	Unit
TX Power				0-14		dBm
TX EVM				11	13	%

5 Power Consumption

Power Consumption of each power mode.

Table 5.1: Power Modes & Whole-chip Current

Mode		Note	Performance @25°C			
			Min.	Typ	Max.	Unit
RX		RF only		3.5		mA
TX	0dBm	RF only		4.8		
	10dBm	RF only		17		
	14dBm	RF only		45		
Power Down Sleep		64kB RAM retention		10		μA
Hibernate		4kB RAM retention		1.7		
		RTC wakeup		1.5		
		GPIO wakeup		1.0		
Shut-down				0.1		

6 Electrical Specifications

6.1 Absolute Maximum Rating

Table 6.1: Absolute Maximum Rating

Pin Name	Min.	Max.	Unit
VDDIO_1	-0.3	3.63	V
VDDIO_2	-0.3	3.63	V
VDDIO_3	-0.3	3.63	V
VSSBUS_USB	-0.3	5.5	V
AVDD33_AON	-0.3	3.63	V
AVDD33_PA	-0.3	3.63	V
AVDD33_RF	-0.3	3.63	V
ESD Protection (HBM)		2000	V
Storage Temperature	-40	125	°C

6.2 Operating Condition

Table 6.2: Recommended Power Operating Range

Pin Name	Min.	Typ	Max.	Unit
VDDIO_1	1.62/1.8	1.8/3.3	1.92/3.63	V
VDDIO_2	1.8	3.3	3.63	V
VDDIO_3	1.8	3.3	3.63	V
VDDBUS_USB	4.5	5	5.5	V
AVDD33_AON	1.8	3.3	3.63	V
AVDD33_PA	1.4/2.97	1.5/3.3	1.6/3.63	V
AVDD33_RF	1.4/2.97	1.5/3.3	1.6/3.63	V

Table 6.3: Recommended Temperature Operating Range

Item		Min.	Max.	Unit
Temperature	Main Die	-40	105	°C
	Multi-Die SiP	-20	85	°C

Table 6.4: General Operating Conditions

Item	Description	Min.	Typ	Max.	Unit
FCPU	CPU/TCM/Cache clock frequency	0	32	144	MHz
FSYS	System clock frequency	0	32	72	MHz

7 Reference Design

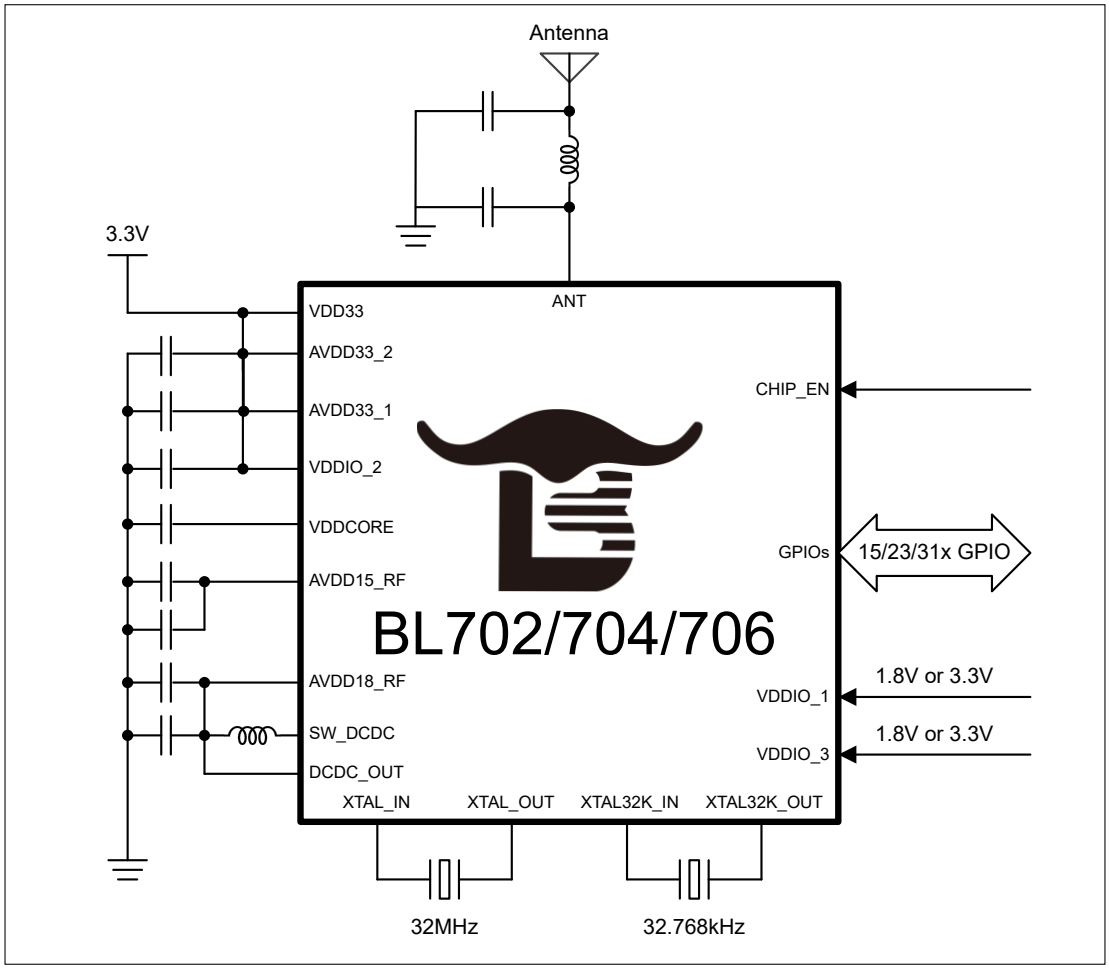

Fig. 7.1: Reference Design

8 Package Information(QFN32)

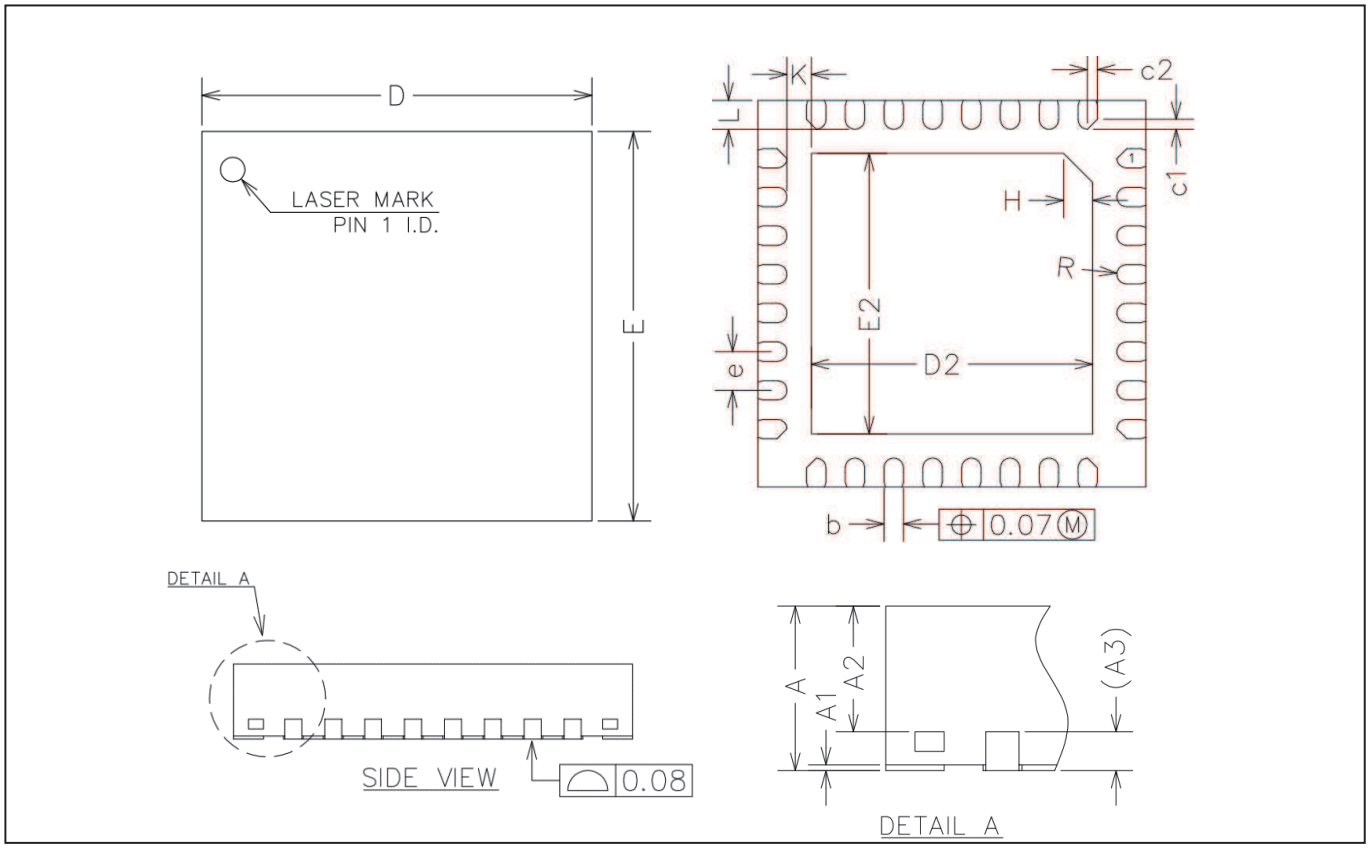

Fig. 8.1: QFN32 Package drawing

Table 8.1: QFN32 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05

Table 8.1: QFN32 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30REF		
K	0.25REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

9 Package Information(QFN40)

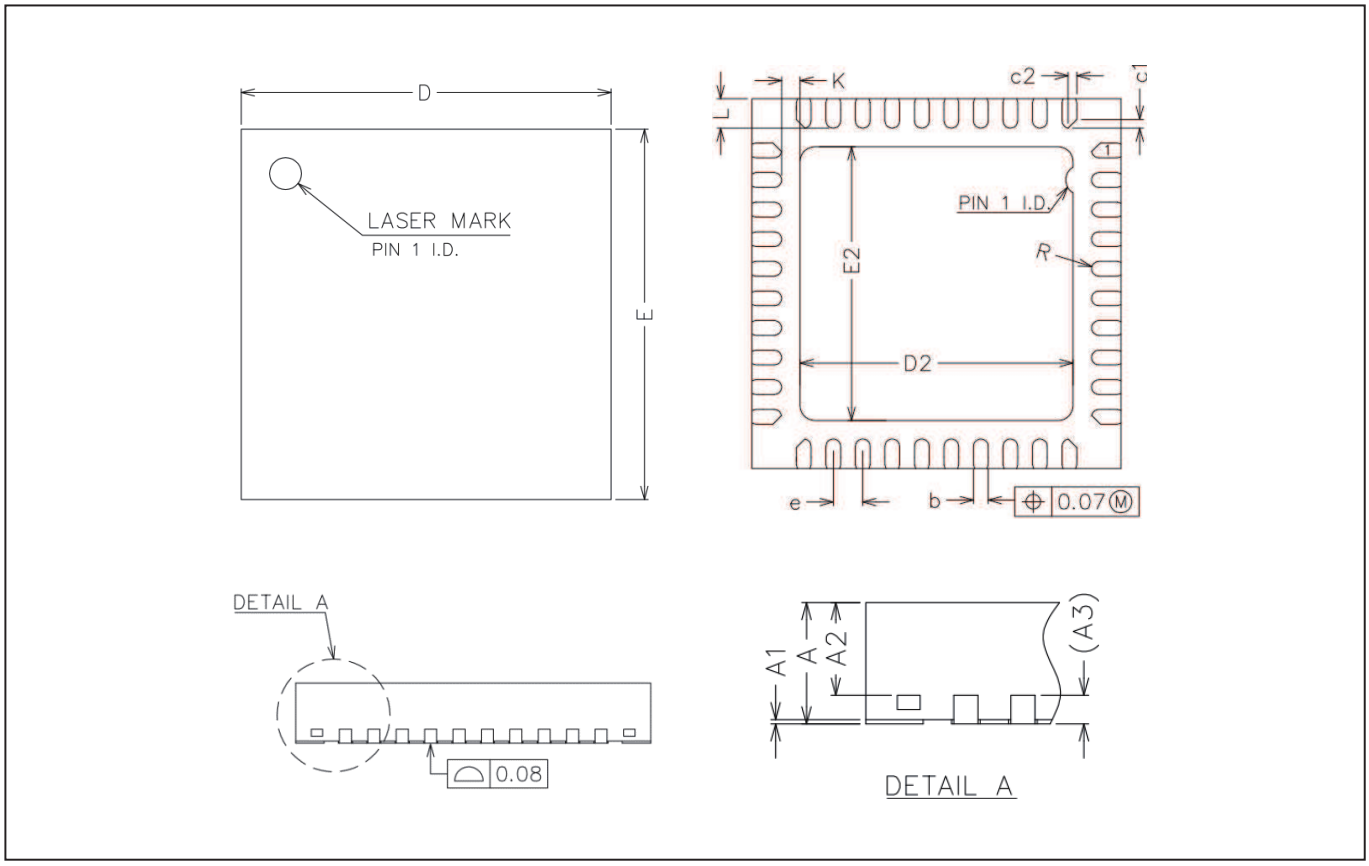

Fig. 9.1: QFN40 Package drawing

Table 9.1: QFN40 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05

Table 9.1: QFN40 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A2	0.60	0.65	0.70
A3	0.20REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
C1	-	0.12	-
C2	-	0.12	-

10 Package Information(QFN48)

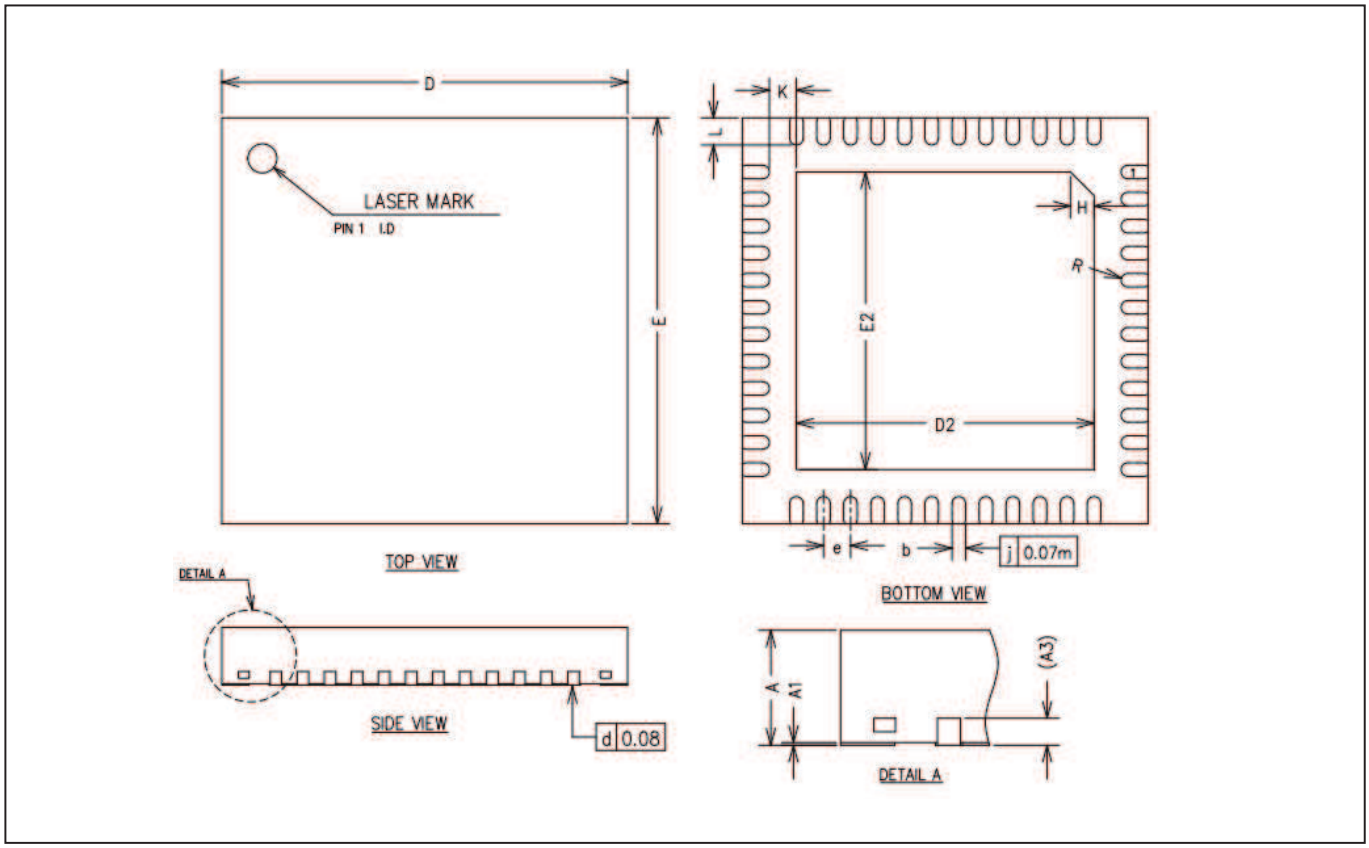

Fig. 10.1: QFN48 Package drawing

Table 10.1: QFN48 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05

Table 10.1: QFN48 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A3	0.20REF		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.30	4.40	4.50
E2	4.30	4.40	4.50
e	0.30	0.40	0.50
H	0.35REF		
K	0.30	0.40	0.50
L	0.30	0.40	0.50
R	0.075	-	-

11 Top Marking Definition

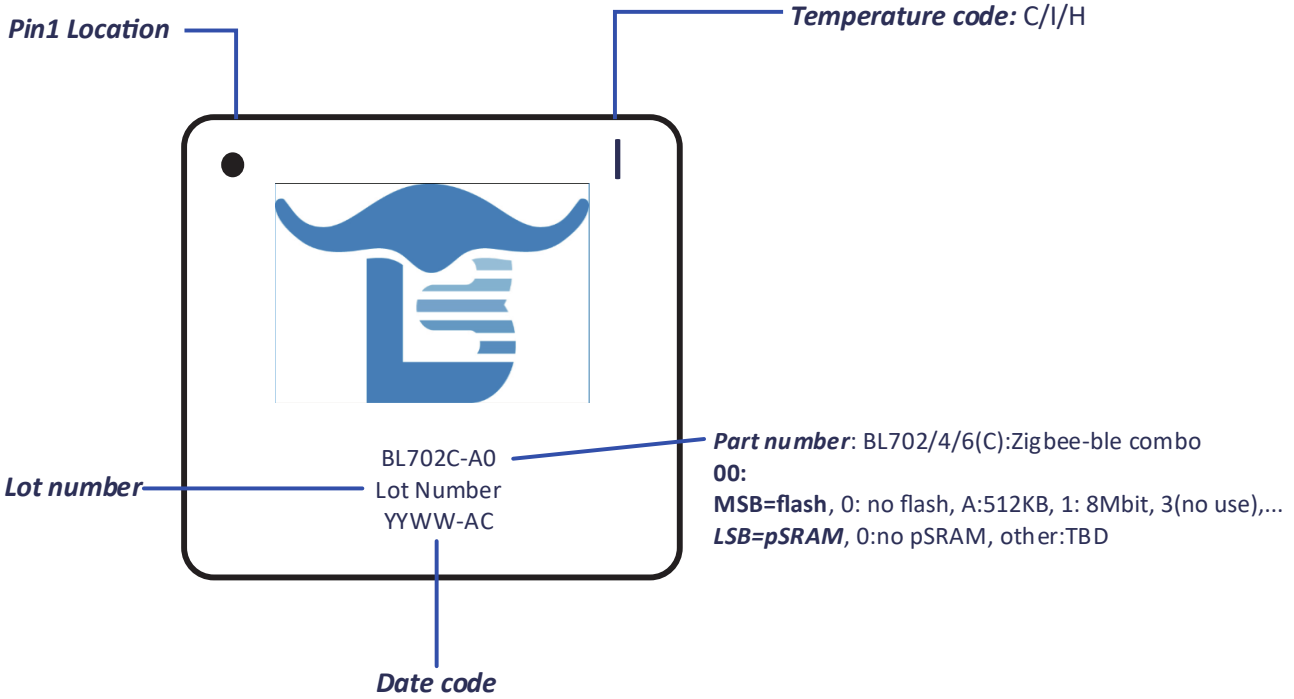

Fig. 11.1: Top Marking Definition

12 Ordering Information

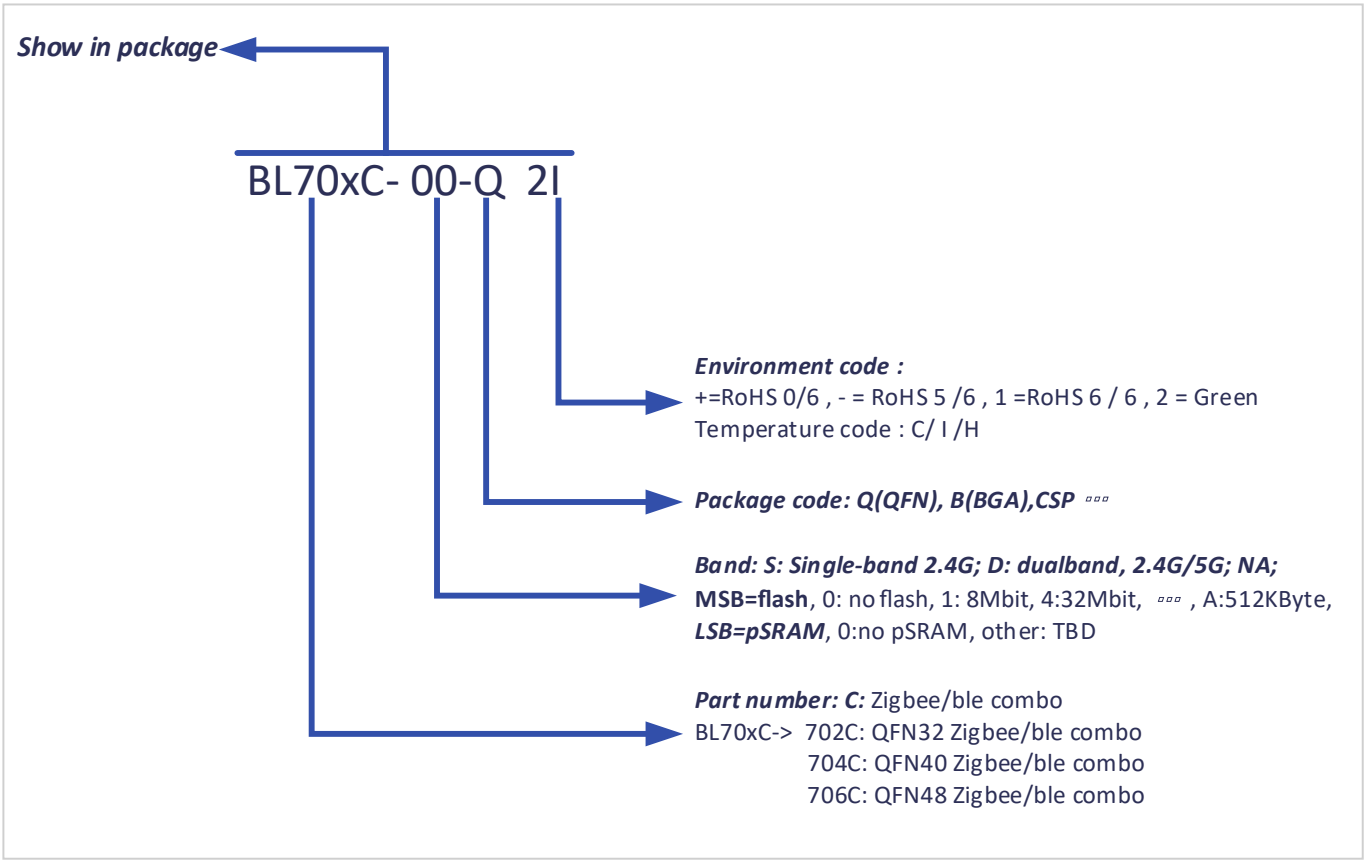

Fig. 12.1: Part Number

Table 12.1: Part Order Options

Product No.	Description
BL702C-A0-Q2I	Zigbee/BLE combo, QFN32,flash 512kB
BL704C-00-Q2I	Zigbee/BLE combo, QFN40

Table 12.1: Part Order Options

Product No.	Description
BL704C-10-Q2I	Zigbee/BLE combo, QFN40, Flash 1MB
BL706C-00-Q2I	Zigbee/BLE combo, QFN48

13 Revision history

Table 13.1: Document revision history

Date	Revision	Changes
2020/9/15	1.0	Initial release
2020/9/22	1.1	Add package information(QFN48)
2020/10/20	1.2	Modify the number of TIMER
2020/11/13	1.3	Update PDS/HBN power consumption data
2020/12/4	1.4	Differentiate different package information
2020/1/11	1.5	Add GPIO Muxed Pins
2020/1/22	1.6	Add Reference design