

# 1. Description

# 1.1. Project

Project Name	stm32genscope
Board Name	NUCLEO-G431KB
Generated with:	STM32CubeMX 6.10.0
Date	12/31/2023

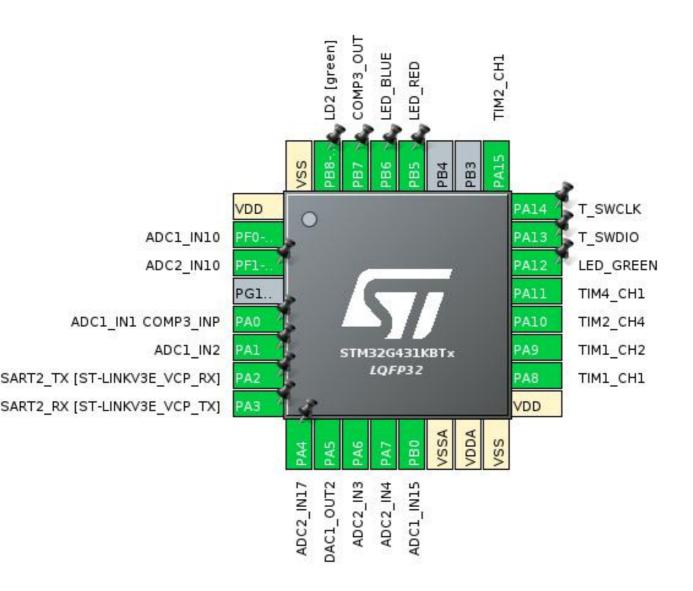
## 1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x1
MCU name	STM32G431KBTx
MCU Package	LQFP32
MCU Pin number	32

# 1.3. Core(s) information

Core(s)	ARM Cortex-M4

# 2. Pinout Configuration

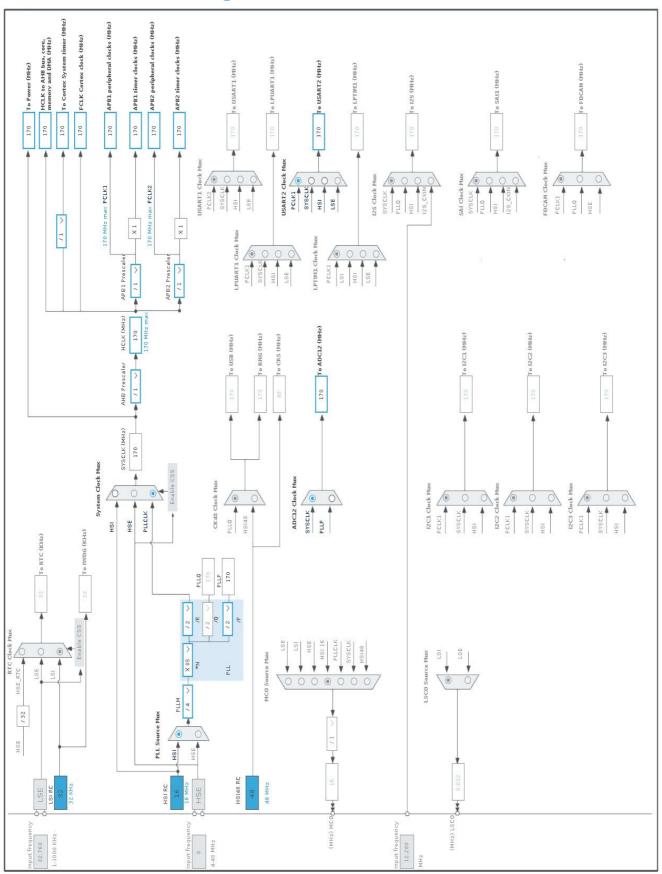


# 3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0-OSC_IN	I/O	ADC1_IN10	
3	PF1-OSC_OUT	I/O	ADC2_IN10	
5	PA0	I/O	ADC1_IN1, COMP3_INP	
6	PA1	I/O	ADC1_IN2	
7	PA2	I/O	USART2_TX	USART2_TX [ST- LINKV3E_VCP_RX]
8	PA3	I/O	USART2_RX	USART2_RX [ST- LINKV3E_VCP_TX]
9	PA4	I/O	ADC2_IN17	
10	PA5	I/O	DAC1_OUT2	
11	PA6	I/O	ADC2_IN3	
12	PA7	I/O	ADC2_IN4	
13	PB0	I/O	ADC1_IN15	
14	VSSA	Power		
15	VDDA	Power		
16	VSS	Power		
17	VDD	Power		
18	PA8	I/O	TIM1_CH1	
19	PA9	I/O	TIM1_CH2	
20	PA10	I/O	TIM2_CH4	
21	PA11	I/O	TIM4_CH1	
22	PA12 *	I/O	GPIO_Output	LED_GREEN
23	PA13	I/O	SYS_JTMS-SWDIO	T_SWDIO
24	PA14	I/O	SYS_JTCK-SWCLK	T_SWCLK
25	PA15	I/O	TIM2_CH1	
28	PB5 *	I/O	GPIO_Output	LED_RED
29	PB6 *	I/O	GPIO_Output	LED_BLUE
30	PB7	I/O	COMP3_OUT	
31	PB8-BOOT0 *	I/O	GPIO_Output	LD2 [green]
32	VSS	Power		

<sup>\*</sup> The pin is affected with an I/O function

# 4. Clock Tree Configuration



Page 4

# 5. Software Project

# 5.1. Project Settings

Name	Value	
Project Name	stm32genscope	
Project Folder	/home/andrei/STM32CubeIDE/workspace_1.14.0/stm32genscope	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_G4 V1.5.0	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

# 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

## 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART2_UART_Init	USART2
5	MX_ADC1_Init	ADC1
6	MX_ADC2_Init	ADC2
7	MX_TIM4_Init	TIM4
8	MX_TIM2_Init	TIM2
9	MX_DAC1_Init	DAC1
10	MX_TIM6_Init	TIM6
11	MX_TIM1_Init	TIM1

Rank	Function Name	Peripheral Instance Name
12 MX_COMP3_Init		COMP3
13	MX_DAC3_Init	DAC3

# 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x1
мси	STM32G431KBTx
Datasheet	DS12589_Rev0

## 1.2. Parameter Selection

Temperature	25
Vdd	3.0

## 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

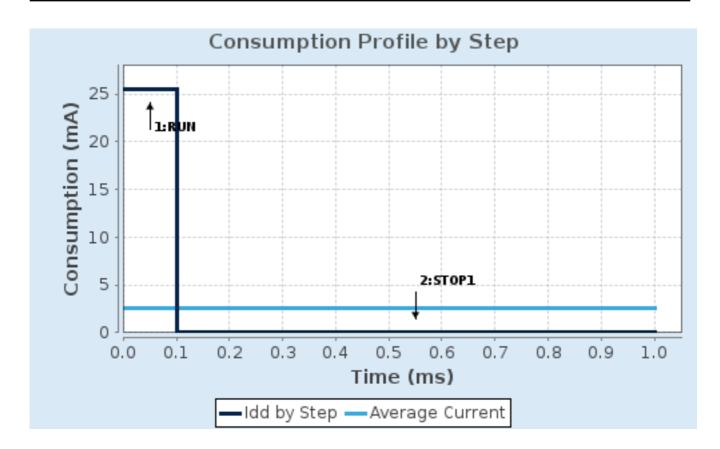
# 1.4. Sequence

C4am	Ct 4	Ct 0
Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	25.5 mA	59 µA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	124.19	129.99
Category	In DS Table	In DS Table

## 1.5. Results

Sequence Time	1 ms	Average Current	2.6 mA
Battery Life	1 month, 23 days,	Average DMIPS	212.5 DMIPS
	22 hours		

# 1.6. Chart



# 2. Peripherals and Middlewares Configuration

2.1. ADC1

IN1: IN1 Single-ended IN2: IN2 Single-ended

mode: IN10 mode: IN15

2.1.1. Parameter Settings:

#### ADCs\_Common\_Settings:

Mode Dual regular simultaneous mode only \*

DMA Access Mode DMA access mode enabled

Delay between 2 sampling phases 1 Cycle

ADC\_Settings:

Clock Prescaler Asynchronous clock mode divided by 8 \*

Resolution ADC 12-bit resolution
Data Alignment Right alignment

Gain Compensation 0

Scan Conversion Mode Enabled

End Of Conversion Selection End of sequence of conversion \*

Low Power Auto Wait Disabled

Continuous Conversion Mode Enabled \*

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

Overrun behaviour Overrun data preserved

ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 4 \*

External Trigger Conversion Source Timer 1 Trigger Out event 2 \*

External Trigger Conversion Edge Trigger detection on the falling edge \*

Rank

Channel 1

Sampling Time 640.5 Cycles \*

Offset Number No offset
Rank 2 \*

Channel 10 \*
Sampling Time 640.5 Cycles \*

Offset Number No offset

<u>Rank</u> 3 \*

Channel 15 \*
Sampling Time 640.5 Cycles \*

Offset Number No offset Rank 4 \*

Channel 2 \*

Sampling Time 640.5 Cycles \*

Offset Number No offset

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

**Analog Watchdog 1:** 

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:** 

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:** 

Enable Analog WatchDog3 Mode false

2.2. ADC2

IN3: IN3 Single-ended

mode: IN4 mode: IN10

**mode: IN17 Single-ended** 2.2.1. Parameter Settings:

ADCs\_Common\_Settings:

Mode Dual regular simultaneous mode only \*

DMA Access Mode DMA access mode enabled

Delay between 2 sampling phases 1 Cycle

ADC\_Settings:

Clock Prescaler Asynchronous clock mode divided by 8 \*

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Gain Compensation 0
Scan Conversion Mode Enabled

End Of Conversion Selection End of sequence of conversion \*

Low Power Auto Wait Disabled
Continuous Conversion Mode Enabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

Overrun behaviour Overrun data preserved

ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 4 \*
Rank 1

Channel 3

Sampling Time 640.5 Cycles \*

Offset Number No offset Rank 2 \*

Channel 4 \*
Sampling Time Channel 4 \*
640.5 Cycles \*

Offset Number No offset
Rank 3 \*

Channel 17 \*
Sampling Time Channel 17 \*
640.5 Cycles \*

Offset Number No offset Rank 4 \*

Channel 10 \*
Sampling Time Channel 10 \*

Offset Number No offset

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

**Analog Watchdog 1:** 

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:** 

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:** 

Enable Analog WatchDog3 Mode false

2.3. COMP3

mode: Input [+]

Input [-]: DAC3 OUT1 mode: ExternalOutput

## 2.3.1. Parameter Settings:

**Basic Parameters:** 

Trigger Mode Rising Edge Event \*

Hysteresis Level **Level 70mV** \*

**Output Configuration:** 

Blanking Source None

Output Polarity COMP output on GPIO is inverted \*

#### 2.4. DAC1

### OUT2 mode: Connected to external pin and to on chip-peripherals

### 2.4.1. Parameter Settings:

#### **DAC Out2 Settings:**

Mode selected Normal Mode
Output Buffer Enable

DAC High Frequency Mode Automatic

DMA Double Data Disable
Signed Format Disable

Trigger Out event \*

Trigger2 None
Wave generation mode Disabled

User Trimming Factory trimming

#### 2.5. DAC3

mode: OUT1 mode

### 2.5.1. Parameter Settings:

#### **DAC Out1 Settings:**

Mode selected Normal Mode
Output Buffer Disable

DAC High Frequency Mode Automatic

DMA Double Data Disable
Signed Format Disable
Trigger None
Trigger2 None

User Trimming Factory trimming

#### 2.6. RCC

### 2.6.1. Parameter Settings:

**System Parameters:** 

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 4 WS (5 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 64
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

**Power Parameters:** 

Power Regulator Voltage Scale 1 boost

**Peripherals Clock Configuration:** 

Generate the peripherals clock configuration TRUE

2.7. SYS

**Debug: Serial Wire** 

**Timebase Source: SysTick** 

mode: save power of non-active UCPD - deactive Dead Battery pull-up

2.8. TIM1

Slave Mode: Trigger Mode Trigger Source: TI1FP1

Clock Source: Internal Clock
Channel2: PWM Generation CH2

mode: One Pulse Mode2.8.1. Parameter Settings:

**Counter Settings:** 

Prescaler (PSC - 16 bits value) 170-1 \*

Counter Mode Up

Dithering Disable

Counter Period (AutoReload Register - 16 bits value ) 20000 \*

Internal Clock Division (CKD)

No Division

Repetition Counter (RCR - 16 bits value) 0
auto-reload preload Disable
Slave Mode Controller Trigger Mode

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

Trigger Event Selection TRGO2 Output Compare (OC2REF) \*

#### **Break And Dead Time management - BRK Configuration:**

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

**BRK Sources Configuration** 

Digital Input
COMP1
Disable
COMP2
Disable
COMP3
Disable
COMP4
Disable

#### **Break And Dead Time management - BRK2 Configuration:**

BRK2 State Disable
BRK2 Polarity High
BRK2 Filter (4 bits value) 0

**BRK2 Sources Configuration** 

- Digital Input
- COMP1
- COMP2
- COMP3
- COMP4
Disable
Disable
Disable

#### **Break And Dead Time management - Output Configuration:**

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

**Clear Input:** 

Clear Input Source Disable

Trigger:

Trigger Polarity Rising Edge

Trigger Filter (4 bits value) 0

**PWM Generation Channel 2:** 

Mode PWM mode 1

Pulse (16 bits value)

Output compare preload

Fast Mode

CH Polarity

CH Idle State

10000 \*

Enable

Disable

Low \*

Reset

#### 2.9. TIM2

Slave Mode: Trigger Mode Trigger Source: TI1FP1

Clock Source : Internal Clock
Channel4: PWM Generation CH4

mode: One Pulse Mode 2.9.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0

Counter Mode Down \*

Dithering Disable

Counter Period (AutoReload Register - 32 bits value ) 170000 \*

Internal Clock Division (CKD) No Division
auto-reload preload Disable

Slave Mode Controller Trigger Mode

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO

Output Compare (OC4REF) \*

#### **Clear Input:**

Clear Input Source Disable

#### Trigger:

Trigger Polarity Rising Edge

Trigger Filter (4 bits value) 0

#### **PWM Generation Channel 4:**

Mode PWM mode 1
Pulse (32 bits value) 17000 \*
Output compare preload Enable
Fast Mode Disable
CH Polarity Low \*

#### 2.10. TIM4

Clock Source: Internal Clock
Channel1: PWM Generation CH1

### 2.10.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 1700-1 \*

Counter Mode Down \*

Dithering Disable

Counter Period (AutoReload Register - 16 bits value) 14000 \*

Internal Clock Division (CKD) No Division auto-reload preload Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Update Event \*

**Clear Input:** 

Clear Input Source Disable

**PWM Generation Channel 1:** 

Mode PWM mode 1

Pulse (16 bits value) 500 \*

Output compare preload Enable
Fast Mode Disable
CH Polarity High

#### 2.11. TIM6

mode: Activated

#### 2.11.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 170-1 \*

Counter Mode Up
Dithering Disable
Counter Period (AutoReload Register - 16 bits value ) 10 \*
auto-reload preload Disable

#### **Trigger Output (TRGO) Parameters:**

Trigger Event Selection

**Update Event \*** 

#### 2.12. USART2

### **Mode: Asynchronous**

### 2.12.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 9600 \*

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

#### **Advanced Parameters:**

Data Direction Receive and Transmit

Over Sampling 8 Samples \*

Single Sample Disable
ClockPrescaler 1

Fifo Mode Enable \*

Txfifo Threshold 3 quarts full configuration \*

Rxfifo Threshold 3 quarts full configuration \*

#### **Advanced Features:**

Disable Auto Baudrate TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable Data Inversion Disable TX and RX Pins Swapping Overrun Enable DMA on RX Error Enable MSB First Disable

#### \* User modified value

# 3. System Configuration

# 3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PF0-OSC_IN	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PA0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PF1- OSC_OUT	ADC2_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC2_IN17	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC2_IN4	Analog mode	No pull-up and no pull-down	n/a	
COMP3	PA0	COMP3_INP	Analog mode	No pull-up and no pull-down	n/a	
	PB7	COMP3_OUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	
DAC1	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	T_SWDIO
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	T_SWCLK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA10	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PA11	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART2_TX [ST- LINKV3E_VCP_RX]
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART2_RX [ST- LINKV3E_VCP_TX]
GPIO	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_BLUE
	РВ8-ВООТО	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green]

### 3.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
DAC1_CH2	DMA1_Channel2	Memory To Peripheral	Low

### ADC1: DMA1\_Channel1 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Word \*
Memory Data Width: Word \*

### DAC1\_CH2: DMA1\_Channel2 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Word \*
Memory Data Width: Word \*

# 3.3. NVIC configuration

# 3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
DMA1 channel1 global interrupt	true	4	0	
DMA1 channel2 global interrupt	true	4	0	
TIM1 update interrupt and TIM16 global interrupt	true	0	0	
TIM1 capture compare interrupt	true	0	0	
TIM2 global interrupt	true	0	0	
TIM4 global interrupt	true	5	0	
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	true	1	0	
TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts	true	0	0	
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused			
Flash global interrupt	unused			
RCC global interrupt		unused		
ADC1 and ADC2 global interrupt	unused			
TIM1 break interrupt and TIM15 global interrupt				
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused			
COMP1, COMP2 and COMP3 interrupts through EXTI lines 21, 22 and 29	unused			
FPU global interrupt	unused			

# 3.3.2. NVIC Code generation

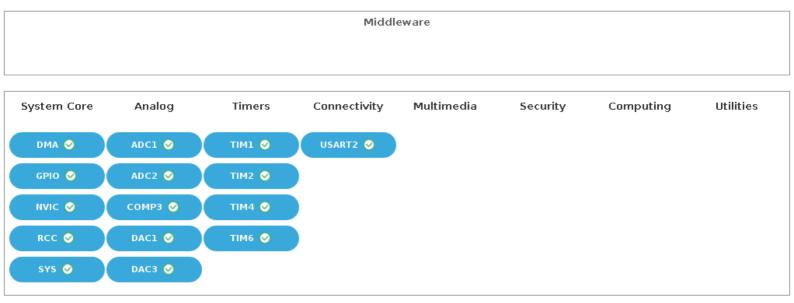
Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
TIM1 update interrupt and TIM16 global interrupt	false	true	true
TIM1 capture compare interrupt	false	true	true
TIM2 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
USART2 global interrupt / USART2 wake- up interrupt through EXTI line 26	false	true	true
TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts	false	true	true

<sup>\*</sup> User modified value

# 4. System Views

- 4.1. Category view
- 4.1.1. Current



# 5. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl\_model/stm32g4\_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis\_model/stm32g4\_ibis.zip

System View https://www.st.com/resource/en/svd/stm32g4\_svd.zip

Description

Presentations https://www.st.com/resource/en/product\_presentation/microcontrollers\_st

m32g4\_series\_product\_overview.pdf

Presentations https://www.st.com/resource/en/product\_presentation/stm32-

stm8\_embedded\_software\_solutions.pdf

Presentations https://www.st.com/resource/en/product\_presentation/stm32\_eval-

tools\_portfolio.pdf

Presentations https://www.st.com/resource/en/product\_presentation/stm32\_stm8\_functi

onal-safety-packages.pdf

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solutions-presentation.pdf

Presentations https://www.st.com/resource/en/product\_presentation/stm32-

stm8\_software\_development\_tools.pdf

Presentations https://www.st.com/resource/en/product\_presentation/microcontrollers-

stm32-family-overview.pdf

Brochures https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-

and-smart-i-os.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32g4.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32nucleo.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32trust.pdf

Flyers https://www.st.com/resource/en/flyer/fldpstpfc11120.pdf

Application Notes https://www.st.com/resource/en/application\_note/an1181-electrostatic-

discharge-sensitivity-measurement-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application\_note/an1709-emc-design-

guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application\_note/an2606-stm32-

- microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4232-getting-started-with-analog-comparators-for-stm32f3-series-and-stm32g4-series-devices-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4277-using-stm32-device-pwm-shutdown-features-for-motor-control-and-digital-power-conversion-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4296-use-stm32f3stm32g4-ccm-sram-with-iar-embedded-workbench-keil-mdkarm-stmicroelectronics-stm32cubeide-and-other-gnubased-toolchains-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4635-minimization-of-

- power-consumption-using-lpuart-for-stm32-microcontrollersstmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
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