AION Verilog Testbench

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Scope

This document describes the tools and steps needed to simulate the local testbenches of the design. Due to the large memory requirements of Equihash (210,9), simulating with such a large memory pool is not feasible so the local testbenches have been designed for quick verification on a subset of tests.

Equihash Example Block

Description of the block. Inputs, outputs and functionality.
Test descriptions.

Tools

Icarus Verilog

http://iverilog.icarus.com/

The opensource simulator allows for easy and quick simulation of verilog code. Please follow the installation guide (http://iverilog.wikia.com/wiki/Installation_Guide) which supports building from scratch or prebuilt binaries (Linux, Windows etc).

Make

http://gnuwin32.sourceforge.net/packages/make.htm

In order setup the build files properly and include all the necessary files, Make was used to keep things simple.

GTKWave

http://gtkwave.sourceforge.net/

This is an opensource waveform viewer which can be used across platforms. As part of the Icarus Verilog install, an older version of GTKWave will be installed but can be upgraded to suit the users need.

Build

By typing *make* in the $ROOT/src/build folder, Icarus Verilog *iverilog* will be called and all available test benches will be built. The output generated are {TESTBENCH}.sim files which can be used for simulation.

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Simulate

Once build has successfully completed, we can now call on the *vvp* {TESTBENCH}.sim to simulate the design. The output generated is a {TESTBENCH}.vcd

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Waveform Viewing

Once simulation has completed, one can call on *gtkwave* {TESTBENCH}.vcd to open up a waveform of the simulation.

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