Luke McNeil
Milestone 1 Work

1) Wednesday, September 30, 2020

[10 min]
Talked with team through chat and decided to do a stack architecture.

2) Saturday, October 3, 2020

[2 hours]
Wrote a first draft of the GCD and RELPRIME functions
This included making up instructions as I went along. I used instructions presented in Sid's lecture on the stack architecture, as well as borrowing ideas for stack manipulation from Forth.

3) Sunday, October 4, 2020

[1 hour]
Spent some time trying to figure out what actually uses a stack architecture in the real world, and get a better idea of how it is implemented in hardware. Did some googling and wikipedia reading. Watched youtube videos on Forth and Java Bytecode.

4) Monday, October 5, 2020

[2 hours]
Met with team to discuss various requirements for M1.
These include coming up with what additional registers we would need (none). We designed the format types O and A. After the meeting and having talked to Sid for some advice I decided that we could have two stacks of registers. One is the main stack which is for computations, and the other is a return address stack. This way nested functions can always remember where they should return to. This also allowed me to describe the function calling conventions. I wrote a code fragment where main calls f1 which calls f2 which calls f3 showing these conventions in use.

5) Tuesday, October 6, 2020

[1 hour]
I converted my RELPRIME and GCD to the table format that is in the design doc. I then refined the descriptions of our format types. I then listed out all of our instructions so far in a table providing their format type, argument if any, and a description. I also then created a table explaining how to convert O types to machine code which is pretty easy.

[1.5 hours]
Met as a group discussed how to convert all instructions to machine code. Figured out the addressing modes we are going to use. I wrote some additional code fragments explaining simple addition and getting input.

This is what we decided on was our plan for Milestone 2
M2 task assignment:

a) 1st meeting: break instructions into small steps and move data from one register to another, determine single-cycle or multi-cycle
b) Luke & Austin: RTL Description of each instruction\
c) Jinhao & Yiju : A list of generic components specifications needed for RTL
d) 2nd meeting: debug and test the processor through Xilinx ISE and fix

Woah, already?

existed problems