Name? Title?

Milestone 1

Monday, Oct 5, 2020: 2 hours
Writing design document and figuring out processor specifics: stack-based, addressing, registers

Tuesday, Oct 6, 2020: 2 hours
Writing sample programs in assembly
Converting said assembly to machine code

M2 task assignment:
1st meeting: break instructions into small steps and move data from one register to another, determine single-cycle or multi-cycle
Luke & Austin: RTL Description of each instruction
Jinhao & Yiju: A list of generic components specifications needed for RTL

Milestone 2

2nd meeting: debug and test the processor through Xilinx ISE and fix existed problems

Wednesday, Oct 14, 2020: 1.5 hours
Reviewing Luke's RTL descriptions
Creating Executive Summary

M3 task assignment: Create design diagram
Begin Xilinx work
Begin Xilinx testing

Milestone 3

Sunday, Oct 18, 2020: 2.5 hours
Verifying RTL
Created initial datapath design

Tuesday, Oct 20, 2020: 1.5 hours
Created ALU with unique operations

you need to elaborate — what did you do, what decisions did you make, what did you learn?

Created ALU testing program

Wednesday, Oct 21, 2020: 2 hours
Came up with integration plan
Refine datapath, unit specification

M4 task assignment:
Things for Milestone 4

- Continue implementing necessary components and adding unit tests
  - Jinhao - sign-extender
  - Austin - adder
  - Jinhao - left-shifter
  - Luke - register
  - Someone - memory blocks
- Start on integration testing plans
  - Group Meetings (might split out individual work later)
- Implement Control
  - Luke

Milestone 4